POWER AMPLIFIER IMPROVEMENT TECHNIQUES/CIRCUITS IN 0.35 MICRON SiGe HBT TECHNOLOGY FOR 5 GHz WIRELESS LAN BAND

by

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Abstract

In this thesis, a 5 GHz radio frequency power amplifier for IEEE 802.11a WLAN applications is designed, the ideas of on-chip power combining and using transmission lines as an RF on-chip choke are tested and layouts are drawn. The power amplifier employs SiGe HBT's in AMS 0.35 μm BiCMOS process and it is designed to operate in Class A mode with a supply voltage of 3 Volts. Since the power amplifier is the final block and the final amplification stage of the transmitter chain in a wireless system, it must produce enough RF power to overcome the channel losses. At the same time, the power produced by the power amplifier should obey the power levels dictated by the operating standard. Therefore, in this work much consideration is given to design a power amplifier which provides enough output power for IEEE 802.11a WLAN standard. The power amplifier is designed to operate in Class A, and the bias points are chosen accordingly in order to preserve linearity. After the design of a single stage power amplifier, different versions of the circuit are designed and layouts are drawn. To decrease the dye area and the parasitic losses, the inductor which is used as the RF choke is replaced with capacitively loaded transmission lines. Moreover, in order to improve the linearity and obtain higher output power levels, two single stage power amplifiers are combined via on-chip Wilkinson power combiner made of lumped elements. Simulations are performed in ADS and Cadence environments in a parallel fashion.

0.35 MİKRON SiGe HBT TEKNOLOJİSİ İLE, 5 GHz KABLOSUZ İLETİŞİM BANDINDA GUÇ AMFİSİ GELİŞTİRME TEKNİKLERİ VE DEVRELERİ

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Özet

Bu tezde, 802.11a WLAN uygulamaları için yüksek frekans bir güç kuvvetlendiricisi AMS'in 0.35 μm SiGe BiCMOS teknolojisiyle 5 GHz frekansinda tasarlanmış ve serimi yapılmıştır. Bunun yaninda, tümleşik güç birleştirici yöntemi ve iletim hattını tümleşik endüktans olarak kullanma fikri test edilmiştir. Bu güç kuvvetlendiricisi tasarımında AMS'in 0.35 μm BiCMOS prosesinde bulunan SiGe HBT'ler yer alıp, kuvvetlendirici 3 Volt kaynak voltajı ile Sınıf A'da çalışacak şekilde tasarlanmıştır. Güç kuvvetlendiricisi, gönderici hattındaki son yükseltici blok olduğu için, kanal kayıplarını aşabilmek için yeterli miktarda yüksek frekans çıkış gücü oluşturabilmelidir. Aynı zamanda, üretilen çıkış gücü, çalıştırma standardının öngördüğü çıkış gücü seviyelerini aşmamalıdır. Bu sebepten dolayı, bu çalışmada IEEE 802.11a standardı için yeterli seviyelerde güç üretebilen bir kuvvetlendirici tasarlamaya özen gösterilmiştir. Sınıf A'da çalıştırılmak üzere tasarlanan güç kuvvetlendiricisinin kutuplama noktalari bu doğrultuda seçilmiş ve doğrusallık korunmuştur. Tek sıralı güç kuvvetlendiricisi tasarlandıktan sonra, aynı devrenin değişik versiyonları tasarlanıp test edilmiştir. Kırmık boyutunu küçültmek ve parazitik kayıpları azaltmak için, RF choke görevi gören endüktans devreden çıkartılıp yerine kapasitif yüklenmiş iletim hattı yerleştirilmiştir. Doğrusallığı ve çıkış gücünü arttırmak içinse, iki tek sıralı güç kuvvetlendiricisi tümleşik Wilkinson güç birleştiricisi ile birleştirilmiştir. Simülasyonlar ADS ve Cadence ortamlarında eş zamanlı olarak yapılmıştır.

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LIST OF ABBREVIATIONS

ADS	Advanced Design System
AMS	Austria Micro Systems
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BPSK	Binary Phase Shift Keying
CPW	Coplanar Waveguide
FFT	Fast Fourier Transform
HBT	Heterojunction Bipolar Transistor
GI	Guard Interval
IC	Integrated Circuit
I&Q	Inphase and Quadrature
IEEE	Institute of Electrical and Electronics Engineers
IFFT	Inverse Fast Fourier Transform
LO	Local Oscillator
LOS	Line of Sight
NLOS	Non Line of Sight
OFDM	Orthogonal Frequency Division Multiplexing
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
SiGe	Silicon Germanium
UNII	Unlicensed National Information Infrastructure
WLAN	Wireless Local Area Network

Chapter 1

1 INTRODUCTION

The wireless local area network market has been growing rapidly for the past several years. The IEEE 802.11 WLAN standards have extended the frequency band from 2.4 GHz to 5 GHz bands in order to increase the data transmission rate. The new generation of 802.11a WLAN and HiperLAN/2 standards operating in the 5 GHz spectrum using OFDM are becoming popular due to high speed, greater system capacity and low interference [1]. Each of these standards requires a power amplifier as the final amplification block of the transmitter and each of them allow a specific maximum output power generated by the power amplifier.

IEEE 802.11a has different maximum output power levels depending on whether the transmission occurs in the lower (5.15 GHz-5.35 GHz) or the upper band (5.725 GHz-5.825 GHz). Typically, the required output power level for the IEEE 802.11a standard in 5.15-5.25 GHz, 5.25-5.35 GHz and 5.725-5.825 GHz bands is 40 mW, 200mW and 800 mW respectively [2].

Traditionally, power amplifier circuits at high frequencies have been implemented in III-V compound semiconductor technologies such as GaAs and InP [3]. However, RF Si ICs have recently demonstrated their competitive advantages for WLAN applications. SiGe BiCMOS technology is a silicon based technology that takes advantage of the maturity of silicon processing techniques and results into low cost elements. Recently, SiGe HBT power amplifiers are emerging as a contender for RF power amplifier applications at higher frequencies. However, SiGe devices capable of operating at 5 GHz have a low collector-emitter breakdown voltage, making it difficult to extract high output power from a single transistor [3]. Therefore, the solution to the difficulty of extracting high output power from a SiGe device operating at 5 GHz could be to use power combining techniques and to decrease losses such as conductor and

dielectric substrate losses. In this thesis, two new ideas are tested and implemented to obtain higher output power. First idea is on-chip power combining using Wilkinson power combiner and the second idea is to decrease substrate losses of low Q-inductors by replacing them with transmission line inductor elements.

This thesis describes the design of a key RF block in the transmitter chain - the Power Amplifier and this work is based on SiGe BiCMOS process of AMS. We address the design of a 5 GHz PA for WLAN 802.11a applications. Our aim is to design a PA which produces enough output power for operating at the lowest frequency band of the IEEE 802.11a standard. This corresponds to 40 mW (16 dBm) output power for the 5.15 GHz-5.25 GHz frequency band. We start from the basic device I-V characteristics and designed the PA input/output matching and bias networks, accordingly. After the design of a single stage Class A PA suitable for IEEE 802.11a applications, the simulation results of the two different topologies deducted from the main PA topology are also performed. First topology to be simulated is the on-chip power combined PA circuit which utilizes a powerful technique to increase the output power and to improve the linearity. This method is tested in order to obtain higher output powers for the upper frequency bands of the IEEE 802.11a standard. Other than the power combined PA circuit, the idea of replacing the low Q inductors with capacitive loaded transmission lines is also simulated and implemented. Layouts for the single stage PA and its new version with RF choke replaced with the transmission lines are also drawn in a die size of 977*981 μm^2 including RF and DC bias pads.

The material in this thesis is organized as follows: In Chapter 2, the general principles and specifications of the IEEE 802.11a WLAN standard are presented. Also in this chapter, transmitter and receiver chains of a 802.11a system are investigated and basic principles of power amplifiers are presented. Role of power amplifier in a transmitter chain, power amplifier design parameters and different classes of power amplifiers are all given in detail in Chapter 2. In Chapter 3, basic design procedure of a 5GHz Class A single stage power amplifier is given in detail. The device I-V characteristics, load pull simulations and input/output matching network design are all presented as part of the PA design roadmap. Chapter 3 also introduces the theoretical background of the two ideas implemented in this thesis; namely on-chip Wilkinson power combining technique and capacitively loaded transmission line equivalent model of low Q inductors. This chapter also includes some ADS simulation results of the implementation of these ideas. In Chapter 4, preliminary numerical results of a more

realistic simulation of three different PA circuits will be presented. First, the simulation results of the single stage power amplifier with AMS components and layout of this topology are presented. Then, the same simulations are performed for the on-chip power combined PA topology which is also implemented with AMS components. Finally the simulation results of the single stage PA design with the transmission line structure used as the RF choke are given along with the layout. At the end of Chapter 4, an analysis of how the technology used in the design affects the characteristics of the capacitively loaded transmission line structure is done. Finally, in Chapter 5 a brief conclusion of this thesis and future work are given.

Chapter 2

2 BACKGROUND

In this chapter, brief background information about the power amplifier basics is given. Chapter 2 starts with the IEEE WLAN 802.11a standard specifications which cover the frequency allocation, output power levels, error vector magnitude values and transmit spectrum masks. Afterwards the architecture of an IEEE WLAN 802.11a transceiver is presented. Both the receiver and the transmitter parts are investigated in detail. Finally different power amplifier classes (linear and nonlinear) are mentioned in the last subsection.

2.1 IEEE WLAN 802.11a Standard Specifications

IEEE 802.11 or Wireless Fidelity (Wi-Fi) denotes a set of Wireless LAN standards developed by working group 11 of IEEE 802. These specifications define an over-the-air interface between a wireless client and a base station; or between two or more wireless clients. The 802.11 family currently includes three separate protocols that focus on encoding (a, b, g); other standards in the family are service enhancement and extensions, or corrections to previous specifications.

IEEE Std. 802.11a is a high speed Wireless Local Area Network (WLAN) standard designated in 1999. This standard operates at radio frequencies between 5 GHz and 6 GHz. As seen in Table 1, there are three frequency bands allocating the 5-6 GHz band for this standard; lower band: 5.15-5.25 GHz, middle band: 5.25-5.35 GHz and the upper band: 5.725-5.825 GHz. Each band has its own maximum output power limit dictated by the IEEE 802.11a standard. As also given in Table 1, three transmit power levels are specified: 40 mW, 200mW and 800mW. The upper band defines transmit

power levels suitable for bridging applications and the lower band specifies transmit power levels suitable for short range indoor home and small office environments. Using the 5 GHz band gives 802.11a the advantage of less interference, since 2.4 GHz band is heavily used. However, this high carrier frequency restricts the use of 802.11a to almost line of sight.

Frequency Band (GHz)	**Maximum output power with up to 6 dBi antenna gain (dBm)**
5.15-5.25	40 (2.5 mW/MHz)
5.25-5.35	200 (12.5 mW/MHz)
5.725-5.825	800 (50 mW/MHz)

Table 2.1: Transmit power levels for the United States

IEEE 802.11a standard has 12 non-overlapping channels, with a channel spacing of 20 MHz, as shown in Figure 2.1. Each channel is an OFDM modulated signal with consisting of 52 subcarriers. The basic principle of OFDM is to split a high data rate data stream into a number of lower rate streams that are transmitted simultaneously over a number of subcarriers. Because the symbol duration increases for the lower rate parallel subcarriers, the relative amount of dispersion in time caused by multipath delay spread is decreased. Intersymbol interference (ISI) is eliminated almost completely because the OFDM allows us to insert adequate guard interval between successive OFDM symbols.

As shown in Figure 2.1, the lower band contains four channels with channel numbers; 36, 40, 44, and 48 with center frequencies; 5180, 5200, 5220, and 5240 MHz respectively. Likewise, the middle band contains channels 52, 56, 60, and 64 with center frequencies; 5260, 5280, 5300, and 5320 MHz respectively. Finally, the upper band contains channels 149, 153, 157, and 161 with center frequencies; 5745, 5765, 5785, and 5805 MHz respectively.

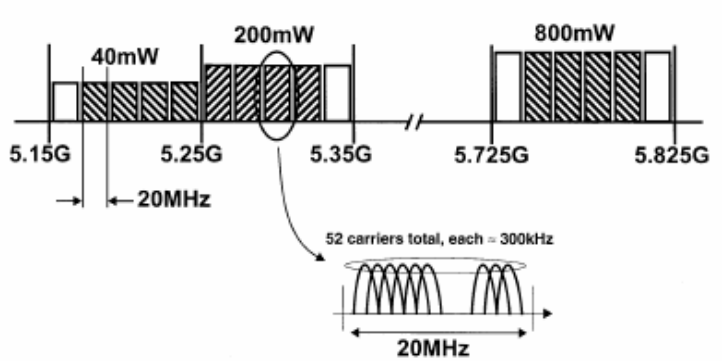


Figure 2.1: OFDM PHY frequency channel plan for the United States

The IEEE 802.11a standard specifies an OFDM physical layer (PHY) that splits an information signal across 52 separate subcarriers to provide transmission of data at a rate of 6, 9, 12, 18, 24, 36, 48, or 54 Mbps. The 6, 12, and 24 Mbps data rates are mandatory in the IEEE 802.11a standard. From the 52 subcarriers, four are the pilot subcarriers that the system uses as a reference to disregard frequency or phase shifts of the signal during transmission. The remaining 48 subcarriers provide separate wireless pathways for sending the information in a parallel fashion. Since there are 64 possible subcarrier frequency slots in a 20 MHz channel in the IEEE 802.11a standard, the resulting subcarrier frequency spacing is 312.5 kHz.

The IEEE 802.11a standard system uses 52 subcarriers that are modulated using BPSK, QPSK, 16 QAM, or 64 QAM, as shown in Table 2. Depending on the data rate chosen, the binary serial signal is divided into groups (symbols) of one, two, four, or six bits and converted into complex numbers representing applicable constellation points. For example, if a data rate of 18 Mbps is chosen, the data bits are mapped to a QPSK constellation.

Data Rate (Mbits/sec)	Modulation
6	BPSK
9	BPSK
12	QPSK
18	QPSK
24	16-QAM
36	16-QAM
48	64-QAM
54	64-QAM

Table 2.2: Modulation types for different data rates

The IEEE 802.11a standard requires receivers to have a minimum sensitivity ranging between -82 dBm (at 6 Mbps data rate) and -65 dBm (at 54 Mbps data rate). The IEEE 802.11a standard also specifies maximum allowable Error Vector Magnitude (EVM) values for each data transmission rate, as shown in Table 3 [2].

Data Transmission Speed (Mbps)	Allowable EVM (dB)
6	-5
9	-8
12	-10
18	-13
24	-16
36	-19
48	-22
54	-25

Table 2.3: Allowed relative constellation error versus data rate

The transmitted spectral density of the transmitted signal should fall within the spectral mask, as shown in Figure 2.2.

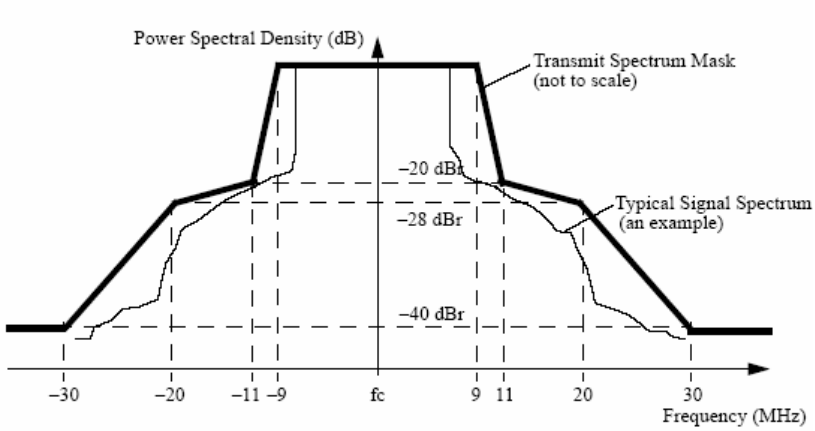


Figure 2.2: Transmit spectrum mask

According to this transmit mask, the transmitted spectrum should have a 0 dBr bandwidth not exceeding 18 MHz, –20 dBr at 11 MHz frequency offset, –28 dBr at 20 MHz frequency offset and –40 dBr at 30 MHz frequency offset and above. The dBr unit is defined as the dB relative to the maximum spectral density of the signal.

2.2 Architecture of an IEEE 802.11a WLAN Transceiver

The spectral efficiency of the 802.11a standard comes at the expense of a more complicated transceiver with strict requirements on the radio performance. For example, the use of 64-QAM modulation requires a signal-to-noise ratio (SNR) of 30 dB, which is substantially greater than that required by the FSK modulation in Bluetooth and the QPSK modulation in 802.11b. This high SNR translates to stringent phase noise requirements for the frequency synthesizer and tight matching constraints for both the transmitter and receiver. OFDM, which is highly desirable because of its resilience to multipath interference, can substantially complicate the transceiver design [4]. Figure 2.3 indicates the block diagram of an IEEE 802.11a transmitter.

As shown in the Figure 2.3, data is first encoded using Forward Error Correction (FEC) encoder and then interleaved and mapped. After that, Inverse Fast Fourier Transform (IFFT) is applied and Guard Interval (GI) is added. After the symbol shaping is done, data is Inphase and Quadrature (I&Q) modulated and the then mixer is used to upconvert the signal to a specific frequency value with the help of the local oscillator

(LO). Finally the power amplifier is the last stage in the transmitter chain just before the antenna and it is used to increase the power level of the signal to be transmitted.

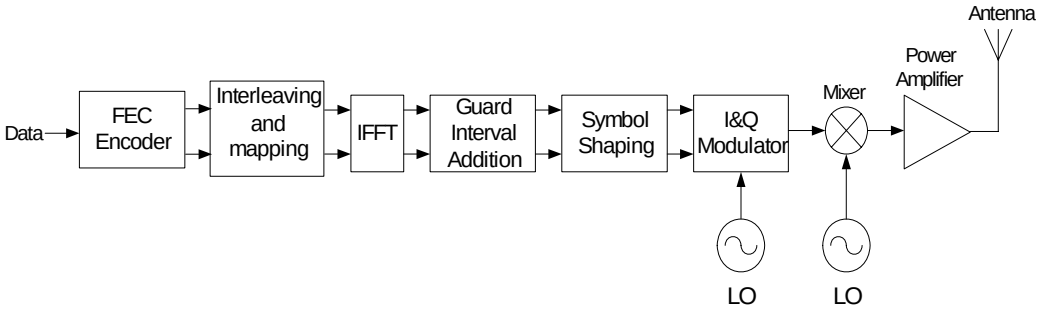


Figure 2.3: Block diagram of an IEEE 802.11a transmitter

Figure 2.4 indicates the block diagram of an IEEE 802.11a receiver. The receiver topology looks like the reverse of the transmitter. First block is the Low Noise Amplifier (LNA) after the signal is captured with an antenna. The mixer follows the LNA to downconvert the signal. The mixer output is fed into an Automatic Gain Control Amplifier. Then I&Q demodulation takes place. Automatic Frequency Control Recovery is utilized after this block in order to achieve a flawless demodulation and after that GI is removed and Fast Fourier Transform (FFT) is applied. After demapping and deinterleaving stage, FEC decoder decodes the original data.

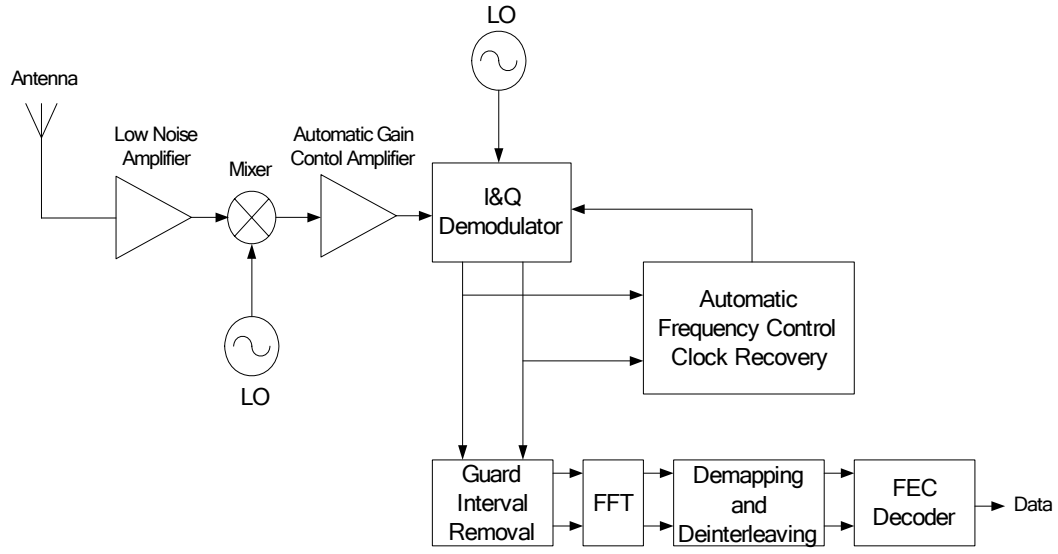


Figure 2.4: Block diagram of an IEEE 802.11a receiver

2.3 Power Amplifier Background

2.3.1 Introduction

In any wireless communication system there is a transmitter part and in any transmitter one of the most challenging components is the Power Amplifier. Power Amplifier is the last amplification stage in the transmitter chain and it is a key part of the RF front end in any transmitter, as shown in Figure 2.5.

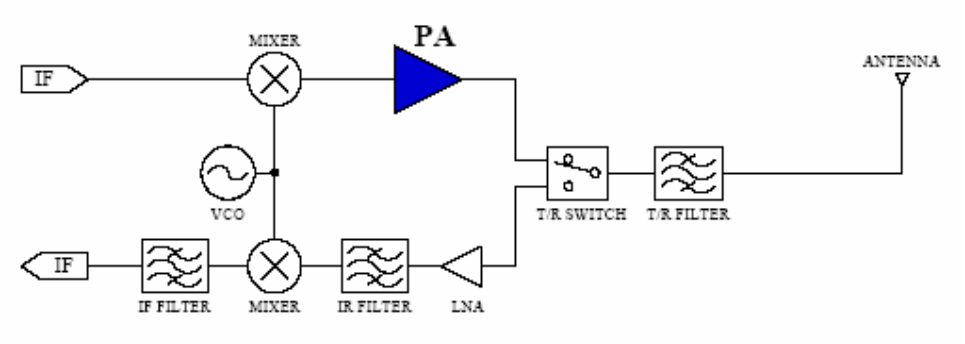


Figure 2.5: Block diagram of an RF transceiver

Power amplifier (PA) takes the signal to be transmitted and amplifies it to a proper level such that the transmitted signal overcomes the channel losses and receiver senses adequate power to recover the desired signal. That specific power level is determined by the communication system and for different applications the order of magnitude of the transmitted power varies. For example, while the transmitted power level is on the order of thousands of watts for satellite communications, this level drops to tens to hundreds of milliwatts for portable wireless communication devices. Even the generated output power levels differ greatly; the underlying principles of the power amplifier design are much the same.

Because the power that should be sent to the transmitting antenna is often quite high, PA is the largest power consumer in most wireless communication systems. A major design requirement of a PA is how efficiently the PA converts the DC power into RF output power.

A power amplifier usually consists of an active device, which is a transistor, input and output matching networks and some extra circuitry, like the bias network. Figure 2.6 shows the basic topology of a basic power amplifier.

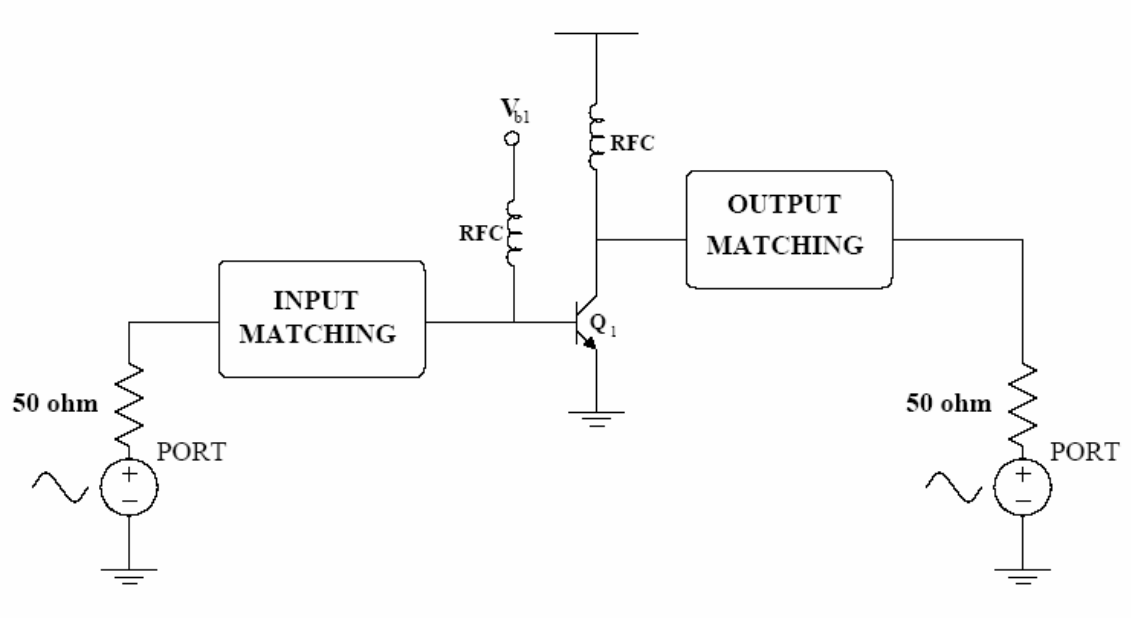


Figure 2.6: Basic topology of a power amplifier

According to the target application of the PA; transistor type, class of operation and the matching circuit topologies are determined.

2.3.2 Power Amplifier Performance Parameters

Some of the important terms and specifications of a PA are as follows:

Frequency of Operation

The PA should be designed for a specific range of frequency in a narrowband application. Each communication standard specifies its own frequency range of operation and for this thesis the PA is designed at 5 GHz frequency and all of its parameters are simulated at 5 GHz. That is compatible with IEEE 802.11a WLAN standard which occupies the 5 GHz frequency band.

Output Power

Output power is the amount of power that needs to be delivered to the transmitting antenna. As mentioned earlier, the output power levels of 802.11a transmitters are specified by the IEEE 802.11a standard. With upto 6 dBi antenna gain,

for the lower frequency band (5.15 GHz-5.25 GHz) the output power level should not exceed 40 mW; for the middle frequency band (5.25 GHz-5.35 GHz) the maximum output power level is 200 mW and for the upper frequency band (5.725 GHz- 5.825 GHz) this level is specified as 800 mW.

When considering power output, a common unit used is dBm, which is the output power in dB referenced to 1 mW. The output power in dB is given by

$$P_{dBm} = 10\log\frac{P}{0.001W} \tag{2.1}$$

where P is defined in Watts. In dB scale, the specified maximum output power levels for IEEE 802.11a standard are 16 dBm, 23 dBm and 29 dBm for the lower, middle and upper frequency bands respectively.

Power Gain

PAs provide a certain level of power gain in order to boost the incoming signal to required levels. Power gain is defined as the ratio of the output power delivered to the load to the input power available from the source. It is desired that the power gain be flat over the frequency band, with a tolerance of ± 0.5 dB.

Efficiency

The measure of how much power a PA consumes while converting the DC power into RF power delivered to the load is a key performance parameter of a PA. This parameter is known as the PA's efficiency. Efficiency is most basically defined as the ratio of the "power delivered to the load" to the "power drawn from the source". The maximum efficiency is 1, or 100% since the PA is converting the DC supply power into RF power delivered to the load. This happens if there is no power consumed in the PA, which is only ideally possible.

There are variations of this metric that give more information about the PA. The most common efficiency metric used is the Power Added Efficiency (PAE). PAE is defined as

$$PAE = \frac{P_{RF_{OUT}} - P_{RF_{IN}}}{P_{DC}} \tag{2.2}$$

It is important to note that there is a tradeoff between efficiency and linearity. That is why nonlinear power amplifiers offer much higher efficiencies compared to their linear counterparts.

Linearity

Input output relation of a PA must be linear in order to preserve signal integrity. It is desired that the PA operates with high linearity, meaning that the output power be linear with the input power. As the input power level increases, device gets closer to saturation point and eventually reaches the saturation point. This introduces harmonics in the output power spectrum. In order to measure linearity of a PA, 1 dB compression point and third order intercept points are used.

1 dB compression point can be defined both as input referred and output referred. For example, input referred 1 dB compression point is defined as the input power at which the linear gain of the amplifier is compressed by 1 dB [7]. The output referred 1 dB compression point is the sum of the input referred 1 dB compression point and the gain of the amplifier. Figure 2.7 shows a plot of the 1 dB compression point characteristics.

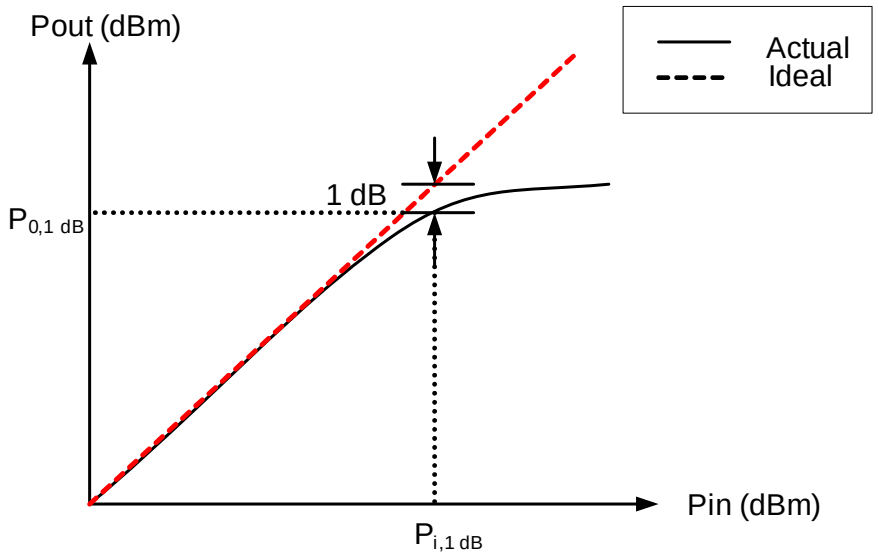


Figure 2.7: 1 dB compression characteristics

Third order intercept point is another useful metric for measuring linearity. When there are interferers very close to the fundamental frequency, the nonlinear behavior of the PA generates inter-modulation products. Third order intermodulation (IM3) product is the most important of the products, because it falls directly into the frequency band of interest as indicated in Figure 2.8.

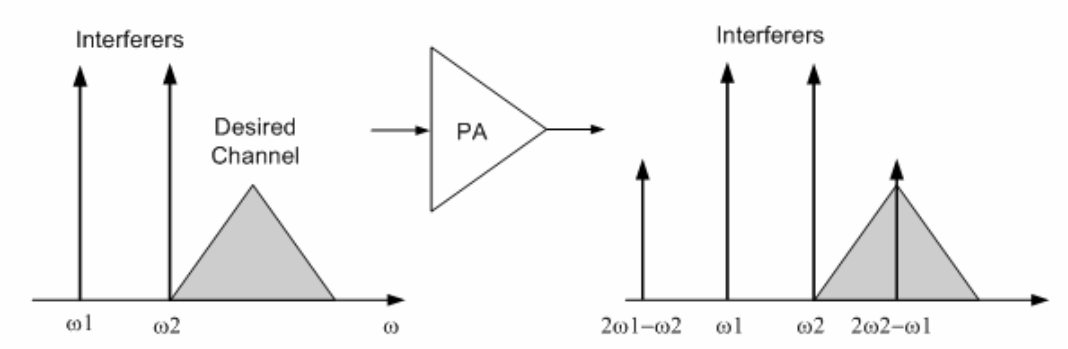


Figure 2.8: Corruption of the desired signal due to nearby interferers

The amplitude of the IM3 product term increases in the order of cube of the fundamental amplitude. The third order intercept point is the extrapolated intersection of this IM3 product term and the fundamental power, as shown in Figure 2.9.

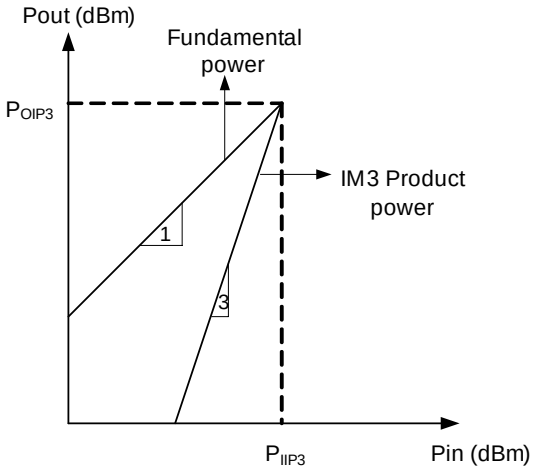


Figure 2.9: Third Order Intercept Point

In general, modulation schemes can be separated into two basic categories: constant envelope and non-constant envelope. In the constant envelope modulation schemes, there is no symbol information contained in the transmitted signal amplitude, therefore a linear relationship between the input and the output is not required. In the non-constant envelope case, there is symbol information contained in the transmitted signal amplitude. As a result, extremely linear power amplifiers are required for non-constant envelope modulation techniques, while the linearity can be traded for efficiency in constant envelope modulation schemes. There are a variety of well established linearization techniques, such as feedback techniques, predistortion

technique, feedforward technique, etc. The linearization methods will not be covered in this thesis.

Error Vector Magnitude (EVM)

EVM represents the distance between the measured and expected carrier magnitude and phase at some point in time after it has been compensated in timing, amplitude, frequency, phase and DC offset. Figure 2.10 shows the error vector magnitude representation as the phase and magnitude difference between the actual and ideal carriers. For IEEE 802.11a, the error vector between the vector representing the transmitted signal and the vector representing the error-free modulated signal defines modulation accuracy. The magnitude of the error vector is called error vector magnitude (EVM).

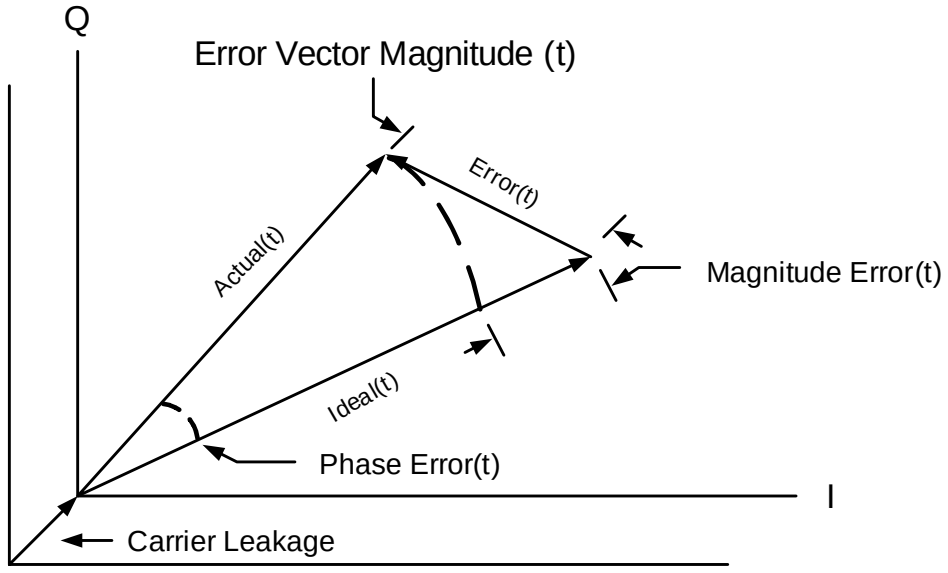


Figure 2.10: Error Vector Magnitude representation

2.3.3 Power Amplifier Classes

Although there are many different classes, in general PAs can be categorized into two groups; linear and non-linear (switching mode) amplifiers. In the former category of PAs, the active device (transistor) acts as a current source, while in the latter category device acts as a switch. Class A, B, AB and C amplifiers fall into linear amplifier category where the output amplitude of the signal is a linear function of the input signal amplitude. For this type of amplifiers the voltage and current waveforms through and across the transistor are full or partial sinusoids. On the other hand, class D, E and F are some of the switching mode PA types. These types of amplifiers can achieve high efficiency levels, but very nonlinear performances.

Brief background information about different classes of PAs will be presented in the next subsections. However, Class A will be emphasized more than other classes.

Linear Power Amplifiers

Linear PA generally refers to a PA which operates at a constant gain and needs to preserve amplitude information. For this type of amplifiers, the active device operates in its amplifying region. The amplifying region is the saturation region for FET devices, while it is the forward active region for bipolar devices.

There are four types of PAs, distinguished primarily by bias conditions that may be termed “linear”; Class A, AB, B, and C. All may be understood by studying the single model given in Figure 2.11. In this figure, R_L is the load into which the output power is delivered. The inductor named, RFC is used as an RF choke to feed DC power to the collector. Likewise, C_b is a DC blocking capacitance, which is used to prevent any DC dissipation in the load. The LC network is used as an output matching network [5].

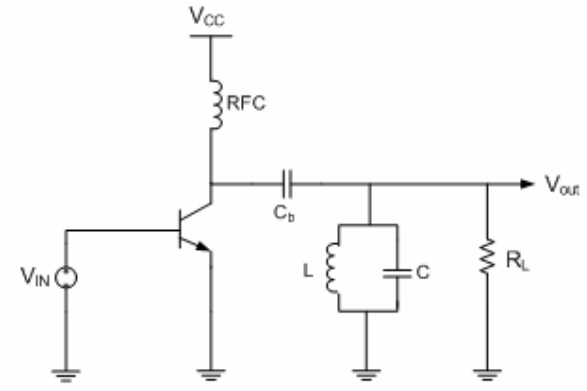


Figure 2.11: General linear power amplifier model

The design of linear PAs depends on the load line theory. This theory states that the maximum power that can be supplied by a transistor to a load is determined by the supply voltage and the maximum current passing through the transistor. As shown in Figure 2.12, load line is defined as the line drawn between the two specific points on the transistor I-V curve. These points are the knee point where the maximum collector current (I_{max}) during AC operation is obtained and the I_c=0, $V_{CE,max}$ point, where the maximum allowed V_{CE} value is located. Load line technique is used to find the optimal bias point for different classes of linear PAs, i.e. for each class, a different optimal bias point should be chosen on the load line.

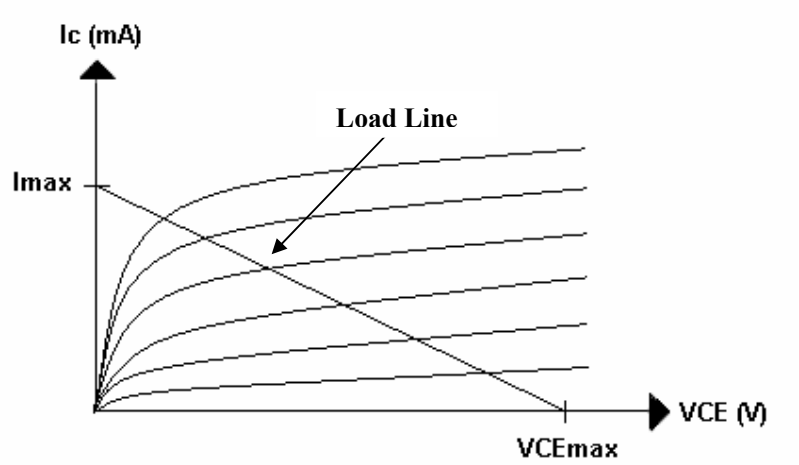


Figure 2.12: I-V characteristics of a transistor

To utilize the maximum current and voltage swing of the transistor, an optimum load resistance value, R_{opt}, would need to be selected, and simply this resistance is the ratio:

$$R_{opt} = \frac{V_{DC}}{\left(\frac{I_{\max}}{2}\right)} = \frac{2V_{DC}}{I_{\max}} \tag{2.3}$$

This equation is derived from the fact that the current swings over its maximum linear range (zero to Imax), that is with an amplitude of $I_{max}/2$ and the voltage swings over its maximum linear range of zero to $2V_{DC}$ [6].

This means that power amplifiers can deliver maximum power to a load given by $R_{opt.}$ Since the transmitting antenna is acting as a 50 Ω load, this R_{opt} resistance is then transformed to 50 Ω by a matching network.

The most linear PAs are those in which the active device is always conducting current. This type is known as Class A power amplifiers. To design a Class A PA, it is

important to make sure that the active device conducts current for the entire input sinusoid cycle. The input bias voltage is set such that the device remains in its amplification region all the time. As mentioned earlier, the class of operation is determined by the operating point on the load line which is obtained from the I-V characteristics of the transistor. For a Class A operation, the transistor should be biased at the center of the load line to maximize the output voltage and current swings as shown in Figure 2.13. This shows that the transistor is in the active region at all times.

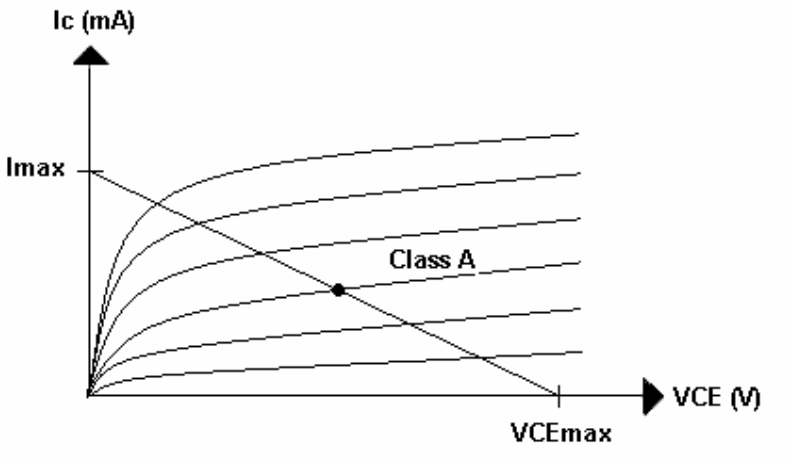


Figure 2.13: Class A Optimal Bias Point

Conduction angle, α, is defined as the time for which the transistor is conducting. For Class A operation, since the transistor is conducting all the time, the conduction angle is 2π.

The linearity of Class A PAs is perfect as the input and output waveforms are preserved without any distortion but the maximum efficiency of a Class A PA is only 50%. However, an efficiency of about only 30% can be attained from a fully Class A PA implementation. This is mainly because, in real life, it is usually not possible to get a peak voltage swing as the active device leaves its amplification region and enters the resistive (this corresponds to saturation region for bipolar devices and linear region for FET devices) region.

For Class B operation, amplifier is biased at the threshold voltage of the transistor, such that the device is shut off half of every cycle. Because the transistor is conducting only half of every cycle, the conduction angle is π. The most practical of Class B amplifiers are push-pull configurations of two transistors. The peak current and maximum output voltage for Class B amplifier are same as for the Class A amplifier,

but the theoretical efficiency is about 78% for Class B amplifies. In practice, efficiency drops to 50% or less. However, linearity is worsened in these types of amplifiers. In conclusion, distortion is accepted in exchange for a significant improvement in linearity with the Class B amplifier.

Class AB amplifier, as its name suggests conducts somewhere between 50% (as Class B amplifiers) and 100% (as Class A amplifiers) of a cycle, depending on the bias level chosen. Accordingly, its efficiency and linearity are intermediate between those of a Class A and Class B amplifier. The conduction angle for Class AB amplifiers is $\pi<\alpha<2\pi$.

Class C amplifiers are biased in such a way that the transistor conducts less than half the time. Consequently, the conduction angle is $\alpha< \pi$. Class C amplifiers offer efficiencies approaching 100%, but both power-handling capability and power gain approach zero at the same time. This class of amplifiers sacrifices linear operation to improve the efficiency. Also, it is actually difficult to design and construct Class C amplifiers with bipolar devices.

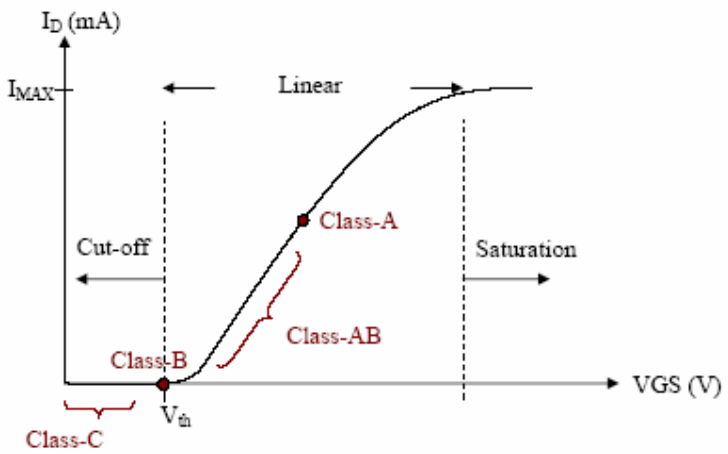


Figure 2.14: Q point of Class A, AB, B and C PAs

In sum, Class A, AB, B and C PAs fall into the linear PA category. Each class is biased at a different quiescent point as shown in Figure 2.15. For the Class A operation, the transistor should be biased at the center of the load line, while for the Class B operation transistor is biased at the threshold voltage, V_{th}. As the name suggested, for the Class AB operation, transistor should be biased between the Class A and Class B bias points. The corresponding conduction angles for each linear type PA is given in Figure 2.15.

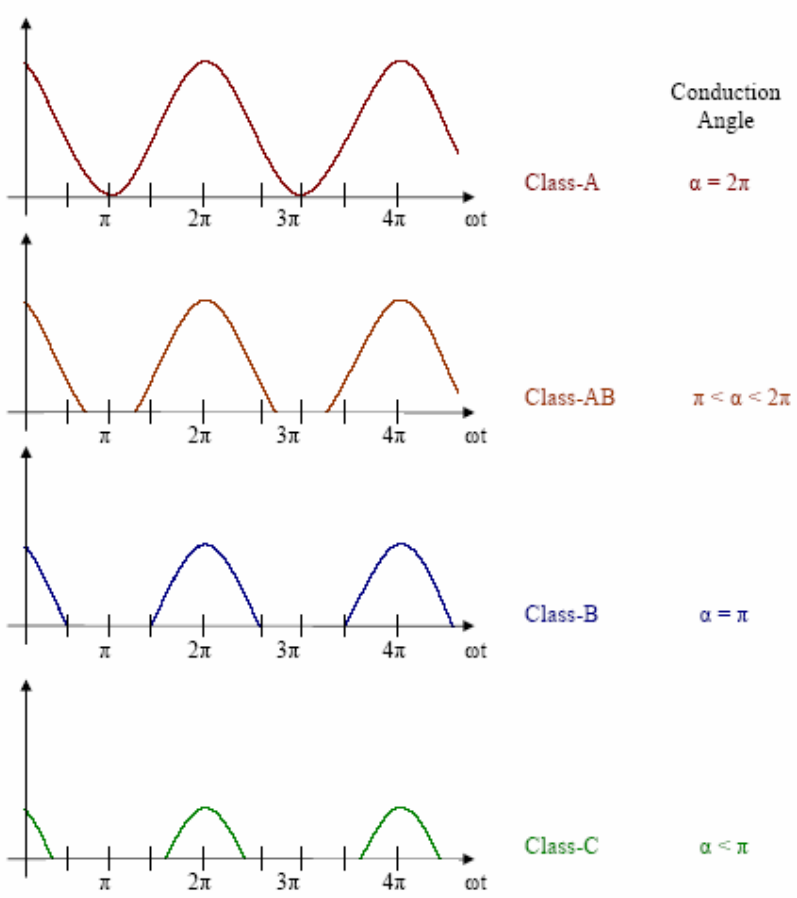


Figure 2.15: Summary of Class A, AB, B and C conduction angles

Figure 2.16 summarizes the maximum theoretical efficiency as a function of conduction angle for different kinds of linear power amplifiers. As seen from this figure, maximum theoretical efficiency (100%) can be achieved with the Class C operation where the conduction angle varies between zero to π. Class B operation can reach theoretical efficiencies up to 78.5%, where the conduction angle is between π. Class A operation is the least efficient of all, where the maximum theoretical efficiency that can be reached is only 50% with a conduction angle of 2π. Class AB mode has efficiency and conduction angle values between those of Class A and Class B modes. Theoretically, any efficiency value can be reached between 78.5% and 100% for Class AB operation.

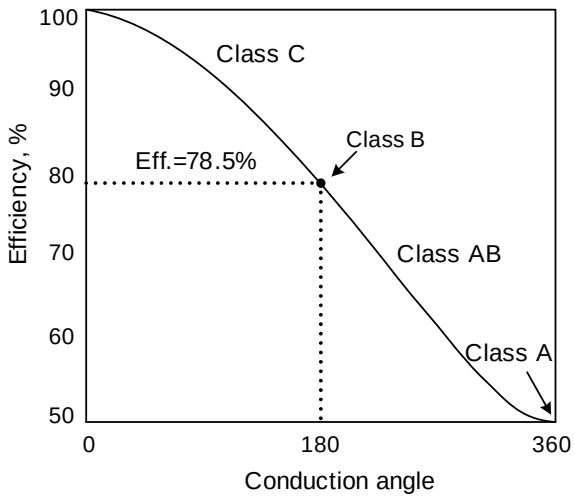


Figure 2.16: Maximum theoretical efficiency of an ideal amplifier as a function of conduction angle

Non-Linear (Switching mode) Power Amplifiers

Switching mode amplifiers are used in applications where efficiency is the primary concern. They are driven with a large amplitude signal which turns the device ON or OFF, as a switch. There are various kinds of switching mode amplifiers, but Class D, E and F are the most common configurations. For high efficiency RF applications, Class D and Class E configurations have received the most attention.

Among several classes of switching mode PAs, the Class E configuration is the most suitable for RF operation. Figure 2.17 shows a Class E PA topology. The RFC provides a DC path to the supply and approximates an open circuit at RF. Under ideal conditions, the voltage of the switch transistor drops to zero and has zero slope just as the transistor turns on and conducts current. This ensures that neither voltage nor current exists simultaneously in the circuit [7]. Therefore, the theoretical peak efficiency of the Class E PA is 100%.

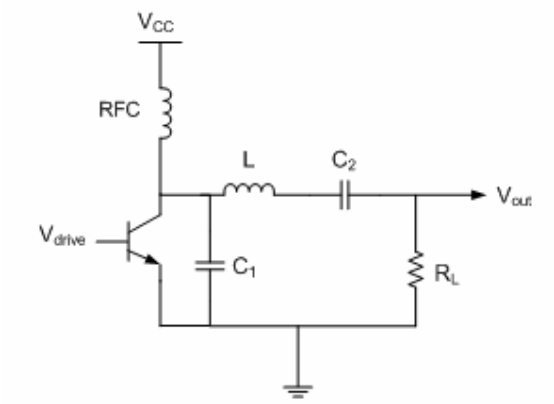


Figure 2.17: Class E amplifier

Class-F amplifiers employ harmonic resonators at the output to shape the drain waveforms. Figure 2.18 shows the Class F topology.

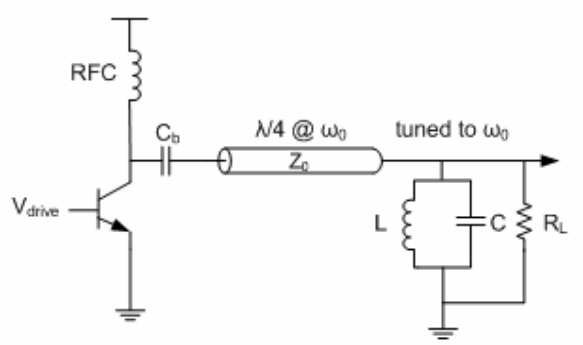


Figure 2.18: Class F amplifier

The harmonic traps are designed in such a way that the voltage waveform resembles a square wave and the current wave resembles a half sine wave. Both the voltage and current waveforms do not exist simultaneously, thus achieving good efficiency. With higher harmonics, the efficiency can be improved up to 100%, but linearity is severely worsened.

Chapter 3

3 PA DESIGN METHODOLOGY

In this chapter, basic design procedure of a 5GHz Class A power amplifier is given in detail. This chapter starts with a basic design roadmap to be followed during a PA design. Then in the consequent subsections; the device I-V characteristics, load pull simulations and input/output matching network design are presented. Our main contribution in this thesis is to increase the output power and improve the linearity performance by using on-chip power combining technique and also to decrease conductor/substrate losses by replacing the low Q inductors by their transmission line equivalents. Therefore, the theory of Wilkinson Power Combiner and Transmission line equivalent model of low Q inductors, along with their simulation results in ADS environment are also presented in the last two subsections of this chapter.

3.1 Design Roadmap

The design starts with determining the requirements and device selection. As a rough approximation, device I-V curves are plotted and to support the current; number and size of the transistors are decided. In this PA design our main requirement is to obtain 40 mW output power to obey the 802.11a standard power specifications for the lowest frequency band. Power amplification in RF frequencies can be accomplished by using any one of many different devices; BJT, MOSFET, GaAs MESFET, HBT, etc. In this thesis, the PA is designed in AMS 0.35μm SiGe BiCMOS HBT technology and high voltage npn Bipolar transistors available in this process are used as the active device. The transistors are symbolized as npn <2><5><4>h5 HBT and the numbers refer to the number of collector, base and emitter contacts, respectively. Active

components are usually limited to 2 or 3 transistors in signal path, therefore in order to obtain enough output power (40 mW), 3 of these high voltage transistors are paralleled. Moreover, in order to maximize the output power, transistor sizes are also set to the maximum limit specified by the process, which corresponds to an emitter length of 96μm.

Figure 3.1 presents the design steps to be followed after the technology is chosen.

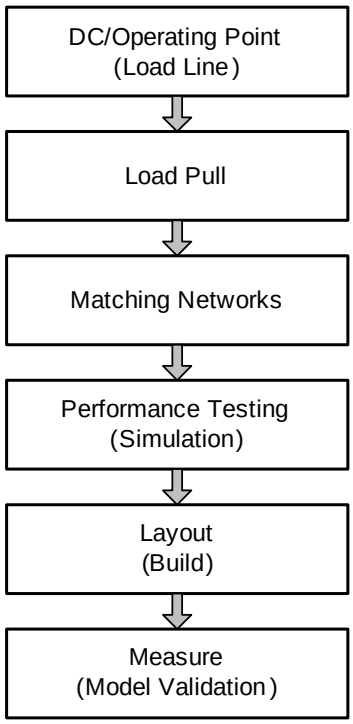


Figure 3.1: PA design roadmap

As seen in Figure 3.1, the first step in the design roadmap is to obtain device I-V curves which are used to determine the optimum bias points for the certain class of operation. After the DC operating points are determined from the device I-V curves, the next step will be to determine the optimum output impedance for maximum power. Load pull simulations are essential in terms of determining the optimum load impedance at the transistor array output, because load pull data gives a simple target area on the Smith Chart to base the strategy for suitable matching network design. Therefore, the optimum load impedance is determined from load pull simulations and then an output matching network is designed to transform 50 Ω load to the optimum load impedance at the transistor output. The following step is to design the input

matching network for gain (complex conjugate) match. Then the overall performance of the PA design is tested via simulation tools; ADS and Cadence. Finally, the circuit layout is drawn and post layout simulations are performed and performances are compared.

3.2 Device I-V curves

After the technology is selected, the first step in designing a PA is to determine the I-V characteristics of the active device.

As mentioned earlier, AMS's high voltage npn Bipolar transistors are used with their emitter length set to the allowed maximum level, which is 96 μm. Three transistors are connected in parallel in order to increase the total emitter length and transistor sizes are maximized in order to deliver required output power. The BJT curve tracer shown in Figure 3.2 generates transistor I-V curves by sweeping base current (IBB) and collector-emitter voltage (VCE).

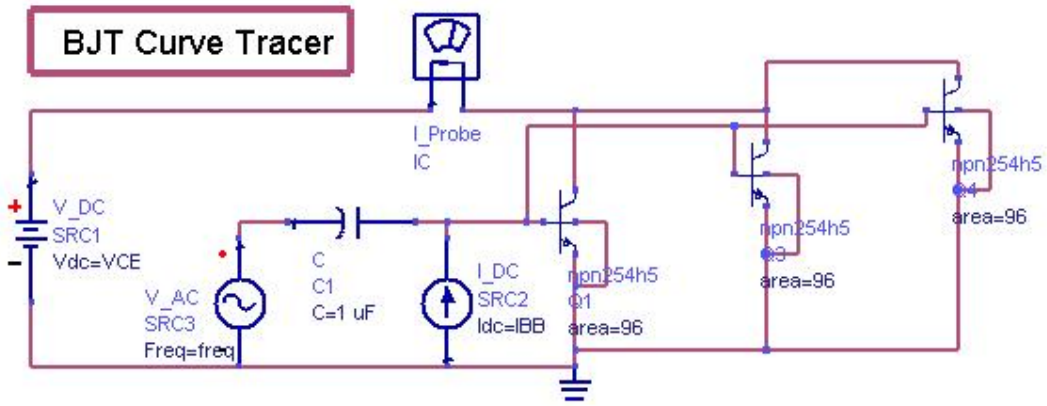


Figure 3.2: This circuit generates I-V curves and computes optimal bias for Class A operation

I-V curves of three bipolar transistors are given in Figure 3.3, where VCE-IC curves are generated for different IBB values. The maximum collector current during AC operation is set by moving marker m2 to the knee of the I-V curve as shown in Figure 3.3. Then the maximum allowed VCE, VCE_{max} is specified as 5.1V. After that, load line is drawn between marker m2 and the (IC=0, VCE=VCE_{max}) points. The

optimal bias point values are determined from this load line. Load line method is a useful priori design method to use as a starting point for the design process.

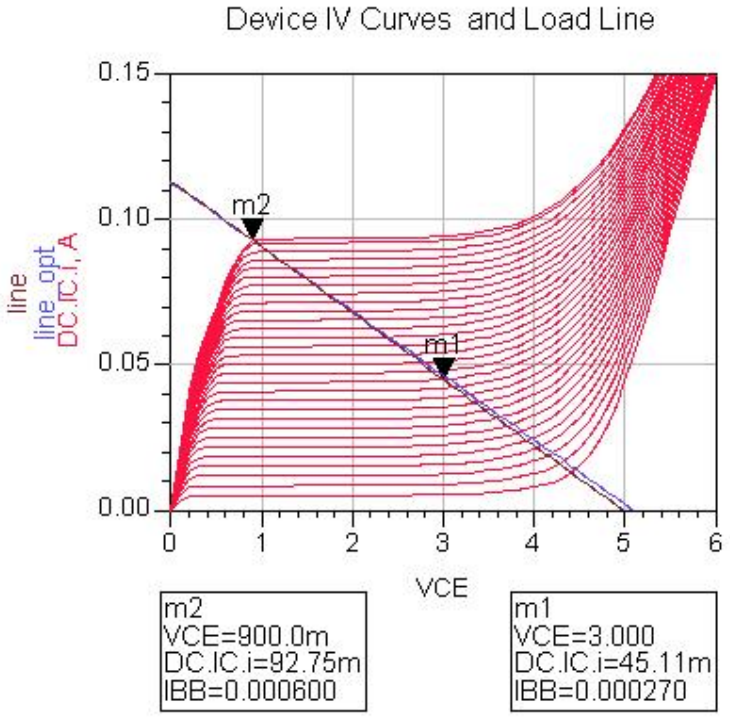


Figure 3.3: Transistor I-V curves

For Class A operation, the center of the load line should be chosen as the bias point. Therefore, marker 1 (m1) is set to the center of the load line. As seen in Figure 3.3, the optimal VCE is 3V and IBB is 270 µA for the Class A operation. At this biasing point (m1), transistor's DC current gain (beta) is about 167, as seen in Figure 3.4.

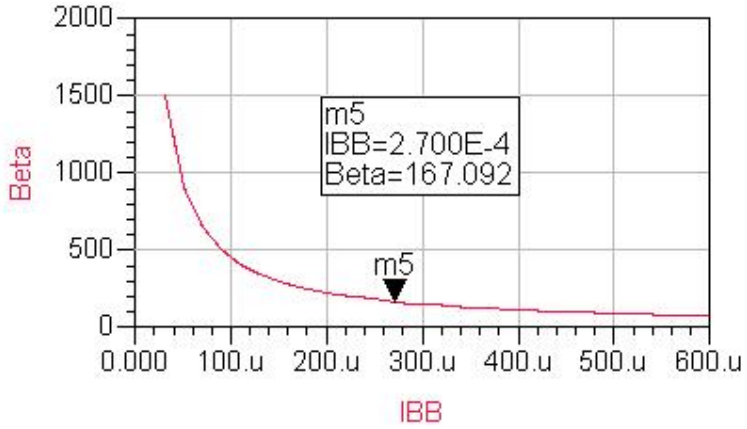


Figure 3.4: Beta versus IBB at ICE which is specified by the marker m1

ADS also generates the optimal Class A bias point values as a result of device I-V curves. As given in Table 3.1, optimal VCE is 3V and optimal ICE is 46.38 mA. Table 3.2 shows the output power and efficiency levels that can be reached at the bias point, m1. In case the transistors are loaded with the Rload value given in Table 3.2, and other bias conditions are satisfied, an efficiency of 35% and an output power of 16.76 dBm can be obtained. These are preliminary results based on linear approximations.

Output Power at Optimal Bias (dBm)	16.87
Rload at Optimal Bias (ohm)	45.282
DC to RF Efficiency (%)	35
Optimal VCE (V)	3
Optimal ICE (mA)	46.38
DC Power Consumption (mW)	139.1

Table 3.1: Optimal bias point values for Class A operation

Output power (dBm)	16.76
Rload (ohm)	44.082
DC to RF Efficiency (%)	35
DC Power Consumption (mW)	135.3

Table 3.2: Marker m1 bias point values, assuming Class A operation and AC current limited to marker m2 value and AC voltage no higher than $VCE_{max} = 5.1V$

In the next subsection, transistors are biased at point m1 by applying a 3V DC bias voltage to the collector and by ensuring that the bias current is 270 μA.

3.3 Load Pull

Load pull is varying or pulling the load impedance seen by a device under test (DUT) and measuring the performance of the DUT. This technique is important for nonlinear devices where the operating point may change with power level. In our case, we performed load pull analyzes by varying the load impedance of a power amplifier in order to obtain the optimal load impedance for maximum output power.

After the bias conditions are satisfied, load pull simulations are performed in order to obtain more realistic load impedance values for maximum power transfer. The load pull setup shown in Figure 3.5 performs one tone load pull simulations. As a result, the output power and PAE are found at each fundamental frequency.

In the Figure 3.5, the capacitors connected to the base and the collector are for DC blocking and they have a capacitance of 30 pF. The inductor at the collector is an RF choke with an inductance of 5 nH, which is used to feed DC power to the collector. The resistor connected to the base is for biasing purposes and finally the output is terminated with variable load impedance. RF choke has a comparatively large inductance in order to act as an open circuit at high frequencies (by showing high impedance at RF), thus isolates RF signals from DC signals. The impedance of the RF choke used in this design can be calculated from a basic equation:

$$Z_L = wL \text{, where } w = 2 * \pi * f \tag{3.1}$$

Since the operating frequency is 5GHz, the impedance of the RF choke at 5 GHz is:

$$Z_L = wL = (2 * \pi * 5 * 10^9) * (5 * 10^{-9}) = 157\Omega \tag{3.2}$$

On the other hand, DC blocking capacitors act as short circuit at high frequencies and as open circuit at DC. This is possible by showing very low impedance at RF. At 5 GHz, the impedance of the DC blocking capacitors used in this design (30 pF) is calculated as follows:

$$Z_C = \frac{1}{wC} \tag{3.3}$$

$$Z_C = \frac{1}{wC} = \frac{1}{(2 * \pi * 5 * 10^9) * (30 * 10^{-12})} = 1\Omega \tag{3.4}$$

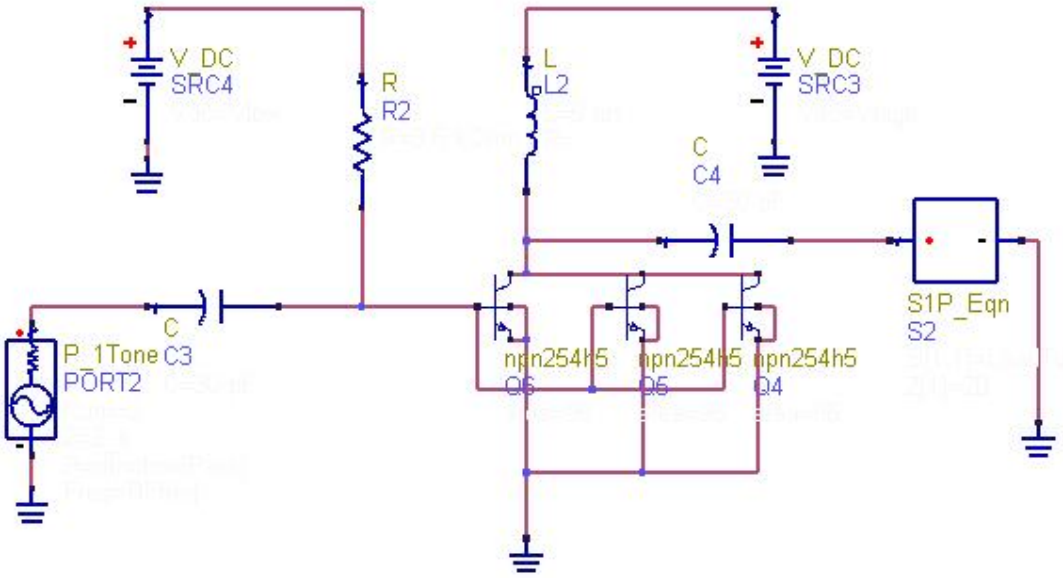


Figure 3.5: Load Pull Setup in ADS

Load pull setup shown in Figure 3.5 generates power and efficiency circle at each load impedance and this results in concentric circles on the Smith Chart. Figure 3.6 shows the maximum PAE (33.93%) and output power (17.51 dBm) that can be obtained from this circuit. The target area on the Smith Chart for obtaining maximum power added efficiency and maximum output power can also be determined from the same figure.

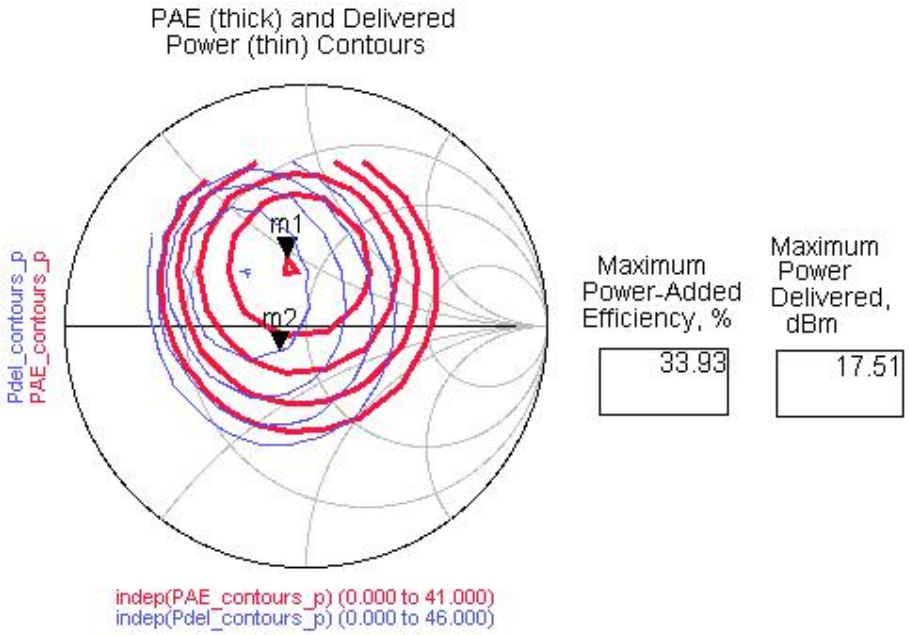


Figure 3.6: Maximum PAE and Pout circles on the Smith Chart

According to the target area on the Smith Chart indicated in Figure 3.6, the best point on the Smith Chart should be chosen as the optimum load impedance. As seen in Figure 3.7, each point on the Smith Chart represents different load impedance values and among these points, point m3 is chosen as the optimum load impedance. Impedance at marker m3 is 28.127 + j14.34 and with this load impedance, 32.06% PAE and 17.51 dBm output power could be obtained.

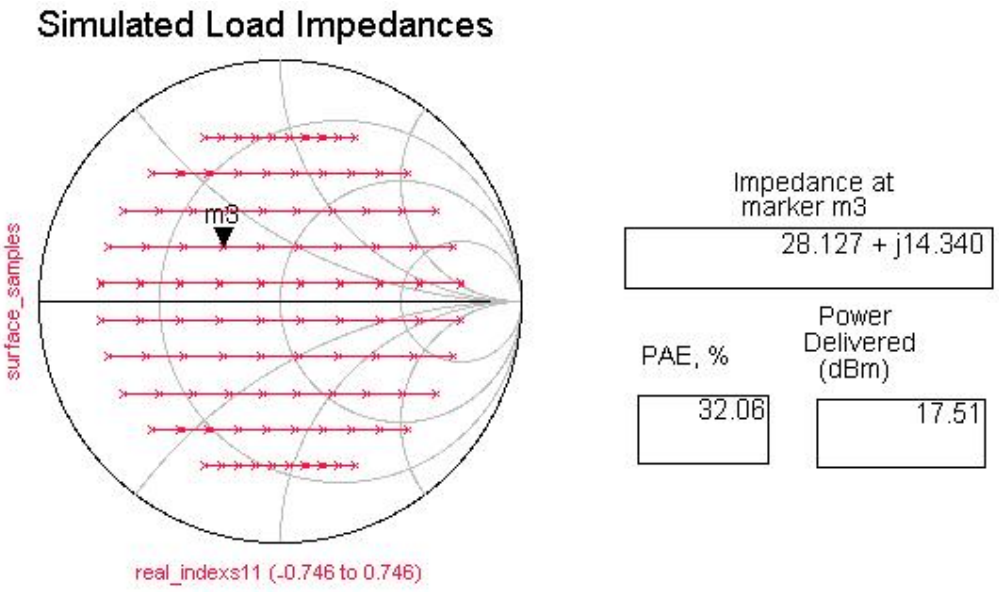


Figure 3.7: Simulated load impedances

3.4 Matching Network Design

In an RF or microwave system, the terminal impedances are all designed to be 50Ω by convention. Thus the antenna is modeled as a 50Ω resistor. Since PA drives the antenna, some conversion must take place between the PA output and the antenna, in order to ensure desired power levels to be obtained at the antenna. This conversion process is accomplished by designing a matching network which converts the optimum load impedance, found from load pull simulations, to 50Ω antenna. The matching network consists of passive, ideally lossless components such as capacitors and inductors. The output and input matching network design will be mentioned in the following subsections.

3.4.1 Output Matching

After the optimum load impedance is determined from the load pull simulations, the next step is to design an output matching network. This network should transform the desired load impedance, which is 28.127 + j14.34 to 50Ω antenna impedance. The best way to design ideally lossless matching networks is to equip LC matching networks. The design of the matching network is done in ADS's Smith Chart Utility as shown in Figure 3.8. During the matching network design; inductive and capacitive losses are taken into account.

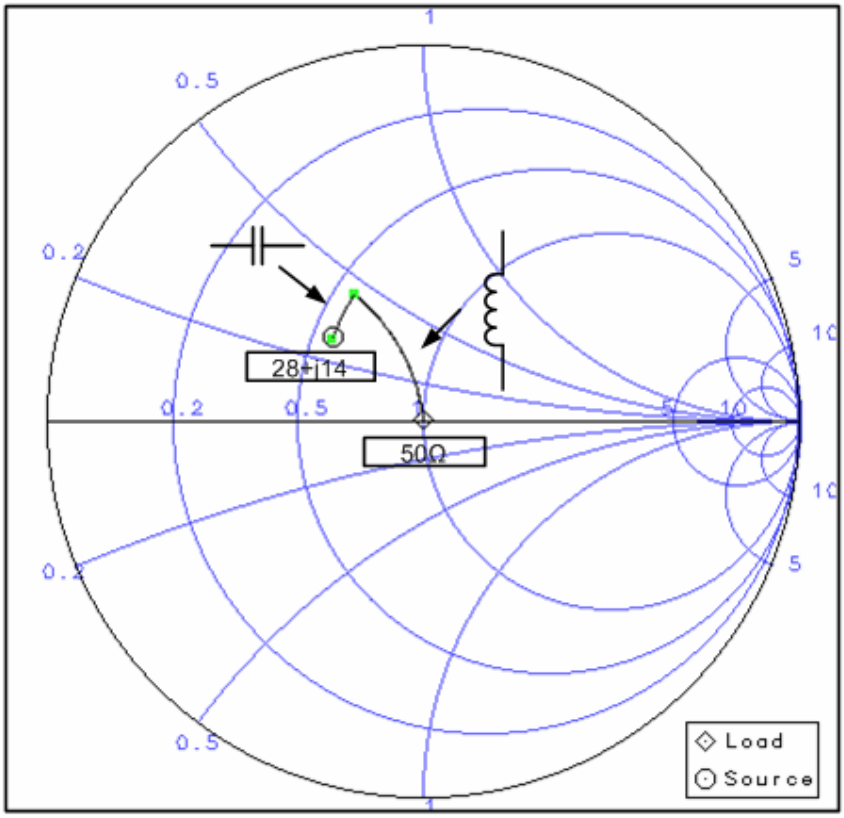


Figure 3.8: Output matching network design using ADS Smith Chart utility

The output matching network which transforms the optimum load impedance, 28.127 + j14.34 to 50Ω is given in Figure 3.9.

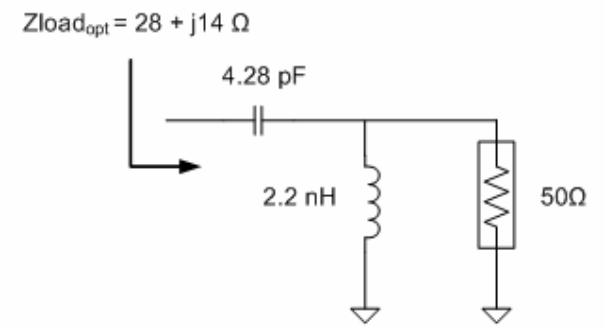


Figure 3.9: Output matching network

3.4.2 Input Matching

Bipolar devices show significant dependency between output power and input load. Therefore, input matching is a crucial part of the PA design. After the desired output load impedance is matched to 50 Ω, such that maximum power is transferred to the antenna, the next step is the design of the input matching network.

Basic design issue is to satisfy the conjugate match principle at the input for maximum power transfer. This principle is to show the conjugate match of s11 to the transistor input in order to obtain a gain match at the output. Accordingly, s11 is 4.4 - j2.8 at 5GHz when the optimum load impedance is shown to the output port. In order to obtain an input match, the complex conjugate of s11, which is 4.4 + j2.8, should be shown to the input. This is very low impedance since the transistors are connected in parallel. As such a large transistor array has very low input impedance, a matching network with a highest possible quality factor is necessary. Since we are using AMS's SiGe process, from AMS's library of thick metal inductors, we seek to use the inductor model with the highest Q at 5GHz. Therefore we choose the inductor model SP011S200T which has an inductance of 1.05 nH and a quality factor of 11.8 at 5GHz.

Again using ADS's Smith Chart Utility, an LC network is designed which matches 50 Ω to 4.4 + j2.8, as shown in Figure 3.10. Figure 3.11 shows this matching circuit, which consists of two capacitors, one in parallel and one in series, and a single inductor connected in series.

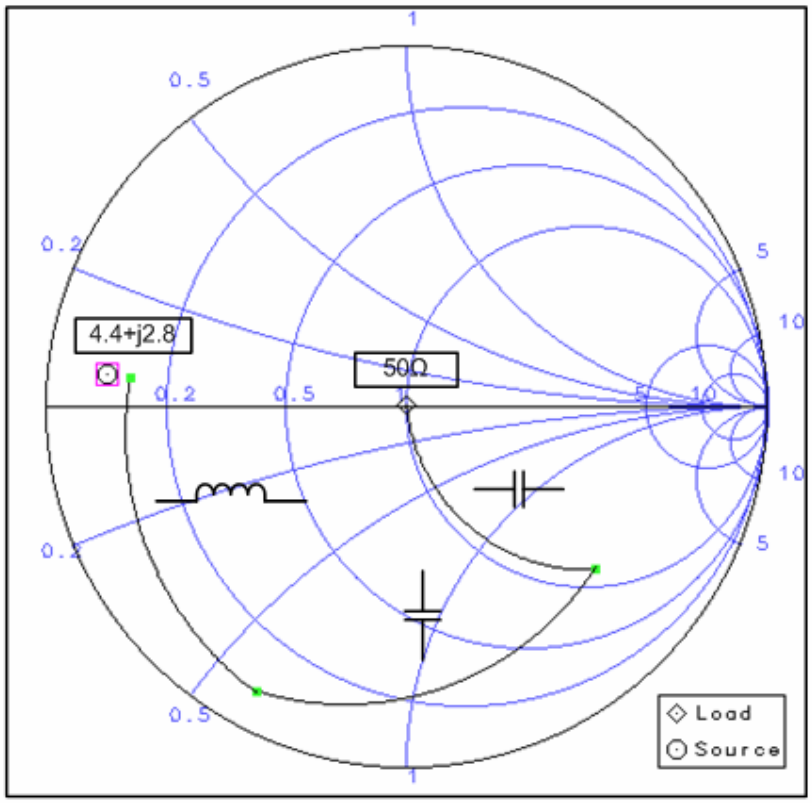


Figure 3.10: Input matching network design using ADS Smith Chart utility

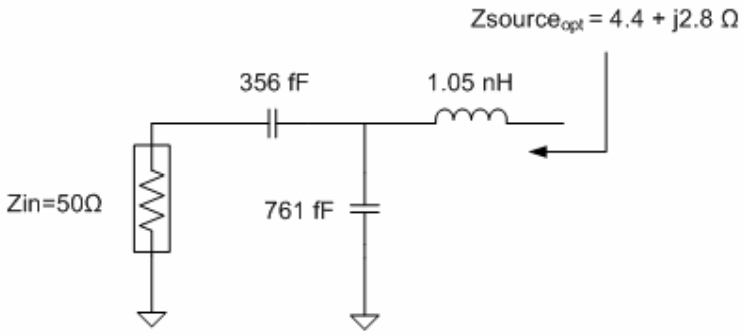


Figure 3.11: Input matching network

3.5 Overall Class A Single Stage PA Schematic

After output and input matching network design, the overall single stage PA circuit which is operated in Class A is shown in Figure 3.12. DC blocking capacitors are integrated into the matching circuitry and the bias conditions are satisfied via the resistor connected to the base and the RFC connected between the collector and the DC

voltage source. All of the components are ideal elements taken from the ADS library and the circuit is designed to operate at 5GHz.

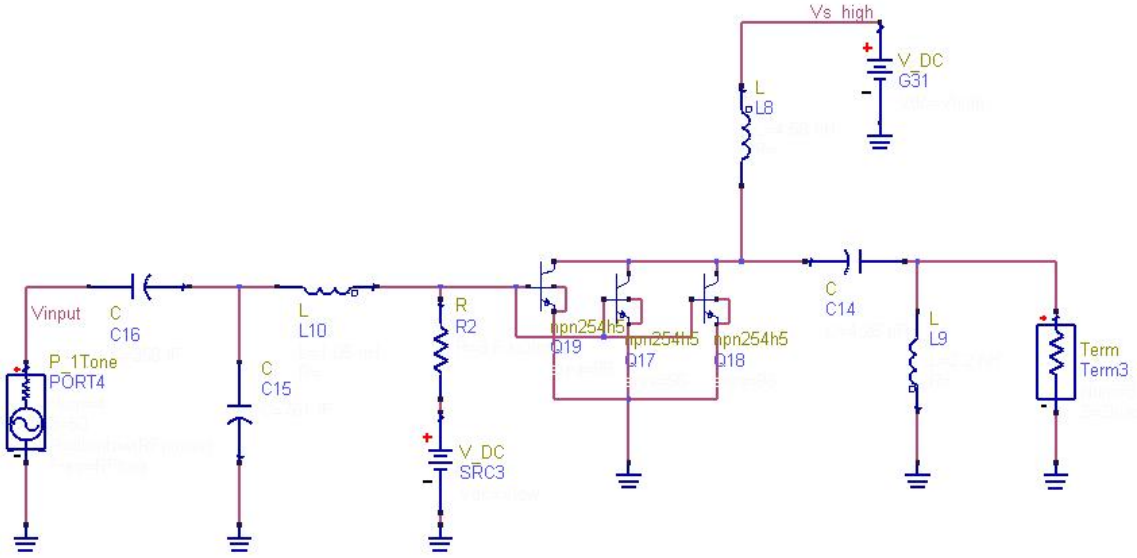


Figure 3.12: Class A PA schematic with ideal elements in ADS

This single stage Class A PA circuit provides 15.8 dBm output power at the 1 dB compression point, as given in Figure 3.13. The input power at 1 dB compression point is -3.5 dBm and at this point PAE is about 23%, which is an expected result of Class A operation. Maximum PAE is about 40% as shown in Figure 3.14.

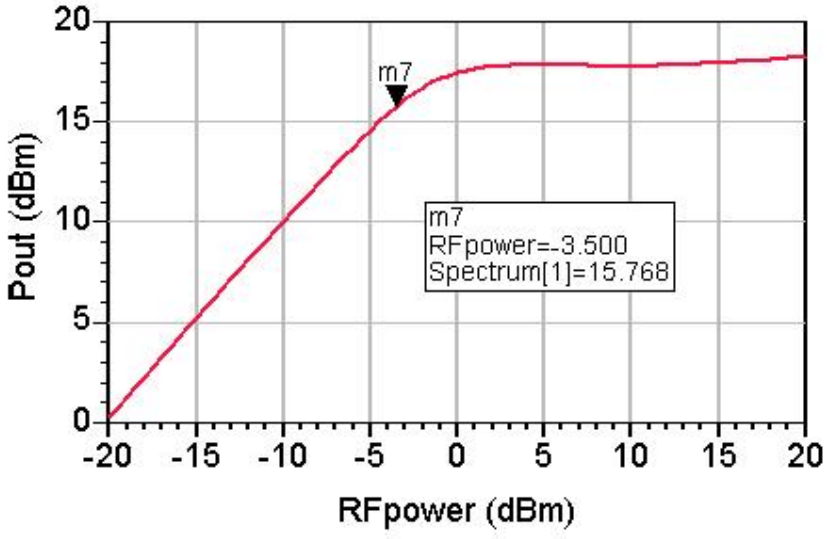


Figure 3.13: Single stage Class A output power and 1 dB compression point

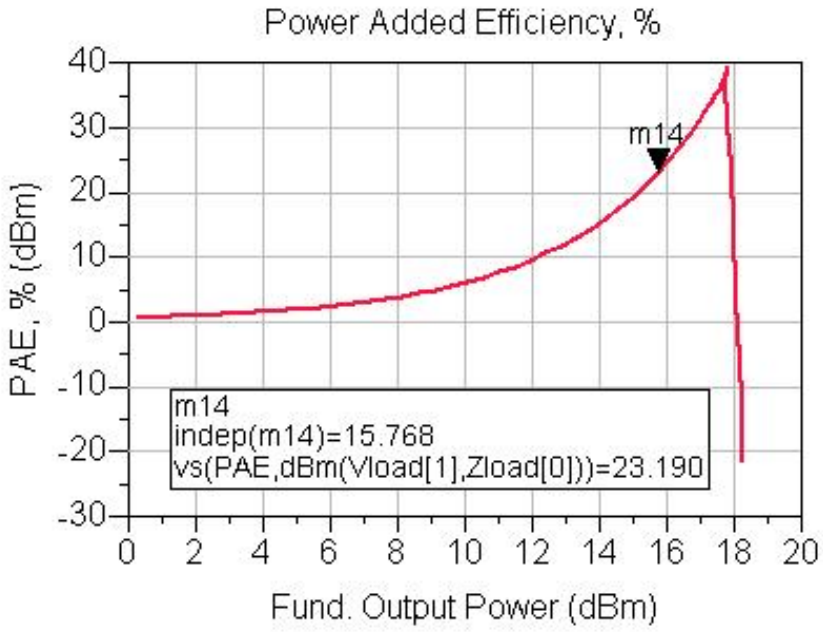


Figure 3.14: Single stage Class A PAE curve

As seen from the Figure 3.13, single stage PA provides an output power level very close to the IEEE 802.11a specified maximum output power level, which is 16 dBm (40 mW). However, our main goal is to obtain higher output power levels at 5GHz and to achieve this goal, the on-chip power combining technique is used, where two single stage Class A PAs are combined. This technique is described in detail in the following section.

3.6 Wilkinson Power Combiner/Splitter Design

The first idea to be tested in this thesis is combining two single stage Class A PAs via power combining techniques in order to increase the output power and improve the linearity performance. Out of many power combining techniques, Wilkinson power combiner method is utilized. In Figure 3.15, two power amplifiers are combined via on-chip Wilkinson power combiners.

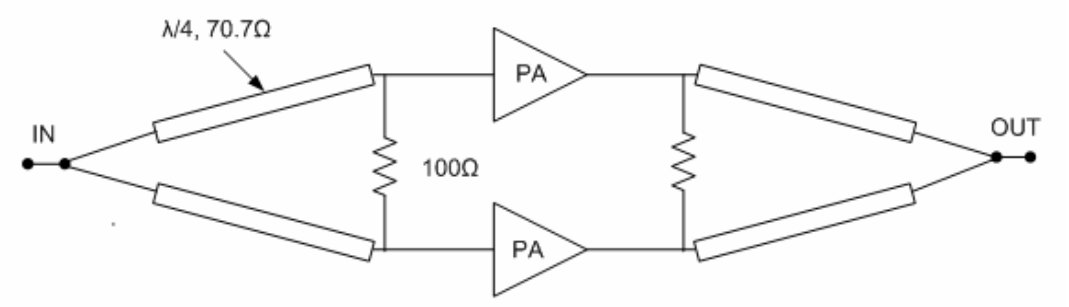


Figure 3.15: In-phase power combining using Wilkinson power combiners

A classical microstrip Wilkinson power splitter consists of two quarter wave microstrip line segments with characteristic impedance $Z_0 * \sqrt{2}$ at the operating center frequency f_0 and a $2 * Z_0$ lumped resistor connected between the two ports, as shown in Figure 3.16. Wilkinson power combiners can be interpreted as 2:1 impedance transformers, which transform each 50Ω input to 100Ω, where the two are paralleled. The function of the isolation resistance is to terminate any odd mode signals.

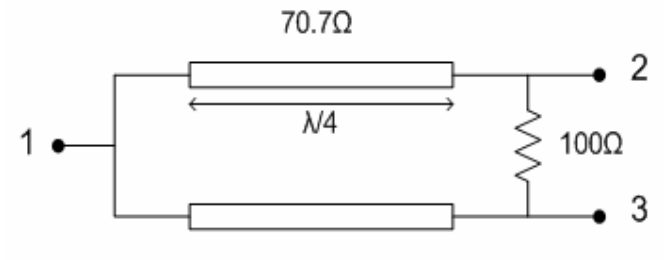


Figure 3.16: Microstrip Wilkinson combiner

The S parameters for such a three port network are given by the matrix [8]:

$$[S] = \frac{-1}{\sqrt{2}} \begin{bmatrix} 0 & j & j \\ j & 0 & 0 \\ j & 0 & 0 \end{bmatrix} \tag{3.5}$$

The figures of merit of a Wilkinson power combiner are the return loss at ports 1 and 2 (RL_1 and RL_2), the coupling between ports 1 and 2 (CP_{12}) and isolation between ports 2 and 3 (IL_{23}).

$$RL_1 = -20\log|S_{11}| \tag{3.6}$$

$$RL_2 = -20\log|S_{22}| \tag{3.7}$$

$$CP_{12} = -20\log|S_{21}| \tag{3.8}$$

$$IL_{23} = -20\log|S_{23}| \tag{3.9}$$

Ideally, return loss and isolation should approach negative infinity at the center frequency and the coupling should be very close to 3dB. Therefore, Wilkinson power splitter provides low loss, equal split, matching at all ports and high isolation between output ports [9]. In fact, at RF frequencies the quarter wave transmission line sections can have unrealistic dimensions. Thus, at higher frequencies the classical microstrip realization can be replaced with its lumped element counterpart, as given in Figure 3.17. Lumped element Wilkinson power splitter is obtained by replacing both quarter wave transmission line sections with their equivalent lumped element "Pi" LC network model at the design center frequency f_0.

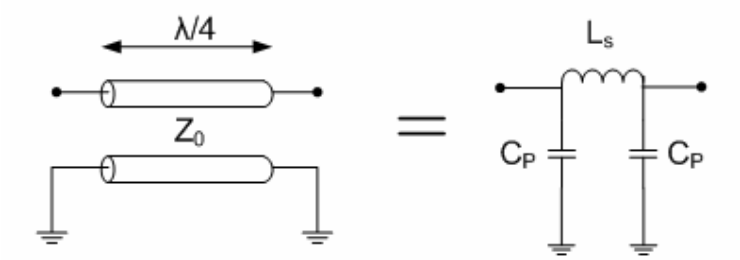


Figure 3.17: "Pi" LC network model of a quarter wavelength transmission line

The inductance and capacitance values associated with the "Pi" LC equivalent network can be found from the below equations:

$$L_S = \frac{Z_0}{2 * \pi * f_0} \tag{3.10}$$

$$C_P = \frac{1}{2 * \pi * f_0 * Z_0} \tag{3.11}$$

At 5GHz center frequency, L_S and C_P values are found for two way equal Wilkinson power divider from the below equations.

$$L_S = \frac{50\sqrt{2}}{2 * \pi * 5 * 10^9} = 2.25 \text{ nH} \tag{3.12}$$

$$C_P = \frac{1}{2 * \pi * 5 * 10^9 * 50\sqrt{2}} = 450 \text{ fF} \tag{3.13}$$

From the above equations, we obtain C_P = 450 fF and L_S = 2.25 nH at 5GHz. With these capacitance and inductance values, a lumped element equal 2-way Wilkinson power splitter at a center frequency of 5GHz is obtained as shown in the Figure 3.18.

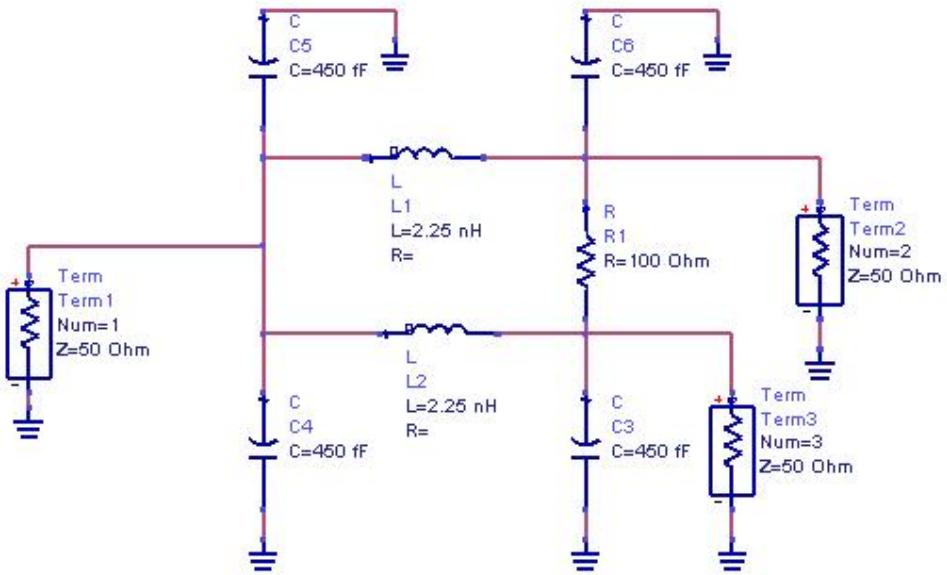


Figure 3.18: Lumped element Equal split Wilkinson power divider at 5GHz center frequency

The lumped element Wilkinson power splitter exhibits perfect isolation at the input port and equal power division at the output ports. These can be seen from s_{11}, s_{21} and s_{31} plots in Figure 3.19, obtained via ADS tool.

At 5 GHz, s_{11} drops down to -65 dB, when simulated with ideal elements. Likewise, s_{21} and s_{31} values are -3 dB as expected, indicating that the power is equally divided into two at 5 GHz. However, it should be noted that a Wilkinson divider/combiner is not a broadband device. Typical frequency bandwidths do not exceed 20% of the center frequency.

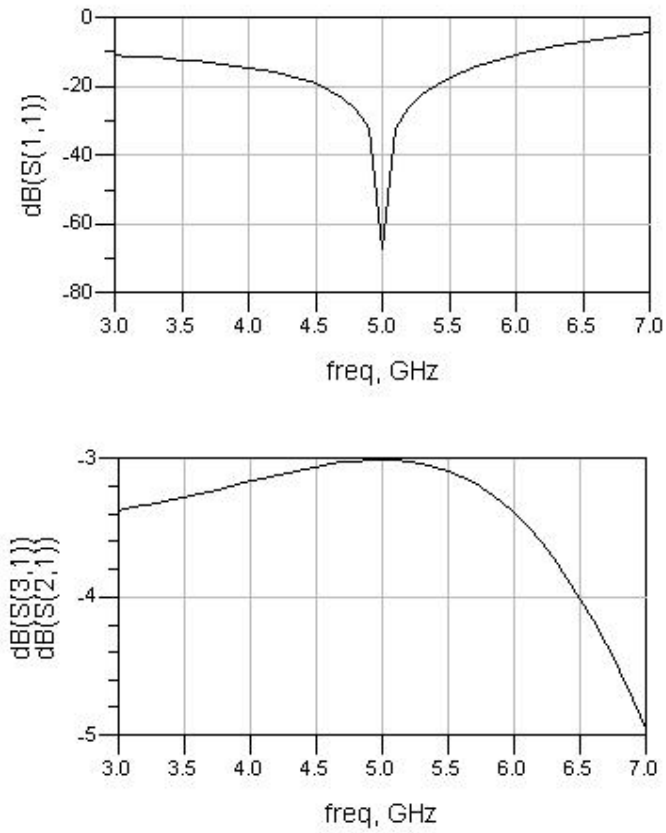


Figure 3.19: Simulated s_{11}, s_{21} and s_{31} parameters of lumped element Wilkinson power splitter model

In the upcoming sections, this Wilkinson power splitter configuration will be used to combine two single stage Class A power amplifiers in order to obtain higher output power levels and better 1 dB compression values, therefore to improve the linearity.

3.7 Microstrip Line/Coplanar Waveguide Equivalent Model of RF Choke

In this section the idea of using capacitively loaded microstrip transmission lines instead of low Q inductors will be discussed. The purpose of doing such a replacement is to reduce conductor and substrate losses, while shrinking the die area.

First, the performance simulations of capacitively loaded microstrip lines are performed in ADS environment. Then, the same simulations are done, again in ADS, for capacitively loaded coplanar waveguide. But, before discussing the ADS simulations for two different configurations, brief background information about the transmission line theory will be given.

3.7.1 Theoretical Foundation

Input impedance of any transmission line is given by the formula:

$$Z_{in} = Z_c \frac{Z_L + jZ_c \tan \beta l}{Z_c + jZ_L \tan \beta l} \tag{3.14}$$

where Z_c is the characteristic impedance of the line, Z_L is the load impedance, l is the length and β is the propagation constant.

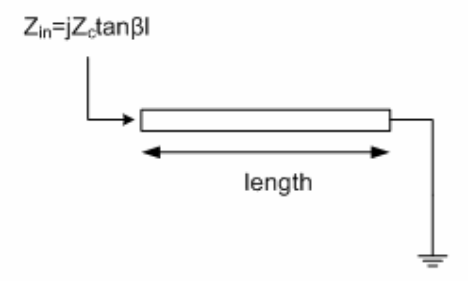


Figure 3.20: Short circuited transmission line

If the line is terminated with short circuit as in Figure 3.20, load impedance would be zero, i.e. Z_L=0 and the input impedance expression takes the form:

$$Z_{in} = jZ_c \tan \beta\ell \tag{3.15}$$

where $\beta = \frac{2\pi}{\lambda}$ and $\beta\ell$ defines the electrical length of the line.

As the length of the line is changed, it can either be used as an inductor or a capacitor, as shown in Figure 3.21. This is the idea behind using a microstrip line with a

certain length as an RF choke inductor. The length of the line is adjusted in such a way that it shows a big inductance.

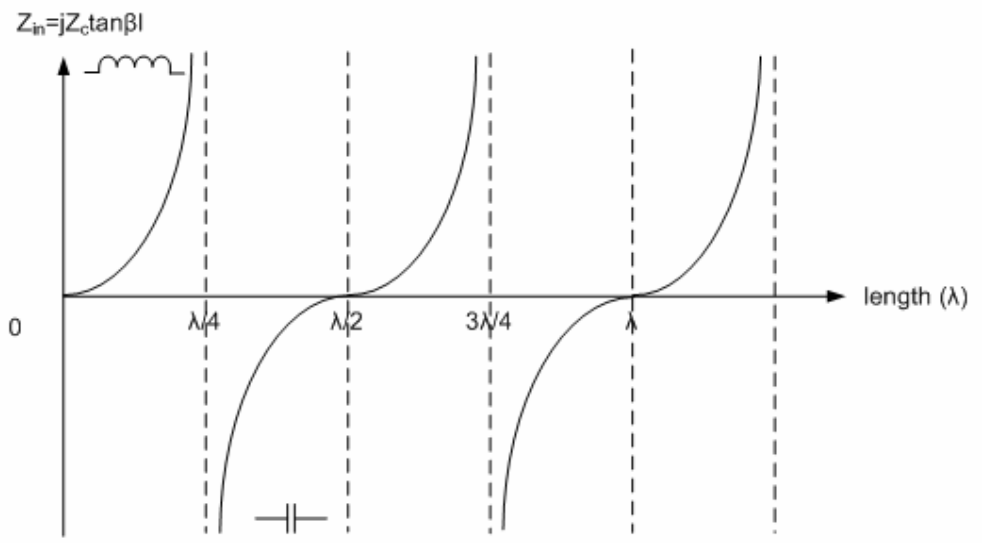


Figure 3.21: Input impedance versus length

At 5 GHz, the wavelength is:

$$\lambda = \frac{c}{f} = \frac{3*10^8}{5*10^9} = 6cm \tag{3.16}$$

This means that in order to obtain a big inductance, we need a lengthy microstripline model. One way to shorten the length of the microstripline/CPW is to load it with shunt capacitors. However, loading the microstripline/CPW with shunt capacitors has a drawback; it actually affects the quality factor (Q) of the model in a bad way. Before giving the theoretical proof of this drawback, brief definition of the quality factor will be given.

The efficiency (quality) of any oscillating system can be expressed as the ratio of energy stored by the system to the power the system dissipates per cycle. This ratio is called the quality factor. For a low loss line, where L_0 and R_0 are the inductance and resistance per unit length, and w_0 is the fundamental resonant angular frequency;

$$Q = \left|\frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)}\right| = \frac{wL_0}{R_0} \tag{3.17}$$

However, the effect of adding a shunt capacitor to a line can be understood from the following calculations.

First the new input impedance (Z_{new}) of the line with the capacitor in parallel will be calculated. Then, the new quality factor (Q_{new}) can be found by dividing the real part of this new input impedance to its imaginary part.

$$Z_{new} = \frac{(R + jX)\frac{1}{wC}}{(R + jX) + \frac{1}{wC}} = \frac{R + jX}{wRC + jwXC + 1} \tag{3.18}$$

$$Z_{new} = \frac{(R + jX)(1 + wRC - jwXC)}{(1 + wRC + jwXC)(1 + wRC - jwXC)}$$

$$Q_{new} = \left|\frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)}\right| = \left|\frac{X}{R(1 + wRC) + wX^2C}\right| \tag{3.19}$$

Q_{new} expression shows that, when a shunt capacitor is added to a line with Z_{in}=R+jX, quality factor decreases as a function of the capacitance added. Although capacitive loading a line decreases the line's quality factor, it also substantially decreases the length of the line. Therefore, we still support the idea of replacing RF choke inductors with capacitive loaded microstripline model, because as will be discussed in the next chapter, processing this model is much easier compared to processing inductors. Moreover, layout size of this model is comparable with inductor sizes.

Two examples that support this idea are presented in sections 3.7.2 and 3.7.3.

3.7.2 Capacitively Loaded Microstrip Line Example

The Figure 3.22 shows a microstrip line model constructed in ADS. Microstrip lines have a length of only 100μm and a width of 10μm. MSub defines the microstrip substrate. With this MSub model, substrate thickness is set to 6.5 μm, ε_r (relative dielectric constant) is set to 4.1, Mur (relative permeability) is set to 1, T (conductor thickness) is set to 3 μm and TanD (dielectric loss tangent) is set to 0.001. Conductor surface roughness (Rough) is set to its minimum and conductor conductivity (Cond) is set to a very high value.

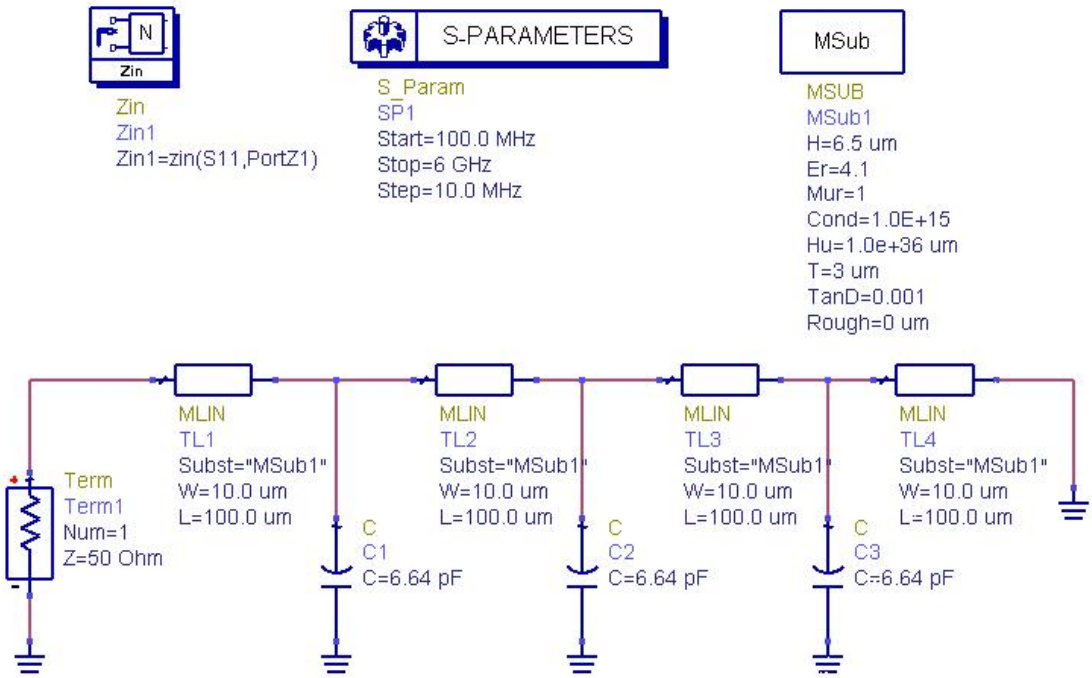


Figure 3.22: Capacitively loaded microstrip line model

ADS simulation results show that the capacitively loaded microstrip line model given in Figure 3.22 has an inductance of 4.66 nH at 5 GHz, as shown in Figure 3.23. To find the impedance of a 4.66 nH inductance at 5 GHz, the following calculations are done.

$$Z_L = wL = (2*\pi*5*10^{9})*(4.66*10^{-9}) = 146\Omega \qquad (3.20)$$

This inductance value is suitable to be used as an RF choke. Therefore, we can replace the RF choke inductance with the transmission line model in the PA design. However, this model is very sensitive to frequency, meaning that it only acts as an inductance of 4.66 nH at 5 GHz and starts to act capacitively at higher frequencies, thus the design will be narrowbanded.

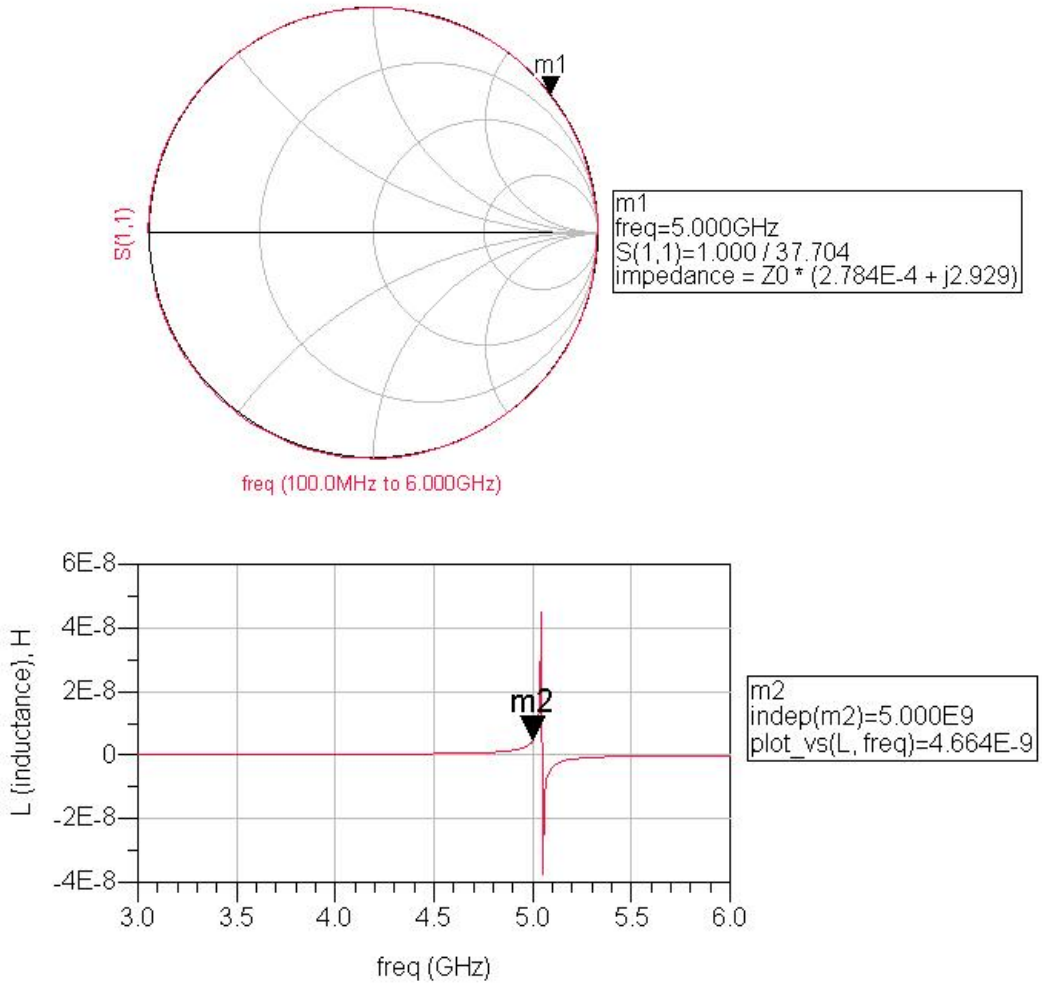


Figure 3.23: Inductance of capacitively loaded microstrip line model

3.7.3 Capacitively Loaded CPW Example

After the performance simulations are done for microstripline model, for the next step the same simulations are performed for coplanar waveguide model as shown in Figure 3.24. The same substrate as MSub is defined for the coplanar waveguide substrate, CPWSub. Again, the length and the width of the coplanar waveguide sections are set to 100µm and 10µm, respectively. "G" is the spacing between center conductor and ground plane and it is set to 35 µm.

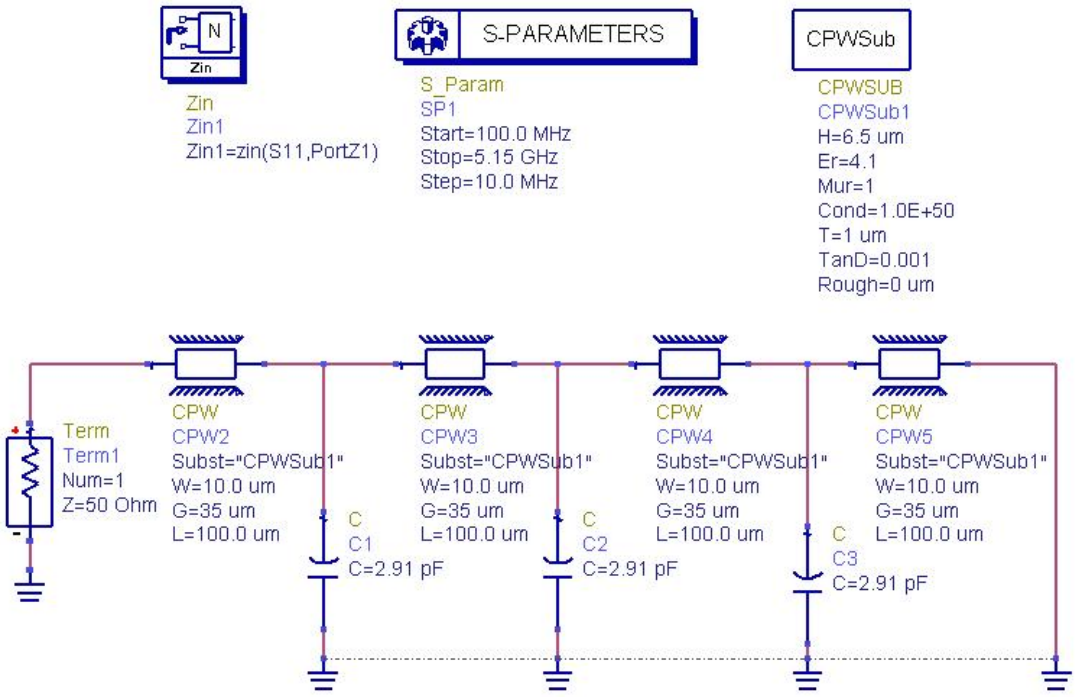


Figure 3.24: Capacitively loaded coplanar waveguide model

ADS simulations show that the capacitively loaded coplanar waveguide model is similar to its microstripline counterpart, in terms of inductance characteristics. Figure 3.25 shows that CPW model acts as a 4.84nH inductor at 5GHz. This model is also very sensitive to frequency, thus it is very narrowbanded. This behavior can be seen from Figure 3.25. At 5 GHz, this structure shows the maximum inductance value and this value drops as the frequency is decreases. At 5.1 GHz, the structure reaches its minimum inductance value and after this point it acts as capacitance rather than inductance. However, in both ways, either as inductance or capacitance, this structure shows high impedance as desired.

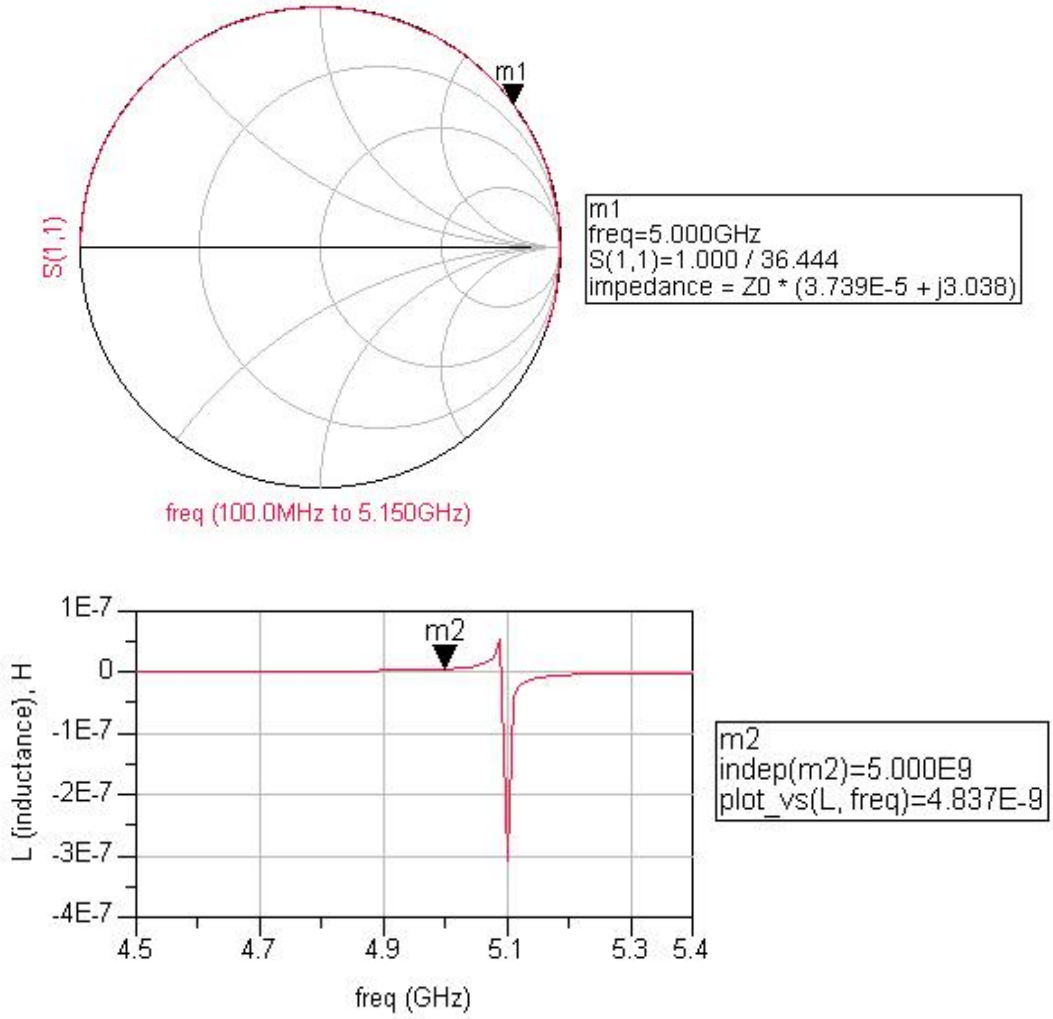


Figure 3.25: Inductance of capacitively loaded coplanar waveguide model

These two examples give an insight about the idea of using capacitively loaded microstripline/CPW models as RF choke. In the next chapter, a more detailed analyzes of these models will be done with more realistic conductivity (Cond) values. Our main purpose is to compare these models with spiral inductors in terms of size, loss (Q) and ease of process.

Chapter 4

4 NUMERICAL RESULTS

4.1 Introduction

In this chapter, a more realistic simulation of the single stage PA will be provided together with preliminary numerical results. These simulations are performed in Cadence environment. The design is based on SiGe BiCMOS process of AMS and Cadence supports passive and active AMS models. Therefore such a transferring the design from ADS environment into Cadence was necessary. Concerning the passive elements, the technology features 4 aluminum metal levels, which makes possible the realization of a large range of capacitances and inductances. Thus, the same circuit is simulated in Cadence environment with AMS models, such as thick metal (spiral) inductors, metal-metal capacitors (CMIM), bipolar transistors (npn 254H5) and Poly2 resistors. These simulations will provide a better insight on the behavior of the PA with real AMS models.

In Cadence environment, different PA topologies are tested in order to realize the ideas presented in the previous chapters. One of the ideas was to use capacitively coupled microstrip lines instead of low Q inductors in order to decrease the conductor and substrate losses, and the second idea was to utilize Wilkinson power combining technique to obtain higher output power levels.

The organization of Chapter 4 will be as follows:

Three different circuits with different elements will be presented. First, a 4.58 nH inductor from the AMS library is connected between the collector and the 3 V DC voltage source of a single stage Class A PA. The purpose of this inductor is to provide a DC path from the source to the collector. The rest of the components, such as capacitors, inductors, resistors and transistors are also from the AMS library, thus they

are non-ideal. The performance simulation results and the circuit layout are presented. Then, the designed single stage PA is inserted into a WLAN 802.11a transmitter chain constructed in ADS environment. This transmitter is simulated to test whether the transmitted signal spectrum falls into the 802.11a transmit spectrum mask.

After single stage power amplifier topology is simulated, two single stage power amplifiers are combined with an on-chip Wilkinson power combiner. The performance simulations of this topology are also given in detail.

The final topology to be tested is the single stage power amplifier circuit in which capacitive loaded microstrip line is used as the RF choke. The performance simulations of this topology are given at the end of this chapter.

4.2 Single Stage PA Performance Analyzes

4.2.1 Cadence Simulation Results

First of all, performance simulations of the basic PA topology, given in Figure 4.1 are done in Cadence environment with all components taken from AMS library.

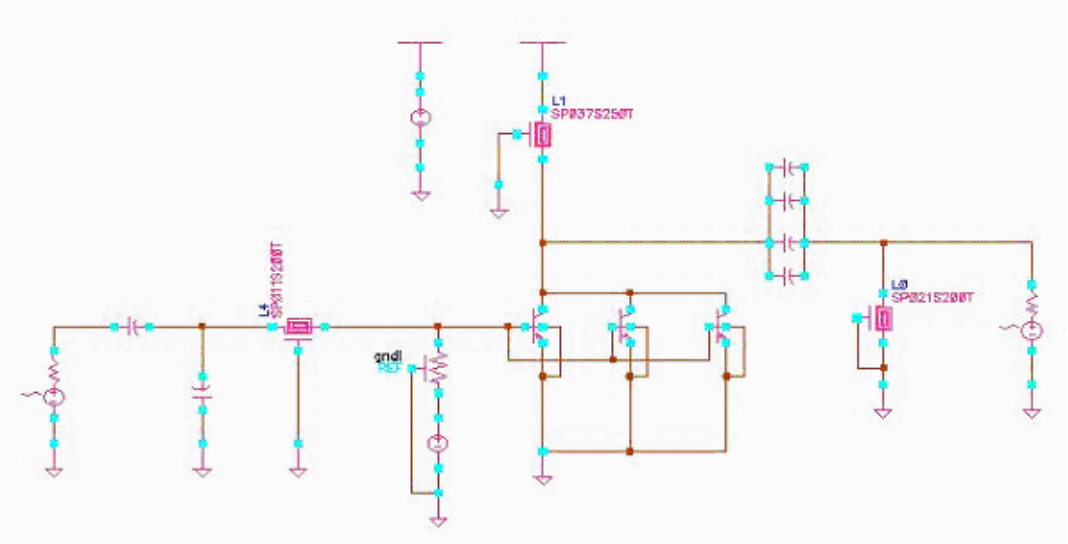


Figure 4.1: Simulation setup of single stage PA circuit

- Spiral inductor model, SP037S250T, which has an inductance of 4.58 nH and a quality factor of 6.2 is used as the RF choke to supply DC power to the transistors.

- AMS's thick metal spiral inductor model SP011S200T, which has an inductance of 1.05 nH and a quality factor of 11.8 at 5GHz, is a part of the input matching network.
- Spiral inductor model, SP021S200T, which has an inductance of 2.20 nH and a quality factor of 9.3 at 5GHz, is a part of the output matching network.
- RPoly2 resistance, which has a resistance of 3600Ω, is used at the biasing network in order to provide current to the base of the transistor array.

The capacitors at the input and the output matching circuitry are all metal-metal capacitors (CMIM) taken from the AMS library. These capacitors are ranging from 0.1pF - 1pF. Therefore, usually they are used in parallel form to obtain higher capacitances. Based on theoretical calculations the series resistance lies in the order of 0.1 Ω resulting in quality factors significantly exceeding 100. AMS npn bipolar transistors are used as the active device. In order to obtain high output power levels, three transistors are paralleled and maximum possible emitter length, which is 96 μm is utilized. We simulated circuit in Figure 4.1 by applying a 3 Volt DC to the collector and 17mA current flows through the collector of each transistor.

Input/output referred 1 dB compression points, power added efficiency (PAE), s_{11}, s_{22} and s_{21} (power gain) are the main performance parameters which are obtained via Cadence simulations and the results are presented in this subsection.

As mentioned before, 1 dB compression point is an important metric to understand the power amplifier performance. Linearity is directly related to 1 dB compression point in such a way that, higher the 1 dB compression point, better the linearity. There are two ways to define 1 dB compression point. First definition, which is called input referred 1 dB compression point, is the input RF power where the linear gain is dropped by 1 dB. Other definition, which is called the output referred 1 dB compression point, is the output power where the linear gain is dropped by 1 dB.

Figure 4.2 shows the input referred 1 dB compression point of the circuit given in Figure 4.1. As shown in Figure 4.2, input referred 1 dB compression point of the single stage PA topology is -0.6 dBm. At 1 dB compression point, the output power is 14.3 dBm. It can be interpreted from this metric that the PA operates linearly until the input power level reaches -0.6 dBm (and the output power level reaches 14.3 dBm). The gain of the amplifier at the linear region is 16 dB, therefore at 1 dB compression point, gain is about 15 dB. Also, maximum output power at saturation is about 18 dBm.

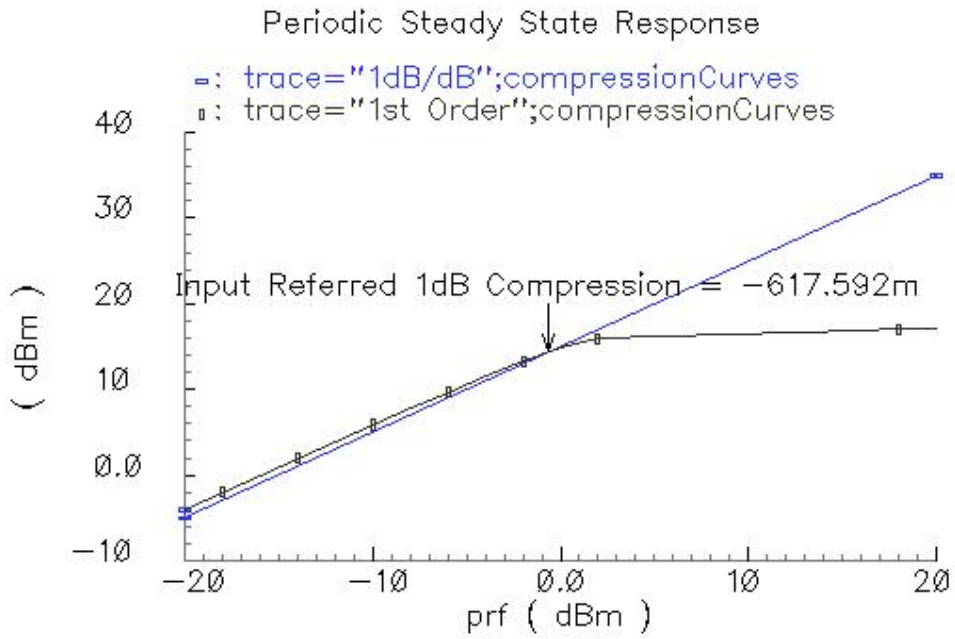


Figure 4.2: Input referred 1 dB compression point (Gain=14.95 dB at 1 dB compression point)

Another important metric is the power added efficiency, which gives an idea about the efficiency performance of the PA. Although the maximum efficiency is 50 % for a Class A operated PA, typical PAE values for the Class A operation is about 30%. Because, in real life, it is often not possible to get a peak voltage swing as the active device leaves its amplification region and enters the resistive region.

We are interested in the PAE value at 1 dB compression point, mainly because we intend to operate our PA in its linear region. PAE versus input RF power plot is given in Figure 4.3. As seen in this figure, PAE is about 17% at -0.6 dBm input power. This is an expected result, since the PA is operating in Class A mode.

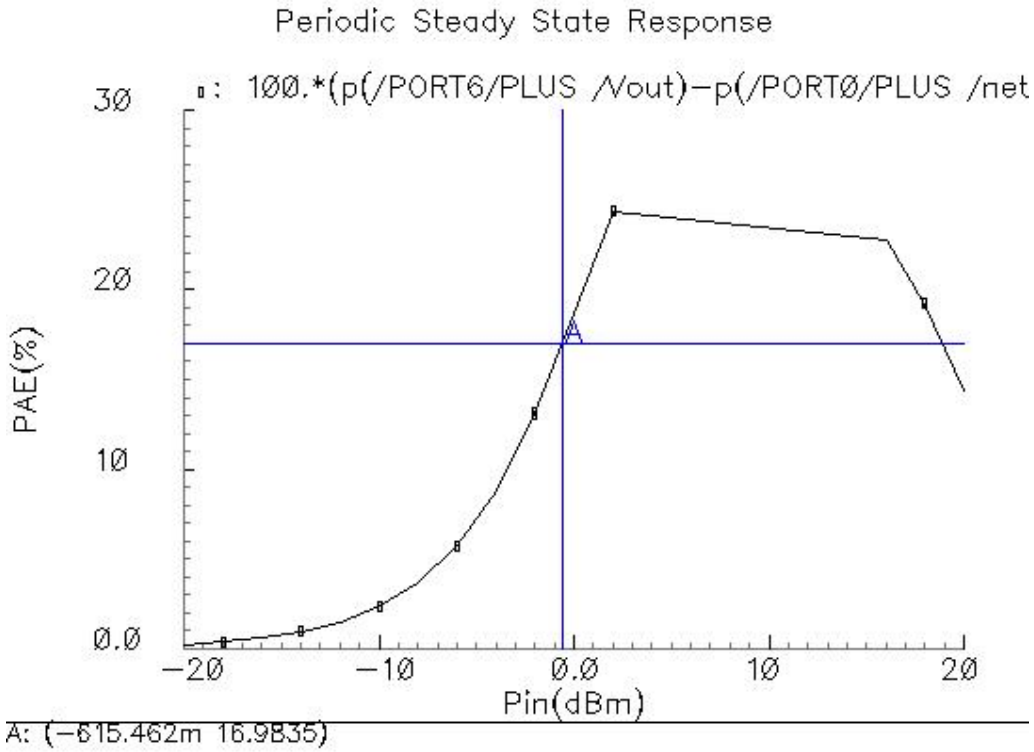
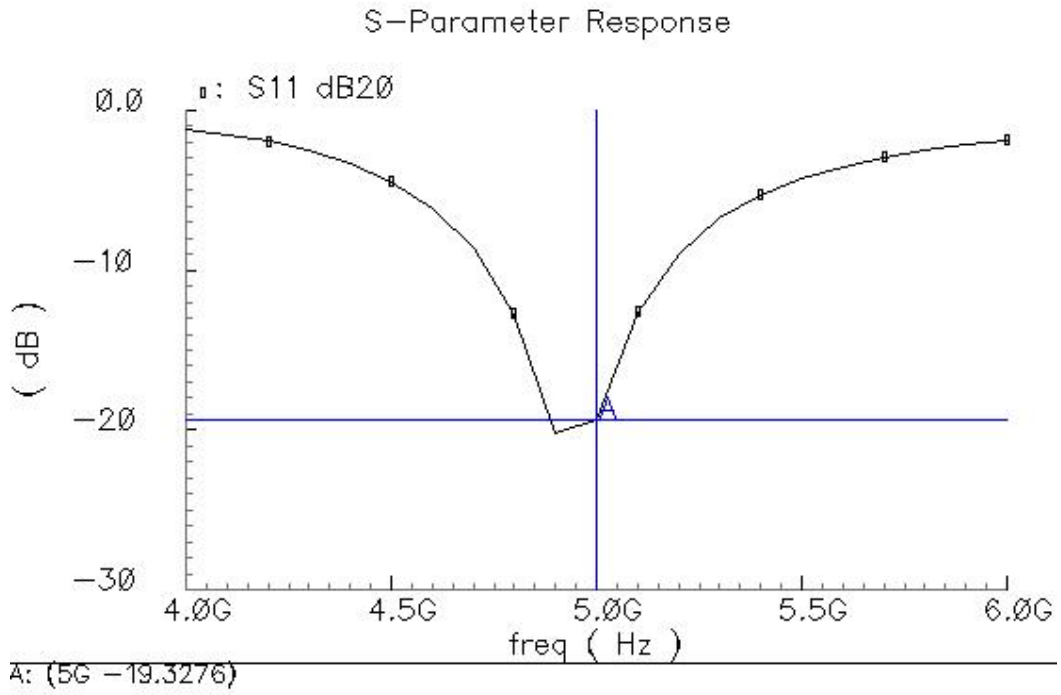
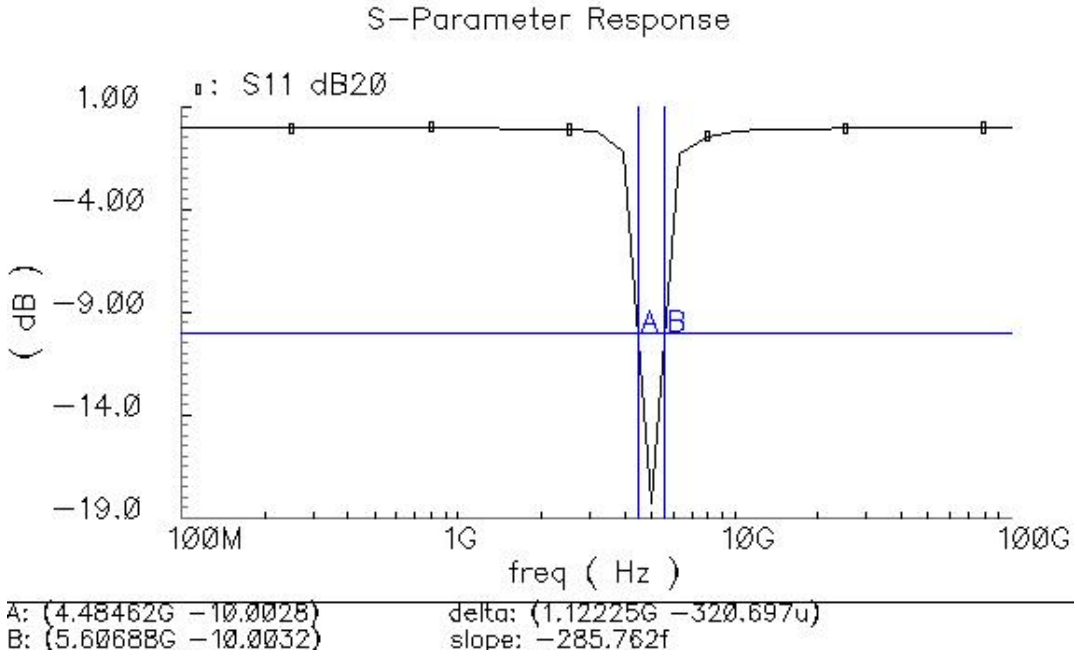


Figure 4.3: Power Added Efficiency (PAE)

Figure 4.4 (a) shows the simulation results of s_{11} from 4GHz to 6GHz. Simulations indicate that s_{11} reaches a value of -19.3 dB at 5GHz. Concerning the frequency bandwidth, Figure 4.4 (b) shows a 1.12 GHz bandwidth between 4.48 GHz and 5.6 GHz where s_{11} drops below -10 dB. Figure 4.5 shows the s_{22} response, which is -5.7 dB at 5 GHz. This rather high s_{22} is an expectable result since the output is matched according to the results of the load pull in order to obtain the maximum output power. Additionally the power gain (s_{21}) of the PA is shown in Figure 4.6. It shows that the power gain reaches 16.4 dB at 5 GHz.



(a)



(b)

Figure 4.4: (a) s_{11} response (b) frequency bandwidth in which s_{11} drops below -10 dB

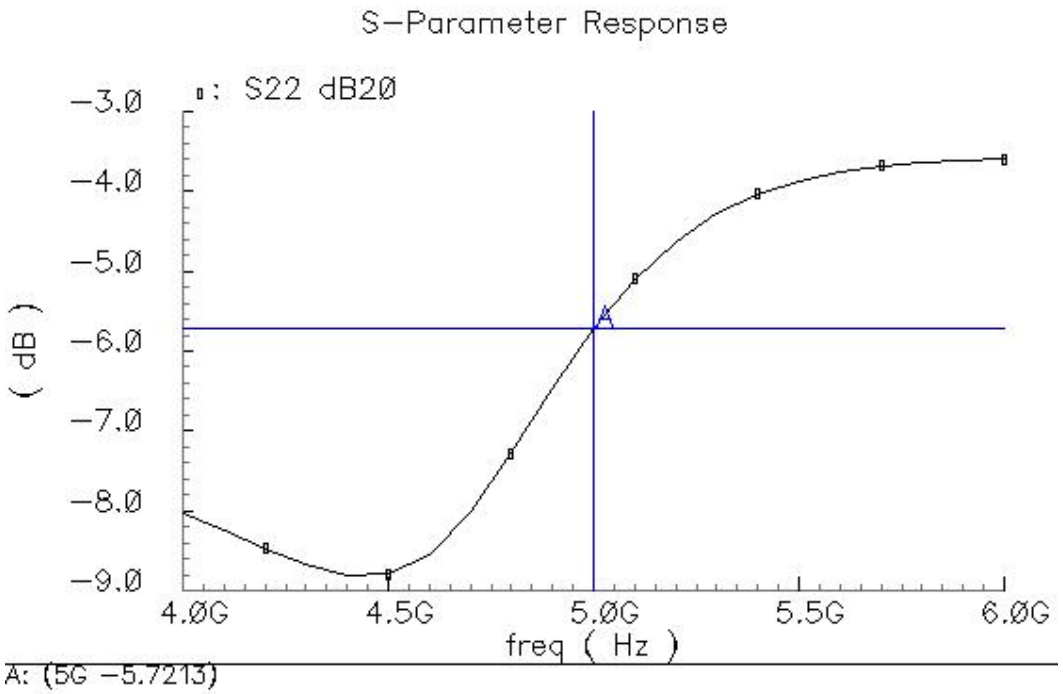


Figure 4.5: s_{22} response

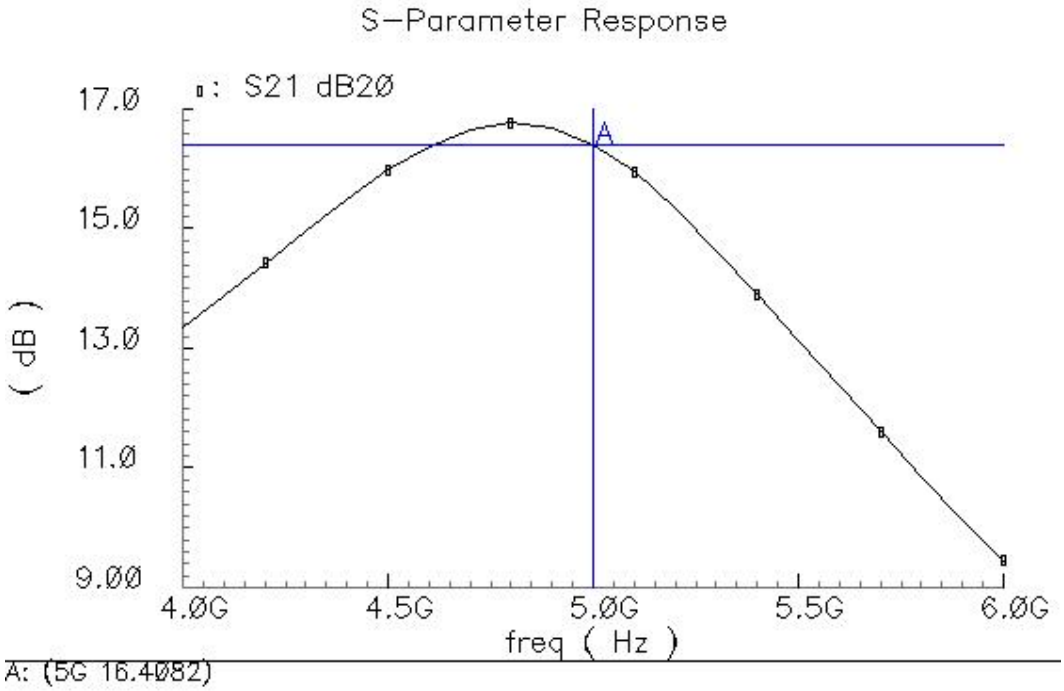


Figure 4.6: Power gain

Finally, third order intercept point is obtained by plotting third products versus input power which predicts a 3:1 response intersecting the 1:1 response at the third

order intercept point. The 3:1 terminology means that for every dB increase in input power, third order products will increase by 3 dB. Third Order Intercept will be approximately 10 to 20 dB higher than 1 dB compression point. Figure 4.7 shows the third order intercept point for the single stage PA case. As seen from Figure 4.7, first order and third order curves intersect at 30 dBm output power level, therefore output referred third order intercept point is 30 dBm.

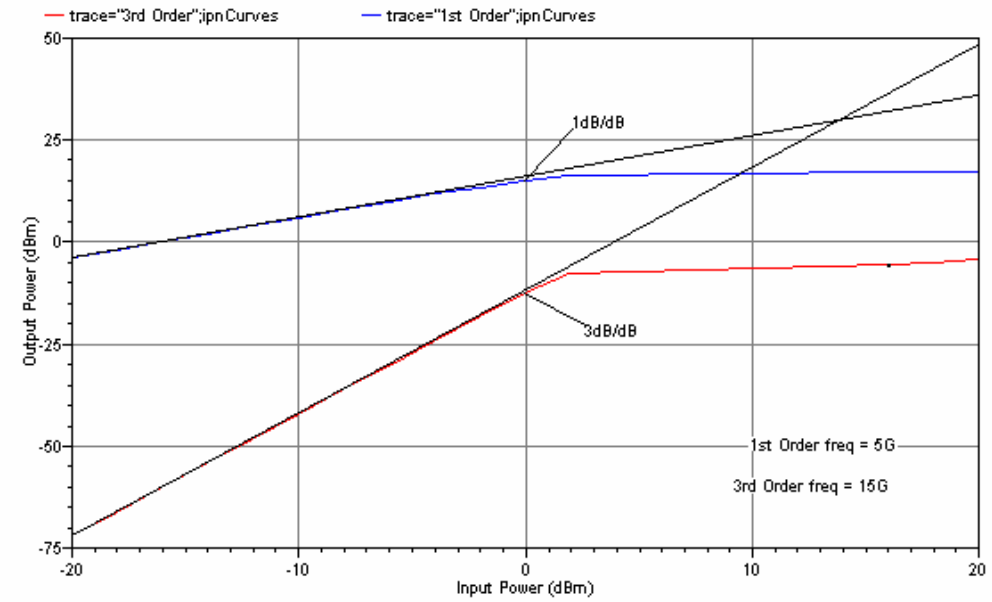


Figure 4.7: Third Order Intercept point

4.2.2 Final Schematic and Layout

After performance simulations are done, the final circuit schematic of the 5 GHz Class A single stage PA is drawn, as shown in Figure 4.8. In this figure, decoupling capacitors are connected between the DC sources and the ground to improve the DC-RF isolation. The layout of the single stage PA is given in Figure 4.9. In this layout, three bipolar npn transistors with emitter length of 96 μm are connected in parallel to form a transistor array. Substrate contacts are places around the transistor array to minimize the substrate losses. Capacitances were realized as metal/insulator/metal (MIM) capacitors. Three inductors are employed in the layout; one in the input matching, one in the output

matching and the one as the RF choke. The die size is 977*981 μm^2, including RF and DC bias pads.

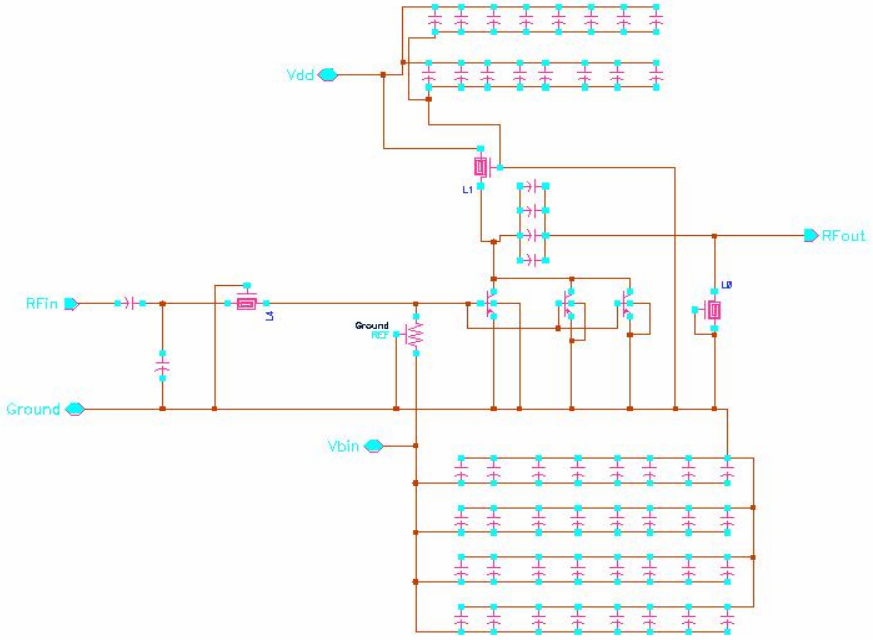


Figure 4.8: Final schematic of single stage PA

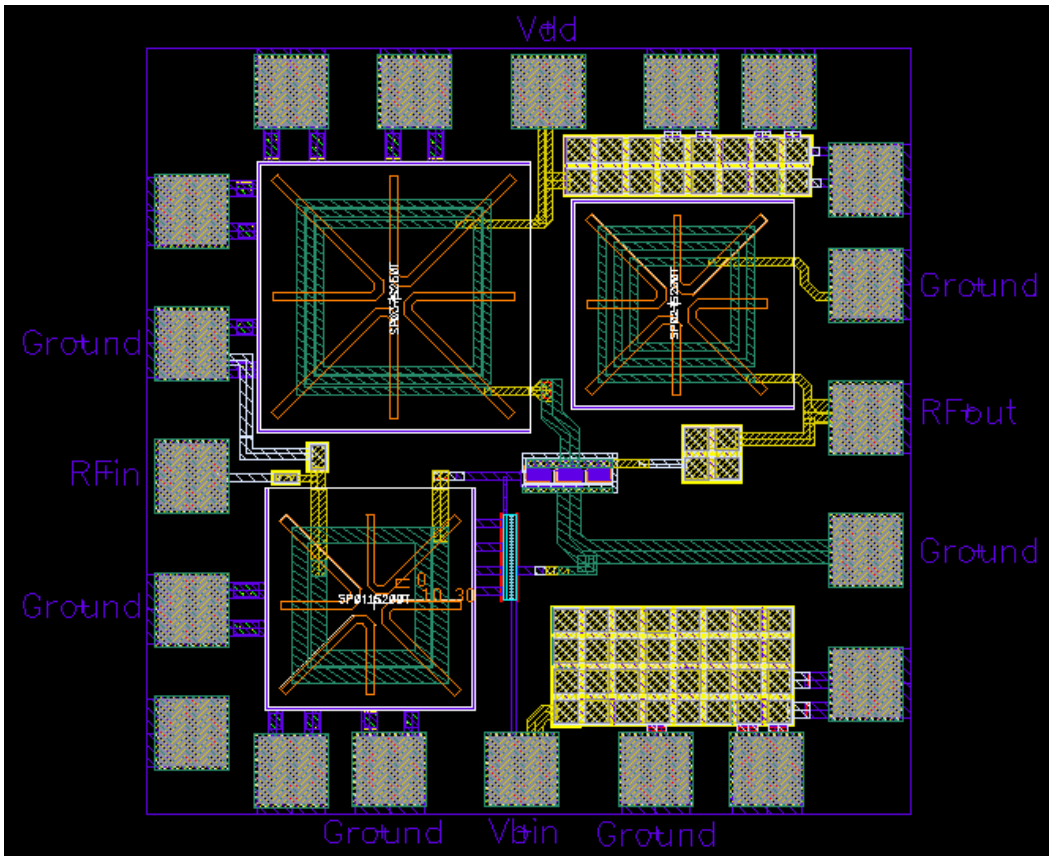


Figure 4.9: Layout of the single stage PA

4.2.3 WLAN 802.11a Spectrum Measurements

After the performance simulations of the single stage PA circuit is done in Cadence and its layout is drawn, different ADS setups are presented which are used to perform key measurements such as output RF spectra and EVM. These measurements are very useful to test and verify the designed PA. First, designed PA is inserted into a transmitter chain to determine its behavior under WLAN 802.11a conditions. This means that the transmitter is fed with a WLAN 802.11a RF signal source and the output signal is analyzed via the spectrum analyzer. The purpose of this design is to verify that the output RF spectrum doesn't exceed the spectrum mask requirements of IEEE 802.11a standard.

In Figure 4.10, the ADS setup for obtaining WLAN 802.11a output spectrum is given. It is a simple setup where the WLAN 802.11a transmitter is fed with a WLAN RF source and the transmitter output is connected to a spectrum analyzer.

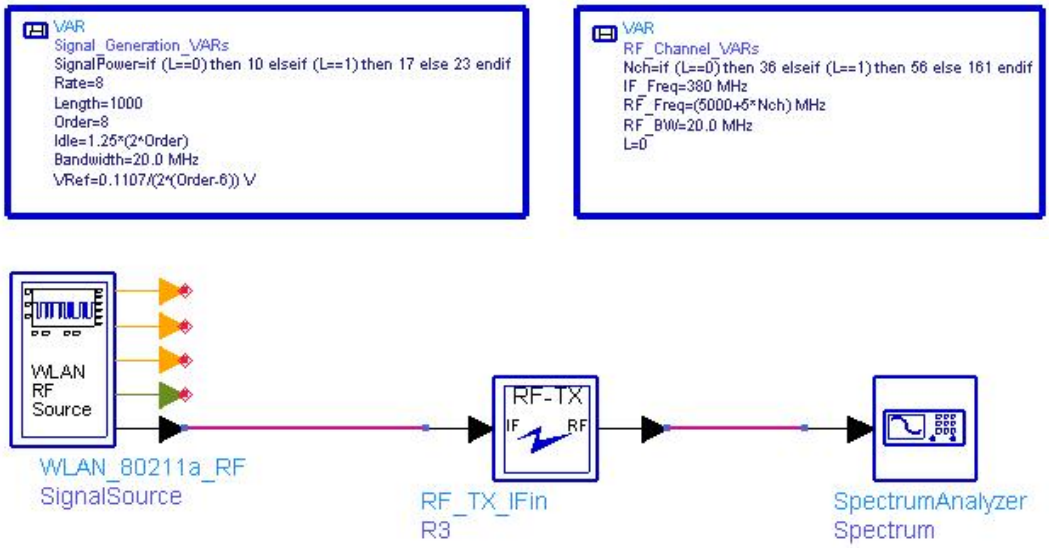


Figure 4.10: WLAN 802.11a spectrum measurement setup

Figure 4.11 shows the inside view of the WLAN 802.11a transmitter block given in Figure 4.10. The transmitter chain starts with the mixer which upconverts the input signal to the desired frequency. In this case the desired frequency is the frequency band specified by the IEEE 802.11a standard. The upconverted signal is fed into a Butterworth filter to get red of unwanted signals in the band. There are two filters in the transmitter and changing the filter parameter "N" will change the filter shape. The

filtered signal is first pre-amplified with the preamplifier. Then after the second filtering, the signal reaches the power amplifier block. We inserted our power amplifier into this transmitter chain by modifying the basic parameters of the PA model in Figure 4.11.

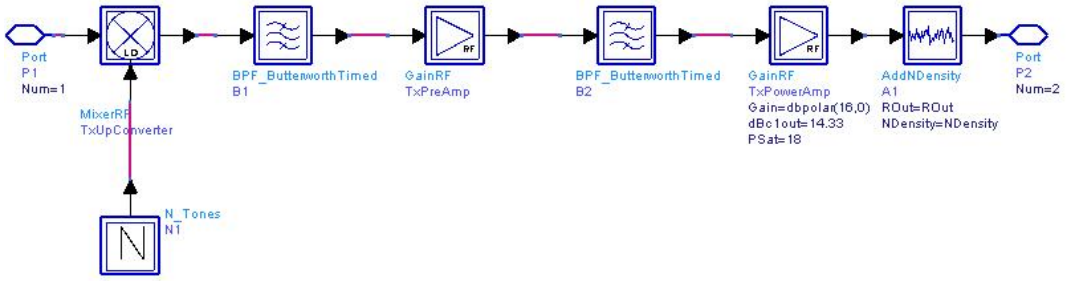


Figure 4.11: WLAN 802.11a transmitter

The PA parameters we have modified are the saturation power (Psat), output referred 1 dB compression power (dBc1out), output referred third order intercept power (TOIout), gain compression at saturation (GCSat) and gain. These parameters can be better understood from Figure 4.12.

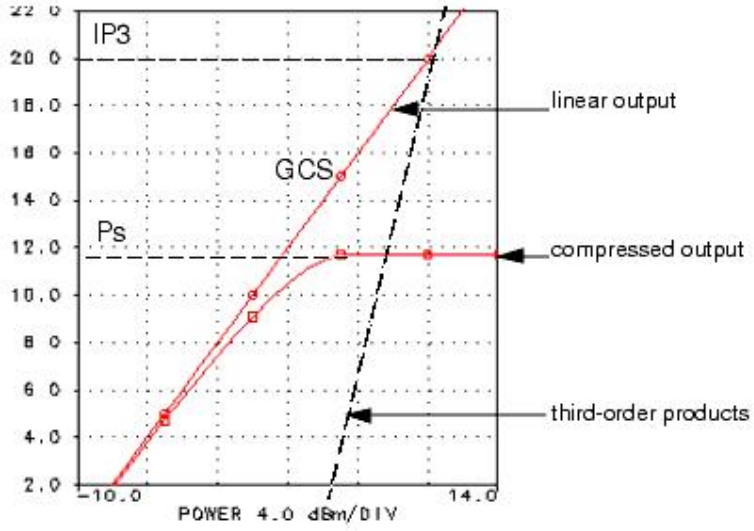


Figure 4.12: Important PA metrics

Input and output resistances of the PA are set to 50 Ω. The saturation power is set to 18 dBm, third order intercept power is set to 30 dBm, 1 dB compression point is set to 14.33 dBm and the gain is set to 16 dB. These values are obtained via Cadence simulations, which were given in section 4.2.1. In figure 4.13, the required transmit

spectrum masks are drawn and it is tested whether the transmitted signal obeys these masks. As can be seen from this figure, with designed PA parameters inserted into the PA model in the transmitter chain, the transmitted spectrum totally obeys the transmit spectrum mask specified by the IEEE 802.11a standard. This indicates a successful test result.

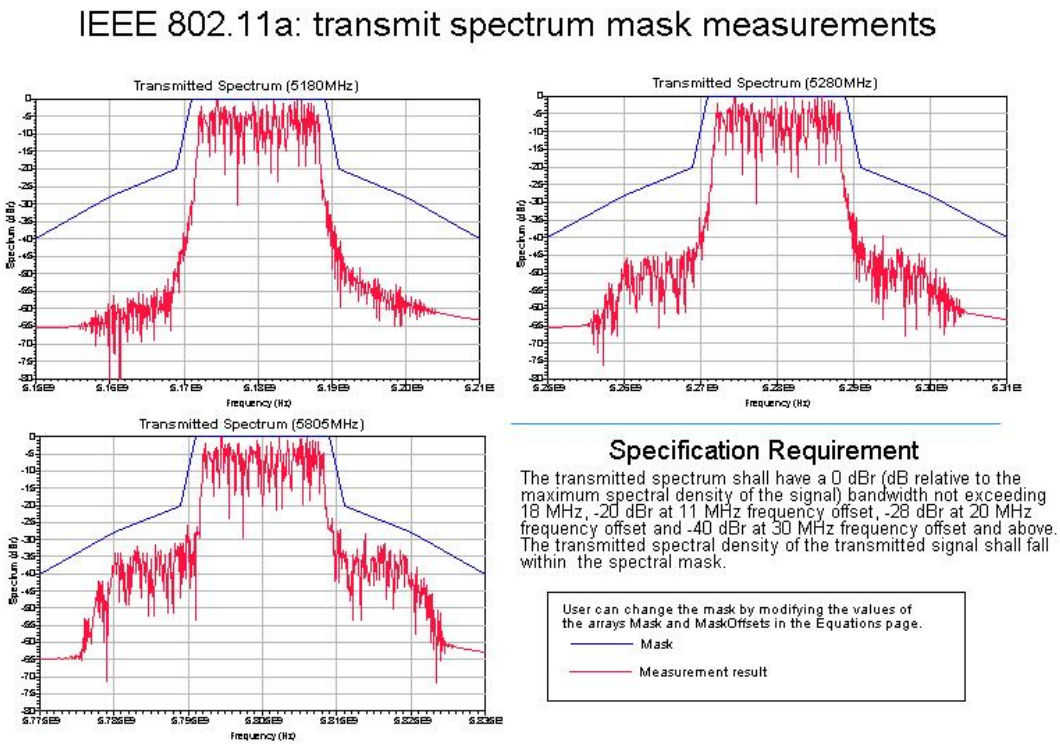


Figure 4.13: 802.11a transmit spectrum mask measurement results for three different frequency bands of 802.11a standard

This test can be improved by adding different channel models after the transmitter chain. By this way, under multipath channel environments, designed PA can be tested and verified in order to prove that this component can meet the WLAN standard. There are five WLAN channel models (A, B, C, D, E) defined in ADS. Channel models simulate a multi-path fading channel based on a taped-delay line model. The multipath delay profile determines the frequency selective nature of the channel. The WLAN channel models can be summarized as follows:

- Channel model A corresponds to a typical office environment with non line of sight (NLOS) conditions and 50ns average rms delay spread.

- Channel model B corresponds to typical large open space environment with non line of sight conditions or an office environment with a large delay spread. Average rms delay spread of channel model B is 100ns.
- Channel model C and E correspond to typical large open space indoor and outdoor environments, respectively with a large delay spread. Average rms delay spread of channel model C and channel model E are 150ns and 250ns, respectively.
- Channel model D corresponds to line of sight conditions in a large open space indoor or outdoor environment. Average rms delay spread of this channel model is 150ns.

More detailed information about the ADS WLAN channel models can be found in Appendix.

Out of these WLAN channel models, Channel model A is chosen as the transmitting medium for the 802.11a signals since it corresponds to a typical office environment with NLOS conditions. First the setup in Figure 4.10 will be modified by adding Channel Model A between transmit and receive antenna base stations, as shown in Figure 4.14. The base stations are located at the same height and there is a distance of 100 m between them. Again the designed PA parameters are inserted into the PA model, which is in the transmitter block. The transmit RF spectrum measurement results for the Channel model A case is given in Figure 4.15. As seen in this figure, the output RF spectrum doesn't exceed the spectrum mask requirement of IEEE 802.11a.

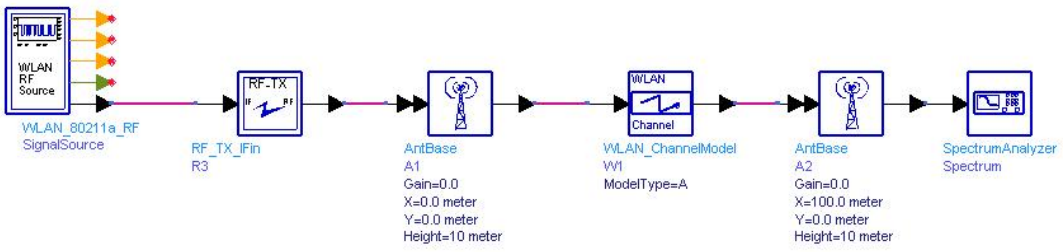


Figure 4.14: ADS setup for the IEEE 802.11a transmit RF spectrum measurements in the presence of WLAN channel model A

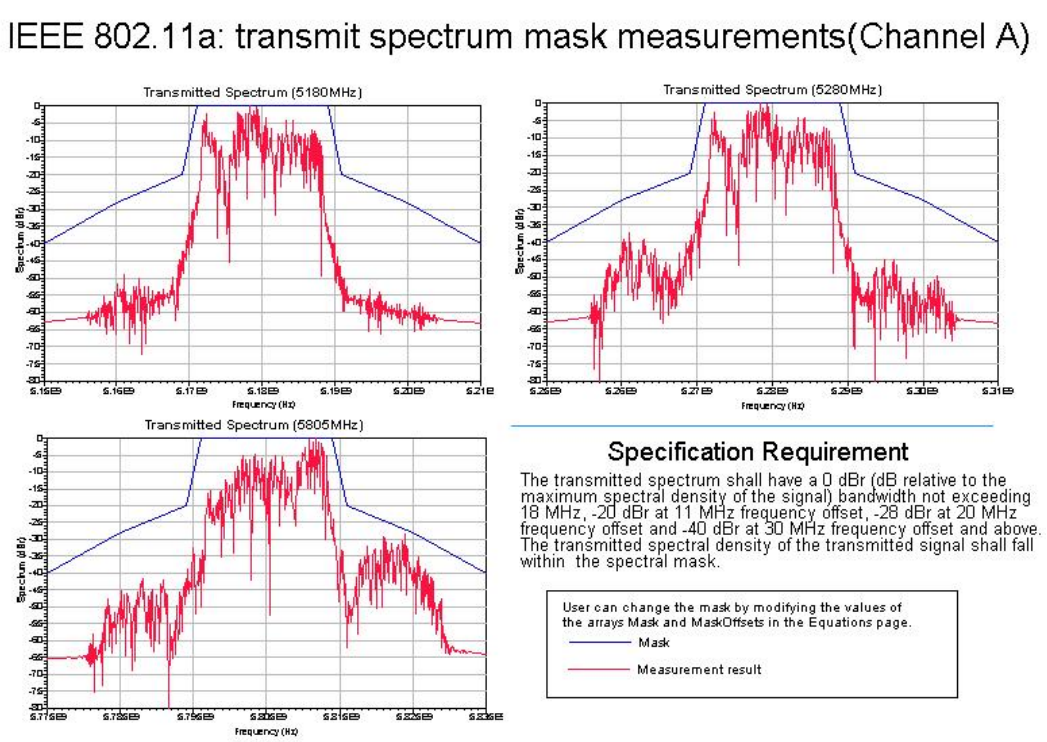


Figure 4.15: 802.11a transmit spectrum mask measurement results in the presence of WLAN channel model A

After measuring the output spectrum of the 802.11a transmitter with the designed PA parameters inserted, the next set of simulations is done in order to obtain the error vector magnitude (EVM) measurements. EVM measurements are essential because for IEEE 802.11a EVM defines the modulation accuracy. It is essential to obey the EVM requirements of the 802.11a standard. For EVM measurements, the ADS setup shown in Figure 4.16 is used.

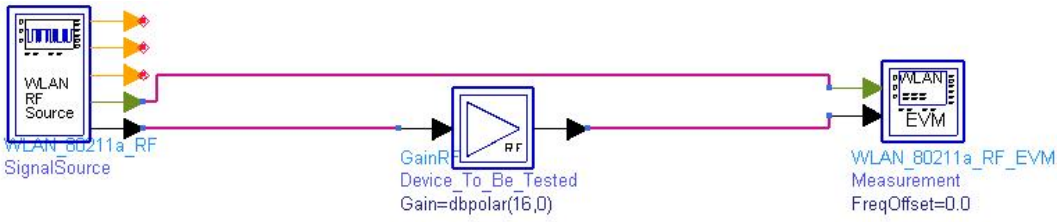


Figure 4.16: ADS setup for the IEEE 802.11a PA EVM measurements

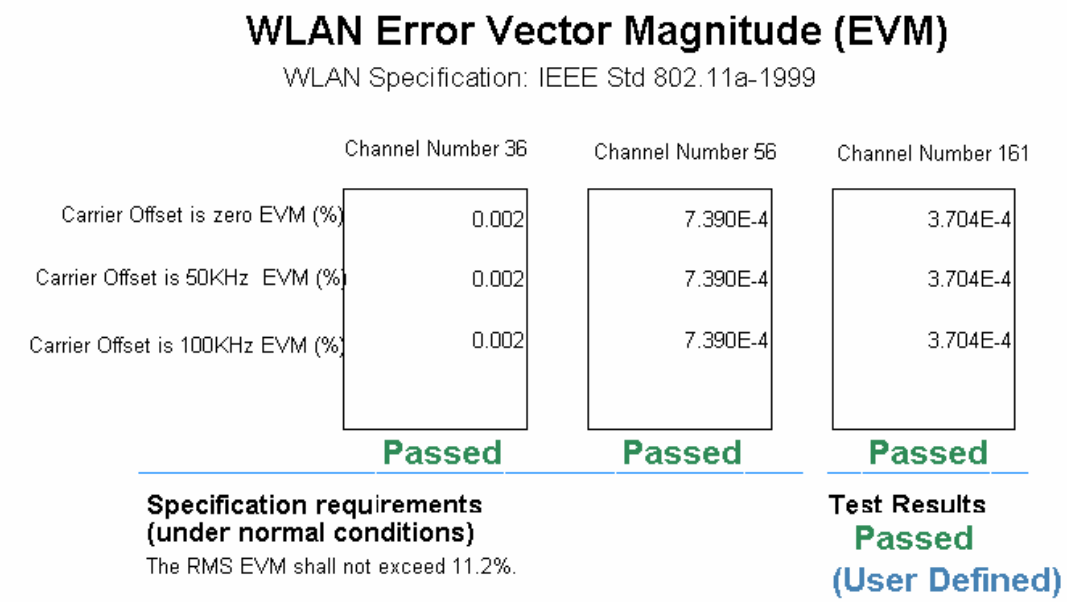


Figure 4.17: PA EVM measurement results

Figure 4.17 shows the EVM test results. The EVM values are automatically compared to the required EVM values by the IEEE 802.11a standard and the final result is shown. The EVM values are bounded by 11.2 % which is the requirement by IEEE 802.11a for Channel 36 with a center frequency of 5180 MHz. As seen in Figure 4.17, under 802.11a excitation, EVM test results are given for different carrier offset frequencies. As seen in this figure, EVM results are satisfactory for all the three channels. EVM is 0.2% for the channel 36, 0.07% for channel 56 and 0.037 for channel 161. It should be noted that Channel 36 has 5180 GHz, Channel 56 has 5280 GHz and Channel 161 has 5805 GHz center frequencies. Therefore, for Channel 36, Channel 56 and Channel 161, EVM test is passed.

4.3 Wilkinson Power Combined PA Topology

The idea of combining two single stage Class A power amplifiers via on-chip Wilkinson power combiner is simulated in Cadence environment. Two of the previously designed PA are combined via lumped element on-chip equal split Wilkinson combiner, as shown in Figure 4.18. In this architecture, the RF signal (at 5GHz) is first equally splitted into two and feed two identical single stage power amplifiers. The output stages of the two amplifiers are then combined with an on-chip lumped element Wilkinson power combiner. Actually, the same circuit topology is used both as the Wilkinson divider and the combiner.

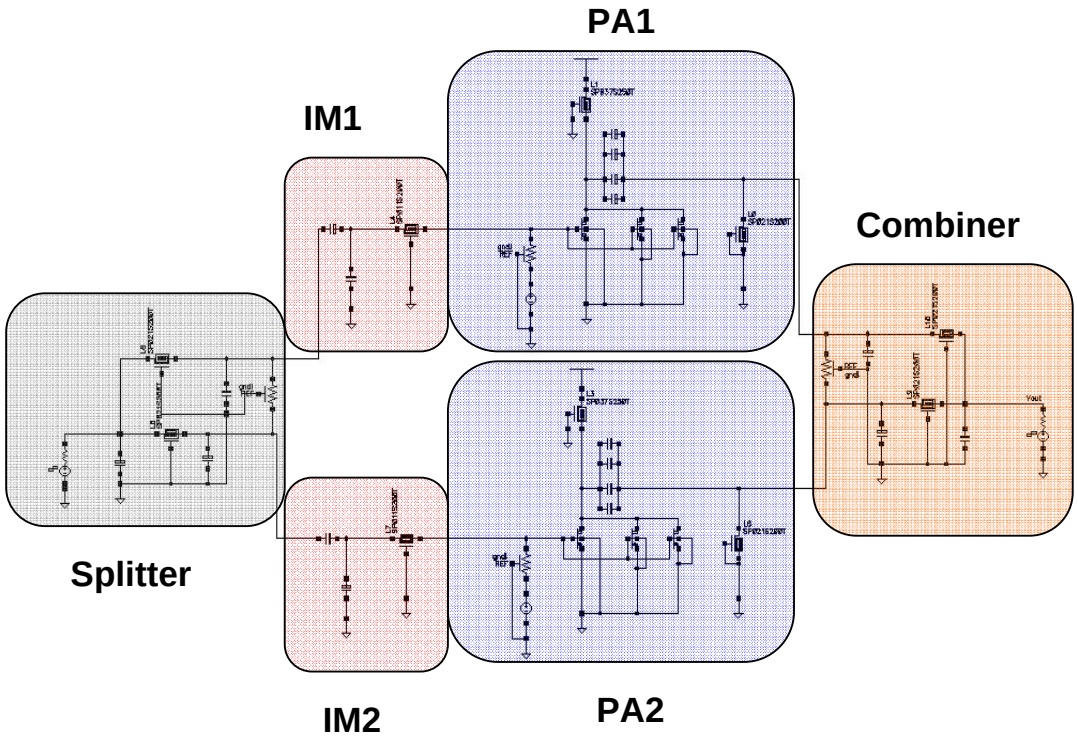


Figure 4.18: Combined power amplifier

The same performance simulations as the single stage PA circuit are performed for the power combined architecture. First, input and output referred 1 dB compression points are obtained. As given in Figure 4.19, input referred 1 dB compression point is 3.18 dBm which is much higher than the single stage PA case where the input referred 1 dB compression point was -0.6 dBm. For the power combined topology, output referred 1 dB compression point is 16.27 dBm, which is higher than the output referred 1 dB compression point of the single stage PA circuit. The difference between the input and

output referred compression points gives the gain at 1 dB compression, i.e. Gain is 13 dB. This means that the linear gain of the power combined topology is 14 dB.

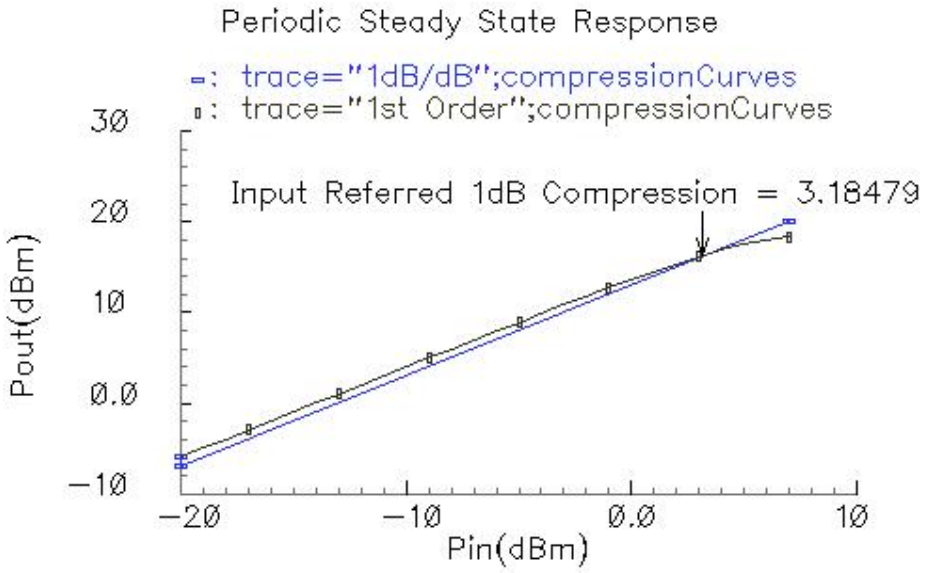
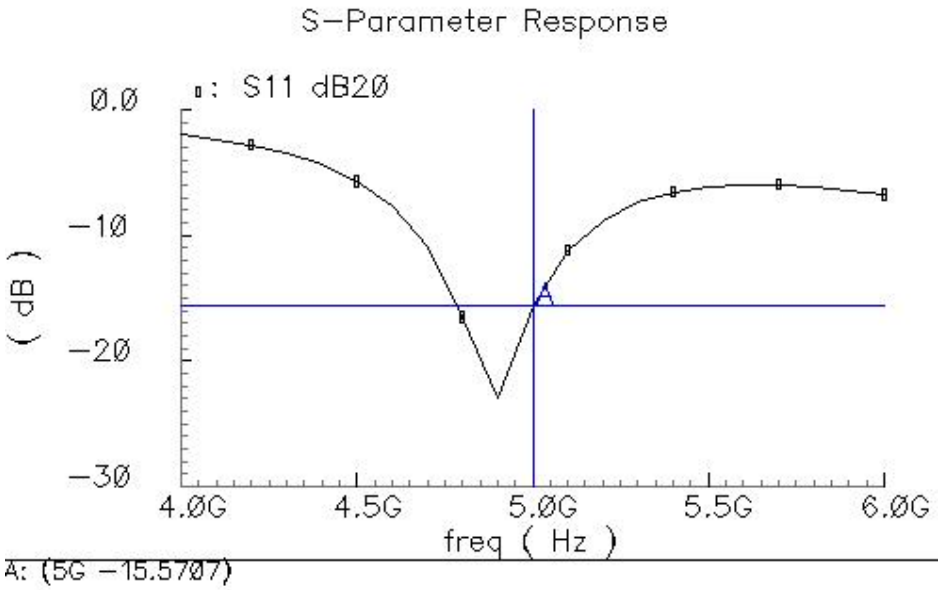
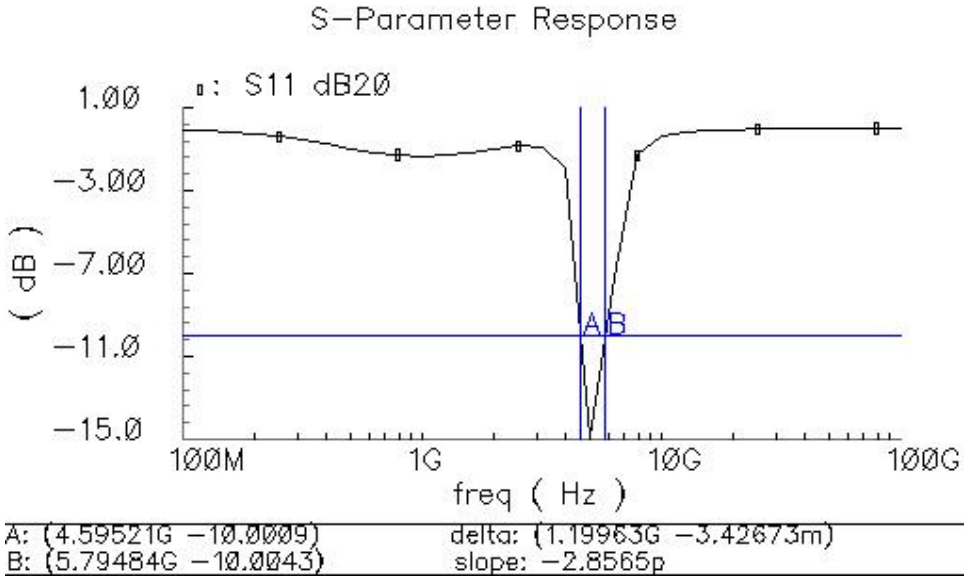


Figure 4.19: Input referred 1 dB compression point (Gain=13 dB at 1 dB compression point)

In figures 4.20 (a) and 4.20 (b) s_{11} plots are given. As can be seen from these figures, at 5 GHz s_{11} is -15.6 dB and looking in a logarithmic scale as in 4.20 (b), from 4.59 GHz to 5.79 GHz, s_{11} stays below -10 dB. This means that in a bandwidth of 1.2 GHz, very reasonable s_{11} value is obtained. Figure 4.21 shows the s_{22} response, which is -9.8 dB at 5 GHz. This s_{22} value is much better than the s_{22} value obtained in the previous subsection for the single stage PA case. Additionally the power gain (s_{21}) of the power combined PA is shown in Figure 4.22. It can be seen from this figure that the power gain is about 14.3 dB at 5 GHz.



(a)



(b)

Figure 4.20: (a) s_{11} response (b) s_{11} in a logarithmic scale (s_{11} is below -10 between 4.59 – 5.79 GHz bandwidth)

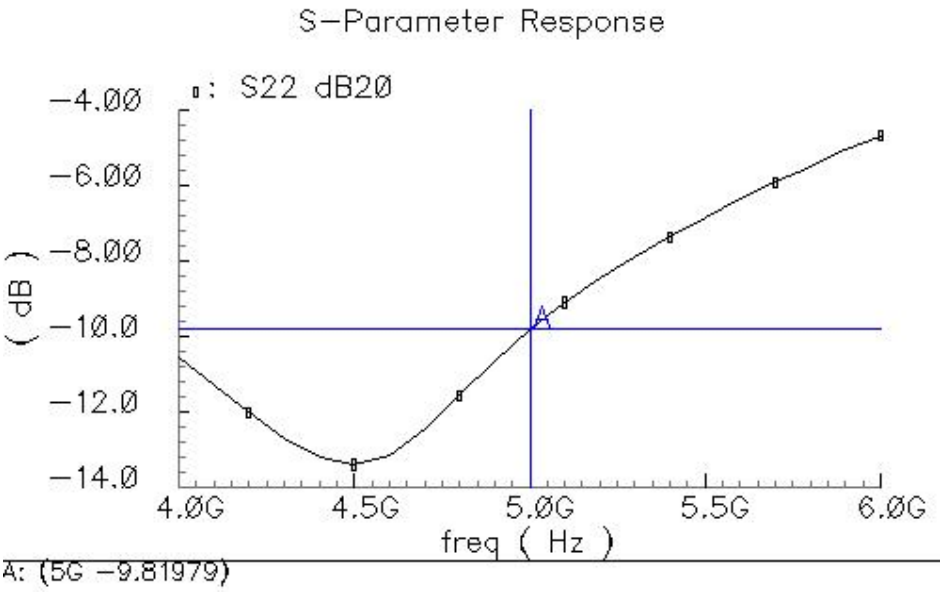


Figure 4.21: s_{22} response

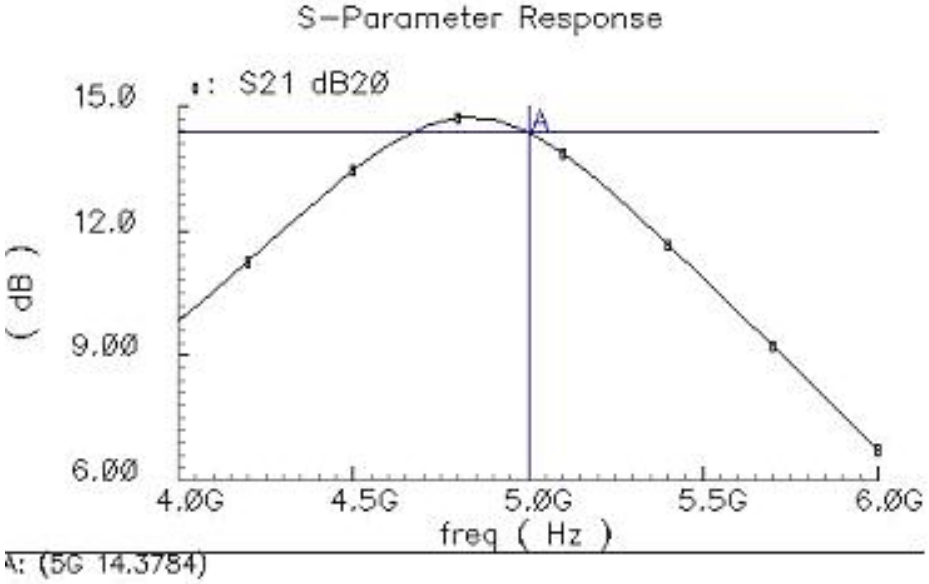


Figure 4.22: Power Gain (s_{21})

4.4 RF Choke Alternative (Transmission Line Structures)

In Chapter 3, theoretical basics of the capacitive loaded microstripline/CPW model are given along with two example models constructed in ADS. In this chapter the same CPW model will be simulated with more realistic coplanar waveguide substrate characteristics. But before presenting those results, Cadence simulation results of the single stage PA circuit shown in Figure 4.23 will be given. In this circuit, RF choke is replaced with a single transmission line. This line is 5000μm in length and it shows an inductance of 4.5 nH at 5 GHz. The reason we inserted a single transmission line model instead of a capacitive loaded coplanar waveguide is that Cadence is unable to solve the capacitive loaded CPW model. This simpler structure is easy to simulate and it shows very similar characteristics to capacitive loaded transmission line model. Thus, simulating this circuit gives us an insight about the behavior of the new RF choke structure under overall PA configuration.

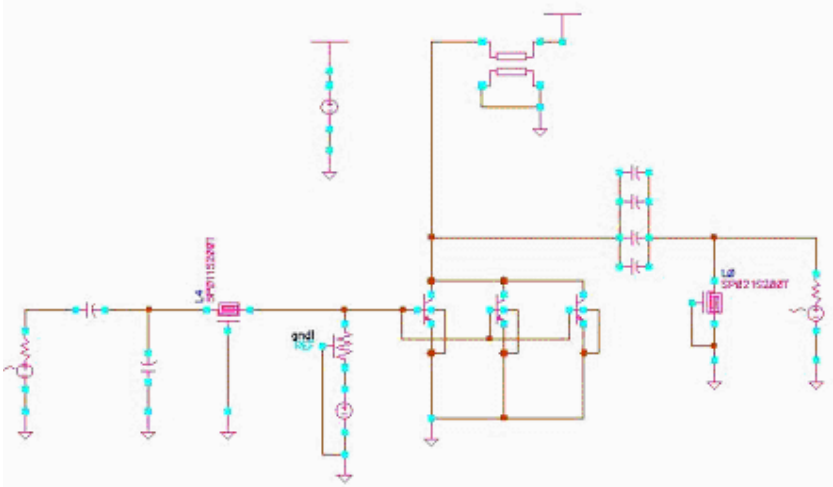


Figure 4.23: Cadence test setup for testing the CPW structure

Since Cadence could not perform periodic steady state (pss) analysis with distributed components, we could not directly obtain input power versus output power plot of the PA circuit shown in Figure 4.23. In order to plot input power versus output power graph, we first performed transient analysis and then obtained the voltage swing at the output. Our aim is to calculate the power at the output from the voltage swing at the output node. With the aid of the calculator tool of Cadence, we took the dft (discrete Fourier transform) of the output voltage waveform for a certain time interval (from 0ns to 10 ns) and a certain number of samples (512). Then, to obtain the output power

spectrum the following mathematical expression is applied to the discrete Fourier transform of the output voltage waveform.

$$PoutSpectrum = dB20\left|dft(outputvoltagewaveform)\right| \tag{4.1}$$

This expression gives the output power spectrum from DC to ~25 GHz frequency range. Since the PA is designed at 5 GHz, the power level at 5GHz is marked. The power level at 5GHz is added up with 10 to obtain the real output power level.

As a result, this mathematical expression gives the output power spectrum. An example of the voltage waveform and the output power spectrum is given in Figure 4.24. This simulation is done with an input power level of -10 dBm.

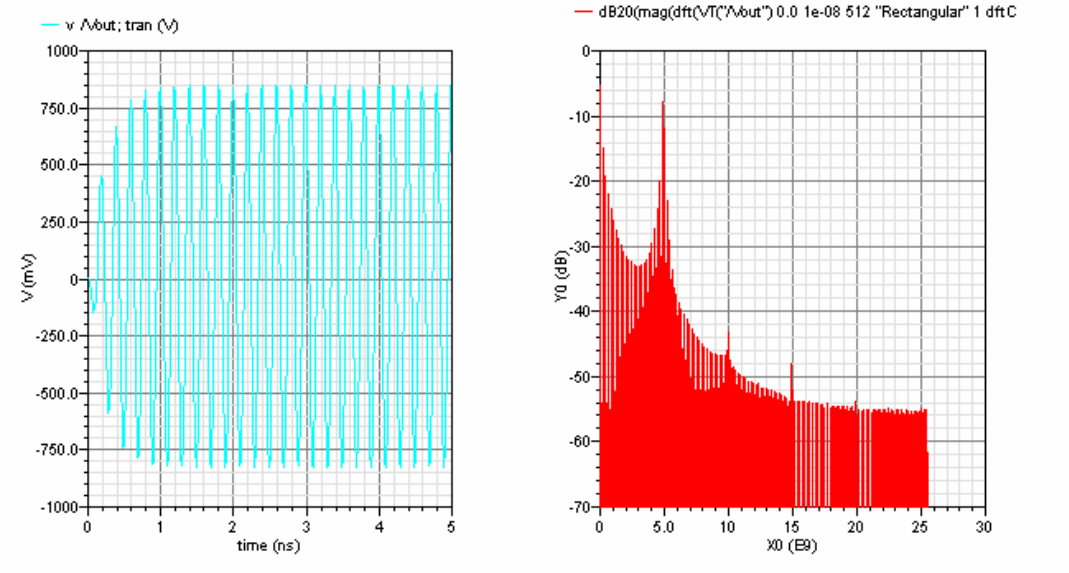


Figure 4.24: Output voltage waveform and power spectrum at -10 dBm input power

These calculations were performed for different input power levels (from -20 dBm to 20 dBm) by taking about 20 data points. After the calculations, input and output referred 1 dB compression points of the PA design in Figure 4.23 are found to be 1 dBm and 16.5 dBm respectively. Thus, the gain at 1 dB compression point is 15.5 dB and the linear gain is 16.5 dB. The overall results of these calculations are given in Figure 4.25. Power added efficiency of 27% is obtained at 1 dB compression point, as shown in Figure 4.26. Finally the s parameter responses are obtained. S_{11} is -19 dB at 5 GHz, and remains below -10 dB from 4.5 GHz to 5.6 GHz, as shown in Figure 4.27. At 5GHz, s_{22}

is -5.8 dB and s_{21} (power gain) is 16.7 dB as shown in Figure 4.28 and Figure 4.29, respectively.

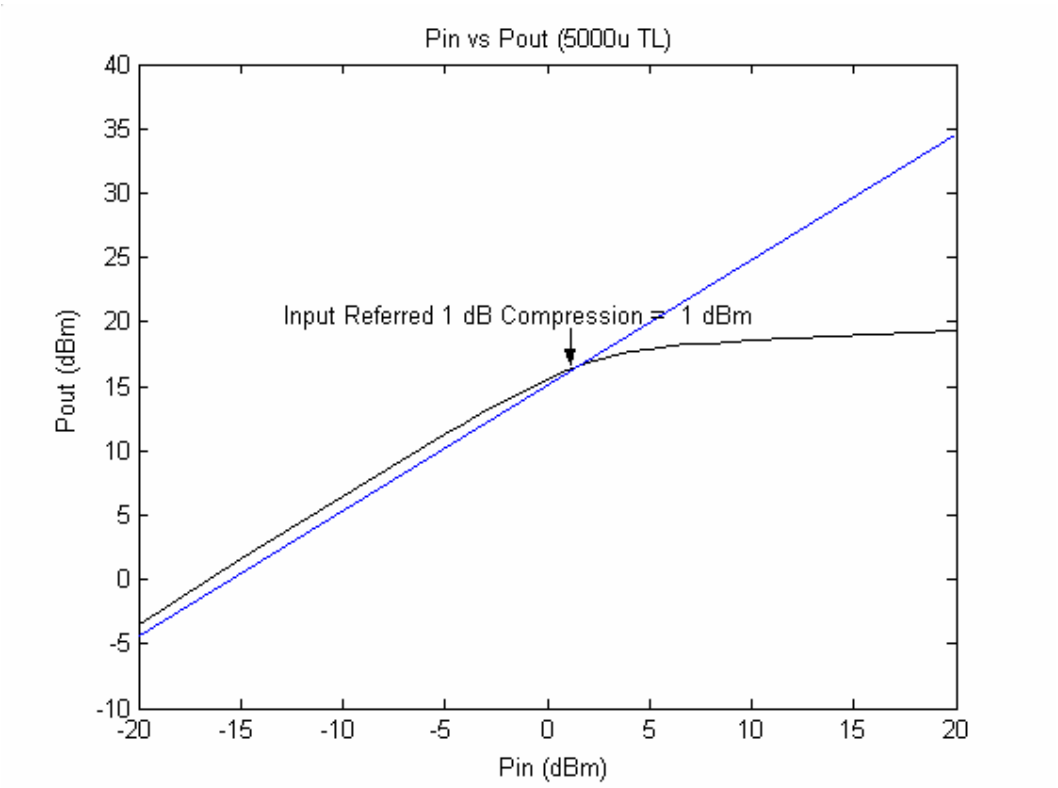


Figure 4.25: Input referred 1 dB compression point (Gain=15.5 dB at 1 dB compression point)

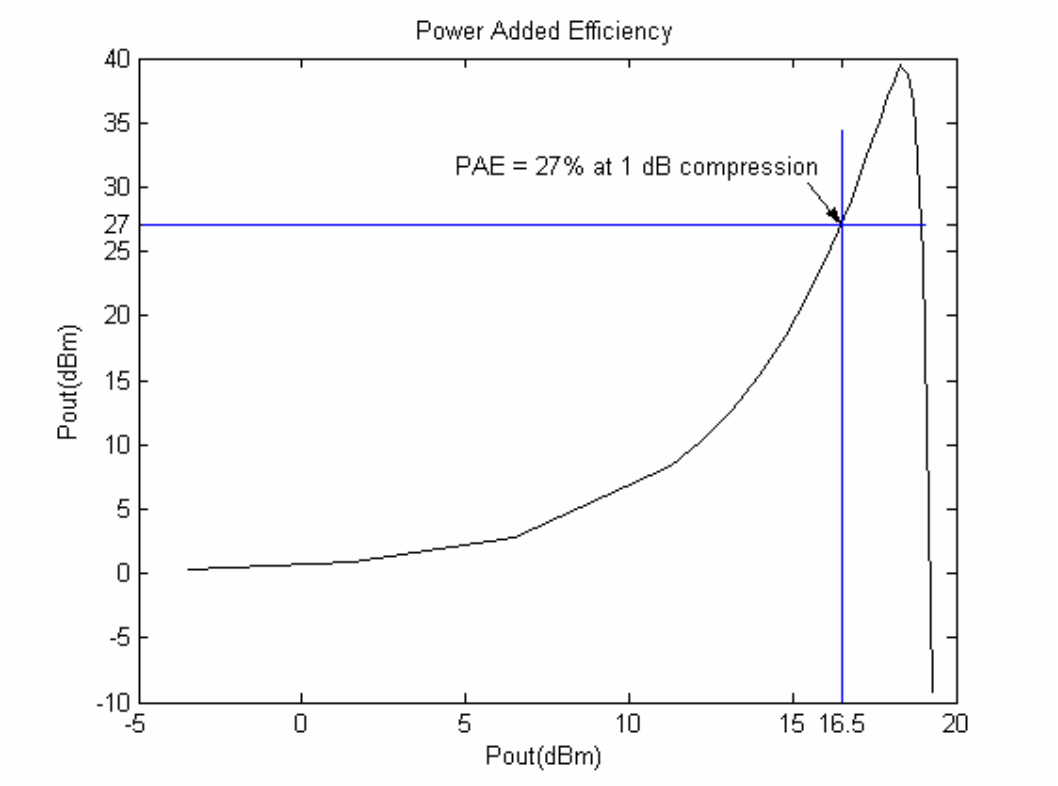
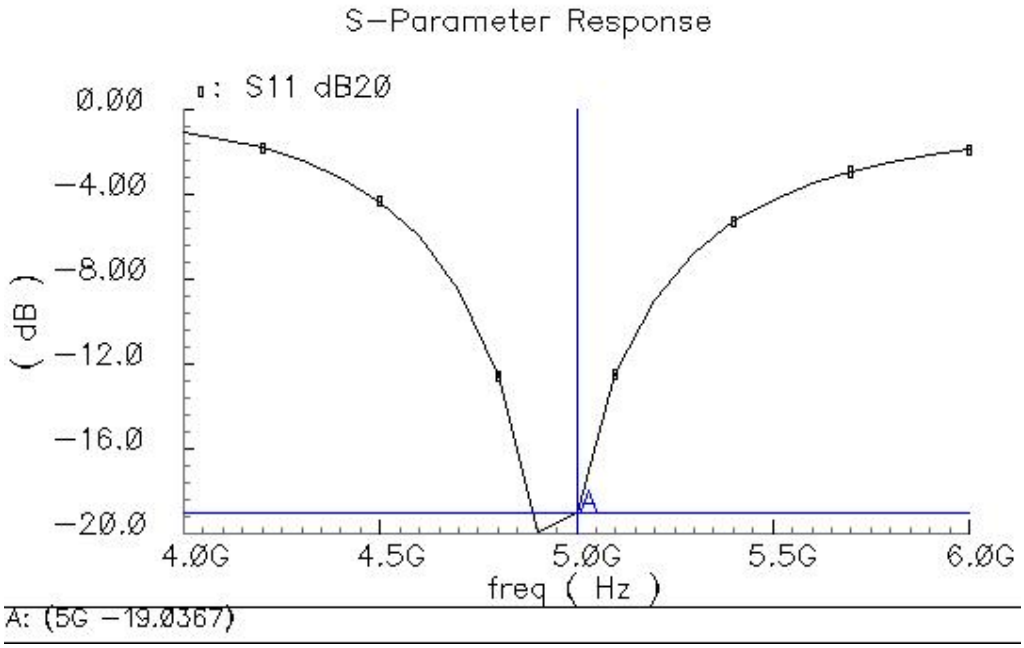
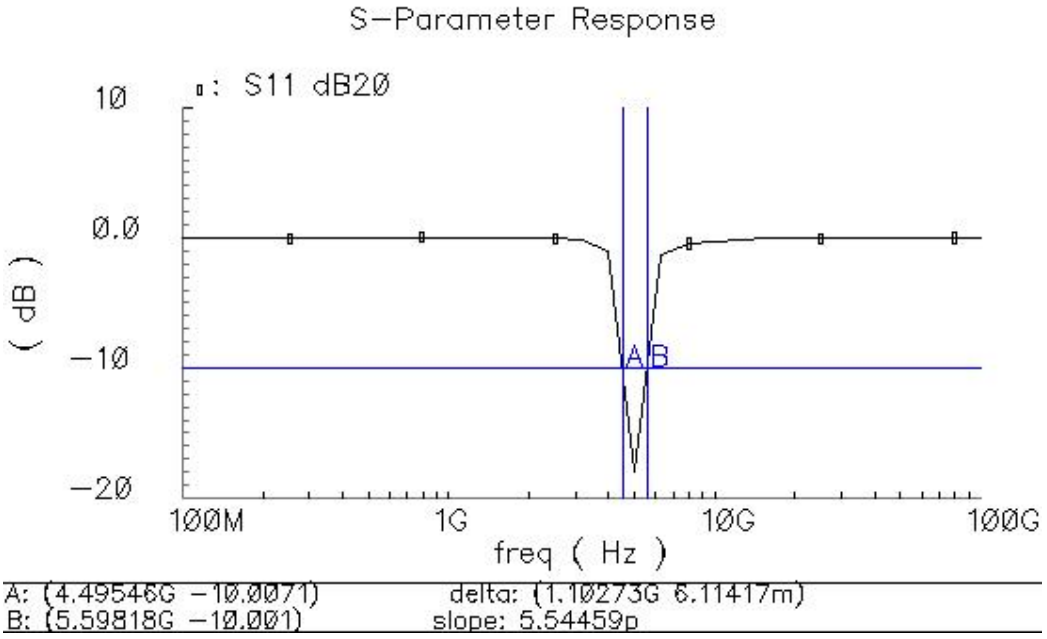


Figure 4.26: Power added efficiency



(a)



(b)

Figure 4.27: (a) s_{11} response (b) s_{11} in a logarithmic scale (s_{11} is below -10 dB from 4.5 GHz to 5.6 GHz)

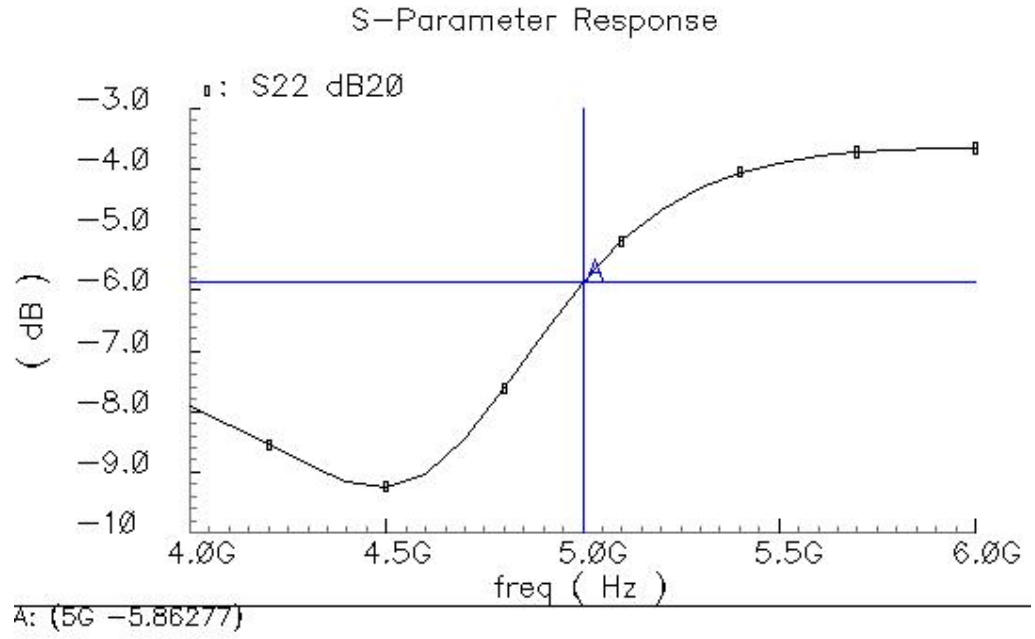


Figure 4.28: s_{22} response

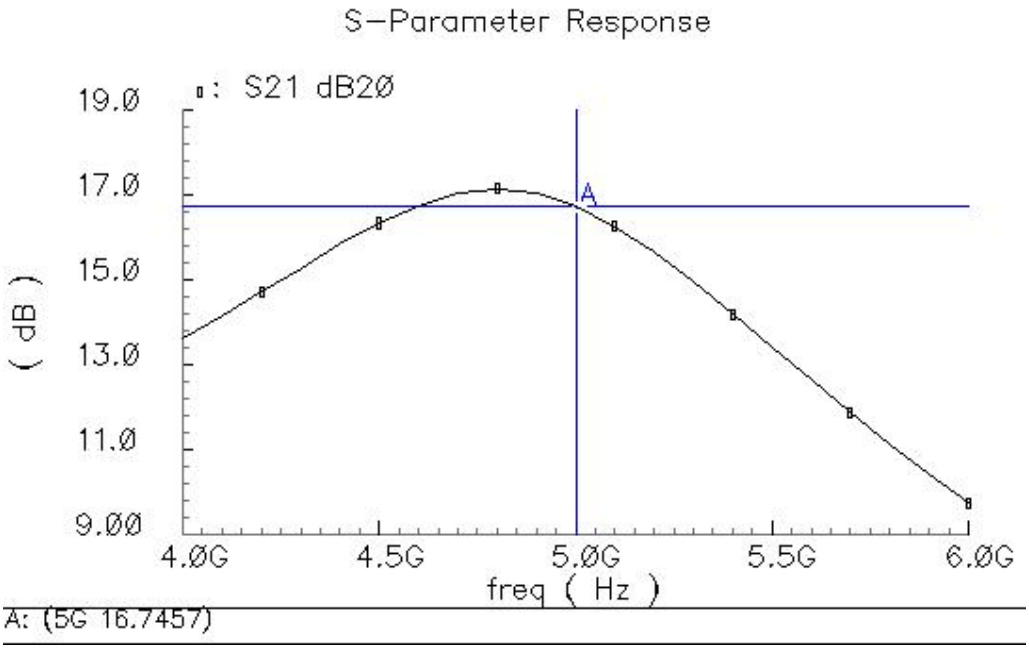


Figure 4.29: Power Gain (s_{21})

CPW structure was realized using thick upper layer (MET4) for the signal line. In order to find the conductor (MET4) conductivity, we referred to the sheet resistance values from AMS's design parameters. For the MET4 layer, typical sheet resistance is 10 mohm/square and the maximum sheet resistance is 15 mohm/square. The electrical conductivity of MET4 can be found from the following formulas.

$$R = \frac{\rho L}{A} \tag{4.2}$$

$$\sigma = \frac{1}{\rho} = \frac{L}{R * A} \tag{4.3}$$

where R is the electrical resistance, ρ is the resistivity, L is the length, A is the cross section area of the conductor (A=L*T) and σ is the electrical conductivity. The MET4 thickness (T) is about 3.1 μm and typical sheet resistance of MET4 layer is 10 mohm/ square. Inserting these values into the conductivity expression, we obtain:

$$\sigma = \frac{L}{10 * 10^{-3} * L * 3.1 * 10^{-6}} = \frac{1}{3.1 * 10^{-8}} = 3.2 * 10^{7} \text{ siemens/meter} \tag{4.4}$$

Using this conductivity value ($3.2*10^7$ siemens/meter) we modified the capacitive loaded CPW model example which is given in Chapter 3.7.3. The new version of this model with more realistic conductor conductivity value is shown in Figure 4.30. Here CPWSub defined the coplanar waveguide substrate characteristics.

All the values are realistic since they are in accord with the AMS 0.35 µm SiGe BiCMOS process characteristics. In Figure 4.30, a single CPW with a length of 1600 µm, gap of 15 µm and width of 10 µm is connected in parallel with a capacitor of 1.19 pF. Reducing the capacitances and extending the length of the CPW were unavoidable, because the conductivity is dropped from $1*10^{15}$ to $3.2*10^{7}$ siemens/meter.

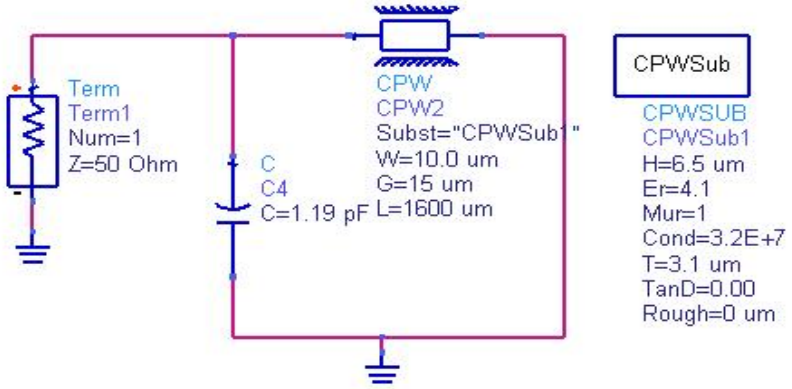


Figure 4.30: Modified CPW structure

As given in Figure 4.31, this CPW structure provides an inductance of about 3 nH at 5 GHz. However, the quality factor is not exceeding 1.

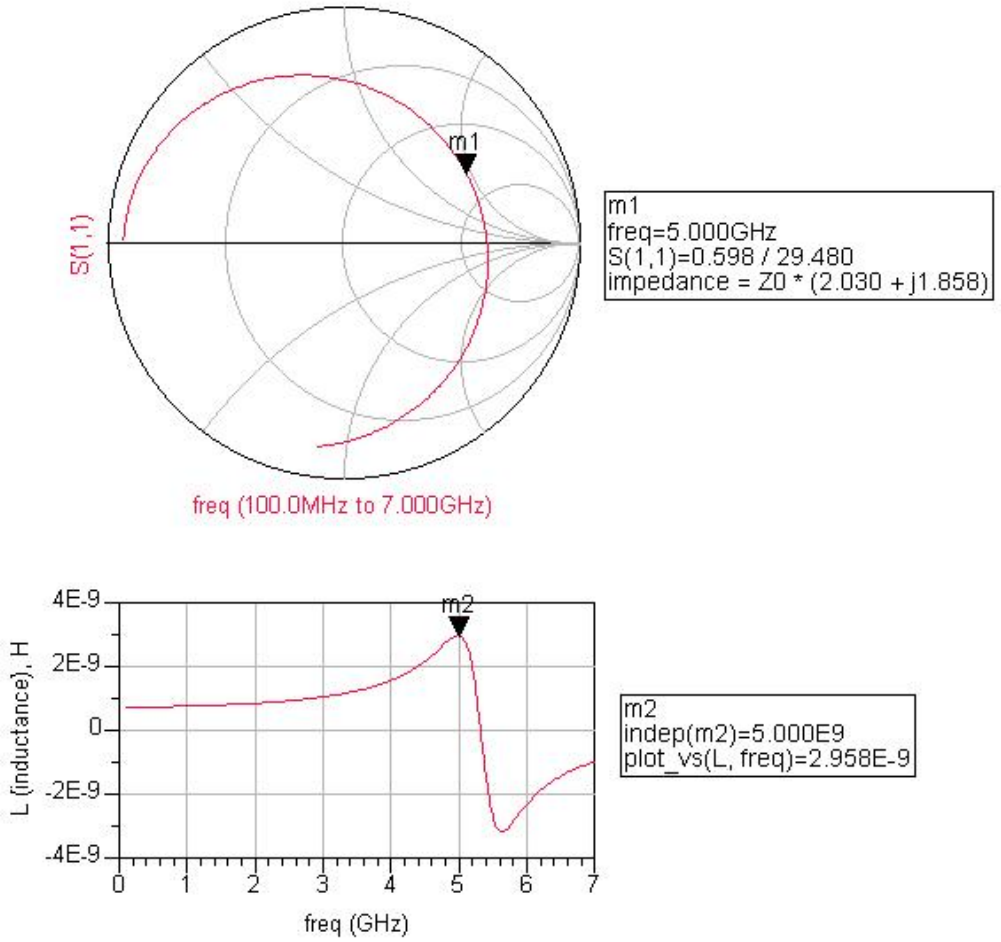


Figure 4.31: Inductance of the CPW structure in Figure 4.33

Keeping all parameters the same except the Gap (G) width of the coplanar waveguide and the shunt capacitance, higher inductance values can be obtained while trading off the quality factor. This is possible by increasing the Gap width from 15 μm to 30 μm and reducing the capacitance from 1.19 pF to 0.95 pF. ADS simulation setup and the simulation results of this structure are given in Figure 4.32 and Figure 4.33, respectively. Figure 4.34 shows the layout of the single stage PA circuit with the CPW structure inserted.

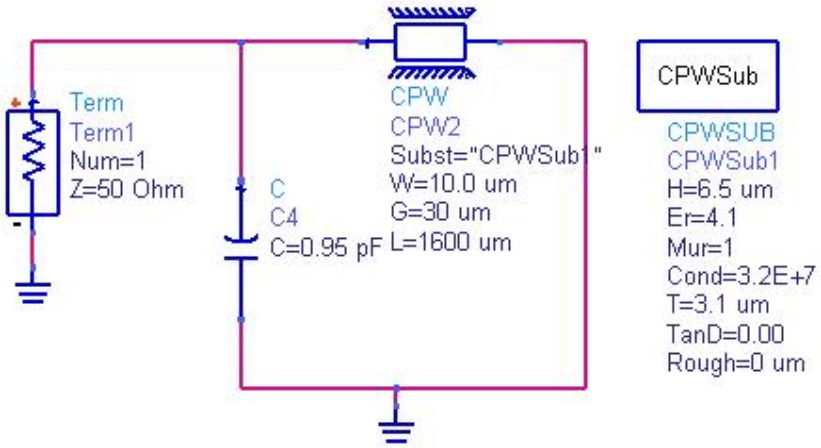


Figure 4.32: CPW structure

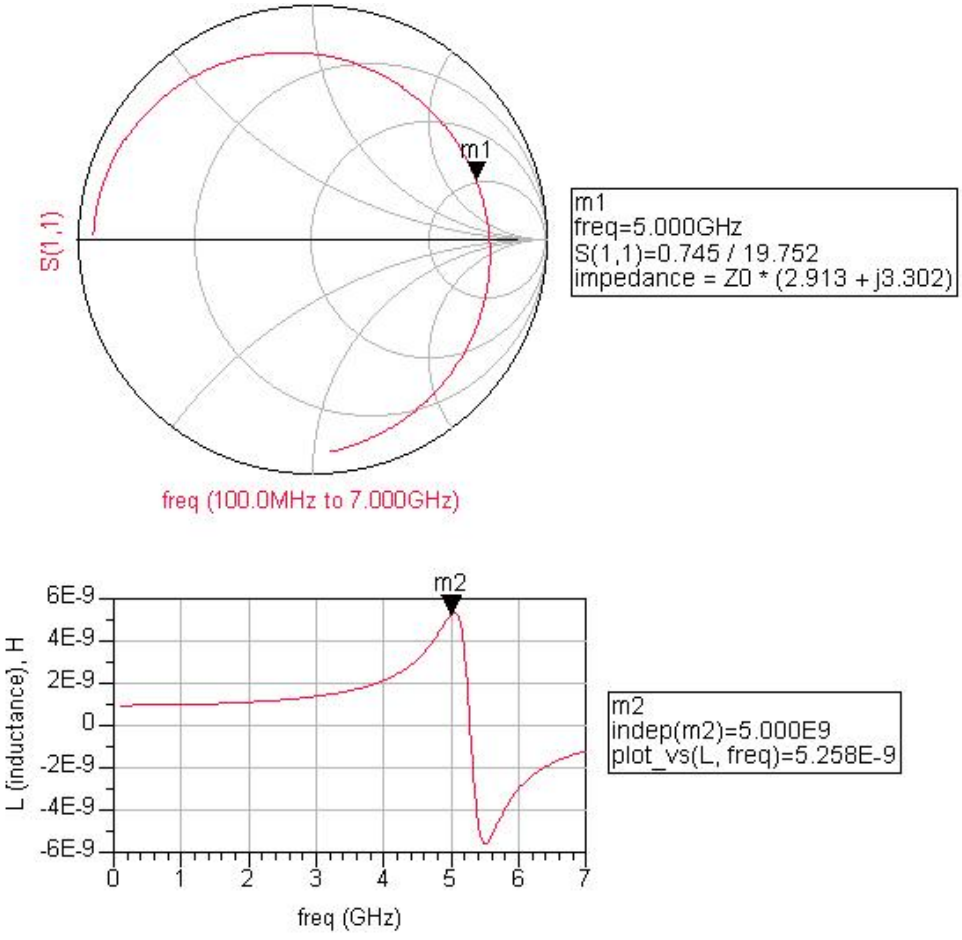


Figure 4.33: Inductance of the CPW Structure in Figure 4.35

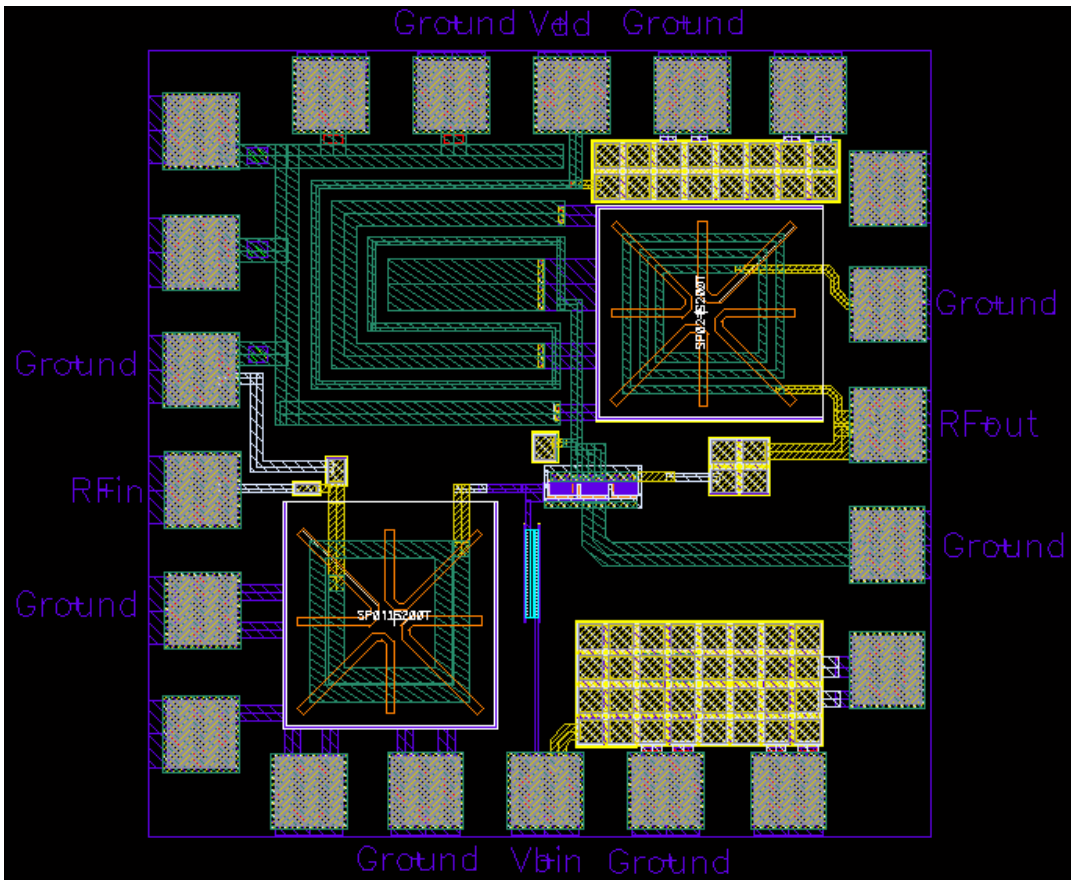


Figure 4.34: Layout of the single stage PA with the CPW Structure in Figure 4.35

Chapter 5

5 CONCLUSIONS AND FUTURE WORK

Ever since the IEEE 802.11a standards have extended the frequency band from 2.4 GHz to 5 GHz frequency bands, the new generation of 802.11a Wireless LAN standard is becoming popular due to high speed, greater system capacity, low interference and less congestion.

In this thesis, we presented the design of a power amplifier, which is one of the most challenging components in transceiver architecture. The PA is designed in AMS 0.35μm SiGe BiCMOS technology for IEEE 802.11a Wireless LAN standard, actually for the lowest frequency band allocated for this standard.

The PA is a single stage Class A design and uses three npn HBT transistors in parallel in order to achieve an output power level of 40 mW, which is the maximum required output power level as specified for the lowest frequency band of 802.11a standard. Since the SiGe devices capable of operating at 5 GHz have a low collector emitter breakdown voltage, it is difficult to extract high output power from a single transistor. This can be overcome by using power combining techniques. Accordingly, this idea is tested and implemented by combining two single stage PAs via on-chip Wilkinson power combiner to obtain higher output power levels. Also in order to decrease the conductor and dielectric substrate losses of low Q inductors and also to decrease the die area, idea of using capacitively coupled transmission line model instead of low Q inductors is implemented.

As a future work, the on-chip Wilkinson power combining technique can be extended. In this thesis we concentrated on combining only two single stage power amplifiers, but this method can be applied to N numbers of PAs. The layout of the combined PA topology can also be drawn and fabricated. Also, the post layout simulations of the layout given in this thesis can be done and those circuits can be

fabricated. Additionally, idea of using capacitively loaded transmission lines as an inductor can be investigated in more detail. In this work, we developed this idea but as a future work, the exact values of shunt capacitors and the lengths of the transmission lines in this structure can be found in order to obtain high inductances with better quality factors.

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APPENDIX

Appendix A

WLAN Channel Model

Description channel model
Library WLAN, Channel
Class TSDFWLAN_ChannelModel
Derived From channel
Required Licenses

Parameters

Name	Description	Default	Type	Range
Algorithm	fading algorithm: Jakes, NoiseFilter	NoiseFilter	enum	
ModelType	fading model: NoMultipath, A, B, C, D, E, UserDefined	A	enum	
PathNumber	number of multipath echoes, effective only when ModelType is set as UserDefined	4	int	[1, 150]
PowerArray	average relative power of path array, in dB, effective only when ModelType is set as UserDefined	0.0 -14 -18 -20	real array	(-∞, ∞)
DelayArray	delays associated with path array, in nsec, effective only when ModelType is set as UserDefined	0.0 56 106 185	real array	[0, ∞)
FadingType	fading type of first path, effective only when ModelType is set as UserDefined: Rayleigh, Ricean	Rayleigh	enum	
RiceanFactor	Ricean factor, effective only when ModelType is set as UserDefined and FadingType is set as Ricean	10	int	[1, ∞)
Seed	integer number to randomize channel output(Jakes model)	1234567	int	(-∞, ∞)
N	number of oscillators in Jakes model	80	int	(PathNumber, ∞)
Pathloss	option for inclusion of large-scale pathloss: No, Yes	No	enum	
Env	environment type options:	TypicalUrban	enum	

Pin Inputs

Pin	Name	Description	Signal Type
1	input	channel input signal	timed

Pin Outputs

Pin	Name	Description	Signal Type
2	output	channel output signal	timed

Notes/Equations

1. The multipath delay profile determines the frequency selective nature of the channel. Delay profile is specified by the user via the ModelType, DelayArray and PowerArray parameters.
2. This component is used to simulate a multi-path fading channel based on a tapped-delay line model. Each firing, one token is consumed at the input pin, and one token is produced at the output pin.
3. The fading type of the first path can be Rayleigh or Ricean; if FadingType= Ricean, RiceanFactor determines the power ratio of the direct signal to all other indirect signals.
4. ModelType = A, B, C, D or E, the PathNumber, DelayArray, FadingType, and Ricean Factor parameters are automatically set.

   If ModelType = UserDefined, the user determines channel characteristics by setting these parameters

   If ModelType = NoMultipath, only Doppler frequency shift is incorporated.
5. The delay spread is modeled via a tapped delay line where the number of taps is based on the size of DelayArray and PowerArray. In each case the input signal is delayed and the carrier phase due to the delay signal is incorporated. Figure A.1 illustrates this modeling process when connected to a simple antenna.

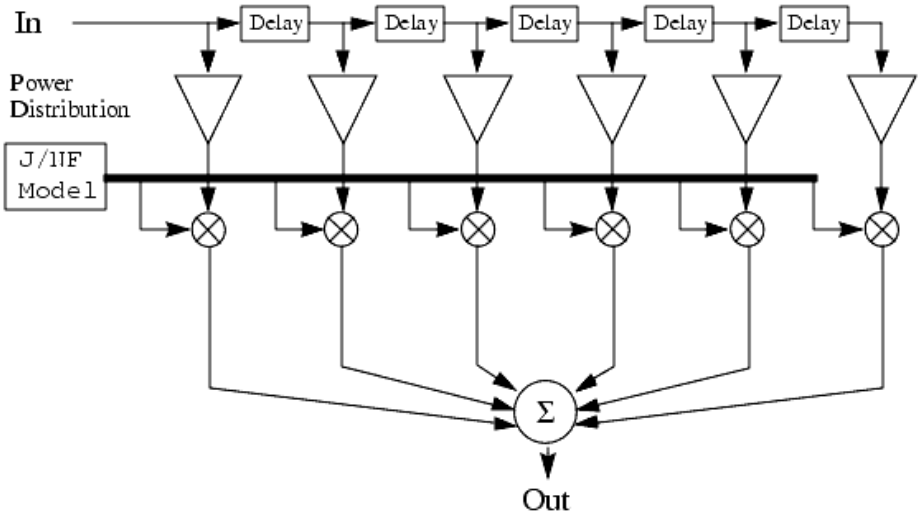


Figure A.1: Delay and Doppler Spread and Carrier Phase Shift

6. If Delay Array values are not the time as Tstep, the interpolation is made to gain this point of signal and a delay of 64 tokens is introduced.

7. For each tap, Jakes model or noise filter model provides Doppler spectrum as well as the fading channel specifications. Jakes model uses N_0 low frequency oscillators to generate a fading waveform.

8. If speed is zero, the channel is time invariant. However, multipath still exists so a static channel is applied and each tap is a complex constant value. The complex constant value is randomly generated and can be changed by changing the Seed parameter.

9. Five model types have been designed:

- Model A corresponds to a typical office environment.
- Model B corresponds to a typical large open space environment with NLOS conditions or an office environment with a large delay spread.
- Model C and E correspond to typical large open space indoor and outdoor environments, respectively with a large delay spread.
- Model D corresponds to LOS conditions in a large open space indoor or outdoor environment.

Characteristics of these models are listed in Table A.1 through Table A.5.

Tap Number	Delay(ns)	Average Relative Power	Ricean K	Doppler Spectrum
1	0	0.0	0	Class
2	10	-0.9	0	Class
3	20	-1.7	0	Class
4	30	-2.6	0	Class
5	40	-3.5	0	Class
6	50	-4.3	0	Class
7	60	-5.2	0	Class
8	70	-6.1	0	Class
9	80	-6.9	0	Class
10	90	-7.8	0	Class
11	110	-4.7	0	Class
12	140	-7.3	0	Class
13	170	-9.9	0	Class
14	200	-12.5	0	Class
15	240	-13.7	0	Class
16	290	-18.0	0	Class
17	340	-22.4	0	Class
18	390	-26.7	0	Class

Table A.1: Model A, typical office environment with NLOS conditions and 50ns average rms delay spread

Tap Number	Delay(ns)	Average Relative Power	Ricean K	Doppler Spectrum
1	0	-2.6	0	Class
2	10	-3.0	0	Class
3	20	-3.5	0	Class
4	30	-3.9	0	Class
5	50	0.0	0	Class
6	80	-1.3	0	Class
7	110	-2.6	0	Class
8	140	-3.9	0	Class
9	180	-3.4	0	Class
10	230	-5.6	0	Class
11	280	-7.7	0	Class
12	330	-9.9	0	Class
13	380	-12.1	0	Class
14	430	-14.3	0	Class
15	490	-15.4	0	Class
16	560	-18.4	0	Class
17	640	-20.7	0	Class
18	730	-24.6	0	Class

Table A.2: Model B, typical large open space and office environments with NLOS conditions and 100ns average rms delay spread

Tap Number	Delay(ns)	Average Relative Power	Ricean K	Doppler Spectrum
1	0	-3.3	0	Class
2	10	-3.6	0	Class
3	20	-3.9	0	Class
4	30	-4.2	0	Class
5	50	0.0	0	Class
6	80	-0.9	0	Class
7	110	-1.7	0	Class
8	140	-2.6	0	Class
9	180	-1.5	0	Class
10	230	-3.0	0	Class
11	280	-4.4	0	Class
12	330	-5.9	0	Class
13	400	-5.3	0	Class
14	490	-7.9	0	Class
15	600	-9.4	0	Class
16	730	-13.2	0	Class
17	880	-16.3	0	Class
18	1050	-21.2	0	Class

Table A.3: Model C, typical large open space environment with NLOS conditions and 150ns average rms delay spread

Tap Number	Delay(ns)	Average Relative Power	Ricean K	Doppler Spectrum
1	0	0.0	10	Class+spike
2	10	-10.0	0	Class
3	20	-10.3	0	Class
4	30	-10.6	0	Class
5	50	-6.4	0	Class
6	80	-7.2	0	Class
7	110	-8.1	0	Class
8	140	-9.0	0	Class
9	180	-7.9	0	Class
10	230	-9.4	0	Class
11	280	-10.8	0	Class
12	330	-12.3	0	Class
13	400	-11.7	0	Class
14	490	-14.3	0	Class
15	600	-15.8	0	Class
16	730	-19.6	0	Class
17	880	-22.7	0	Class
18	1050	-27.6	0	Class

Table A.4: Model D, typical large open space environment with LOS conditions and 150ns average rms delay spread; a 10 dB spike at zero delay has been added resulting in an rms delay spread of approximately 140ns

Tap Number	Delay(ns)	Average Relative Power	Ricean K	Doppler Spectrum
1	0	-4.9	0	Class
2	10	-5.1	0	Class
3	20	-5.2	0	Class
4	40	-0.8	0	Class
5	70	-1.3	0	Class
6	100	-1.9	0	Class
7	140	-0.3	0	Class
8	190	-1.2	0	Class
9	240	-2.1	0	Class
10	320	0.0	0	Class
11	430	-1.9	0	Class
12	560	-2.8	0	Class
13	710	-5.4	0	Class
14	880	-7.3	0	Class
15	1070	-10.6	0	Class
16	1280	-13.4	0	Class
17	1510	-17.4	0	Class
18	1760	-20.9	0	Class

Table A.5: Model E, typical large open space environment with NLOS conditions and 250ns average rms delay spread

Appendix B

High Voltage HBT Module Parameters (npn254h5)

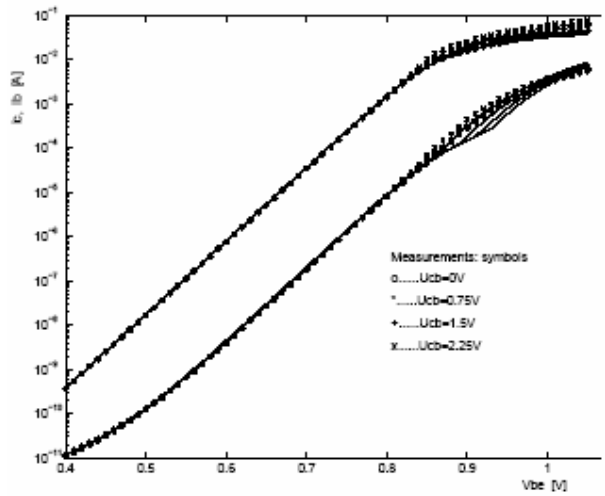


Figure A.2: Gammel Plots of a bipolar transistor (npn254h5; 24µm emitter length)

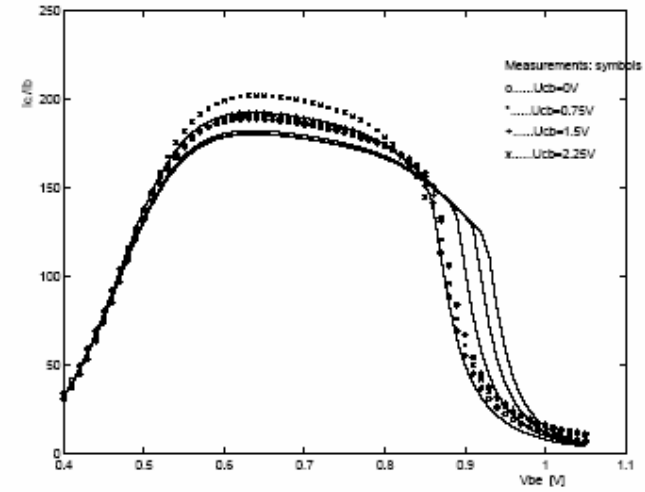


Figure A.3: Beta plots of a bipolar transistor (npn254h5; 24µm emitter length) for a typical wafer

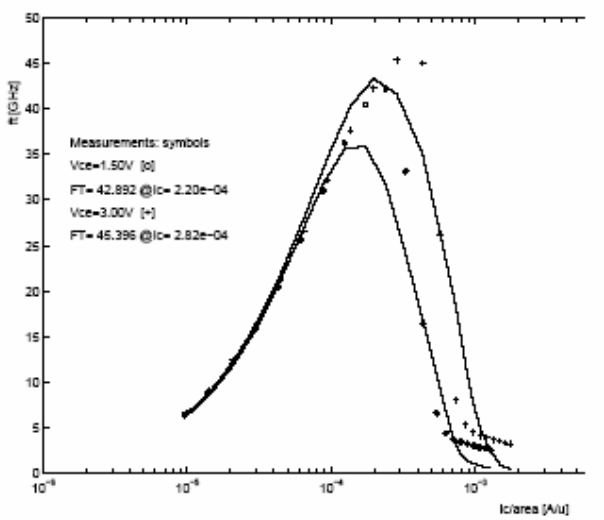


Figure A.4: Ft plots of a bipolar transistor (npn254h5; 12µm emitter length) for a typical wafer

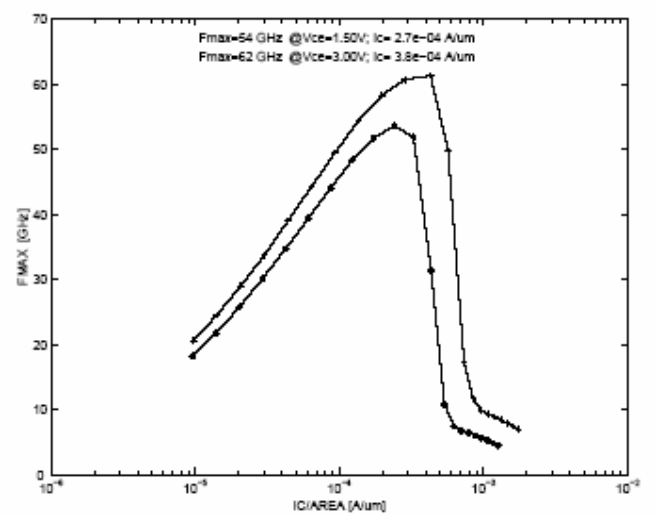


Figure A.5: Fmax plots of a bipolar transistor (npn254h5; 12µm emitter length) for a typical wafer

Main Parameters of Thick Metal Inductors

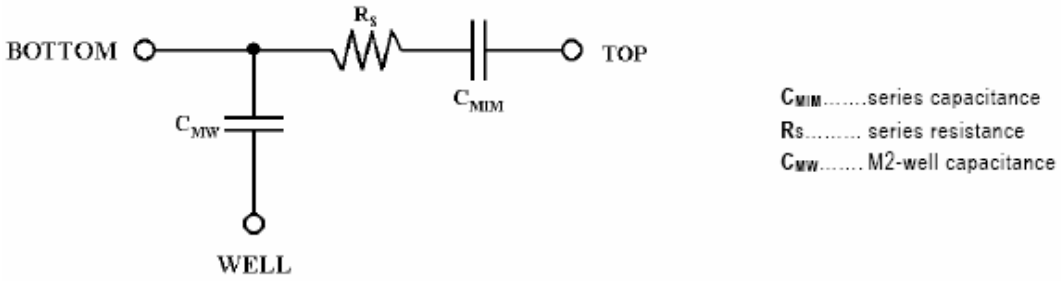
Inductor	Inductance [nH]			Qmax	Q		fRES [GHz]
	Ls	@2.4GHz	@5.0GHz		@2.4GHz	@5.0GHz	
SP011S200T	1.07	1.04	1.05	11.9@4.4GHz	8.7	11.8	>6
SP015S250T	1.52	1.49	1.58	11.7@3.9GHz	9.6	10.2	>6
SP020S250T	2.02	2.04	2.17	10.4@3.9GHz	7.9	9.8	>6
SP021S200T	2.10	2.10	2.20	9.9@3.9GHz	7.8	9.3	>6
SP024S250T	2.42	2.42	2.75	9.6@2.70GHz	9.3	6.5	>6
SP031S250T	3.07	3.17	3.63	8.9@3.0GHz	8.4	6.6	>6
SP033S150T	3.25	3.32	3.52	9.4@4.33GHz	6.9	9.0	>6
SP037S250T	3.67	3.82	4.58	9.4@2.70GHz	9.0	6.2	>6
SP047S250T	4.66	4.90	5.98	8.3@3.7GHz	7.2	6.4	>6
SP049S300T	4.85	5.30	8.13	8.8@2.46GHz	8.6	3.7	>6
SP060S300T	6.00	6.59	10.09	7.2@3.0GHz	6.8	4.3	>6
SP073S250T	7.25	8.11	12.20	7.7@2.5GHz	7.5	3.2	>6
SP100S250T	10.02	12.08	19.23	7.2@2.0GHz	6.8	1.1	6
SP133S300T	13.30	19.06	-	6.7@1.7GHz	5.5	-	4.3

Table A.6: Extracted L, Qmax and resonance frequencies of thick metal inductors

Metal-Metal Capacitor (CMIM)

The metal metal capacitor is built up of: METALC (top-plate) – insulator (silicon nitride) – METAL2 (bottom plate). Capacitors with values ranging from 0.1 pF to 1 pF were measured. Based on theoretical calculations the series resistance lies in the order of 0.1 Ω resulting in quality factors of significantly exceeding 100.

Subcircuit model of the MIM capacitor:



The major Q limiting factor is the top plate contact resistance.

The model is valid in the following range:

Frequency range: up to 6 GHz

Capacitance range: 0.1 pF to 1 pF

Well terminal (n well) connected to the substrate or AC ground (e.g. Vcc)

Measured and simulated series capacitance and normalized impedance: