Realization of a Low Noise Amplifier using 0.35 μm SiGe-BiCMOS Technology for IEEE 802.11a Applications

by

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Realization of a Low Noise Amplifier using 0.35 μm SiGe-BiCMOS Technology for IEEE 802.11a Applications

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Abstract

The trend demand for towards interactive multimedia services has forced the development of new wireless systems that has greater bandwidths. The evolution of current wireless communication systems has been very rapid. The main goal has been small-size and low-cost transceivers that can be designed for different applications.

Data communication systems in compliant with IEEE 802.11a wireless local area network (WLAN) standard has found widespread use, meeting the market demands, for the last few years. Next generation WLAN operates in the 5-6 GHz frequency range. A front-end receiver capable of operating within this frequency range is essential to meet the current and future of products. One of the critical components, allowing the common use of the technology can be attributed to the high performance Low Noise Amplifiers (LNA) in the receiver chain of the 802.11a transceivers. In IEEE 802.11a, there are three frequency bands; 5.15GHz - 5.25GHz, 5.25GHz - 5.35GHz and 5.725GHz - 5.825GHz.

In this thesis, we designed and fabricated a single-stage cascode amplifier with emitter inductive degeneration using 0.35 μm-SiGe BiCMOS process for IEEE 802.11a receivers. The electromagnetic (EM) simulations of the passive components are performed by using Agilent MOMENTUM® tool and all the parasitic components are extracted and compensated, a crucial step for optimizing the performance parameters of the LNA. The simulation results are very similar to measurement results, confirming the effectiveness of design methodology provided in this work.

Özet

Günümüzde, çoklu ortam iletişim uygulamalarına olan ilginin artması sonucunda, yeni telsiz iletişim sistemlerine olan araştırma eğilimi giderek artmaktadır. Bu sistemlerin sahip olduğu yüksek bant genişliği, bu alana olan yönelimin en önemli sebebidir. Yeni kuşak *telsiz yerel alan ağı* (WLAN) uygulamalarının çalışma frekans aralığı, 5–6 GHz frekans bandı olarak belirlenmiştir. Bir ön-uç alıcı yapısının sahip olması gereken özellikler, bu alıcının çalışacağı protokol tarafından belirlenmektedir. Alıcının, belirli olan bu protokolde çalışabilmesi için, protokol tarafından belirlenen bir takım özelliklere sahip olması gerekmektedir. Düşük gürültülü kuvvetlendirici (LNA) bloğu, WLAN uygulamalarından biri olan IEEE 802.11a protokolünde çalışması gereken bir alıcının, içerdiği bloklar içerisinde en önemli olanlardan biridir. IEEE 802.11a standardında üç tane frekans bandı kullanılmaktadır; 5.15GHz - 5.25GHz, 5.25GHz - 5.35GHz ve 5.725GHz - 5.825GHz. Genellikle, telsiz iletişiminde alıcı için her zaman birincil öneme sahip özellik, düşük gürültü olması değil, taşınabilirlik açısından daha düşük güç tüketimi olmaktadır.

Bu makalede, Austria Micro Systems (AMS) 0.35µm SiGe BiCMOS teknolojisi kullanılarak 5–6 GHz bandındaki WLAN uygulamalarına uyumlu, düşük güç tüketimi ve düşük gürültü sayısına sahip olan LNA tasarımı ve ölçüm sonuçları sunulmaktadır. LNA tasarımı için tek katlı, kaskot, endüktif emetör dejenerasyonuna sahip kuvvetlendirici topolojisi kullanılmıştır. Kırmık-içi endüktans tasarımının zorluğu ve günümüz teknolojilerinde gerçeklenen endüktans yapılarının performanslarının yeterli olmamasına çözüm olarak, RF-MEMS teknolojisi kullanılarak alternatif daha yüksek performanslı devreler oluşturulabileceği gösterilmiştir. Ayrıca, bu devre ile uyumlu, RF-MEM endüktör, tasarlanmış ve üretilmiştir. Ölçümler sonucunda, tüm pasif elemanları kırmık içerisinde olan, 14 dB kazancı ve giriş-çıkış dönüş kaybı -15 dB den daha düşük olan LNA bloğu, 10.6 mW güç harcaması ile elde edilmiştir. Gürültü ölçümleri ve RFMEMS endüktörlerle olan birleşim işlemleri ise devam etmektedir.

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Chapter 1

INTRODUCTION

1.1 Motivation and Research Goals

The trend demand for towards interactive multimedia services has forced the development of new wireless systems that has greater bandwidths. The evolution of current wireless communication systems has been very rapid. The main goal has been small-size and low-cost transceivers that can be programmed for different applications. Future communications systems will offer new wireless services for devices such as laptops and PDAs as well as increase on the existing wireless capabilities of devices such as cellular telephones and pagers. These applications include internet accessing services, video teleconferencing, high-fidelity audio transmission, and other high-speed services.

Wireless connectivity is not limited to only portable devices. It can also be used for applications including local area networks (LANs) and local loop applications such as Integrated Services Digital Network (ISDN) and Digital Subscriber Line (DSL), both of which rely on copper twisted pair, as well as cable applications, which rely on a combination of fiber optic and coaxial cables. Bluetooth is one example of a wireless standard which is targeted at applications which currently rely on wires. Emerging

wireless solutions for LAN applications include the IEEE 802.11a and 802.11b standards at 5 GHz and 2.4 GHz, respectively, in the United States as well as the ETSI HIPERLAN standards in Europe [1].

The performance of these systems will depend closely on their ability to provide high capacity while maintaining low cost, small form factor, and low power consumption in the portable units. However, many existing commercial transceivers are expensive, consist of a large number of discrete components, and exhibit moderate to high levels of power consumption. To increase the performance of the transceiver architectures, designers started to find a new ways to perform it. One popular way for improving the performance of Radio Frequency Integrated Circuits (RFICs) is using the Micro Electro Mechanical System (MEMS) technology. Using MEM devices, it can be possible to realize the transceiver on a single chip which includes the RF front-end and intermediate frequency blocks.

One of the most challenging building blocks in multi-mode receivers is the low-noise amplifier (LNA). In order to increase the overall performance of the receiver, LNA should be designed carefully. The tricky part to improve the performance of the LNA is passive components that are used in the input and output matching networks. Achieving high performance passive components is not possible in typical BiCMOS processes. In this work, a low noise amplifier (LNA) is designed and fabricated using Austria Micro Systems (AMS) 0.35 μm SiGe BiCMOS process. Some test structures are also fabricated to integrate the MEM Inductors which are fabricated in Sabanci University Clean-Room. The main goal is improving the performance of LNA using MEM passive structures. The measurement of LNA and fabrication of inductors are finished and will be presented in this thesis. The measurement and integration of MEM inductors to LNA block is assigned to future work.

1.2 Organization of the Thesis

In Chapter 2, an introduction to the RF fundamentals is given. These fundamentals include noise and linearity background, the system specifications, and receiver architectures. Therefore, it is important to understand the basic concepts and limitations. Furthermore, this helps the designer in implementing and combining multiple systems on a single chip because of the effects of the one stage to another.

Chapter 3 describes the LNA design and concentrates on the important design challenges. The main emphasis is on justifying why an inductively-degenerated LNA is chosen as the basis and the advantages of this topology. The LNAs in this thesis are targeted on heterodyne transceiver type. Thus, the design aspect of the LNA-filter interface is also considered in this chapter and the output of the LNA is matched to 50 Ω. The design of low-value inductor also explained in this chapter. At the end of the chapter, the measured results are given and they are compared to simulated ones.

Chapter 4 gives a general theory about planar inductors and concentrates on the design of MEM inductor. This chapter also explains the Above-IC concept and gives the process steps of this technology. The design and fabrication of MEM inductors are included in this chapter. The measurements of these inductors are still on going and with the integration of these inductors to LNA work is also assigned to future work of this thesis.

Finally the last chapter contains a summary and some suggestions for future work.

2

Chapter 2

RF FUNDAMENTALS

2.1 Introduction

The goal of this chapter is to provide the important definitions about RF circuit design. These definitions are the basic concepts that have to be known before trying to understand the RF electronics. The design of RF circuits strongly requires a background in these topics. Hence, the following chapters are related to the basic concepts of RF electronics which can be sorted as noise, sensitivity, linearity, interference and impedance matching parts.

2.2 Issues in RF Design

2.2.1 Noise

Noise can be determined as a result of random fluctuations in current flow and it limits all the sensitivity of all radio systems. In universe, any matter above 0 K contains thermal energy and it moves atoms and electrons around in a random way, leading to random currents in circuits. These types of noises are generated by the circuits but some other sources also generate noise to the environment. Radio antennas, microwave ovens also

generate noise and affect the operating of nearby devices [2]. Noise can be summarized as a simple example; any level of signal power could be transmitted if there were no noise in environment but in fact that the signal will be competing with an ever present environment of random signals or noise.

Electrical noise can take several forms including $1/f$ (Flicker) noise, thermal noise and shot noise. 1/f noise can be determined as the noise that decreases with ascending frequency. In RF front-end circuits, generally the interest of frequency is high and $1/f$ noise is not the main concern. But some frequency generating/converting circuits, such as voltage control oscillators and mixers, $1/f$ noise comes to a critical design consideration.

2.2.2 Linearity and Distortion

The receiver must be able to detect the desired signal in the presence of other interfering signals. The signal powers at the receiver input may vary from -110dBm to 0dBm. These signals are partially filtered out by the pre-select filter, but the signals at the reception band pass through the filter. Besides that, the transmitter signal and other signals used in the transceiver may leak to the LNA input. In the worst case, these signals and their mixing products can corrupt the reception of the desired signal by desensitizing some particular receiver block [3].

This is due to the non-linear property of active devices. Ideally, the input-output relationship of a linear, time-invariant system can be modeled as:

$$y(t) = a_1 x(t) \tag{2.1}$$

where x(t) and y(t) are the input and output of the non-linear system. But, due to non-linearity, the system input-output relationship is modified to be as following:

$$y(t) = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) + \ldots \tag{2.2}$$

The coefficients a_2, a_3 provide information on the non-linearity of a device or a circuit. When a sinusoidal signal $A\cos wt$ is applied to the system in (2.2), the output y(t) would be:

$$y(t) = \frac{a_2 A^2}{2} + \left(a_1 + \frac{3a_3 A^2}{4} \right) A\cos wt + \frac{a_2 A^2}{2}\cos 2wt + \frac{a_3 A^3}{4}\cos 3wt \qquad \textbf{(2.3)}$$

From (2.3), the output contains not only the fundamental frequency term. It also contain many higher order harmonics caused by $x^2(t)$ and $x^3(t)$. Typically, high-order terms are negligible. However as the input amplitude becomes large enough, their effect become to affect the output significant. If the circuit is implemented in fully-differential architecture, the even-order harmonics can usually be neglected. Among the high-order harmonics, the most troublesome harmonic is the third-order. Usually, the linearity of the receiver is characterized using the gain compression and third-order input intercept point (IIP3) [4].

The gain compression determines how large an input signal can be accepted at the receiver input. This can easily be determined with a single-tone analysis. As the power is increased, the gain of most circuits decreases, as shown in Figure 2-1.

The gain compression can be calculated using the (2.2) and (2.3). It can be seen that the term at the frequency of interest also depends on the third-order term. Thus, the output signal is decreased when α_3 has an opposite sign to α_1. In RF circuits, the gain compression is defined as the "-1dB compression point", which is the point where the gain is decreased by 1dB from the gain at small signal levels. In receivers, the compression point is usually defined at the input (ICP) and in transmitters at the output (OCP).

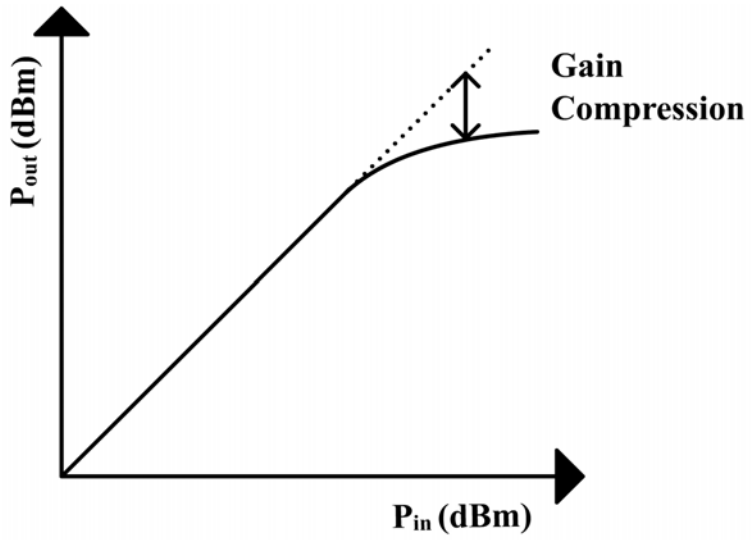


Figure 2-1: Compression of Output Power

The characterization of the RF circuits with harmonic distortion is not practical, since RF circuits are usually frequency-dependent and the harmonic components fall far away at the stop-band of the circuit. A more useful characterization for RF circuits is to use the intermodulation products. Instead of using the single-tone input in the system defined in (2.1), two signals at different frequencies $\left(A\cos\left(w_1 t\right)+B\cos\left(w_2 t\right)\right)$ are used as input signals. Thus it can be calculated that the following signals appear at the system output:

$$
\begin{aligned}
& y(t)=\frac{1}{2}\alpha_2\left(A^2+B^2\right) \\
& +\alpha_1 A\cos\left(w_1 t\right)+\alpha_3\left(\frac{3}{4}A^3+\frac{3}{2}AB^2\right)\cos\left(w_1 t\right) \\
& +\alpha_1 B\cos\left(w_2 t\right)+\alpha_3\left(\frac{3}{4}B^3+\frac{3}{2}A^2 B\right)\cos\left(w_2 t\right) \\
& +\frac{1}{2}\alpha_2 A^2\cos\left(2w_1 t\right)+\frac{1}{2}\alpha_2 B^2\cos\left(2w_2 t\right) \\
& +\frac{1}{4}\alpha_3 A^3\cos\left(3w_1 t\right)+\frac{1}{4}\alpha_3 B^3\cos\left(3w_2 t\right) \\
& +\alpha_2 AB\cos\left(w_1-w_2\right)t+\alpha_2 AB\cos\left(w_1+w_2\right)t \\
& +\frac{3}{4}\alpha_3 A^2 B\cos\left(2w_1-w_2\right)t+\frac{3}{4}\alpha_3 AB^2\cos\left(2w_2-w_1\right)t \\
& +\frac{3}{4}\alpha_3 A^2 B\cos\left(2w_1+w_2\right)t+\frac{3}{4}\alpha_3 AB^2\cos\left(2w_2+w_1\right)t
\end{aligned}
\qquad \textbf{(2.4)}
$$

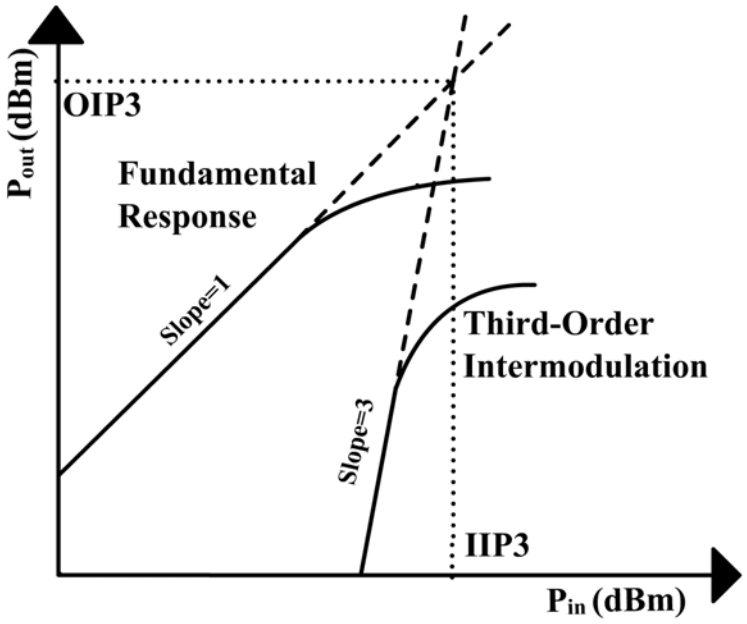


Figure 2-2: Behavior of fundamental and third-order components

Hence, the output signals include the signal, harmonics, and intermodulation components. The most harmful intermodulation products in LNA design are at the frequencies $2f_2$-f_1 and $2f_1$-f_2. It should be taken into account to control the power of the third-harmonic.

The receiver linearity for these signals can now be specified using the third-order intercept point. Again, in receivers, the intercept point is usually referred to the input (IIP3) and in transmitters to the output (OIP3). The intercept point is determined as the crossing point where the fundamental and third-order terms have equal power, as illustrated in Figure 2-2 . The third-order intercept point IP3 must be defined when the device is operating in a weakly nonlinear area [5]. As illustrated in Figure 2-2, the fundamental and third-order terms have different slopes at higher input power levels.

2.2.3 Impedance Matching

To achieve maximum power transfer, impedance matching between the load and the source is the essential requirement. Usually this matching is accomplished by passive

networks connected between the source and the load. These matching networks works not only are designed to achieve minimum power loss between the load and the source, but also are based on minimizing noise influence, maximize power handling capability and linearizing the frequency response [6].

Maximum power will be transferred from the source to the load if the load resistance equals the source resistance. However in the case of AC or time-varying wave forms, this theorem states that the maximum power transfer occurs when the load impedance is equal to the *complex conjugate* of the source impedance [7]. If the source impedance is described, by $Z_S = R + jX$, then the load impedance should be $Z_L = R - jX$, its complex conjugate.

Transistor, transmission lines, LNAs, mixers, antenna systems and all the other active or passive components has an input or output impedance of *complex* because devices contain some reactive components. Therefore it is very important to know how to handle these reactive components. There are two different ways to handle these. One is the analytical method and the other is the graphical method using the Smith chart. The first approach yields very precise results but is complicated. The second approach is more intuitive, easier, and fast because it does not require complicated computation. In this thesis, all the matching circuits are realized using smith chart and all the filter characteristics and other parameters are calculated using Agilent ADS® simulator.

2.3 Receiver Architectures

Two metrics which are used to evaluate receiver performance are sensitivity and selectivity. A receiver with high sensitivity can correctly process a very weak desired signal whereas a receiver with high selectivity can correctly process a desired signal in the presence of very strong interferers at adjacent frequencies. The required sensitivity and selectivity of a receiver are highly dependent on the specifications of the underlying communications system. In order to meet the sensitivity and selectivity requirements of a

particular system while facilitating a highly-integrated, low-power implementation and the architecture used for the receiver must be carefully considered.

2.3.1 Heterodyne Architecture

This topology is well known as its superior selectivity and sensitivity, and it is still widely used in different applications. The heterodyne architecture is probably the most commonly used architecture in current commercial receiver implementations [8].

To filter a narrow band signal that is centered at high frequencies requires very high *Q*–factors. In fact, in heterodyne architectures, the signal band is translated to much lower frequencies by mixing operation; as a result, the *Q* required to filter the narrow–band signal is more relaxed.

The block diagram of a superheterodyne receiver, with one intermediate frequency (IF) is shown in Figure 2-3. In a superheterodyne receiver, the signal passes through the LNA, which is usually connected and matched to filters at both sides. The pre-select filter preceding the LNA passes the whole reception band for the desired system and attenuates signals outside this band. The following filter is required for image noise filtering because the LNA frequency response is not usually selective enough to suppress the noise at the image band. Hence, without this filter, the mixer would downconvert the noise from the image to the first IF. In addition, this filter may be used to filter out possible out-of-band tones that could corrupt reception. As an alternative, this filter can be replaced with an image-reject down-converter [3]. However, this requires additional hardware and good matching between different components in order to achieve high image suppression. After down-conversion, a channel-select filter limits the spectrum for the following stages to the desired signal by attenuating those signals which are out-of-channel. Hence, the linearity of the following stages is relaxed. The channel-select filter is usually an external passive surface acoustic wave (SAW) filter, which is not an adjustable filter. Therefore, the first VCO must have a frequency which is adjustable for the whole reception band. Furthermore, the first IF must be higher than half of the

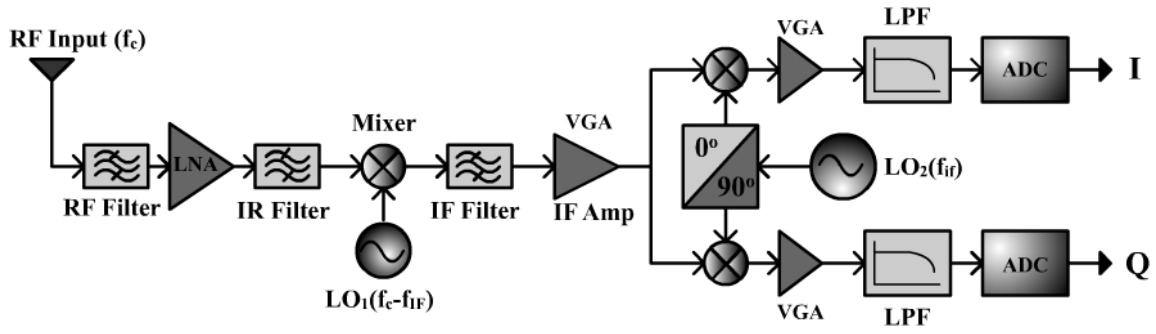


Figure 2-3: Heterodyne architecture block diagram

reception bandwidth. Hence, the image is then always outside the reception band. The channel-select filter is followed by a variable-gain amplifier and demodulator, which divides the signal into I and Q branches.

A second IF stage may be used, which performs part of the channel filtering and interference cancellation. However, the use of a second IF may increase costs, and, because of the third LO, frequency planning becomes more difficult. Obviously, the channel filtering and gain may be distributed among different blocks in order to achieve an adequate performance. This

distribution of gain and filtering is the reason why this architecture gives a good performance. The main reason why this architecture is currently starts to unpopular is that it requires expensive external components [9]. The pre-select, image, and channel-select filters cannot be integrated with current technologies. Thus, the size and cost of the receiver increase. Therefore, other architectures, which can be integrated on a single chip, have been widely explored.

Although transceivers based on superheterodyne architectures are actually realized and commercialized, they present more problems to the integration because it is difficult or impractical to realize at high frequency, as an integrated CMOS solution, the high–*Q* typical of discrete components. In particular the integration of the receive path requires the elimination of the external image–rejection filter and IF filter [9].

Another drawback in the superheterodyne architecture consists in the fact that if the IR filter is realized as a passive external component, the integrated LNA has to be designed to drive 50 Ω input impedance of this external filter. And this constraint limits NF, IIP3 and gain performances of the LNA [6]. The RF and IF filters are typically implemented using ceramic filter technology while the IR filter is typically implemented using surface acoustic wave (SAW) technology. In this thesis, the filter that follows the LNA assumed as an external filter so the output of the LNA matched to 50 Ω which is the input impedance of the external filter.

2.3.2 Direct-Conversion (Homodyne) Architecture

This architecture, which is also known as zero-IF or homodyne, converts the center of the desired RF signal directly to DC in the first mixers which is shown in Figure 2-4. The direct-conversion receiver (DCR) suffers from special problems that do not appear in superheterodyne receivers.

A typical DCR includes a pre-select filter, an LNA, and quadrature mixers, followed by channel-select filters, variable-gain amplifiers, and A/D converters as shown in Figure 2-4. The pre-select filter is required prior to the LNA in order to attenuate out-of-band signals, as in the superheterodyne receiver, because of poor front-end selectivity. The image filter after the LNA is not required because the desired signal is on both side bands. Obviously, this relaxes the design of the LNA-Mixer interface because there is no need to drive external impedance, for example, 50Ω. The quadrature I and Q channels are necessary while receiving typical phase- and frequency modulated signals, because the two sidebands of the RF spectrum contain different information and result in irreversible corruption if they overlap each other without being separated into two phases. Channel filtering in DCRs is performed with low-pass filters, which can be implemented with on-chip active circuits. The amplification and channel filtering can be distributed across the baseband chain to improve the performance of the receiver [10].

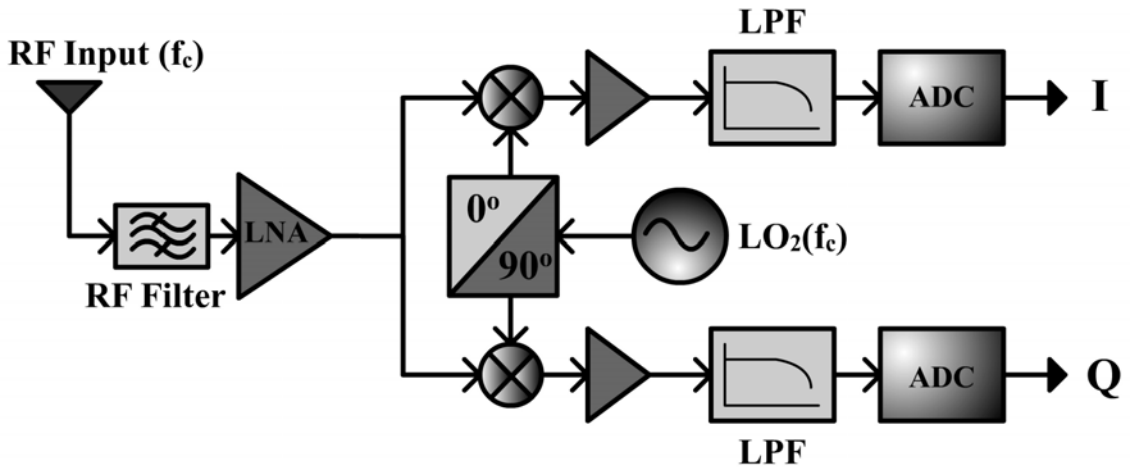


Figure 2-4: Direct-Conversion Receiver Architecture

DC offset is present above all because there is not perfect isolation between the LO port and the input of the LNA and of the mixer; in fact very strong LO signals (at frequency $f_{LO}=f_C$) can be transferred to the LNA and mixer inputs by capacitive or substrate coupling. This leakage signal is then mixed and downconverted to DC, producing a DC component at the output of the low–pass filter (self–mixing). This problem is exacerbated by the fact that the effects of LO leakage can be a function of the impedance seen at the antenna [11]; this DC offset can also be time varying, making very hard the possibility of eliminate this kind of problem, in particular in frequency hopping receivers. These are the reasons for choosing the heterodyne architecture to design the LNA in this thesis.

3

Chapter 3

DESIGN AND IMPLEMENTATION OF LNA

3.1 Introduction

Data communication systems in compliant with IEEE 802.11a wireless local area network (WLAN) standard has found widespread use, meeting the market demands, for the last few years. Next generation WLAN operates in the 5-6 GHz frequency range. A front-end receiver capable of operating within this frequency range is essential to meet the current and future of products. One of the critical components, allowing the common use of the technology can be attributed to the high performance Low Noise Amplifiers (LNA) in the receiver chain of the 802.11a transceivers.

In IEEE 802.11a, there are three frequency bands; 5.15GHz - 5.25GHz, 5.25GHz - 5.35GHz and 5.725GHz - 5.825GHz. A well-designed LNA should not only supply sufficient gain to suppress the overall noise figure but also have adequate bandwidth to cover all three frequency bands. Recently, many LNAs have been implemented using various semiconductor technologies with excellent low noise figures (NFs) [12-16]. These low noise figures are achieved at the expense of very high dc power consumption, or other trade-offs such as high input/output return loss, low linearity, or unsatisfactory dynamic ranges. The compensation of the trade-offs depends on applications as such ultra

low noise may not be priority because of the need for low power dissipation, longer battery lifetime of portable communication systems. For such portable systems, the total power consumption could be as low as 15 mW, acceptable to be called as a low power consumption [17]. It is also possible to achieve low noise together with low power consumption by using GaAs technologies or by using off-chip matching components. However, these solutions also come at high technology cost. There has been increasing effort toward the realization of low-cost, on-chip high-Q inductors to keep the cost lower.

One of the key design criteria of LNA covering the specified frequency range is to provide sufficient gain to overcome the noise contributed by its subsequent stages. To achieve this criterion LNA has to add a minimum noise to the overall system that could be lower than 3 dB. In addition, as the antenna is generally designed for 50-Ω terminations, and the image-reject filter that follows the LNA in heterodyne transceiver architectures, input and output impedance of the LNA should also be matched to 50-Ω. This design, simulation and optimization procedures will be outlined and detailed further in following parts of this chapter.

3.2 Survey of Previous LNAs

Since the field of RFIC research is a much applied topic, it is not surprising that market forces have driven the research focus. New and current wireless standards (AMPS, PCS, 3GHz cellular, Bluetooth, 802.11a, 802.11b, HiperLAN2, WiMAX, etc.) are usually the application targets for published research. As a result, most previously published RFIC LNAs have been designed to operate in the 900 MHz, 1.8 GHz, 2.4 GHz, and 5 GHz frequency bands. Very few published LNAs operating above the 5 GHz band have been implemented in standard CMOS or SiGe BiCMOS.

The majority of published RFIC LNAs operating at or above 5 GHz have been implemented with bipolar or hetero-junction-bipolar transistors. The fabrication technology was either silicon BJT, or silicon germanium HBT. These technologies have a noise figure advantage over CMOS for a given frequency of operation and level of power consumption.

Low noise amplifier schematics are generally quite simple; they employ minimal numbers of transistors and passive components. Although a single transistor in common-emitter configuration can be used for amplification [18], a two-transistor cascode architecture is often preferred because of increased stability, reduced reverse path leakage, and reduced input capacitance [19]. Inductive degeneration is very commonly used to provide real 50 input impedance. Noise matching the input involves optimizing the transistor geometry and bias current. However, due to the rapid pace of RFIC research, most RFIC-LNA design accomplishments are reported in conference proceedings as opposed to journal articles, and lack detailed discussion on these optimization strategies [19]. Output matching can be performed through on-chip passives, or through an emitter-follower buffer [20].

Table 3-1 presents a summary of previously published LNAs operating around 5 GHz. As mentioned before, most LNAs at these frequencies are implemented in SiGe processes. Operating at higher frequencies yields higher noise figures. Also, for a given operating frequency, LNAs implemented in higher f_T processes had lower noise figures. This can be seen by comparing [20] and [21] in rows 2 and 3 of Table 3-1.

Table 3-1: Previously published LNAs operating at 5 GHz

Source	Technology	f_T (GHz)	Freq. (GHz)	S_{11} (dB)	Gain (dB)	NF (dB)	Implementation
[22]	SiGe:C HBT	50	5.3	-	15	1.6	Cascode
[20]	Si BJT	53	5.6	-	26	1.8	Cascode with E-F
[21]	Si BJT	25	5.8	-10	7	4.2	Cascode
[23]	CMOS 0.35 µm	50	5.8	-11	7	3.2	Two-stage C-S
[24]	SiGe HBT	40	5.8	-	12	1.8	C-E
[19]	SiGe HBT	80	6	-12	16	1.9	Cascode
[20]	SiGe HBT	54	6.2	-	31	1.3	Cascode with E-F
[25]	0.18 µm CMOS	90	5	-5	56	6.5	Cascode with E-F
[26]	0.18 µm CMOS	90	5.2	-	11	2.9	Cascode with E-F
[27]	0.35 µm SOI	60	5.2	-	8	2.3	Cascode
[28]	0.25 µm CMOS	80	5.8	-35	11	2.2	Two-stage C-S
[29]	0.25 µm SiGe	100	5	-14	13	2.2	Cascode
[30]	0.35 µm SiGe BiCMOS	40	5.4	-	20	1.6	Cascode

E-F = Emitter-Follower, C-E = Common-Emitter, C-S = Common-Source

3.3 LNA Design

In LNA circuits, gain can be achieved by a three terminal single transistor. One of the terminal serve as an input while the rest are allocated for output and ac ground. Using different connection possibilities, different modes of operation can be obtained; Common-Emitter (CE), Common-Collector (CC) and Common-Base (CB). The CE

operating mode is most often used as a driver for an LNA. The CC stage has high input impedance and low output impedance, a good candidate for buffer stages. The CB is generally used as a cascode in combination with the common-emitter driver stage, most often used topology in LNA applications for achieving high gain at RF frequencies. The loads of the topologies can be made by using resistor for broadband applications or by using tuned resonators for narrow-band applications. The decision procedure of choosing input-matching network is similar to load choice procedure. An LNA with resistive input-matching has high noise figures due to the resistances in the input of the circuit, generally not preferred for low-noise applications. This problem can be solved by using inductors for simultaneous input and noise matching. In this work, our topology of choice is "emitter-degenerated cascode", as detailed in the next subsections.

3.3.1 Topology of the Circuit and Detailed Description

Figure 3-1 illustrates the schematic of a cascode-connected, common-emitter LNA with inductive emitter degeneration. The cascode amplifier has the advantage of having high gain, low noise and stability, provided by large isolation. The transistor Q_1 provides the gain of the amplifier and must be chosen out of the technology library carefully. As will be discussed in following section, the designer is only allowed to change the emitter length, hence change the effective emitter area of the Q_1. Emitter length directly changes the C_{be} capacitance and the input impedance of the transistor. The latter one carries more importance because; C_{be} can be compensated by tuning the value of L_e. As the emitter length of the transistor increases, the input impedance of the transistor Q_1 decreases, becoming more difficult to match to the source impedance. Same problem occurs when the length is chosen as a small value, making the input impedance large. Therefore, the emitter length of the transistor must be chosen large to achieve the desired gain and for impedance match as well. The typical application for achieving large area transistors is connecting them in parallel. This becomes necessary as the maximum length of the transistors is restricted by the manufacturer to 32-μm for the specific transistors and technology of our choice.

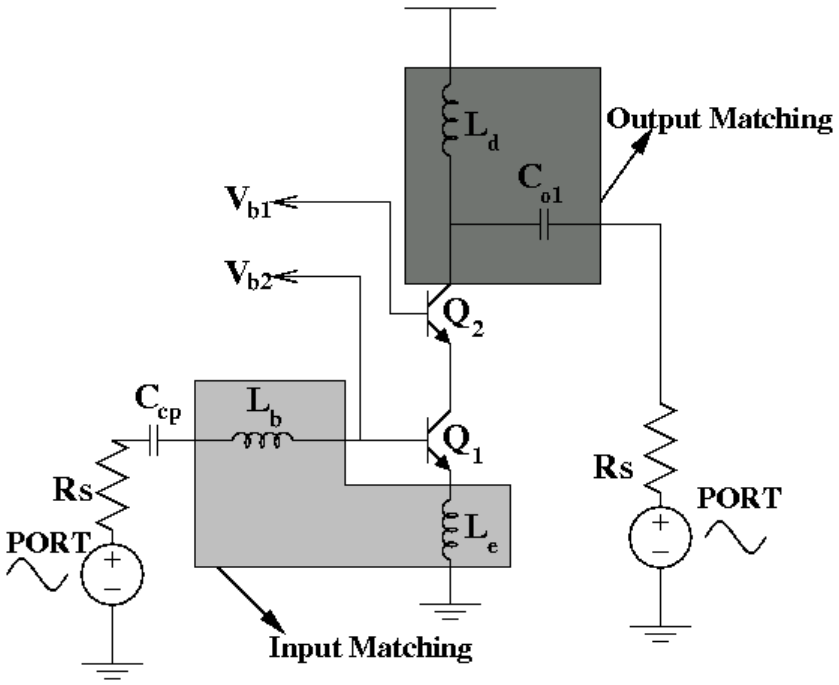


Figure 3-1: Cascode LNA circuit

The transistor Q_2 is a common-base amplifier and provides the reverse isolation by reducing the Miller capacitance between its input and output. The cascode transistor reduces the feedback of $C_{\mu 1}$, resulting in an increased high-frequency gain. The dimensions of Q_2 largely affect the output impedance of the LNA at the frequency of our interest. Also, the parasitic capacitances, having a value of a few hundred fF in our technology, can extremely change the output impedance of the circuit at our operating frequency of 5 GHz. Hence, the dimensions of the Q_2 obtained by adjusting the parasitic capacitance of Q_2. Using cascode transistor has a disadvantage of decreasing the output swing of the circuit when compared to a single transistor LNA counter parts, because of the need for an extra voltage drop across the cascode transistor. The inductor L_d is used for biasing, loading and output matching purposes. L_d must be chosen as large enough to block the flow of ac signal to V_{dd} and also to increase the load of the circuit while keeping in mind that L_d is also a part of output matching circuit. C_{o1} is used for both loading and matching the output of the circuit to 50-Ω source impedance by decreasing the inductive part of the output impedance. Also it is used for dc blocking of output of the circuit. The C_{cp} capacitor at the input is used for the purposes of both dc-blocking and

input-matching. L_g and degeneration inductance L_e are used to provide both the power and noise matching. Also for broadband applications, a resistor can be used instead of L_e but this is not suitable for low-noise and narrowband applications. In the frequency range of 5 GHz, typical values for L_e is about 200-500 pH. These are the values that the technology libraries don't have. Design and sizing the L_e and L_b will be studied in the input and noise matching sections.

3.3.2 Low-Noise Transistor Design

One of the main efforts during the LNA design is given into optimizing the bias currents and geometries of the transistors for obtaining low noise figure. In bipolar transistors, the major noise contributors are thermal and shot noises, arising from the base resistance r_b and collector current I_C, respectively. Using multi-emitter transistors or placing a large number of transistors in parallel decreases r_b while increasing the base-collector capacitance Cμ, hence placing a limitation on the minimum achievable value of noise figure [31]. Also, minimum achievable noise figure (NF_{min}) can be decreased by increasing I_C with increased power consumption. For a given technology, the attainable noise figure is basically dependent on the operating current density.

The main limitation of the NF of the overall circuit is the minimum noise figure of the driver transistor, Q_1 in Fig. 1. NF_{min} can be achieved by matching to its optimum source impedance. It can be expresses as [32]:

$$NF\min(J_C) = 1 + \frac{n}{\beta} + \sqrt{\frac{2J_C}{V_T}(r_b + r_e)_u\left(\frac{f_0^2}{f_T^2} + \frac{1}{\beta}\right) + \frac{n^2}{\beta}} \qquad \textbf{(3.1)}$$

where J_C is dc collector current density, V_T is thermal voltage, f_0 is operating frequency, f_T is unity current gain frequency (transition frequency), β is dc collector-base current gain, n is junction grading factor and $(r_b + r_e)_u$ are the base and emitter ohmic resistances of a unit device, respectively.

In (3.1), all the parameters, including f_T, are bias dependent. Hence, it is useful to plot the minimum achievable noise figure to initiate the noise optimization for a given process technology and frequency.

The geometry of a bipolar transistor is defined by the emitter stripe width (W_e) and the emitter length (L_e), discussed later. In general, some common approaches can be said to find the optimum geometries for a given transistor; the W_e in a SiGe HBT BiCMOS process is typically proportional to the minimum feature size and improves when the emitter width decreases. Therefore the noise performance of SiGe HBTs will improve with lateral scaling. The suitable choice of emitter width is the minimum allowable feature size for improving NF_{min}. The appropriate choice of emitter length is relatively easier in a way that the minimum emitter length should be used for achieving the NF_{min}. The problem, with use of the minimum emitter length is the optimum source impedance having too small value, required for the minimum noise figure. This means that the input impedance of the circuit is too far away from the 50-Ω source impedance and is difficult to match. Complex matching circuits also add noise to the overall noise of the circuit. Hence, appropriate emitter length must be chosen which is small and close to 50-Ω source impedance.

In general, design specific technological details of the process data are not available for interested frequency range. For finding the J_{Copt} of the unit device, the simulated or measured data could be used. We have started the LNA design from simulations of the available transistors in AMS library to obtain the noise characteristics of transistors with respect to bias points and emitter areas. The transistor, circuit simulations are performed by using Agilent Design System (ADS®) and Cadence® design tools. In AMS 0.35µm SiGe HBT technology, there are seven different high-speed HBT transistors, in different from each other with number of contacts at each terminal [33]. The number of contacts at each terminal determines the contact resistances, hence the resulting noise response of the transistors. For example, the symbol **npn232**, the numbers 2, 3, and 2 refer to the number of contacts of collector, base and emitter terminals, respectively. Of the seven transistors

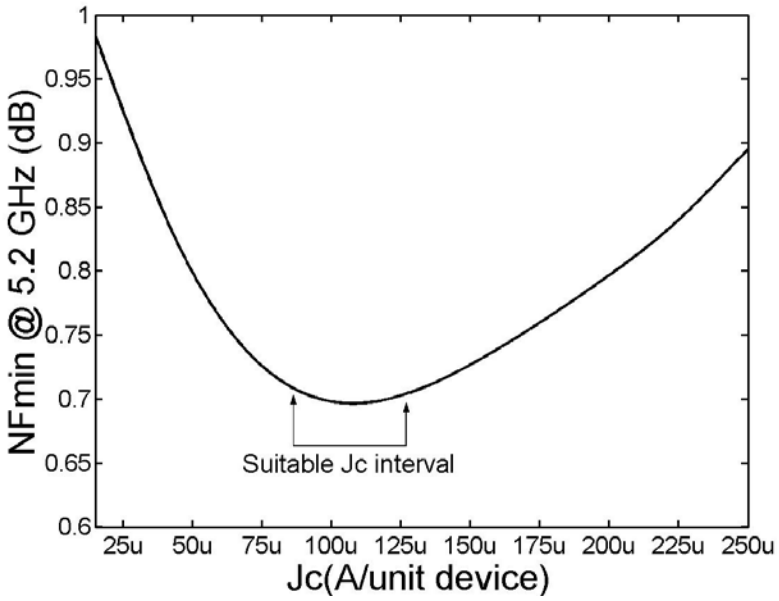


Figure 3-2: NFmin versus I_C curve for npn232 transistor

simulated at their optimum bias points (minimum NF), npn232 has shown the lowest noise figure, hence chosen to be used in our LNA circuit. The noise figure of a transistor depends on collector current density (I_c/Area) instead of only collector current (I_c). The noise figure versus collector current curves of npn232 transistor at 5.2 GHz are shown in Figure 3-2 for the unit device area.

As seen in Figure 3-2, 80 - 125 μA of collector current range provides the lowest noise figure and is suitable for the npn232 transistor with unit device area for the 5.2 GHz frequency band. Other collector currents increase the NF_{min} of single transistor, directly increasing the overall NF of the LNA.

The next step in the design process is to find the corresponding R_n (Noise Resistance) and to adjust this resistance to 50-Ω for input matching. By using Y-parameters of two-port noise model of a single HBT transistor [32] as seen in Figure 3-3, noise resistance can be specified as:

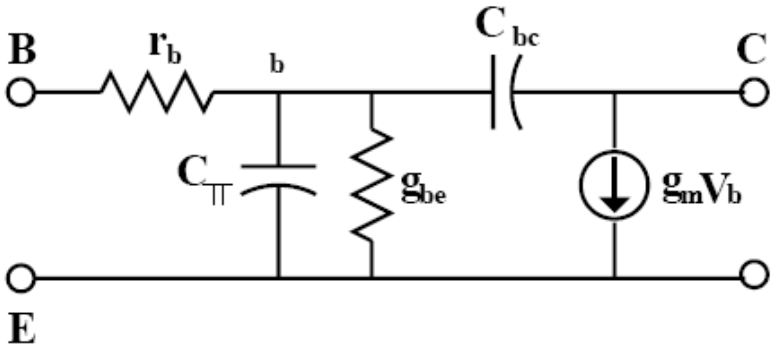


Figure 3-3: Equivalent Circuit of the single HBT

$$R_n = r_b + \frac{1}{2} g_m \qquad \textbf{(3.2)}$$

(3.2) indicates that R_n is directly proportional to the r_b (base resistance), and is thus independent of frequency at a given bias point. Generally r_b is large enough for neglecting the $\frac{1}{2} g_m$. The result of noise resistance analysis is presented in Figure 3-4. Here the device input noise resistance is simulated for different areas of the device over the frequency range of our interest. As seen in Figure 3-4, the 50-Ω of R_n resistance is provided by A=15μm and I_c =2mA, hence selected as optimum area and DC bias point, respectively.

3.3.3 Simultaneous Input and Noise Matching

In LNAs, gain versus noise figure trade-off is well-known issue [34]. Gain and noise figure circles are easy way of finding the optimum impedances which give the maximum gain and maximum NF respectively. Typically, gain-circle centers and noise figure-circle centers don't intercept at the same point in the smith chart. So, this shows the difficulty to match the input and noise simultaneously. There is also input matching versus noise figure trade-off exists in the LNAs. The latter is more important one since the gain is not the priority in LNAs. There are several methodologies present that can be applied to obtain a very low noise figure at the same time a good input matching. In this work we

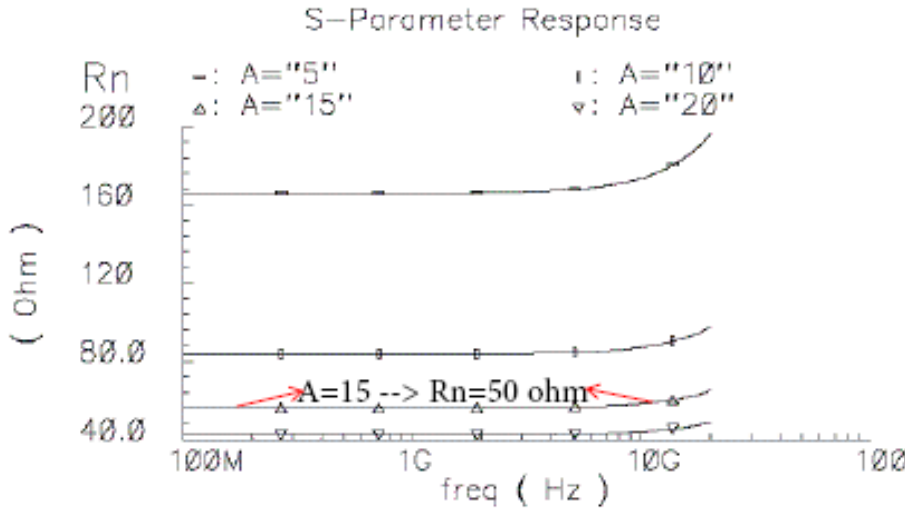


Figure 3-4: Frequency curves with different areas for npn232

will use the smith chart to deal with this trade-off because the desired impedances can be obtained simultaneously on the same smith chart. Hence a designer can easily choose where the circuit should operate.

According to linear noise theory, one can model the noise of a noisy two-port system with the two equivalent input noise generators [35], as seen in Figure 3-5, by a series voltage source and a shunt current source.

The two noise sources are related by the correlation admittance. The noise factor, F, is described as:

$$F = F_{\min} + \frac{R_n}{G_S}\left|Y_S - Y_{opt}\right|^2 \qquad \textbf{(3.3)}$$

where R_n is the equivalent noise resistance of the noisy two-port. Y_s is the source admittance and $Y_s = G_s + jB_s$, Y_{opt} is the optimum source admittance and $Y_{opt} = G_{opt} + jB_{opt}$, and F_{min} is the minimum noise factor which is a function of source admittance, Y_s. Thus one can plot the noise factor contour on the source admittance Smith chart, which also represents the noise circles of the circuit. When $Y_S = Y_{opt}$, the center of the noise

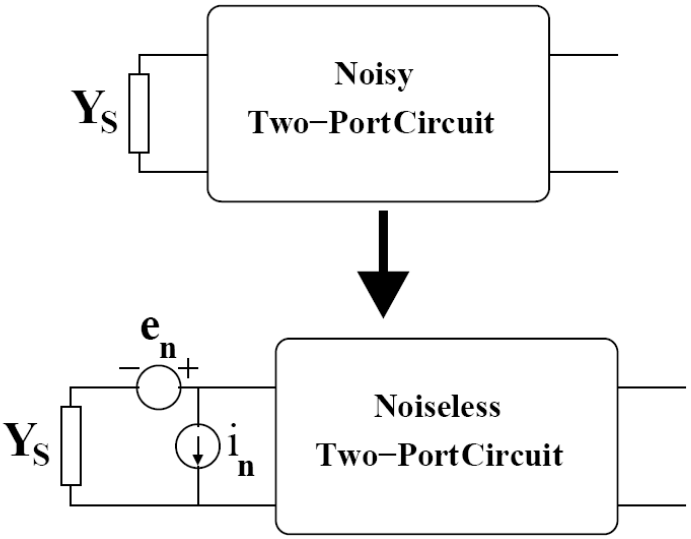


Figure 3-5: Two-port Noise Theory

factor contour corresponds to F_{min}. In another words, if the source admittance is equal to Y_{opt}, one can achieve the minimum noise figure and eliminate the second term in (3.3). One can move the center of the source admittance Smith chart, Y_{opt}, by changing transistor dimensions, bias current and/or input matching network design. A wise choice is to move the center of the noise circles to the center of the Smith chart so that $Y_{opt} = R_s$. By doing this, an input matching is also provided since LNA input must be matched to 50-Ω source impedance, located to the center of the smith chart. We performed noise-matching by designing the input-matching network so that the center of the LNA's noise circles (NC) moves to the center of the source admittance Smith chart, presented in Figure 3-6. However, in order to maximize the available gain at the frequency of interest, we also moved the center of the available gain circle (GAC) to the center of the source admittance Smith chart. This can be done by tuning the output matching of the circuit, also presented later in the paper.

Since the LNA is the first component in the receiver chain, the input must be matched to 50-Ω that is the output impedance of the previous stage. Many methods for matching have been presented and depend on bandwidth and degrees of complexity of the circuit being implemented. The most convenient method requires two inductors to provide the power and noise match for the LNA. This matching topology can be seen in Figure 3-7.

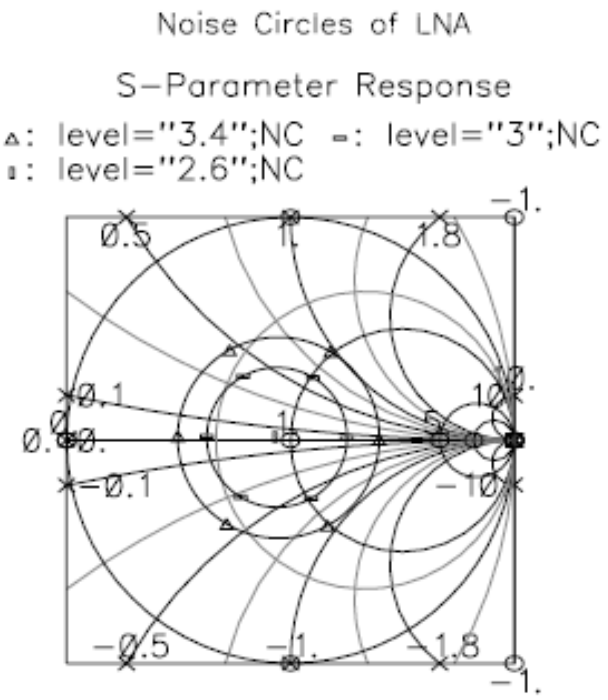


Figure 3-6: Noise Circles of LNA

Here in Figure 3-7 the inductors L_b and L_e are designed to be on-chip, as all the other passives in this circuit.

As the circuit topology is cascode, the effects of Miller capacitance and r_π resistance can be ignored while the calculating the input impedance for the sake of simplicity. Hence, the input impedance for this transistor can be written as:

$$Z_{in} = \frac{-j}{wC_\pi} + jwL_e + \frac{g_m L_e}{C_\pi} + jwL_b \qquad \textbf{(3.4)}$$

For input matching, the real part of the input impedance in (3.4) must be equal to source resistance (50-Ω). That is,

$$R_s = \frac{g_m L_e}{C_\pi} \qquad \textbf{(3.5)}$$

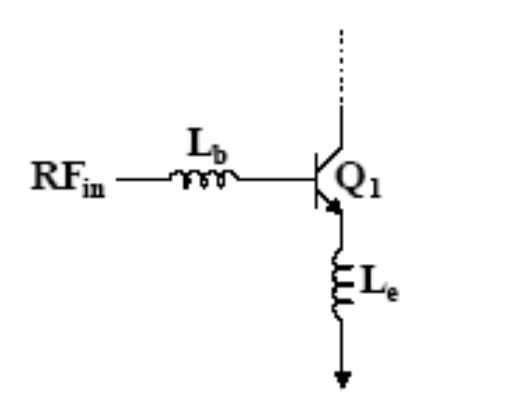


Figure 3-7: LNA Driver Transistor with two Inductors

Also, the imaginary part of the input impedance must be equal to zero to obtain the value for L_b as:

$$L_b = \frac{1}{C_\pi w^2} - \frac{R_s C_\pi}{g_m} \tag{3.6}$$

We have also used an additional C_{be} capacitance for input matching. Without the use of additional C_{be}, the transistor size can also be adjusted (to larger size), resulting an increase in the internal capacitance C_π of the transistor. However, an increase in the transistor size will cause an increase in the minimum noise figure or power consumption of the overall system. The S_{11} data before and after input matching are shown on smith charts in Figure 3-8.

As one can see in Figure 3-8, before the matching, input of the circuit is capacitive due to the C_π capacitance of the input transistor. L_e in Figure 3-1 tunes the real part of the input impedance and L_b in Figure 3-1 tunes the imaginary part of the input impedance. As a result, final input impedance is near the center of the smith chart, providing pure real 50-Ω input impedance, as seen in Figure 3-8. As discussed in the following section, the center of the smith chart also provides the optimum source impedance, giving us the maximum achievable NF_{min} of this circuit.

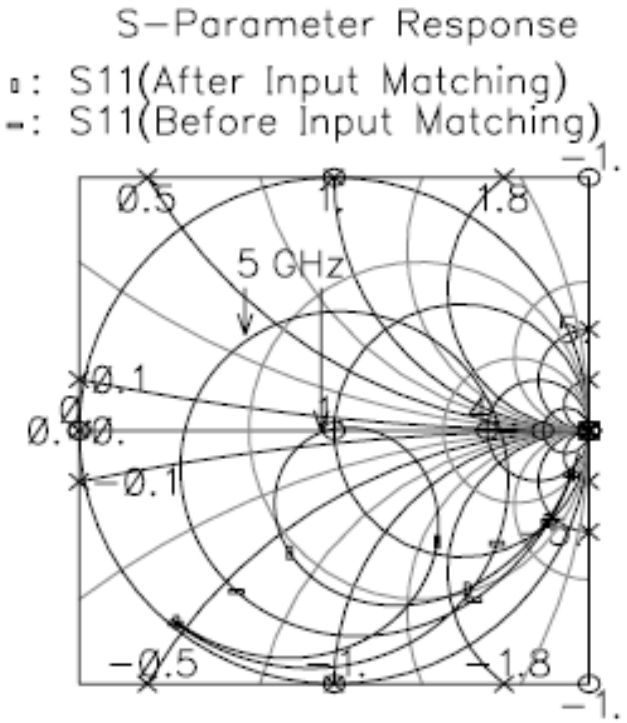


Figure 3-8: S_{11} Curve before and after Input Matching (100MHz-20 GHz)

3.3.4 Design of a Low-value Integrated Inductor

Inductors store magnetic energy and as a result of magnetic induction they are capable of producing voltage across its terminals. Inductors are circular or spiral in shape to achieve a large inductance in a small area. For all frequencies, ideal passive components show constant values with constant phase. But all non-ideal components exhibit change in value with frequency due to their non-linear loss factors such as series resistances or parasitic capacitances.

Typically, standard inductor designs enabling on CMOS and SiGe technologies result in a Q value of 6-12 at 2-6 GHz frequency range due to high resistivity of silicon substrate and high-resistance interconnect with aluminum/poly-silicon [36]. The substrates used today have a relatively high resistivity (10-2000 ohm-cm), thereby reducing the eddy current losses underneath the inductor. These losses are strongly limiting the performance of the voltage-controlled oscillators (VCOs), power or low-noise amplifiers when

compared to designs using off-chip passive components [37]. The use of off-chip components increases the complexity and cost while also degrading performance parameters such as dynamic-range and power-dissipation of the design, hence not preferred to be used in conjunction with single chip ICs.

The inductors are integrated on the top metal layer using a thick metal layer, separated from the silicon substrate by using 2 to 6-μm-thick oxide layers [38]. Oxide layers reduce the parasitic capacitances to the substrate and they allow the integration of large value inductors without having problems with the inductor resonant frequency.

For planar inductors, the problem is the parasitic capacitance between the inductor and the ground plane. These parasitic components decrease the quality factor (Q) of the inductors and make a self-resonance frequency that limits the maximum frequency of operation, making the devices insufficient for high frequency RF communication system applications. For high frequencies, special interest must be given for designing low value inductors.

Generally, due to fabrication limitations, on-chip inductors were made as square spirals as shown in Figure 3-9. For calculating the inductance of on-chip square inductors as the one in Figure 3-9, we can use the expression [39]

$$L = 2.34\mu_0 \frac{N^2 d_{avg}}{1 + 2.75\psi} \tag{3.7}$$

where is the number of turns and μ_0 is the permeability of free space, d_{avg} is given by

$$d_{avg} = \frac{1}{2}\left(D_{out} + D_{in}\right) \tag{3.8}$$

and ψ is given by

$$\psi = \frac{\left(D_{out} - D_{in}\right)}{\left(D_{out} + D_{in}\right)} \tag{3.9}$$

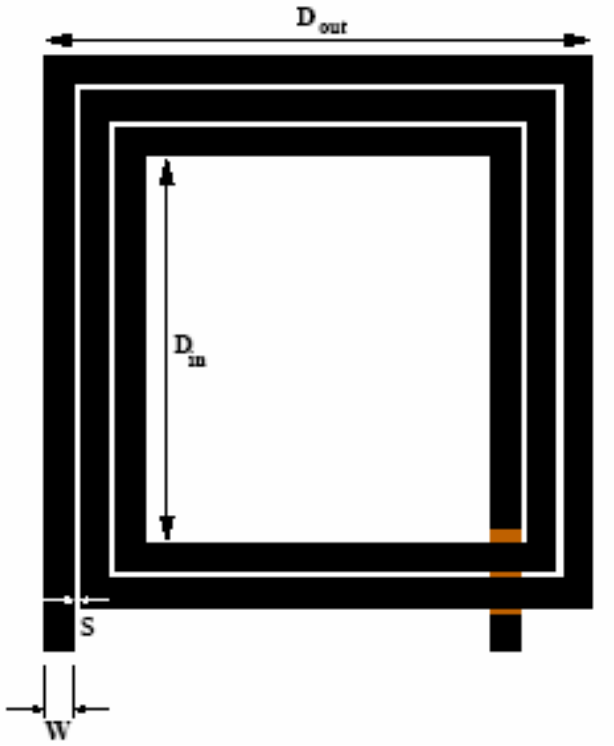


Figure 3-9: A Single-Ended Inductor Layout

The quality factor of a passive component can be defined as

$$Q = \frac{\mathrm{Im}(Z_{11})}{\mathrm{Re}(Z_{11})} \qquad \textbf{(3.10)}$$

(3.10) indicates that, as the resistive part of the coil decreases, the quality factor increases and the inductor behaves more ideal. At low frequencies, the Q tends to increase with increasing frequency because the resistive part of the coil is relatively constant while the imaginary part starts to increase. Beyond a specific frequency with respect to the geometry, the resistive part of the coil extremely increases because of the magnetic effects and skin effect. The optimization of the inductor should be performed to ensure that the inductor has peak performance at the frequency of our interest. The optimization can be performed by using simulators such as ASITIC (**A**nalysis and **S**imulation of **I**nductors and **T**ransformers for **I**ntegrated **C**ircuits [40]) or three-dimensional EM solvers. In this paper, we used ASITIC to extract the parasitic components of passive elements but also used 2.5-D EM solver MOMENTUM® to improve the accuracy of the

simulations. ASITIC provides a sufficient model behavior for our design and decreases the simulation time, hence used to optimize the inductor geometry for the highest inductance and lowest associated series resistance. ASITIC can be used for modeling the electrical and magnetic behavior of passive metal structures residing above lossy conductive substrates. ASITIC works with a *technology file* [41] that describe the substrate and metal layers residing in the technology. We described the substrate and metal layers according to AMS 0.35 μm SiGe BiCMOS process.

ASITIC uses "Π model" for modeling the inductor, as shown in Figure 3-10 [41], including designed inductor and parasitic components. All the values belong to an inductor value of 200 pH at 5 GHz and extracted from ASITIC. In Figure 3-10, R models the series resistance of the metal lines, used to form the inductor. This series resistance will increase at higher frequencies due to skin effect. C_{C1} and C_{C2} model the capacitance from the lines to substrate. These capacitors are parallel-plate capacitors between the inductor metal and the substrate. R_{S1} and R_{S2} model the losses due to magnetic effects and conductance of the substrate. The model that we use is suitable for non-symmetric inductance topologies. For the differential-inductor, small signal model is different from the one in Figure 3-10. These differential-inductor models are commonly used for RF circuits like voltage-controlled oscillators (VCOs).

We can get the Q of the inductor from "Π model" by using

$$Q = \frac{\omega L}{R} \tag{3.11}$$

The simulated Q factor of the inductor in the frequency range of 10 MHz to 20 GHz is given in Figure 3-11.

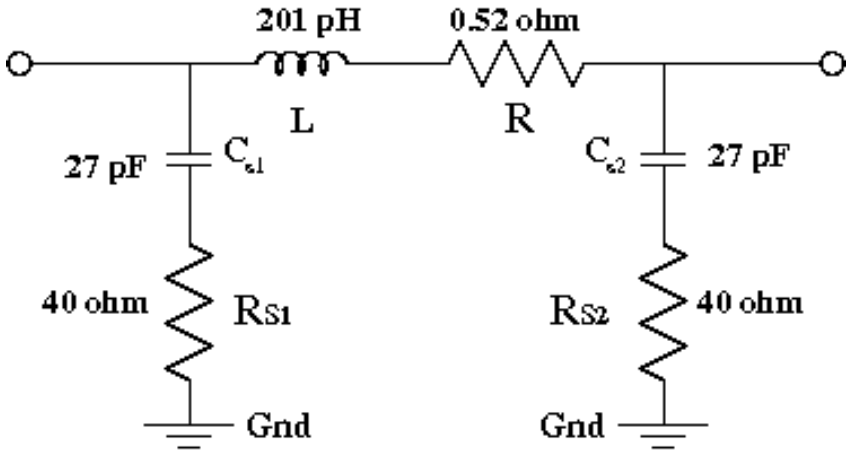


Figure 3-10: The "π" model of the inductor

One can observe in Figure 3-11 that the quality factor increases with frequency, meaning that we are away from the self-resonance frequency of the inductor and the quality factor is only limited by ohmic losses in the metallization. Further seen in Figure 3-11, it is possible to get high quality factor of silicon substrates if the self-resonance frequency of the inductor can be designed high enough. Another critical part of the inductor design, besides the modeling, is generating the layout. Due to self-generated magnetic forces, the inductor must be isolated from the other parts of the circuit. Typically, a ring of substrate contacts is added around each inductor to prevent the coupling the substrate. Generally, three to five line widths away from the inductor is suitable for these substrate contacts.

Magnetic coupling is also another limiting factor for IC-based high-Q inductors. In a dynamic inductor behavior, capacitive and magnetic coupling currents are induced in to the substrate. Generally, capacitive coupling is more dominant over magnetic one. One approach to limit this is to generate a ground plane above the substrate to prevent the currents from entering into the substrate [42]. However, this will also increase magnetic currents hence causing reduction of the inductance. To eliminate this reduction in the inductance, the ground plane is specifically patterned so that magnetically generated currents are blocked from flowing. This method also comes with a disadvantage of increasing the coupling capacitance to the ground hence

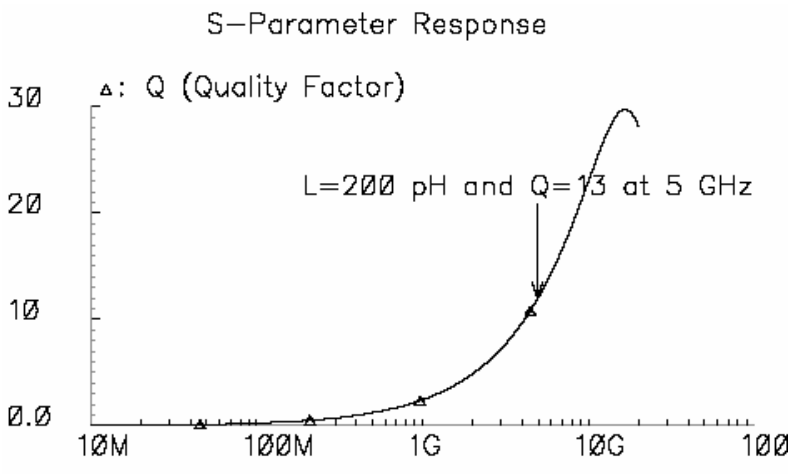


Figure 3-11: Quality Factor (Q) of the inductor

decreasing the self-resonance frequency. Because of this, the shielding must be implemented far away from the inductor to decrease the coupling capacitance and remain above the substrate. In this paper, the inductor shielding is made by using the poly-silicon layer. Figure 3-12 presents the designed 200 pH inductor layout with isolating substrate contacts and pattern ground shields.

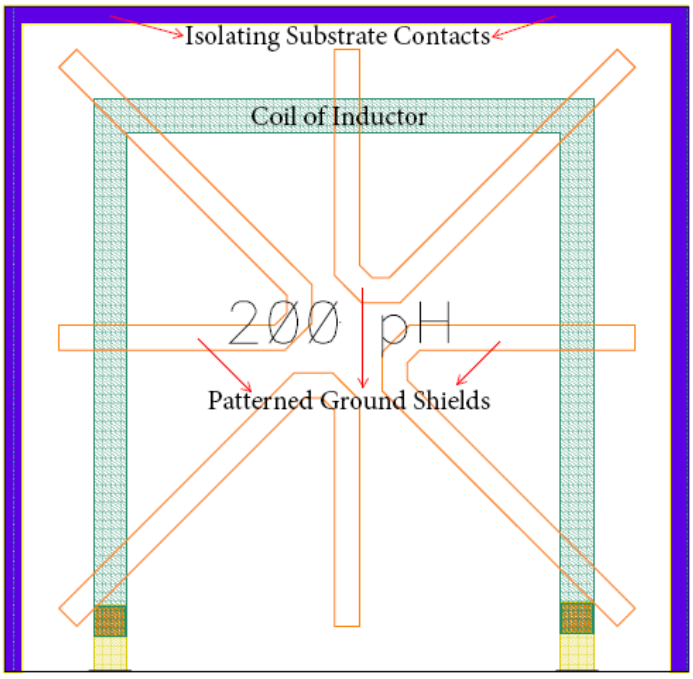


Figure 3-12: Layout of a low value inductor

3.4 Simulation Results

In this section, the simulation results of 5-6 GHz wideband single-stage cascode LNA are presented. All the simulations are performed using Agilent Design System (ADS) and Cadence® design tools with AMS 0.35µm SiGe HBT technology. This technology has a peak f_T value of 50 GHz. Figure 13 presents the result of gain simulation of the frequency range of our interest. As seen in Figure 3-13, the cascode feedback LNA achieves a power gain of above 15 dB in the 5-6 frequency range. The flatness of gain within 0.2 dB in this frequency range covers all the three band of 802.11a standard; 5. 15 GHz-5.25 GHz, 5.25 GHz-5.35 GHz and 5.725 GHz -5.825 GHz.

It is not a coincidence that the maximum gain is achieved in the desired frequency range of 5-6 GHz. Where the maximum gain is achieved can also be analyzed by using available gain circles (GAC) of the circuit. The GAC of our circuit is shown in Figure 3-14. In Figure 3-14, 50-Ω source impedance can be seen and our circuit gives the maximum available gain close to 50-Ω output impedance, also satisfying the desired output impedance for the output matching of the circuit.

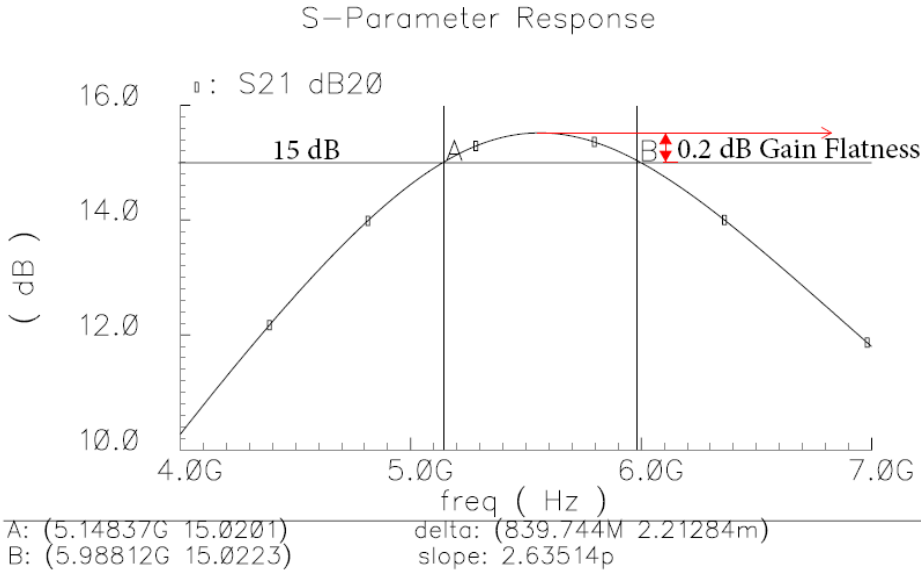


Figure 3-13: Gain Curve of the LNA (S_{21})

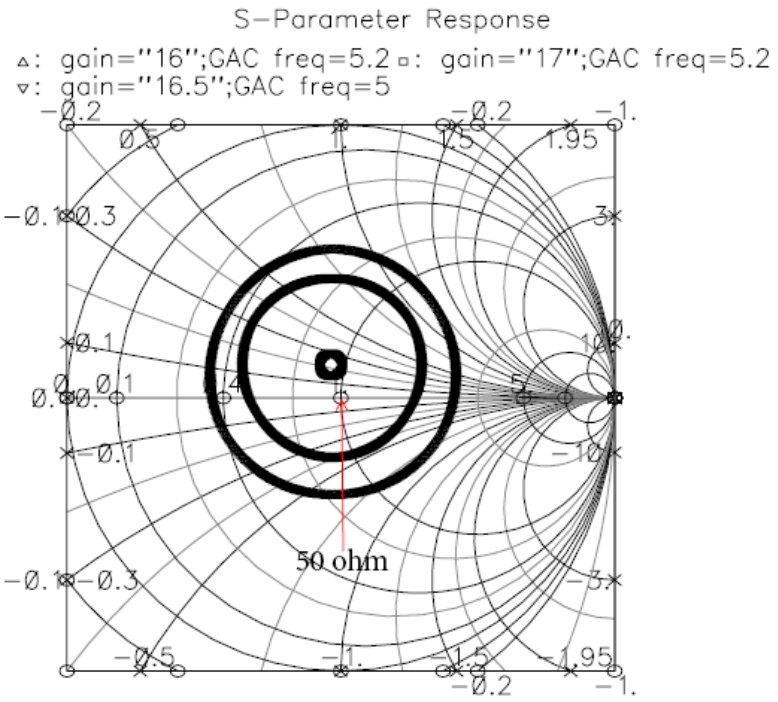


Figure 3-14: Gain Circles of LNA

NF_{min} and NF curves of our LNA circuit are shown in Fig. 15. A noise matching at the desired frequency range (5-6 GHz) and change of NF of 2.8 dB in 5-6 GHz band can be observed in Figure 3-15. In literature, noise simulations generally don't include the inductors and series resistances of wires.

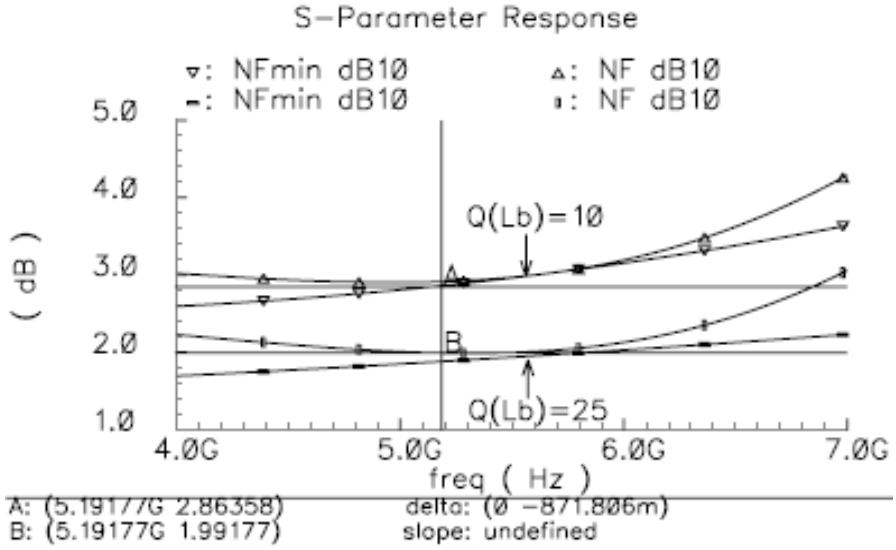


Figure 3-15: NFmin and NF analysis of the LNA

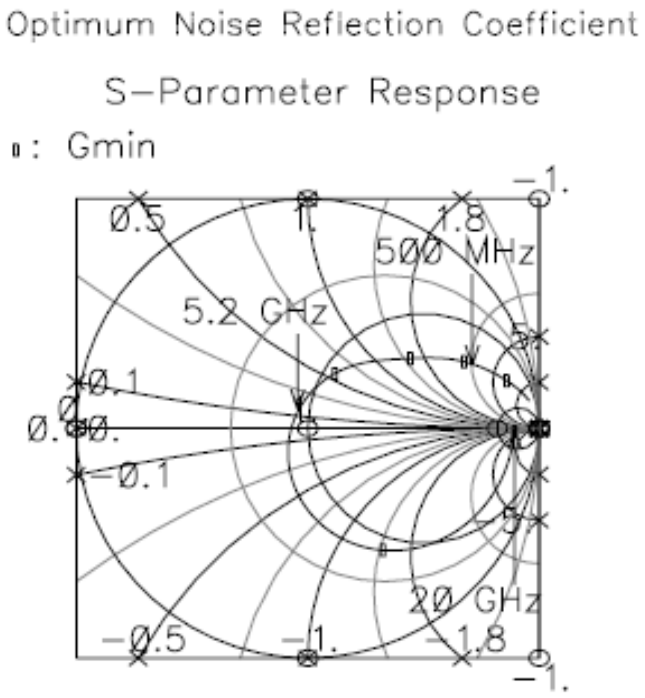


Figure 3-16: Optimum Noise Reflection Coefficient of LNA vs frequency Curve

As seen in Figure 3-15, NF of the circuit is nearly same to the NF_{min} of the circuit which is highly desired. Also observed in Figure 3-17, the input impedance of the circuit gives the best value in the same frequency range with NF. Figure 3-16 provides further details on why the two specifications (NF_{min} and input matching) give the best result in the frequency range of interest, presenting the optimum noise reflection coefficient (ONRC). ONRC provides the best S_{11}, resulting the NF_{min}. As observed in Figure 3-16, for 5.2 GHz, the ONRC of the circuit is very close to the 50-Ω source impedance, indicating the best result for input matching. This is also expected because, as explained in noise matching part, it has provided in Figure 3-6 that the NC curves gives the minimum noise for the impedance value of the same in ONRC curve.

The input matching of our circuit is also adequate for WLAN applications. Figure 3-17 illustrates a good input impedance match of 50-Ω. S_{11} of the circuit is below -15 dB at the frequency of interest. This also shows us that simultaneous input and noise matching is obtained.

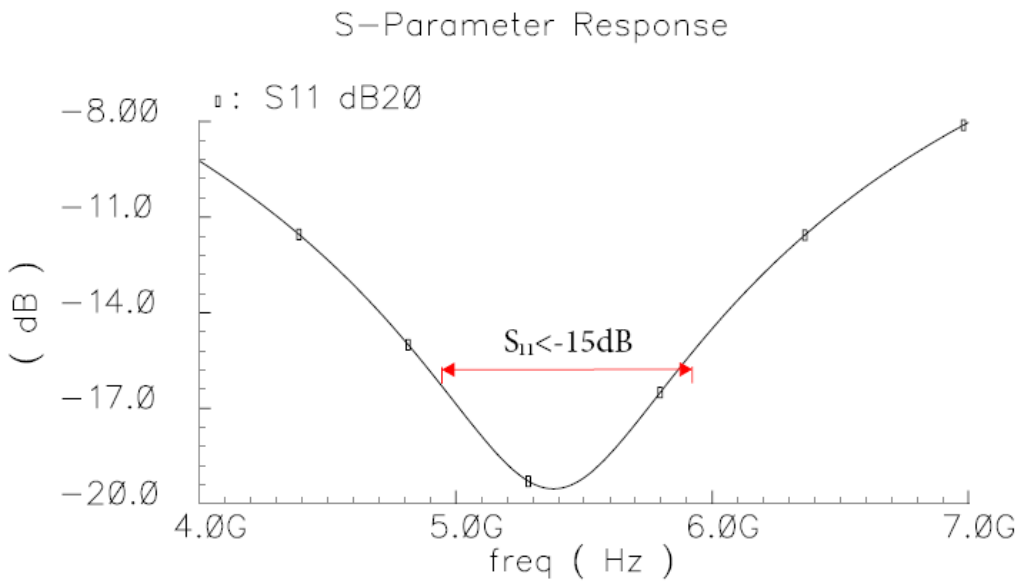


Figure 3-17: Input Matching of the LNA (S_{11})

Impedance matching at the input is always required while at the output it is only necessary with the LNA driving an external image-reject filter, placed between the LNA and mixer. On the other hand, direct on-chip connection between the LNA and mixer provides better linearity and saves the power consumption. But more stringent performance specifications of the image-reject filter are required to avoid noise-figure degradation. In this work, output is also matched to 50-Ω source impedance. The S_{22} result of the circuit is presented in Figure 3-18. In the frequency of interest, S_{22} is smaller than -10dB which is enough for heterodyne transceiver architectures [3].

Due to cascode nature of our circuit, a reverse isolation (S_{12}) of below -63dB is obtained and shown in Figure 3-19, is also a good result [3]. Figure 3-20 indicates that our circuit is unconditionally stable all over the interested frequency range.

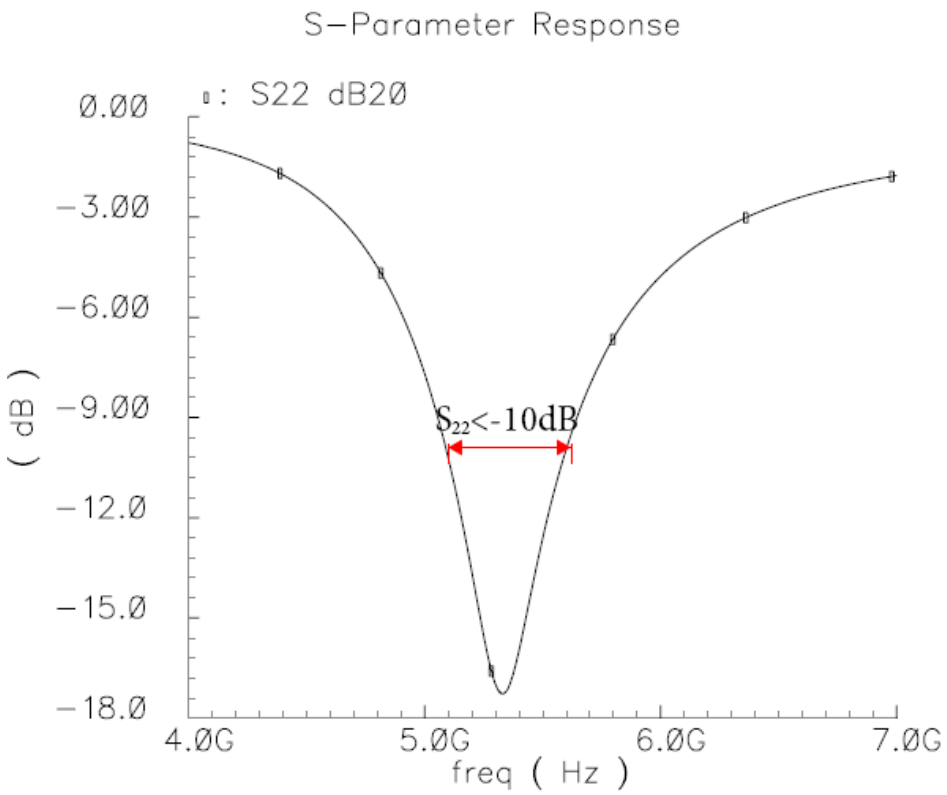


Figure 3-18: Output Matching of the LNA (S_{22})

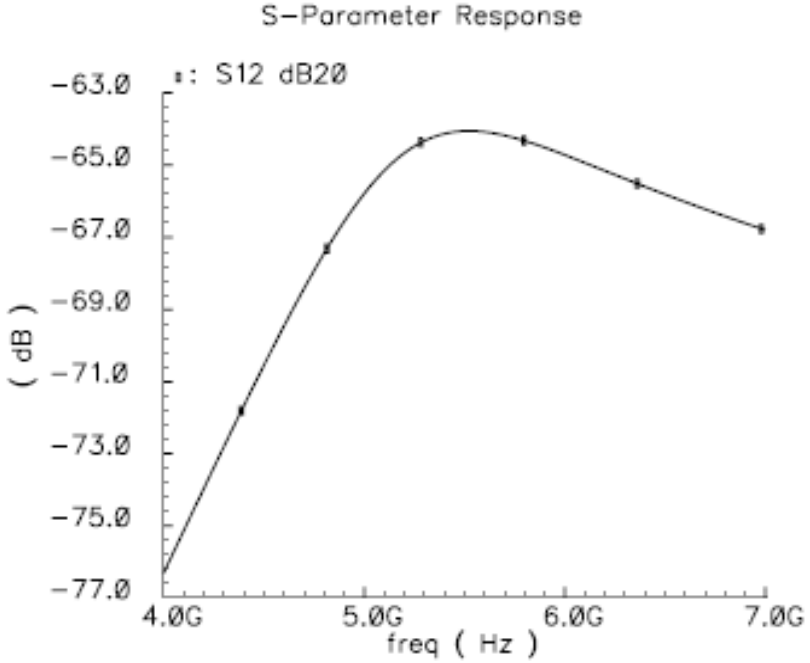


Figure 3-19: Reverse Isolation of LNA (S_{12})

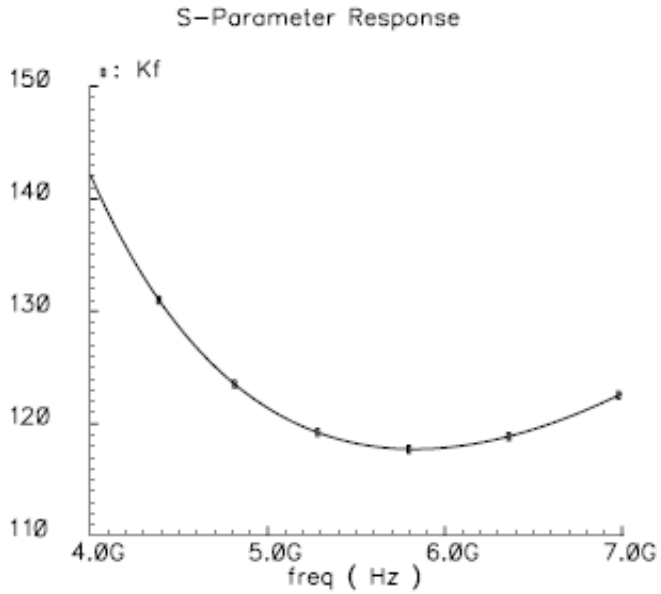


Figure 3-20: Stability Factor of LNA

3.5 Layout Issues

The complete LNA layout, including bias circuitry, is presented in Figure 3-21. All components are on-chip, including the dc blocking and by-pass capacitors. The LNA under study was designed and simulated with a standard 0.35 µm SiGe BiCMOS technology on a p-type substrate. There are four metal layers in this technology and top metal layer has a thickness of 3µm [33], ideally suited for realizing inductors .

Analog circuits usually include resistors for current limiting or voltage division and general biasing circuits. Most processes offer a choice of several different resistor structures utilizing different materials. One type of resistor that can be used in IC is well-resistors. Most important feature of well resistors is the relative high sheet resistance, on the order of 1 to 10 kilo-ohms per square. The disadvantages of well resistors are high temperature coefficients, voltage dependency, and large parasitic capacitances to ground since the well is located close to the substrate. Also another important point for well resistors is, when laying out well resistors, the width should be at least twice as large as the depth of the well. Otherwise the resistor does not achieve full junction depth and the sheet resistance becomes much higher than the values reported by the foundry data sheets

[43]. Metal layer for creating a resistance is sometimes the best choice when small resistances are desired. Sheet resistance of the different metal layers (especially first and second) is typically in the range 20 to 40mΩ/sq. The advantages of metal resistors are low parasitic coupling to the substrate, low-voltage dependency, and low TCs but can give really small values. Also, diffused resistors can be realized in a CMOS process by making contacts to each side of an implanted region Resistors made this way exhibit sheet resistance in the range 20 to 50Ω/sq if silicide blocks are used. Hence, using this resistor type may add extra cost to the manufacturing. This resistor type is not often used, since most CMOS processes offer poly resistors that have equal or greater sheet resistances which has better performance to optimize. Poly-silicon is used in all modern CMOS processes for producing the gate of the MOS transistors. After deposition, the poly is heavily doped to improve conductivity for obtaining high-speed operation of the MOS transistors. The sheet resistance of heavily doped poly lies in the range of 1 to 20 Ω/sq [44]. At en extra cost, a mask can be manufactured that stops heavy poly doping at regions where resistors are desired. As a result, lightly doped poly can be produced with sheet resistance varying between 20 to 1000 Ω/sq [44]. The TC of poly resistors can have both positive and negative values depending on the doping density and the type of doping atoms used. In general, the absolute value of the TC increases with the sheet resistance. For al these reasons, poly capacitors are chosen for realizing the entire resistor in LNA circuit.

In LNA circuit, there are also capacitors in the matching circuits. Also capacitors are used for blocking the DC current. The capacitor choice is also important due to the using area of capacitor. There are two general ways to realize a capacitor in IC circuits. Both plates of a poly-insulator-poly (or simply poly-poly) capacitor are made of deposited poly-silicon that is doped to keep the resistivity low. The bottom plate is usually implemented using the same layer as the poly gate of MOSFETs. The other plate must be supported by a second poly layer.

There are extra processing steps involved in poly-poly capacitors since the insulator is unique to this structure. Of course, the shielding is not perfect and there is a parasitic

capacitance connected between the bottom plate and the substrate. The capacitance per unit area of poly-poly capacitors changes from one technology generation to the next because both vertical and lateral dimensions are scaled. Hence, it is not possible to provide a number that can be universally applied. For example, at the 0.5-μm technology node, the capacitance per unit area was around 1 fF/μm^2. There is a voltage modulation of poly-poly capacitors caused by poly-depletion since the conductivity of the poly-silicon plates is finite. Usually, the voltage dependency can be modeled using a second-order polynomial, which shows the non-linearity of poly-poly capacitors. If the linearity of poly-poly capacitors is not sufficient, metal-insulator-metal capacitors should be used. The drawback of such capacitors is the low capacitance per unit area (typically 0.05 fF/μm^2) [33] since the oxide used between metal layers is quite thick. Such capacitors will not be further discussed here. In modern state-of-the-art processes, MIM capacitors are replacing poly-poly capacitors owing to their improved linearity and mismatch characteristics since the conductivity of the metal plates is higher than that for the corresponding poly-silicon plate. Usually, the MIM capacitor is realized using one of the conventional metal layers as the bottom plate and a dedicated thin metal layer placed between two conventional metal layers to realize the top plate as in the AMS process that we use for fabrication of the designed LNA. Also, in MIM capacitances, the plates of the capacitor are made of metal, reduces the ohmic resistance resulting in a higher quality factor value. All the capacitors used in this design are MIM capacitors due to their linearity. The unit capacitance of the process used for fabrication of the LNA is ~1 *f*F/μm^2 which is close to the poly-poly capacitor value. In RF circuits, sometimes huge DC blocking capacitors are required. In this case, poly-poly capacitors give large values with small area which suitable for DC blocking. But in this thesis, there is no need to large capacitance because all the blocking are performed using the series capacitance of input and output matching networks.

At a 5 GHz of operating frequency, all the paths will have parasitic capacitances, resistances and also inductances. Typical simulators can extract RC parasitic components but inductance extraction is a very much interesting topic for today's RF and Microwave research/company communities. Inductance extraction can also be performed by using

EM solvers but it takes very long simulation time and processor power. Therefore, in this work all the parasitic inductances are extracted by using ASITIC tool. It is a very typical example that some thin paths in layout have an inductance of a few pH. This value is comparable with the emitter inductor of the LNA. Lastly, all the paths in input part of the LNA are realized by using the top metal layer because of the reduction of series resistance. These series resistances are directly adds noise and increase the overall noise performance of the system. LNA circuit occupies an area of 595 × 925 μm^2. It is operated with 3.3 V supply voltage for increasing the output swing of the LNA. It only consumes 10.6 mW power, very low as compared to similar bipolar LNAs [12-16].

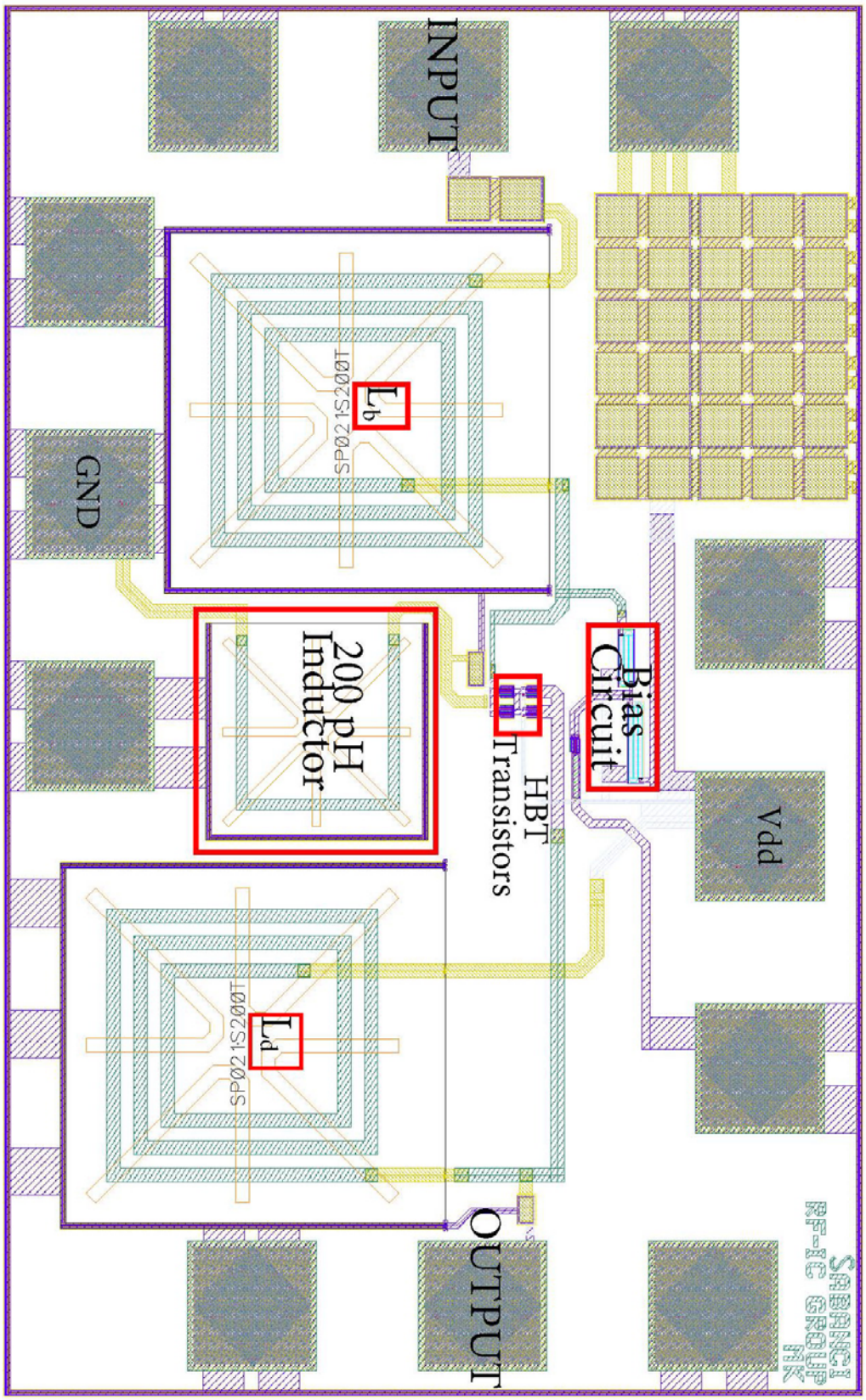


Figure 3-21: Layout of the LNA (595 × 925 µm^2)

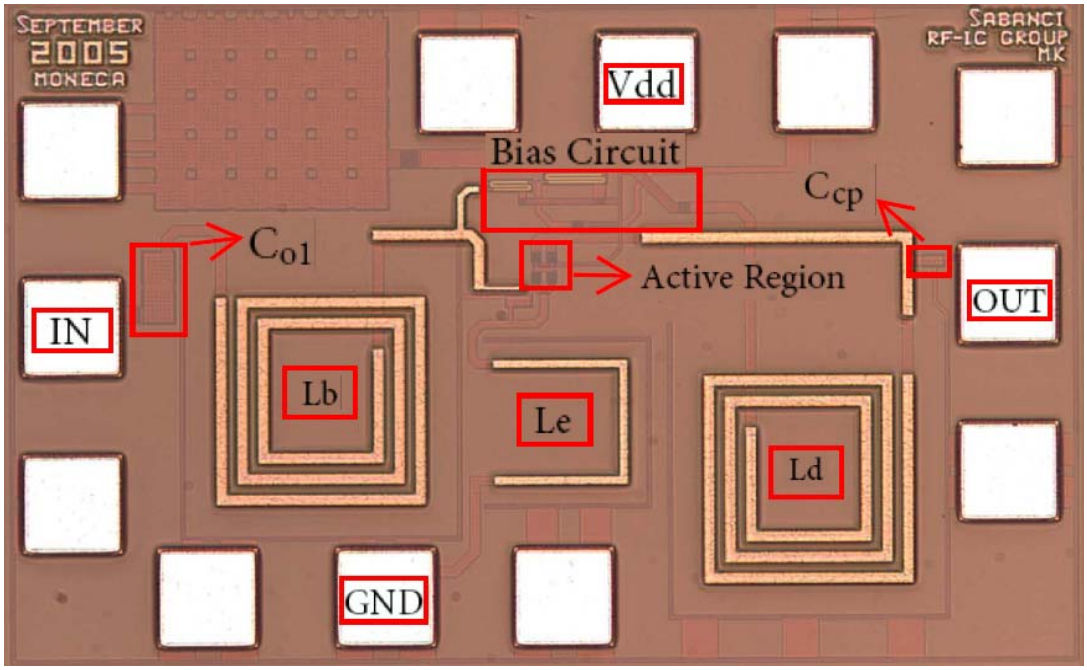


Figure 3-22: Die Photograph of the LNA

3.6 Experimental Results

The LNA has been fabricated using 0.35µm-SiGe BiCMOS technology. Figure 3-22 shows a photograph of the die with an active area of 595×925µm^2 and labeled circuit. The circuit operates with a 3.3 V supply voltage. The measurements are taken by using Agilent 8719ES Network Analyzer, integrated into a Karl-Suss PM5 RF Probe Station.

The measurement result for input return loss of the LNA is given in Figure 3-23. it can be seen that the resonance frequency quite shifts to 6 GHz. But, at 5 GHz the return loss is still under -10 dB.

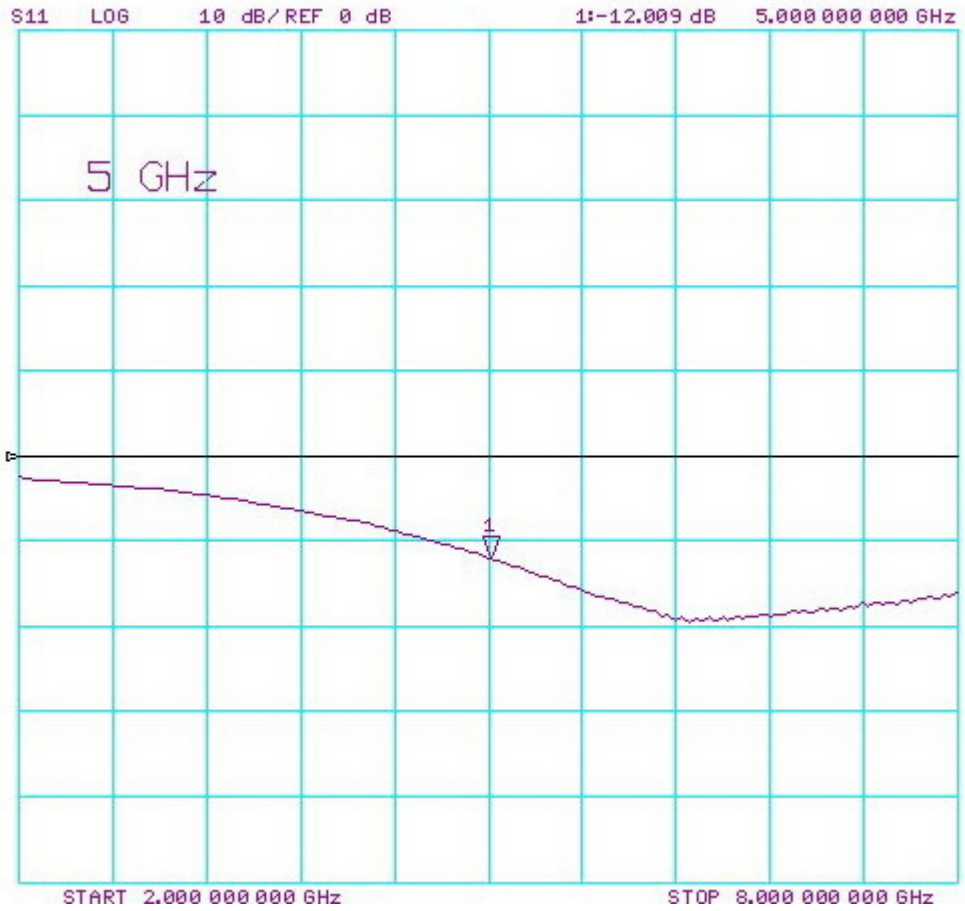


Figure 3-23: Measurement result of S_{11}

The power gain measurement result of the LNA is shown in Figure 3-24. the gain of the amplifier is not expected value of 15 dB. There is a 1-2 dB loss shown in Figure 3-24. It cam be occur due to some voltage drop with substrate and the ground of the circuit. But also the calibration of the measurement systems also affects the measurement results. Gain simulations also performed using new calibration kits and different measuring setups (with signal generator and spectrum analyzer).

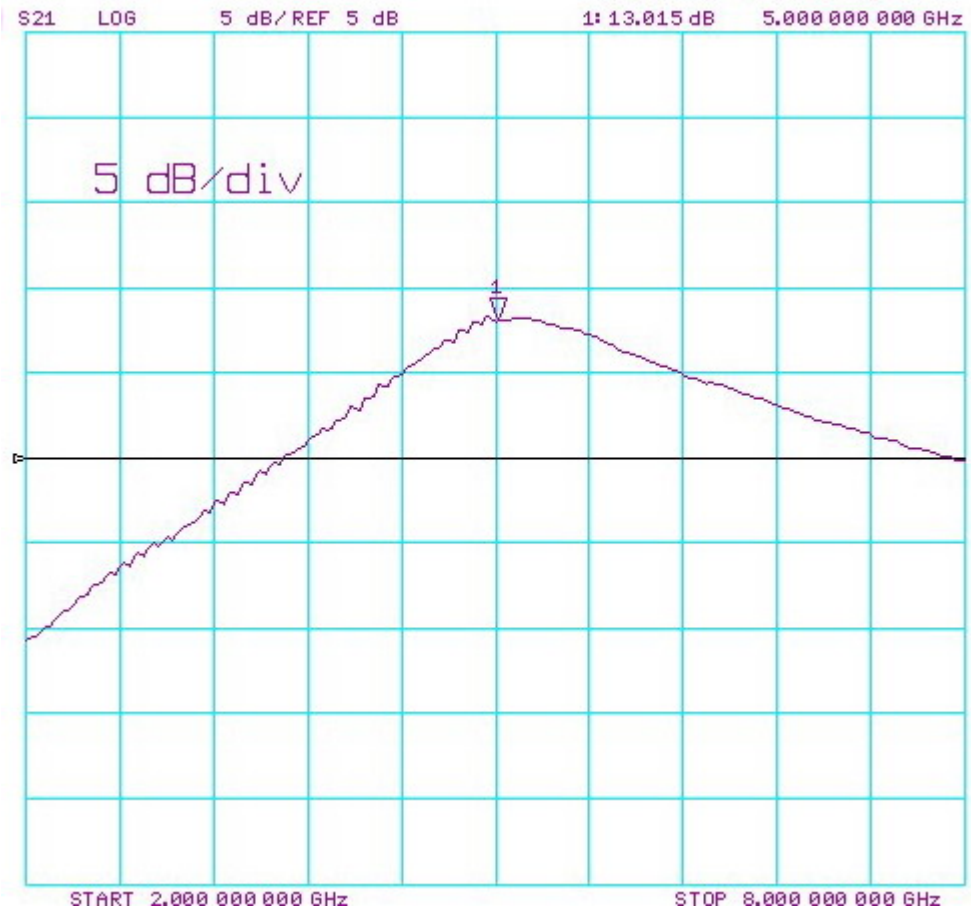


Figure 3-24: Measurement result of S_{21}

The output return loss of the circuit is quite better than expected and shown in Figure 3-25. It can be clearly seen that the output of the circuit resonates at 5-6 GHz frequency range. Also the reverse isolation of the circuit is above 25 dB which is enough for heterodyne receiver architectures [3]. The measurement result of S_{12} is shown in Figure 3-26.

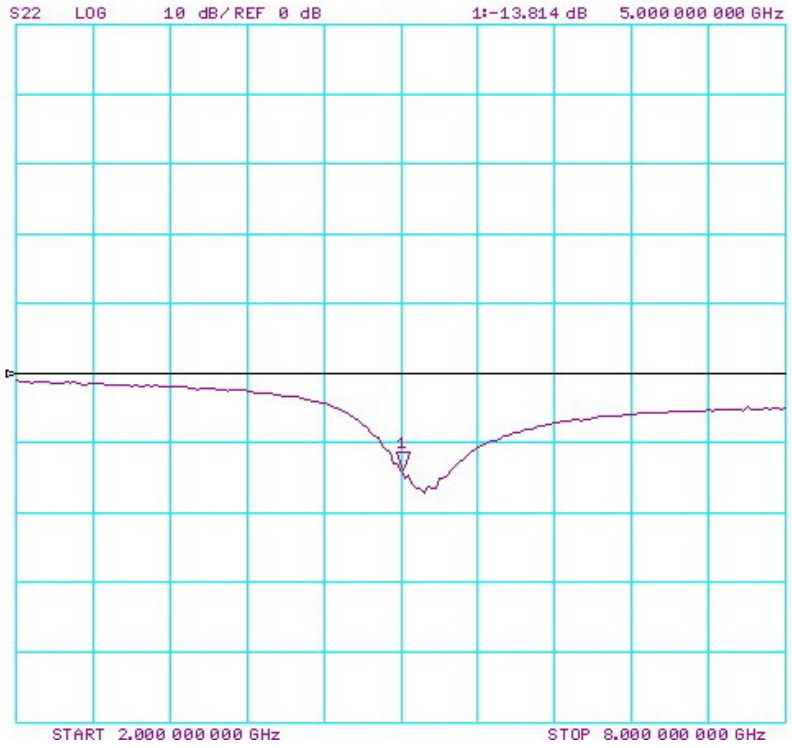


Figure 3-25: Measurement result of S_{22}

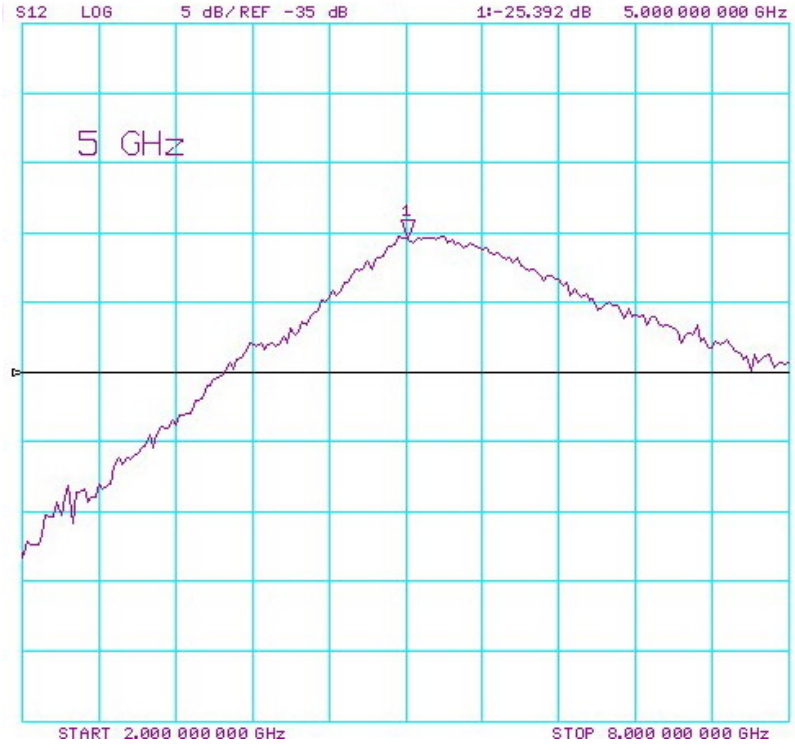


Figure 3-26: Measurement result of S_{12}

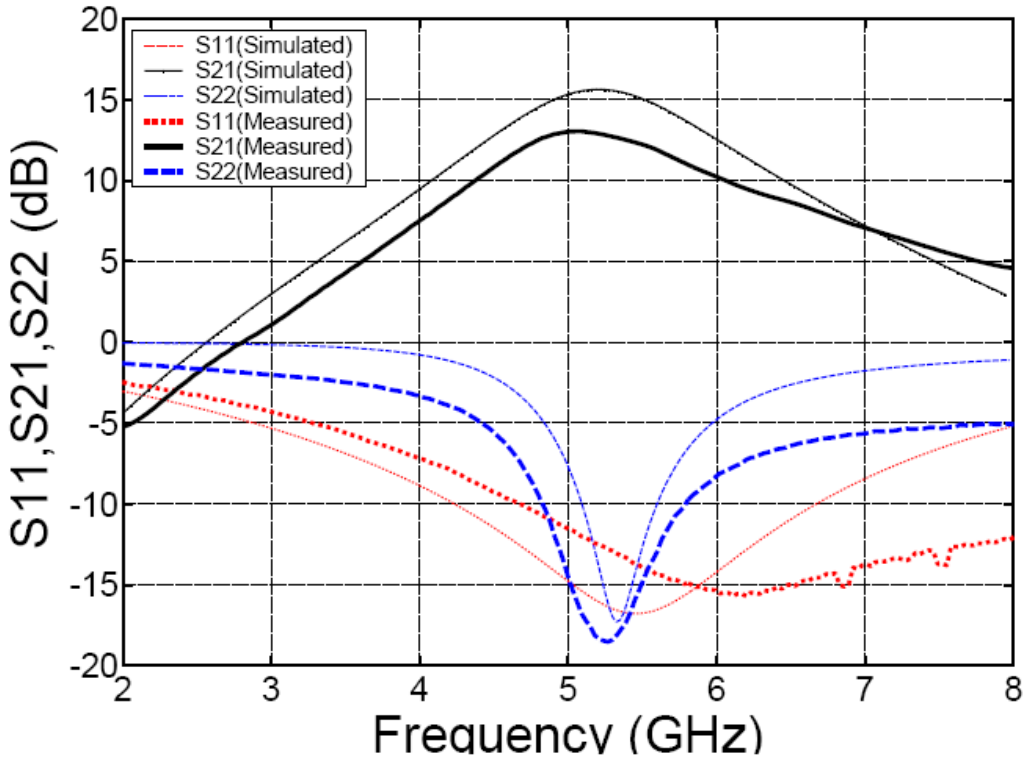


Figure 3-27: Comparison of Measured and Simulated S-parameters

A comparison of simulated and measured S-parameters of the LNA in the 5-6 GHz range is provided in Figure 3-27. These simulations were performed using Agilent Design System (ADS)® and Cadence® design environments. As seen in Figure 3-27, the measured data is very close to simulated data, evidence of good parasitic extraction and compensation process performed for the circuit. Since above 5 GHz of operating frequency, the extraction of inductance becomes very difficult using the conventional circuit simulators, EM solvers, such as MOMENTUM®,HFSS® or MOMENTUM® should be used to extract the parasitic inductances.

The measurement results show that power gain of the LNA deviates by 2-dB from the simulated value of 14-dB. Figure 3-27 also illustrates a good input impedance match of 50-Ω. S_{11} of the circuit is below -10 dB at the frequency of interest. However, the resonance frequency slightly shifts to 6 GHz, instead of the designed/simulated value of 5.5 GHz, due to an unexpected drop of the value of emitter inductor. Impedance

matching at the input is always required while, at the output, it is only necessary if/when the LNA driving an external image-reject filter, placed between the LNA and mixer. In this work, the output of the LNA is also matched to 50-Ω source impedance.

The noise figure of the LNA is still being measured and not available for reporting at the time of submitting the thesis. The simulation setup is created and early noise figure results are taken in the range of 3-4 dB levels but the calibration and measurements are still on going. Noise figure of the circuit is measuring using Y-method which is performed by applying a specified noise with noise sources and observing the total noise level at the output of the LNA with spectrum analyzer. The Agilent E4407B spectrum analyzer has a noise figure module which make easy to measure the noise figure and phase noise of RF circuits.

4

Chapter 4

SPIRAL INDUCTORS AND RFMEMS TECHNOLOGY

4.1 Introduction

One of the critical limitations on integrating high performance LNAs on chip are spiral inductors. Unlike resistors and capacitors, whose their values are well estimated except for variations due to the process (around 10%), on-chip spirals are still not well optimized in terms of shape, metal width, metal spacing, quality factor and value. Modern CMOS process usually consists of a heavily doped epi layer which is highly conductive; eddy current induced by the magnetic field of the inductor onto the substrate degrades the inductor performance.

For all frequencies, an ideal passive component must show constant values with constant phase. But all non-ideal components exhibit change in value with frequency. For an inductor, self-resonance frequency is important because beyond this frequency the element becomes capacitive and the quality factor is practically zero [45].

4.2 Problems in IC Technology

Typically, standard inductor designs on CMOS and SiGe substrates have resulted in a Q of 12-18 at 2 GHz and 16-22 at 6 GHz. Now, we can use electromagnetic simulation software like HPADS MOMENTUM, ASITIC to optimize the inductor geometry for the highest inductance and lowest associated series resistance. Also, the substrates used today have a relatively high resistivity, reducing the eddy current losses underneath the inductor.

The inductors are integrated on the top metal layer using a 3-um-thick conductive layer and separated from the silicon substrate by using 2 to 6-um-thick oxide layers. The parasitic capacitances to the substrate are reduced by oxide layers and they allow the integration of large value inductors without having problems with the inductor resonant frequency. But the main problems in the BiCMOS processes are;

- Thickness of the metal line is thin; therefore the sheet resistance is high. For example, the process that that used in this project is AMS 0.35 SiGe BiCMOS process and the thickness of the last metal layer is typically 2,5 μm. This gives only 15 m-ohm/square sheet resistance. This is high sheet resistance for inductor design and therefore the quality factor are generally limited about 10-12 [33].

- The other problem is the coupling capacitance between coil and the substrate. Because the k value of the material between the coil and substrate is not small enough, the capacitance between them is not too small. Generally the oxide layer is about 6 to 10 μm between the substrate and the last metal layer. This parasitic capacitance resonates with the inductance of the coil and determines the self-resonance frequency of the coil. In AMS process, the self-resonance frequencies of the inductors are about 6-8 GHz, which is very low for high frequency applications.

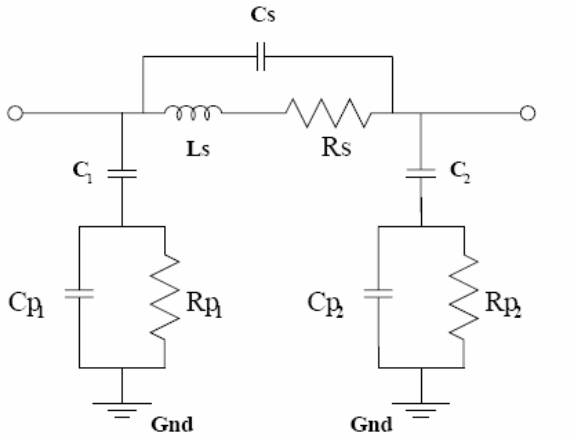


Figure 4-1: Spiral Inductor Model

4.3 Theory of the Planar Type Spiral Inductors

A general model of a spiral inductor is shown in Figure 4-1. L_s is the low frequency inductance, R_s is the series resistance of the coil, C_s is the capacitance between the different windings of the inductor and includes the fields in air and in the supporting dielectric layers, C_1 is the capacitance in the oxide (or polyamide) layer between the coil and the silicon substrate, C_p is the capacitance between the coil and the ground through the silicon substrate, and R_p is the eddy current losses in the substrate. This model is the most frequently used small signal model by industry and academic labs because it fits very well with Y and S-parameter measurements of planar inductors.

4.4 Frequency Response of Planar Inductors

The low frequency value of planar inductors is generally obtained by using Greenhouse formulas but an accurate equivalent model of a planar inductor can be obtained using a full-wave electromagnetic simulator such as ADS-Momentum, ASITIC or other EM programs. The simulated S-parameters are typically converted to Z or Y parameters and then fitted to obtain accurate values for L_s, C_s, C_p and R_s. In general, Ls and Rs are fitted using low-frequency simulations, while C_p and C_s are fitted around the resonant frequency of the planar inductor [41]. At low frequencies, the impedance of the inductor model is:

$$Z = R_s + jwL_s \tag{4.1}$$

However, at high frequencies, the capacitances must be taken to account. Generally, R_p can be neglected and C_1 and C_{p1} are lumped together. This means the model can be simplified by ignoring the coupling capacitances of the windings and the capacitance between the coil and the ground through the silicon substrate. This model is also used in the electromagnetic simulation tool "ASITIC" and shown in Figure 4-2 [41].

4.5 Q of the Planar Inductors

At low frequencies, and for medium values of L_s resulting in $X=jwL_s=25$ to 70 ohm, the capacitances can be neglected and the model simplifies to a series L_s, R_s circuit. The inductor Q is defined as

$$Q = \frac{Energy\ stored\ in\ the\ inductor}{Energy\ lost\ in\ a\ cycle}$$

$$= -\frac{\mathrm{Im}(Y_{11})}{\mathrm{Re}(Y_{11})} \tag{4.2}$$

$$\cong \frac{wL_s}{R_s}$$

This definition is not accurate around the resonant frequency of the inductor. The resonance occurs due to the effect of the parasitic capacitances, and it is unavoidable in inductors unless capacitance is reduced to zero.

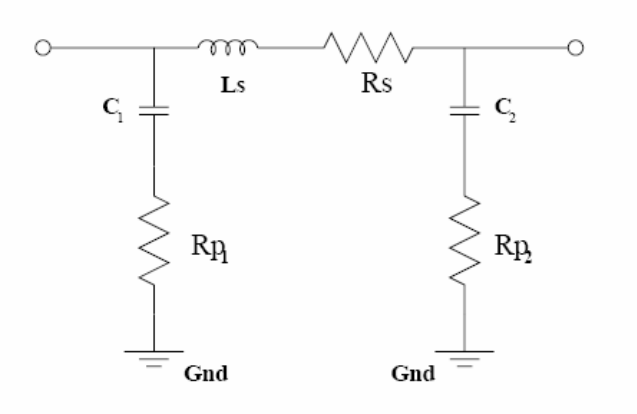


Figure 4-2: Inductor Model used for ASITIC Simulations

4.6 Effect of the Metallization Thickness

Increasing the conductor thickness since it reduces the series resistance can enhance the Q value of spiral inductors. Series resistance is the most important parameter that reduces the Q value of the inductor below 3 GHz [39]. Even though the thick metallization is a non-standard IC processing, it could be achieved after the standard IC processing for the rest of the circuit. Above 5-μm thickness of copper, electroplating technique is adequate. It is experimentally observed that enhancing the thickness of the metallization from 4.5 μm to 9 μm and placing inductors on top of a 10 μm polyimide (or BCB) layer improves the Q factor by 93%, compared with standard inductors fabricated in silicon substrate [46]. It is important to note that in the case of planar inductors, there is an additional resistance that is given by the induced eddy currents within the coil itself. A reduction in the series resistance greatly increases the Q at low to medium frequencies, but has virtually no effect on the reactance or the resonant frequency of the planar inductor.

4.7 Effect of the Parasitic Capacitance

The parasitic capacitance in the substrate is the dominant capacitance for medium to large value inductors, and the inductor resonant frequency is given using the circuit of Figure 4-2.

$$f_r \cong \frac{1}{2\pi\sqrt{L_s C_p}} \tag{4.3}$$

In general, $C_s << C_p$ and can be neglected in the resonant frequency calculations [39]. However, for micro-machined inductors with a very low parasitic capacitance and a high resonant frequency, C_s must be taken into account in the circuit model. In this case, the resonant frequency becomes:

$$f_r \cong \frac{1}{2\pi\sqrt{L_s (C_p + C_s)}} \tag{4.4}$$

A reduction in the parasitic capacitance not only makes the resonant frequency higher but also results a large-reactance, high-Q inductor at high frequencies. The reason is that the reactance is proportional to f , while the series resistance is approximately proportional to $\sqrt{f}$.

In this project, the solution for improving the performance of the LNA is, using high-Q MEMS inductors. The approach is fabricating the MEMS inductors using in-house capabilities of Sabanci University clean-room and performing the integration of these inductors to fabricated LNA die. For this, the modeling of the inductors and the fabrication steps of MEMS inductors are given in following part of this chapter.

4.8 RF MEMS Inductors

Extensive research is being conducted in the area of wireless front-end circuitry aiming at the construction of efficient passive components such as inductors. Inductors are found e.g. in filters, impedance matching networks and voltage controlled oscillators. The performance of both transceivers and receivers depends heavily on this component.

MEMS inductors aim to increase the performance of on chip inductors in terms of quality factor “Q” and resonant frequency. MEMS inductors try to achieve higher Q than the off chip discrete inductors. Two methods are used for this purpose in the MEMS structures: Bulk micromachining and surface micromachining [47]. In bulk micromachining the wafer is been processed and the substrate has been eliminated from underneath the spiral trace. In Surface micromachining, layers are deposited on the substrate and solenoid-like inductors are created above the substrate [48].

Micromachined inductors will therefore be used for high-Q applications (Q>30) in low noise oscillators, high-gain amplifiers, on-chip matching networks, and integrated LC filters. Currently, thick metal layer and substrate etching are additional fabrication processes and increased cost [49].

MEMS fabrication procedures are still not well-suit for typical BiCMOS IC processes and increase the cost of the product. A new post process called Above-IC is very compatible for post-processing of the typical IC processes [50]. In this thesis, suspended micro-machined inductors and inductors that are formed using Above-IC technology are fabricated. The goal of the fabrication is produce high-Q inductors and increasing the performance of the LNA.

Design Example

The inductor models can be designed with 3 masks in this project. The important parameters for an inductor are width, thickness, number of turns, outer diameter, inter diameter and air gap thickness. The inductance of the coil is not related with the process. So, the inductance of the coil can be achieved for specified lengths and spacing as [51]:

$$L(nH) = 0.03937 \frac{a^2 n^2}{8a + 11c} \quad \textbf{(4.5)}$$

Where n: the number of turns,

$$a = \frac{(D_0 + D_i)}{4} \quad \textbf{(4.6)}$$

$$c = \frac{(D_0 - D_i)}{2} \quad \textbf{(4.7)}$$

D_0 and D_i are the outer and inner diameters of the rectangular inductor. For the 30u width, 30u spacing, 500u outer diameter, 200u inner diameter and 3 number of turns;

$$a = \frac{500 + 200}{4} = 175 \quad \textbf{(4.8)}$$

$$c = \frac{500 - 200}{2} = 150 \quad \textbf{(4.9)}$$

And the inductance is;

$$L(nH) = 0.03937 \frac{175^2 .3^2}{8.175 + 11.150} = 3.5578 \quad \textbf{(4.10)}$$

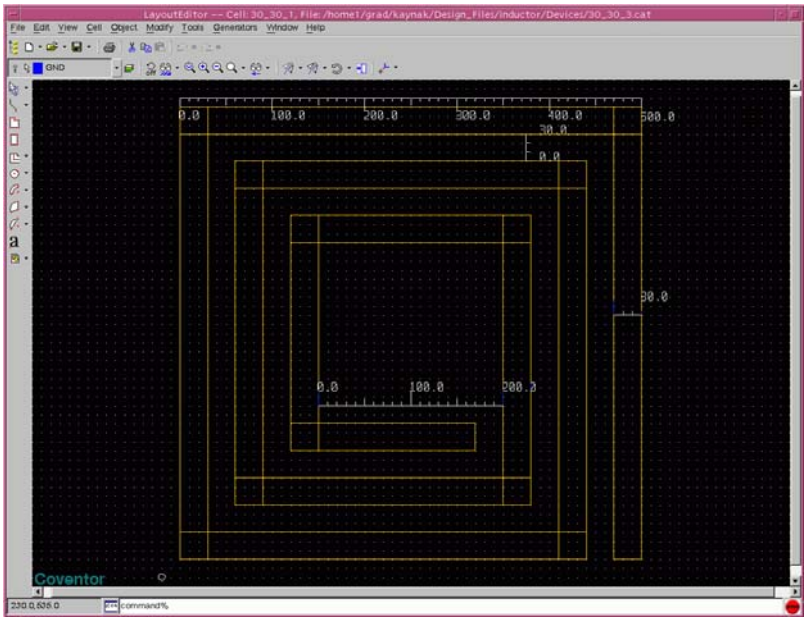
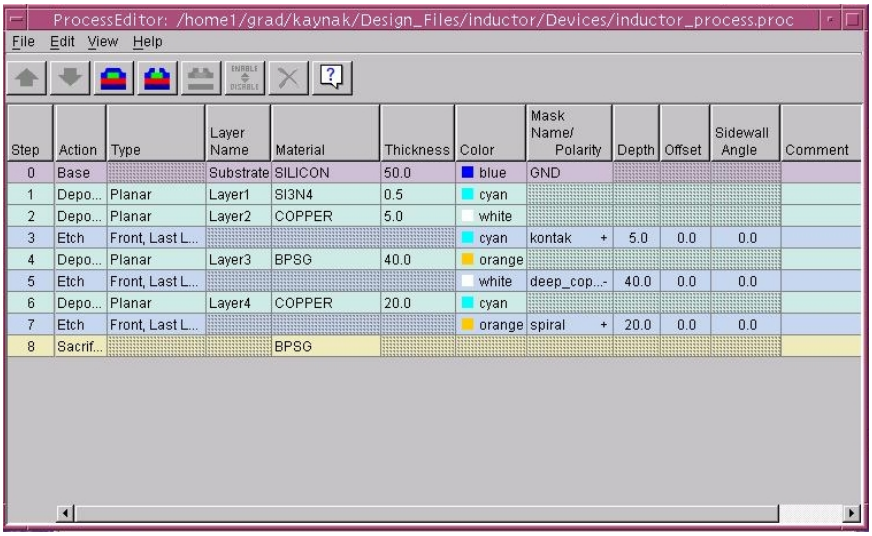


Figure 4-3: Coil of the Inductor

The inductor mainly consist of the coil part which is spiral, the contacts (in and out ports) and the via part which connects the contact part and the coil. The spiral is 3 turns, 30um in width, has 30um spacing and its outer diameter is 500um. The simulations of the designed inductors are performed using simulators such as Coventor® (MemHenry Module), ASITIC, and Agilent MOMENTUM®. A typical design and simulation procedure using Coventor MemHenry environment is given below:

The coil mask is shown in Figure 4-3. Vias have the size of 30 µm-30 µm. And the contacts have the size of 120 µm -120 µm. This is large because, while measuring the inductor, we need to large contacts.

Inductor fabrication is a 4 layer and 3 mask process. Copper used as the material of inductor for simulation. First a dielectric nitride layer of 0.5 µm thickness is deposited on to the silicon wafer. Then the sacrificial layer PSG of 40 µm thickness is deposited on to the nitride. The contact holes are filled with copper and then it is etched with the contact mask. Then the sacrificial layer of 40 µm thickness is deposited on to the copper contacts and it is etched with via mask negatively to open holes for vias like we did for the



Step	Action	Type	Layer Name	Material	Thickness	Color	Mask Name/ Polarity	Depth	Offset	Sidewall Angle	Comment
0	Base		Substrate	SILICON	50.0	blue	GND				
1	Depo...	Planar	Layer1	SI3N4	0.5	cyan					
2	Depo...	Planar	Layer2	COPPER	5.0	white					
3	Etch	Front, Last L...				cyan	kontak +	5.0	0.0	0.0	
4	Depo...	Planar	Layer3	BPSG	40.0	orange					
5	Etch	Front, Last L...				white	deep_cop...-	40.0	0.0	0.0	
6	Depo...	Planar	Layer4	COPPER	20.0	cyan					
7	Etch	Front, Last L...				orange	spiral +	20.0	0.0	0.0	
8	Sacrif...			BPSG							

Figure 4-4: Process flow of Inductors

contacts. Then copper is deposited on to the sacrificial layer planar type and it is etched with via mask. Then 30 μm thick copper is deposited and it is etched with the coil mask. The process flow is shown in Figure 4-4. Finally we etch the sacrificial layers and get out final structure shown in Figure 4-5.

In order to make analyses first we have to create meshed structure. Meshing is very important for the sensitivity of the simulation. Meshed structure is shown in Figure 4-6.

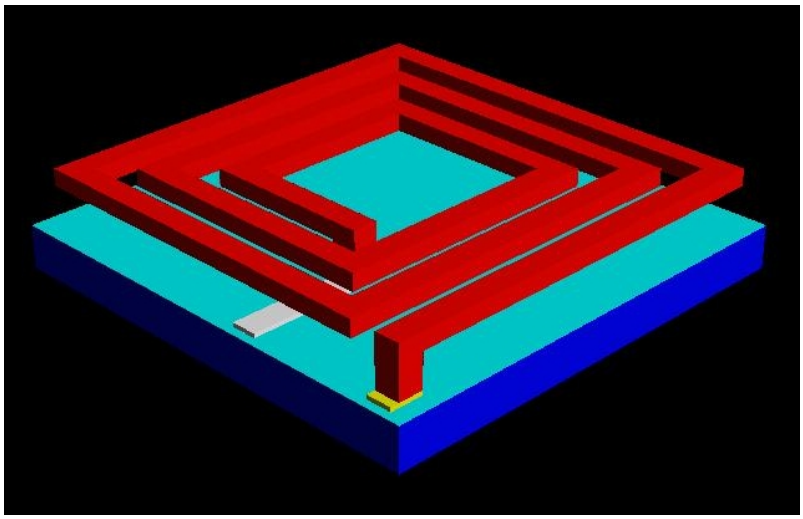


Figure 4-5: Final view of simulated inductors

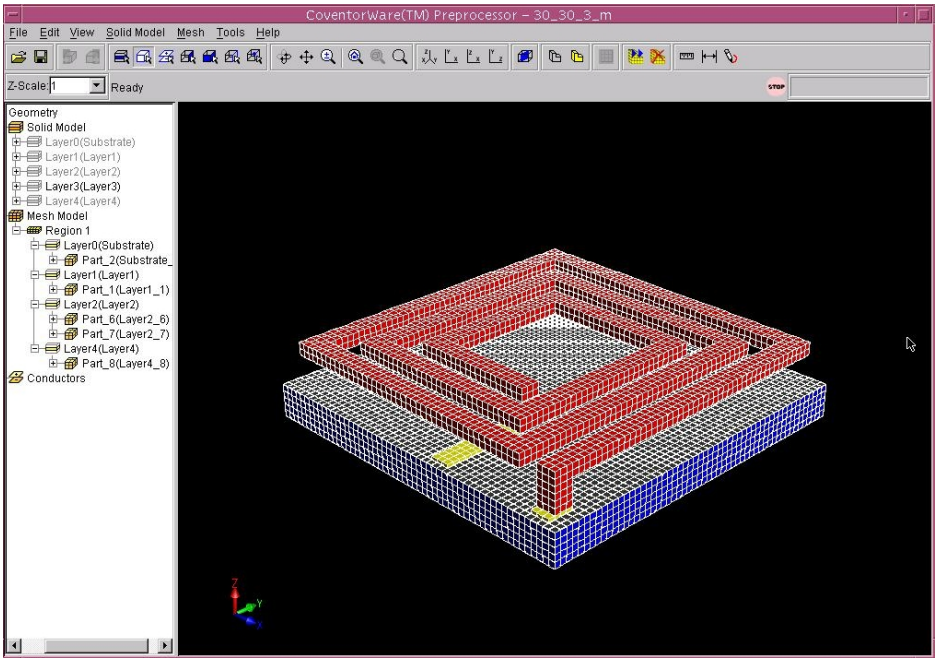


Figure 4-6: Meshed structure of inductor

Memhenry® module is the most suitable simulator for analyzing the inductor. The Memhenry® module computes the frequency-dependent resistance and inductance matrices for the set of conductors. In this project, we can only simulate the inductor at the frequency of 5GHz. There are a lot of different topologies simulated and the inductance-resistance values are listed in Table 4-1. (All of the values are find at the frequency of 5 GHz)

Table 4-1 includes the inductance values from 1 nH to 8 nH which is the suitable range for IC design. These simulations give an idea of the MEM inductor topologies and the Q values that are elegant for RFIC design. The most important part of the designing inductors is creating the substrate files for simulators. Coventor defines the material properties and do not need any substrate file. But this is not the case in other simulators like ASITIC or Agilent MOMENTUM®.

All these simulations are performed under ideal cases but fabricating these inductors is not an easy step. Fabrication description and the problems occurs during fabrication are given in next part of this chapter.

Table 4-1: Inductor Simulation Results

Width of the coil (µm)	Spacing (µm)	Outer Diameter (µm)	Air Gap Thickness (µm)	Thickness of the coil (µm)	Number of turns	L (nH)	R (Ω)	Q
20	10	500	40	20	1	**1.1**	**0.8**	**40**
20	10	500	40	20	2	**3.3**	**2.4**	**42**
20	10	500	40	20	3	**5.8**	**4.6**	**39**
20	10	500	40	20	4	**8.2**	**7.4**	**34**
20	20	500	40	20	1	**1.1**	**0.8**	**41**
20	20	500	40	20	2	**3**	**2.2**	**43**
20	20	500	40	20	3	**5**	**3.9**	**40**
20	20	500	40	20	4	**6.5**	**5.8**	**35**
20	30	500	40	20	1	**1.1**	**0.8**	**41**
20	30	500	40	20	2	**2.8**	**2.0**	**44**
20	30	500	40	20	3	**4.3**	**3.4**	**39**
20	30	500	40	20	4	**5.2**	**4.8**	**34**
30	10	500	40	20	1	**1**	**0.5**	**56**
30	10	500	40	20	2	**2.7**	**1.3**	**63**
30	30	500	40	20	1	**1**	**0.5**	**54**
30	30	500	40	20	2	**2.3**	**1.1**	**65**
30	30	500	40	20	3	**3.3**	**1.6**	**65**
30	30	500	40	20	4	**3.6**	**1.9**	**60**

4.9 Fabrication of Suspended Inductors

4.9.1 Fabrication Steps of Suspended Inductors

Mainly the process steps of the inductors include four layers and three masks. The process starts with the deposition of Si_3N_4 that is used for insulation. Then copper layer is deposited on to nitride layer and patterned to form the bottom electrodes. Following this step, sacrificial layer, which is AZ5214 photoresist in our case, is coated that directly

Table 4-2: Si_3N_4 RF sputtering parameters

Type	RF magnetron sputtering
Target	Si_3N_4
Temperature	250 ^oC
Cleaning	10min
RF power	150 W
Ar flow	35 sccm
Chamber Pressure	$2x10^{-2}$ mbar (GV5 position 650)
Deposition time	60 min

defines the spacing of the inductor from the ground plate. Then openings for anchors is opened on the sacrificial layer and copper is deposited to fill these openings and in parallel to form the top metal layer. Next step is to pattern the top layer and form the inductor. Finally the sacrificial layer is released and our inductor is created.

- **Deposition of Nitride**

After the p doped 100 oriented silicon wafer is cleaned with general cleaning recipe 0.3 μm thick Si_3N_4 layer is deposited using RF magnetron sputtering from a high purity Si_3N_4 target. The chamber is heated up to 250 ^oC and then plasma cleaning is applied to Si_3N_4 target with 120 W RF power, 35 sccm argon (Ar) flow and $2x10^{-2}$mbar chamber pressure for 10 minutes. After that deposition step is started with 150 W RF power, 35 sccm Ar flow and $2X10^{-2}$mbar chamber pressure for 60 minutes resulting ~300nm of oxide. The parameters are given in Table 4-2.

- **Deposition of Aluminum**

The aluminum deposition started directly following the nitride deposition. Al deposition is made by DC magnetron sputtering using high purity Al target. As a first step target

Table 4-3: Al DC sputtering parameters

Type	DC magnetron sputtering
Target	Al
Temperature	150 ^{o}C
Cleaning	3min
DC power	200 W
Ar flow	35 sccm
Chamber Pressure	$2x10^{-2}$ mbar (GV5 position 500)
Deposition time	20 min

cleaning is carried out with 150W DC power, 35 sccm Ar plasma and main chamber pressure of $2x10^{-2}$ mbar for 3 minutes in order to clean the residues on the target which can be affect the deposition quality. After that the DC power adjusted to 200W and with the same plasma (35 sccm Ar and $2x10^{-2}$ mbar chamber pressure) the deposition is carried out at 150^{0}C for 20 minutes resulting in 300 nm Al layer. The parameters are given in the Table 4-3.

- **Patterning and Etching of Aluminum**

Following aluminum deposition, the wafer is taken to wet bench in order to pattern the metal contacts. Shipley's S1813 positive tone photoresist (PR) is used for photolithography step. First the sample is spin coated with PR using spinner. The program is selected as 500 rpm for 5 seconds to spread the PR, then 2000 rpm for 10 seconds and finally 4500 rpm for 45 seconds which results in 1.3µm uniform PR layer. Then 35 sec. of soft bake applied on hot plate with 95^{0}C temperature. Then the sample is taken to contact aligner and exposed to UV light for 35 seconds using bottom contacts mask. After that step, sample is directly put in the Shipley's MF 319 developer for approximately 45 sec. to remove the photoresist from the parts that is not covered with mask. The develop time is directly related to hard bake and exposure time. Sometimes the duration of the develop time is increased to 1 minute because of the quality of

Table 4-4: S1813 Photolithography parameters

Spinning	500rpm-5sec./2000rpm-10sec./4500rpm-45sec.
Soft Bake	95^{o}C Hot Plate 35 sec.
Expose	35 sec.
Develop	40-60 sec.
Hard Bake	105^{o}C Hot Plate 60 sec.

transparency masks such that the light areas of the mask do not passes the light as much as glass masks. This time is optimized for each mask by repeating this step and inspecting it under optic microscope. After we have good patterns the sample is put on the hot plate again for hard baking at 105^{o}C temperature for 60 seconds. Hard bake step hardens the PR in order to make it unaffected from wet etching. All these parameters are listed in Table 4-4.

Last step in the forming process of bottom electrodes is wet etching of the Al layer that has PR patterns on it. Wet etching is chosen for patterning process because of it is easy and fast process. . Al etchant is selected as $16.H_3PO_4$-$1.CH_2COOH$-$1.HNO_3$-$1.H_2O$ with an etch rate given as 2600-6600 A^0/min [52]. The wet etching takes about 1 minutes approximately and finally print our mask to the metal layer [52]. Finally the remaining PR is removed with acetone rinse for 2 minutes and isopropanol rinse for 2 minutes. Also 2 min O_2 plasma descum is applied to remove the PR completely. Resulting bottom contact is illustrated in Figure 4-7.

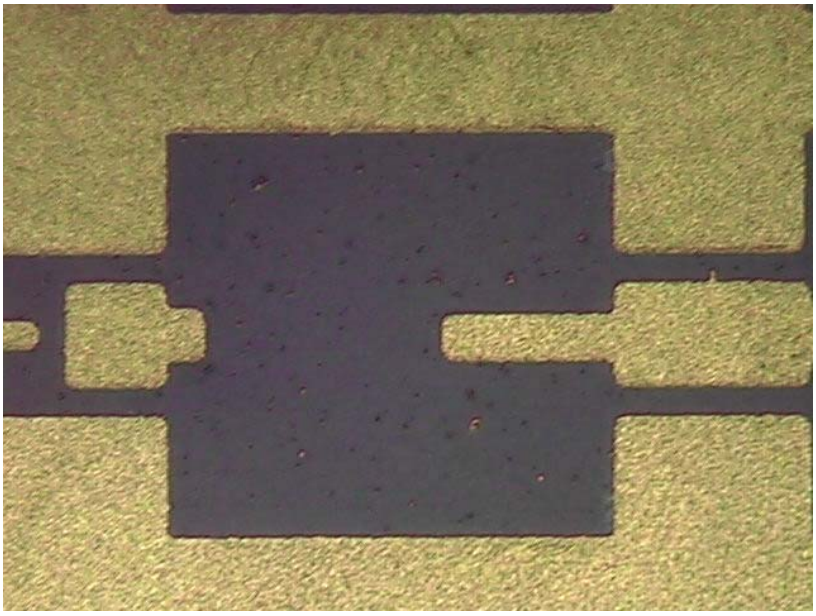


Figure 4-7: Bottom contacts (Al) of the fabricated inductor

- **Coating and Patterning of Sacrificial Layer**

After the electrodes are patterned, dual tone photoresist AZ 5214 is spin deposited in order to form the sacrificial layer. Photoresist is used as sacrificial because it is easy to deposit and made the process simpler and also it is easier to release it than other sacrificial layers. PR is spin coated at 500 rpm for 5 sec., 2000 rpm for 10 sec. and 4500 rpm for 45 sec. resulting in a thickness of 1.4 μm. Then the sample is soft baked on the hotplate of 95^{o}C for 1 min. Next step is to expose the coated PR under UV light with the anchor opening mask for 20 second. Then the sample is again put onto hot plate at 110 ^{o}C for 30 second and once mode the sample is flood exposed with no mask that inverts the mask. Developer step follows this, for 40 sec. with AZ 726 developer. Summary of the AZ5214 negative tone photolithography steps are given in Table 4-5. Resulting structures are shown in Figure 4-8 and Figure 4-9.

Table 4-5: AZ5214 Photolithography parameters

Spinning	500rpm-5sec./2000rpm-10sec./4500rpm-45sec.
Soft Bake	95°C Hot Plate 60 sec.
1st Expose	20 sec.
2nd Bake	110°C Hot Plate 30 sec.
Flood Expose	60 sec.
Develop	40 sec.
Hard Bake	105°C Hot Plate 60 sec.

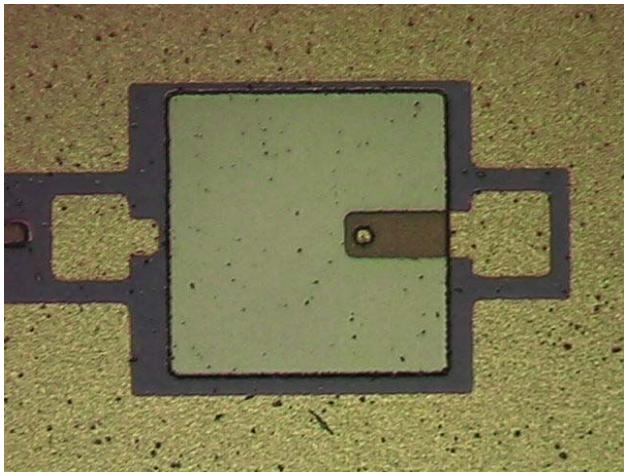


Figure 4-8: Sacrificial layer coated and patterned on bottom electrodes

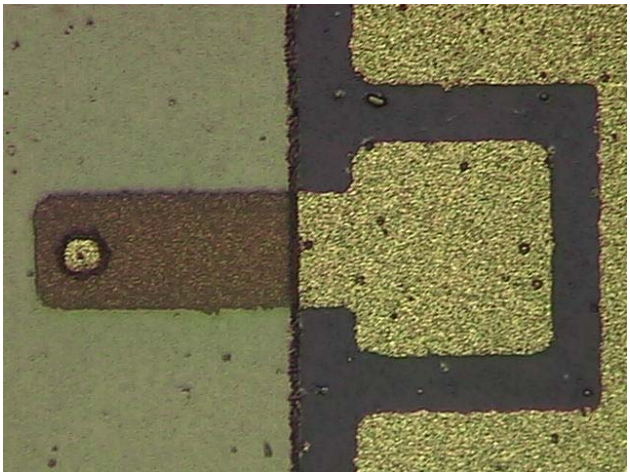


Figure 4-9: Closer view of the via openings in sacrificial layer

- **Top Copper Layer Deposition and Patterning**

This top layer deposition of copper is one of the most crucial steps in process flow. The copper layer has to fill the anchor openings and connect well to the coil. This step is repeated for a few times because most of the times when releasing the photoresist sacrificial layer, the top coil part is corrupted. Deposition time finally increase to 60 min resulting in 2.5 μm that fill the anchor openings well as well as the anchor parts stick to the coil part better.

Copper deposition is made by DC magnetron sputtering using high purity Cu target. As a first step target cleaning is carried out with 150W DC power, 35 sccm Ar plasma and main chamber pressure of $2x10^{-2}$ mbar for 5 minutes in order to clean the residues on the target which can be affect the deposition quality. After that the DC power adjusted to 200W and with the same plasma (35 sccm Ar and $2x10^{-2}$ mbar chamber pressure) the deposition is carried out below 100^0C for 60 minutes resulting in 2.5 μm Cu layer. The temperature is kept low in order not to harden the PR sacrificial layer which will be problem in releasing it. The parameters are given in the Table 4-6.

Following that the sample is patterned again using PR with parameters in Table 4-4. After that the Cu layer is patterned the uncovered parts are removed using the Cu etchant. Cu etchant is selected as 4% HNO_3 (nitric acid) with an etch rate of 40nm/sec. is used to pattern the top metal and the etchant is applied for around 60 second.

- **Releasing of Sacrificial Photoresist**

Acetone is used to release the underlying photoresist sacrificial layer. As seen as an easy step this part is the most problematic part of the inductor fabrication steps. Because the photoresist sticks to copper very well, when rinsed with acetone, in some parts the underlying photoresist are not released. In some parts, acetone removes the photoresist, however; it also removes the top part of the inductors. One other problem is when acetone is exposed to photoresist; it cannot completely remove the photoresist such that some parts stick to coil. There are techniques such as super critical carbon dioxide drying

Table 4-6: Cu DC sputtering parameters

Type	DC magnetron sputtering
Target	Cu
Temperature	<100 ^{o}C
Cleaning	5min
DC power	200 W
Ar flow	35 sccm
Chamber Pressure	2x10^{-2} mbar (GV5 position 500)
Deposition time	60 min

and isotropic dry etching that helps to remove the remaining photoresist. Using dendritic material as a dry-release sacrificial layer to create micro-scale gaps is another solution to this problem. Dentric material is released with no remaining when they are exposed to temperatures like 500 ^{o}C. These are left for future work. There are images of some inductors after photoresist release shown in Figure 4-10, Figure 4-11.

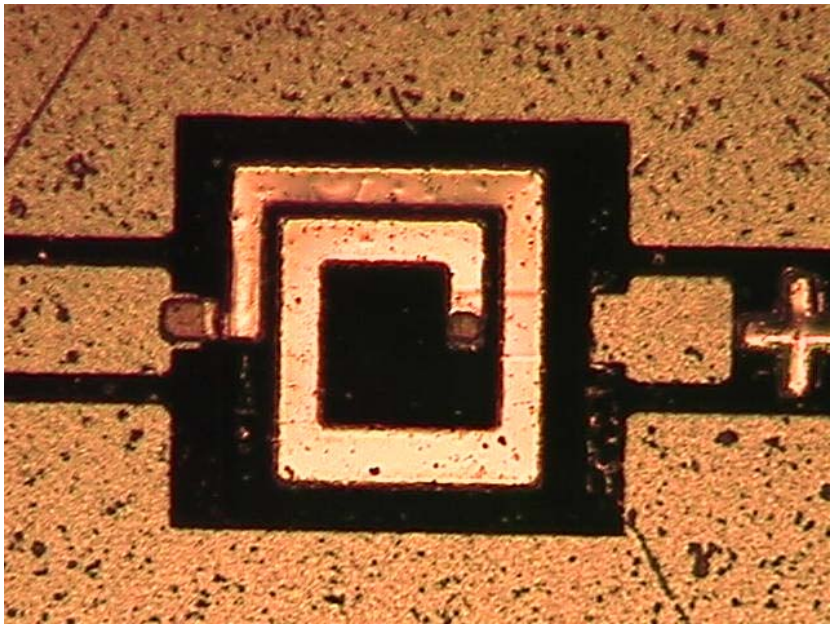


Figure 4-10: Final structure of 1.5 turn square spiral inductor

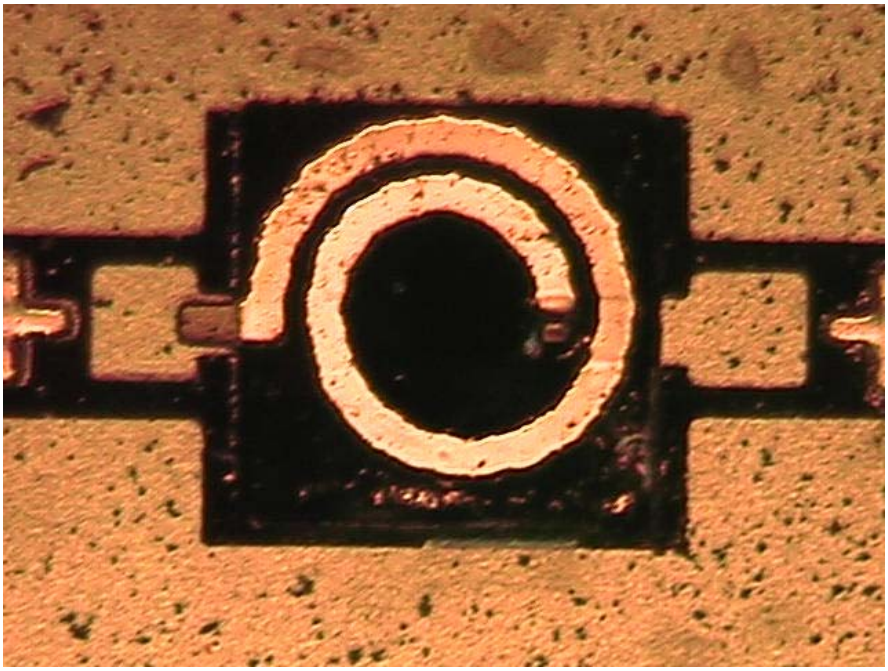


Figure 4-11: Final structure of 1.5 turn spiral inductor

4.10 Above-IC Process

4.10.1 Description of the Above-IC Process

The passive components can be built using an IC-compatible process that is called "Above-IC" [53]. The main advantage of this fabrication technique is the ability to build the inductors and varactors directly over the electronic circuit. The performance of ordinary coils fabricated using standard IC process is usually poor. The main reason for the degradation of the performance of a coil is the presence of a resistive substrate. Another key issue is the intrinsic resistance of the coil, mainly determined by the nature of the metal and its cross-section. Thus, the use of a thick metal layer greatly improves the performance of the coil. The process described here allows us to fabricate high-performance passives in a simple deposit and pattern technology, without the need for complex steps. At the same time this optimizes the isolation from the resistive substrate and the coil resistance.

Below is the process flow of the Above-IC process and Figure 4-12 illustrates this process flow;

(A) Starting wafer with the top metal level and the openings in the passivation
(B) Deposition of the low-k dielectric
(C) Opening of vias to the top metal layer
(D) Deposition of the seed metallic layer
(E) Deposition and patterning of the thick photo-resist
(F) Electro-deposition of the thick coil layer
(G) Removal of photo-resist.
(H) Removal of the seed metal layer
(I) Thick low-k dielectric deposition as the passivation layer or;

Above the normal IC-passivation, a thick low-k dielectric layer is deposited. The passivation layer should have clearances in the location where the inductor will be connected to the IC-circuitry. The vias needed to contact the underlying metal connections are then patterned. The vias ensure the electrical connection between the last IC metal layer and the inductor. A thick electroplated copper layer is realized in order to create the coil. In order to protect the coil, a passivation layer can be deposited as the last step. This fabrication flow is carried out below 250 °C, which is suitable for post-IC processing [54].

4.10.2 Fabrication of Above-IC Inductors

Like MEM inductors, Above-IC type inductors also have high Q values. The thick BCB layer decreases the parasitic capacitance to the substrate. The main reason is low k value of the BCB material. This is the way that to achieve high Q values in inductors.

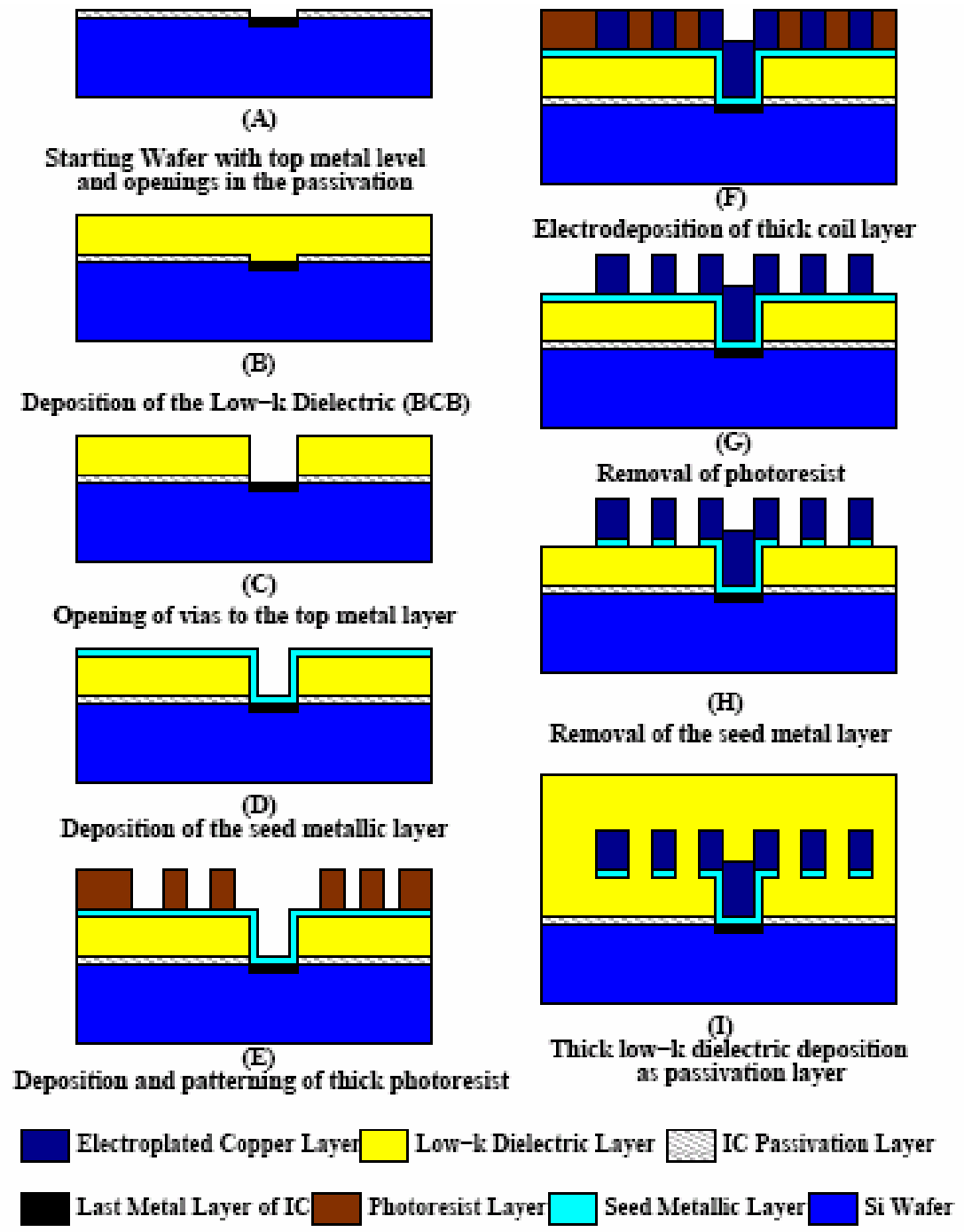


Figure 4-12: Above-IC Process Flow

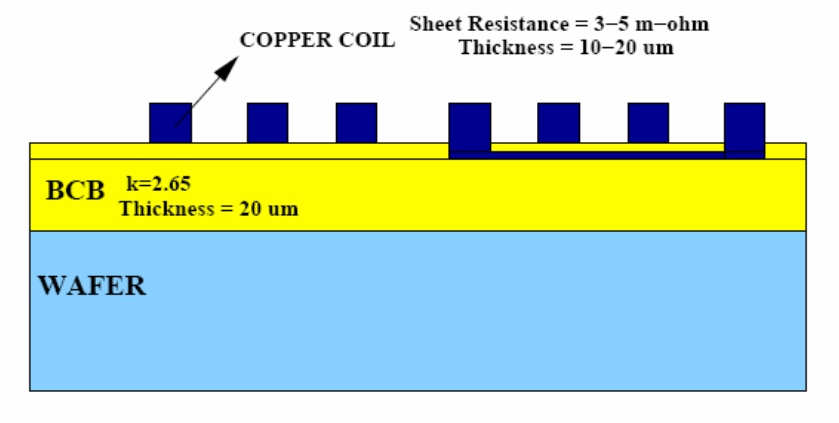


Figure 4-13 Cross-view of Above-IC Process

Decreasing the parasitic capacitive effect is important but another important thing that increase Q value is decreasing the sheet resistance. This is accomplished by using thick copper layer. Thick copper cannot be achieved by using thin film deposition methods like sputtering. The method that used widely for thick copper layer is electroplating method. By using this method, thickness of above 15 µm can be achieved. Also we start to generate the setup of copper electroplating and achieved copper layer thickness above 10 µm by using in house capabilities. Also by using the electroplating method, the quality of the copper is better than the sputtering method. This is directly affects the sheet resistance of the coil. All the thickness values can be seen in the Figure 4-13.

Micromachined-inductors at different geometries/values (1 – 8nH) designed and simulated using electromagnetic (EM) simulation tools such as ASITIC® and MOMENTUM®. Additionally, full EM simulations of the selected geometries are carried out using HFSS®. BCB (Benzocyclobutene) is chosen in this work as the passivation layer because it allows thick layers (13.8µm at 1000rpm) and low-k value of 2.65 [55]. Different spiral inductor types with different turns ranging from 0.5 to 3 and with 3µm thickness were fabricated over 10 µm BCB layer. Figure 4-14 shows the cross-section of one of the fabricated inductors. Figure 4-15 and Figure 4-16 shows the fabricated

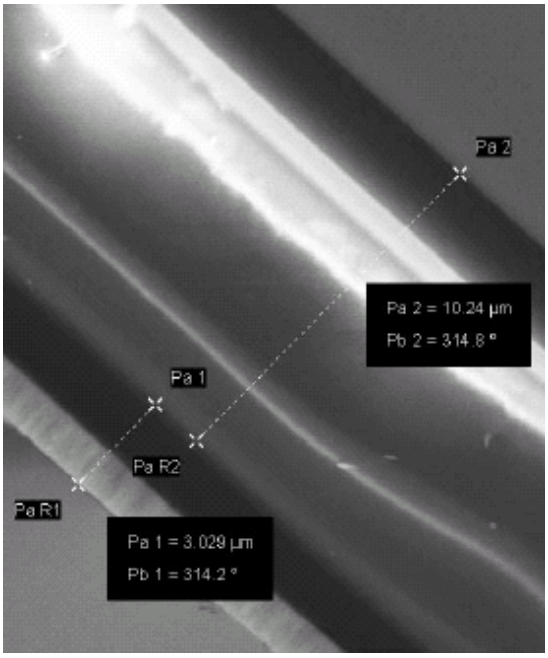


Figure 4-14: Cross-Section of the fabricated inductor above the BCB layer

inductors, designed for 1-nH and 1.58-nH, respectively. These values are suitable for the integration of fabricated LNA which improves the noise performance of the LNA. Next part includes the approach for integration of the RFMEMS inductor with fabricated SiGe BiCMOS LNA.

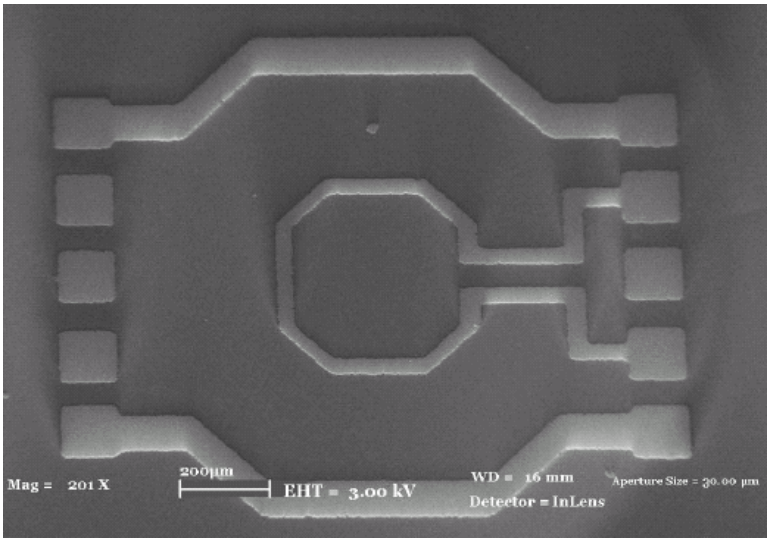


Figure 4-15: Fabricated 1 nH inductor

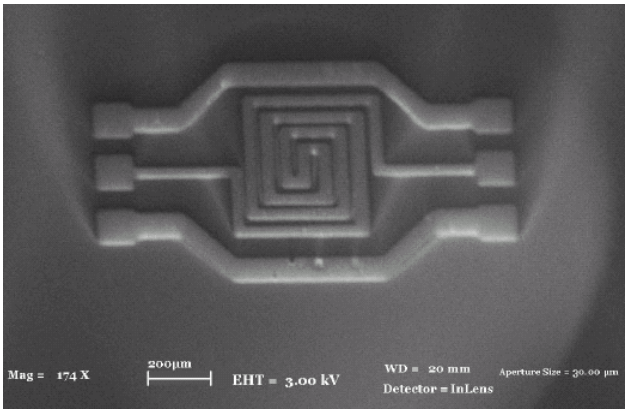


Figure 4-16: Fabricated 1.58 nH inductor

4.11 Measurement of MEM Inductors

The last step of our work is measuring the fabricated inductor values. For this measurement we must consider the Z parameters of these inductors. A typical set of test structures for measuring an inductor in a pad frame is shown in Figure 4-17.

High-frequency ground-signal-ground probes will be landed on these pads so that the S parameters of the structure can be measured. However, while measuring the inductor, the pads themselves will also be measured, and therefore two additional de-embedding structures will be required. Once the S parameters have been measured for all three structures, a simple calculation can be performed to remove the unwanted parasitics [51]. The dummy open and dummy short are used to account for parallel and series parasitic effects, respectively. The first step is to measure the three structures, the device as $Y_{DUT,}$ the dummy open as $Y_{dummy\text{-}open}$, and the dummy short as $Y_{dummy\text{-}short.}$ Then the parallel parasitic effects represented by $Y_{dummy\text{-}open}$ are removed, leaving the partially corrected device admittance as Y'_{DUT} and corrected value for the dummy short as $Y'_{dummy\text{-}short}$.

$$Y'_{DUT} = Y_{DUT} - Y_{dummy\text{-}open}$$

$$Y'_{dummy\text{-}short} = Y_{dummy\text{-}short} - Y_{dummy\text{-}open}$$

The final step for measuring the inductor is to subtract the series parasitics by making use of the dummy short. Once this is done, this leaves only Z_{device}, the device itself.

$$Z_{device} = Z'_{DUT} - Z'_{dummy\text{-}short}$$

Where Z'_{DUT} is equal to $1/ Y'_{DUT}$ and $Z'_{dummy\text{-}short}$ is equal to $1/ Y'_{dummy\text{-}short}$.

The measurements of the fabricated inductors are still on-going. The inductance values of interest are very low which makes measurement process harder because of the parasitic effects. Also the calibration of the measurement devices is being optimized to achieve more realistic results. This work is also defined as the future work of the thesis.

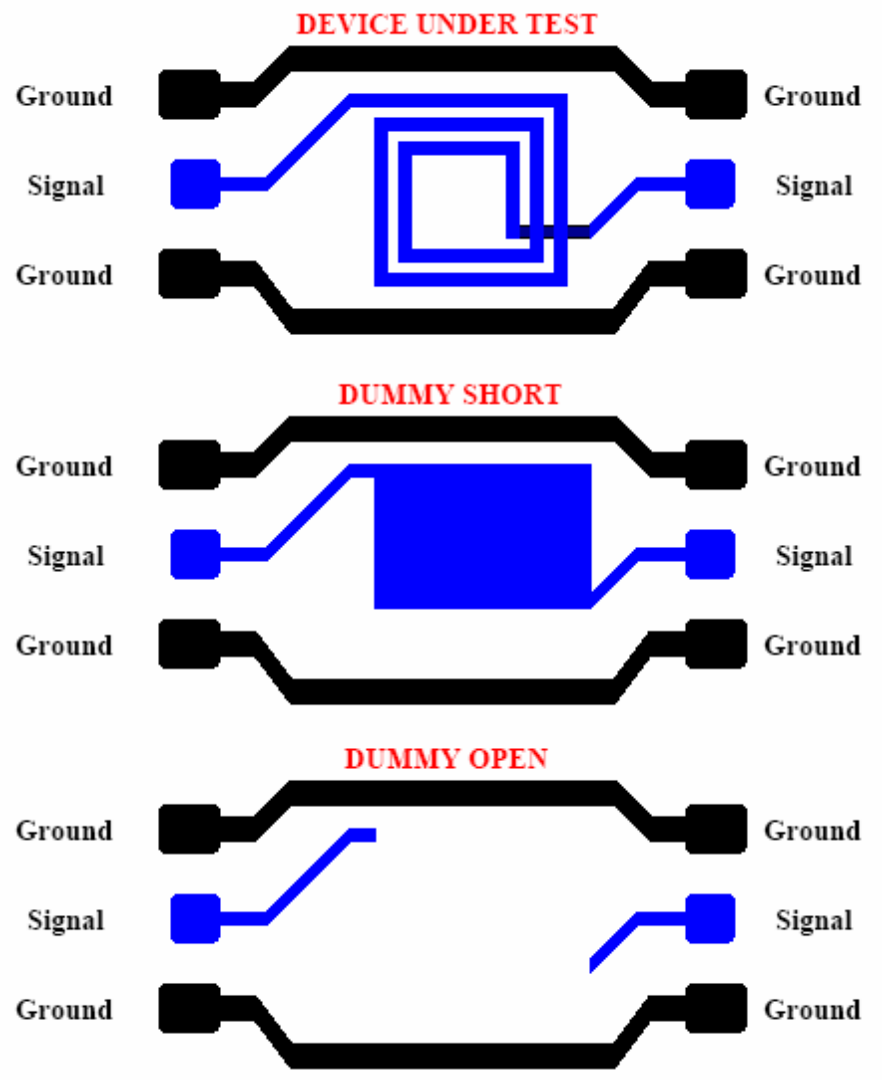


Figure 4-17: Test structures for measuring the inductor

4.12 Performance Improvement of High-Q RFMEMS Inductors: LNA Example

The receiver block mainly specifies the sensitivity of the overall transceiver architecture, whose major block is the LNA, specifying overall NF. In low noise applications, most common topology is the cascode-connected, common-emitter LNA with inductive emitter degeneration, shown in Figure 4-18 and fabricated using 0.35 µm SiGe-BiCMOS process.

Based on the analysis that we have performed on this circuit shows the noise generate by L_1 affects the noise figure performance of the circuit up to %20. This effect is simulated for quality factors, ranging from 5 to 100, and plotted in Figure 4-19.

It is illustrated that quality factors higher than 30 improve the NF of the LNA from 2.8dB to 1.8dB. All the noise contributors to the NF of the circuit are shown in Tab. 1. For an example, addition of series resistance of L_b, increases the noise figure from 2.1 dB to 2.8 dB.

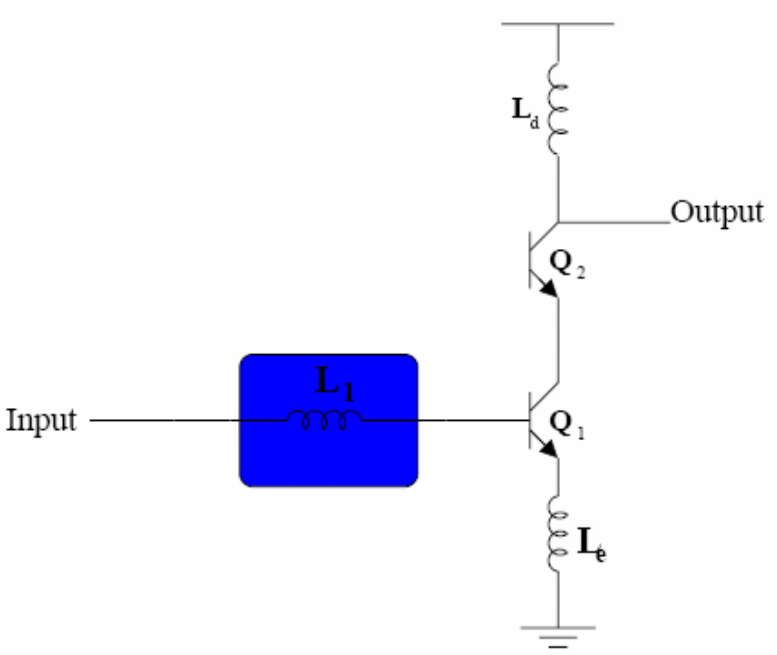


Figure 4-18: Inductive degenerated cascode LNA

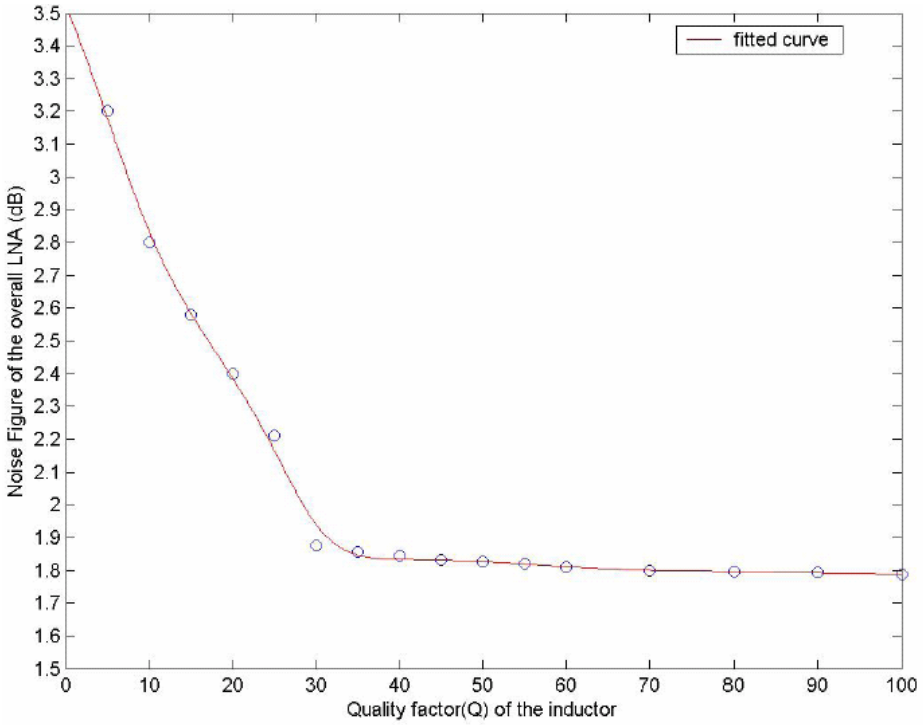


Figure 4-19: NF of the LNA for different Qs of L_1

The fabricated RFMEMS inductors will be integrated to the LNA test structure which is shown in Figure 4-20. In this test structure, the LNA was fabricated without the L_1 inductor and this inductor will be formed using RFMEMS inductors via bond-wire integration. Also, the post processing of the test structures will be performed using Above-IC process and will also be mentioned in future work part.

Table 4-7: Noise Contributors

Source of the Noise	Contribution to Overall NF (%)
RF Port (R_S)	48
Transistors	28
Parasitic components of L_b	21
Others	3

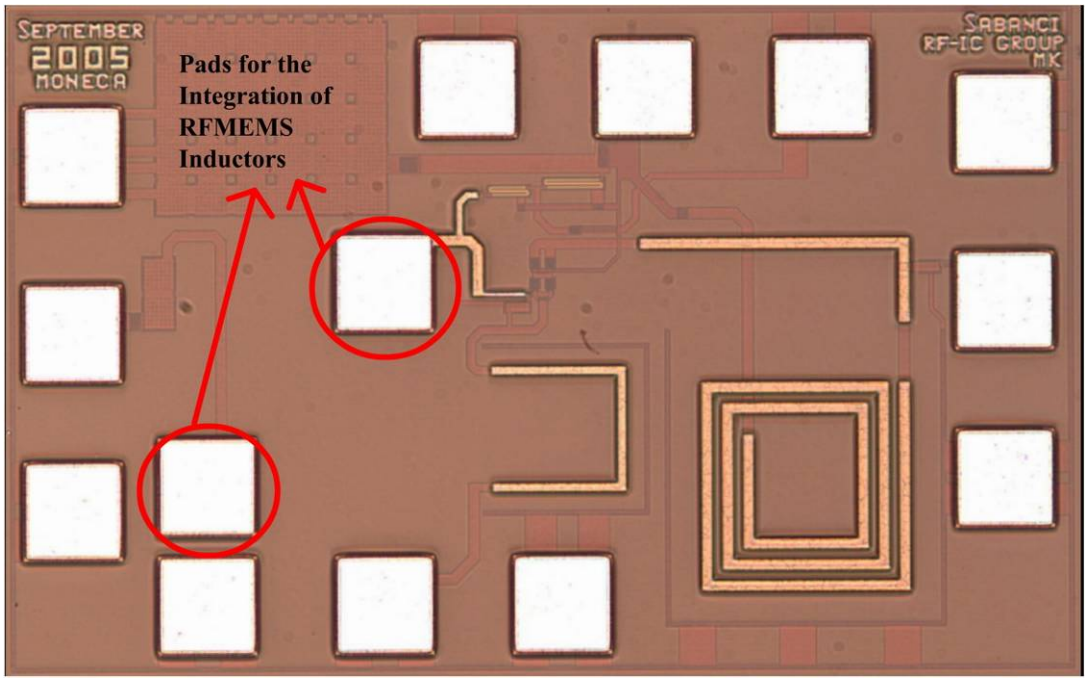


Figure 4-20: Test structures for RFMEMS inductor Integration

5

Chapter 5

CONCLUSION AND FUTURE WORK

This thesis presented a study on designing low noise amplifier for IEEE 802.11a WLAN applications. It began with an explanation of the background and the fundamental principles of designing RFICs at high frequencies. It then briefly explained the design techniques of amplifier circuits and making this amplifier has a low noise. As the frequency increases, it can be realized that the parasitic components starts to dominate the some parts of the circuit. The important parts started related to this concern which takes the most time of the thesis. Electrical simulators can extract parasitic resistances and capacitances easily but inductance extraction is quite different from other extractions. Especially in high frequency circuits, mutual inductances of the close inductors should be taken into account. These are all related to how the layout is drawn. The extraction of the inductors started using some 3D EM solvers like HFSS or Coventor. But the extraction of simple inductor takes to much time if the desired accuracy is high. ASITIC extraction tool is used for all extraction of simple lines for finding the effective inductance of these lines. Some parasitic inductance values was extracted which are extremely affects the performance of the circuit. So, it can be clearly said that, the parasitic inductances of paths should be taken into account for accurate simulation results. Also if the inductors are not far away from each other, the mutual inductance extraction should be performed.

In this thesis, three inductors are not close to each other and the distance between them is minimum ten times of the width of anyone which the case that mutual inductance could be ignored. However, critical paths are extracted and the specified values of inductors are added to extracted view of the circuit which is already includes the parasitic resistance and capacitances.

The designed LNA is fabricated using 0.35 SiGe technology and the measured results are close to simulated results as formerly supposed to be. Due to the measured results, the LNA gives up to 14 dB power gain in the frequency range of 5.1 - 5.4 GHz which is generally enough for typical heterodyne receivers. The input and the output matching circuits works properly at the interested frequencies. The challenging part of this work is the noise figure of the LNA but the measured results are not performed yet. Because it is suppose to be the minimum noise figure of the circuit could occur at the interested frequencies and it should be below 3 dB. 1-dB compression point of LNA is nearly -13 dBm which is input referred. The power consumption of the LNA is also the challenging one and has a value of 10.6 mW.

In parallel to LNA design, RFMEM inductor design and fabrication are also accomplished. The desired value of inductor are targeted and fabricated. As the inductor fabrication steps are not so complicated, the suspended type inductor fabrication has a lot of problems which are given in Chapter 4. After the effort on optimizing the devices and chemicals, the suspended and Above-IC type inductors are fabricated. Other difficult part is the measurement of this inductors. As the values of the indutors are below 2 nH, calibrating the measurement results and canceling the parasitic effects are so important and not easy to performed. There are lots of measurements are performed on fabricated inductors however, still the stability can not be achieved but very close to end. Furthermore, not only the measurement devices, but also the test structures are important for measuring inductors which should have the open and short circuits to de-embedding the unwanted path parasitics.

The future work of this thesis can be defined as measuring the noise figure of the LNA. Also, two-tone test measurements should be done for finding the IIP3 point of LNA. On the other hand, measurements of fabricated inductors will be done. After measuring the inductors and finding the desired value of inductor, the integration of the RFMEM inductor to LNA test chip will be performed via bond-wire technique. Finally, the comparison of the simple LNA and inductor integrated LNA will give the amount of performance improvement on noise figure of the circuit which will make it possible to high performance single chip transceivers.

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