Realization of Micromachined-Electromechanical Devices for Wireless Communication Applications

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Realization of Micromachined-Electromechanical Devices for Wireless Communication Applications

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Abstract

As the communication technology evolves day by day, the demands for low cost, low power, multifunctional and higher-speed data communication circuits are increasing enormously. All these essential requirements enforce significant challenges on the current technology and illustrate the need for new designs and advanced architectures. The challenges of reconfigurability, spectrum efficiency, security, miniaturization and cost minimization can only be met by ensuring that the transceiver/receiver is comprised of low-energy, low-cost, adaptive and high performance RF devices.

With the potential to enable wide operational bandwidths, eliminate off-chip passive components, make interconnect losses negligible, and produce almost ideal switches and resonators in the context of a planar fabrication process compatible with existing IC processes, micromachining and Micro-Electro-Mechanical Systems (MEMS) has emerged to overcome the aforementioned problems of communication circuits. Up to date RF MEMS technology prove that on-chip switches with zero standby power consumption, low switching power and low actuation voltage; high quality inductors, capacitors and varactors; highly stable (quartz-like) oscillators and high performance filters operating in the tens of MHz to several GHz frequency range can be realized. The availability of such RF and microwave components will provide designers with the elements they have long hoped for to create novel and simple, but powerful, reconfigurable systems.

In this thesis, realization of RF MEMS components such as capacitive switches, parallel plate variable capacitors, micromachined inductors and resonators for wireless communication applications are presented. The design and fabrication of each component are given in detail. The performance improvement of some blocks by integrating RF MEMS devices is demonstrated. Also the fabrication process problems limiting the performance parameters of RF MEMS components are addressed.

Özet

Komünikasyon teknolojisi günden güne ilerledikçe, düşük maliyetli, düşük güç tüketen, çok fonksiyonlu ve yüksek hızlı bilgi transferi sağlayan komünikasyon sistemlerine olan ihtiyaç oldukça fazla artmaktadır. Bütün bu temel gereksinimler, şu anki teknolojiye önemli zorluklar doğurmakta, yeni tasarımlar ve gelişmiş mimarilere olan ihtiyacı ortaya çıkarmaktadır. Yeniden yapılandırılabilme, spektrum verimliliği, güvenlik, küçülme ve maliyet düşürme gibi zorluklar ancak düşük enerjili, ucuz, uyumlu ve yüksek performanslı RF (yüksek frekans) aygıtlarından oluşan alıcı/verici devreleri tarafından karşılanabilir.

Büyük bant genişliği sağlaması, kırmık dışı pasif elemanları ortadan kaldırması, ara bağlantı kayıplarını yok denecek kadar düşürmesi ve varolan IC (tümdevre) prosesi ile uyumlu düzlemsel fabrikasyon metotlarıyla ideale çok yakın anahtar yapıları ve rezonans devrelerine imkan kılma potansiyeli ile mikroişleme ve Mikro-Elektro-Mekanik Sistemler (MEMS), daha önce sözü geçen problemlerin üstesinden gelmek için kullanılmaya başlandı. Bugüne kadar RF MEMS teknolojisi, çok düşük güç tüketimli kırmık üstü anahtar yapılarının, yüksek kalite faktörüne sahip endüktörlerin, kapasitörlerin ve varaktörlerin , yüksek derecede kararlı osilatörlerin ve yüksek performanslı filtrelerin gerçeklenebileceğini kanıtlamıştır. Bu tür RF ve mikrodalga yapılarının gerçeklenebiliyor olması, tasarımcılara uzun süredir umdukları özgün, basit fakat güçlü ,yeniden yapılandırılabilir sistemleri yaratabilmelerini sağlamaktadır.

Bu tezde, kablosuz iletişim uygulamaları için, kapasitif anahtar yapılar, paralel plaka değişken kapasitörler, mikroişlenmiş endüktörler ve rezonatörler gibi RF MEMS yapılarının gerçeklenmesi verilmektedir. Her yapının tasarım ve fabrikasyon süreci ayrıntılı bir şekilde işlenmektedir. Buna ek olarak bazı alıcı/verici bloklarının RF MEMS yapılarının entegre edilme sonucundaki performans gelişimi de gösterilmektedir. Ayrıca RF MEMS yapılarının performanslarını kısıtlayan bazı fabrikasyon problemleri de tartışılmaktadır.

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1

Chapter 1
Introduction

1.1 Motivation

As the communication technology evolves day by day, the demands for low cost, low power, multifunctional and higher-speed data communication circuits are increasing enormously. All these essential requirements enforce significant challenges on the current technology and illustrate the need for new designs and advanced architectures. The challenges of reconfigurability, spectrum efficiency, security, miniaturization and cost minimization can only be met by ensuring that the transceiver/receiver is comprised of low-energy, low-cost, adaptive and high performance RF devices. Additionally these devices need to be developed for microwave up to sub-millimeter-wave frequencies, since the next generation of the communication networks will be specifically designed in these bands, due to their significant advantages in bandwidth and miniaturization.

The existing technology enables the design and fabrication of all the basic transceiver components (Low-noise amplifiers, oscillators, mixers, power amplifiers, filters, antennas, switches and so on) on planar substrates. Most of these components are built on the mature well-known semiconductor technology based on diodes and transistors. In addition to this, some components such as crystal and SAW resonators that are used for frequency selection because of their high quality factor (Q), discrete inductors and variable capacitors that are used to properly tune and couple the front end sense and power amplifiers and to implement

widely tunable voltage-controlled oscillators (VCOs) are off-chip components and must interface with integrated electronics at the board level. These off-chip devices present an important bottleneck against the ultimate miniaturization and portability of wireless transceivers.

With the potential to enable wide operational bandwidths, eliminate off-chip passive components, make interconnect losses negligible, and produce almost ideal switches and resonators in the context of a planar fabrication process compatible with existing IC processes, micromachining and Micro-Electro-Mechanical Systems (MEMS) has emerged to overcome the aforementioned problems of communication circuits. Up to date RF MEMS technology prove that on-chip switches with zero standby power consumption, low switching power and low actuation voltage; high quality inductors, capacitors and varactors; highly stable (quartz-like) oscillators and high performance filters operating in the tens of MHz to several GHz frequency range can be realized. The availability of such RF and microwave components will provide designers with the elements they have long hoped for to create novel and simple, but powerful, reconfigurable systems.

In this thesis, realization of RF MEMS components such as capacitive switches, parallel plate variable capacitors, micromachined inductors and resonators for wireless communication applications are presented. The design and fabrication of each component are given in detail. The organization of the thesis will be explained in next subsection.

1.2 Organization of Thesis

In chapter 2 general information about switches that are being used in blocks of transceivers and receivers are presented. Types of switches are explained and advantages of RF MEMS switches over other type of switches are listed. Also the performance parameters in evaluating a switch are given in detail. Additionally, literature survey has been made about RF MEMS switches and a detailed RF MEMS library is formed which can be used to compare and evaluate any designed switch with state of the art designs. Moreover, important steps in designing RF MEMS switches are given in detail with various formulas and sketches. Two RF MEMS capacitive switch designs, for a MPW process and to fabricate in our Cleanroom, are presented and their design steps and fabrication steps are given in detail.

In chapter 3 RF MEMS based varactors are studied. Types of the art MEMS varactors are given. Also selected publications are examined and a MEMS varactor library is formed. A dual gap parallel plate varactor structure with a tuning range of 350% is designed. Design steps and hand calculations are given in detail. The fabrication steps and problems are given in detail.

Chapter 4 gives the basics of High Q MEMS Inductors and also defines the recently adopted Above-IC process technology.. The important steps in the inductor design are given and also detailed information about the designed inductors given. Large range of inductors, inductance values form 1.1 to 6.5 and quality factors about 20-40 are being designed and simulated. These inductors are aimed to be integrated in to RF Blocks to improve their performance parameters. An LNA example is given in which an high Q inductor (Q=30) in the input matching stage improves the noise figure from 2.8dB to 1.8dB. Also, Above IC process is studied and some test structures are created which is a first step in the way of post processing. Additionally fabrication steps of a suspending MEMS inductor is given in detail. Inductor designs, simulations, above-IC concept and LNA integration part is contributed by Mehmet Kaynak .

In Chapter 5 general information about MEMS resonators are given. Various MEMS resonators are described and library formation is formed. Free-free beams are described and their design process is presented in detail. Various free-free beam resonator designs which are operating in 1st, 2nd and 3rd modes and have 200 MHz resonant frequencies are designed, simulated and compared. Also a resonator targeting 500 MHz operating frequency is designed and simulated.

Chapter 6 discusses the performance parameters of the aforementioned designs and presents the problems. Also discusses the future works for each design.

2

Chapter 2
MEM Switches

2.1 Introduction

A sample heterodyne RF transceiver front-end is shown in Figure 2-1 (a). In this architecture, the received RF signals are first passed through a bandpass filter, and then switched to a low-noise amplifier (LNA). Due to its gain, the LNA essentially sets the signal-to-noise ratio for the receiver chain. The amplified signals are filtered for improved image-rejection and down-converted to an intermediate frequency (IF) with a mixer. The signals at IF are then filtered for channel-selection and shifted in frequency to baseband by a second mixer.

The transmission process is complementary to the reception process. During transmission, the signals at baseband are upconverted to the RF carrier using an IF stage. A power amplifier (PA) is used to drive the antenna. A transmit-receive (T/R) switch is used to connect/disconnect the antenna for transmit and receive processes.

The direct downconversion or homodyne architectures mix the incoming RF signals with the carrier frequency to generate signals directly at baseband as shown in Figure 2-1 (b). Similarly, the signals are directly upconverted to the RF carrier using only one mixing step during transmission. The IC-design industry is increasingly looking at direct downconversion architectures to facilitate further integration by reducing the number of components required.

As indicated previously in Figure 2-1, several key blocks still cannot be integrated. Amongst these blocks, the T/R switch stands out as a candidate for on-chip integration because the MOSFET device is optimized to operate as a switch. Despite the improved switching performance of the MOSFET due to scaling, the performance of integrated CMOS T/R

switches falls significantly short of the transceiver requirements. In general - to date - performance of MOSFETs as a RF switches is found to be unsatisfactory.

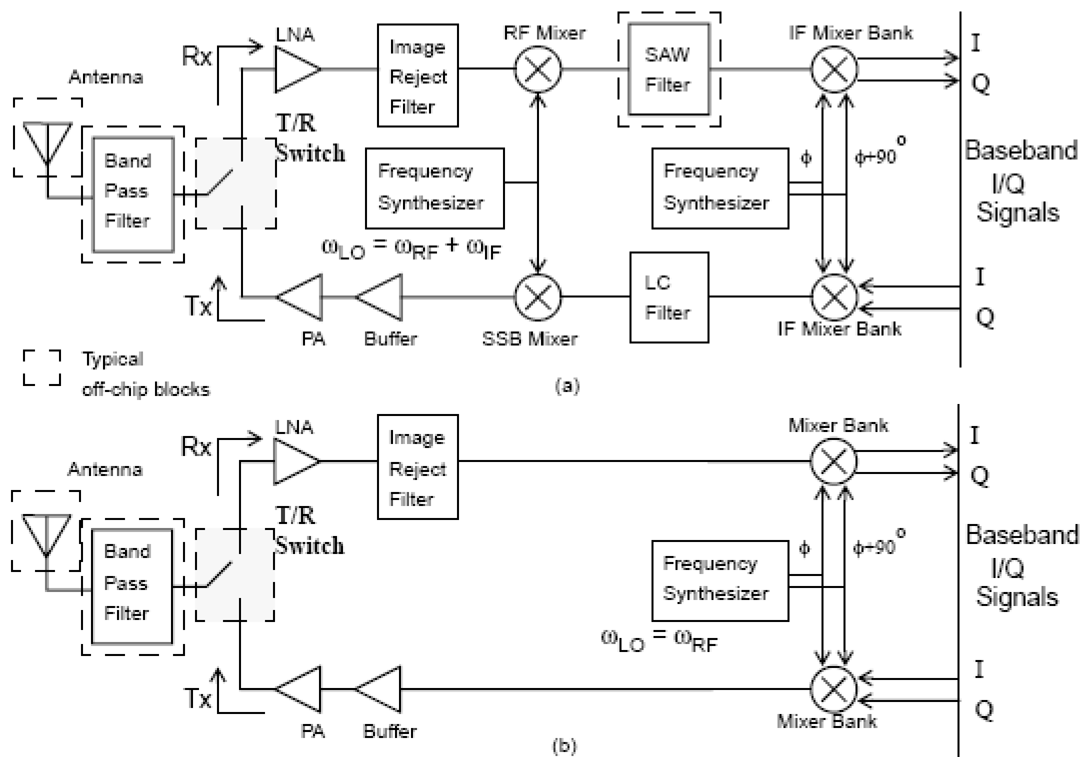

Figure 2-1: Simple RF transceiver architectures (a) Heterodyne or IF based and (b) Homodyne or direct downconversion [1]

RF switches can be used in several places in RF front-ends. In a T/R switch, a two-pole single-throw arrangement of switches multiplexes the use of the antenna between the PA and the LNA. T/R switches must have a high linearity to ensure that the high power signals (~2 W) at the output of the PA are transmitted to the antenna with minimum distortion. This linearity requirement presents a serious challenge in integrating T/R switches into on-chip designs especially as the supply voltage in standard CMOS continues to decrease.

In addition to the T/R switch application mentioned above, RF switches could be used to select capacitors, e.g., tuning of a voltage-controlled oscillator (VCO), tuning of matching circuits in power amplifier (PA) or low noise amplifier (LNA). In these applications, the challenge is to obtain a low on-resistance and a low off-state capacitance. A similar problem is encountered while switching inductors in and out of operation. The on-resistance must be low enough that the quality of inductor, when switched in, is not significantly degraded by the presence of a series resistance element. At the same time, the off-state capacitance must be low enough to ensure that the series resonance with the inductor, when it is switched out, does

not affect the performance of the rest of the circuit. In a given technology, the on-resistance and off-state capacitance are inversely related to each other. Since the resistance-capacitance product in a modern CMOS technology is not as low as desired, a T/R switch designed using a MOSFET as a switching element results in inferior performance.

2.2 Switch Performance Parameters

Ideally, switches are components that turn RF power on or off, or perform high-frequency signal routing [2]. It is mostly desirable for a switch to be noninvasive with respect to circuit/system performance. The degree of noninvasiveness exhibited by a switch is given by its electrical parameters that are given below [3].

2.2.1 Insertion Loss

The insertion loss of an RF switch refers to the RF loss dissipated in the device, typically characterized by S_{21} between the input and output of the switch in its pass-through state, which is the closed state for a series switch. The main contributing factors include resistive loss due to the finite resistance of the signal lines and contact at low to medium frequencies, and loss due to the skin depth effect at high frequencies.

2.2.2 Return Loss

The return loss of an RF switch refers to the RF loss reflected back by the device, typically characterized by S_{11} at the input of the switch in its pass-through state. The main contributing factors include the mismatch of the switch's total characteristic impedance

2.2.3 Isolation

The isolation of an RF switch refers to the RF isolation between the input and output, typically characterized by S_{21} of the switch in its blocking state, which is the open state for a series switch. The main contributing factors include capacitive coupling and surface leakage.

2.2.4 RF Power Handling

This is a measure of how much and, in some respects, how well a switch passes the RF signal. To quantify RF power handling, the 1-dB compression point is commonly specified. That point is a measure of the deviation from the linearity of the 1-dB output power with respect to

the input power. Alternatively, in pulsed-power operation conditions, the peak pulsed power, the repetition rate, and the duty cycle are specified. In switches containing PN-junctions power handling is a function of frequency [4].

2.2.5 Linearity

If a ratio of a switch's output power to input power (which can be defined as gain) is a function of the input power level, then the switch is said to behave as a nonlinear device [4]. When signals of different frequencies are simultaneously passed through the switch, then in addition to the input frequencies, the switch's output will also contain frequencies related to the sum and difference of the harmonics of the input frequencies. The extrapolation of the distortion power to the power level of the drive signals, assuming the switch has no compression of the signals, is defined as input and output third order intercept point, denoted IIP3 and OIP3 [4].

2.2.6 Transition Time and Switching Speed

Transition time is basically the time required for RF voltage envelope to go from 10% to 90% for on-time, or 90% to 10% for off-time, as shown in Figure 2-2. At the 90% point, the signal is within 1 dB of its final value.

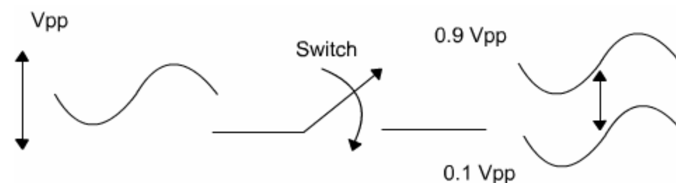

Figure 2-2: Transition time

Switching speed is the time required for the switch to respond at the output when the control line input voltage changes. Switching speed includes drive propagation delay as well as transition time and is measured from the 50% point on control voltage to 90% (for the on-time) or 10%(for the off-time) of the RF voltage envelope, shown in Figure 2-3. Therefore, by definition, switching time will be always longer than transition time.

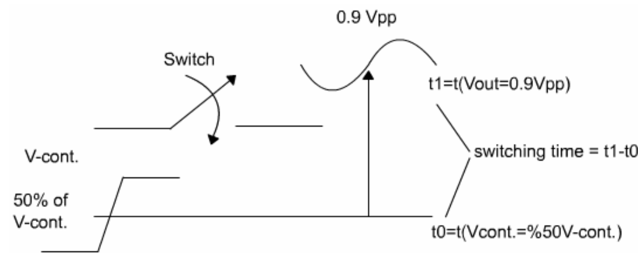

Figure 2-3: Switching speed

2.2.7 Operational Lifetime

This is the number of cycles the switch is able to operate with both dc bias voltage and RF power applied. A cycle is usually specified by a waveform that includes a dead time, the time period during which the switch is transitioning between OFF and ON states, or resting. The dead time is usually required to not exceed 5% to 10% of the cycle [4].

2.2.8 Power Consumption and Actuation Voltage

This is the power it takes to set the switch in a given state. Static power dissipation must be kept as low as practical. Power consumption of less than 1 mW is desirable. Actuation voltage is the voltage necessary to effect switching. This is especially important in RF MEM switches.

2.2.9 Operating Environment

Operating environment specifies the temperature range, the humidity level, and the radiation level the switch must withstand while operating and continuing to meet specs.

2.2.10 Cold and Hot Switching

These refer to whether a switching occurs in the absence/presence of signal power respectively.

2.3 Types and Comparison of RF Switches

2.3.1 MESFET

MESFETs are majority carrier devices which makes them suitable for high speed operation and they can be implemented using silicon, GaAs, InP, and as heterostructures [5]. However,

silicon based MESFET are incapable of handling large powers and typically are slower than those implemented using the other materials. For high-power (> 1 W) and high-frequency (> 1GHz) applications, MESFETs implemented using GaAs are commonly used for the reason that GaAs has a large bandgap, and hence a large breakdown voltage that allows high-voltage operation with no reliability concerns. Moreover, the high low-field mobility of GaAs enhances the usable bandwidth of the device. GaAs MESFETs also use a semi-insulating substrate which further lowers loss in the device.

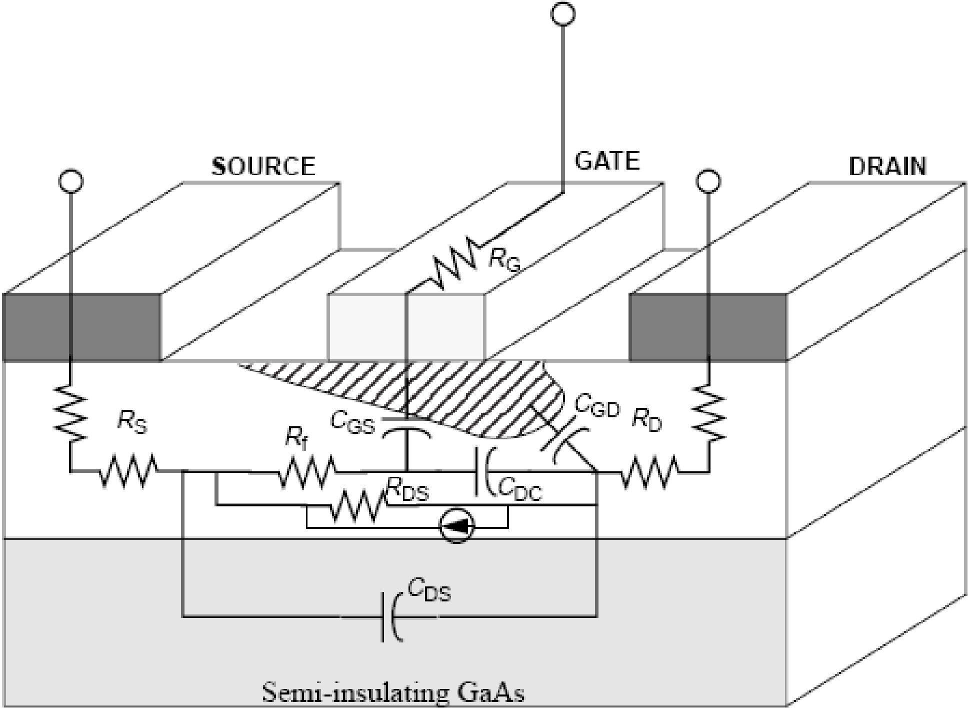

Figure 2-4: Simplified GaAs MESFET cross-section and physical origin of main RF equivalent circuit elements [5]

For the design of a GaAs MESFET, the main trade-off is between its on-resistance and off-state capacitance. In order to achieve a low insertion loss, a large device with a low on-resistance can be used. This degrades the isolation performance since the off-state capacitance, C_{DS} in Figure 2-4, will be large. Another limitation of GaAs MESFET switches is their power handling capability, as compared to PIN diodes, when low control voltages are used. An important thing to note is that GaAs FET switches, unlike PIN diodes, do not consume static power, which makes them attractive for low-power hand-held wireless communication devices. An important limitation is that they cannot be integrated with silicon-based transceivers.

2.3.2 PIN Diodes

Diodes are widely available in CMOS technologies and also as discrete components. PN-junction diodes found in standard CMOS, however, have a low breakdown voltage of about 10 V and are unsuitable for controlling large signal swings. As a result, discrete PIN diodes have been used for high-power RF switches. In the on-state, the diode is biased using a large current of about 10 mA which ensures that the ac resistance is low. In the off-state, the PIN structure has a low junction capacitance which ensures large isolation. PIN diodes can be fabricated in silicon, GaAs, or even using heterostructures. While PIN diodes show excellent insertion loss (< 1dB) and power handling (> 5 W) up to very high frequencies, their static power consumption due to the bias current remains a severe limitation [5]. Since a large bias current is typically required for switch operation, it must be supplied through a choke. Since integrating chokes on silicon is technologically challenging, monolithic-microwave-integrated-circuits (MMICs) with integrated chokes using PIN diode switches are rarely found. Due to limitations of static power consumption and the absence of MMIC diode switches - despite superior performance - diode switches are being gradually replaced by GaAs MESFET MMICs, which offer only slightly worse performance for significantly lower static power consumption.

2.3.3 MOSFET

The MOSFET is one of the cheapest of aforementioned switch options. It is available in a CMOS process and its performance improves every generation. Only silicon-based MOSFETs, however, are viable due to the absence of a good gate insulator for other materials. The on-resistance of silicon MOSFET is significantly worse than a GaAs MESFET due to poor electron and hole channel-mobilities at low electric fields. Modern technology offers very small channel length MOSFETs with a good $R_{on}xC_{off}$ product. The thin gate dielectric and small channel length, however, permit a low-voltage operation only. These switches cannot be used for high-power RF applications. The typical performance of MOSFET switch at RF is poor compared to its GaAs and PIN diode counterparts.

Figure 2-5 shows the small-signal equivalent circuit of the MOSFET for RF applications. The channel resistances, RC1 and RC2, and the substrate resistances, RB1, RB2, and RB3, are the main sources of loss in the MOSFET. The substrate resistance, RB3, may be reduced by grounding the substrate as close to the device as possible. The low quality factor of the source

and drain parasitic junction capacitors, CSB and CDB, (Q ~ 10-20 @5 GHz) can also lead to significant losses, especially as the frequency of operation increases. The linearity of the MOSFET switch is limited for large signal swings due to conductivity modulation caused by a changing gate-source (Vgs) and drain-source (Vds) voltage for a large-signal input. Another cause of non-linearity is the parasitic source and drain junction diodes which can clip the signal at about 0.7 V above the power supply or 0.7 V below ground [5].

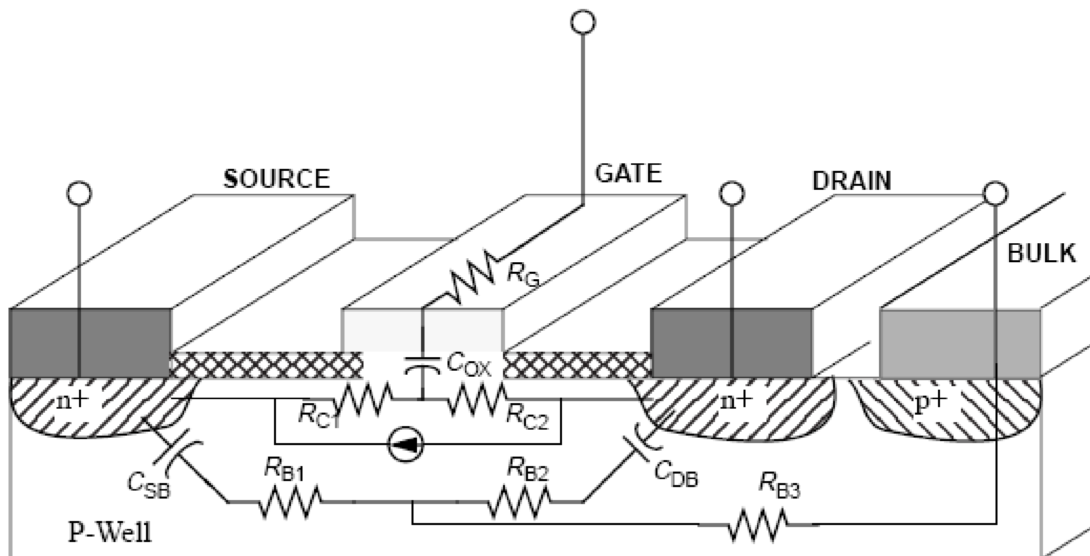

Figure 2-5: Simplified MOSFET cross-section and physical origin of main RF small-signal equivalent circuit elements [5].

2.3.4 MEMS Switches

MEMS switches are surface-micromachined devices which use a mechanical movement to achieve a short circuit or an open circuit in the RF transmission-line. More generally, the physical mechanical movement of an RF MEMS switch controls the impedance of an RF transmission line. Specifically RF MEMS switches designed to operate in milimeterwave (0.1 to 100 GHZ) or microwave frequencies.

RF MEMS switches has a remarkable advantage over the traditional RF switches with their extremely broadband operation, very high isolation, extremely low insertion loss, low power consumption, simple biasing networks and low intermodulation products. However they suffer several disadvantages like slow switching speed in the orders of us, high actuation voltage requirement and hot switching in high power applications. Packaging is the other major problem with the RF MEMS switches. They need to be packaged in inert atmosphere

(Nitrogen, Argon, etc...) and in very low humidity which results in hermetic or near hermetic seals. The cost of hermetic packaging are currently very high, the packaging process techniques adversely affect the reliability of the MEMS switch [6].

RF MEMS switches can be divided in three general configurations;

- Mechanical Structure: Cantilever, air-bridged and diaphragm
- FR circuit configuration: series and shunt
- Form of contact: resistive and capacitive.

The cantilever switch, as seen in the Figure 2-6 (a) consist of a thin strip of metal or dielectric with one end is fixed to substrate or signal line and the other end is suspended over an electrode, which is used for electrostatic actuation of the membrane, and an RF transmission line with an air gap. Air bridge switch is a metal/dielectric strip that is fixed at the both ends and suspended over the electrode and an RF transmission line with an air gap in the middle as seen in Figure 2-6 (b).

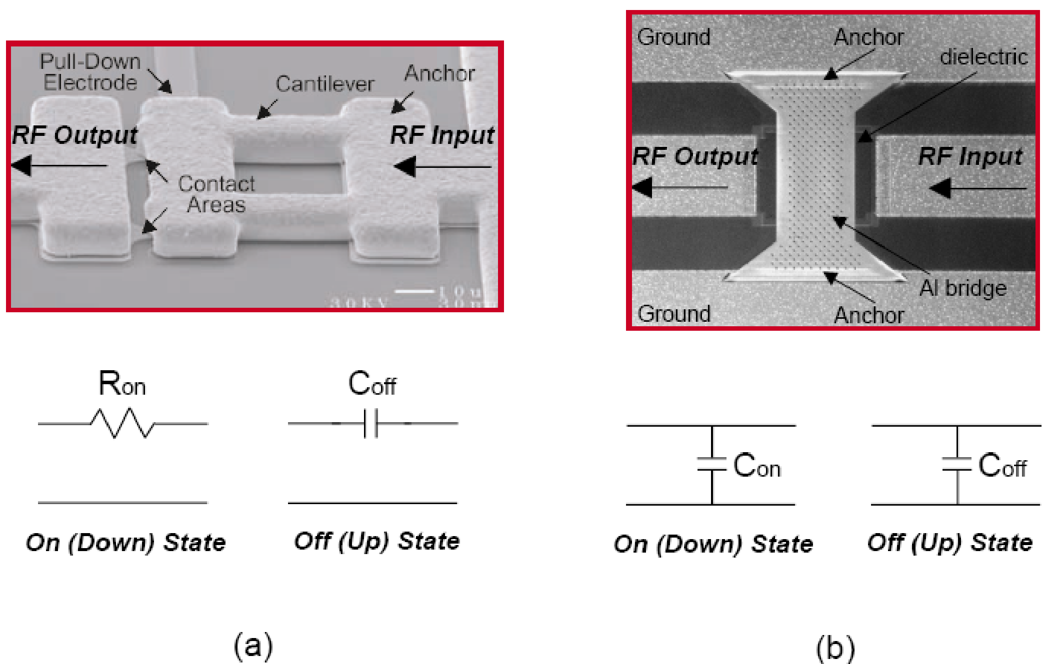

Figure 2-6: Common RF MEMS structures a) Series switch developed by Analog Devices/Northeastern University and a simple equivalent circuit [7]. b) Shunt switch developed by Raytheon and simple equivalent circuit [8].

The series MEMS switches is excellent for DC to +0 GHz application with a typical isolation of %0 dB at 1GHz and 30 dB at 10 GHz, while shunt design lead to 35-40dB isolation at 30-40 GHz. Typically capacitive switches have been used in shunt configuration and DC contact switches are placed in series. The reason is that it is easier to get a good isolation with a limited impedance ratio (such as the capacitive switch) in a shunt configuration than in a series configuration [9]. Both cantilever and air bridged types can be configured in series or shunt. Contact can be either capacitive (metal-insulator-metal) or resistive (metal-to-metal), capacitive contact is characterized by the capacitance ratio between the up-state (open circuit) and the down state (short circuit) positions and typical values are 80-160 depending on the design. On the other hand metal-to metal DC contact switches can operate from 0.01 to 40 GHz, with the up-state open position capacitance of 1-5 fF, in the short circuit position DC contact becomes a series resistor with 0.5 to 2 ohm value [10].

2.3.5 Comparison of RF Switches

MEMS switches show remarkable advantages over their solid state counterparts (PIN diodes or FET transistors) that make them very attractive for many applications [11]. Table 1.1 presents the performance parameter comparison of the RF MEMS, PIN diode and FET transistor switches [12]. The first obvious advantage of RF MEMS is that they have nearly zero power consumption. Although their electrostatic actuation requires higher voltages than solid state switches, which is in the range of 10-80V, as seen in the Table 2-1, they do not consume any current that leads to very low power dissipation values which is in the order of μW as compared to mW for diodes. Another significant advantage of MEMS switches over solid state counterparts is their very high isolation. As a consequence of RF MEMS being fabricated with air gaps, they have very low off-state capacitances (2-4 fF) resulting in excellent isolation at 0.1-60GHz. Also, capacitive switches with a capacitance ratio of 60-160 provide excellent isolation from 8-100GHz. Moreover; they are characterized by very small series ohmic resistance, on the order of 0.5 to 2Ω. Their on-state insertion loss is rarely above 0.3 dB which is very low comparing to PIN diodes and FETs whose insertion losses are in the range of 0.4 – 2.5. Furthermore, they are much more linear than solid state devices, since they are completely passive components with no semiconductor junctions. This improves the intermodulation distortion by approximately 30 dB. Since no other technology has been able to match this RF performance, the RF MEMS potential is very promising in a number of

commercial (tunable filters, phase shifters, wireless telecommunications switches) and defense (phased arrays, high-performance matching networks) applications.

Table 2-1: Comparison of the performance parameters of FETs, PIN Diodes and RF MEMS switches [12].

Parameter	RF MEMS	PIN	FET
Voltage (V)	10-80[a]	± 3-5	3-5
Current (mA)	0	3-20	0
Power Consumption[b] (mW)	0.05-0.1	5-100	0.05-0.1
Switching Time	1-300 μsec	1-100 nsec	1-100 nsec
C_{up} (series) (fF)	1-6	40-80	70-140
R_s (series) (Ω)	0.5-2	2-4	4-6
Capacitance ratio[c]	40-500[d]	10	N/A
Cutoff frequency[e]	20-80	1-4	0.5-2
Isolation (1-10 GHz)	Very High	High	Medium
Isolation (10-40 GHz)	Very High	Medium	Low
Isolation (60-100 GHz)	High	Medium	None
Loss (1-100GHz) (dB)	0.05-0.3	0.3-1.2	0.4-2.5
Power Handling (W)	<1	<10	<10
Third-order intercept point (dBm)	+66-80	+27-45	+27-45

[a] Actuation voltages as low as 5V are reported
[b] Includes voltage upconverter of drive circuitry
[c] Capacitive switch only
[d] A ratio of 500 is achieved only with very smooth and high-ε_r dielectrics
[e] The cutoff frequency f_c is defined as the frequency where the ratio of the off (up state) capacitance and on (down-state) resistance degrades to unity $f_c = 1/(2\Pi C_{up} R_s)$

On the other hand, RF MEMS switches are three orders of magnitude slower than PIN diodes due to inertia. As a result, their switching speed is typically in the order of 1-300 μsec which cannot be suitable for some certain communication and radar applications. In addition, special consideration is needed for high power operation. If the RF power is sufficiently high, self actuation of the switch may occur, due to the associated rectified voltage. Power handling of MEMS switches is relatively low comparing to FET and PIN switches which can handle up to 10mW power. Moreover, MEMS are very sensitive to important environmental factors (humidity, dust, etc.) Consequently, their RF performance, as well as their reliability, can be seriously degraded in a dirty environment. Packaging, therefore, is essential and it remains an open research area at this day. Additionally reliability of mature MEMS switches is 0.1-40 Billion cycles. However, many systems require switches with 20-200 Billion cycles. Also, the

long term reliability (years) has not yet been addressed. It is now well known that the capacitive switches are limited by the dielectric charging which occurs in the actuation electrode, while the metal-contact switches are limited by the interface problems between the contact metals, which could be severe under low contact forces (in electrostatic designs, the contact forces are around 40-100 µN per contact). It is important to note that the reliability and packaging issues have been the limiting factors to the quick deployment of RF MEMS switches, and they are currently under intense investigations.

2.4 RF MEMS Switch Library Formation

2.4.1 RF MEMS Library Formation

Published studies from various companies, design groups and universities are examined and Table 2-2 is formed. Table 2-2 includes typical performance parameters of RF MEMS switches, such as; insertion loss, isolation, total on resistance, total off capacitance, actuation voltage, switching time and operating frequency. As clearly seen on Table 2-2 MEMS switches operate in a wide range of frequency from DC up to tens of GHz. Switches operating down to 50 MHz are reported ([13]) as well as switches operating up to 40 and 50 GHz ([14], [15], [13] …). Most listed MEMS switches perform insertion loss smaller than 0.5 dB and also insertion losses as low as 0.05 dB is reported [12]. Also MEMS switches demonstrate very high isolation which is desired for a good switch. Their isolation values ranges from 20 dB up to 70 dB. They have low on resistance values that are smaller than 2 Ω. Some designs show excellent on state resistance values of 0.08 Ω [12]. Actuation voltages of RF MEMS switches are generally a few tens of volts however some designs have very low actuation voltage values as 3-5 V [12], [16]. Switching speeds of RF MEMS switches are usually slower than solid state counterparts. Starting from a few microseconds, they can go up to 250 microseconds. which is probably not suitable for many communication applications. To sum up, this table includes the state of the art parameters for RF MEMS switches and may be beneficial to compare the performance of designed switches.

Table 2-2: Library formation of selected published MEMS switches

Name / Company	Insertion loss (dB)	Isolation (dB) at	Total on resistance (ohm)	Total off capacitance (pF)	Actuation Voltage (V)	Switch time (us)	Operation Freq
[17] Nanyang Technological University	0.4 dB <26.5 GHz	26 dB at 10 GHz, 27 dB at 26 GHz.	1.3	30	N/A	N/A	1-26.5 GHz
[13] Tsaur, Kazumaza	−0.5 dB (0.05–20GHz)	−30 to -65 dB (0.05 - 57GHz)	N/A	N/A	N/A	N/A	50 MHz – 57 GHz
[18] Park, Kim, Chung, Bu	0.08 dB at 10 GHz	42 dB at 5 GHz	N/A	50 (on/off ratio of 600)	8	N/A	5-10 GHz
[19] Rangra, Margesin, Lorenzelli	0.25 dB at 10 GHz.	35 dB at 10 GHz	N/A	N/A	8-10	N/A	8–14 GHz
[16] Radant MEMS Inc.	0.27 (4Ghz)	-29 (4GHz)	<1	N/A	40	5	4 GHz
[20] Rockwell SC	0.1 at 4GHz	-50	N/A	N/A	N/A	30	4GHz
[12] Rayhteon	0.07 (10-40 GHz)	-20 (10GHz) -35 (30GHz)	0.25-0.35	N/A	N/A	3	40 GHz
[12] Univ. of Michigan [1]	0.1 (1-40 GHz)	-25 (30GHz)	0.2 – 0.3	N/A	N/A	20	40 GHz
[12]Univ. of Michigan [2]	0.05 (30GHz)	-30 (30 GHz)	0.08-0.15	N/A	N/A	6	30 GHz
[21] CEA-LETI & ST	0.4 (6GHz)	-40 (6GHz)	2	N/A	N/A	250	6 GHz
[22] UIUC	<0.1 (40GHz)	-20 (40GHz)	N/A	N/A	15	22	40 GHz
[23] HRL	<0.25 40GHz	20dB at 40GHz	N/A	N/A	NA	NA	NA
[14] UIUC	0.5	-15 at 40GHz	0.3	N/A	NA	NA	40GHz
[15] ASU	0.18 at 30GHz	-50	2	N/A	9	60	40GHz
[24] Gatech	0.9 40GHz	-25dB	NA	N/A	15	NA	40GHz
[25] Pacheco and Kastehi	0.17 40GHz	-15.5 at 40GHz	NA	N/A	NA	NA	40GHz
[26] Li, Liu, Kim	0.18 30GHz	-30 at 30GHz	2	N/A	NA	60	30GHz

[1] Low-voltage capacitive MEMS shunt switch (Pacheco, Peroulis, Katehi (1997-2000)

[2] Low-height Ti/ Gold capacitive MEMS shunt switch (Rebeiz, Muldavin, Hayden, Tan)

2.5 Capacitive RF MEMS Switch Design Flow

2.5.1 Electromechanical Design

The mechanical design of most electrostatically based switches starts with considering the required DC actuation voltage. Equation (2-1) presents a widely cited formula (e.g. [12]) for calculating the pull-in voltage of fixed-fixed beams, or airbridges

$$V_P = \sqrt{\frac{8K_z g_o^{\ 3}}{27\varepsilon_o A}} \quad \textbf{(2-1)}$$

K_z is the equivalent spring constant of the moving structure in the direction of desired motion (typically z-direction), g_0 is the gap between the switch and the actuation electrode, ε_0 is the free space permittivity and A is the switch area where the electrostatic force is applied. Formula (2-1) implies that there are several ways that may decrease the required actuation voltage [27]. For instance, reducing g_0 can significantly lower the pull-in voltage. Although this solution can be partly applied to low-frequency applications (< 10 GHz), it will adversely affect the high-frequency off-state switch performance by compromising the switch isolation (for a series switch), or insertion loss (for a shunt switch). A second approach in lowering the pull-in voltage would be to increase the actuation area A. This area, however, has to stay within reasonable limits, primarily imposed by our desire for miniaturized circuits. The third alternative which offers the maximum design flexibility for a low to moderate actuation voltage is to lower the switch spring constant, hence designing a compliant switch.

2.5.1.1 Spring Design

If we want to apply MEMS switches to low voltage (<5-10) mobile communication applications, we definitely have to decrease the pull-in actuation voltage of them. As mentioned in the previous part, decreasing the gap of the suspended membrane, increasing the area of the membrane and lowering the switch spring constant, all, decreases the actuation voltage of the switch. However, decreasing the gap results in degraded isolation performance, and increasing the area of the switch is limited because of the compactness; consequently decreasing the spring constant by adapted mechanical design is the most effective and flexible way to decrease actuation voltage.

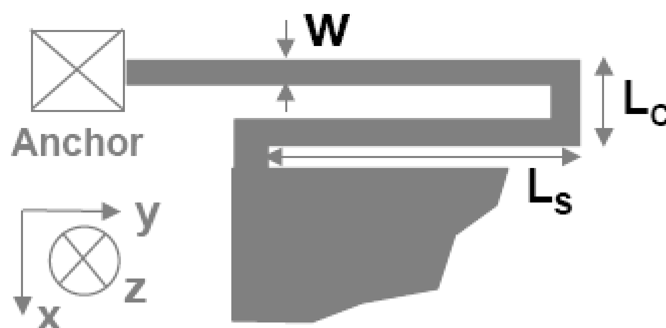

Figure 2-7: Folded suspension arm in order to decrease spring coefficient of the beam [28]

Figure 2-7 depicts a folded suspension beam which is used in order to decrease spring coefficient. We take advantage of folded suspension beams in order to decrease the spring coefficient of the beam in a small area. The formula 2-2 estimates the spring coefficient of a single folded suspension beam and we can see that for $L_S >> L_C$ the spring coefficient is independent of Poisson's ratio (*v*). In the formula 2-2 L_S is span beam length, L_C is connector beam length, w stands for width of the beam, t is the metal thickness of the beam, E is Young's modulus of the material and *v* stands for Poisson's ratio [28].

$$k_z = \frac{\left(\frac{Ew}{2}\right)\left(\frac{t}{L_C}\right)^3}{1+\frac{L_S}{L_C}\left[\left(\frac{L_S}{L_C}\right)^2 + 12\frac{1+v}{1+(w/t)^2}\right]}$$

(2-2)

$$for\ L_S >> L_C \rightarrow k_z = 2Ew\left(\frac{t}{L_S}\right)^3$$

$$k_x = 2Et\left(\frac{t}{L_C}\right)^3 \quad and \quad k_y = 2Et\left(\frac{t}{L_S}\right)^3$$

2.5.1.2 Material Considerations

The material parameters that determine the threshold voltage, the resonance frequency, and the maximum deflectable distance are the elastic modulus, the yield strength, and the dielectric constant. Table 2-3 lists these properties for different class of materials [4].

Table 2-3: Elastic Modulus, Yield Strengths, Dielectric Constants of Various Materials

Class	**Material**	**Elastic Modulus E(N/m²)**	**Yield Strength σy(N/m²)**	**Dielectric Constant εr**
Ceramics	Ta_2O_5	$6.0x10^{10}$	----	25
	SiO_2	$7.17x10^{10}$	$8.4x10^9$	3.94
	Si_3N_4	$1.3x10^{11}$	$1.4x10^{10}$	7
	Al_2O_3	$5.3x10^{11}$	$1.54\ x10^{10}$	10
Metals	Au	$6.13x10^{10}$	$3.24\ x10^8$	----
	Al	$7x10^{10}$	$1.7\ x10^8$	----
	Cr	$1.8x10^{11}$	$3.62\ x10^8$	----
	Ni	$2.07x10^{11}$	$5.9x10^8$	----
Semiconductor	Si	$1.90x10^{11}$	$7.0\ x10^9$	13.5
Diamond	C	$1.04x10^{12}$	$5.3\ x10^{10}$	5.68

The values of the mechanical and electrical properties of the materials depend heavily on microstructure, such as whether the material is single or polycristal (grain size and grain orientation), amorphous, as-deposited, or annealed.

Contact metallurgy plays also a crucial role in the engineering of MEMS switches, since their wear and tear drastically reduces switch lifetime. The key parameter characterizing the contacts is their resistance R_C, particularly in context of a contact force F_C [29]. Theoretical studies on contact physics [30] have established this relationship as;

$$R_C \approx F_C^{\ 3} \tag{2-3}$$

when the contact force results in pure elastic deformation. The studies also show that contact resistances that are lower than 50mΩ can be achieved by contact forces F_C lower than 1 mN for gold and gold alloys.

Selecting the appropriate material for the switch is a crucial step in the design flow. A case study presented in [28] clarifies the question of selecting metal or polysilicon as the switch material. One serpentine spring with dimensions L_S = 220µm, L_C = 18 µm, t=2 µm and w= 6µm is designed with materials gold (Au), aluminum (Al) and polysilicon.

Table 2-4: Parameters of the designed different type material serpentine springs [28]

Au	Al	Polysilicon
E_{AU}~80GPa	E_{AL}~70GPa	$E_{Si\text{-}Poly}$~170GPa
V_{Au}~0.22	V_{Al}~0.3	$V_{Si\text{-}poly}$~0.3
K_{zAu}=0.721N/m	K_{zAl}=0.631N/m	K_{zpoly}=1.533N/m
K_{xAu}=1.19x10^4 N/m	K_{xAl}=1.04x10^4 N/m	K_{xpoly}=2.52x10^4 N/m
K_{yAu}=6.49N/m	K_{yAl}=5.68N/m	K_{yzpoly}=13.79N/m
V_{PIAu}^*=4.4V/21.9V	V_{PIAl}^*=4.1V/20.6V	V_{PIpoly}^*=6.4V/32V

*Estimated V_{PI} (area=100x100/20x20 µm^2, 2 µm^2 gap)

As it can be seen in Table 2-4 metals presents lower spring coefficients and lower actuation pull-in voltages than polysilicon. Therefore it can be said that metal appears to be better choice for RF MEMS switches compared to polysilicon.

2.5.1.3 Switching State and Damping

MEMS switches dynamic behavior can be modeled using a simple one-dimensional (1-D) nonlinear model. This model treats the switch as a single lumped mass and applies classical Newtonian mechanics to predict its behavior under the applied electrostatic force. The following equation of motion if the basic formula for the 1-D model:

$$mz'' + bz' + K_z z = F_e \qquad \textbf{(2-4)}$$

Where m is the switch mass, b is the damping coefficient and Kz is the spring coefficient in the direction of motion. These coefficients are explained in formulas 2-5, 2-6, 2-7 .

$$F_e = \frac{\varepsilon_o A V^2}{2\left(g_o + \frac{t_d}{\varepsilon_r} - z\right)^2} \qquad \textbf{(2-5)}$$

$$b = \frac{K_z}{\omega_o Q} \qquad where \qquad \omega_o = \sqrt{\frac{K_z}{m}} \qquad \textbf{(2-6)}$$

$$Q = Q_o\left(1 - \left(\frac{z}{g_o}\right)^2\right)^{3/2}\left(1 + 9.638\left(\frac{\lambda}{g_o - z}\right)^{1.159}\right) \qquad \textbf{(2-7)}$$

A is the switch actuation area, go is the initial gap, ε_r and t_d are the dielectric layer constant and thickness, respectively, V is the applied dc voltage Fe is the electrostatic force. Equation 2-7 calculates the switch quality factor and takes into account the damping dependence on the switch height. If this is ignored, the second term of the right-hand side should be replaced by one. Furthermore, the third term reduces the gas flow resistance underneath the switch because of the slip effect, where particles can have fewer interactions before escaping. The λ variable of this term is the called the mean free path and is approximately 0.1 µm at standard temperature pressure (STP). The damping coefficient, which is related to Q_o by 2-6, has been derived in 2-8 for a square plate with area

A as;

$$b = \frac{3}{2\pi}\frac{\mu A^2}{g_o^3} \qquad \textbf{(2-8)}$$

where µ is the air viscosity (at STP $\mu = 1.845 \times 10^{-5}$ Pa.s) [31].

2.5.2 Electromagnetic modeling

Figure 2-8 shows a lumped-element equivalent circuit for this structure that is accurate up to 80 GHz [32].

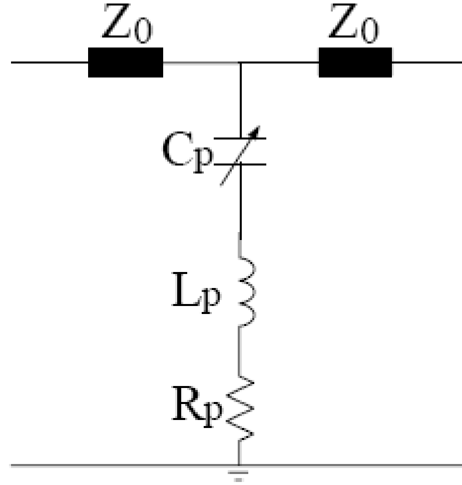

Figure 2-8: Lumped element equivalent model for capacitive switch

Up state and down state capacitance, C_{off} and C_{on} respectively can be applied to Cp in the lumped element model using the formulas 2-9 and 2-10

$$C_{off} = \frac{1}{\left(g_i/\varepsilon_D A\right) + \left(h_a/\varepsilon_o A\right)} \tag{2-9}$$

$$C_{on} = \frac{\varepsilon_D A}{g_i} \tag{2-10}$$

where g_i is the thickness of the dielectric layer, h_a is the air gap between the switch top electrode and the dielectric layer, ε_o and ε_D are the permittivity of air and relative permittivity of dielectric layer respectively, A is the area of the contact area of membrane.

The folded suspension arms, which we will call inductive connecting beams, play a crucial role in the RF performance of the switch, because they form the path the RF signal has to follow to reach the ground. Consequently, the shunt inductance L_p and resistance R_P primarily depends on the geometry of these beams. Example connecting beams and their resonant frequencies, inductances and resistances are given in Figure 2-9.

	Inductive Connecting Beam	Resonant Frequency [GHz]	Inductance [pH]	Resistance [Ω]
A	(1μm thick Au) 50μm, 8μm, 8μm, 180μm	16.3	87	1.95
B	60μm, 10μm, 10μm, 180μm	21.5	50	1.7
C	60μm, 100μm	27.3	31	1.1
D	60μm, 140μm	29.8	26	0.9
E	60μm, 10μm	43.8 (simulated)	12	0.6
F	60μm, 40μm	107.3 (simulated)	2	< 0.2

Figure 2-9: Inductive beams and their resulting resonant frequencies, inductances and resistances. (for C_D=1.1pF) [12]

2.6 Designed RF MEMS Capacitive Switch

Figure 2-10 shows a 3D view of our proposed switch in a coplanar waveguide (cpw) configuration. The switch consists of a movable metallic plate suspended over the cpw lines. This plate is connected to the substrate at four points (anchors) through four beams. Because of their shape, we will call these beams serpentine springs or folded-suspension beams. The switch is typically suspended 3 μm above the cpw line and is electrostatically actuated when a DC voltage is applied between the switch and the cpw ground planes.

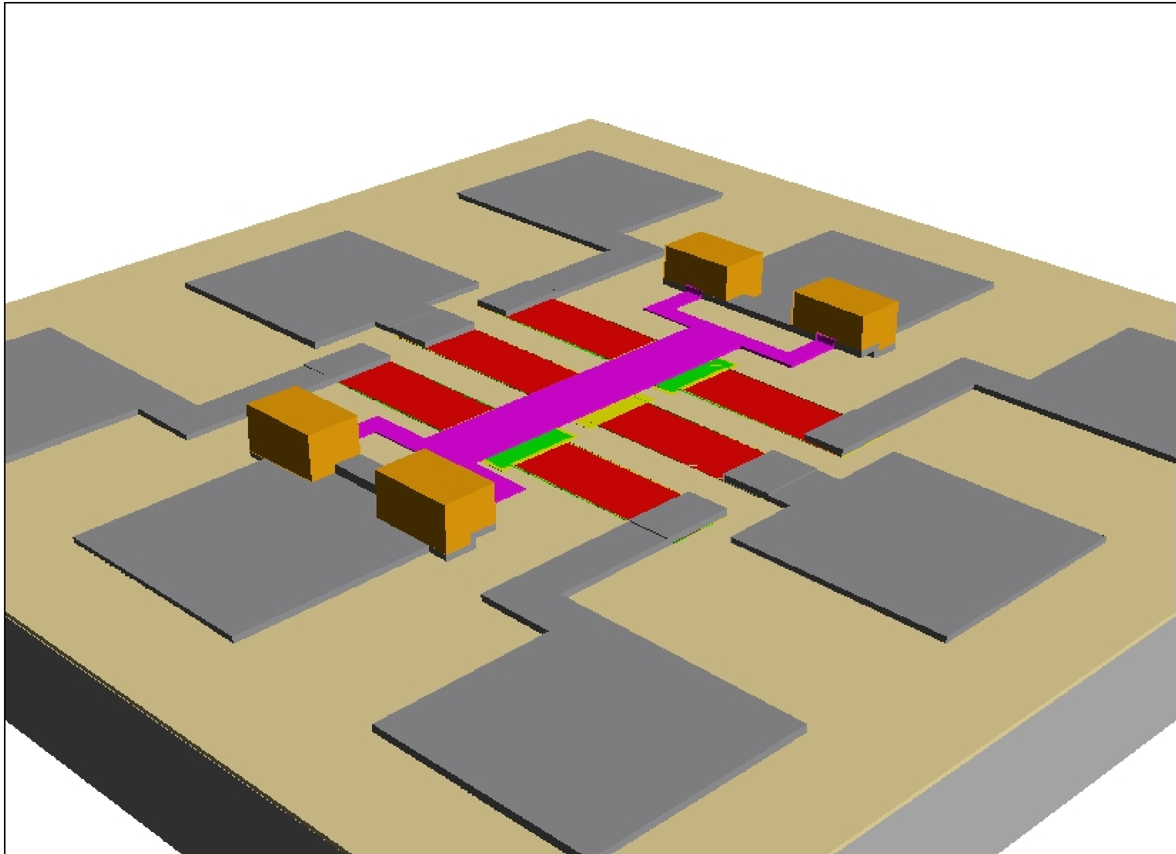

Figure 2-10: 3D view of the designed RF MEMS capacitive switch

When no DC bias is applied, the switch presents a very small shunt capacitance (typically in the order of a few fF) between the center conductor and the ground planes. This is called the up or off state and the RF signal can propagate with minimal loss (typically with 0.2dB up to 40 GHz). On the other hand, if the applied bias exceeds the actuation voltage, the switch collapses on the dielectric layer underneath it. The switch then presents a significant shunt capacitance, which is equivalent to an RF short-circuit. This is called the down or on state and virtually all the incident RF power is reflected back to the source.

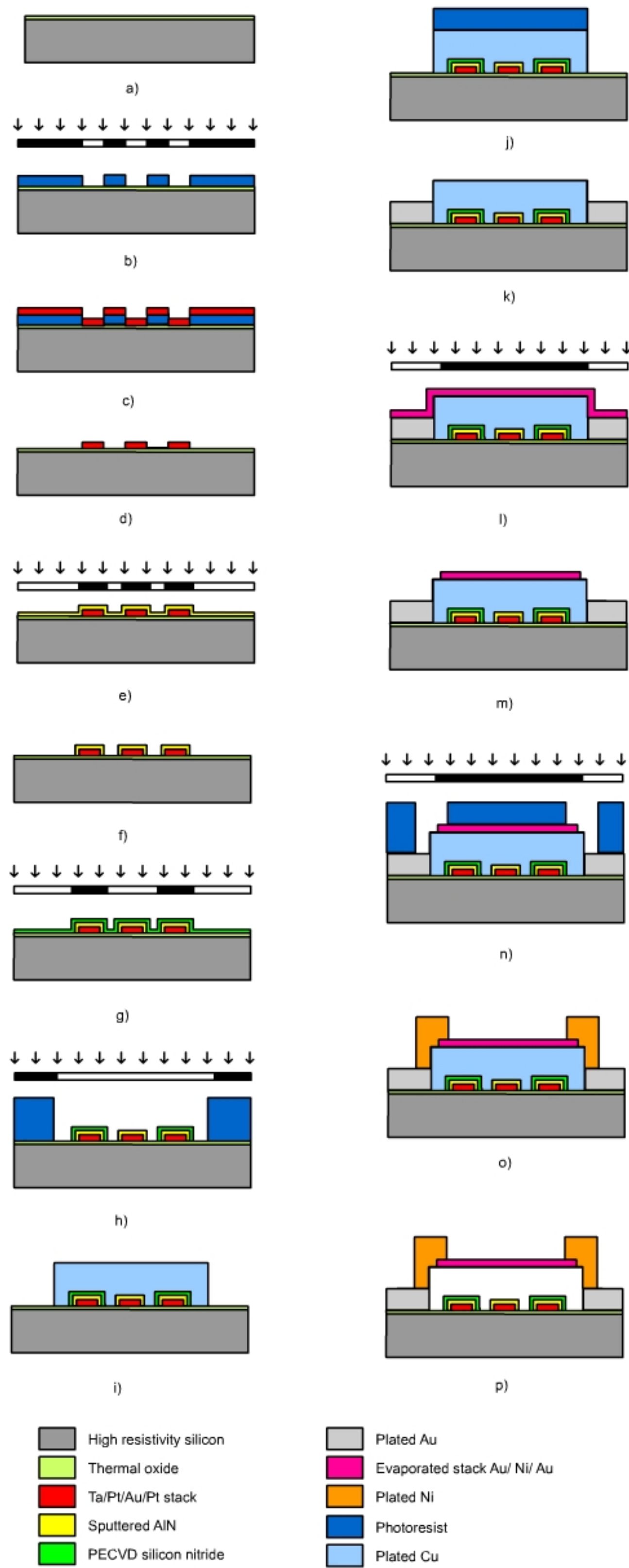

Figure 2-11: Process Flow of MEMS Switch

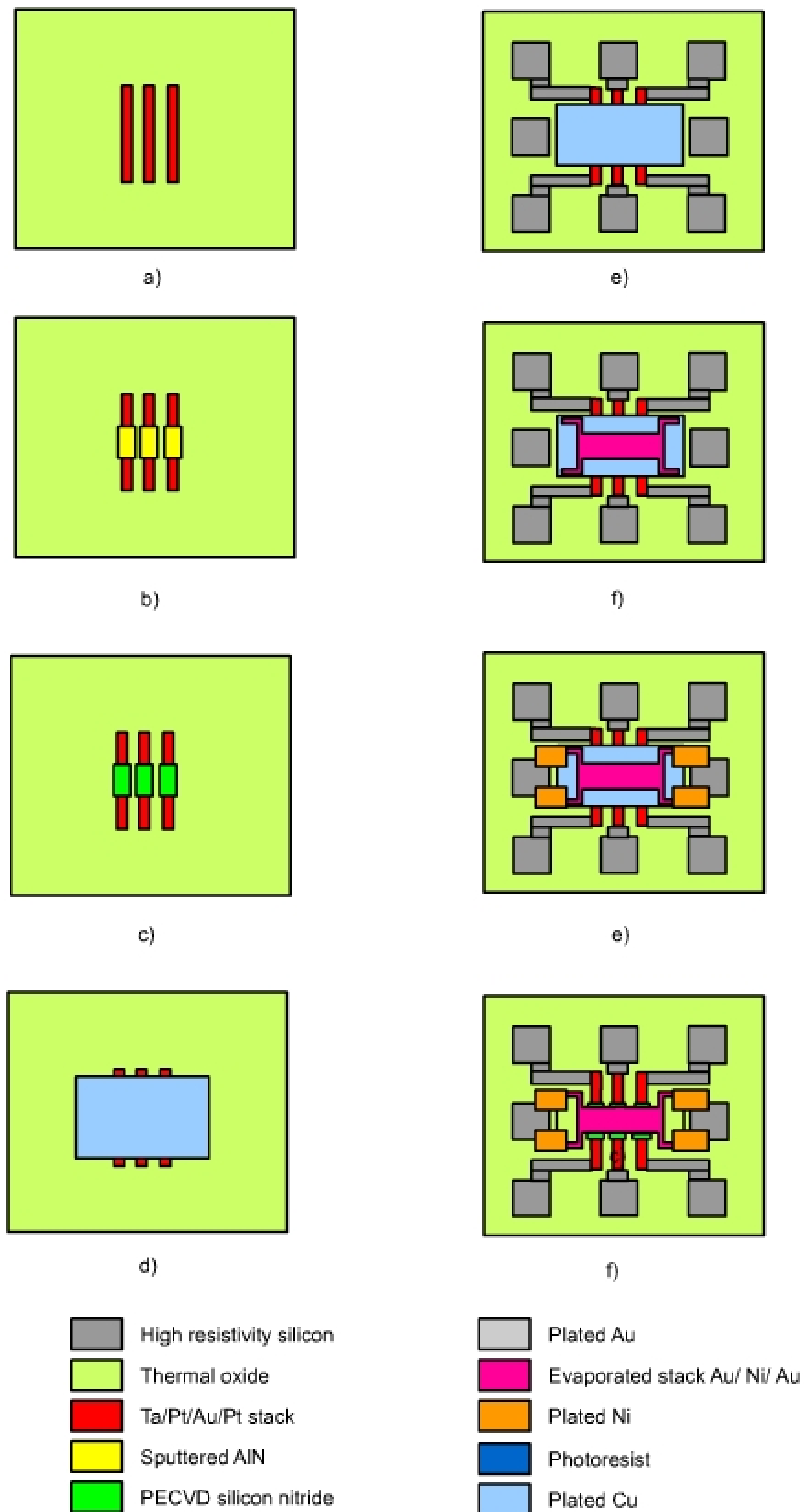

Figure 2-12: Top view of the process flow of MEMS Switch

Table 2-5: Layer names and material properties of MPW process.

No	layer	object	material to be structured material	structuring	properties	remarks
1	UPATH	underpath metallization	evaporated Ta/ Pt/ Au/ Pt	lift-off with resist mask	≈ 0.10 Ω/sq	20 nm/ 40 nm/ 300 nm/ 60 nm
2	PASS 1	thick dielectric on actuation electrodes	PECVD silicon nitride	RIE	300 nm thick ε = 7.5	contact holes minimum 10 × 10 µm if required
3	PASS 2	thin dielectric in the active switch area	sputtered AlN	wet etching	200 or 300 nm thick ε = 10	contact holes minimum 10 × 10 µm if required,
4	OS 1	sacrificial layer	plated Cu	wet etching	≈ 3 µm thick (after CMP)	starting layer 20 nm Ti/ 150 nm Cu,
5	LINES	conductive lines and interconnections	plated Au		≈ 3 µm thick	starting layer 10 nm Ti/ 100 nm Au,
6	BRIDGE	switch membrane	evap. stack Au/ Ni/ Au	ion-beam etching	≈ 0.06 Ω/sq	200 nm / 500 nm/ 200 nm, ≈ 5×10^8 Pa tensile stess
7	SPRING	anchoring structures and stiffening bars	plated Ni		≈ 16 µm thick	nearly zero stress, is plated on the same starting layer as LINES

2.6.1 RF MEMS Switch Process Flow

The fabrication steps of MEMS switch is depicted in Figure 2-11 and their top views are given in Figure 2-12. The process begins with a high resistivity silicon substrate with higher

than 3000 $\Omega \times cm^{-1}$. Its thickness is 675 μm and has 2000 nm thermal oxide on it as seen in step (a) of Figure 2-11. Then Ta/Pt/Au/Pt stack (20 nm/ 40 nm/ 300 nm/ 60 nm) is deposited by lift-off using a resist mask and forms the underlying metal contacts of the switch which can be seen in steps (b), (c) and (d) of Figure 2-11 and the mask can be seen step (a) of Figure 2-12. Following that two dielectric layer are deposited on to underlying contacts. First AlN of 200 or 300 nm thick is sputter deposited and patterned with reactive ion etcher (RIE) for both on the active area of the switch and on the actuation electrodes as seen in step (e) and (f) of Figure 2-11 and step (b) of Figure 2-12. Then additional PECVD silicon nitride (300nm thick) used to strengthen the dielectric on top of actuation electrodes used for switch operation as seen in steps (g) and (h) of Figure 2-11 and step (c) of Figure 2-12. Next, 3 μm Cu is electroplated and polished (with an evaporated starting layer of 20 nm Ti/ 100 nm Cu) which is the main sacrificial layer, and which should be below the free standing parts of the device as seen in the steps (h) and (i) of Figure 2-11 and step (d) of Figure 2-12. Following that, Au is plated with a starting layer of starting layer of 10 nm Ti and 100 nm Au which forms the CPW lines and pads of the switch (steps (j) and (k) of Figure 2-11 and step (e) of Figure 2-12). Then movable membrane of the switch is formed by evaporating a stack of Au/ Ni/ Au (200 nm / 500 nm/ 200 nm) and patterning by ion-beam etching (steps (l) and (m) of Figure 2-11 and step (f) of Figure 2-12). As the last lithography 16 μm step Ni is plated which forms the rigid anchors of the switch as seen in steps (n) and (o) of Figure 2-11 and step (e) of Figure 2-12. Finally, sacrificial layer is removed by wet etching and our switch is formed (steps (p) Figure 2-11 and step (f of Figure 2-12). This process flow is a part of multi wafer project and properties of the materials are given in Table 2-5.

2.6.2 Design Considerations, Calculations, Simulations

The dimensions of the designed switch are illustrated in Figure 2-13 and also the dimensions and properties of the used materials are given in Table 2-6.

The membrane of the switch composed of stack Au/ Ni/ Au materials of 200nm/500nm/200nm. So effective youngs modulus, poisson's ratio and density is calculated using equations 2-11,

$$E_{eff} = \frac{(E_{Au} \times E_{Ni})}{V_{Au} \times E_{Au} + V_{Ni} \times E_{Ni}}$$

$$\nu_{eff} = \frac{(\nu_{Au} \times \nu_{Ni})}{\nu_{Au} \times V_{Au} + \nu_{Ni} \times V_{Ni}} \qquad \textbf{(2-11)}$$

$$d_{eff} = \frac{(d_{Au} \times d_{Ni})}{V_{Au} \times d_{Au} + V_{Ni} \times d_{Ni}}$$

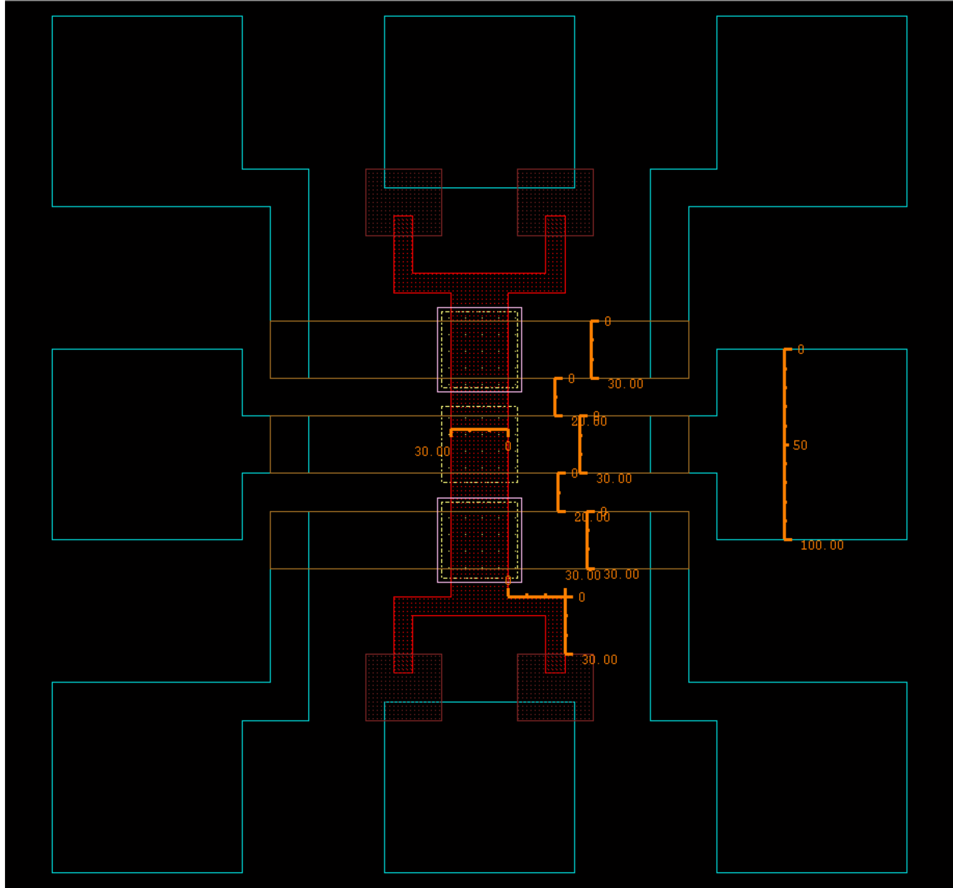

Figure 2-13: Dimensions of the designed switch.

where E_{Au} , ν_{Au}, d_{Au} and V_{Au} is the golds youngs modulus, poisson's ratio, density and volume fraction and E_{Ni} , ν_{Ni}, d_{Ni} and V_{Ni} is the nickels youngs modulus, poisson's ratio, density and volume fraction respectively.

Spring coefficient of the switch is calculated using formula 2-2 and the values in Table 2-6. Effective spring constant of four supporting beams in parallel with switch membrane is found as 1.33 N/m.

Table 2-6: Dimensions and properties of the designed switch

W=width of the membrane	30 μm
L= Length of the membrane	180 μm
t= thickness of the membrane	0.9 μm
Ws= width of supporting beam	10 μm
Ls= length of supporting beam x direction	30 μm
Lc= length of supporting beam y direction	30 μm
g = initial gap of membrane from substrate	3 μm
E_{eff}= Effective Youngs Modulus	98.73 GPa
Y_{eff}= Effective Poisson's Ratio	$12*10^7 N/m^2$
D_{eff}= Effective density	$12630 kg/m^3$

Equation (2-1) is used to calculate the pulling voltage to pull the membrane down and V_p is found as 20.23V. Equation 2-6 gives the damping ratio and resonant frequency of the switch which are found as $9.51x10^{-6}$ and 415 kHz. Also from equation 2-6 quality factor (Q) of the beam is calculated as 3.869.

A closed form solution for the switching time can be obtained for inertia-limited systems, that is for beams with a small damping coefficient and Q>2 as [12];

$$t_s = 3.67 \frac{V_p}{V_s \omega_0} \quad \textbf{(2-12)}$$

where t_s is the estimated switching time, V_p is pull-in voltage, V_s applied voltage and ω_0 is the resonant frequency. for $V_s=V_p$ the switching time is calculated as 8.84 μs. Decreasing the switching time is possible for higher applied voltages.

Lumped element model of the capacitive switch as seen in Figure 2-8 is created to evaluate the switch parameters as isolation and insertion loss. Up state and down state capacitance is found as 23.658 fF and 2.398 pF respectively using equations 2-9 and 2-10. L_p and R_p is evaluated as 50pF and 3 Ω from [12].

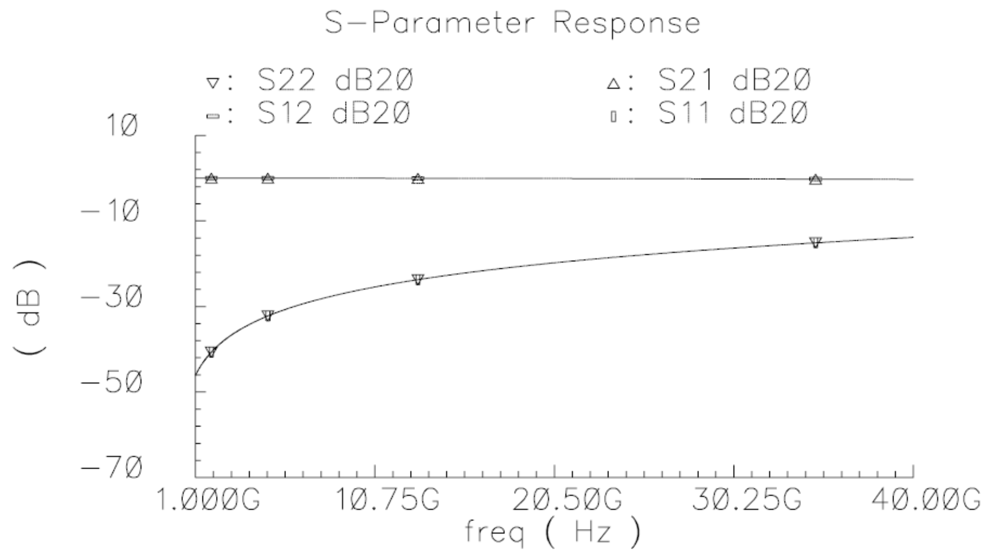

Figure 2-14: Up state RF performance parameters of Designed Switch

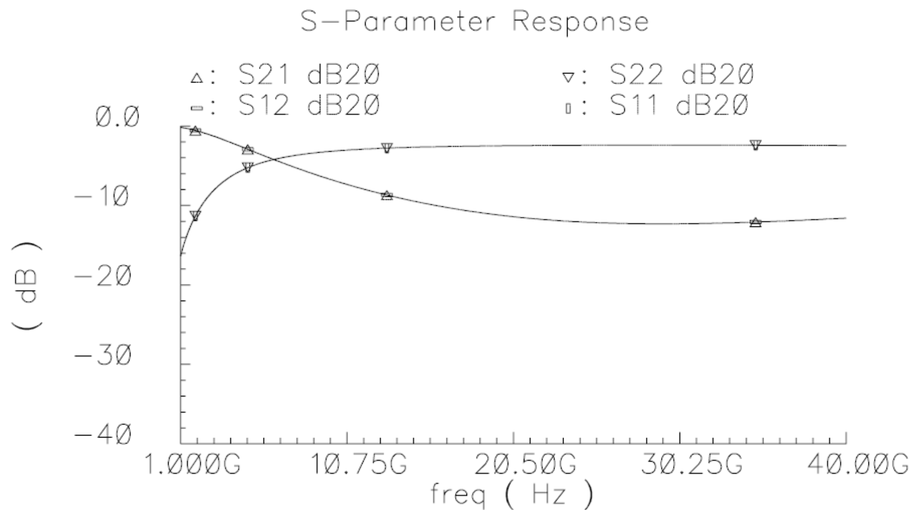

Figure 2-15: Down state RF parameters of designed capacitive switch

Figure 2-14 illustrates up state RF parameters of the designed switch. S_{12} describes the insertion loss of the switch. The switch shows very low insertion loss <0.1dB up to 40 GHz. Also it has a return loss which can be depicted by S_{11} below -20 dB up to 30 GHz. When the switch is down state the RF parameters is shown in Figure 2-15. Parameter S_{21} explain the isolation behavior of the switch in its down position, which is maximum (around -15 dB) between 20-30 GHz.

2.7 Design of RF MEMS Capacitive Switch Fabricated with In-house Capabilities

In addition to previous design, an RF MEMS capacitive switch is designed considering out in house capabilities for mask printing and fabrication capabilities. The mask printing is done on transparency with 15 μm minimum resolvable limit. The fabrication process had been carried out in Sabanci University Class-1000 Cleanroom.

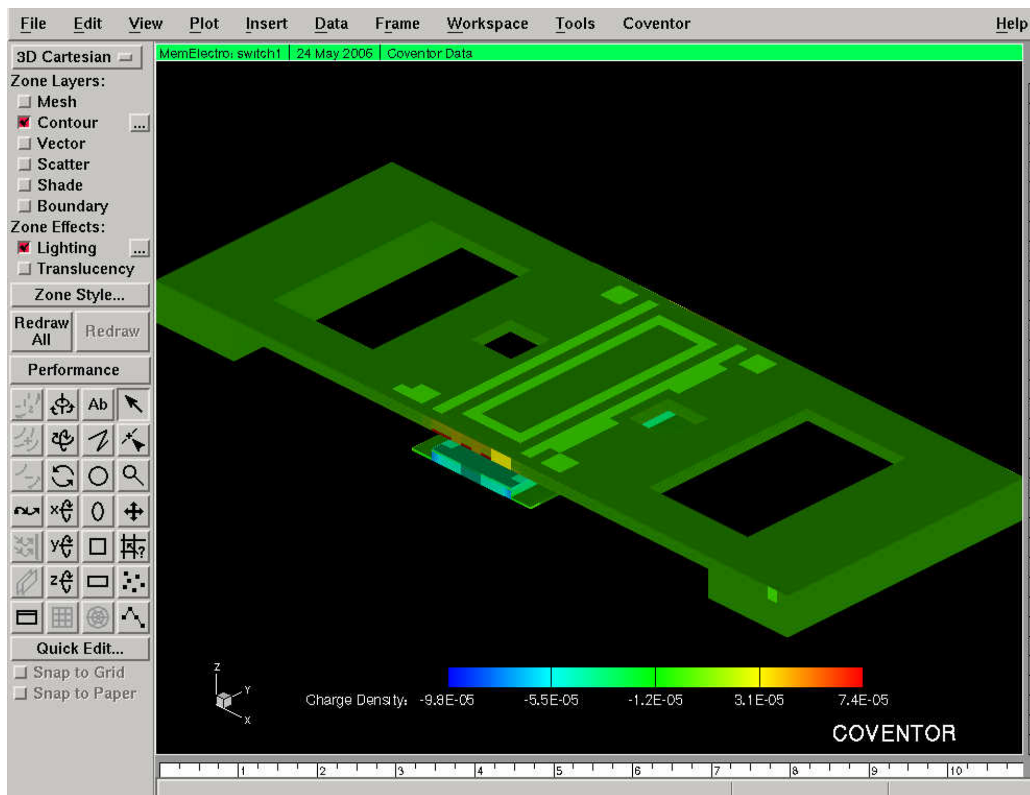

Figure 2-16: 3D view of designed capacitive switch for in-house fabrication

This capacitive switch design is very similar to abovementioned switch design and depicted in Figure 2-16. This switch also consists of a movable metallic plate suspended over the ground electrode and connected to the substrate at four points (anchors) through four beams but this time not L shape but simple cantilever beams. Also some samples include holes on the membrane in order to reduce damping. The switch is typically suspended 1.3 μm above the ground electrode and is electrostatically actuated when a DC voltage is applied between the switch and the ground electrode planes. When no DC bias is applied, the switch presents a very small shunt capacitance (typically in the order of a few fF) between the center conductor

and the ground planes. This is called the up or off state and the RF signal can propagate with minimal loss On the other hand, if the applied bias exceeds the actuation voltage, the switch collapses on the dielectric layer underneath it. The switch then presents a significant shunt capacitance, which is equivalent to an RF short-circuit. This is called the down or on state and virtually all the incident RF power is reflected back to the source.

2.7.1 Process Flow

Process flow starts with 300 nm silicon oxide sputter deposition on to silicon substrate as seen in step (a) of Figure 2-18. Then 200 nm of tungsten is deposited and patterned to form the underlying electrode as seen in step (b) and (c) of Figure 2-18 and step (b) of Figure 2-18. Then ~150 nm of silicon nitride is deposited and patterned to isolate underlying electrode as seen in steps (d) and (e) of Figure 2-18 and step (c) of Figure 2-18. Following that 1.3 µm PR is deposited and patterned as sacrificial layer (steps (f) and (g) of Figure 2-18 and step (d) of Figure 2-18). After that 1µm of Al is deposited and patterned to form the movable switch membrane shown in step (h) of Figure 2-18 and step (e) of Figure 2-18. Finally the sacrificial PR is released and our structure is formed as seen in step (i) of Figure 2-18 and step (f) of Figure 2-18. The details of each step will be given in following fabrication subsection.

Table 2-7: Dimensions and material properties of the switch

W=width of the membrane	120 µm
L= Length of the membrane	140 µm
t= thickness of the membrane	1 µm
Ws= width of supporting beam	20 µm
Ls= length of supporting beam x direction	70 µm
g = initial gap of membrane from substrate	1.3 µm
E= Youngs Modulus	70 GPa
Y= Poisson's Ratio	$17*10^7$N/m^2
d= density	2700 kg/m^3

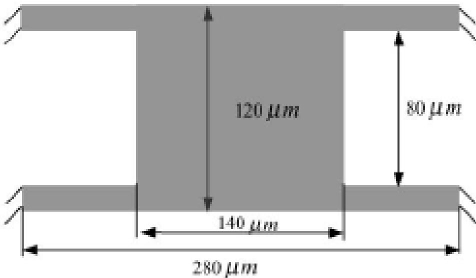

Figure 2-17: Dimensions of the membrane

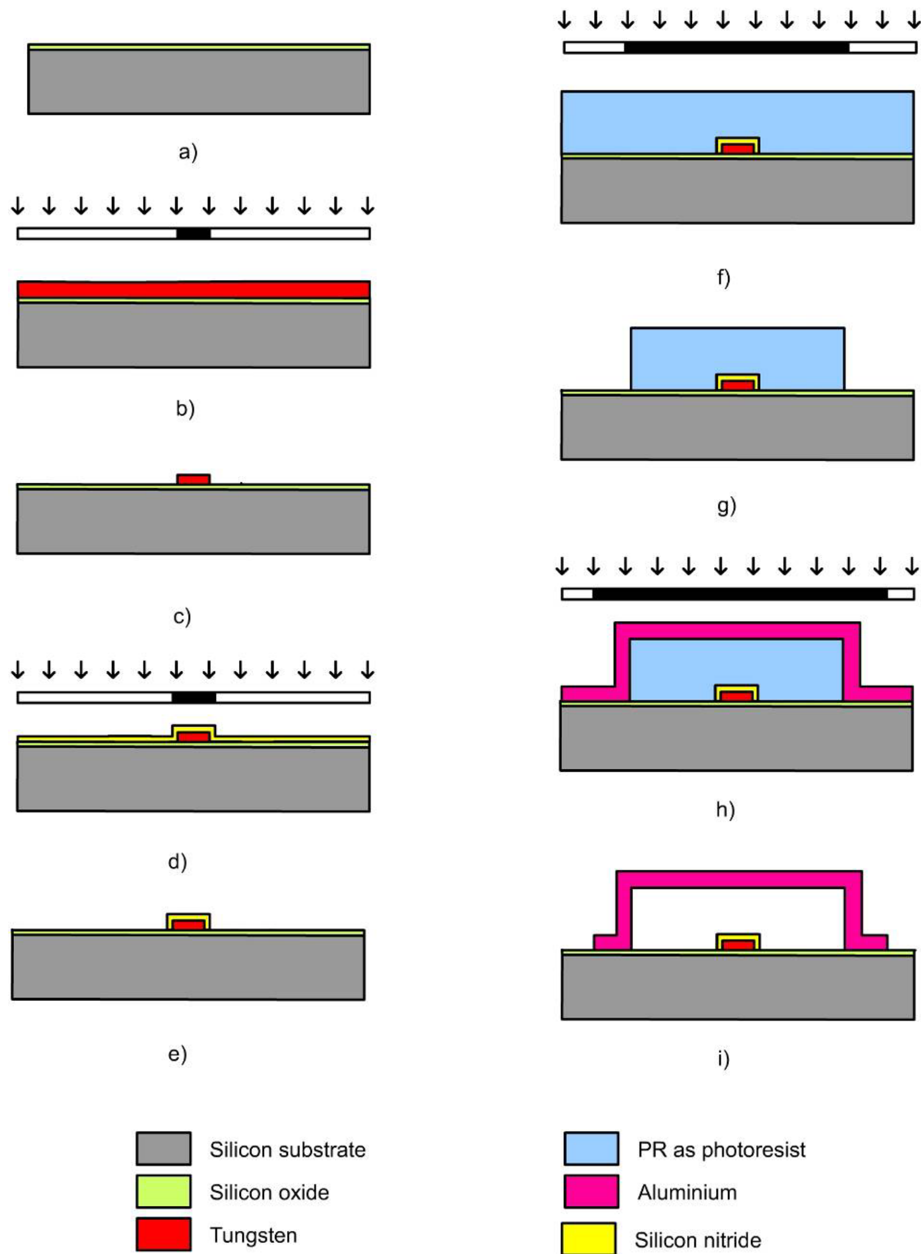

Figure 2-18: Process flow of the designed switch for in-house fabrication

2.7.2 Design Considerations, Calculations, Simulations

The dimensions of the designed switch are illustrated in Figure 2-18 and also the dimensions and properties of the used materials are given in Table 2-7.

Spring coefficient of the switch is calculated using formula 2-2 and the values in Table 2-7 . Spring coefficient of a single supporting beam is found as 2.4 N/m and effective spring coefficient for the switch is found as 8.1633 N/m.

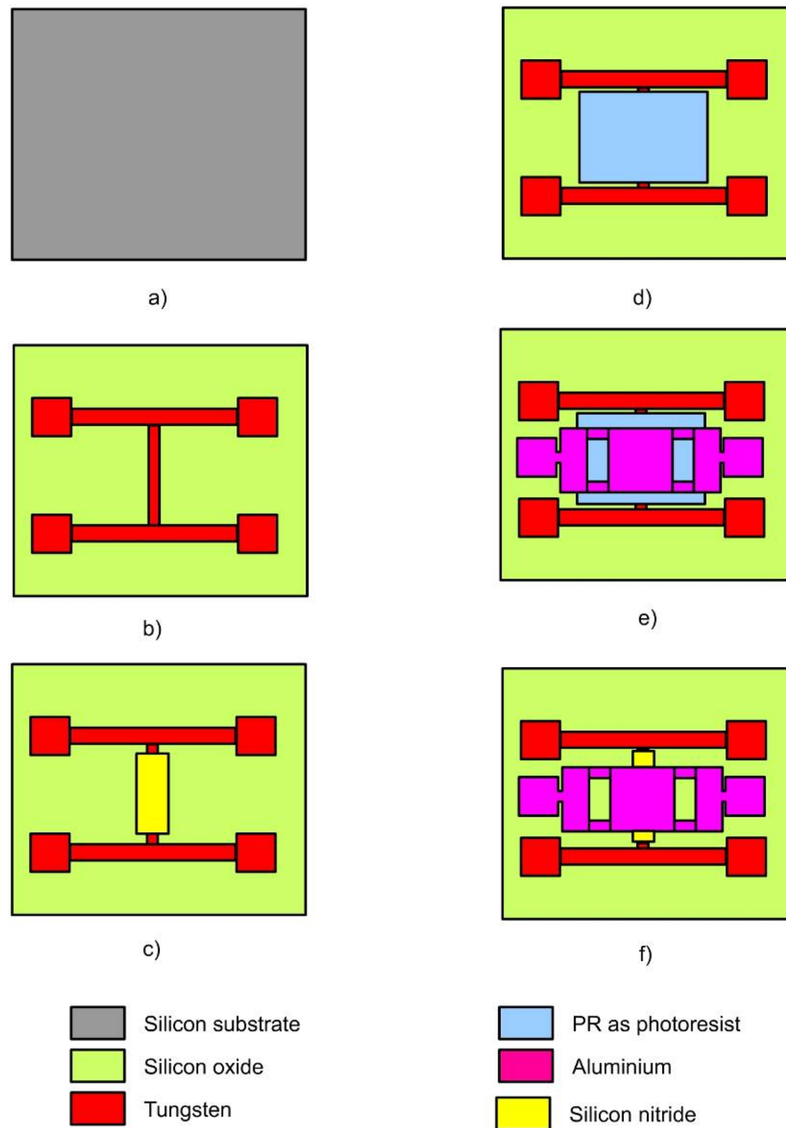

Figure 2-19: Top view process flow for in-house fabricated switch.

Equation (2-1) is used to calculate the pull-in voltage to pull the membrane down and V_p is found as 11.18V which is a low pull-in voltage and makes the switch suitable for low power applications. Also CoSolve tool of Coventorware® is used to calculate pull-in voltage and it is found as approximately 8.5V. Equation 2-6 gives the damping ratio and resonant frequency of the switch which are found as 1.1×10^{-3} and 367 kHz.

For high damping ratio switches (Q<0.5) switching time is estimated as [12];

$$t_s \cong \frac{9Vp^2}{4\omega_0 Q V_s^2} \quad \textbf{(2-13)}$$

where t_s is switching time, V_p is pull-in voltage, ω_0 is resonance frequency, Q is the quality factor and V_s is the applied voltage. For V_s=V_p switching time is calculated as 311µs.

Lumped element model of the capacitive switch is created to evaluate the switch parameters as isolation and insertion loss. Up state and down state capacitance is found as 31.6 fF and 0.99 pF respectively using equations 2-9 and 2-10. Lp and Rp is evaluated as 30pH and 8 Ω by simulations.

Figure 2-14 illustrates up state RF parameters of the designed switch. S_{12} describes the insertion loss of the switch. The switch shows very low insertion loss <0.1dB up to 40 GHz. Also it has a return loss which can be depicted by S_{11} below -20 dB up to 40 GHz. When the switch is down state the RF parameters is shown in Figure 2-15. Parameter S_{21} explain the isolation behavior of the switch in its down position, which is maximum (around -30 dB) near 30 GHz.

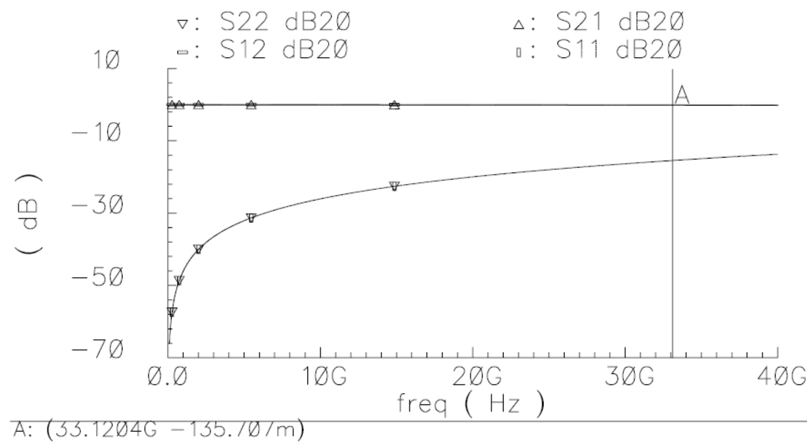

Figure 2-20: Up state RF parameters for the designed switch

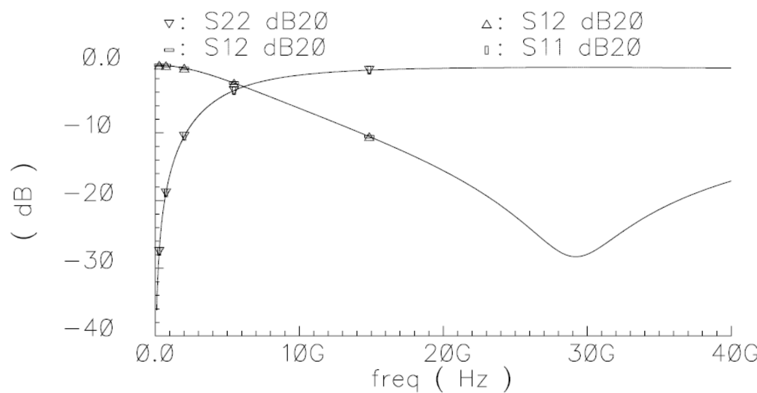

Figure 2-21: Down state RF parameters for the designed switch

2.7.3 Fabrication of designed switch

The designed switch is realized in Sabanci University's Class 1000 standard Cleanroom. The RF MEMS capacitive switch fabrication process is a five layer, 4 mask process. The masks are created in Coventorware® Layout Editor tool and shown in Figure 2-22 . The steps of the process are given in Table 2-8. Each step will be discussed in detail.

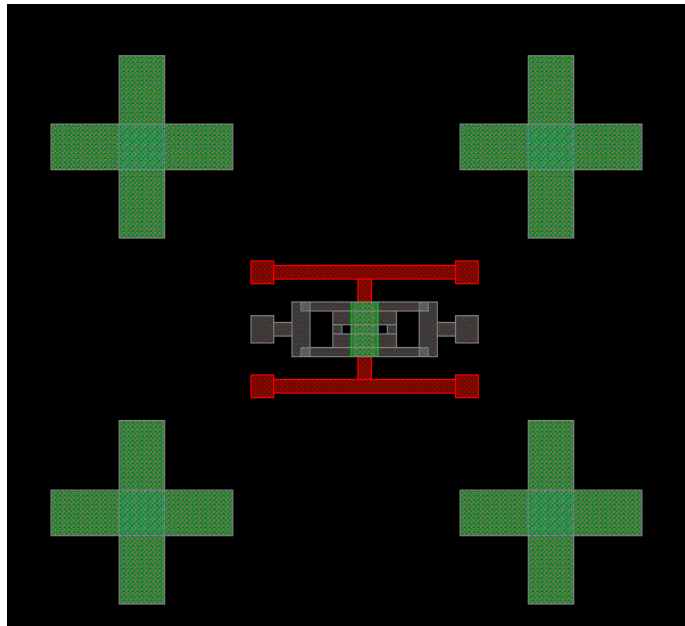

Figure 2-22: Masks of switch process created in Coventorware Layout Editor.

2.7.3.1 Substrate Cleaning

Silicon four inch wafers with orientation 100 is used in this process. As first step, we start with cleaning the samples. This step is a crucial step because any particles on the surface will affect the subsequent steps negatively. Typical cleaning process used is as follows;

- 5 minute acetone soak (optionally at 70-80 oC) in an ultrasonic shaker that removes particles from the surface by agitation. (Acetone removes almost all organics including PR residue. Acetone is highly volatile, and one should never let ACE dry on its sample)
- 5 minute methanol soak (optionally at 70-80 ^{o}C)
- 5 minute isopropanol soak (optionally at 70-80 ^{o}C) (methanol and isopropanol are primarily to clean ACE of the surface)

- 5 min DI-water rinse
- 5 min O2 plasma descum (usually at 300mT with 100W power)

Table 2-8: Fabrication steps summary of capacitive switch

Layer Name	Coating	Lithography	Etching
Isolation layer	SiO_2, sputter	--	--
Bottom electrodes	Tungsten, sputter	Photoresist (S1813), 35 seconds under UV	Wet etched with H_2O_2
Dielectric layer	Si_3N_4, sputter	Photoresist (S1813), 35 seconds under UV	Dry etched with SF_6 Plasma
Sacrificial layer	Photoresist (S1813), spinner	Photoresist (S1813), 35 seconds under UV	---
Bridge layer	Al, sputter	Photoresist (S1813), 35 seconds under UV	Wet etched with Al etchant*
Sacrificial Release	-----	-----	Shipley 1615 Remover, Acetone

* Al etchant: $16.H_3PO_4$-$1.CH_2COOH$-$1.HNO_3$-$1.H_2O$

2.7.3.2 Insulation Layer

After the cleaning part a 300 nm layer of oxide is deposited on to wafer using sputter deposition. RF magnetron sputtering is used with a SiO_2 target of 99.999% purity. The chamber is heated up to 250 ^oC and then plasma cleaning is applied to SiO_2 target with 120 W RF power, 35 sccm argon (Ar) flow and $2x10^{-2}$mbar chamber pressure for 10 minutes. After that deposition step is started with 150 W RF power, 35 sccm Ar flow and $2X10^{-2}$mbar chamber pressure for 90 minutes resulting ~400nm of oxide. The parameters are given in Table 2-9.

Table 2-9: SiO_2 RF sputtering parameters

Type	RF magnetron sputtering
Target	SiO_2
Temperature	250 ^oC
Cleaning	10min
RF power	150 W
Ar flow	35 sccm
Chamber Pressure	$2x10^{-2}$ mbar (GV5 position 650)
Deposition time	90 min

2.7.3.3 Bottom electrode and pads

Following isolation oxide deposition, the bottom electrode and pads are formed by sputter depositing and patterning tungsten (W). The W deposition started directly following the oxide

deposition. Tungsten deposition is made by DC magnetron sputtering using high purity W target. As a first step target cleaning is carried out with 200W DC power, 35 sccm Ar plasma and main chamber pressure of $2x10^{-2}$ mbar for 5 minutes in order to clean the residues on the target which can be affect the deposition quality. After that the DC power adjusted to 220W and with the same plasma (35 sccm Ar and $2x10^{-2}$ mbar chamber pressure) the deposition is carried out at 150^0C for 20 minutes resulting in 200 nm W layer. The parameters are given in the Table 2-10

Table 2-10: W DC sputtering parameters

Type	DC magnetron sputtering
Target	W
Temperature	150 ^{o}C
Cleaning	5min
DC power	220 W
Ar flow	35 sccm
Chamber Pressure	$2x10^{-2}$ mbar (GV5 position 500)
Deposition time	20 min

Following that, the wafer is taken to wet bench in order to pattern the metal contacts. Shipley's S1813 positive tone photoresist (PR) is used for photolithography step. First the sample is spin coated with PR using spinner. The program is selected as 500 rpm for 5 seconds to spread the PR, then 2000 rpm for 10 seconds and finally 4500 rpm for 45 seconds which results in 1.3µm uniform PR layer. Then 35 sec. of soft bake applied on hot plate with 95^0C temperature. Then the sample is taken to contact aligner as seen in Figure 2-23 and exposed to UV light for 35 seconds using bottom contacts mask. After that step, sample is directly put in the Shipley's MF 319 developer for approximately 45 sec. to remove the photoresist from the parts that is not covered with mask. The develop time is directly related to hard bake and exposure time. Sometimes the duration of the develop time is increased to 1 minute because of the quality of transparency masks such that the light areas of the mask do not passes the light as much as glass masks. This time is optimized for each mask by repeating this step and inspecting it under optic microscope. After we have good patterns the sample is put on the hot plate again for hard baking at 105°C temperature for 60 seconds. Hard bake step hardens the PR in order to make it unaffected from wet etching. All these parameters are listed in Table 2-11.

Table 2-11: Photolithography parameters

Spinning	500rpm-5sec./2000rpm-10sec./4500rpm-45sec.
Soft Bake	95°C Hot Plate 35 sec.
Expose	35 sec.
Develop	40-60 sec.
Hard Bake	105°C Hot Plate 60 sec.

Last step in the forming process of bottom electrodes is wet etching of the W layer that has PR patterns on it. Wet etching is chosen for patterning process because of it is easy and fast process. 30% H_2O_2 is used to etch W with an etch rate of 1000 A^0/min [33]. The process takes around 2 minutes and shown in Figure 2-24. Finally the remaining PR is removed with acetone rinse for 2 minutes and isopropanol rinse for 2 minutes. Also 2 min O2 plasma descum is applied to remove the PR completely. Resulting bottom contact is illustrated in Figure 2-25.

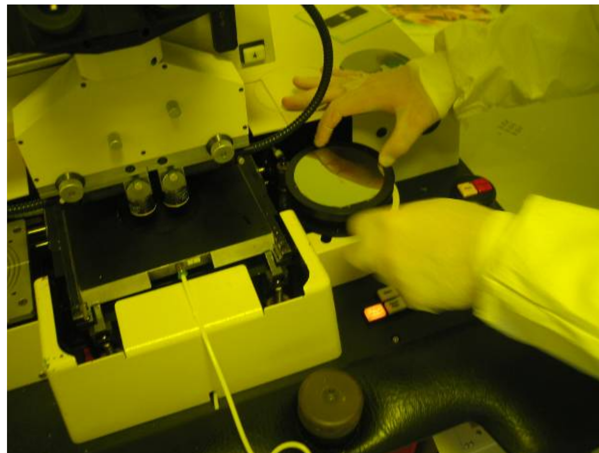

Figure 2-23: Sample placing in the contact aligner with cassette loader

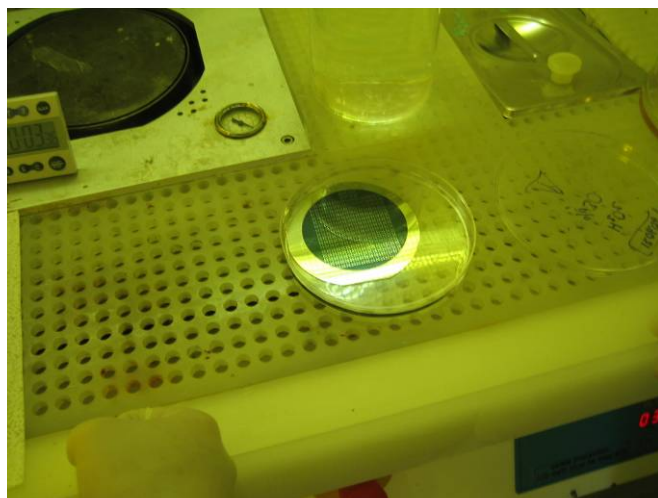

Figure 2-24: Wet etching of sample

2.7.3.4 Dielectric Layer Process

After forming bottom electrodes 150 nm layer of silicon nitride (Si_3N_4) is deposited on to wafer using sputter deposition. RF magnetron sputtering is used with a high purity Si_3N_4 target. The chamber is heated up to 250 ^oC and then plasma cleaning is applied to Si_3N_4 target with 120 W RF power, 35 sccm argon (Ar) flow and $2x10^{-2}$mbar chamber pressure for 10 minutes. After that deposition step is started with 150 W RF power, 35 sccm Ar flow and $2X10^{-2}$mbar chamber pressure for 60 minutes resulting ~150nm of oxide. The parameters are given in Table 2-12.

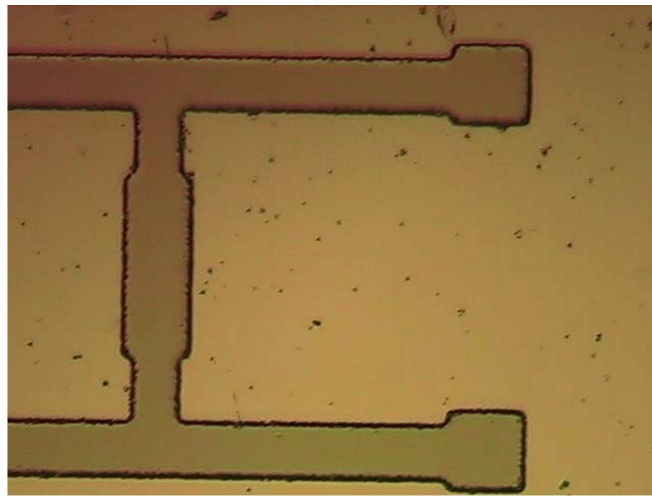

Figure 2-25: Bottom electrodes of the switch

Table 2-12: Si_3N_4 RF sputtering parameters

Type	RF magnetron sputtering
Target	Si_3N_4
Temperature	250 ^oC
Cleaning	10min
RF power	150 W
Ar flow	35 sccm
Chamber Pressure	$2x10^{-2}$ mbar (GV5 position 650)
Deposition time	60 min

After deposition step the sample is taken again to wet bench for patterning the coated layer with photolithography steps. The same parameters with the photolithography step of aforementioned layer are used which are shown in Table 2-11. However the different part of this patterning step was in the contact aligner part before UV light is applied. Because of

second mask is used, it must be aligned to the underlying pattern. So we align it using the alignment markers as shown in Figure 2-26.

Then reactive ion etcher (RIE) is used to etch the underlying nitride layer. The sample is put in the main chamber of RIE and it is vacuumed to the 0.0018 mbar for 30 minutes. Then SF_6 plasma is formed and the etching takes 10 min. Then the PR is removed using acetone and isopropanol rinses and O_2 plasma descum. Resulting structure is demonstrated in Figure 2-27.

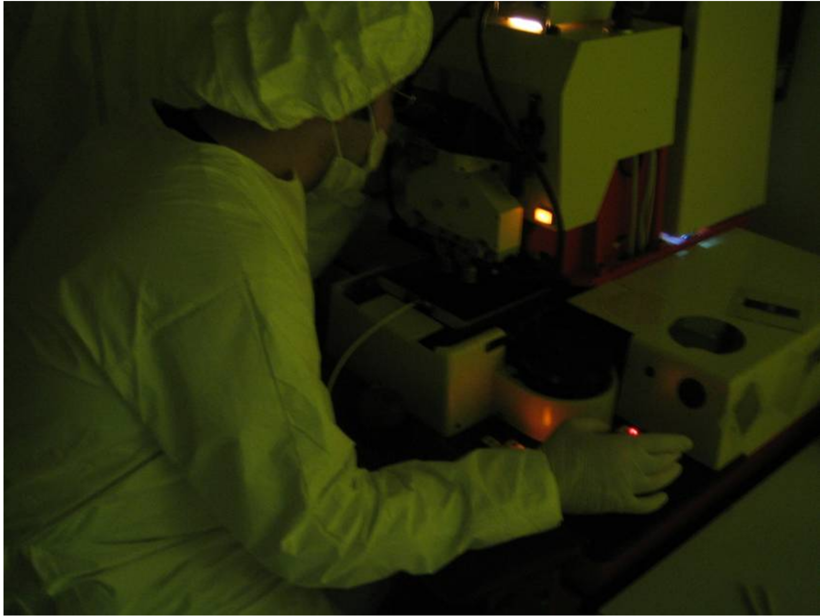

Figure 2-26: Aligning the mask to the underlying pattern

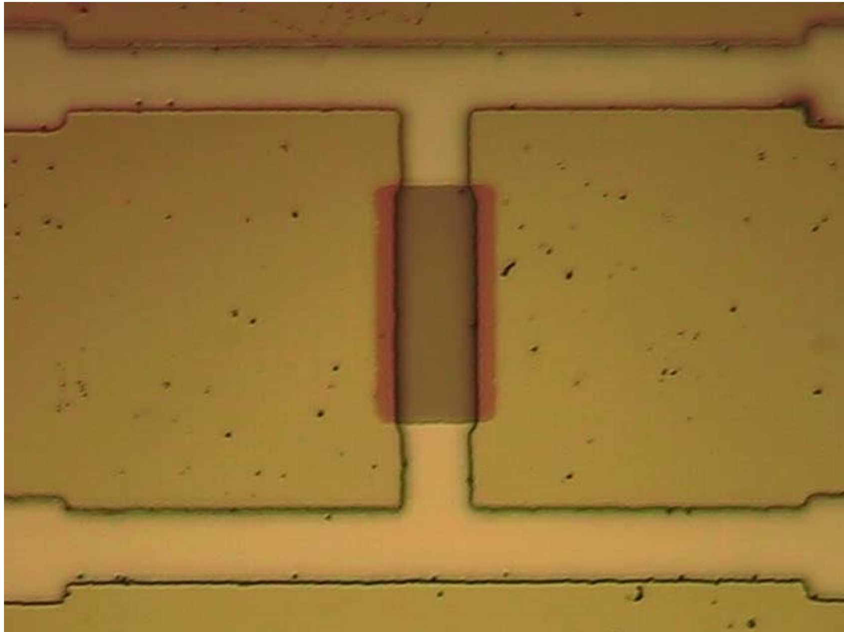

Figure 2-27: Patterned nitride layer on bottom electrodes

2.7.3.5 Sacrificial Layer

The sacrificial layer is necessary to suspend the bridge structure. Shipley's S1813 photoresist is used as sacrificial layer in order to make the process easier. The same photolithography parameters are used which is shown in Table 2-11 resulting 1.3µm thickness of PR layer. After the process O_2 plasma descum is applied in order to remove the PR residues completely which could be problem when releasing the structure. Resulting structure is shown in Figure 2-28.

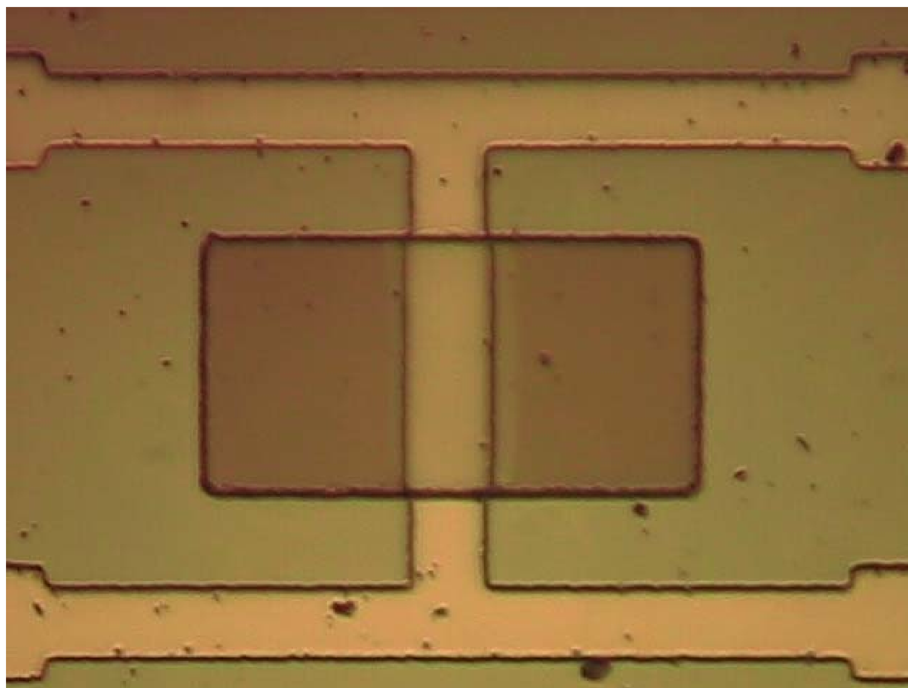

Figure 2-28: Structure after sacrificial layer is coated over bottom electrodes and dielectric layer

2.7.3.6 Bridge Layer

After coating sacrificial layer, the final deposition is the Al deposition which will form the suspended membrane of the switch where the RF signal will be passing. It also contains two pads for connecting the RF signal in and signal out. The deposition of Al is made by DC sputter deposition.

Al deposition is made by DC magnetron sputtering using high purity Al target. As a first step target cleaning is carried out with 200W DC power, 35 sccm Ar plasma and main chamber

pressure of $2x10^{-2}$ mbar for 5 minutes in order to clean the residues on the target which can be affect the deposition quality. After that the DC power adjusted to 220W and with the same plasma (35 sccm Ar and $2x10^{-2}$ mbar chamber pressure) the deposition is carried out below 100^0C for 40 minutes resulting in 1 µm Al layer. The temperature is kept low in order not to harden the PR sacrificial layer which will be problem in releasing it. The parameters are given in the Table 2-10

Table 2-13: Al DC sputtering parameters

Type	DC magnetron sputtering
Target	Al
Temperature	150 ^{o}C
Cleaning	5min
DC power	220 W
Ar flow	35 sccm
Chamber Pressure	$2x10^{-2}$ mbar (GV5 position 500)
Deposition time	20 min

Following that the sample is patterned again using PR with parameters in Table 2-11. The mask is aligned to underlying pattern using contact aligner.

After that the Al layer is patterned the uncovered parts are removed using the Al etchant. Al etchant is selected as $16.H_3PO_4$-$1.CH_2COOH$-$1.HNO_3$-$1.H_2O$ with an etch rate given as 2600-6600 A^0/min [33]. The wet etching takes about 3 min 30 sec.

2.7.3.7 Releasing the Sacrificial Layer

Final step of the switch fabrication process is releasing the sacrificial layer in order to form a free-standing membrane. As PR is used as sacrificial layer, Shipley's Microposit® remover 1165 is used to release it. The sample is put in to microposit remover bath for 15 min. and then isopropanol rinse is applied to remove the residues. Also some samples are released directly with acetone bath for 30 min. Resulting structures of the fabricated capacitive RF MEMS switches are shown in Figure 2-29 and Figure 2-30.

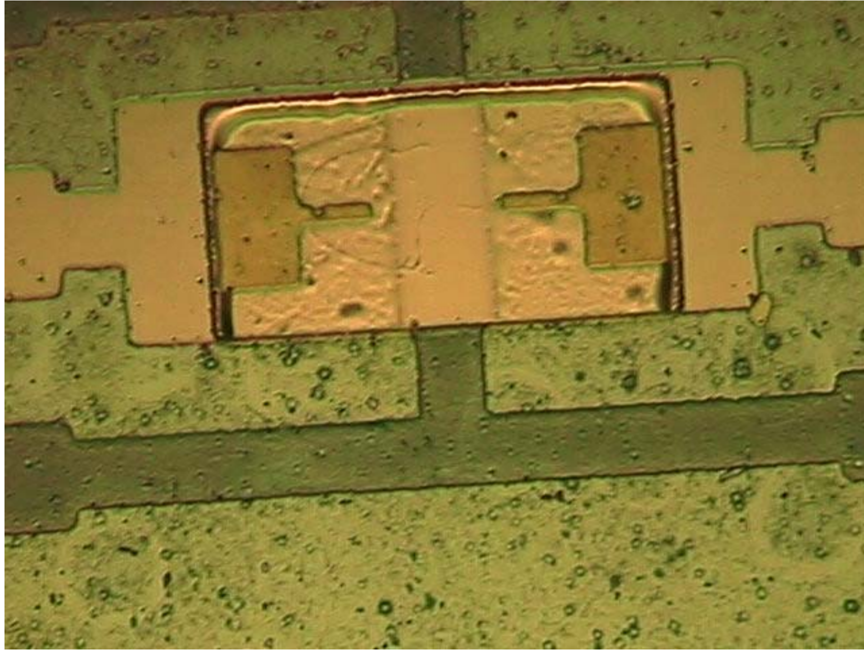

Figure 2-29: Final switch structure after sacrificial layer

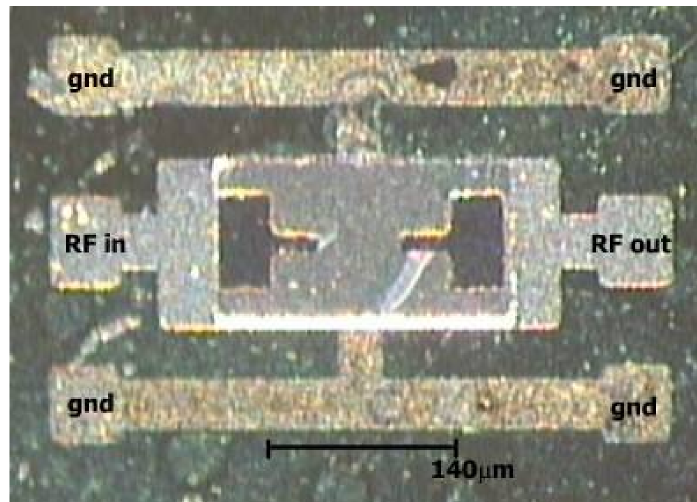

Figure 2-30: Final switch structure and definitions of pads

2.8 Testing of Fabricated RF MEMS Capacitive Switches

The fabricated capacitive switches are being tested using Karl-Zuss PM5 probe station with RF-DC probes. The RF performance tests are not completed for now and still being carried out and the test setup is trying to be calibrated. However using DC probes we have tested the

switching action of the fabricated switch. We have applied DC voltage between the ground electrode and membrane, and we have observed the movement of bridge. For voltages around 14-15 V the membrane touch down to bottom electrode as illustrated in Figure 2-31, and Figure 2-32. This voltage was close to our simulations and calculations which results around 8.5V and 11V pull-in voltage respectively. However there are stiction problems such as the top electrode do not come to its initial position when no DC voltage applied. The reason could be the flexibility of the anchors is not enough to pull membrane back. Another reason can be the PR residues between the membrane and ground plane.

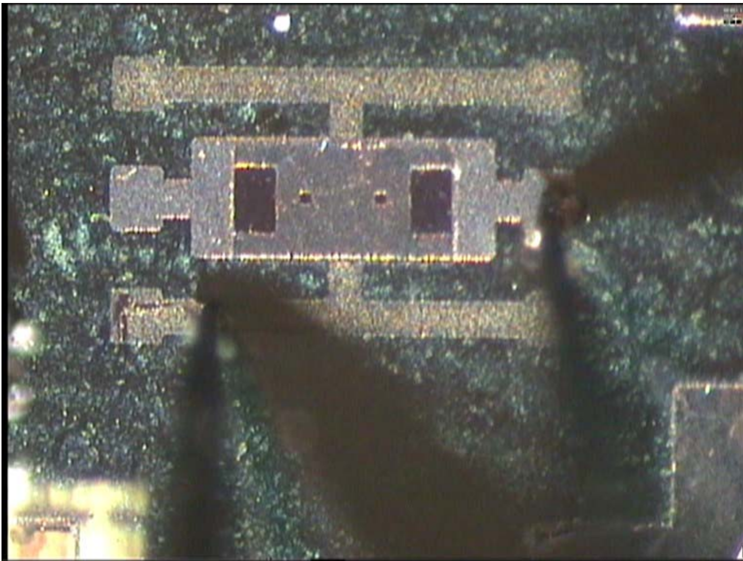

Figure 2-31: DC probes pulled down to top and bottom electrodes, switch is in its up position

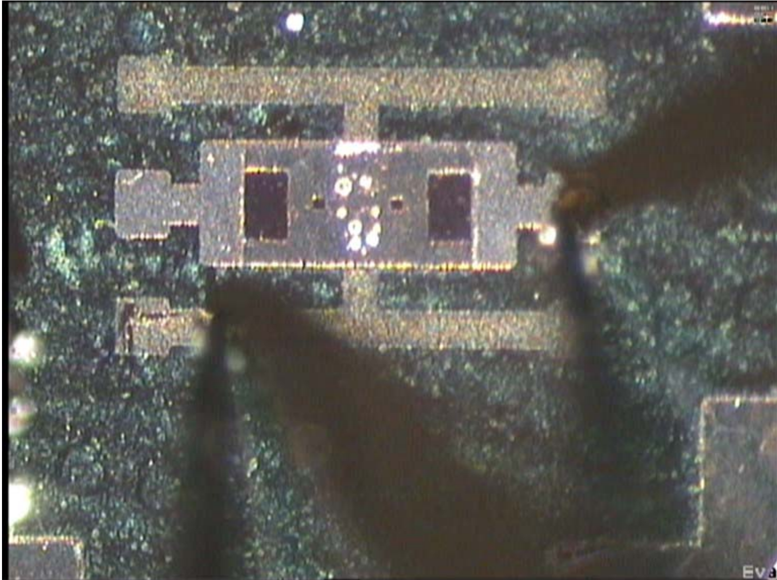

Figure 2-32: DC voltages of 14-15 V pull the membrane down and put switch in its down position

2.9 Conclusion and Future works

In this chapter general information about switches that are being used in blocks of transceivers and receivers are presented. Types of switches are explained and advantages of RF MEMS switches over other type of switches are listed. Also the performance parameters in evaluating a switch are given in detail. Additionally, literature survey has been made about RF MEMS switches and a detailed RF MEMS library is formed which can be used to compare and evaluate any designed switch with state of the art designs.

Moreover, important steps in designing RF MEMS switches are given in detail with various formulas and sketches. Two RF MEMS designs, for a MPW process and to fabricate in our Cleanroom, are presented and their design steps and fabrication steps are given in detail. There are some problems in the process. First problem is the sacrificial layer planarization. Due to non-planar surface profile of the sacrificial layer, the top beam layer is not planar and this probably changes the spring coefficient and occurring electrostatic force due to applied voltage. Slightly high pull-in voltage of 14V in measurement comparing to the simulated value of 8.5 V and hand calculated 11V can be resulted according to that effect. The other problem is when releasing the sacrificial photoresist some portion of it remains which probably affects the dielectric constant. This step must also be optimized.

The switch designed for MPW process have pull-in voltage of 20V and have a resonance frequency of 415 kHz. Its switching time is estimated as 8.84 μs for 20V applied voltage. Its up state and down state capacitance is found as 23.658 fF and 2.398 pF respectively. The switch shows very low insertion loss <0.1dB up to 40 GHz. Also it has a return loss -40 dB up to 40 GHz. The isolation behavior of the switch in its down position is maximum (around -25 dB) in 20-30 GHz range.

Switch designed and fabricated using in-house capabilities have a low pull-in voltage of around 14V. It has a resonant frequency of 267 kHz. The switching time of the switch is very high as 300 μs which left is out of the applications that needs fast switching time. The switch shows very low insertion loss <0.1dB up to 40 GHz. Also it has a return loss which can be depicted by S_{11} below -20 dB up to 40 GHz. The isolation behavior of the switch in its down position is maximum (around -15 dB) near 30 GHz.

The RF measurements of the fabricated switch are still continuing and measurements of MPW process switch is left for future work. The results of measurements will reveal the performances of switches better. It can be said that the switches are not competitive to state of the art switches but definitely it is a good step in the way of designing high performance switches.

3

Chapter 3
MEMS Varactors

3.1 Introduction

Present day communication systems require high quality passive components to realize filters and voltage controlled oscillators. Also circuit tunability has gain very high importance because of the desire for multiband circuits. Varactors are essential components wherever circuit tunability is required such as tunable matching networks, tunable filters, loaded line phase shifters and frequency controlling element in the LC tank of the voltage controlled oscillators (VCOs). However, as the move toward more compact form factors persists, and since good semiconductor varactors are incompatible with conventional IC processes, a number of efforts to demonstrate the performance level enabled by Microelectromechanical System (MEMS) varactors have been undertaken.

Varactors are an important component in many circuits. In IC technology a varactor is realized with reverse biased p–n junction. Asymmetrical doping is required to achieve a large tuning range. But lower doping on one side results in large series resistance thereby reduces the quality factor. Hence there is a trade-off between dynamic range and quality factor. Also Q varies with applied voltage. Thus passive components with very high quality-factor (Q) are difficult to achieve in conventional IC technology. Hence components like inductors and varactors are currently off-chip, in the applications requiring high quality factor. Microelectromechanical systems have the potential to replace these off chip components and enhance the performance. Most of the problems with diode varactor can be avoided with MEMS varactors. The main advantage of MEMS varactors is their high quality factor, which

is crucial for use in frequency selection. Additionally MEMS varactors do not produce harmonic distortion as in the case of diode varactors. Tuning range, and low actuation voltage are the two main factors that are the focus of the current research in varactors.

3.2 Varactor Characteristics

Varactor is a capacitor capable of changing its capacity through external volatge source. Varactors are characterized by a number of performance parameters: tuning ratio (C_{max}/C_{min}), quality factor (Q), absolute capacity value (C_{max} C_{min}), C-V characteristic, self resonance frequency and several others.

Among the parameters the tuning ratio and the quality factor are the most important. Varactor capacity is described by a well-known parallel-plate capacitor formula 3-1 with fringing fields neglected:

$$C = \frac{\varepsilon_o \varepsilon A}{d} \tag{3-1}$$

where ε0 is the electric permittivity of vacuum, ε is the relative dielectric constant of the medium between plates, A is the overlapping area of the parallel plates, and d is the gap between the plates. The quality factor of varactors and other passive components is defined as (where a sinusoidal excitation (voltage or current) is assumed to be applied to the component):

$$Q = 2\pi \frac{\left| E_{\max c} - E_{\max L} \right|}{E_{dis}} \tag{3-2}$$

where E_{maxc} is the maximum stored capacitive energy, E_{maxL} is the maximum stored inductive energy, E_{dis} is energy dissipated per cycle. From equation 3-2 it is seen that Q is a relative measure of the inherent losses, which must be as small as possible. As the inherent losses are included in the denominator, a large Q is desirable. If a varactor is modeled as an ideal capacitor and a resistor in series, then its quality factor can be expressed as in:

$$Q = \frac{1}{R\omega C} \tag{3-3}$$

where R is the resistivity of the resistor, ω is signal angular frequency, and C is ideal capacity .

3.3 Varactor Types

Within discrete circuit design only one varactor type seems to be available. This type is the capacitance diode, also called varactor diode or tuning diode (Figure-1). It utilizes the junction capacity associated with a pn-junction. When a reverse voltage is applied to a pn junction, the holes in the p-region are attracted to the anode terminal and electrons in the n-region are attracted to the cathode terminal creating a region where there is little current. This region, the depletion region, is essentially devoid of carriers and behaves as dielectric of a capacitor. The depletion region increases as reverse voltage across it increases. Therefore the junction capacity will decrease as the voltage across the pn-junction increases.

In contrast to the discrete case, two main types of varactors are available in integrated circuit design using a CMOS process. These main types are the junction varactor and the MOS varactor (Figure 3-2 [34]). Working principle of the former is identical to one of the varactor diode. In the latter, the variable capacitance is obtained through the gate-to bulk capacitance which is a function of the gate bias voltage.

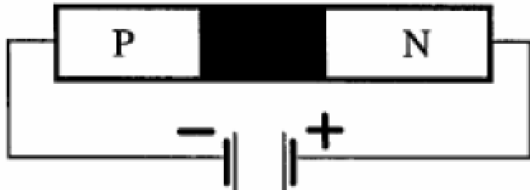

Figure 3-1: Discrete varactor diode

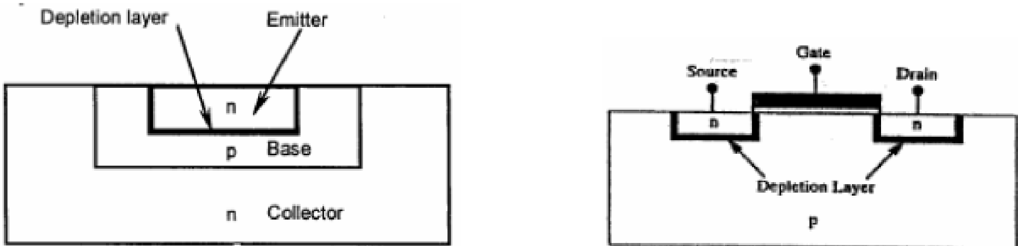

Figure 3-2: Integrated pn Junction Varactor on left and MOS Varactor on the right

There are also attempts to develop varactors based on ferroelectric materials [35], [36]. In such varactors one uses the ability of ferroelectrics ($BaTi0_3$, $PbTi0_3$, Ba,Srl-,Ti03 [35], SrTi03 [36]) to change their dielectric constants in response to applied voltage.

3.4 MEMS Varactors

In MEMS varactors either of parameters can be varied depending on the varactor type. Thus, there are varactors based on variation of the dielectric media between the plate, on variation of the overlapping plates area, and on variation of the gap between the plates. To realize this, various actuation principles employed in MEMS technology are used. The most popular among them are the electrothermal drive, the piesoelectric drive, and the electrostatic drive (which is most widely used). Electrothermal and piesoelectric drives allow to achieve good values of the tuning ratio (2.7 [37], 3.1[38]) and of the quality factor (200-300 at 10 GHz [37], [38]) and a linear CV-characteristic. However, these actuation types consume power and their switching time is normally larger than that for the electrostatic drive.

3.4.1 Varactors with Variable Dielectric:

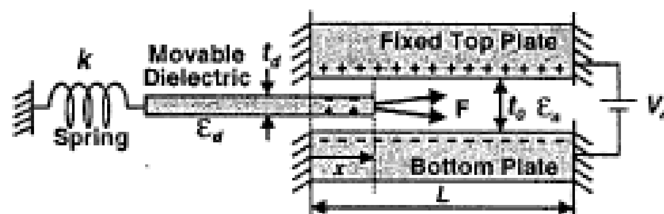

Figure 3-3: Schematic of a varactor with Variable dielectric

This function principle was realized in [39] Figure 3-3. A dielectric slab (silicon nitride) is suspended between the two capacitor plates (Cu) and anchored to the substrate outside the two plates vie spring structures. This dielectric is free to move, and is electrostatically displaced to alter either the overlap between it and the capacitor plates, or the fringing fields between them. In the former case, when a DC bias is applied between the two plates, the charges on the capacitor plates exert an electrostatic force on the induced charges in the dielectric to pull the dielectric into the gap.

3.4.2 Varactors with Variable Overlap Area

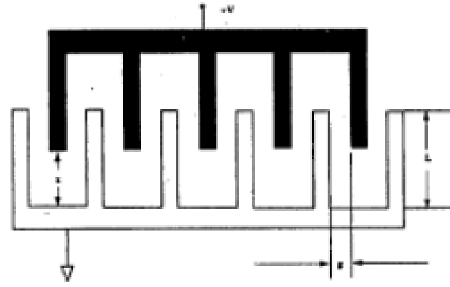

Figure 3-4: Schematic top view of comb drive varactor

This varactor type is represented by the comb-drive varactors (Figure 3-4). One of the combs is fixed whereas the other one can move towards it and back [40] or parallel to it (up and down) [41]. As the movable comb changes its position, the overlap area of the comb fingers also changes which leads to a change in capacity. Usually such varactors are made of polysilicon. Since resistance of polysilicon is comparatively high, quality factors of the varactors are not large. Metallic constructions generally have higher quality factors. However, to produce metallic comb-drive varactors one needs using LIGA or a similar high aspect ratio lithography method (that are quite expensive), because vertical structure dimensions are larger than horizontal ones.

3.4.3 Varactors with Variable Gap

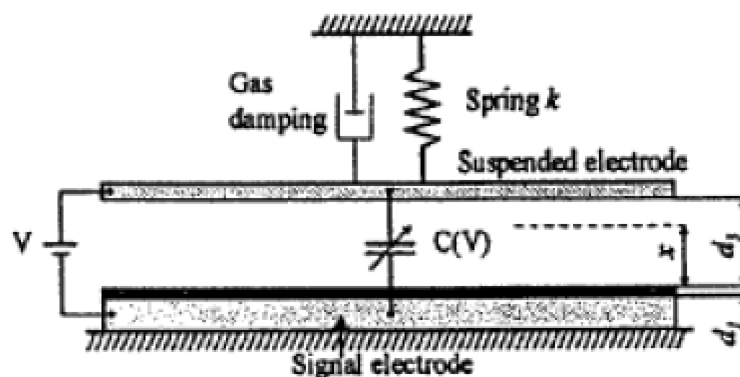

Figure 3-5: Functional model of parallel plate varactor.

This kind of MEMS varactors usually has a movable membrane (fixed at one or two ends) and one or several electrodes actuating it (they also can play a role of the capacitor plate or a signal line) and is very similar to a MEMS switch in design (Figure 3-5 [42]). Let us consider such a construction applying increasing voltage to it. In the off-state the membrane is not

actuated. As we increase the voltage between the membrane and the electrode below it, the membrane starts bending towards the electrode. During this step the electrostatic force and the restoring mechanical force are in equilibrium. This equilibrium exists, however, only if the gap between the membrane and the electrode is larger than 2/3 of the initial gap. As soon as the gap gets smaller (and simultaneously the applied voltage overcomes a certain threshold), the pull-in occurs and the membrane falls onto the electrode. If now we start to decrease the voltage, the membrane will not return to the initial position at once, but will stay on the electrode till the voltage reaches another threshold.

There exist two voltage ranges where equilibrium of forces is maintained and continuous change of the capacity is possible: below the first threshold (so called pull-in voltage) and above the second threshold (so called release voltage).

3.5 RF MEMS Varactors Library

Published studies from various companies, design groups and universities are examined and Table 3-1 is formed. This table includes typical performance parameters of RF MEMS varactors, such as; tuning range, maximum and minimum capacitance, quality factor and tuning voltage. With some processes MEMS varactors can have very high tuning ranges up to 2400% [43]. Parallel plate varactors' tuning range are typically vary from 200% to 1900%. Generally the min-max capacitance ratios are in the order of a few hundred fF to a few pF. Moreover, Quality factors up to 200 are reported. Actuation voltages are generally low however, in some designs it can go up to 40V [44].

3.6 RF MEMS Varactor Design

3.6.1 Design Flow and Hand Calculations

The simplest parallel-plate varactor type is shown in Figure 3-6 which consists of one suspended top plate and one fixed bottom plate, with an overlap area of A and initial spacing of x_0. When a DC voltage (V_{DC}) is applied across these two plates, the spacing will be decreased to $x_0 - x$.

Table 3-1: Library Formation of the RF MEMS Varactors

	Type	Tuning Range	C_{min} and C_{max}	Quality Factor	Tuning Voltage
[45]	Parallel Plate	56%-100%	0.3-0.8nF	High Q N/A	N/A
[46]	Finger Type	200%	1.75-5.3pF	N/A	N/A
[47]	Parallel Plate	410%	1.78-10pF	14.6	8.2V
[48]	Finger Type	14.5%-352%	153-175 fF 42-148 fF	24 -52	6 – 24 V
[49]	Parallel Plate	8.5% in air 10% in oil	317-344fF 725-799fF	72 in air 40 in oil	N/A
[50]	Parallel Plate	200%-1900%	300fF-2.25pF	30-200	N/A
[51]	Dual gap relay type	Up to 700%-1600%	0.2pF-1.6pF 0.75pF-12pf	250	~12
[52]	Parallel Plate	600%	0.5pF-3.5pF	N/A	2-3V
[44]	Parallel Plate	280%	5pF-17pF	8.784	40V
[43]	Parallel Plate Self Assembly	2400%	20fF-500fF	High Q N/A	N/A
[53]	Parallel Plate	39%	1.43pF-1.65pF	N/A	17
[53]	Dual Gap	310%	0.12pF-0.9pF	N/A	20V

While neglecting the fringe effect, the value of the capacitance (*C*) and the tuning range can be determined by;

$$C = \frac{\varepsilon A}{(x_0 - x)} \qquad \textbf{(3-4)}$$

where ε is the dielectric permittivity of the material between two plates and x is the displacement.

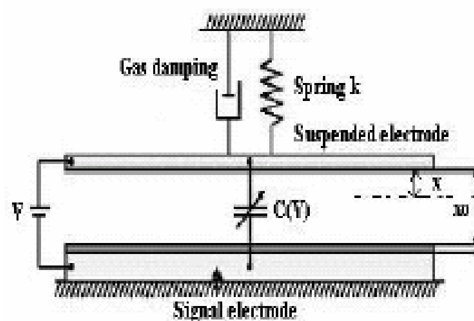

Figure 3-6: Parallel Plate Varactor

An electrostatic force (*Fe*) occurs when *V*DC is applied, between the two plates, which can be calculated by; [12]

$$F_e = \frac{1}{2}\frac{\partial C}{\partial x}V_{DC}^2 = \frac{1}{2}\frac{CV_{DC}^2}{(x_0 - x)} \quad \textbf{(3-5)}$$

The electrical spring constant k_e for the electrostatic force can be defined as; [12]

$$k_e = \left|\frac{\partial F_e}{\partial x}\right| = \frac{CV_{DC}^2}{(x_0 - x)^2} \quad \textbf{(3-6)}$$

Also, there is another spring constant k_m, *which* occurs by the mechanical suspension of the top plate. When the top plate is displaced, the suspension produces a restoring force (F_m). The magnitude of F_m is given by $Fm=k_m x$. At equilibrium, the magnitudes of F_e and F_m are equal, thus the expression for k_e in terms of k_m is

$$k_e = \frac{2k_m x}{(x_0 - x)} \quad \textbf{(3-7)}$$

From the above equation, two force constants are equal in magnitude when the value of x reaches x_0 /3. The corresponding value of *V*DC (at $x= x_0$ /3) is called the *pull-in* voltage (*V*PI). If *V*DC is continuously increased beyond *V*PI and x is beyond the critical point of x_0 /3, no equilibrium position can be reached until the two plates are snapped into contact (*pull-in* effect) since the mechanical springs essentially cannot provide sufficient restoring force to support the suspended top plate. In this case, the capacitance of the tunable capacitor can only be controllably changed to 150% of its original value at most. Theoretically, the maximum controllable tuning range is then 50% for an electro statically actuated parallel-plate tunable capacitor.

The spring constant of a fixed-fixed beam is found using;

$$k = 32EW\left(\frac{t}{L}\right)^3 \quad \textbf{(3-8)}$$

where E is Young's modulus, t is the thickness, W is the beam width, and L is the beam length [12].

The schematic model of another wide-tuning range tunable capacitor is shown in Figure 3-7. This varactor has a very high dynamic range but it is nonlinear as the capacitance varies inversely with the distance. It consists of three plates that are designated as E_1, E_2, and E_3.

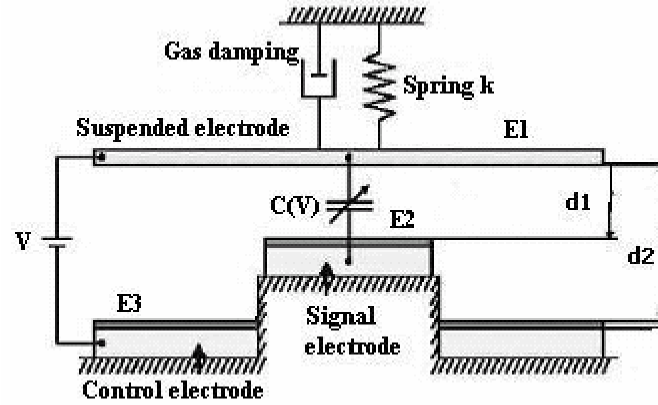

Figure 3-7: Dual Gap Structure

The fixed plate E_2 forms a variable capacitor with the plate E_1. DC voltage is applied between the movable top plate E_1 and fixed plate E_3. E_3 and E_1 are used to provide the electrostatic actuation and the distance between them is d_2. The capacitance between plates E_1 and E_2 is tuned by adjusting the magnitude of V_{DC}. When the top plate E_1 is pulled down by a distance x at a given applied V_{DC}, the tuning range is derived as

$$\frac{C - C_0}{C_0} = \frac{\frac{\varepsilon_0 A}{d_1 - x} - \frac{\varepsilon_0 A}{d_1}}{\frac{\varepsilon_0 A}{d_1}} = \frac{x}{d_1 - x} \quad \textbf{(3-9)}$$

This derived tuning range is valid as long as the pull-in effect between plates E_3 and E_1 does not occur.

If $d_1 > d_2/3$, then the maximum tuning range can be found by plugging in $x=d_2/3$ into above equation, thus maximum tuning range is $d_2/(3d_1 - d_2)$.

In the second case, $d_2/3 \geq d_1$, the pull-in effect will not occur at all. Assuming the plate E_1 can be pulled in by a distance ($x=d_1-\varepsilon$), where ε is infinitesimal, the maximum tuning range becomes $(d_1-\varepsilon)/\varepsilon$.

Theoretically, arbitrary tuning range can be achieved controllably. In reality, the achievable tuning range value also depends on other factors, such as surface roughness and curvature of E_2 and E_1.

The designed dual gap varactor is depicted in Figure 3-8. The designed varactor is in principle similar to the modified structure explained above; however, the only difference is that it is composed of three electrode pairs side by side in order to achieve greater capacitance values. Also integrating it with RF MEMS switches in order to increase the tuning range by switching these three capacitances is being thought to but this part is left as a future work.

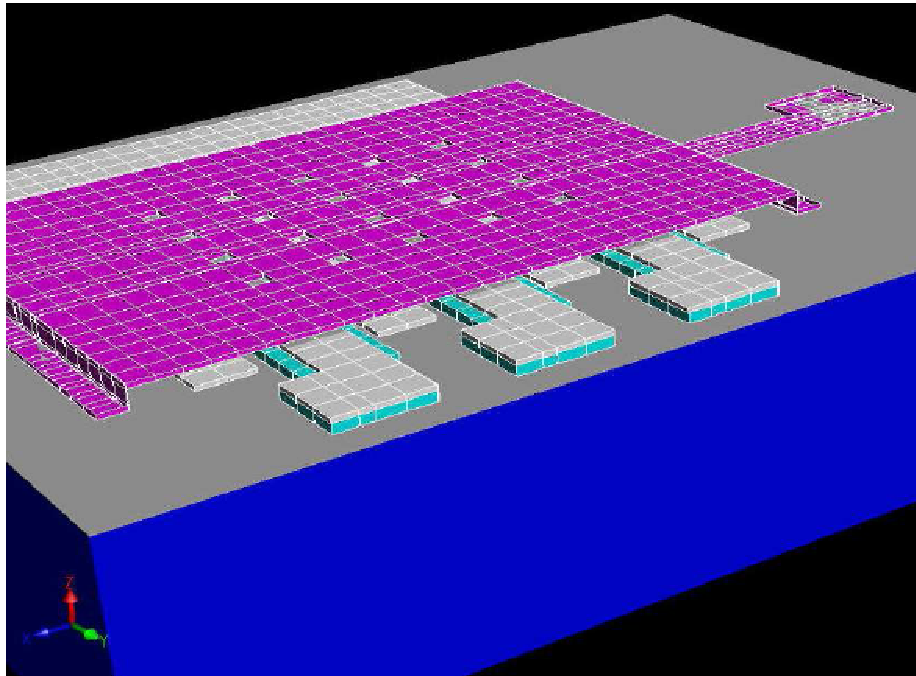

Figure 3-8: Designed dual gap varactor

The top beam has dimensions of W and L as 400µm and 600µm respectively and a single bottom electrode has a width (W_s) and effective length (L_e) (the part that is under top beam) of 50µm and 400µm respectively. The design includes four actuation electrodes, so the effective actuation area is given as;

$$A_{eff} = 4 \times W_s \times L_e \tag{3-10}$$

Spring coefficient of the beam is found using the equation 3-8 as 4.1481 N/m. Equating the applied electrostatic force with the mechanical resorting force due to the stiffness of the beam

(F=kx) actuation voltage can be calculated. So, using the formula 3-7 the actuation voltage in order to move the top plate 0.9μm is found as 4.46 V.

3.6.2 Fabrication Steps

Figure 3-10 describes the fabrications steps of designed MEMS Varactor. Fabrication process of dual gap varactor starts with coating oxide on silicon substrate as shown in step (a). Then 500nm thickness silicon nitride (Si_3N_4) is deposited and patterned with the purpose of forming various gap structure and leveling the bottom actuation and signal electrodes as seen in steps (b) and (c). Then 500nm of Al is deposited and patterned that creates the bottom electrodes of the dual gap structure as seen in steps (d) and (e). Later 100nm of SiO_2 is deposited and etched with a mask that leaves oxide only on the signal electrodes and these steps are demonstrated in steps (f) and (g). Following that, the sacrificial layer of BPSG (boron doped phospo-silicate-glass) is deposited and patterned with a mask that leaves it only under the suspending areas of the top layer as seen in steps (h) and (i). Then the top metal layer of Al is deposited and patterned forming the suspended membrane of the parallel plate varactor (step j and k). Last step is releasing the structure by etching the underlying BPSG and our final structure is formed (k).

3.6.3 Simulations

The simulations are performed using MemCap, MEMMech and CoSolve tools of Coventorware software. The mentioned fabrication steps in previous subsection are applied in to Coventorware. Also the masks are drawn using layout editor as shown below.

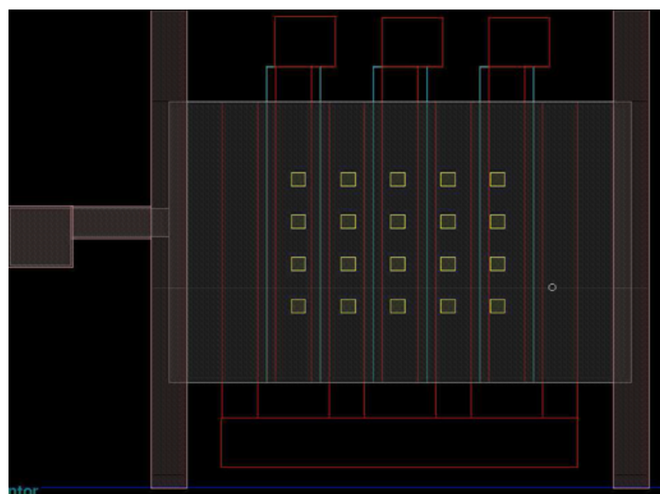

Figure 3-9: Mask layouts of designed MEMS Varactor

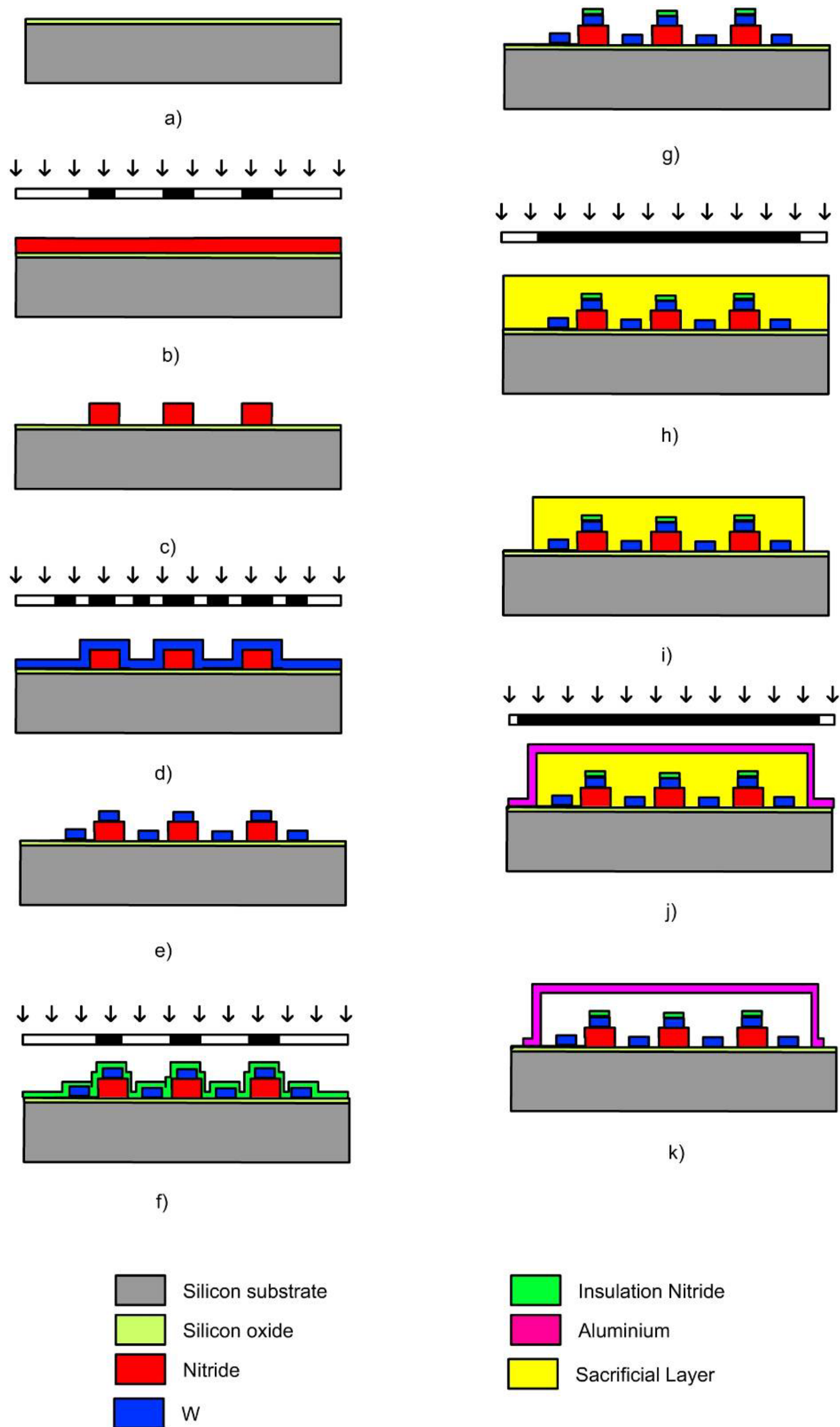

Figure 3-10: Fabrication process of dual gap RF MEMS Varactor

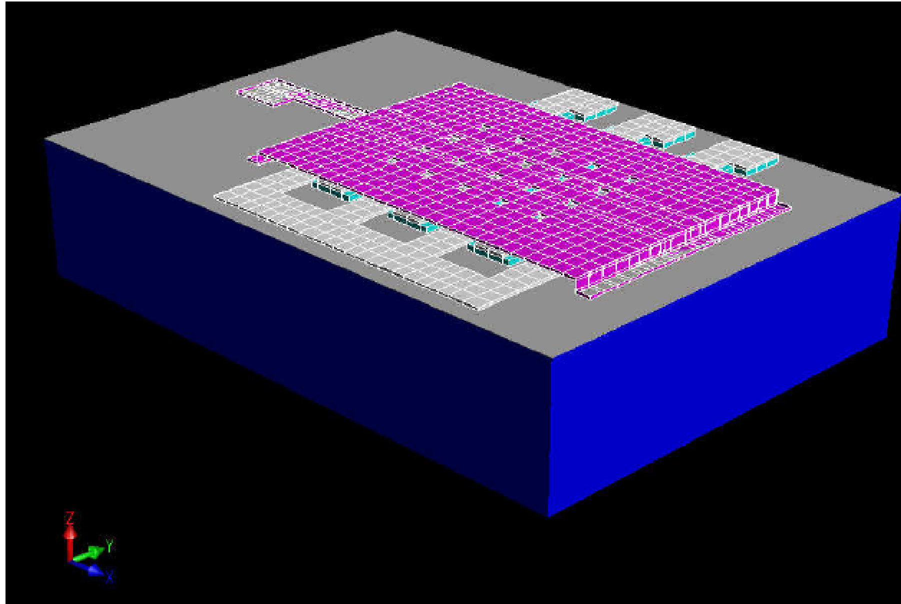

Figure 3-11: 3D structure of designed MEMS Varactor

Then the fabrication steps and layouts are combined to generate the 3D varactor structure which is shown in Figure 3-11.

First, an electrostatic analysis of the designed structure is performed by MemElectro tool. This solver basically produces an electrostatic solution by solving for the charge and capacitance interaction between top beam and the bottom electrodes. The resulting inter-electrode and self capacitance values are given in Figure 3-12

Capacitance Matrix (pF)

	Conductor_0	Conductor_1	Conductor_2	Conductor_3	Conductor_4
Conductor_0	9.007319E-01	-2.707141E-01	-2.105762E-01	-2.093835E-01	-2.100581E-01
Conductor_1	-2.707141E-01	2.831855E-01	-4.522539E-03	-1.897293E-03	-6.051563E-03
Conductor_2	-2.105762E-01	-4.522539E-03	2.167077E-01	-1.238191E-03	-3.707331E-04
Conductor_3	-2.093835E-01	-1.897293E-03	-1.238191E-03	2.137872E-01	-1.268214E-03
Conductor_4	-2.100581E-01	-6.051563E-03	-3.707331E-04	-1.268214E-03	2.177486E-01

Figure 3-12: Capacitance matrix result of MemElectro.

Conductor_1 is the bottom electrode, Conductor_0 is the top electrode, and Conductor_2, Conductor_3 and Conductor_4 are the signal electrodes, respectively.

It is observed that the initial capacitance of a single line is around 210 fF which is measured between top electrode and single signal electrode. This is the minimum capacitance value obtained since there is no mechanical bending of the structure. Since we have three of these lines in total, the resulting capacitance is three times this value, which is 630 fF.

On the other hand, the hand calculations yield a capacitance value for single electrode yields 177fF by the equation 3-4 which is close to the capacitance that Coventor had calculated for a single electrode. The difference might have been due to the complex capacitive interactions between different electrodes that are completely ignored in the theoretical analysis for the sake of simplicity.

The snapshot below shows the charge density at the electrode surfaces. It can be observed that the charge density is highest at the points where the top and the bottom electrodes are just on top of each other. This is mainly due to the voltage difference and the resulting capacitance between these two electrodes.

Next, mechanical simulation was performed using MemMech tool. As an external force on the top beam, 100 Pa pressure was applied. The computed displacements in x, y and z directions and the corresponding reaction forces are given in Figure 3-13. Although the maximum displacement occurs in the z direction, the maximum stress due to the applied pressure on the top beam is focused on anchor points. This is mainly due to the lateral stress caused by the applied pressure on the top.

The 3 dimensional side view of the varactor under external pressure is seen below. With a 100 Pa pressure on the top beam, the deflection amount is on the order of 1μm and the top and the signal electrodes make a contact.

mechDomain

	Maximum	Minimum
Node Displacement	1.251352E00	0
Node X Displacement	3.475145E-02	-1.27389E-01
Node Y Displacement	4.809938E-02	-4.496787E-02
Node Z Displacement	1.244993E00	-1.037415E00

rxnForces

	Fx	Fy	Fz
Anchor2	-1.788065E03	1.331278E-02	1.163361E01
Anchor1	1.788065E03	-1.331369E-02	1.164325E01

Figure 3-13: MemMech results of Node Displacements and rxn Forces

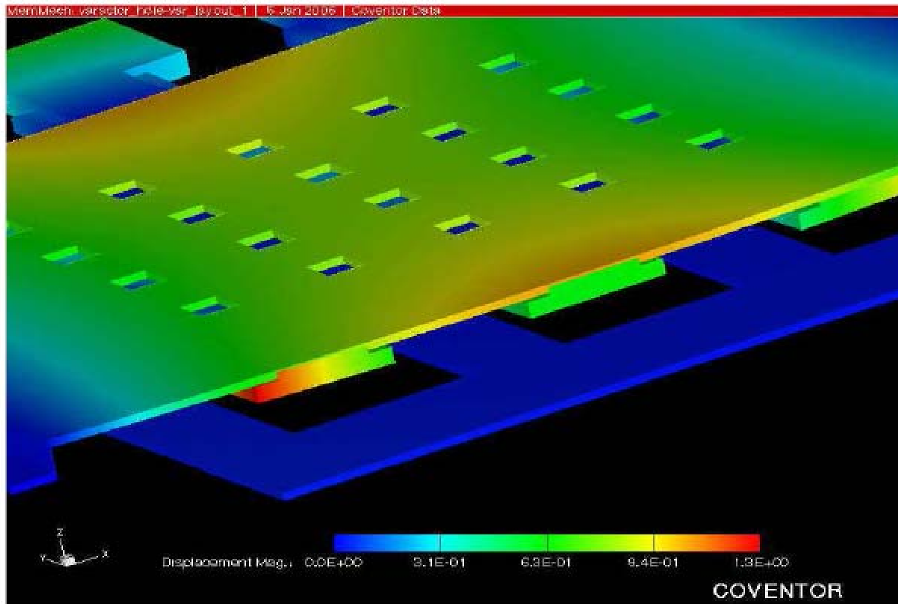

Figure 3-14: Deflection with 100 Pa pressure is applied to the beam

After that coupled electrostatic and mechanical analysis is performed by CoSolve tool of Coventor. This analysis gives us the deflection of the beam and the forces occurred under applied voltage. It has been observed that around 5V the top beam begin touching only middle electrode due to non uniform bending of the beam. The required voltage for the beam to touch the all bottom electrodes completely is found approximately 9V. These values differ with the hand calculation result of 4.5V. This is due to effects like non uniform bending and some parasitic elements are not taken into account in hand calculations.

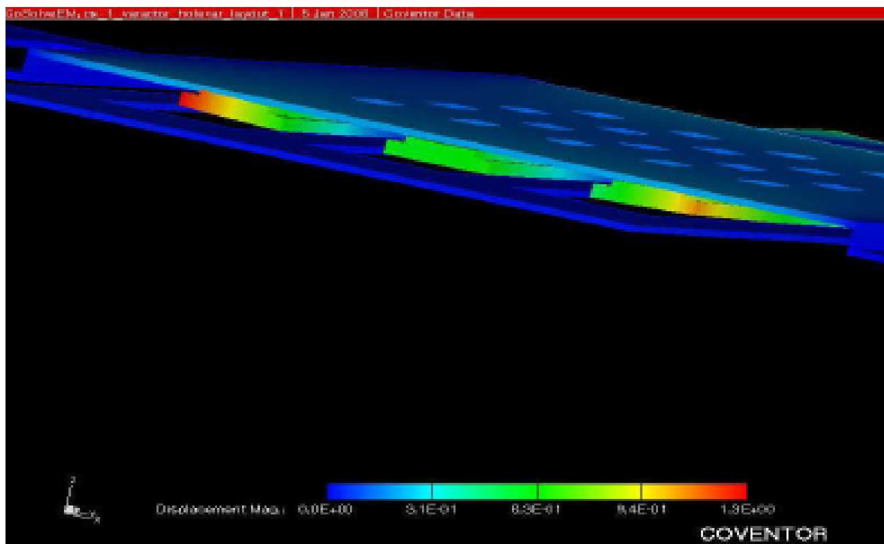

Figure 3-15: Beam deflection under applied voltage

Taking both the simulation results and hand calculations into account the capacitance change with increasing voltage is graphed and shown in Figure 3-16. Deflections for different voltages are simulated and Capacitance values according to these deflections are calculated in order to approximate the tuning range. It is seen that the capacitance changes from 531 fF for 0V to 2410fF for 9V. So the approximate tuning range is 350%. Also, the quasi-parabolic curve is in agreement with the theory since there is a square relation between the spring constant and the electrical potential.

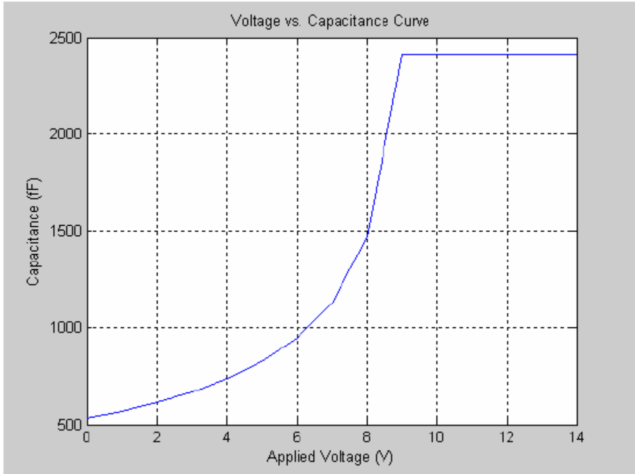

Figure 3-16: Capacitance change due to applied voltage

3.6.4 Fabrication Process

The designed varactor is realized in Sabanci University's Class 1000 standard Cleanroom. The RF MEMS varactor fabrication process is a six layer, five mask process. The masks are created in Coventorware® Layout Editor tool and shown in Figure 3-9.

3.6.4.1 Substrate Cleaning

Silicon four inch wafers with orientation 100 is used in this process. As first step, we start with cleaning the samples. This step is a crucial step because any particles on the surface will affect the subsequent steps negatively. Typical cleaning process used is as follows;

- 5 minute acetone soak (optionally at 70-80 ^{o}C) in an ultrasonic shaker that removes particles from the surface by agitation. (Acetone removes almost all organics including PR residue. Acetone is highly volatile, and one should never let ACE dry on its sample)

- 5 minute methanol soak (optionally at 70-80 ^{o}C)
- 5 minute isopropanol soak (optionally at 70-80 ^{o}C) (methanol and isopropanol are primarily to clean ACE of the surface)
- 5 min DI-water rinse
- 5 min O2 plasma descum (usually at 300mT with 100W power)

3.6.4.2 Insulation Layer

After the cleaning part a 300 nm layer of oxide is deposited on to wafer using sputter deposition. RF magnetron sputtering is used with a SiO2 target of 99.999% purity. The chamber is heated up to 250 oC and then plasma cleaning is applied to SiO2 target with 120 W RF power, 35 sccm argon (Ar) flow and 2x10-2mbar chamber pressure for 10 minutes. After that deposition step is started with 150 W RF power, 35 sccm Ar flow and 2X10-2mbar chamber pressure for 90 minutes resulting ~400nm of oxide. The parameters are given in Table 2-9.

Table 3-2: SiO_2 RF sputtering parameters

Type	RF magnetron sputtering
Target	SiO_2
Temperature	250 ^{o}C
Cleaning	10min
RF power	150 W
Ar flow	35 sccm
Chamber Pressure	2x10^{-2} mbar (GV5 position 650)
Deposition time	90 min

3.6.4.3 Bottom electrode and pads

Following isolation oxide deposition, next step is the bottom electrode formation. In dual gap design signal and actuation electrodes must be leveled and this is achieved by first depositing and patterning a nitride layer and then depositing and patterning Al contacts as considered in the design. However due to our in-house fabrication limitations depositing of thick nitride layer with sputter, copper is used in spite of nitride for leveling.

The Cu deposition started directly following the oxide deposition. Tungsten deposition is made by DC magnetron sputtering using high purity W target. As a first step target cleaning is carried out with 150W DC power, 35 sccm Ar plasma and main chamber pressure of $2x10^{-2}$ mbar for 5 minutes in order to clean the residues on the target which can be affect the deposition quality. After that the DC power adjusted to 200W and with the same plasma (35 sccm Ar and $2x10^{-2}$ mbar chamber pressure) the deposition is carried out at $150^{0}C$ for 20 minutes resulting in 500 nm Cu layer. The parameters are given in the Table 2-10

Table 3-3: Cu DC sputtering parameters

Type	DC magnetron sputtering
Target	Cu
Temperature	150 oC
Cleaning	5min
DC power	200 W
Ar flow	35 sccm
Chamber Pressure	2x10-2 mbar (GV5 position 500)
Deposition time	20 min

Following that, the wafer is taken to wet bench in order to pattern the metal contacts. Shipley's S1813 positive tone photoresist (PR) is used for photolithography step. First the sample is spin coated with PR using spinner. The program is selected as 500 rpm for 5 seconds to spread the PR, then 2000 rpm for 10 seconds and finally 4500 rpm for 45 seconds which results in 1.3µm uniform PR layer. Then 35 sec. of soft bake applied on hot plate with $95^{0}C$ temperature. Then the sample is taken to contact aligner and exposed to UV light for 35 seconds using bottom contacts mask. After that step, sample is directly put in the Shipley's MF 319 developer for approximately 45 sec. to remove the photoresist from the parts that is not covered with mask. After that the sample is put on the hot plate again for hard baking at $105^{o}C$ temperature for 60 seconds. Hard bake step hardens the PR in order to make it unaffected from wet etching. All these parameters are listed in Table 3-4.

Table 3-4: Photolithography parameters

Spinning	500rpm-5sec./2000rpm-10sec./4500rpm-45sec.
Soft Bake	95oC Hot Plate 35 sec.
Expose	35 sec.
Develop	40-60 sec.
Hard Bake	105oC Hot Plate 60 sec.

Following lithography process the underlying copper layer is wet etched. 8% HNO_3 is used to etch Cu. The process takes around 30-40sec. Finally the remaining PR is removed with acetone rinse for 2 minutes and isopropanol rinse for 2 minutes. Also 2 min O2 plasma descum is applied to remove the PR completely.

After forming the leveling part Al layer deposited and patterned to form the contacts. Al deposition is made by DC magnetron sputtering using high purity Al target. As a first step target cleaning is carried out with 200W DC power, 35 sccm Ar plasma and main chamber pressure of $2x10^{-2}$ mbar for 5 minutes in order to clean the residues on the target which can be affect the deposition quality. After that the DC power adjusted to 220W and with the same plasma (35 sccm Ar and $2x10^{-2}$ mbar chamber pressure) the deposition is carried out at 150^0C for 20 minutes resulting in 300 nm Al layer. The parameters are given in the Table 3-5.

After deposition part Al layer is patterned with the lithography steps described in Table 3-4. Following that the Al layer is patterned the uncovered parts are removed using the Al etchant. Al etchant is selected as $16.H_3PO_4$-$1.CH_2COOH$-$1.HNO_3$-$1.H_2O$ with an etch rate given as 2600-6600 A^0/min [33]. The wet etching takes about 1 min 20 sec. The resulting pattern is 300nm thick Al electrodes with a level difference of 500nm. The surface profile is measured and given in Figure 3-17. Also an optic microscope picture is given in Figure 3-18.

Table 3-5: Al DC sputtering parameters

Type	DC magnetron sputtering
Target	Al
Temperature	150 oC
Cleaning	5min
DC power	220 W
Ar flow	35 sccm
Chamber Pressure	2x10-2 mbar (GV5 position 500)
Deposition time	20 min

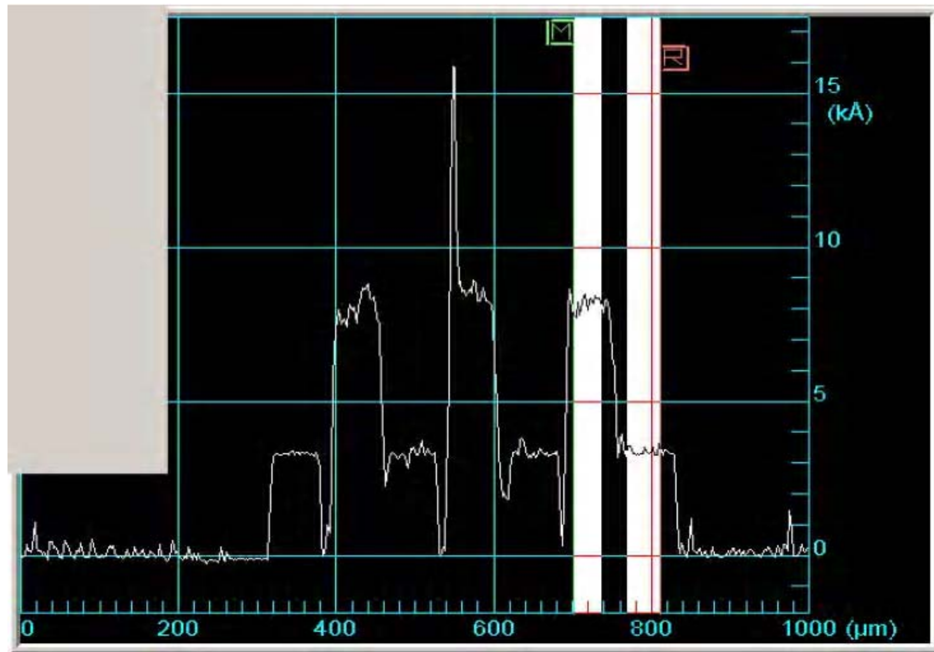

Figure 3-17: Surface profile of the sample after leveled contacts deposited and patterned

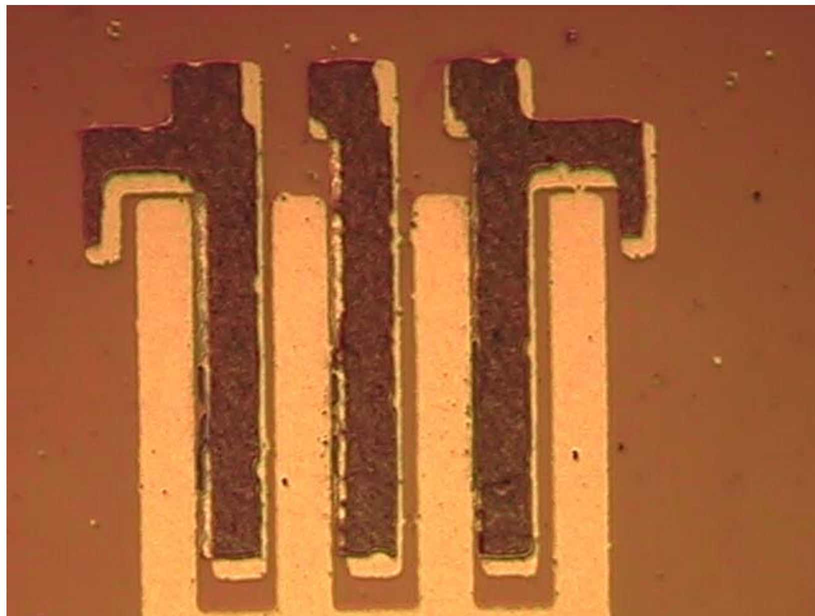

Figure 3-18: Leveled contacts under optic microscope

3.6.4.4 Dielectric Layer Process

After forming bottom electrodes 100 nm layer of silicon nitride is deposited on to wafer using sputter deposition. RF magnetron sputtering is used with a high purity Si_3N_4 target. The chamber is heated up to 250 ^oC and then plasma cleaning is applied to Si_3N_4 target with 120 W RF power, 35 sccm argon (Ar) flow and $2x10^{-2}$mbar chamber pressure for 10 minutes.

After that deposition step is started with 150 W RF power, 35 sccm Ar flow and 2X10^{-2}mbar chamber pressure for 45 minutes resulting ~100nm of nitride. The parameters are given in Table 2-12.

After deposition step the sample is taken again to wet bench for patterning the coated layer with photolithography steps given in Table 3-4

Then reactive ion etcher (RIE) is used to etch the underlying nitride layer. The sample is put in the main chamber of RIE and it is vacuumed to the 0.0018 mbar for 30 minutes. Then SF_6 plasma is formed and the etching takes 10 min. Then the PR is removed using acetone and isopropanol rinses and O_2 plasma descum.

Table 3-6: Si_3N_4 RF sputtering parameters

Type	RF magnetron sputtering
Target	Si_3N_4
Temperature	250 ^{o}C
Cleaning	10min
RF power	150 W
Ar flow	35 sccm
Chamber Pressure	2x10^{-2} mbar (GV5 position 650)
Deposition time	45 min

3.6.4.5 Sacrificial Layer

The sacrificial layer is necessary to suspend the bridge structure. Shipley's S1813 photoresist is used as sacrificial layer in order to make the process easier. The same photolithography parameters are used which is shown in resulting 1.5µm thickness of PR layer. After the process O_2 plasma descum is applied in order to remove the PR residues completely which could be problem when releasing the structure. Also this step is used to make the surface of the sacrificial layer more planar.

3.6.4.6 Bridge Layer

After coating sacrificial layer, the final deposition is the Al deposition which will form the suspended membrane of the switch where the RF signal will be passing. It also contains two pads for connecting the RF signal in and signal out. The deposition of Al is made by DC sputter deposition.

Al deposition is made by DC magnetron sputtering using high purity Al target. As a first step target cleaning is carried out with 200W DC power, 35 sccm Ar plasma and main chamber pressure of $2x10^{-2}$ mbar for 5 minutes in order to clean the residues on the target which can be affect the deposition quality. After that the DC power adjusted to 220W and with the same plasma (35 sccm Ar and $2x10^{-2}$ mbar chamber pressure) the deposition is carried out below 100^0C for 40 minutes resulting in 1 μm Al layer. The temperature is kept low in order not to harden the PR sacrificial layer which will be problem in releasing it. The parameters are given in the Table 3-7.

Table 3-7: Al DC sputtering parameters

Type	DC magnetron sputtering
Target	Al
Temperature	150 ^{o}C
Cleaning	5min
DC power	220 W
Ar flow	35 sccm
Chamber Pressure	$2x10^{-2}$ mbar (GV5 position 500)
Deposition time	40 min

Following that the sample is patterned again using PR with parameters in Table 3-4. The mask is aligned to underlying pattern using contact aligner.

After that the Al layer is patterned the uncovered parts are removed using the Al etchant. Al etchant is selected as $16.H_3PO_4$-$1.CH_2COOH$-$1.HNO_3$-$1.H_2O$ with an etch rate given as 2600-6600 A^0/min [33]. The wet etching takes about 3 min 30 sec.

3.6.4.7 Releasing the Sacrificial Layer

Final step of the switch fabrication process is releasing the sacrificial layer in order to form a free-standing membrane. As PR is used as sacrificial layer, Shipley's Microposit® remover 1165 is used to release it. The sample is put in to microposit remover bath for 15 min. and then isopropanol rinse is applied to remove the residues. Also some samples are released directly with acetone bath for 30 min.

Resulting RF MEMS varactor is depicted in Figure 3-19.

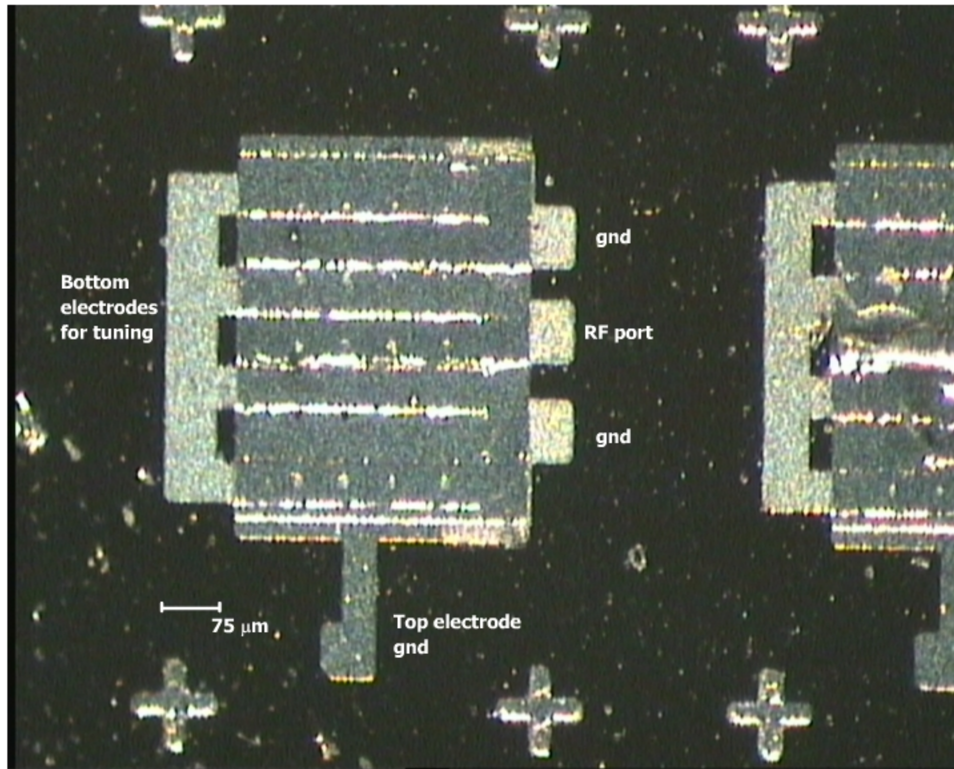

Figure 3-19: Final varactor structure.

3.7 Conclusion and Future Works

In this chapter RF MEMS based varactors are studied. Types and state of the art examples of MEMS varactors are given. Also selected publications are examined and a MEMS varactor library is formed.

A dual gap parallel plate varactor structure is designed. Design steps and hand calculations are given in detail. In hand calculations 0-4.5 V actuation voltage is found sufficient for tuning from C_{min} to C_{max}. C_{min} of a single electrode is calculated as 177 fF. Then the design is simulated using Coventorware. In the result of MemElectro simulation initial capacitance of a single electrode is found as 210fF. This difference is because the fringing capacitance effect is neglected in the hand calculations. Results of CoSolve simulation revealed that at 5V top beam only touches middle electrode and at 9V it touches all electrodes. The difference between the expected actuation voltage and the simulated one is probably because of non-uniform bending of the top beam. Furthermore, approximate capacitance variation with actuation voltage is graphed using simulations and calculations. Designed varactor shows a capacitance change from 530 fF to 2.4 pF for the applied voltage from 0 to 9V and show a tuning range of 350%.

The designed varactor is fabricated using our in-house Cleanroom. However some parts of the design cannot be realized and being changed due to our in-house fabrication limitations. The leveling of the electrodes is decreased to 500nm. Also the planarization of the sacrificial layer cannot be achieved due to fabrication limitations so the two gap values cannot be achieved as in design. However as a starting point a complete varactor fabrication is proposed although the performance parameters of it decreased.

As a future work, ways to prevent non-uniform bending of the beam will be investigated. Although the varactor gives a tuning range of 350%, further ways to increase it can be examined. Using MEMS switches, as mentioned in the chapter, can be good option to accomplish the tuning range improvement which is left for future work. Planarization of the sacrificial layer is another problem that has to be overcome. There are some techniques like CMP or coating thick polymers and then etching them. Exploring them is left for future work.

4

Chapter 4
RF MEMS Inductors & Above IC Technology

4.1 Introduction

Extensive research is being conducted in the area of wireless front-end circuitry aiming at the construction of efficient passive components such as inductors. Inductors are found e.g. in filters, impedance matching networks and voltage controlled oscillators. The performance of both transceivers and receivers depends heavily on this component. Its typically high loss translates into poor noise characteristics or low Q factors and presents a major design bottleneck. Consequently, many centers have been actively involved in research to improve the quality factor of RF inductors. Furthermore, tunable inductors can give the advantage of optimizing the performance of RF front-end circuits by adjusting the center frequency of a band-pass filter, changing the impedance given by a matching network and tuning the oscillation frequency of a VCO [54], [55].

Inductors are key elements determining the performance of tuned circuits, in particular, impedance matching networks, low noise amplifiers and voltage-controlled oscillators (VCO). Improving the gain, power dissipation or phase noise of these circuits has, in turn, led to incorporating MEMS-based on-chip inductors.

MEMS inductors aim to increase the performance of on chip inductors in terms of quality factor "Q" and resonant frequency. MEMS inductors try to achieve higher Q than the off chip discrete inductors. Two methods are used for this purpose in the MEMS structures: Bulk

micromachining and surface micromachining [54], [55]. In bulk micromachining the wafer is been processed and as seen in Figure 4-1 the substrate has been eliminated from underneath the spiral trace.

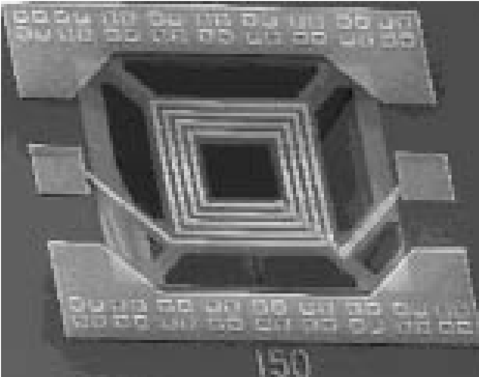

Figure 4-1: Bulk-Micromachined MEM Inductor

In Surface micromachining layers are deposited on the substrate and solenoid-like inductors are created above the substrate as shown in Figure 4-2.

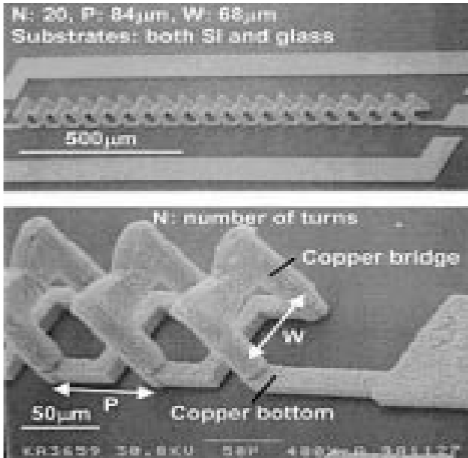

Figure 4-2: Surface-Micromachined MEM Inductor

4.2 Inductors in IC Circuits

An inductor is a circuit component, which is capable of producing voltage across its terminals in response to a changing current flowing through it. Unlike capacitors, inductors store magnetic energy. As a result of magnetic induction, voltage is generated. Inductors are usually coils of wires, circular or spiral in shape, in which windings are necessary to enhance the flux linkage and hence a large inductance in a small area [56]. Inductors are usually coils of wires, circular or spiral in shape, in which windings are necessary to enhance the flux

linkage and hence a large inductance in a small area. Generally, the wires in a circuit affect the devices in three ways;

- The wire capacitance adds load to the driving circuits
- Signal may be delayed due to wire resistance, capacitance and inductance
- Adds noise due to inductive and capacitive coupling in different wires.

For all frequencies, an ideal passive component must show constant values with constant phase. But all non-ideal components exhibit change in value with frequency. For an inductor, self-resonance frequency is important because beyond this frequency the element becomes capacitive and the quality factor is practically zero [12].

In summary, the advantages of using inductors are follows;

- It provides bias current with no significant dc drop, which improves linearity.
- The emitter degeneration increases linearity without an increase in noise. (Because it doesn't add resistive impedance)
- Parasitic capacitance is resonated out.
- Inductive degeneration can lead to simultaneous noise and power matching. (Especially for LNA)

The inductors are integrated on the top metal layer using a 3-um-thick conductive layer and separated from the silicon substrate by using 2- to 6-um-thick oxide layers. The parasitic capacitances to the substrate are reduced by oxide layers and they allow the integration of large value inductors without having problems with the inductor resonant frequency. But the main problems in the BiCMOS processes are;

- Thickness of the metal line is thin; therefore the sheet resistance is high. For example, the process that we use for our designs is AMS 0.35 SiGe BiCMOS process and the thickness of the last metal layer is typically 2,5 µm. This gives only 15 m-ohm/square sheet resistance. This is high sheet resistance for inductor design and therefore the quality factor are generally limited about 10-12. The sheet resistance of the conductive metal is only related to the quality factor of the inductor.

- The other problem is the coupling capacitance between coil and the substrate. Because the k value of the material between the coil and substrate is not small enough, the capacitance between them is not too small. Generally the oxide layer is about 6 to 10 μm between the substrate and the last metal layer. This parasitic capacitance resonates with the inductance of the coil and determines the self-resonance frequency of the coil. In AMS process, the self-resonance frequencies of the inductors are about 6-8 GHz, which is very low for high frequency applications.

Micromachined inductors will therefore be used for high-Q applications (Q>30) in low noise oscillators, high-gain amplifiers, on-chip matching networks, and integrated LC filters. Currently, thick metal layer and substrate etching are additional fabrication processes and increased cost.

For planar inductors, the parasitic capacitance between the inductor and the ground plane is a problem. These parasitics lower the Q of the inductors and create a self-resonance frequency that limits the maximum frequency of operation, making the devices insufficient for communication applications. The measured unloaded Q of inductors on high resistive silicon (3000-7000 ohm cm) shows that the Q's are comparable to those fabricated on GaAs and quartz. Also the silicon-on-sapphire (SOS) technology can provide inductors with high self-resonant frequencies and good quality factors.

High Q inductors are based on four different technologies depending on the frequency range:

- Thick metal electroplating to reduce the inductor series resistance (Generally used at 0.2-6 GHz).

- Three-dimensional solenoid-type inductors to result in large-value designs suitable for 0.2-6 GHz.

- Substrate etching underneath the inductor to reduce the parasitic capacitance to the substrate (Generally used for 1-100 GHz).

- Self-assembly of the inductor away from the substrate to reduce the parasitic capacitance to the substrate (Generally used for 1-100 GHz).

4.3 Theory of the Planar Type Spiral Inductors

4.3.1 Inductor Model

A general model of a spiral inductor is shown in Figure 4-3. L_s is the low frequency inductance, R_s is the series resistance of the coil, C_s is the capacitance between the different windings of the inductor and includes the fields in air and in the supporting dielectric layers, C_1 is the capacitance in the oxide (or polyamide) layer between the coil and the silicon substrate, C_p is the capacitance between the coil and the ground through the silicon substrate, and R_p is the eddy current losses in the substrate. This model is the most frequently used small signal model by industry and academic labs because it fits very well with Y and S-parameter measurements of planar inductors.

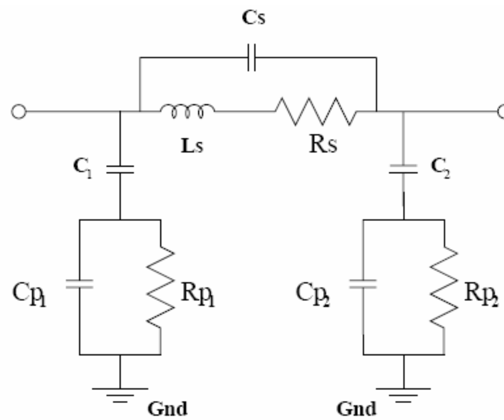

Figure 4-3: Spiral Inductor Model

4.3.2 Inductance of Spiral Inductors

For calculating the inductance of square spiral inductors as the one in Figure 4-4, we can use the expression;

$$L = 2.34\mu_0 \frac{N^2 d_{avg}}{1 + 2.75\psi} \quad \textbf{(4-1)}$$

where N is the number of turns and μ_0 is the permeability of free space, d_{avg} is given by

$$d_{avg} = \frac{1}{2}\left(D_{out} + D_{in}\right) \quad \textbf{(4-2)}$$

and ψ is given by

$$\psi = \frac{(D_{out} - D_{in})}{(D_{out} + D_{in})} \qquad \textbf{(4-3)}$$

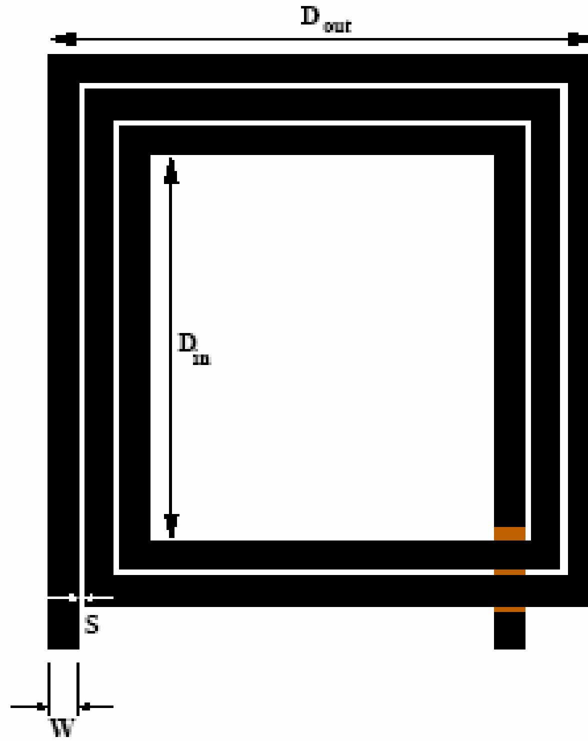

Figure 4-4: A Square Spiral Inductor

4.3.3 Frequency Response of Planar Inductors

The low frequency value of planar inductors is generally obtained by using Greenhouse formulas but an accurate equivalent model of a planar inductor can be obtained using a full-wave electromagnetic simulator such as ADS-Momentum, ASITIC or other EM programs. The simulated S parameters are typically converted to Z or Y parameters and then fitted to obtain accurate values for L_s, C_s, C_p and R_s. In general, Ls and Rs are fitted using low-frequency simulations, while C_p and C_s are fitted around the resonant frequency of the planar inductor. At low frequencies, the impedance of the inductor model is,

$$Z = R_s + jwL_s \qquad \textbf{(4-4)}$$

However, at high frequencies, the capacitances must be taken to account. Generally, R_p can be neglected and C_1 and C_{p1} are lumped together. This means the model can be simplified by ignoring the coupling capacitances of the windings and the capacitance between the coil and the ground through the silicon substrate. This model is also used in the electromagnetic simulation tool "ASITIC" and shown in Figure 4-5 [57].

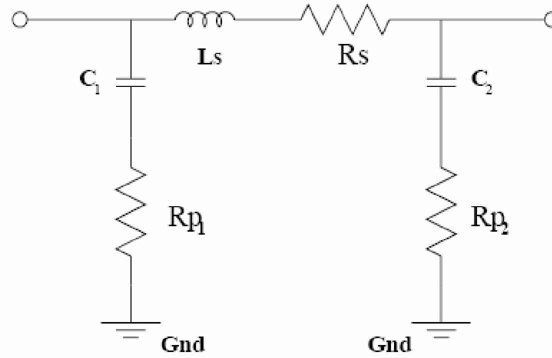

Figure 4-5: Inductor Model used for ASITIC Simulations

We model the desired inductor values for our high-frequency application by using Momentum and ASITIC tool. First we determine the desired inductor and specify the inductance and Q value of the inductor. And then we model the inductor. After modeling, we know the all element values which are shown in Figure 4-5 and then we create a two-port network that defines our inductor.

4.3.4 Q of the Planar Inductors

At low frequencies, and for medium values of Ls resulting in X=jwLs=25 to 70 ohm, the capacitances can be neglected and the model simplifies to a series Ls, Rs circuit. The inductor Q is defined as

$$Q = \frac{energy_stored_in_the_inductor}{energy_lost_in_a_cycle} == -\frac{\mathrm{Im}(Y_{11})}{\mathrm{Re}(Y_{11})} \cong \frac{wL_s}{R_s} \tag{4-5}$$

This definition is not accurate around the resonant frequency of the inductor. The resonance occurs due to the effect of the parasitic capacitances, and it is unavoidable in inductors unless capacitance is reduced to zero.

4.3.5 Effect of the Metallization Thickness

Increasing the conductor thickness since it reduces the series resistance can enhance the Q value of spiral inductors. Series resistance is the most important parameter that reduces the Q value of the inductor below 3 GHz. Even though the thick metallization is a nonstandard IC processing, it could be achieved after the standard IC processing for the rest of the circuit. Above 5-µm thickness of copper, electroplating technique is adequate. It is experimentally observed that enhancing the thickness of the metallization from 4.5 µm to 9 µm and placing

inductors on top of a 10 µm polyimide (or BCB) layer improves the Q factor by 93%, compared with standard inductors fabricated in silicon substrate. it is important to note that in the case of planar inductors, there is an additional resistance that is given by the induced eddy currents within the coil itself .

A reduction in the series resistance greatly increases the Q at low to medium frequencies, but has virtually no effect on the reactance or the resonant frequency of the planar inductor.

4.3.6 Effect of the Parasitic Capacitance

The parasitic capacitance in the substrate is the dominant capacitance for medium to large value inductors, and the inductor resonant frequency is given using the circuit of Figure 4-5.

$$f_r \cong \frac{1}{2\pi\sqrt{L_s C_p}} \quad \textbf{(4-6)}$$

In general, $C_s << C_p$ and can be neglected in the resonant frequency calculations. However, for micromachined inductors with a very low parasitic capacitance and a high resonant frequency, C_s must be taken into account in the circuit model. In this case, the resonant frequency becomes,

$$f_r \cong \frac{1}{2\pi\sqrt{L_s(C_p + C_s)}} \quad \textbf{(4-7)}$$

A reduction in the parasitic capacitance not only makes the resonant frequency higher but also results a large-reactance, high-Q inductor at high frequencies. The reason is that the reactance is proportional to f , while the series resistance is approximately proportional to $\sqrt{f}$.

4.4 Inductor Design

The inductor models can be designed with 3 masks in this project. The important parameters for an inductor are width, thickness, number of turns, outer diameter, inter diameter and air gap thickness. The inductance of the coil is not related with the process. So, the inductance of the coil can be achieved for specified lengths and spacing as:

$$L(nH) = 0.03937 \frac{a^2 n^2}{8a + 11c} \qquad \textbf{(4-8)}$$

Where n: the number of turns,

$$a = \frac{(D_0 + D_i)}{4} \qquad \textbf{(4-9)}$$

$$c = \frac{(D_0 - D_i)}{2} \qquad \textbf{(4-10)}$$

D_0 and D_i are the outer and inner diameters of the rectangular inductor.

For the 30u width, 30u spacing, 500u outer diameter, 200u inner diameter and 3 number of turns;

$$a = \frac{500 + 200}{4} = 175 \qquad \textbf{(4-11)}$$

$$c = \frac{500 - 200}{2} = 150 \qquad \textbf{(4-12)}$$

And the inductance is;

$$L(nH) = 0.03937 \frac{175^2 . 3^2}{8.175 + 11.150} = 3.5578 \qquad \textbf{(4-13)}$$

The inductor mainly consist of the coil part which is spiral, the contacts (in and out ports) and the via part which connects the contact part and the coil. The spiral is 3 turns, 30um in width, has 30um spacing and its outer diameter is 500um. The simulations of the designed inductors are performed using simulators such as Coventor® (MemHenry Module), ASITIC, and Agilent MOMENTUM®. A typical design and simulation procedure using Coventor MemHenry environment is given below:

The coil mask is shown in Figure 4-6.

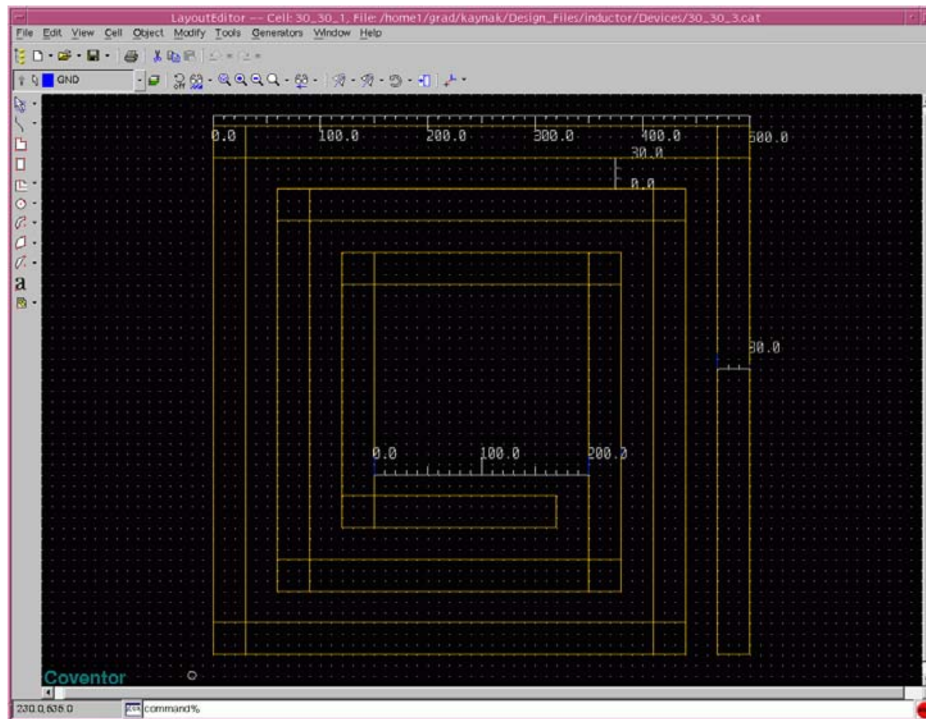

Figure 4-6 Coil of the Inductor

Vias have the size of 30 µm-30 µm. And the contacts have the size of 120 µm -120 µm. This is large because, while measuring the inductor, we need to large contacts. The vias and the contacts are shown in the Figure 4-7 and Figure 4-8.

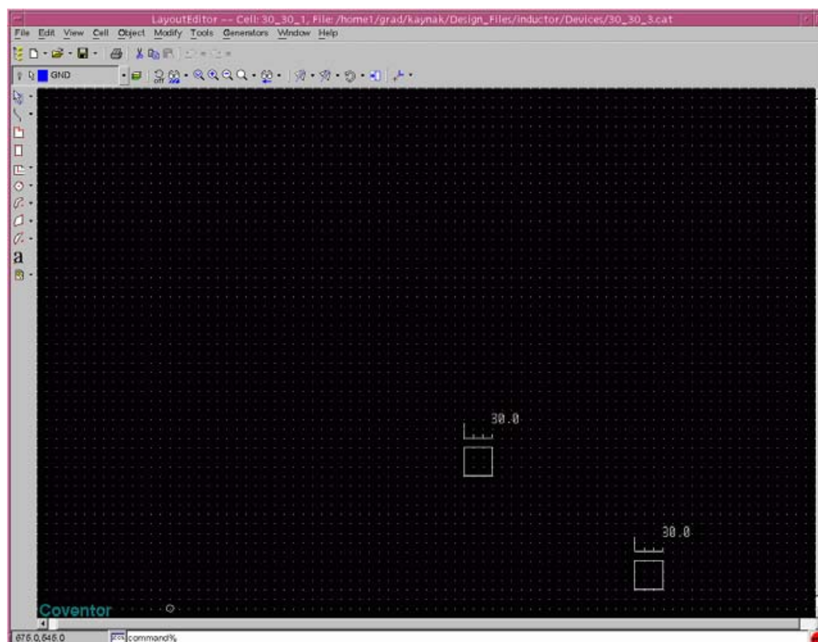

Figure 4-7 Vias of the Inductor

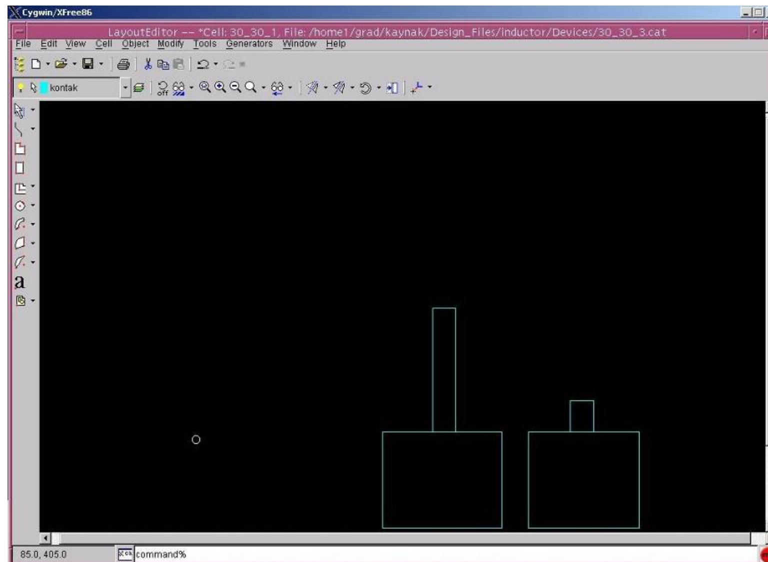

Figure 4-8 Contacts of the Inductor

Inductor fabrication is a 4 layer and 3 mask process. Copper used as the material of inductor for simulation. First a dielectric nitride layer of 0.5 µm thickness is deposited on to the silicon wafer. Then the sacrificial layer PSG of 40 µm thickness is deposited on to the nitride. The contact holes are filled with copper and then it is etched with the contact mask. Then the sacrificial layer of 40 µm thickness is deposited on to the copper contacts and it is etched with via mask negatively to open holes for vias like we did for the contacts. Then copper is deposited on to the sacrificial layer planar type and it is etched with via mask. Then 30 µm thick copper is deposited and it is etched with the coil mask. The process flow is shown in Figure 4-9. Finally we etch the sacrificial layers and get out final structure shown in Figure 4-10.

ProcessEditor: /home1/grad/kaynak/Design_Files/inductor/Devices/inductor_process.proc

File Edit View Help

Step	Action	Type	Layer Name	Material	Thickness	Color	Mask Name/ Polarity	Depth	Offset	Sidewall Angle	Comment
0	Base		Substrate	SILICON	50.0	blue	GND				
1	Depo...	Planar	Layer1	SI3N4	0.5	cyan					
2	Depo...	Planar	Layer2	COPPER	5.0	white					
3	Etch	Front, Last L...				cyan	kontak +	5.0	0.0	0.0	
4	Depo...	Planar	Layer3	BPSG	40.0	orange					
5	Etch	Front, Last L...				white	deep_cop...-	40.0	0.0	0.0	
6	Depo...	Planar	Layer4	COPPER	20.0	cyan					
7	Etch	Front, Last L...				orange	spiral +	20.0	0.0	0.0	
8	Sacrif...			BPSG							

Figure 4-9 Process flow of Inductors

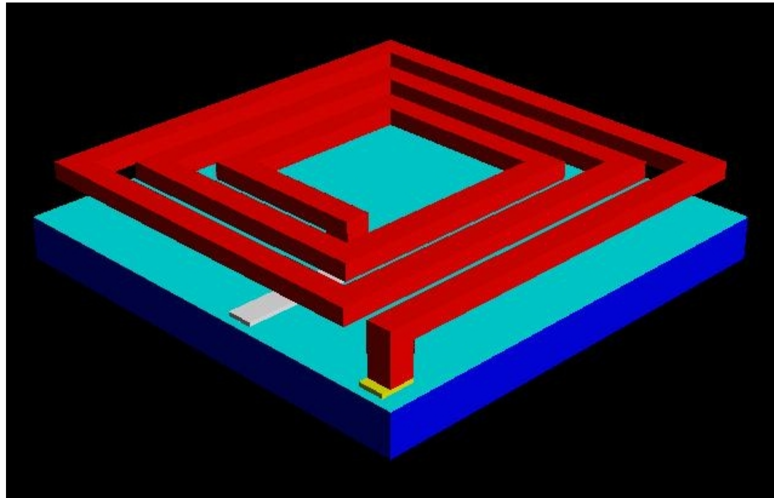

Figure 4-10 Final view of simulated inductors

In order to make analyses first we have to create meshed structure. Meshing is very important for the sensitivity of the simulation. Meshed structure is shown in Figure 4-11.

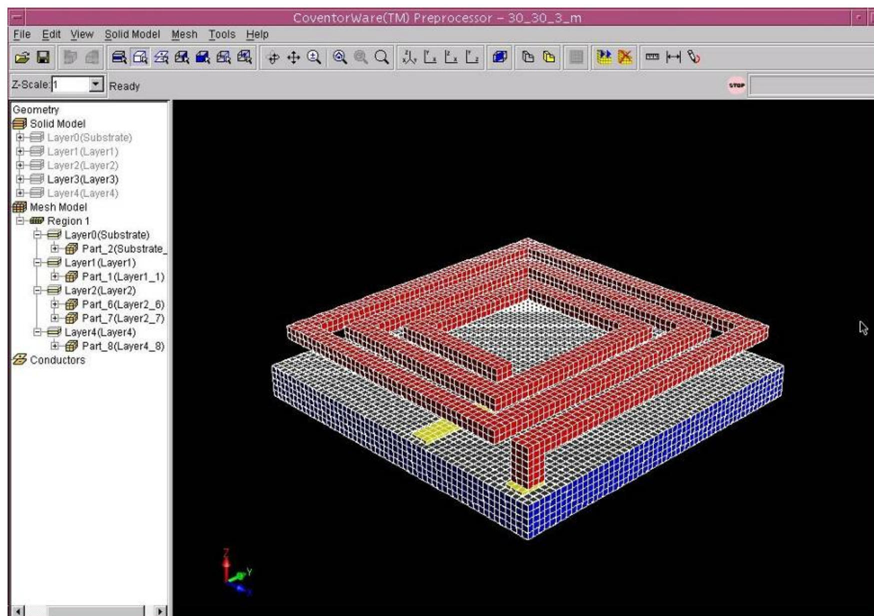

Figure 4-11 Meshed structure of inductor

MemHenry® module is the most suitable simulator for analyzing the inductor. The MemHenry® module computes the frequency-dependent resistance and inductance matrices for the set of conductors. In this project, we can only simulate the inductor at the frequency of 5GHz. There are a lot of different topologies simulated and the inductance-resistance values are listed in Table 4-1. (All of the values are find at the frequency of 5 GHz)

Table 4-1 Inductor Simulation Results

Width of the coil (µm)	Spacing (µm)	Outer Diameter (µm)	Air Gap Thickness (µm)	Thickness of the coil (µm)	Number of turns	L (nH)	R (Ω)	Q
20	10	500	40	20	1	**1.1**	**0.8**	**40**
20	10	500	40	20	2	**3.3**	**2.4**	**42**
20	10	500	40	20	3	**5.8**	**4.6**	**39**
20	10	500	40	20	4	**8.2**	**7.4**	**34**
20	20	500	40	20	1	**1.1**	**0.8**	**41**
20	20	500	40	20	2	**3**	**2.2**	**43**
20	20	500	40	20	3	**5**	**3.9**	**40**
20	20	500	40	20	4	**6.5**	**5.8**	**35**
20	30	500	40	20	1	**1.1**	**0.8**	**41**
20	30	500	40	20	2	**2.8**	**2.0**	**44**
20	30	500	40	20	3	**4.3**	**3.4**	**39**
20	30	500	40	20	4	**5.2**	**4.8**	**34**
30	10	500	40	20	1	**1**	**0.5**	**56**
30	10	500	40	20	2	**2.7**	**1.3**	**63**
30	10	500	40	20	3	**-**	**-**	**-**
30	10	500	40	20	4	**-**	**-**	**-**
30	20	500	40	20	1	**-**	**-**	**-**
30	20	500	40	20	2	**-**	**-**	**-**
30	20	500	40	20	3	**-**	**-**	**-**
30	20	500	40	20	4	**-**	**-**	**-**
30	30	500	40	20	1	**1**	**0.5**	**54**
30	30	500	40	20	2	**2.3**	**1.1**	**65**
30	30	500	40	20	3	**3.3**	**1.6**	**65**
30	30	500	40	20	4	**3.6**	**1.9**	**60**

Table 4-1 includes the inductance values from 1 nH to 8 nH which is the suitable range for IC design. These simulations give an idea of the MEM inductor topologies and the Q values that are elegant for RFIC design.

The most important part of the designing inductors is creating the substrate files for simulators. Coventor defines the material properties and do not need any substrate file. But this is not the case in other simulators like ASITIC or Agilent MOMENTUM®. Prepared substrate file for ASITIC and Agilent MOMENTUM® are given in Appendix XXXXX.

All these simulations are performed under ideal cases but fabricating these inductors is not an easy step. Fabrication description and the problems occurs during fabrication are given in next part of this chapter.

4.5 Fabrication of Suspended Inductors

4.5.1 Fabrication Limitations

The designed and simulated inductors have air gaps of 40 μm and thicknesses of 20 μm however; our fabrication capabilities cannot handle these requirements. Therefore the inductor designs are changed and mainly the new designs are used to optimize the process parameters for future works. In new design, gap spacing of the inductors are limited with the sacrificial layer that are used, which is the AZ 5214 photoresist in our case, which have the thickness of 1.4 μm. Also the coil thickness, which is thought to be 20 μm, is hard to achieve using sputter deposition. Usually these thicknesses are coated using electroplating technique. So the thickness of the coil is taken as 2 μm. Another limiting factor in the process flow is the mask resolution that is the minimum dimensions that can be printed on to mask. The spacing of some inductors such as 10 μm cannot be resolved so they are shorted and look like circular shapes that can be seen in Figure 4-12.

4.5.2 Fabrication Steps of Suspended Inductors

Mainly the process steps of the inductors include four layers and three masks. The process starts with the deposition of Si_3N_4 that is used for insulation. Then copper layer is deposited on to nitride layer and patterned to form the bottom electrodes. Following this step, sacrificial layer, which is AZ5214 photoresist in our case, is coated that directly defines the spacing of the inductor from the ground plate. Then openings for anchors is opened on the sacrificial layer and copper is deposited to fill these openings and in parallel to form the top metal layer. Next step is to pattern the top layer and form the inductor. Finally the sacrificial layer is released and our inductor is created.

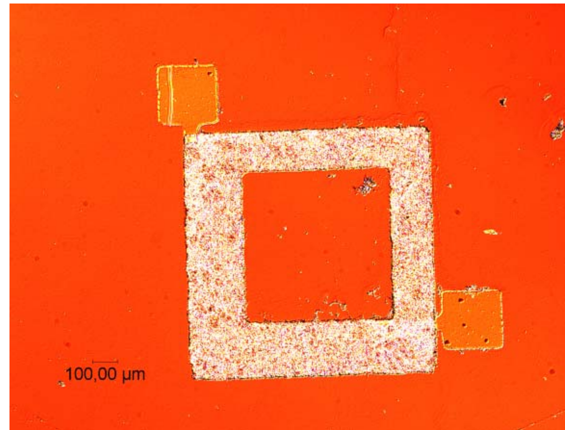

Figure 4-12: Spacing of the inductor coil cannot be resolved

4.5.2.1 Deposition of Nitride:

After the p doped 100 oriented silicon wafer is cleaned with general cleaning recipe 0.3 µm thick Si_3N_4 layer is deposited using RF magnetron sputtering from a high purity Si_3N_4 target. The chamber is heated up to 250 ^oC and then plasma cleaning is applied to Si_3N_4 target with 120 W RF power, 35 sccm argon (Ar) flow and $2x10^{-2}$mbar chamber pressure for 10 minutes. After that deposition step is started with 150 W RF power, 35 sccm Ar flow and $2X10^{-2}$mbar chamber pressure for 60 minutes resulting ~300nm of oxide. The parameters are given in Table 4-2.

Table 4-2: Si_3N_4 RF sputtering parameters

Type	RF magnetron sputtering
Target	Si_3N_4
Temperature	250 ^oC
Cleaning	10min
RF power	150 W
Ar flow	35 sccm
Chamber Pressure	$2x10^{-2}$ mbar (GV5 position 650)
Deposition time	60 min

4.5.2.2 Deposition of Aluminum

The aluminum deposition started directly following the nitride deposition. Al deposition is made by DC magnetron sputtering using high purity Al target. As a first step target cleaning is carried out with 150W DC power, 35 sccm Ar plasma and main chamber pressure of $2x10^{-2}$ mbar for 3 minutes in order to clean the residues on the target which can be affect the

deposition quality. After that the DC power adjusted to 200W and with the same plasma (35 sccm Ar and $2x10^{-2}$ mbar chamber pressure) the deposition is carried out at 150^0C for 20 minutes resulting in 300 nm Al layer. The parameters are given in the Table 4-3

Table 4-3: Al DC sputtering parameters

Type	DC magnetron sputtering
Target	Al
Temperature	150 ^{o}C
Cleaning	3min
DC power	200 W
Ar flow	35 sccm
Chamber Pressure	$2x10^{-2}$ mbar (GV5 position 500)
Deposition time	20 min

4.5.2.3 Patterning and Etching of Aluminum:

Following aluminum deposition, the wafer is taken to wet bench in order to pattern the metal contacts. Shipley's S1813 positive tone photoresist (PR) is used for photolithography step. First the sample is spin coated with PR using spinner. The program is selected as 500 rpm for 5 seconds to spread the PR, then 2000 rpm for 10 seconds and finally 4500 rpm for 45 seconds which results in 1.3µm uniform PR layer. Then 35 sec. of soft bake applied on hot plate with 95^0C temperature. Then the sample is taken to contact aligner and exposed to UV light for 35 seconds using bottom contacts mask. After that step, sample is directly put in the Shipley's MF 319 developer for approximately 45 sec. to remove the photoresist from the parts that is not covered with mask. The develop time is directly related to hard bake and exposure time. Sometimes the duration of the develop time is increased to 1 minute because of the quality of transparency masks such that the light areas of the mask do not passes the light as much as glass masks. This time is optimized for each mask by repeating this step and inspecting it under optic microscope. After we have good patterns the sample is put on the hot plate again for hard baking at 105^oC temperature for 60 seconds. Hard bake step hardens the PR in order to make it unaffected from wet etching. All these parameters are listed in Table 4-4.

Table 4-4: S1813 Photolithography parameters

Spinning	500rpm-5sec./2000rpm-10sec./4500rpm-45sec.
Soft Bake	95°C Hot Plate 35 sec.
Expose	35 sec.
Develop	40-60 sec.
Hard Bake	105°C Hot Plate 60 sec.

Last step in the forming process of bottom electrodes is wet etching of the Al layer that has PR patterns on it. Wet etching is chosen for patterning process because of it is easy and fast process. . Al etchant is selected as 16.H_3PO_4-1.CH_2COOH-1.HNO_3-1.H_2O with an etch rate given as 2600-6600 A^0/min [33]. The wet etching takes about 1 minutes approximately and finally print our mask to the metal layer [33]. Finally the remaining PR is removed with acetone rinse for 2 minutes and isopropanol rinse for 2 minutes. Also 2 min O_2 plasma descum is applied to remove the PR completely. Resulting bottom contact is illustrated in Figure 4-13.

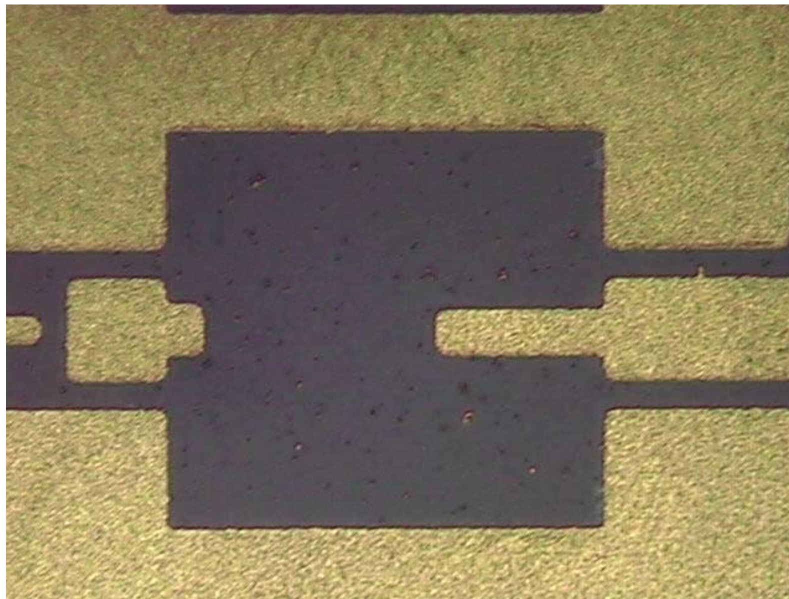

Figure 4-13: Bottom contacts (Al) of the fabricated inductor

4.5.2.4 Coating and Patterning of Sacrificial Layer:

After the electrodes are patterned, dual tone photoresist AZ 5214 is spin deposited in order to form the sacrificial layer. Photoresist is used as sacrificial because it is easy to deposit and made the process simpler and also it is easier to release it than other sacrificial layers. PR is spin coated at 500 rpm for 5 sec., 2000 rpm for 10 sec. and 4500 rpm for 45 sec. resulting in a

thickness of 1.4 μm. Then the sample is soft baked on the hotplate of 95°C for 1 min. Next step is to expose the coated PR under UV light with the anchor opening mask for 20 second. Then the sample is again put onto hot plate at 110 °C for 30 second and once mode the sample is flood exposed with no mask that inverts the mask. Developer step follows this, for 40 sec. with AZ 726 developer. Summary of the AZ5214 negative tone photolithography steps are given in Table 4-5. Resulting structures are shown in Figure 4-14 and Figure 4-15.

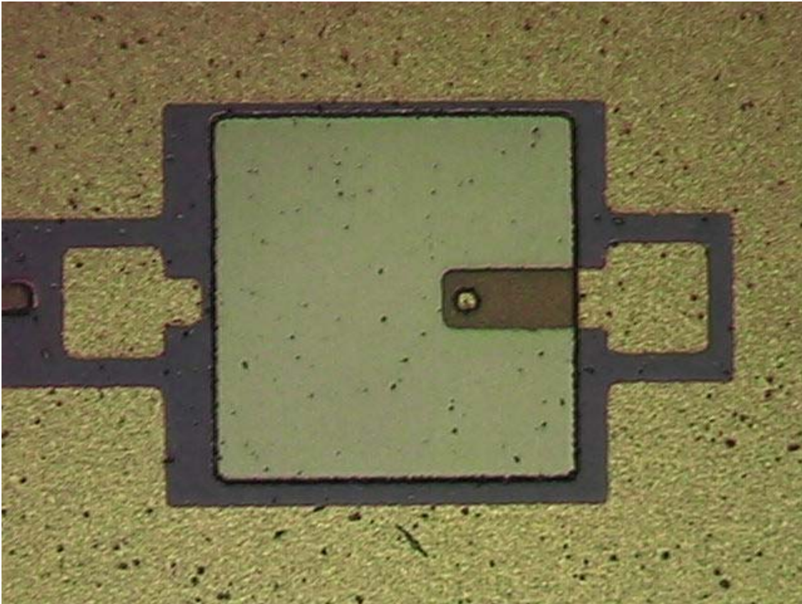

Figure 4-14: Sacrificial layer coated and patterned on bottom electrodes

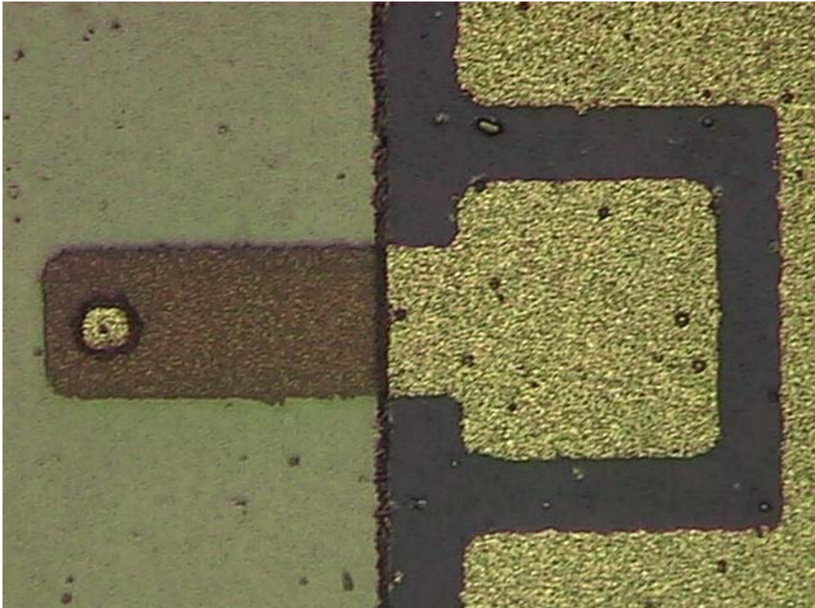

Figure 4-15: Closer view of the via openings in sacrificial layer

Table 4-5: AZ5214 Photolithography parameters

Spinning	500rpm-5sec./2000rpm-10sec./4500rpm-45sec.
Soft Bake	95°C Hot Plate 60 sec.
1st Expose	20 sec.
2nd Bake	110°C Hot Plate 30 sec.
Flood Expose	60 sec.
Develop	40 sec.
Hard Bake	105°C Hot Plate 60 sec.

4.5.2.5 Top Copper Layer Deposition and Patterning:

This top layer deposition of copper is one of the most crucial steps in process flow. The copper layer has to fill the anchor openings and connect well to the coil. This step is repeated for a few times because most of the times when releasing the photoresist sacrificial layer, the top coil part is corrupted. Deposition time finally increase to 60 min resulting in 2.5 μm that fill the anchor openings well as well as the anchor parts stick to the coil part better.

Copper deposition is made by DC magnetron sputtering using high purity Cu target. As a first step target cleaning is carried out with 150W DC power, 35 sccm Ar plasma and main chamber pressure of 2x10^{-2} mbar for 5 minutes in order to clean the residues on the target which can be affect the deposition quality. After that the DC power adjusted to 200W and with the same plasma (35 sccm Ar and 2x10^{-2} mbar chamber pressure) the deposition is carried out below 100^{0}C for 60 minutes resulting in 2.5 μm Cu layer. The temperature is kept low in order not to harden the PR sacrificial layer which will be problem in releasing it. The parameters are given in the Table 4-6.

Table 4-6: Cu DC sputtering parameters

Type	DC magnetron sputtering
Target	Cu
Temperature	<100 ^{o}C
Cleaning	5min
DC power	200 W
Ar flow	35 sccm
Chamber Pressure	2x10^{-2} mbar (GV5 position 500)
Deposition time	60 min

Following that the sample is patterned again using PR with parameters in Table 4-4. The mask is aligned to underlying pattern using contact aligner.

After that the Cu layer is patterned the uncovered parts are removed using the Cu etchant. Cu etchant is selected as 4% HNO_3 (nitric acid) with an etch rate of 40nm/sec. is used to pattern the top metal and the etchant is applied for around 60 second.

4.5.2.6 Releasing of Sacrificial Photoresist

This is one of most crucial part that forms our suspended structure. Acetone is used to release the underlying photoresist sacrificial layer. As seen as an easy step this part is the most problematic part of the inductor fabrication steps. Because the photoresist sticks to copper very well, when rinsed with acetone, in some parts the underlying photoresist are not released. In some parts, acetone removes the photoresist, however; it also removes the top part of the inductors. One other problem is when acetone is exposed to photoresist; it cannot completely remove the photoresist such that some parts stick to coil. There are techniques such as super critical carbon dioxide drying and isotropic dry etching that helps to remove the remaining photoresist. Using dendritic material as a dry-release sacrificial layer to create micro-scale gaps is another solution to this problem. Dentric material is released with no remaining when they are exposed to temperatures like 500 ^{o}C. These are left for future work. There are images of some inductors after photoresist release shown in Figure 4-16, Figure 4-17 and Figure 4-18.

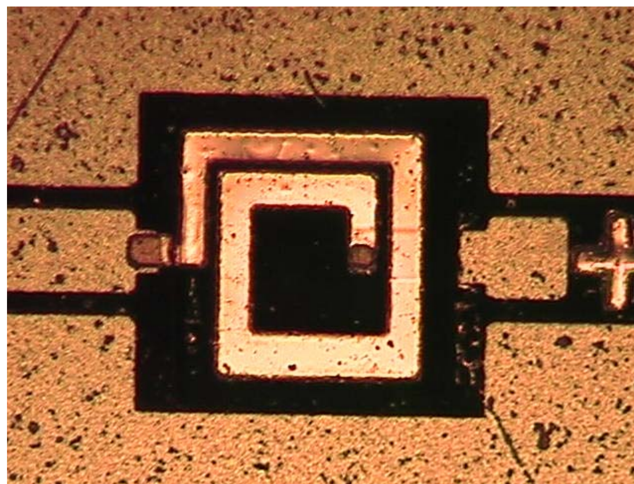

Figure 4-16: Final structure of 1.25 turn square spiral inductor

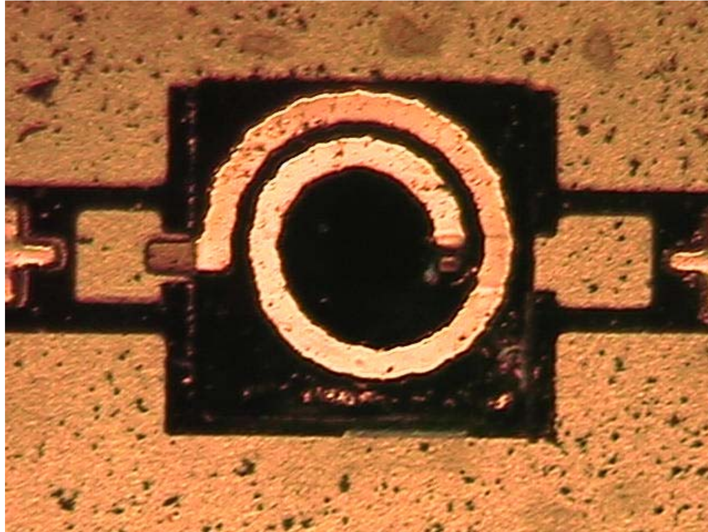

Figure 4-17: Final structure of 1.25 turn spiral inductor

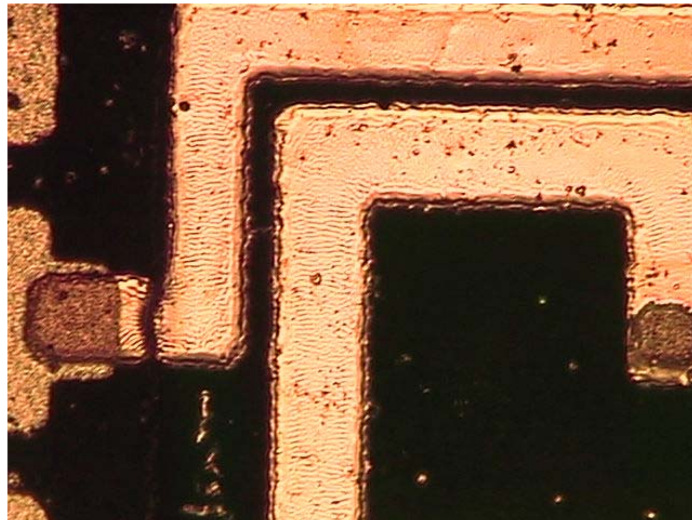

Figure 4-18: Closer view of released 1.25 turn square spiral inductor

4.6 Above-IC Process

4.6.1 Description of the Above-IC Process

The passive components can be built using an IC-compatible process that is called "Above-IC". The main advantage of this fabrication technique is the ability to build the inductors and varactors directly over the electronic circuit. The performance of ordinary coils fabricated using standard IC process is usually poor. The main reason for the degradation of the performance of a coil is the presence of a resistive substrate. Another key issue is the intrinsic

resistance of the coil, mainly determined by the nature of the metal and its cross-section. Thus, the use of a thick metal layer greatly improves the performance of the coil. The process described here allows us to fabricate high-performance passives in a simple deposit and pattern technology, without the need for complex steps. At the same time this optimizes the isolation from the resistive substrate and the coil resistance. The process consists of the following steps:

- Above the normal IC-passivation, a thick low-k dielectric layer is deposited. The passivation layer should have clearances in the locations where the inductor connected to the IC-circuitry.
- The vias needed to contact the underlying metal connections are then patterned. The vias ensure the electrical connection between the last IC metal layer and the passive components.
- A thick electroplated copper layer is realized in order to create the coil.
- In order to protect the coil, a passivation layer can be deposited as the last step.

Below is the process flow of the Above-IC process and Figure 4-19 illustrates this process flow;

a) Starting wafer with the top metal level and the openings in the passivation

b) Deposition of the low-k dielectric

c) Opening of vias to the top metal layer

d) Deposition of the seed metallic layer

e) Deposition and patterning of the thick photo-resist

f) Electro-deposition of the thick coil layer

g) Removal of photo-resist.

h) Removal of the seed metal layer

i) Thick low-k dielectric deposition as the passivation layer or;

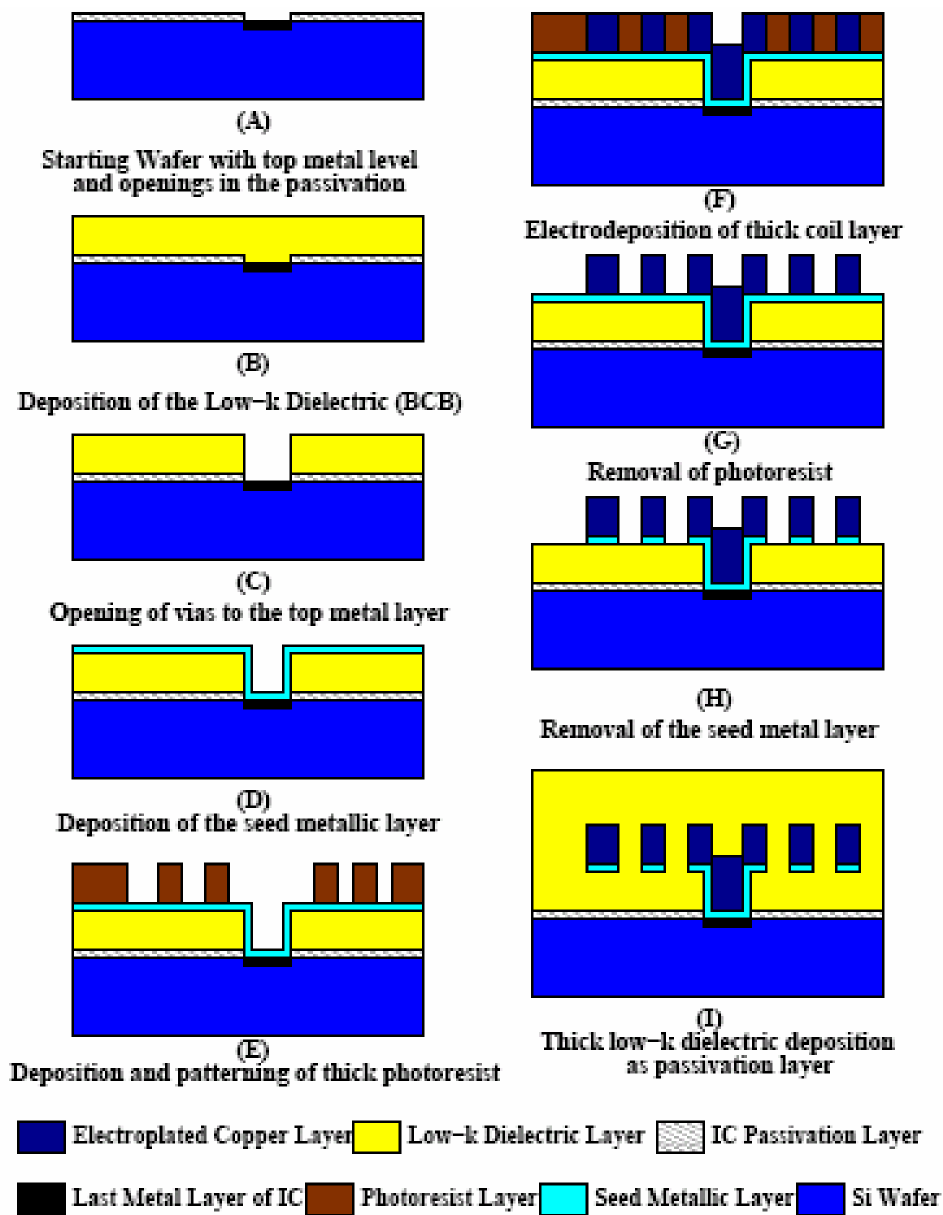

Figure 4-19 Above-IC Process Flow

Above the normal IC-passivation, a thick low-k dielectric layer is deposited. The passivation layer should have clearances in the location where the inductor will be connected to the IC-circuitry. The vias needed to contact the underlying metal connections are then patterned. The vias ensure the electrical connection between the last IC metal layer and the inductor. A thick electroplated copper layer is realized in order to create the coil. In order to protect the coil, a passivation layer can be deposited as the last step. This fabrication flow is carried out below 250 °C, which is suitable for post-IC processing.

4.6.2 Fabrication of Above-IC Inductors

Like MEM inductors, Above-IC type inductors also have high Q values. The thick BCB layer decreases the parasitic capacitance to the substrate. The main reason is low k value of the BCB material. This is the way that to achieve high Q values in inductors. The MEMSCAP process also manufactures inductors by using this method. Decreasing the parasitic capacitive effect is important but another important thing that increase Q value is decreasing the sheet resistance. This is accomplished by using thick copper layer. Thick copper cannot be achieved by using thin film deposition methods like sputtering. The method that used widely for thick copper layer is electroplating method. By using this method, thickness of above 15 μm can be achieved. Also we start to generate the setup of copper electroplating and achieved copper layer thickness above 10 μm by using in house capabilities. Also by using the electroplating method, the quality of the copper is better than the sputtering method. This is directly affects the sheet resistance of the coil. All the thickness values and other parameters can be seen in the Figure 4-20.

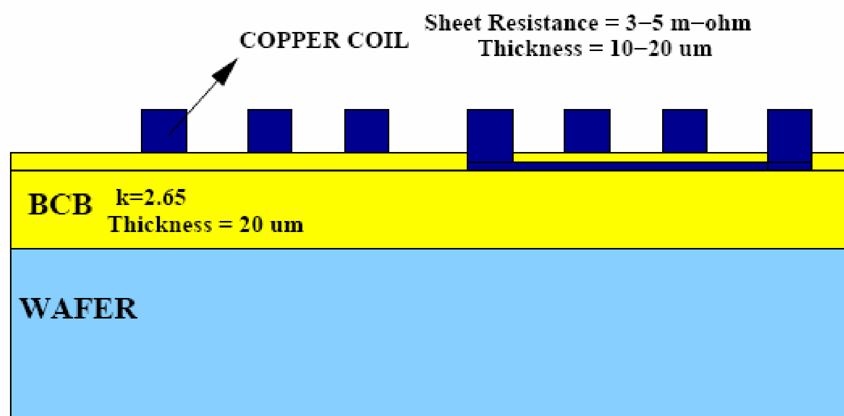

Figure 4-20 Cross-view of Above-IC Process

Micromachined-inductors at different geometries/values (1 – 8nH) designed and simulated using electromagnetic (EM) simulation tools such as ASITIC® and MOMENTUM®. Additionally, full EM simulations of the selected geometries are carried out using HFSS®. BCB (Benzocyclobutene) is chosen in this work as the passivation layer because it allows thick layers (13.8μm at 1000rpm) and low-k value of 2.65. Different spiral inductor types with different turns ranging from 0.5 to 3 and with 3μm thickness were fabricated over 10 μm BCB layer. Figure 4-21 shows the cross-section of one of the fabricated inductors. Figure 4-22 and Figure 4-23 shows the fabricated inductors, designed for 1-nH and 1.58-nH,

respectively. These values are suitable for the integration of fabricated LNA which improves the noise performance of the LNA. Next part includes the approach for integration of the RFMEMS inductor with fabricated SiGe BiCMOS LNA.

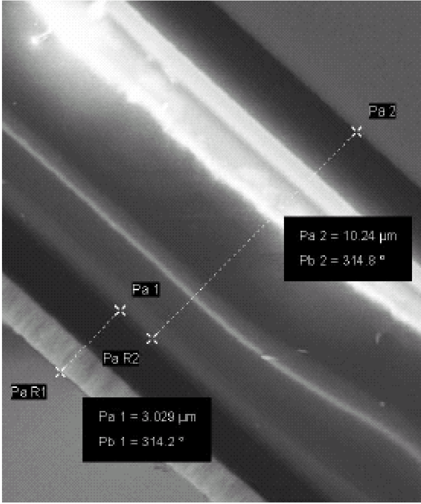

Figure 4-21 Cross-Section of the fabricated inductor above the BCB layer

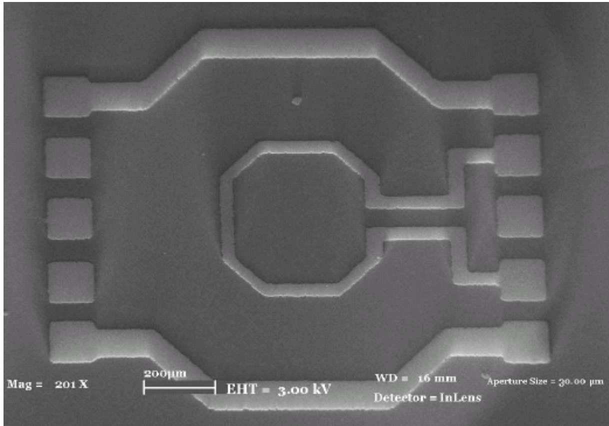

Figure 4-22 Fabricated 1 nH inductor

4.7 Measurement of MEM Inductors

The last step of our work is measuring the fabricated inductor values. For this measurement we must consider the Z parameters of these inductors. A typical set of test structures for measuring an inductor in a pad frame is shown in Figure 4-24.

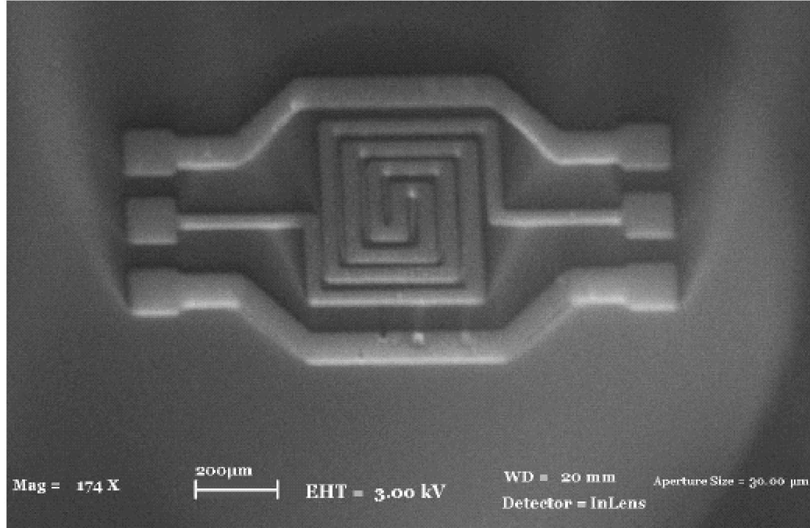

Figure 4-23 Fabricated 1.58 nH inductor

High-frequency ground-signal-ground probes will be landed on these pads so that the S parameters of the structure can be measured. However, while measuring the inductor, the pads themselves will also be measured, and therefore two additional de-embedding structures will be required. Once the S parameters have been measured for all three structures, a simple calculation can be performed to remove the unwanted parasitics. The dummy open and dummy short are used to account for parallel and series parasitic effects, respectively. The first step is to measure the three structures, the device as $Y_{DUT,}$ the dummy open as $Y_{dummy\text{-}open}$, and the dummy short as $Y_{dummy\text{-}short.}$ Then the parallel parasitic effects represented by $Y_{dummy\text{-}open}$ are removed, leaving the partially corrected device admittance as Y'_{DUT} and corrected value for the dummy short as $Y'_{dummy\text{-}short}$.

$$Y'_{DUT} = Y_{DUT} - Y_{dummy\text{-}open}$$

$$Y'_{dummy\text{-}short} = Y_{dummy\text{-}short} - Y_{dummy\text{-}open}$$

The final step for measuring the inductor is to subtract the series parasitics by making use of the dummy short. Once this is done, this leaves only Z_{device}, the device itself.

$$Z_{device} = Z'_{DUT} - Z'_{dummy\text{-}short}$$

Where Z'_{DUT} is equal to $1/ Y'_{DUT}$ and $Z'_{dummy\text{-}short}$ is equal to $1/ Y'_{dummy\text{-}short}$.

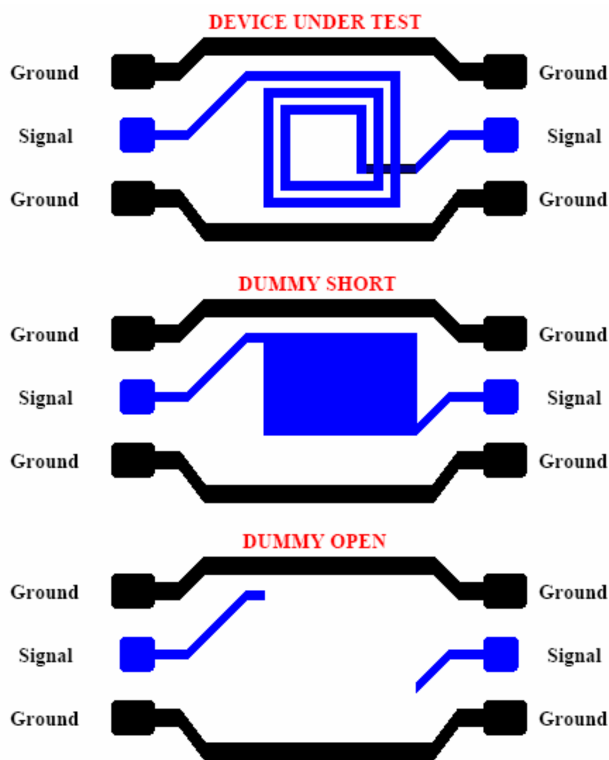

Figure 4-24 Test structures for measuring the inductor

The fabricated suspended inductors are measured using Karl-Zuss PM5 probe station as described above. Inductance values of the fabricated test inductors are around 1nH and their quality factors are calculated from s-parameter results and depicted in Figure 4-25.

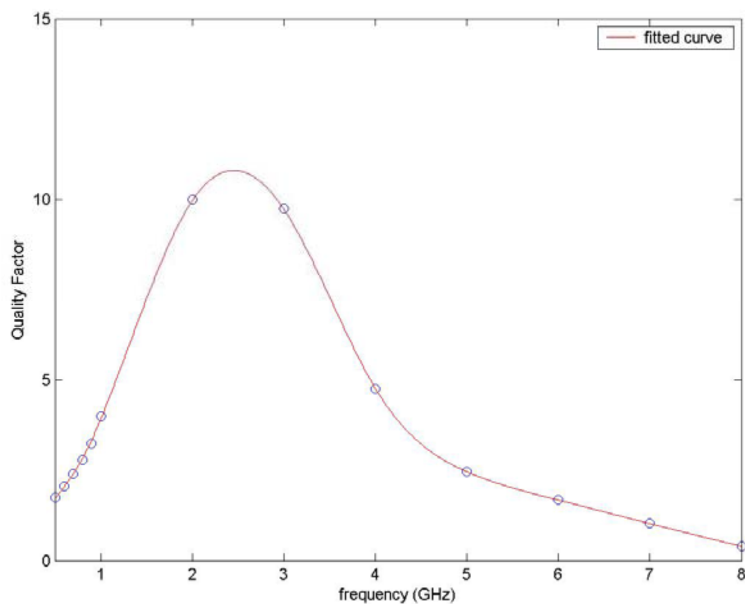

Figure 4-25: Q vs frequency measurement results of fabricated suspended inductors

The quality factors of the fabricated suspended inductors are very low as expected due to fabrication limitations. They give a peak quality factor of 11 between 2-3 GHz. These low Q values are due to the substrate coupling of the coil because the suspension height is very low as 1.4μm as a result of using photoresist as sacrificial layer. Also thickness of the coil was not sufficient to have higher quality factors.

4.8 Performance Improvement of High-Q RFMEMS Inductors: LNA Example

The receiver block mainly specifies the sensitivity of the overall transceiver architecture, whose major block is the LNA, specifying overall NF. In low noise applications, most common topology is the cascode-connected, common-emitter LNA with inductive emitter degeneration, shown in Figure 4-26 and fabricated using 0.35 μm SiGe-BiCMOS process.

Based on the analysis that we have performed on this circuit shows the noise generate by L_1 affects the noise figure performance of the circuit up to %20. This effect is simulated for quality factors, ranging from 5 to 100, and plotted in Figure 4-27. It is illustrated that quality factors higher than 30 improve the NF of the LNA from 2.8dB to 1.8dB. All the noise contributors to the NF of the circuit are shown in Tab. 1. For an example, addition of series resistance of L_b, increases the noise figure from 2.1 dB to 2.8 dB.

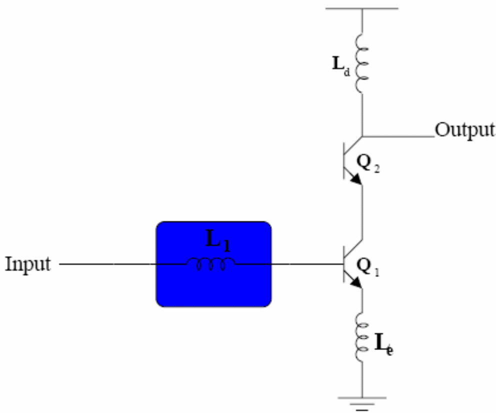

Figure 4-26 Inductive degenerated cascode LNA

The fabricated RF MEMS inductors will be integrated to the LNA test structure which is shown in Figure 4-28. In this test structure, the LNA was fabricated without the L_1 inductor and this inductor will be formed using RFMEMS inductors via bond-wire integration. Also,

the post processing of the test structures will be performed using Above-IC process and will also be mentioned in future work part.

Table 4-7 Noise Contributors

Source of the Noise	Contribution to Overall NF (%)
RF Port (R_S)	48
Transistors	28
Parasitic components of L_b	21
Others	3

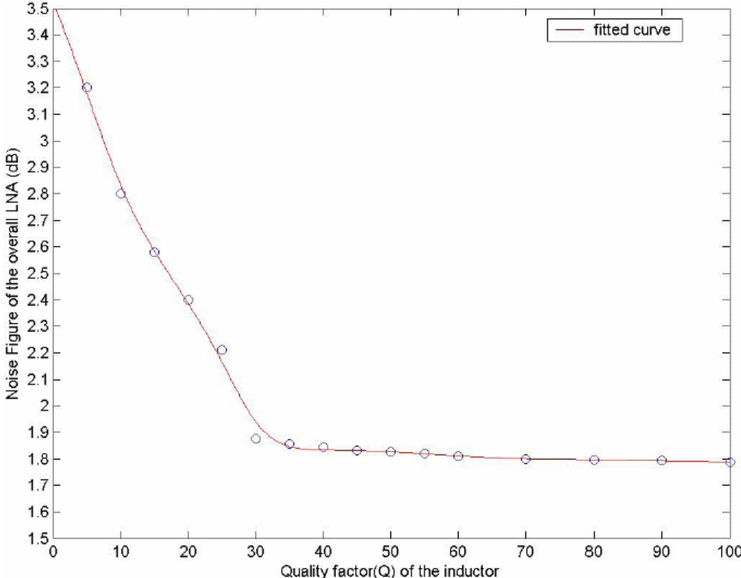

Figure 4-27 NF of the LNA for different Qs of L_1

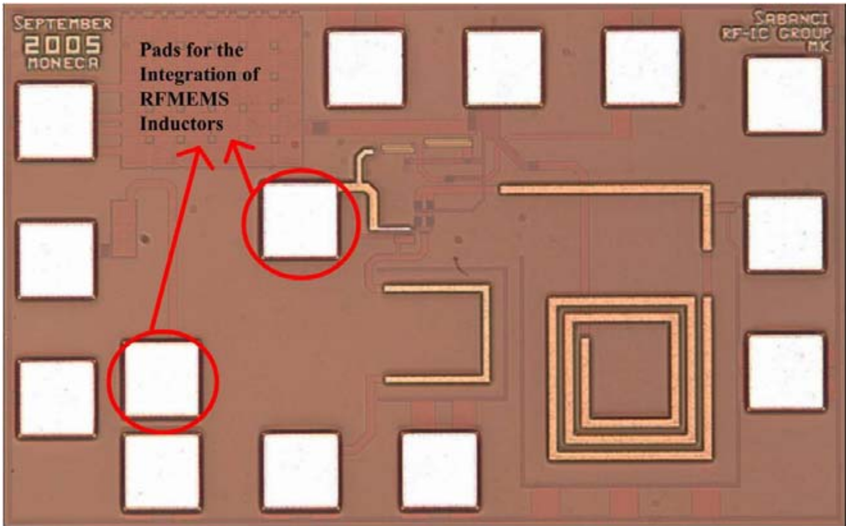

Figure 4-28 Test structures for RFMEMS inductor Integration

4.9 Conclusion & Future Works

This chapter gives the basics of High Q MEMS Inductors and also defines the recently adopted Above-IC process technology. The important steps in the inductor design are given and also detailed information about the designed inductors given.

Large range of inductors, inductance values form 1.1 to 6.5 and quality factors about 20-40 are being designed and simulated. These inductors are aimed to be integrated in to RF Blocks to improve their performance parameters. An LNA example is given in which an high Q inductor (Q=30) in the input matching stage improves the noise figure from 2.8dB to 1.8dB.

Above IC process is studied and some test structures are created which is a first step in the way of post processing. Yet, there are some issues need to be overcome such as filling the deep via holes in dielectric and deposition of thick metal layers. Sputter deposition is not sufficient for the mentioned applications. We have started to use electroplating and trying to optimize the parameters. However, this is left for future work.

Additionally fabrication steps of a suspending MEMS inductor is given in detail. Each step of this process is optimized and finally suspending inductors are structured. However this suspended inductors are different from designed and simulated ones due to the fabrication limitations. . Inductance values of the fabricated test inductors are around 1nH. They give peak quality factor of 11 between 2-3 GHz. These low Q values are due to the substrate coupling of the coil because the suspension height is very low as 1.4µm as a result of using photoresist as sacrificial layer. Also thickness of the coil was not sufficient to have higher quality factors. Improving the fabrication process of these inductors and in parallel their performances as designed is left for future work.

5

Chapter 5
MEMS Resonators

5.1 Introduction

Today's wireless transceivers are designed to minimize or eliminate the off-chip passives to decrease cost and size. Specifically, the ceramic filters, SAW filters, and lately FBAR filters capable of achieving high quality factors needed for RF and IF bandpass filtering are all off-chip components that must interface with IC blocks at the board level which consumed high portion of the chip, increase interconnects that cause parasitic losses and increase the cost. Vibrating micromechanical filters are emerging as attractive candidates for on-chip versions of these high Q mechanical passive components because of their tiny sizes, zero dc power consumption and their IC compatible fabrication techniques. Possible RF MEMS replacements with their off-chip counterparts are shown in Figure 5-1.

The idea of filtering analog signals was first introduced almost one hundred years ago, and has seen tremendous development since then. The majority of filters have been electrical circuitry but there has been a great deal of interest in electromechanical filters in which electrical signal is converted to mechanical signal and passed through a vibrating mechanical system, and then transduced back into electrical energy at the output.

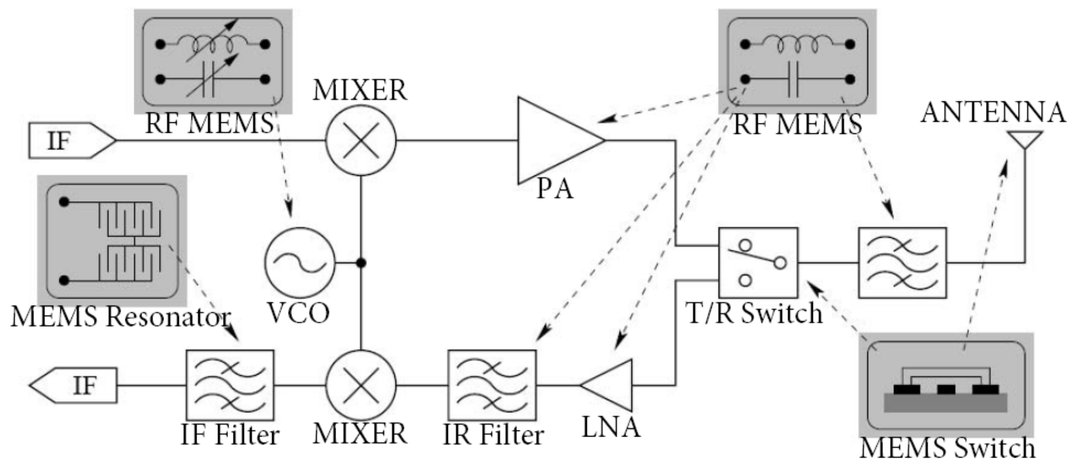

Figure 5-1: Possible RF MEMS replacements with their off-chip counterparts

In electrical filters, resonators are typically inductor-capacitor pairs, while in mechanical filters they are spring-mass systems. Mechanical filters utilize mechanical resonances to accomplish the filtering of electrical signals. They are attractive because of their high selectivity (Q's up to thousands) and high stability. In either type of filter, electrical or electromechanical, the key component is the resonator. In early filters, steel plates were used as the resonators, and wires were used as the mechanical coupling elements [58]. With the development of IC technology and micromachining techniques, there has been an extensive research to develop micro-scale mechanical filters. The idea behind utilizing silicon is its near-perfect mechanical properties. Micromachined resonators with high quality factors are proposed for low-noise oscillators and highly selective filters for communication systems. Because of their small sizes and near-zero dc power consumption, many of the micromechanical filters can be fabricated on to a smaller area. So, rather than using a single macroscopic filter to select one of many channels, a parallel bank of micromechanical filters can be utilized so that switching between frequencies can be achieved [59].

There are generally two approaches to micro-resonators: electric field (voltage-controlled) driven MEMS resonators and piezoelectric MEMS resonators. Electric field driven filters are related to surface micromachining processes. The appealing feature of this approach is its ability to control resonant frequency with changing dc bias which allows designing a tunable filter. Filters according to this principle have been proposed with frequencies up to 200 MHz [60]. For use in telecommunication systems, higher frequencies must be achieved. Piezoelectric MEMS resonators, in which a standing wave is generated within the piezolayer itself, are suitable for GHz range applications. The resonant frequency is determined by the

thickness of piezoelectric layer. The advantages of piezoelectric resonators over the typical voltage-controlled resonators are the exhibition of low-impedance values at high frequencies, good power handling capability and easy packaging (no need for vacuum cavity). An acoustic piezoelectric MEMS resonator is reported with high-Q and low-impedance in the 700 MHz-1.2 GHZ range [61].

The problem with voltage-driven MEMS resonators is the exhibition of high-impedance values at GHz frequency ranges. High impedance levels prohibit VC resonators to transmit no more than mw range power which is not suitable for antenna applications. Moreover, to preverse high-Q values of resonators, air-damping factor must be prevented, which means that hermetic packaging is necessary. Today's research on this type of resonators includes achieving higher frequencies, while preserving the peculiar high selectivity. In order to operate at GHz frequency range, device dimensions must shrink considerably. However, as the geometric dimensions approach the acoustic wavelength, a large number of acoustic modes will exist and cause problems [55].

Piezoelectic MEMS resonators overcome this problem and bring the advantage of operating at high frequencies with high Q's and with low-impedances. The challenges in manufacturing this type of devices are:

• It is hard to deposit good quality piezolayers.

• Since resonant frequency is defined the layer thicknesses, very low thickness tolerances must be met.

Consequently, merging of CMOS process with micromachining has been achieved. It is now possible to build high performance single-chip communication systems. On the other hand, there are still research going on to fully integrate RF MEMS devices with electronics interface and to raise MEMS resonators' operating frequency up to RF range while keeping the high selectivity by using different materials (such as SiC) with unique characteristics.

Large companies which are spending more on R&D in the area are looking to overcome the technical challenges, especially those associated with the high cost of production for RF MEMS, namely packaging. Some researchers are actively looking to develop innovative bonding processes that can be used for packaging of RF MEMS devices.

5.2 Design of RF MEMS Free-Free Beam Resonator

MEMS based resonator filters are designed with the purpose of replacing the crystal or SAW intermediate frequency (IF) filter blocks that take place in the transceiver that is in compliant with IEEE 802.11a communication standard. Free-free beam type resonator structures are selected for IF filter design because they achieve higher frequencies than high Q lateral resonators and clamped-clamped beam resonators, and more IC compatible than high Q and frequency disk resonators. The Free-Free Beam Resonator, which can be fabricated, using surface micromachining, has the advantage of utilizing higher-mode operation, which leads to frequency increase without reducing the size of the beam. Design parameters and different operating modes of free-free beam resonators are studied to design compact devices that achieve selected frequencies.

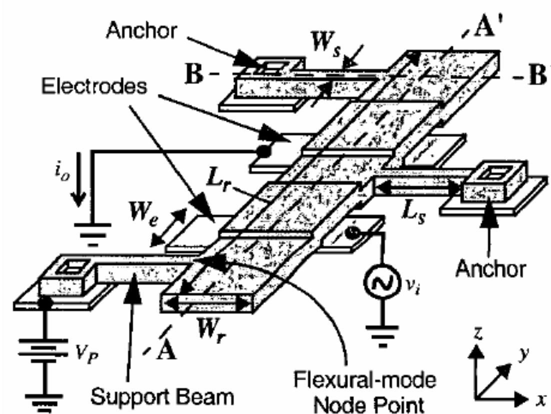

Figure 5-2: 2nd Mode Free-Free Beam [62]

An example of a free-free beam is shown in Figure 5-2. It consist of a single vibrating beam that is suspended over the electrodes and supported by smaller beams attached at precise nodal locations that is to achieve free vibration to decrease the loss of the resonator. The working principle of the resonator is as follows. A DC-bias voltage V_P applied to the resonator structure and an AC drive voltage is applied to one of the electrodes. These voltages create a time varying electrostatic excitation force between beam and electrodes and when AC frequency matches the natural frequency of the beam, it began to vibrate. This results an output current i_o that is generated by the action of V_P across the time-varying (at resonance) electrode-to-resonator capacitor C(z,t) as ($i_o=V_P(\partial C/\partial t)$). The vibration of the beam occurs along the z axis and it is stated in [62] that the resonator exhibits higher Qs in the second

mode vibration where the gap among electrodes changes in opposite directions as shown in Figure 5-3.

The design procedure for the resonator is stated as follows:

1. Resonator Beam Design
2. Support Beams Design
3. Proper Electrode and Support Placement

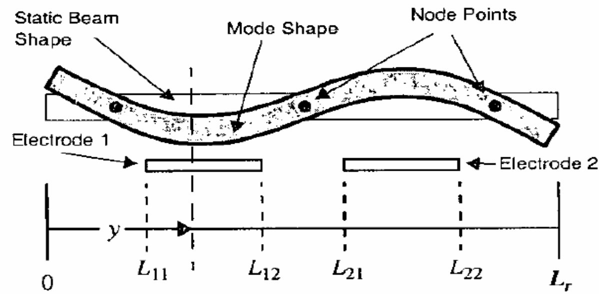

Figure 5-3: Second-mode vibration

5.2.1 Resonator Beam Design

The geometrical dimensions of the beam (L_r, W_r, h) and its material properties determine the resonant frequency. The frequency of the 2nd vibration mode under zero bias is determined using the Euler-Bernoulli formula given below:

$$f_{nom} = \frac{(\beta_n L_r)^2 h}{4\pi\sqrt{3}L_r^2}\sqrt{\frac{E}{\rho}} \qquad \textbf{(5-1)}$$

where E and ρ are young's modulus and density for the beam material and β_n is the mode coefficient given by the nth root of equation;

$$\cos(\beta_n L_r)\cosh(\beta_n L_r) = 1 \qquad \textbf{(5-2)}$$

and for the first three modes β1Lr, β2Lr and β3Lr are 4.73, 7.853 and 10.996 respectively [62].

It is stated that this formula is accurate resonators with large L_r-to-W_r and L_r-to-h ratios. Hence, for higher frequencies where L_r gets smaller, the theory overestimates the actual frequency up to 10 percent and Timoshenko equations should be utilized. For antimetric modes (i.e., even numbered mode, such as the second or the fourth mode) the Timoshenko equation for frequency is;

$$\tan\frac{\beta}{2} - \frac{\alpha}{\beta}\left(\frac{\beta^2 - g^2}{\alpha^2 + g^2}\right)\tanh\frac{\alpha}{2} = 0 \qquad \textbf{(5-3)}$$

where

$$g^2 = (2\pi f_0)^2 L_r^2 \frac{\rho}{E} \qquad \textbf{(5-4)}$$

$$\left.\alpha^2, \beta^2\right\rangle = \frac{g^2}{2}\left[\mp\left(1 + \frac{E}{\kappa G}\right) + \sqrt{\left(1 + \frac{E}{\kappa G}\right)^2 + \frac{4L_r^2 h W_r}{g^2 I_r}}\right] \qquad \textbf{(5-5)}$$

$$G = \frac{E}{2(1+v)} \quad and \quad I_r = \frac{W_r h^3}{12} \qquad \textbf{(5-6)}$$

where G and v are the shear modulus of elasticity and Poisson's ratio, respectively, of the structural material, Ir is the bending moment of inertia, and κ is the shear-deflection coefficient. For a rectangular cross-section, κ is 2/3 [62].

The calculation of the resonance frequency as a function of DC bias is more bulky. It starts with the DC-bias-derived electrical stiffness given below:

$$f_0 = f_{nom}\left[1 - \left\langle\frac{k_e}{k_m}\right\rangle\right]^{\frac{1}{2}} \qquad \textbf{(5-7)}$$

where $\langle k_e/k_m \rangle$ is a parameter representing the effective electrical-to-mechanical stiffness ratio integrated over the electrodes:

$$\left\langle\frac{k_e}{k_m}\right\rangle = \sum_{i=1}^{Ne}\int_{Li1}^{Li2}\frac{V_P{}^2.\varepsilon_0.W_r}{d.k_m(y)}dy \qquad \textbf{(5-8)}$$

where $k_m(y)$ is the mechanical stiffness as a function of beam y axis (A to A') and found as below:

$$k_m(y) = \left[2\pi fnom\right]^2 m_r(y) \quad \textbf{(5-9)}$$

where $m_r(y)$ is the equivalent mass at location y. The N_e in 5-8 denotes number of electrodes where the integral is taken for both electrodes. Li_1 and Li_2 is the start and end points of ith electrode. The $m_r(y)$ is given below:

$$m_r(y) = \frac{p.W_r.h.\int_0^{Lr} Z_{mode}(y')dy'}{\left[Z_{mode}(y)\right]^2} \quad \textbf{(5-10)}$$

where the $Z_{mode}(y)$ is the z-directed displacement at location y and for the nth mode vibration given as; [62]

$$Z_{mode}(y) = \cosh\beta_n y + \cos\beta_n y - \xi(\sinh\beta_n y + \sin\beta_n y) \quad \textbf{(5-11)}$$

where

$$\xi = \frac{\cosh\beta_n L_r - \cos\beta_n L_r}{\sinh\beta_n L_r - \sin\beta_n L_r} \quad \textbf{(5-12)}$$

5.2.2 Support Beams Design

The primary consideration in the design of support beams is the quality factor which depends on the loss to anchors and substrate. To minimize the losses due to torsional motion, the support beam lengths are designed to correspond to a quarter wavelength of the operating frequency such that the beam sees anchors at zero impedance meaning no supports. This condition is met by the formula below [63]:

$$L_S = \left[\frac{1}{4f_0}\sqrt{\frac{G.\gamma}{p.J_S}}\right]^{\frac{1}{2}} \quad \textbf{(5-13)}$$

where J_S is the polar moment of inertia given by:

$$J_S = \frac{h^2 + W_S{}^2}{12} \quad \textbf{(5-14)}$$

and γ is the torsional constant given by:

$$\gamma = 0.214.h.W_S^{\ 3} \quad \textbf{(5-15)}$$

5.2.3 Electrode Design and Placement

The placement of the electrodes is dictated by the excitation of correct mode of a free-free beam resonator such that they should be placed in the center of each node pair. For the second mode the beam locations move in opposite directions such that the input and output signals become in phase and also this maximizes the Q value

5.2.4 Design Considerations, Calculations and Simulations

The crucial points that directly affect the resonator performance are the beam thickness, beam length, and the node points. The main cause of the resonators to give low quality factors is the couplings of resonator vibrations through its supports to its anchors and finally to substrate. To get rid of these losses due to translational motion of the beam, torsional-mode beams are attached to the node points where ideally no translational motion occurs. Also the electrodes are placed between these node points. To select the node points on the beam, displacement versus location on the beams graphs are plotted using the appropriate equations in the MATLAB software as seen in Figure 5-4.

In Figure 5-4 we can see displacement curves for 1st, 2nd and 3rd mode beams. The node points are attached to the intersection points of the curves with x axis where ideally no vertical motion occurs. Therefore for different beam lengths and operating modes this graph has to be plotted and the node points must be calculated to decrease the losses and increase the quality factor of the resonator.

Also losses from torsional motion are strategically prevented by using support beam lengths corresponding to quarter wavelength of the operating frequency. These quarter wave supports effectively transforms the infinite acoustic impedance seen at the anchors to zero impedance at the resonator attachment points.

Another important parameter is the beam length, which directly affects the resonance frequency of the resonator. As the dimensions the beam increases, the mass of the beam increase, which decrease the resonant frequency. This can also be seen if we plot the beam length versus frequency graphs using Timoshenko equations again in MATLAB software. The other dimensions kept fixed and beam length is taken as variable, finally the graph in Figure 5-5 is acquired. As it can be seen from the graph beam length is inversely proportional

with the resonant frequency. Additionally, this graph shows us that higher operating modes give us higher resonant frequencies.

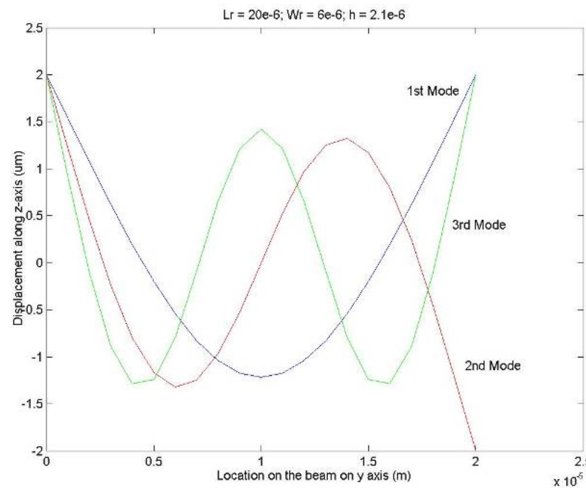

Figure 5-4: Displacement along z-axis versus location on the beam on y-axis for free-free beam resonators operating in the fundamental, second and third modes.

Beam thickness is another parameter that is related with resonant frequency. As seen in the Figure 5-6, for the given thickness range, the value of the resonant frequency increases with increasing beam thickness. It should be kept in mind that the increasing behavior of the resonant frequency value with increased beam thickness is only true for the given thickness range, and should not be generalized. For the given range, the value increases, since an increase in h also causes an increase in the k (spring constant) value of the beam, and hence causes an increase in f_0 value. However, if the thickness was further increased, the mass of the beam would become more effective in the system and the value of f_0 would reach saturation.

Using the plot and the above methodology, the beam thickness of the final design is decided to be set as 2μm.

Understanding the dimensions effects on resonator parameters, next step was to investigate the operating modes. In this part three different free-free beam resonators were designed that operate at first, second and third mode respectively. The designs and their vibrating shapes are shown in Figure 5-7. First mode beam has four supporting beams attached to two node points, second mode beam has three supporting beams attached to three node points and finally third mode beams has 4 supporting beams each attached to a different node points. Thicknesses of beams are taken as 2μm and widths are taken as 6 μm. All of the designs are made in the COVENTOR software and modal analysis applied to them.

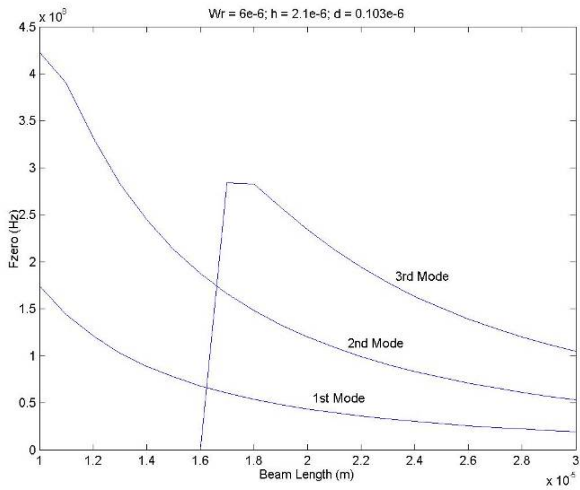

Figure 5-5: Frequency versus beam thickness plot for free-free beam resonators operating in the fundamental, second and third modes.

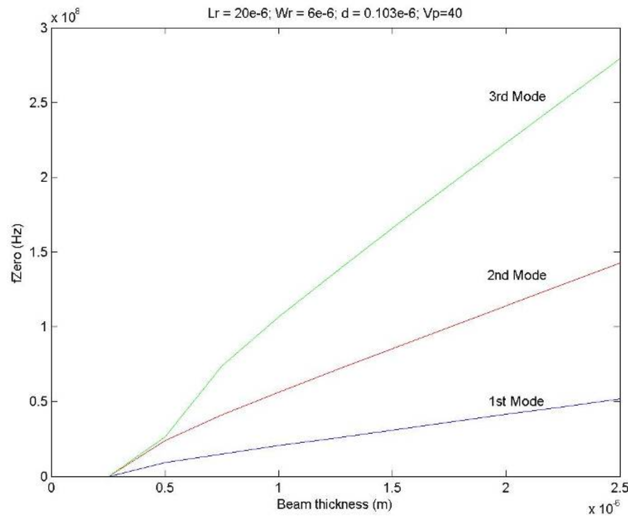

Figure 5-6: Simulated plots of frequency versus beam thickness for free-free beam resonators operating in the fundamental, second and third modes.

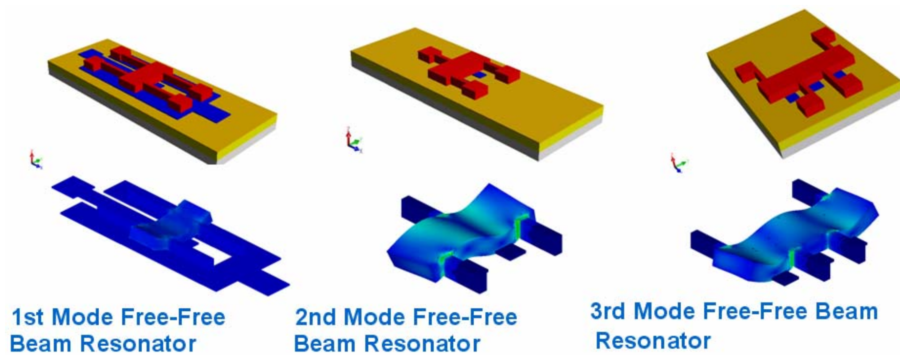

Figure 5-7: First, Second and Third Mode Free-Free Beam Resonator Designs and their behaviors.

First mode and second mode designs have similar beam lengths as 13 μm, however second mode design gives a resonant frequency around 240 MHz whereas first mode have a resonant frequency around 200 MHz. As a result it can be seen that operating in second mode is more advantageous than first mode. Third mode design has a beam length of 20 μm as a consequence of fabrication limitations and it has a resonant frequency of 230 MHz similar to second mode design. So this shows us higher operating modes gives us higher resonant frequencies, yet further increase in the operating mode is no more advantageous due to process limitations. Therefore, second mode beam resonator is selected as optimum design in our further works.

In order to be used in intermediate frequency (IF) filter blocks that take place in the transceiver that is in compliant with IEEE 802.11a communication standard, resonant frequency around 500 MHz is aimed. To achieve this frequency second mode free-free beam design is selected. Four different beam lengths are selected for different second mode resonator designs and additionally each of their node points are determined using MATLAB which are given in the Table below;

Table 5-1: Simulated node points for different beam lengths

	Node 1	Node 2	Node 3
Beam Length = 12 μm	1.6 μm	6 μm	10.4 μm
Beam Length = 10 μm	1.32 μm	5 μm	8.68 μm
Beam Length = 8 μm	1 μm	4 μm	7 μm
Beam Length = 6 μm	0.8 μm	3 μm	5.2 μm

Each beam length with its node points are simulated in the MATLAB and for beam length of 8μm the resonance frequency is found around 485 MHz. Then a compact resonator design having beam length of 8 um and node points as 1μm, 4μm, and 7μm are made as shown in Figure 5-8. Then this design is simulated in COVENTOR using modal analysis tool as shown in Figure 5-9. From the simulation result, resonant frequency of this resonator is found to be 495 MHz and a generalized mass of 2.7x10-14 kg. Furthermore, to have more precise results the free-free beam is modeled using ANSYS tool and applied modal analysis. The resulted frequency obtained from modal analysis is 515 MHz as seen in Figure 5-10 and Figure 5-11.

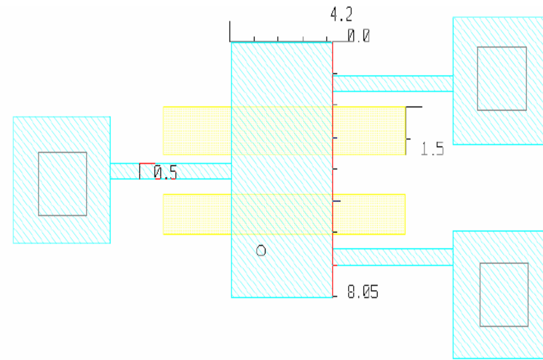

Figure 5-8: Layout of the 500 MHz second mode free-free beam design.

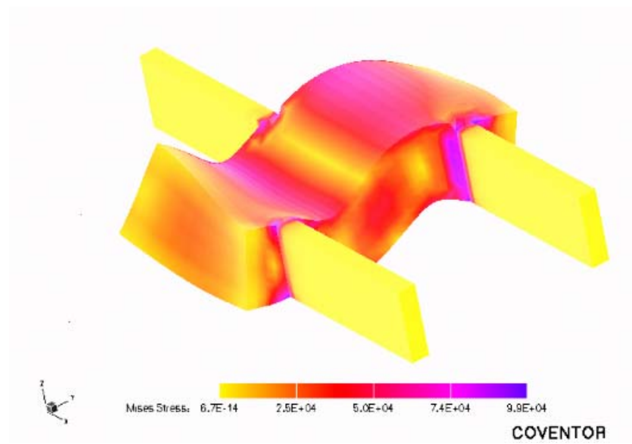

Figure 5-9: 10th mode of the modal analysis (desired second mode behavior)

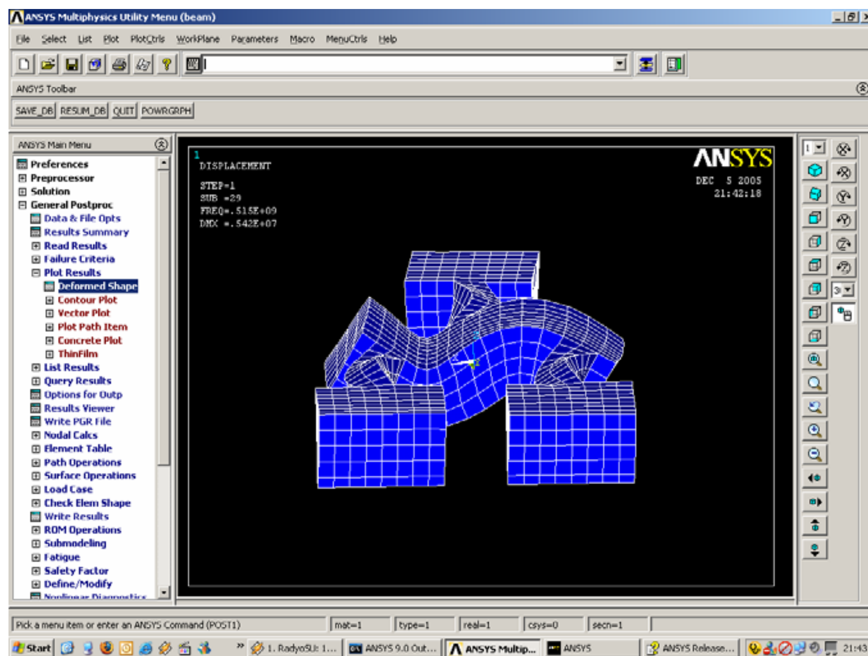

Figure 5-10: Deformed Shape of 2nd Mode Beam

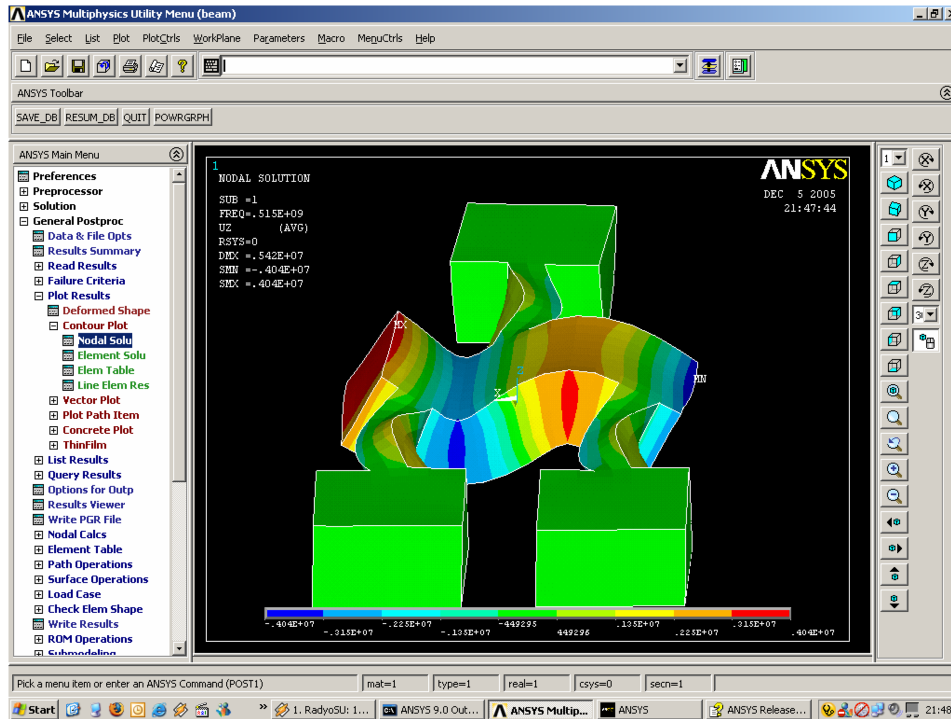

Figure 5-11: Nodal solution of 2nd Mode Beam

5.3 Fabrication Steps of Free-Free Beam Resonator

The fabrication processes of all free-free beam resonators include 5 layers and 3 masks.

The process starts with deposition of 2µm oxide and 0.2µm nitride layers to form isolation layer as seen in step (a) of Figure 5-12 and step (a) and (b) of Figure 5-13. Then with the purpose of forming the electrodes and metal contacts, 0.3µm polysilicon is deposited onto nitride and patterned using electrode mask as seen in step (b) and (c) of Figure 5-12 and step (c) of Figure 5-13. 0.16 µm sacrificial oxide layer deposition, which determines the beam height, follows that and it is patterned with anchor mask and etched in order to form anchors (step (d) of Figure 5-12 and Figure 5-13). Subsequently, 2µm thick polysilicon is deposited onto sacrificial layer and patterned with beam mask to form the beam and supporting beams which is the crucial part of resonator as illustrated in step (e) and (f) of Figure 5-12 and step (e) of Figure 5-13. Finally the sacrificial layer is removed using HF etchant and the final structure is formed as shown in step (g) of Figure 5-12 and step (f) of Figure 5-13.

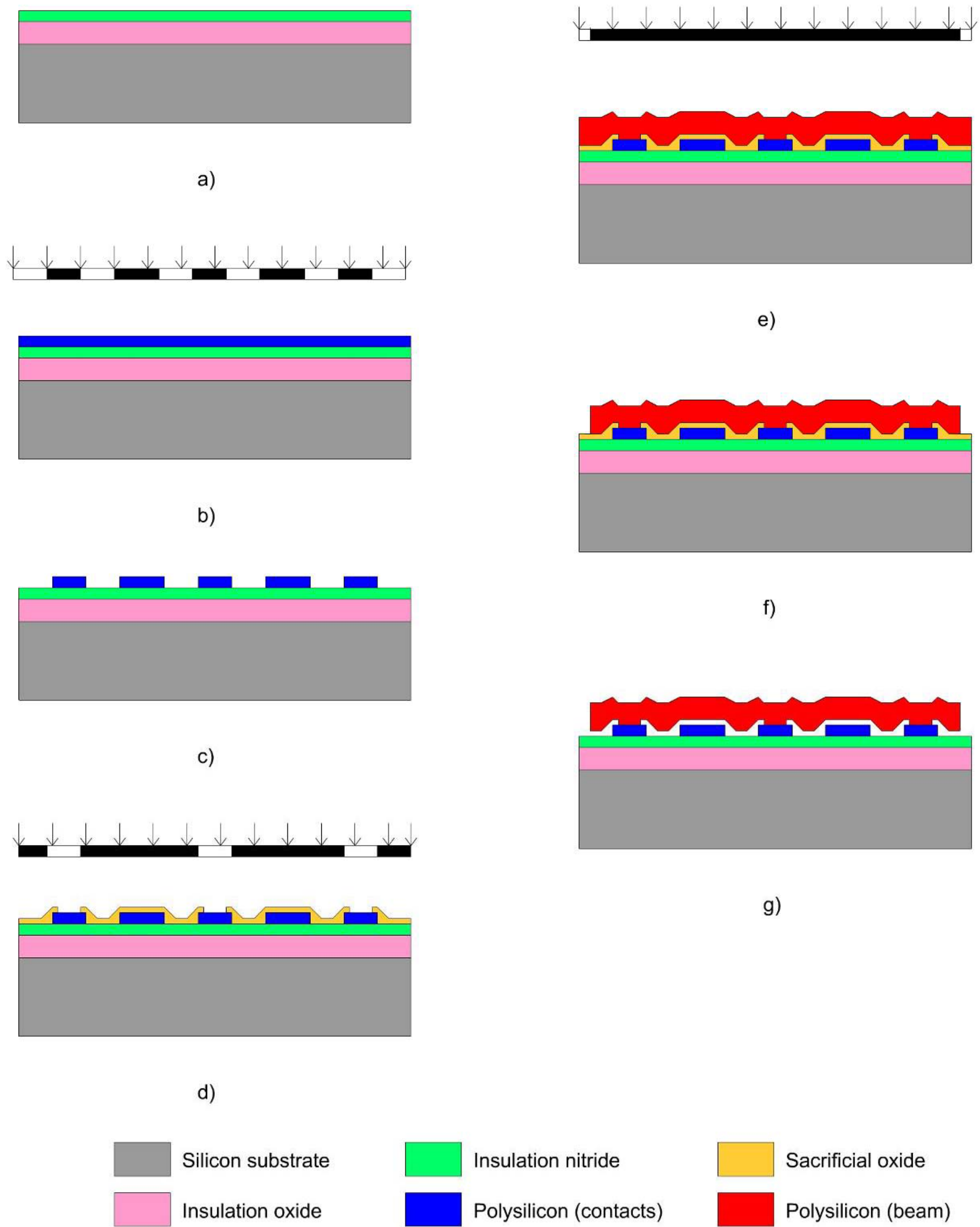

Figure 5-12: Side View of Free-Free Beam Resonator

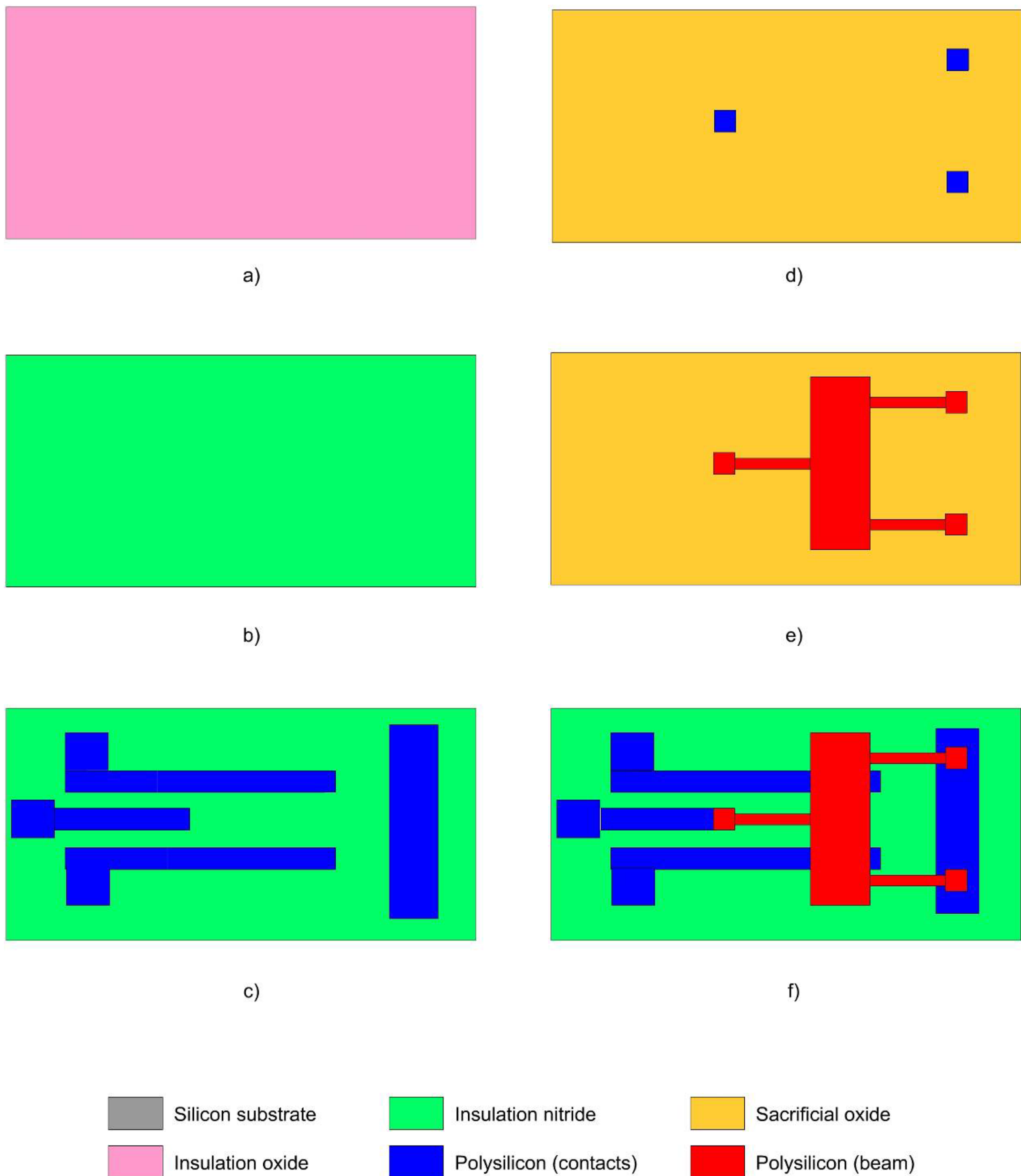

Figure 5-13: Top View of Free-Free Beam Resonators Fabrication Steps

5.4 Free-Free Beam Resonators Designed for MPW process

Aforementioned free-free resonator beam designs are also contained in the multi project wafer which is mentioned in Chapter 3-6 and properties of the materials used in this fabrication are given in Table 2-5.

A 2nd mode free-free beam design with MPW process is illustrated in Figure 5-14.

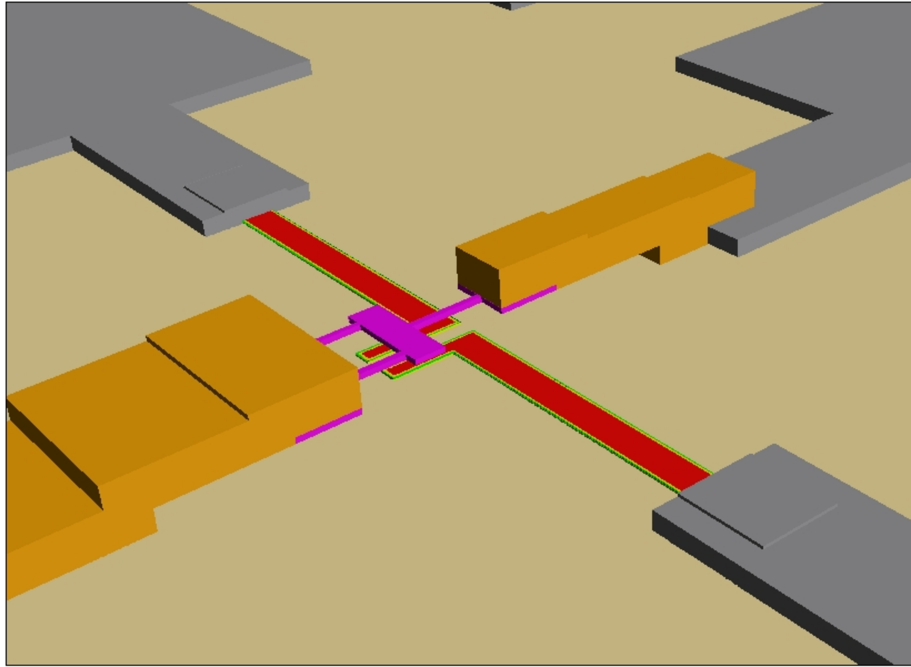

Figure 5-14: 2nd mode free-free beam resonator designed with MPW process

The fabrication steps of the multi project wafer introduce new limitations to designed free-free beam resonators performance parameters. Because of the thin membrane layer, which is 0.9μm Au/Ni/Au stack, the resonance frequency of the resonator dramatically decreases. Also using metal in spite of polysilicon in the beam decreases the stiffness of the beam which is again directly related to resonant frequency of the resonator down to 50-100 MHz range. Also the process has sacrificial layer thickness of 3μm which is very high thinking of beam resonator process. Shortly, this process was not suitable for high performance resonator design. However we used it to investigate the filter characteristics of coupled free-free beams.

To form a band pass filter, two identical resonators have to be mechanically coupled with a flexural beam as shown in Figure 5.18. Such a coupled two-resonator system exhibits two mechanical resonance modes with closely spaced frequencies that define the filter pass-band. The center frequency of the filter is determined primarily by the frequencies of resonators while the spacing between modes is determined by the stiffness of the coupling spring.

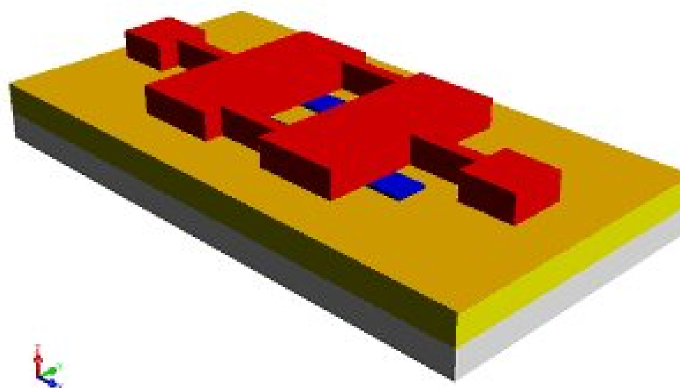

Figure 5-15: Mechanically coupled two 2nd mode free-free beam in order to form a bandpass filter

Various coupled designs are made for the MPW process. 1st mode designs, 2nd mode designs and 3rd mode designs shown in Figure 5-7 are coupled with each other. Also some designs have 1 to 5 resonators coupled in order to increase the bandwith. The fabrication process is still continuing and measurement of RF performances of these filters are left for future work.

5.5 Conclusion & Future Work

In this part general information about MEMS resonators are given. Various MEMS resonators are described and library formation is formed. Free-free beams are described and their design process is presented in detail. Various free-free beam resonator designs which are operating in 1st, 2nd and 3rd modes and have 200 MHz resonant frequencies are designed, simulated and compared. Also a resonator targeting 500 MHz operating frequency is designed and simulated. Fabrications of these designs are left for future work.

Also RF MEMS free-free beam resonators and RF MEMS filters which are composed mechanically coupled free-free beams with various numbers and operating modes are designed for MPW process. The process is still ongoing and measurements of these components are left for future work.

6

Chapter 6
Conclusion & Future Works

This thesis presents realization of RF MEMS components such as capacitive switches, parallel plate variable capacitors, micromachined inductors and resonators for wireless communication applications. Each chapter includes information, literature survey, detailed design procedure, simulations and fabrication steps of each component.

Two RF MEMS designs, for a MPW process and to fabricate in our Cleanroom, are presented and their design steps and fabrication steps are given in detail. There are some problems in the fabrication process. First problem is the sacrificial layer planarization. Due to non-planar surface profile of the sacrificial layer, the top beam layer is not planar and this probably changes the spring coefficient and occurring electrostatic force due to applied voltage. Slightly high pull-in voltage of 14V in measurement comparing to the simulated value of 8.5 V and hand calculated 11V can be resulted according to that effect. The other problem is when releasing the sacrificial photoresist some portion of it remains which probably affects the dielectric constant. This step must also be optimized. The switch designed for MPW process have pull-in voltage of 20V and have a resonance frequency of 415 kHz. Its switching time is estimated as 8.84 μs for 20V applied voltage. Its up state and down state capacitance is found as 23.658 fF and 2.398 pF respectively. The switch shows very low insertion loss <0.1dB up to 40 GHz. Also it has a return loss -40 dB up to 40 GHz. The isolation behavior of the switch in its down position is maximum (around -25 dB) in 20-30 GHz range. Switch

designed and fabricated using in-house capabilities have a low pull-in voltage of around 14V. It has a resonant frequency of 267 kHz. The switching time of the switch is very high as 300 μs which left is out of the applications that needs fast switching time. The switch shows very low insertion loss <0.1dB up to 40 GHz. Also it has a return loss which can be depicted by S_{11} below -20 dB up to 40 GHz. The isolation behavior of the switch in its down position is maximum (around -15 dB) near 30 GHz. The RF measurements of the fabricated switch are still continuing and measurements of MPW process switch is left for future work. The results of measurements will reveal the performances of switches better. It can be said that the switches are not competitive to state of the art switches but definitely it is a good step in the way of designing high performance switches.

In addition to the switches, a dual gap parallel plate varactor structure is designed. In hand calculations 0-4.5 V actuation voltage is found sufficient for tuning from C_{min} to C_{max}. C_{min} of a single electrode is calculated as 177 fF. Then the design is simulated using Coventorware. In the result of MemElectro simulation initial capacitance of a single electrode is found as 210fF. This difference is because the fringing capacitance effect is neglected in the hand calculations. Results of CoSolve simulation revealed that at 5V top beam only touches middle electrode and at 9V it touches all electrodes. The difference between the expected actuation voltage and the simulated one is probably because of non-uniform bending of the top beam. Furthermore, approximate capacitance variation with actuation voltage is graphed using simulations and calculations. Designed varactor shows a capacitance change from 530 fF to 2.4 pF for the applied voltage from 0 to 9V and show a tuning range of 350%. The designed varactor is fabricated using our in-house Cleanroom. However some parts of the design cannot be realized and being changed due to our in-house fabrication limitations. The leveling of the electrodes is decreased to 500nm. Also the planarization of the sacrificial layer cannot be achieved due to fabrication limitations so the two gap values cannot be achieved as in design. However as a starting point a complete varactor fabrication is proposed although the performance parameters of it decreased. As a future work, ways to prevent non-uniform bending of the beam will be investigated. Although the varactor gives a tuning range of 350%, further ways to increase it can be examined. Using MEMS switches, as mentioned in the chapter, can be good option to accomplish the tuning range improvement which is left for future work. Planarization of the sacrificial layer is another problem that has to be overcome. There are some techniques like CMP or coating thick polymers and then etching them. Exploring them is left for future work.

Moreover, Large range of inductors, inductance values form 1.1 to 6.5 and quality factors about 20-40 are being designed and simulated. These inductors are aimed to be integrated in to RF Blocks to improve their performance parameters. An LNA example is given in which an high Q inductor (Q=30) in the input matching stage improves the noise figure from 2.8dB to 1.8dB. Above IC process is studied and some test structures are created which is a first step in the way of post processing. Yet, there are some issues need to be overcome such as filling the deep via holes in dielectric and deposition of thick metal layers. Sputter deposition is not sufficient for the mentioned applications. We have started to use electroplating and trying to optimize the parameters. However, this is left for future work. Additionally fabrication steps of a suspending MEMS inductor is given in detail. Each step of this process is optimized and finally suspending inductors are structured. However this suspended inductors are different from designed and simulated ones due to the fabrication limitations. . Inductance values of the fabricated test inductors are around 1nH. They give peak quality factor of 11 between 2-3 GHz. These low Q values are due to the substrate coupling of the coil because the suspension height is very low as 1.4µm as a result of using photoresist as sacrificial layer. Also thickness of the coil was not sufficient to have higher quality factors. Improving the fabrication process of these inductors and in parallel their performances as designed is left for future work.

Lastly, MEMS free-free beam resonators are described and their design process is presented in detail. Various free-free beam resonator designs which are operating in 1st, 2nd and 3rd modes and have 200 MHz resonant frequencies are designed, simulated and compared. Also a resonator targeting 500 MHz operating frequency is designed and simulated. Fabrications of these designs are left for future work. Also RF MEMS free-free beam resonators and RF MEMS filters which are composed mechanically coupled free-free beams with various numbers and operating modes are designed for MPW process. The process is still ongoing and measurements of these components are left for future work.

To sum up, various MEMS components are designed considering the in-house fabrication capabilities of Sabanci University clean-room and also fabricated. Also some designs are made as a part of multi-wafer project and send for fabrication. It has been shown that integrating micromachined above IC inductors improves the performance parameters of a realized LNA, however, the integration and post processing is left for future work. Also designed switches, after optimizing the fabrication process and overcoming the fabrication problems can be applied to switching matching networks. The designed varactors can be applied to LC tanks of VCO, which is also realized as MEMS integrable version similar to

aforementioned LNA, in order to tune the oscillation frequency. The performance parameters of the designed parts are simulation parameters so they can only estimate the overall performance. The result will be clarified after measurement parts completed. Although the designed components are not state of the designs due to fabrication limitations, they are a promising first step in realizing higher performance devices in future.

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