A FRONT-END INTEGRATED CIRCUIT FOR 3D ACOUSTIC IMAGING USING 2D CAPACITIVE MICROMACHINED ULTRASONIC TRANSDUCER ARRAYS

by

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A FRONT-END INTEGRATED CIRCUIT FOR
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DATE OF APPROVAL: 13.08.2004

Dedicated to my unborn son

Acknowledgments

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Özet

İki boyutlu kapasitif mikro işlenmiş ses ötesi dönüştürücülerle (KMSD) elektronik arabirimlerinin tümleştirilmeleri küçük dönüştürücü boyutları ve bağlantı için gerekli olan kanalların çokluğu nedeniyle gerçekleştirilmesi çok zor olan bir iştir. Bu tezde hacimsel akustik görüntülemede kullanılan iki boyutlu KMSD'lerle arabirim oluşturmak icin bir ön-alıcı-verici tümdevre tasarlanmışır. Devre KMSD'yi sürecek olan ve yüksek gerilime dayanıklı devre elemanlarından oluşan bir sürücü, KMSD'nin dikey olarak tersyüz tümdevre birleştirme teknolojisiyle elektronik arabirimine bağlanacağı dolgulama, yüksek gerilim darbelerinin düşük gerilimle calışan devre elemanlarına ulaşmasını engelleyecek bir koruma devresi ve yansıyan işareti tamponlayacak ve kuvvetlendirecek bir düşük gürültülü kuvvetlendiricisinden oluşur. KMSD'nin elektromekanik modeli geliştirilmiş, model icin gerekli olan parametreler ANSYS programında yapılan üç boyutlu modelleme benzetimleriyle elde edilmiştir. Bu model kullanılarak yapılan serim öncesi her bir alt devre Cadence Spectre benzetim ortamında denenmiştir. 10 pF'lık bir yük kapasitörü devre elemanları arasındaki ve tümdevre dısındaki bağlantıları modellemek için kullanılmıştır. Tasarlanan tümdevre hücresi $200 \times 200\mu m^2$'lik bir alan kaplamaktadır ki bu alan Nyquist örnekleme kriteri uyarınca 3.5 MHz'e karşılık gelen dalga boyunun yarısından daha küçüktür. Tümdevredeki parazitik elemanların devre performansını hangi düzeyde etkileyeceğini belirlemek amacıyla yapılan serim sonrası benzetim sonuçları ile serim öncesi benzetim sonuçlarının uyumlu oldukları gözlenmiştir. Düşük gürültülü okuma kuvvetlendiricisinin girişindeki eşdeğer gürültü 6.45 $\mathrm{nV}/\sqrt{Hz}$ olarak ölçülmüştür. 4×4 hücreden oluşan deneysel tümdevre ilk testler ve sonrasındaki araştırmalarda kullanılmak üzere AMS 0.8 μm 50 V teknolojisiyle üretilecek şekilde tasarlanmıştır. Tasarlanan tümdevre tersyüz tümdevre teknolojisi ya da CMOS üstünde KMSD teknolojisiyle KMSD'lere bağlanabilir.

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Chapter 1

INTRODUCTION

1.1 Capacitive Micromachined Ultrasonic Transducer (CMUT)

The history of practical ultrasonic transducers starts with the World War I. In the history of ultrasonic imaging, many piezoelectric crystals were used such as Rochelle salt and quartz, the pioneer materials used in 30s. Second generation of the materials used for transducers were ceramics, invented after the World War II, such as barium titanate and lead zirconate titanate. In the second half of the 20^{th} century, after the invention of fixed-focus electronic sector scanning in late 60s, polymers such as polyvinylidene fluoride to name one, had become the dominant materials on the ultrasonic transducer market. Further developments in the process technology yielded linear transducer arrays, taking fixed focus electronic sector scanning systems off the throne by providing improved resolution and faster image construction.

The microelectronics revolution during the past 20 years has developed the advanced digital signal processing units which are capable of processing abundant amount of data in a very short time interval. The developments encouraged new algorithms to be derived for reconstructing acoustic images. Nevertheless, the efficiency of these algorithms depends strongly on the quality factors of the received echo signal like signal to noise ratio or bandwidth. Because of this reason from the perspective of image reconstruction the transducer and its front-end analog interface

have vital importance .

In the order of the evolution of acoustic transducers, chronologically, piezoelectric crystals, ceramics, polymers and recently piezo-composite materials [8] are used. Even though the concept of capacitive ultrasonic transducer begins with the piezo counterpart, piezoelectric materials have dominated the market due to the fact that capacitive ultrasonic transducers electric field strength requirements were not realizable in the past. However, today's advanced micro-fabrication technology offers capacitive ultrasonic transducers not only in single but also in 1D or 2D array forms that can compete with piezoelectric transducers. The Capacitive Micromachined Ultrasonic Transducer (CMUT) is a recently invented [1] device, used for the generation and detection of ultrasonic waves. The transducer is built on a heavily doped Si substrate using bulk CMOS compatible micro-fabrication processes. The imaging resolution is proportional to the operating frequency which also determines the dimensions of the device.

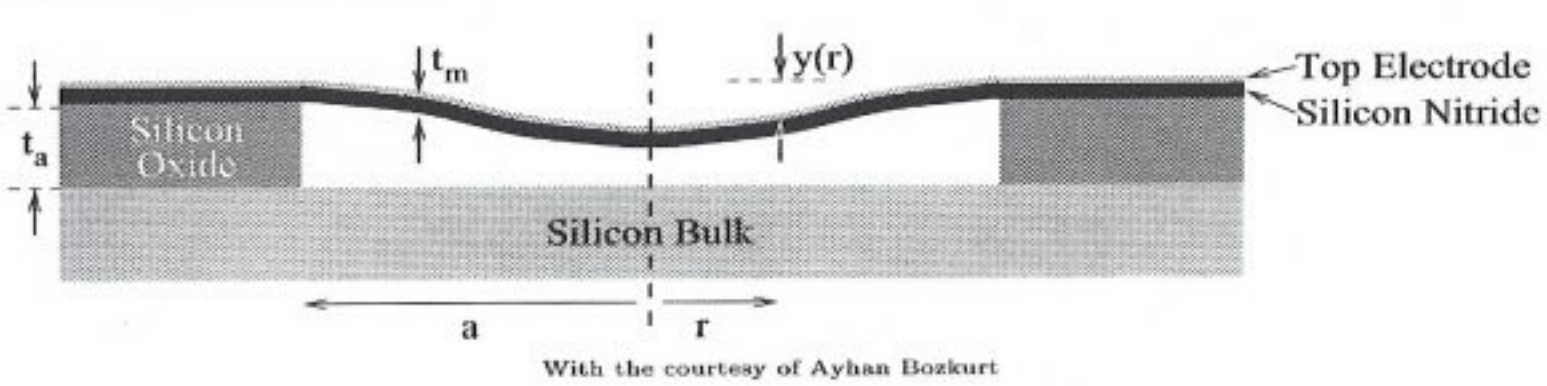


Figure 1.1: Cross sectional view of the CMUT

1.2 The Fabrication Processes of CMUT

Graphical representation of the fabrication flow is given as below:

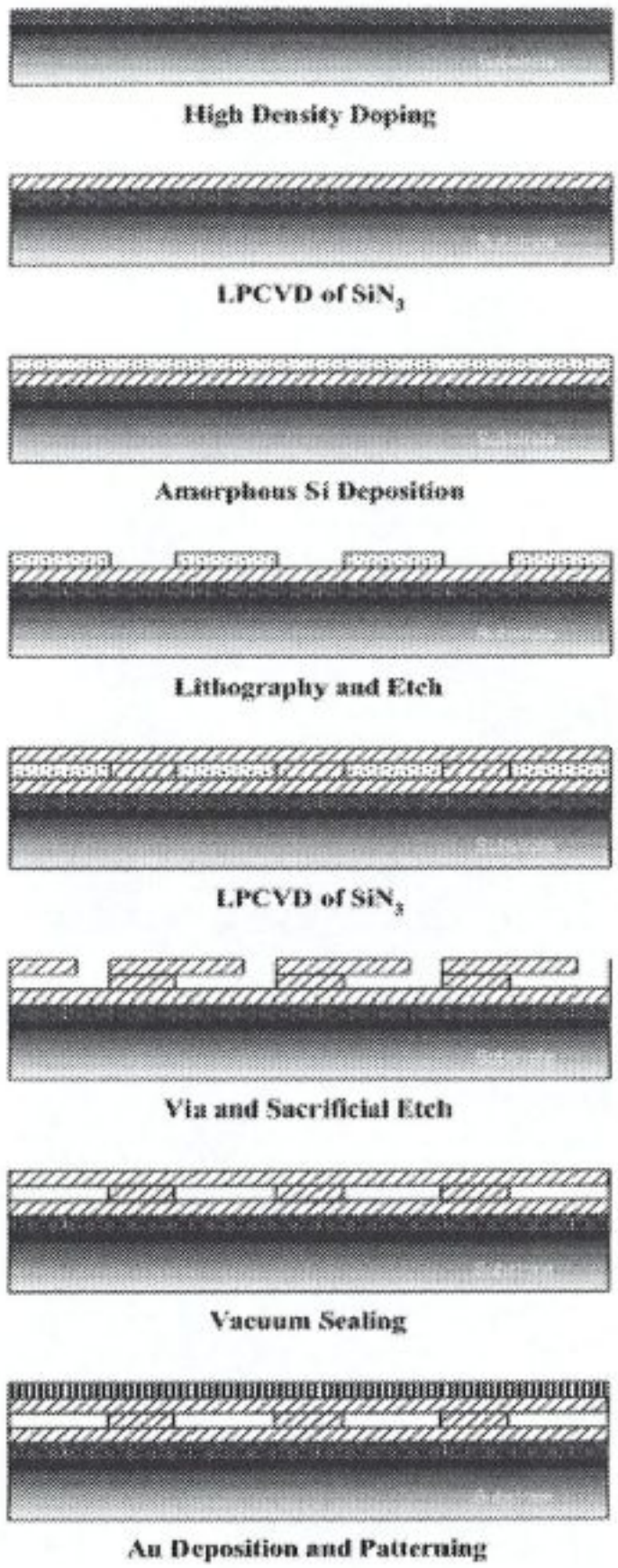
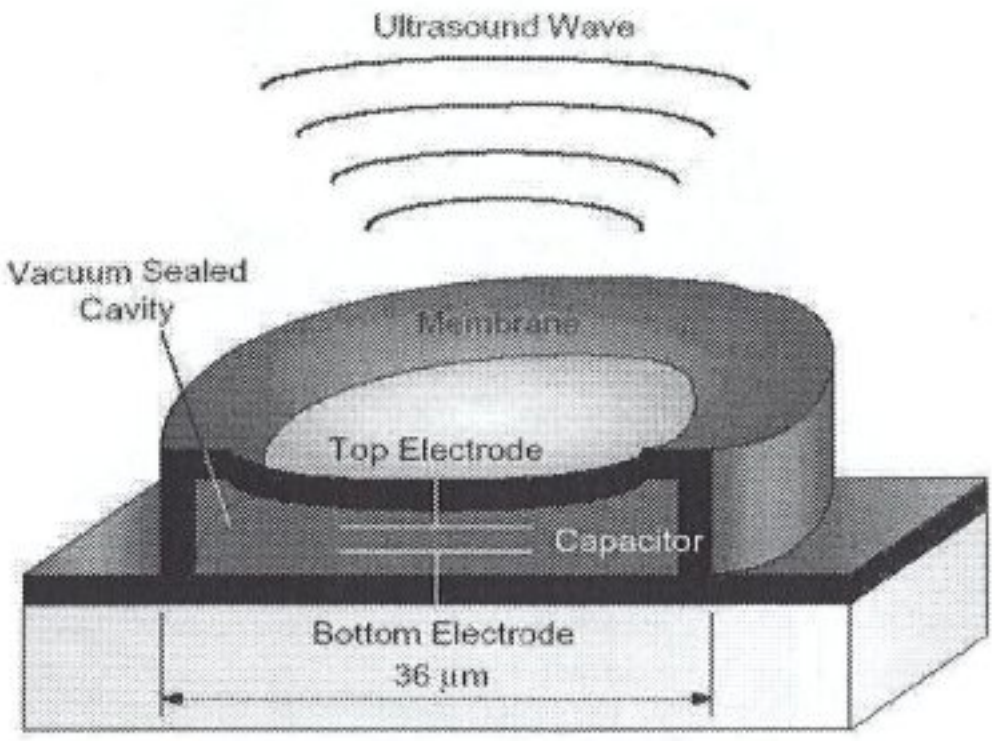


Figure 1.2: Fabrication processes of CMUT

1.3 The Physical Structure of CMUT

CMUT basically consists of a thin Au electrode as the top layer, a flexible SiN_3 membrane under it, a gap formed by the SiO_2 supporting sidewalls and heavily doped Si substrate as the second electrode. The device is usually circular in shape. There exists hexagonal variants to provide maximum density per unit area. The cross-sectional view of the device is shown in figure 1.1 along with the 3D visualization in figure 1.3. The membrane layer is supported by the sacrificial layer from which cylindrical openings are cut.



With the courtesy of E.L. Ginzton Laboratory - Stanford University

Figure 1.3: 3D view of the CMUT

1.4 The Operation of CMUT

CMUT's operation is based on electrostatic attraction which is inclined bias independently towards the electrodes as shown in figure 1.4. For harmonic operation a DC bias is required to hold the Si_3N_4 membrane stretched. For the acoustic wave generation the voltage between the electrodes must be in the form

$$V(t) = V_{DC} + V_{AC}(t) \tag{1.1}$$

The efficiency of the transducer is determined by the DC bias voltage and it is proportional to V_{DC}. Though at first glance it seems that efficiency can be easily

modified by increasing the bias voltage, actually there exists a limit on the V_{DC} because of the unwanted oscillation modes, generated when the membrane collapses to the bottom plate. In addition to this, the process technology will limit the maximum allowable DC bias, $V_{COLLAPSE}$, due to dielectric breakdown phenomenon. Therefore an upper bound for the DC bias voltage exists, not only due to the operation of CMUT but also due to the fabrication process of CMUT.

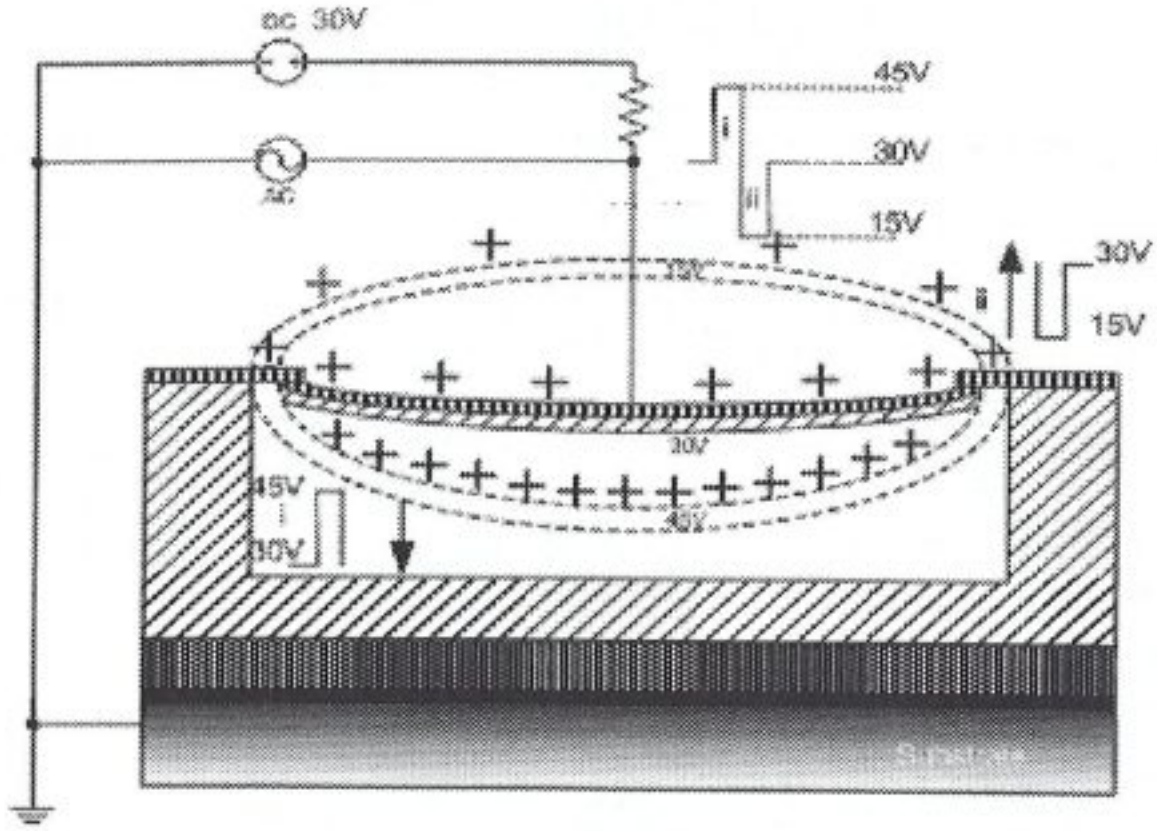


Figure 1.4: CMUT's operation is based on electrostatic attraction

Transducer's capacitance formed by the top and bottom electrodes is modulated by the transmitted and received acoustic signals. In the transmitting phase, high voltage pulse will stretch and loosen the membrane, causing a mechanical vibration at the mechanical resonance frequency of the CMUT which is determined by device dimensions. Acoustic waves created by this vibrations will propagate both inwards and outwards. The inward acoustic waves will be reflected from the bottom plate and will create false echoes on the membrane. Since the thickness and the speed of the acoustic waves in vacuum are known the expected arrival time of these false echoes can be calculated and avoided by proper timing of transmit/receive time windows. In receiving phase the capacitance of the transducer will be modulated by the received echoes causing the device acting as a small signal source. Because of this reason the inherent capacitance of CMUT becomes an important design

parameter. This inherent capacitance offset can be reduced by patterning the top metal electrode with a cost of reduced efficiency. It is found that device's capacitance and efficiency have complex dependencies on electrode shape [2]. It is shown in [2] that an optimum point device performance can be found by judiciously patterning of the top electrode.

1.5 The Model of CMUT

The starting point for the development of a model for CMUT is the equivalent circuit approach of Mason [4] as shown in figure 1.5. The membrane impedance is derived in [2] as

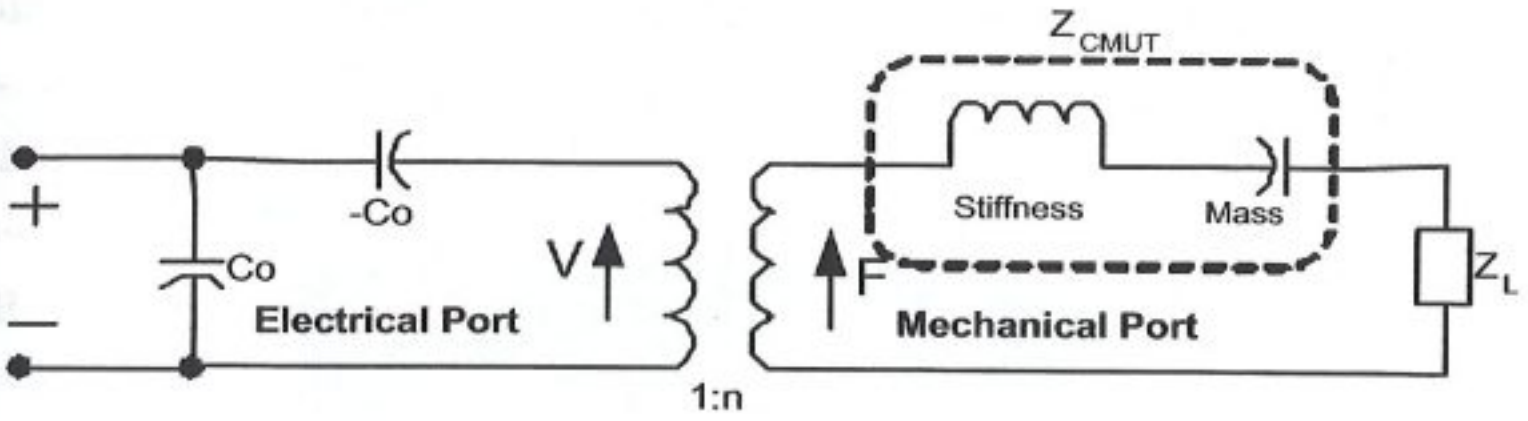


Figure 1.5: Equivalent circuit model

$$Z_a = \frac{\pi a^2 \rho}{v(\omega)} = \frac{j\rho t_n}{\pi a^2} = \left[\frac{\left[k_2 \frac{J_o(k_1 a)}{J_1(k_1 a)} + k_1 \frac{I_o(k_2 a)}{I_1(k_2 a)} \right] \frac{k_1 k_2 a}{2(k_1^2 k_2^2)}}{\left[k_2 \frac{J_o(k_1 a)}{J_1(k_1 a)} + k_1 \frac{I_o(k_2 a)}{I_1(k_2 a)} \right] \frac{k_1 k_2 a}{2(k_1^2 k_2^2)} - 1} \right] \tag{1.2}$$

Coefficients k_1 and k_2 can be calculated by

$$k_1 = \sqrt{\frac{\sqrt{d^2 + 4c\omega^2} - d}{2c}} \tag{1.3}$$

$$k_2 = \sqrt{\frac{\sqrt{d^2 + 4c\omega^2} + d}{2c}} \tag{1.4}$$

and c and d as

$$c = \frac{(Y_o+T)t_n^2}{12(1-\delta^2)} \quad d = \frac{T}{\rho t_n} \tag{1.5}$$

where

a: Radius of the top electrode

ρ: Poisson's ration

t_n: Membrane thickness

T: Residual stress in the membrane material

ω: Frequency

Y_o: Young's modulus

Z_a equation provides an analytic expression for the resonance frequency of the membrane which also determines the operation frequency. The CMUT cell is characterized by its electrical input capacitance C_0, an electro-mechanical transformer with a transfer ration of n (Nt/Volt), and the mechanical impedance of the membrane, Z_a as shown in figure 1.5). An electrical source with an output impedance of R_s provides the electrical drive, while C_p models the interconnection parasitics. The equivalent circuit is terminated by a load impedance R_{load}, which represents the acoustic impedance of the surrounding medium. When the membrane is operated in its fundamental vibration mode, the acoustic impedance of the membrane (Z_a) can be modelled as a tuned circuit with components L_a and C_a representing the mass and stiffness of the membrane [4, 5]. Table 1.1 lists the device parameters used in the simulations [10, 12].

Description	Parameter	Value	Units
Membrane radius	a	15	μm
Nitride membrane thickness	t_n	0.30	μm
Air-gap thickness	t_a	0.15	μm
Insulating layer thickness	t_b	0.15	μm
Number of cells	N	25	

Table 1.1: Characteristic parameters of the CMUT used in simulations

Mechanical properties of the material were taken from standard texts [5], while the nitride membrane is assumed to have a residual stress of 0.9 $\times 10^9$ Pa [6]. For

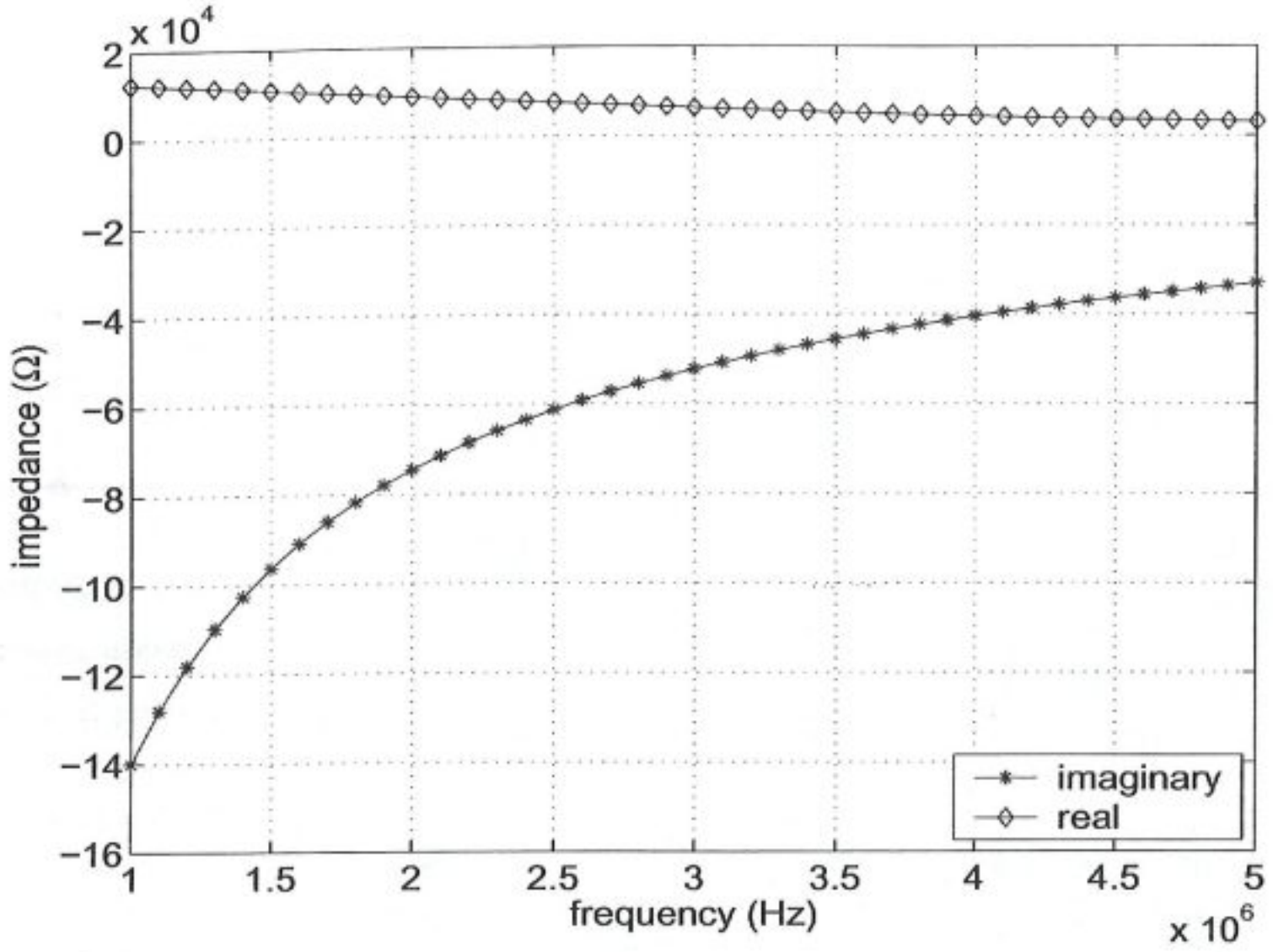


Figure 1.6: The input impedance of the transducer that consists of 25 CMUT cells

the given membrane radius, approximately 25 cells will form an array element of size 200 μm×200 μm. Using Mason's model, The input impedance of the parallel connection of 25 CMUT cells is found as depicted in figure 1.6. These device characteristics were used to find the component values of the model in figure 1.5. To be used in the Spectre circuit simulator (by Cadence Design Systems), modifications were made on the equivalent circuit representation. First, all components on the mechanical side of the model were transferred to the electrical port, so that $R_{mem}=R_{load}/n^2/N$, $L_{mem}=L_a/n^2/N$, $C_{mem}=R_{load}\cdot n^2\cdot N$. Second, the transferred load resistance R_{mem} was replaced by a transmission line of characteristics impedance set to R_{mem}, which represented the liquid medium into which acoustic power was coupled. The transmission line had a length of 10 λ at the operation frequency, and was terminated by a resistance R_{term} where $R_{term} \gg R_{mem}$. Hence, the equivalent circuit represented a CMUT array element with 25 cells, immersed in water with

a perfect half-spherical reflector placed 10 wavelengths away from the transducer. Figure 1.7 shows the equivalent circuit used in simulations.

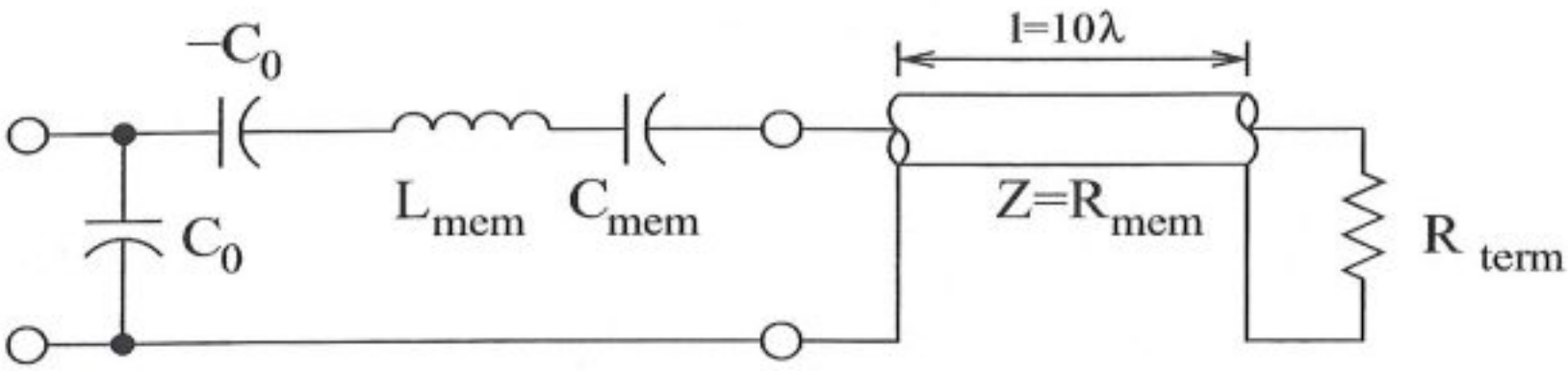


Figure 1.7: Equivalent circuit for the immersion CMUT used in circuit simulations. A transmission line of length 10 λ terminated with $R_{term} \gg R_{mem}$ represents a half-spherical perfect reflector placed 10 wavelengths away from the transducer.

For the listed device parameters in Table 1.1 and a bias voltage of 30 V, the component values of the circuit in figure 1.7 were found as: C_{mem}=2.04×10^{-14} F, L_{mem}=3.27×10^{-3} H. From Mason's model, C_0 and R_{load} are found by multiplying the membrane area by the per unit area capacitance of the device and the acoustic impedance of the liquid medium, respectively. In our case, the computation of C_0 and R_{load} required special treatment: First of all, the CMUT membrane was not fully metalized [3], hence C_0 was smaller than the value found by Mason's model. Secondly, the overall transducer dimensions are smaller than the acoustic wavelength in the surrounding liquid medium, hence the effective radiation resistance seen by the transducer was reduced [7]. To find the impedance scaling factor, finite element method (FEM) simulations were run using ANSYS. A 3-D model for a transducer array element of 25 CMUT cells was constructed, as shown in figure 1.8. A 5×5 array of circular piston transducers were modelled using a solid mesh, and placed in a rigid baffle. Then, the solid model was brought into contact with a liquid half-sphere whose outer surface was meshed by acoustic absorbing elements. A uniform displacement of d=10 nm was applied to the piston elements. The total radiated power by the 25 piston elements was expected to be

$$Pr_{total} = \frac{1}{2} \left(25 \times \pi a^2\right) \left(2\pi f\, d\right)^2 Z_{eff} \tag{1.6}$$

where f was the operation frequency (which was 3 MHz for the particular example)

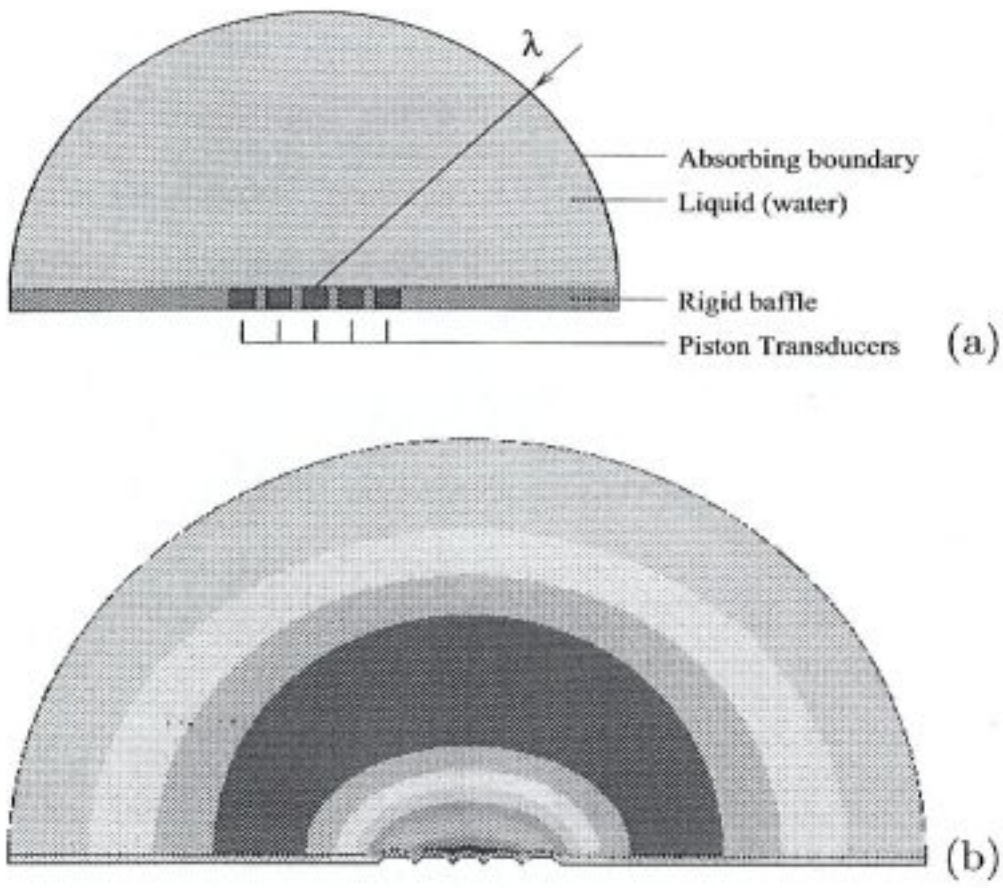


Figure 1.8: 3-D FEM model used for computation of the effective radiation impedance of the CMUT array element.(a) Cross-sectional view of the model (b) Simulated pressure field.

and Z_{eff} was the effective radiation impedance. After a harmonic analysis, the actual radiated power by the transducer array was found by

$$Pr_{total} = \frac{1}{2} \sum_{i} \frac{|P_i|^2}{Z_{water}} \cdot A_i \tag{1.7}$$

where the summation index i was run over all elements forming the absorbing boundary, and, P_i and A_i were the pressure on and the area of the i th element, respectively. The simulation showed that Z_{eff} was 1.04 MRayl, and hence, the impedance scaling factor was found as $\theta_0 = 0.693$. Therefore, for a bias of 30 V, R_{mem} of the equivalent circuit of Fig. 1.7 was 2.191 MΩ.

1.6 The Design Parameters of CMUT

1.6.1 The Collapse Voltage

Maximum allowable DC bias voltage is limited to prevent collapse of the membrane. Conventional capacitors have non -moving, rigid plates and maximum voltage the device can stand is determined by the dielectric breakdown. Since one plate of

the CMUT is a flexible membrane, the electrical field formed by the applied DC bias voltage between the parallel plates, causes the attraction of charges on the plates. So the membrane moves towards the bottom plate and with increasing V_{DC} it collapses to bottom plate. Actually CMUT can operate even the membrane is collapsed to bottom plate, but since unwanted vibration modes are generated this kind of operation is generally avoided. Calculation of $V_{COLLAPSE}$ can be achieved by electromechanically modelling the device with a linear spring between plates as shown in figure 1.9. The spring constant can be obtained as the ratio of pressure to volume displacement [4] as shown in equation (1.8).

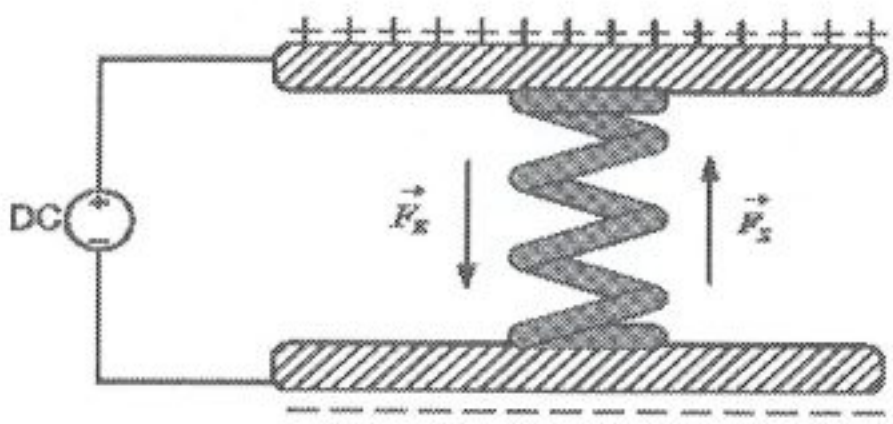


Figure 1.9: Mechanical model of CMUT

$$\kappa = \frac{TAt_n}{\frac{c}{d} - \frac{a}{2}\frac{J_o(a\sqrt{d/c})}{J_1(\sqrt{d/c})}\sqrt{c/d} + a^2/8} \tag{1.8}$$

And auxiliary coefficients can be calculated as

$$c = \frac{(E+T)t_n^2}{12\rho(1-\sigma^2)} \quad d = \frac{T}{\rho} \tag{1.9}$$

where

T: Residual stress

A: Area of the membrane

ρ: Density

σ: Poisson's ratio of the membrane material

The total force on the string is

$$\left|\vec{F}_S\right| = \kappa x \tag{1.10}$$

and the electrostatic force on the membrane is calculated as

$$\left|\vec{F_E}\right| = \frac{A\varepsilon^2 V^2}{2\varepsilon_o(t_n + \frac{\varepsilon}{\varepsilon_o}(t_a - x))^2} \tag{1.11}$$

where t_a is the gap thickness.

The voltage required to keep the membrane at a certain deflection level can be found by equating

$$\left|\vec{F_S}\right| = \left|\vec{F_E}\right|$$

and solving for V. As the voltage increases the membrane will move towards the bottom plate and after collapsing no more deflection will take place. If this is expressed in terms of mathematics, after collapsing

$$\frac{\partial V}{\partial x} = 0 \tag{1.12}$$

Solution of this equation is calculated as

$$V_{COLLAPSE} = V_{DC\,\max} = \sqrt{\frac{8\kappa(t_a + \frac{\varepsilon}{\varepsilon_o}t_n)^3}{27A\varepsilon_o}} \tag{1.13}$$

For small deflections electrical field can be expressed as

$$E(r,t) = \frac{V(t)}{(t_n + \frac{\varepsilon}{\varepsilon_o}t_a)} \tag{1.14}$$

and residual stress will be

$$T(r,t) = \frac{\frac{1}{2}\frac{\varepsilon}{\varepsilon_o}(V_{DC}^2(r) + 2V_{DC}(r)V_{AC}(r)\sin\omega t)}{(t_n + \frac{\varepsilon}{\varepsilon_o}t_a)^2} \tag{1.15}$$

1.6.2 The Bandwidth of Immersion CMUT

If CMUT is assumed to be a parallel plate capacitor then

$$C = \frac{\varepsilon A}{t_n + \frac{\varepsilon}{\varepsilon_o}} \tag{1.16}$$

for small deflections of the membrane electric field can be expressed as

$$E(r,t) = \frac{V(t)}{t_n + \frac{\varepsilon t_a}{\varepsilon_o}} \tag{1.17}$$

$$T(r,t) = \frac{\frac{1}{2}\left[V_{DC}^2(r) + 2V_{DC}(r)V_{AC}(r)\sin\omega t\right]}{\left[t_n + \frac{\varepsilon}{\varepsilon_o}t_a\right]^2} \tag{1.18}$$

and electromechanical transformer ratio n is calculated to be

$$n = A\frac{\varepsilon^2 V_{DC}}{\varepsilon_o(t_n + \frac{\varepsilon}{\varepsilon_o}t_a)^2} \tag{1.19}$$

The time constant of the device is

$$\tau = \frac{C_o Z_L}{n^2} = \frac{\varepsilon_o^2\left(t_n + \frac{\varepsilon}{\varepsilon_o}t_a\right)^3 Z_L}{\varepsilon^3 V_{DC}^2} \tag{1.20}$$

The spring constant has an approximate expression as given in [4]

$$\kappa \cong \frac{16\pi Y_o t_n^3}{(1-\rho^2)\,a^2} \tag{1.21}$$

By using this approximation $V_{COLLAPSE}$ is recalculated to be

$$V_{COLLAPSE} \cong \sqrt{\frac{128 Y_o t_n (t_n + \frac{\varepsilon}{\varepsilon_o}t_a)^3}{27\varepsilon_o(1-\rho^2)a^4}} \tag{1.22}$$

Finally the time constant is

$$\tau \cong Z_W \frac{27(1-\rho^2)a^4}{128 Y_o t_n^3} \tag{1.23}$$

where Z_W denotes the acoustic impedance of the loading medium.

When $V_{DC} = V_{COLLAPSE}$, the bandwidth of CMUT does not depend on the air gap thickness t_a. As a conclusion the resonance frequency of the CMUT membrane is developed as [4].

$$f_R \cong 0.917\sqrt{\frac{Y_o}{12\rho(1-\delta^2)}}\frac{t_n}{a^2} \tag{1.24}$$

To operate a CMUT at a certain frequency, t_n/a^2 ratio has to be constant while adjusting device dimensions in order to increase the bandwidth. This condition when combined with equation (1.23) makes sure that the bandwidth and the thickness of the membrane are proportional. If CMUT is used as an immersion device (loaded with a relatively high acoustic impedance liquid), the composition of Z_L and Z_{CMUT} is going to be a low-Q (wideband) circuit. For the frequencies near the mechanical resonance of the device membrane impedance can be neglected. Since the imaginary part of CMUT's impedance is negligibly small and the real part of

CMUT is much smaller than the real part of loading medium's impedance.

The inherent capacitance formed between the plates of CMUT will affect the efficiency and bandwidth of the device. Since bandwidth is of concern, the effect of C_o can not be easily minimized (such as by forming an LC tank circuit at the resonance frequency). One basic approach to minimize the effect of C_o can be the reduction of the top metal electrode. Without sacrificing from mechanical properties such as electromechanical conversion efficiency n, C_o can be reduced. This idea is based on not only how much the membrane deflects (how much force is applied) but also on the location of applied force. The center of the membrane is the point to apply force which gives the maximum deflection/(constant) force ratio. This approach is justified by simulation results in [2] concluding that electrode metallization area and bandwidth are inversely proportional. The membrane can be partially metallized and for this reason unlike fully metallized membrane the applied force will appear on a fraction of the membrane.

The transformer ratio n depends on the electrode pattern and n can be considered frequency independent as long as the vibrating membrane does not collapse to the substrate. For a smaller electrode a larger bias can be applied. AC stress on the membrane increases in accordance with the DC bias voltage. The dependency is almost linear for small deflections as E_{DC} linearly scales with V_{DC}. For larger deflections, E_{DC} increases faster as the membrane gets closer to the bottom electrode. The transducer with maximum bandwidth should have a top electrode which must be as small as possible. Interconnections to the top electrode will set a limit to how small it can get, as will breakdown mechanisms.

1.7 The Advantages and The Disadvantages of CMUT

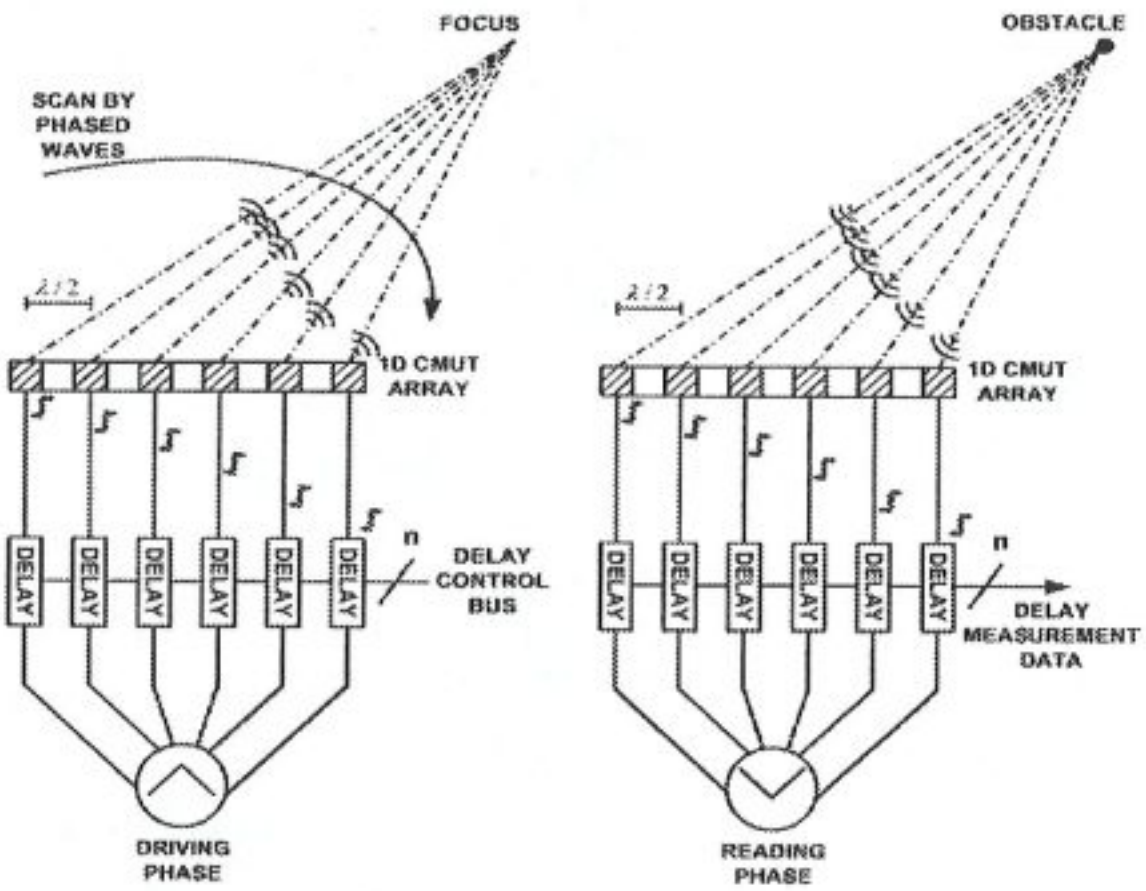
The primary advantage of CMUTs over traditional piezoelectric counterparts is the inclination of integration to VLSI circuits. Fabrication process is CMOS compatible and does not include sophisticated steps. Integrability of CMUT increases the SNR, since integrated electronics can be built on the same substrate at the minimum distance which reduce noise pickup and other SNR degrading effects due to connection media such as cables, connectors etc. In addition to SNR improvements, *Si* level fabrication costs are lower for CMUT. When laid out as 2D arrays higher resolution can be obtained. The efficiency of CMUT is proportional to the bias voltage of the device but which is limited not only by the collapse voltage but also by the dielectric breakdown phenomenon. The only loss mechanism is due to substrate capacitive coupling which is the common loss mechanism in CMOS technology. CMUTs can achieve higher operating frequencies and have higher bandwidths. When operating in air CMUTs outperform conventional piezoelectric transducers. Due to large impedance mismatch between common piezoelectric materials and air, piezoelectric ultrasonic transducers are not very efficient sources of ultrasound in air. In addition, piezoelectric transducers require some kind of impedance matching medium which is usually a liquid that limits the flexibility of their role in portable applications.

The obtrusive disadvantage of CMUT is its bias voltage requirement which puts a limit on integration when it is produced with interface circuits. High efficiency operation dictates a high bias voltage which may not be compatible with the integrated circuit processing technology. In 2D array applications the cell size becomes a constraint for the circuit designer since the cell area and resolution are determined by the operating frequency. Circuit and CMUT must have the same area to make it easy to align the transducer array on the circuit array by means of vertical connection methods such as flip - chip bonding [22, 23]. Signal and bias routing to array elements is another problem especially in such crowded matrices. The spacing between CMUT cells must be small for providing high resolution. Furthermore

cross-talk effects are observed [9]. It is also reported that CMUT cross talk can be reduced by thinning wafer and by etching trenches between array elements [21].

1.8 The Applications of CMUT

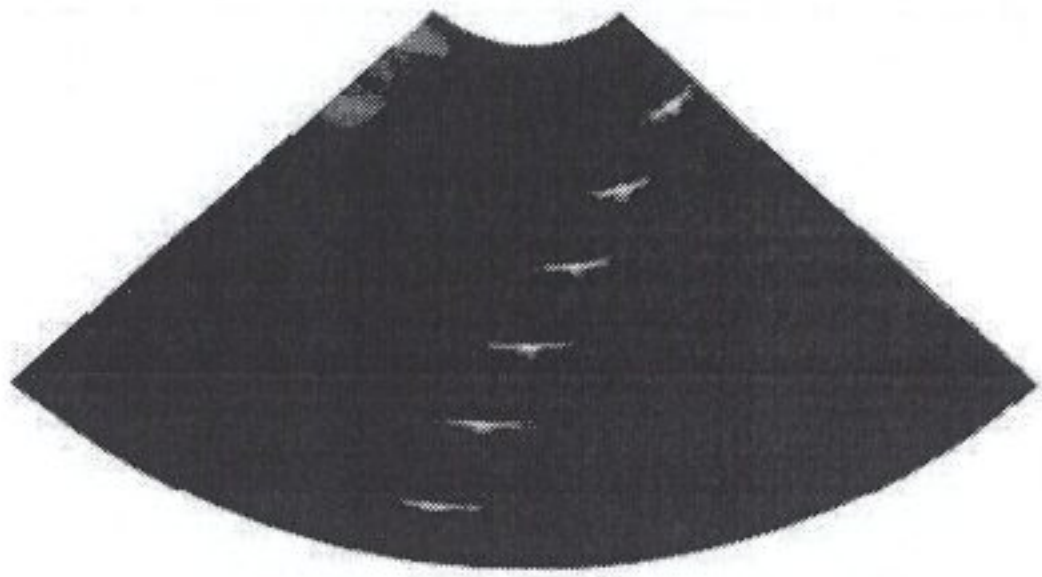
CMUT's applications are only limited by the imagination of the design engineer. Today CMUTs occupy a vital role not only in conventional ultrasonic applications such as medical ultrasound [13], underwater imaging [14] etc; but also in extraordinary applications such as air coupled non - destructive evaluation [15], microphones with RF [16], optical detection schemes [17], smart microfluid channels [19], as well as atomic force microscope [20].



(a) (b)

Figure 1.10: Concept of 2D Imaging by 1D CMUT arrays, driving phase is shown in (a) and receiving phase is shown in(b)

In figure 1.10 the concept of 2D image reconstruction by using 1D CMUT arrays is depicted. In driving phase the array elements are driven with a digitally controlled delay to scan an area by steering the focus in desired direction. In receiving phase



With the courtesy of E.L. Ginzton Laboratory - Stanford

Figure 1.11: Reconstructed 2D image by using 1D CMUT arrays

the delay times between each returning echo is calculated and sent to digital block. In addition the amplitudes of the echoes are also converted to digital and stored. The amplitude and phase data is the used to create an acoustic image like shown in figure 1.11. If the arrays become two dimensional then it is possible to obtain 3D images as experimentally proved in [11], but since the capacitances of the cells reduced so much that these cells can not drive any load formed by interconnection layers due to charge sharing phenomenon. This fact reveals the primary reason of designing a front-end analog circuit to buffer the echoes. Without such circuit it is impossible to get any signal from transducers.

Chapter 2

FRONT-END TRANSDUCER INTERFACE DESIGN

The developments in the VLSI process technology over the last few decades made it possible to fabricate two dimensional CMUT arrays which can be utilized to construct three dimensional acoustic images. There are two fundamental problems associated with volumetric acoustic imaging: the excessive number of elements in 2D CMUT matrix (i.e. 128 $\times$ 128) makes it very difficult to route parallel signal and bias lines with conventional layout techniques. In addition, the dimensions of each cell, consisting of many parallel connected CMUTs, have to be smaller than the half of the wavelength, imposed by the well known Nyquist's sampling criterion. Transducers with small areas have capacitances in the order of parasitics difficult to measure. Parallel connection of many CMUTs and high DC voltage biasing increase the device capacitance and accordingly the efficiency and the sensitivity but it is not easy to find a process technology that permits high voltages on the wafer.

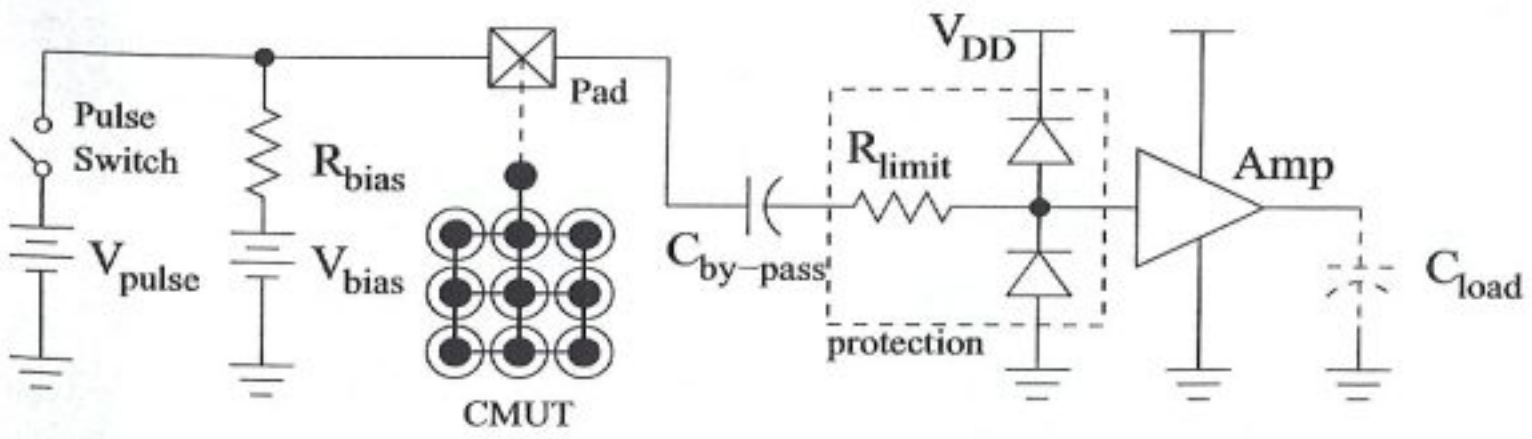


Figure 2.1: Abstract schematic of the system

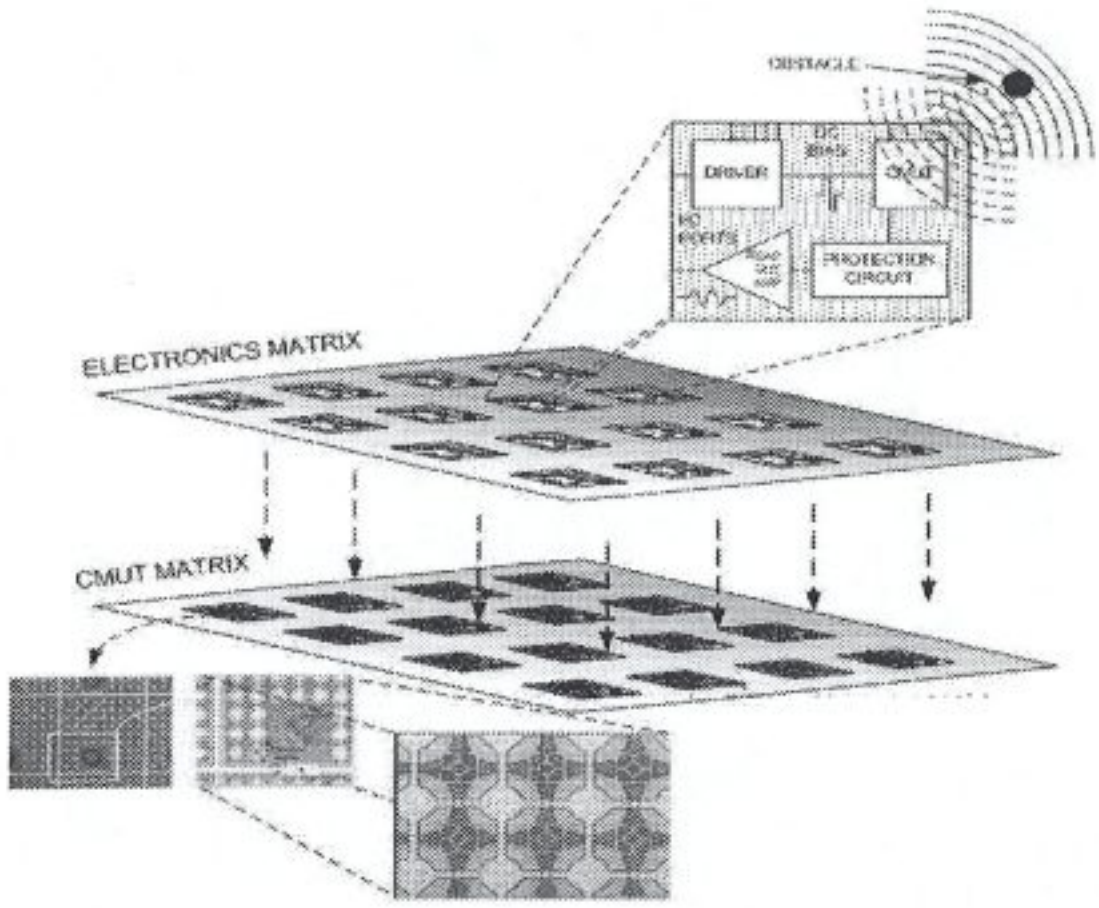


Figure 2.2: Conceptual representation of the system

The front-end interface circuit designed for 3D acoustic imaging contains 2D array of circuits each consisting of a driver circuit, a protection circuit, a read-out amplifier and a bonding pad for vertical connection to the same sized transducer matrix by flip-chip bonding method [22,23]as shown in figures 2.2 and 2.1. Operating frequency of the transducer is 3 MHz with full bandwidth, namely 1.5 - 4.5 MHz range and typical operating medium of water corresponds to 500 μm wavelength as shown in equation (2.1). Dimensions of the device are chosen as 200 μm, smaller than half of the wavelength, to satisfy Nyquist's criterion.

$$v = \lambda f \rightarrow \lambda = v/f = \frac{1500\ m/s}{3\ MHz} = 500\ \mu m \tag{2.1}$$

The most suitable process technology available to designer was Austria Micro System's (AMS) 0.8 μm 50 V high voltage technology which provides high voltage enabled MOSFETs (HVMOSFETs) that are operational up to 50 V as well as low voltage standard 5 V MOSFETs to the design engineer with two layers of metallization, two layers of poly-silicon and a highly resistive special layer. Since high voltage components occupy grudgingly wide area they are used only when there is no other option just like in the case of driver and high voltage protection circuit

design. Readout amplifier and driver preprocessing circuits incorporate standard 0.8 μm 5 V components.

2.1 Design of the Driver Circuit

The driver circuit has two functions: Generation of the appropriate driving signals for HVMOSFETs based on the external trigger signal that will result in a symmetrical mono-cycle at the output of the driver circuit. The second function is the level conversion of these signals to operate HVMOSFETs in their safe operating area (SOA).

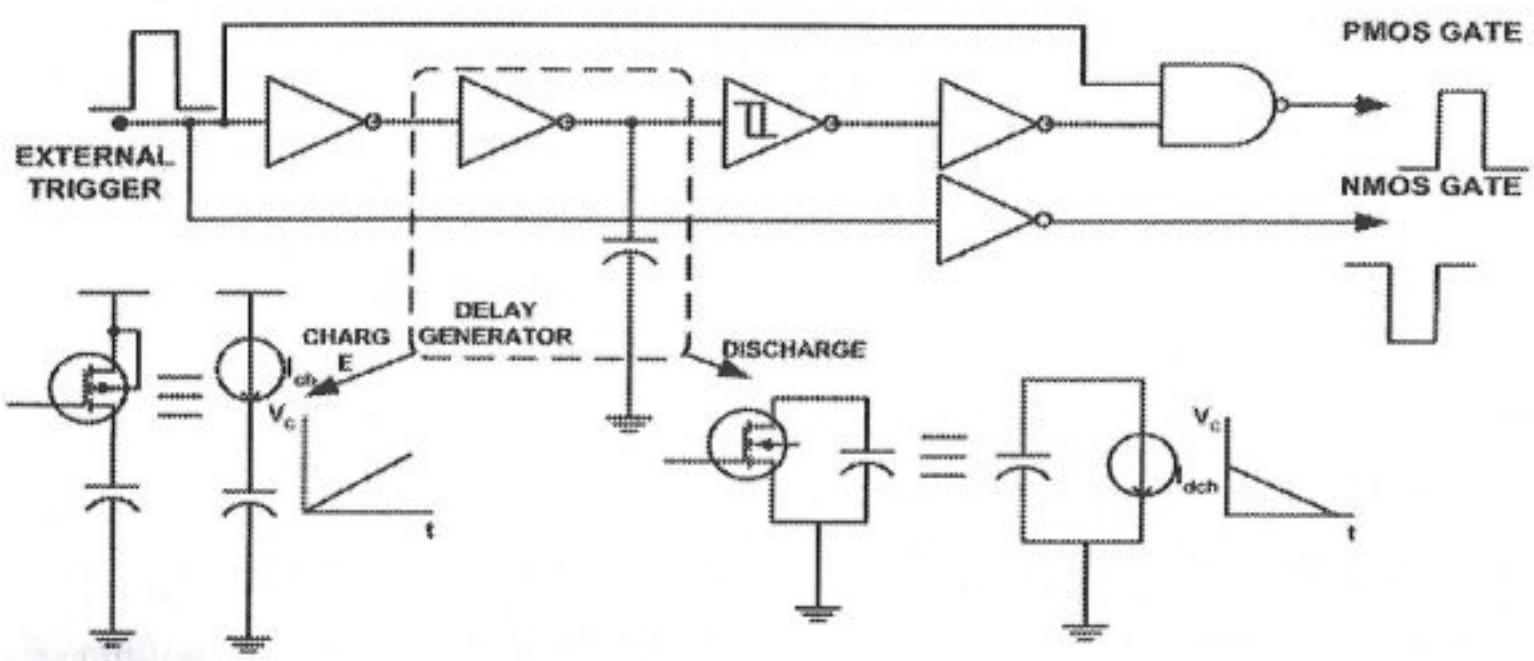


Figure 2.3: Abstract level schematics of the pulse preprocessor

2.1.1 Pulse Preprocessor

CMUT is driven by a push-pull configured complementary HVMOSFET pair. For the generation of a narrow monocycle pulse at the node where the CMUT is connected, proper timing and adjustment of the voltage levels are mandatory. While HVNMOS FET is driven synchronously with the external triggering pulse, HVPMOS FET is driven with an inverted pulse that has a delay of the pulse width of the applied trigger pulse. The delay is generated by charging/discharging a capacitor with a constant current source as shown in figure 2.3. A Schmitt trigger is designed and used to prevent chattering at the gate of HVPMOS FET.

Inverters and NAND gates are designed empirically while the design of schmitt triggered inverter deserves a special mention here. Schmitt trigger circuit shown in figure 2.4 is a well-known circuit and detailed information can be found in the literature [25–27].

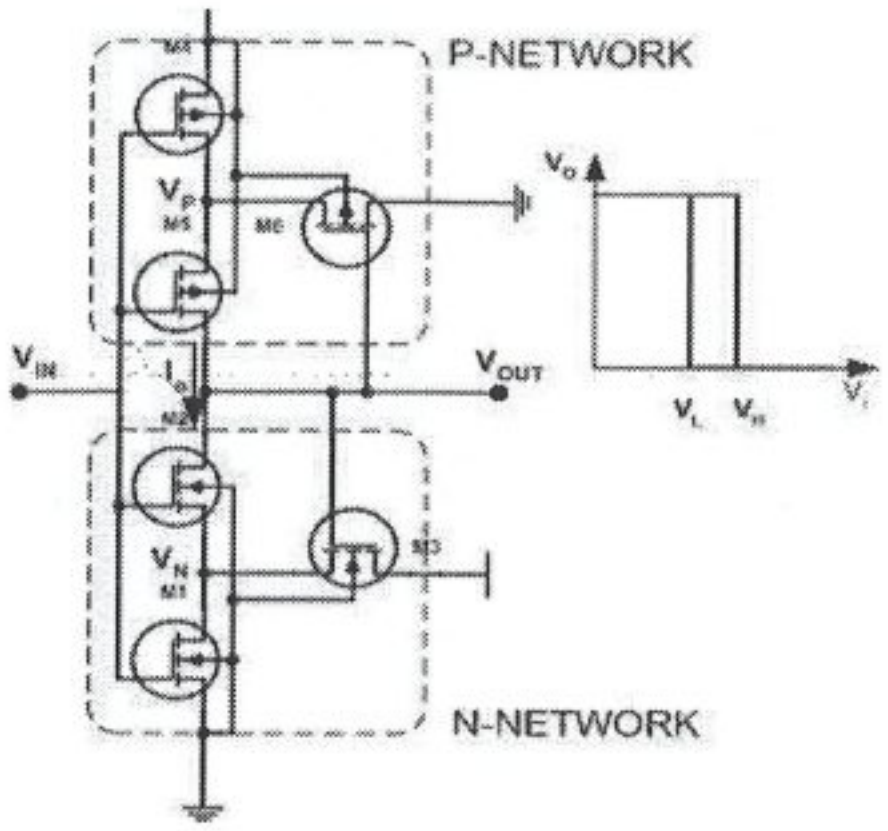


Figure 2.4: Schmitt trigger circuit topology

Assuming that a voltage source V_{out} is connected at the output of the Schmitt trigger while holding V_i at a constant dc voltage such that $V_i > V_TN$. For $V_o \cong 0\ V$, M3 will be turned off, M1 and M2 will be in the triode region. The current I_o for M1 and M2 can be expressed as

$$I_o = \beta_1 \left(V_{in} - V_{TN}\right) V_N \tag{2.2}$$

$$I_o = \beta_1 \left(V_{in} - V_N - V_{TN}\right) \left(V_{out} - V_N\right) \tag{2.3}$$

where

$$\beta_i = \mu_{n,p} C_{ox} \left(\frac{W}{L}\right)_i$$

and $V_{TN,TP}$ is the threshold voltage. For the triode mode of operation $V_N << V_{TN}$ and equation (2.3) can be simplified into

$$I_o = \beta_2 (V_{in} - V_{TN})(V_{out} - V_N) \tag{2.4}$$

From equations (2.2) and (2.4) V_N is calculated as

$$V_N = \frac{\beta_2}{\beta_1 + \beta_2} V_{out} \tag{2.5}$$

and

$$I_o = \frac{\beta_1 \beta_2 (V_{in} - V_{TN})}{\beta_1 + \beta_2} V_{out} \tag{2.6}$$

The output resistance can be calculated as

$$R_o = \frac{\partial V_{out}}{\partial I_o} = \frac{\beta_1 + \beta_2}{\beta_1 \beta_2 (V_{in} - V_{TN})} \tag{2.7}$$

It is observed from equations (2.5) and (2.7) that in this part of operation M1 and M2 are acting as resistors connected in series. When V_{out} is increased, M2 enters into saturation. Then I_o is determined by

$$I_o = \beta_1 \left(V_{in} - V_{TN} - \frac{V_N}{2} \right) V_N \tag{2.8}$$

and

$$I_o = \frac{\beta_2}{2} (V_{in} - V_{TN} - V_N)^2 \tag{2.9}$$

From equations (2.8) and (2.9), it is possible to conclude that

$$V_N = (V_{in} - V_{TN})(1 - \sqrt{\frac{\beta_1}{\beta_1 + \beta_2}}) \tag{2.10}$$

and does not depend on V_{out}. This means that when

$$V_o = V_{in} - V_{TN}$$

the current I_o becomes constant and equals to

$$I_o = \frac{1}{2} \frac{\beta_1 \beta_2}{\beta_1 + \beta_2} (V_{in} - V_{TN})^2 \tag{2.11}$$

If V_{out} is increased further, it will gradually affect the operation when V_{out} is

$$V_o = V_{in} - (V_{in} - V_{TN}) \sqrt{\frac{\beta_1}{\beta_1 + \beta_2}} \tag{2.12}$$

The transistor M3 will be completely turned on. V_N starts to increase, and I_o starts to diminish. When V_{out} equals to

$$V_o = V_{in} + (V_{in} - V_{TN})\sqrt{\frac{\beta_1}{\beta_3}} \tag{2.13}$$

The transistor M2 is completely turned off and I_o becomes zero. At this point

$$V_N = V_{in} - V_{TN}$$

and M1 is entering saturation so its current will be

$$I_{M1} = \frac{1}{2}\beta_1(V_{in} - V_{TN})^2 \tag{2.14}$$

which is completely intercepted by M3. Additional increase of V_{out} up to V_{DD} will not change the current-voltage characteristic of the N-network. Assume that V_{in} is zero, then transistors M1 and M2 are turned off. Transistors M4 and M6 are in the linear mode of operation, but the voltage drop at each is zero because the current in M4 and M5 is equal to the current in M1 and M2. The output voltage V_{out} is equal to V_{DD}. Transistor M3 is on since its gate and drain voltages are equal, but it does not carry any current. When V_{in} rises above V_{TN}, M1 turns on and starts to conduct. The current of M1 is determined by equation 2.14. It is completely intercepted by M3 and the condition of the transistors in P-network does not change. However, V_N starts to decrease due to increased conduction of M1.

The triggering action takes place when V_{in} reaches V_H. At this point, due to simultaneous increase of V_{in} and decrease of V_N, M2 turns on. It is easy to see that if V_{DD} is substituted in equation (2.13) and V_H in V_{in}, the required relationship between the transistor parameters is revealed

$$\frac{\beta_1}{\beta_3} = \left(\frac{V_{DD} - V_H}{V_H - V_{TN}}\right)^2 \tag{2.15}$$

By the analogy between P and N-networks

$$\frac{\beta_4}{\beta_6} = \left(\frac{V_L}{V_{DD} - V_L - |V_{TP}|}\right)^2 \tag{2.16}$$

should be satisfied to ensure the triggering action when the input voltage is equal to V_L. To simplify the design process it is assumed that the transitions are very fast and the circuit does not operate in linear region. When M3 and M6 are large

transistors this can be achieved [24]. In order to generate sharp transitions, $\frac{\beta_2}{\beta_5}$ ratio should be kept constant and $\frac{\beta_2}{\beta_4}$, $\frac{\beta_5}{\beta_1}$ ratios should be increased simultaneously. The transfer characteristic of the designed Schmitt trigger is shown in figures 2.5 and 2.6.

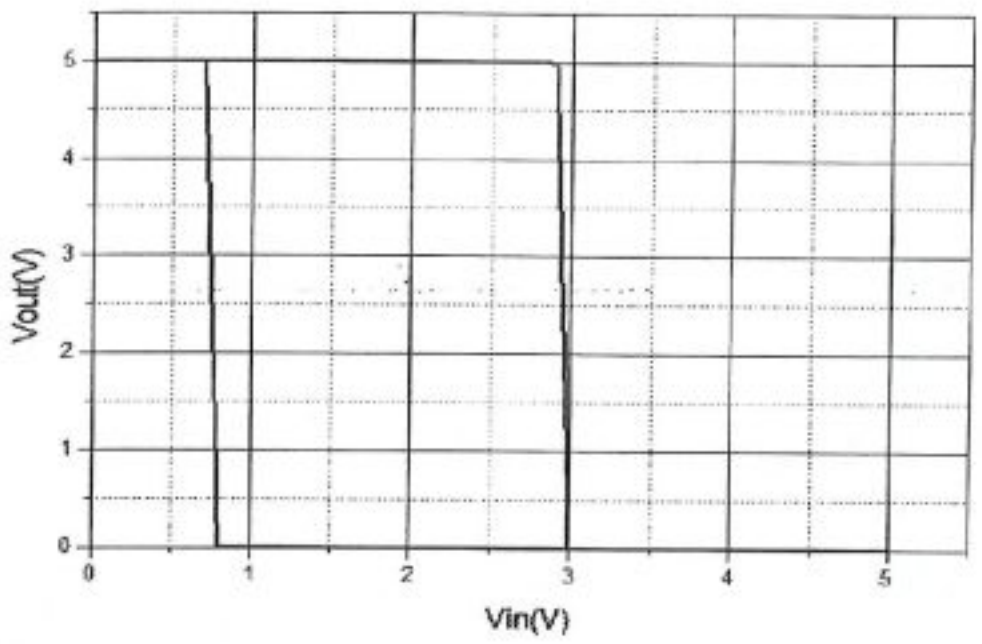


Figure 2.5: DC transfer characteristic of the Schmitt trigger circuit

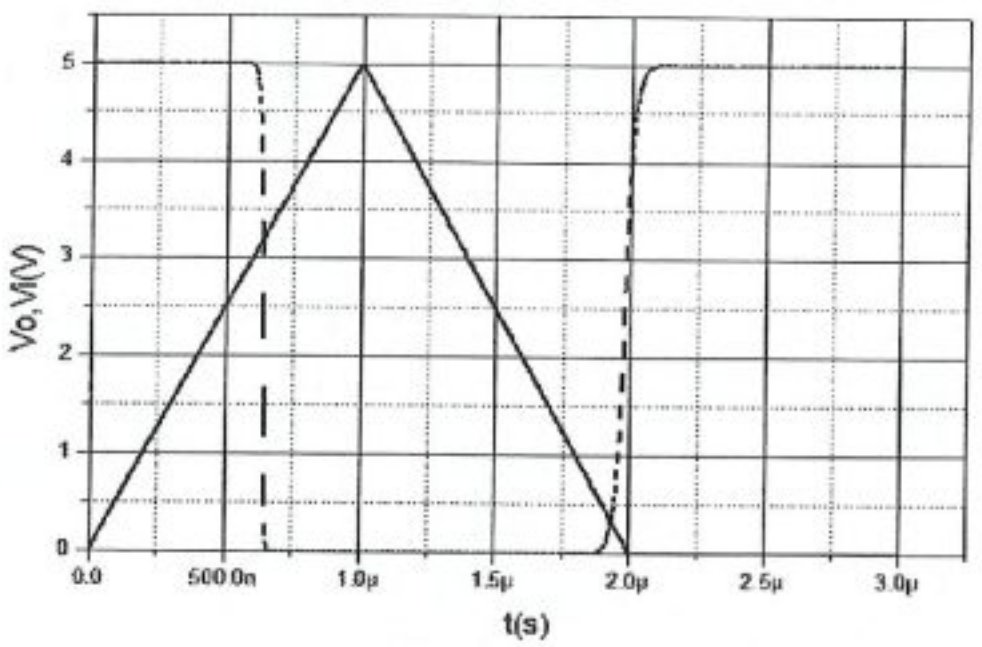


Figure 2.6: Transient response of Schmitt trigger circuit

2.1.2 Level Shifter

Level shifter is designed by utilizing the well known current mirror circuit which is based on the principle that if the gate-source voltages of two identical transistors are equal then the channel currents should be equal. The circuit topology shown in figure 2.7 contains a diode connected LVNMOS FET to bias a HVNMOS FET. For the most general case, taking channel length modulation into account the ratio of currents can be written as in equation (2.17). Since the currents are proportional to the size of the transistors, , the required voltage levels can be adjusted by proper sizing of the transistors and resistances. In the circuit a 0 to 5 V pulse will turn the diode connected LVNMOS FET on, since the gate to source voltages of the LV and HVNMOS FETs are equal, they are going to turn on and at the output the desired (45 V to 40 V) / (20 V to 15 V) pulse can be obtained. To decrease the channel length modulation effect lengths of the transistors should be selected greater than 3 μm.

Figure 2.7: Level shifter circuit schematics

$$\frac{I_2}{I_1} = \frac{W_2/L_2}{W_1/L_1}\left(\frac{V_{GS}-V_{T2}}{V_{GS}-V_{T1}}\right)^2\left(\frac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}}\right)\left(\frac{k_{n2}}{k_{n1}}\right) \tag{2.17}$$

Obviously the drain-source voltages will never be equal due to the voltage level requirements, thus channel length modulation will affect the currents, but its effect on level shifting is compensated by adjusting the sizes of transistors and resistors. The primary advantage of the current mode operation is speed. This topology is

faster than voltage mode level shifters.

2.2 Design of the Protection Circuit

The driving circuit generates high voltage pulses (45 V - 15 V) on the node where CMUT is connected. The readout circuit is designed for low voltage operation for making it feasible to fit inside cell area. If the inputs of the readout circuit is not protected then high voltage pulses can easily break the gate oxide of the input transistors of the readout circuit. To prevent this a protection circuit must be placed between CMUT and readout circuit. Its function will obviously be isolating the readout amplifier from the CMUT during driving (pulse phase) and connecting to the CMUT during reading (echo phase). The protection circuit may involve an external trigger control or it can be self-triggered. Throughout the design process two main approaches are developed.

2.2.1 Active Circuit Approach

The active protection circuit has external triggering capability that brings numerous advantages and disadvantages. One advantage is that the false echoes reflected from the substrate as mentioned in chapter 1 can be avoided by proper timing of the switch. This advantage appears with the cost of additional timing calculation load for the digital signal processing block which is not implemented yet. Timing is critical and any timing errors can yield in permanent damage to amplifiers. In addition, one drawback of this approach is the requirement of control lines which complicates the layout. Four possible switch topologies were investigated, their dynamic R_{DS} characteristics over the full pulse range is shown through figure 2.8 - 2.11.

Figure 2.8 and figure 2.9 shows the respective dynamic resistance of a single HVPMOS transistor and a single HVNMOS transistor over the full pulse range. The change in the resistance is non-linear. They were not intended to be used but only included for comparison purposes only.

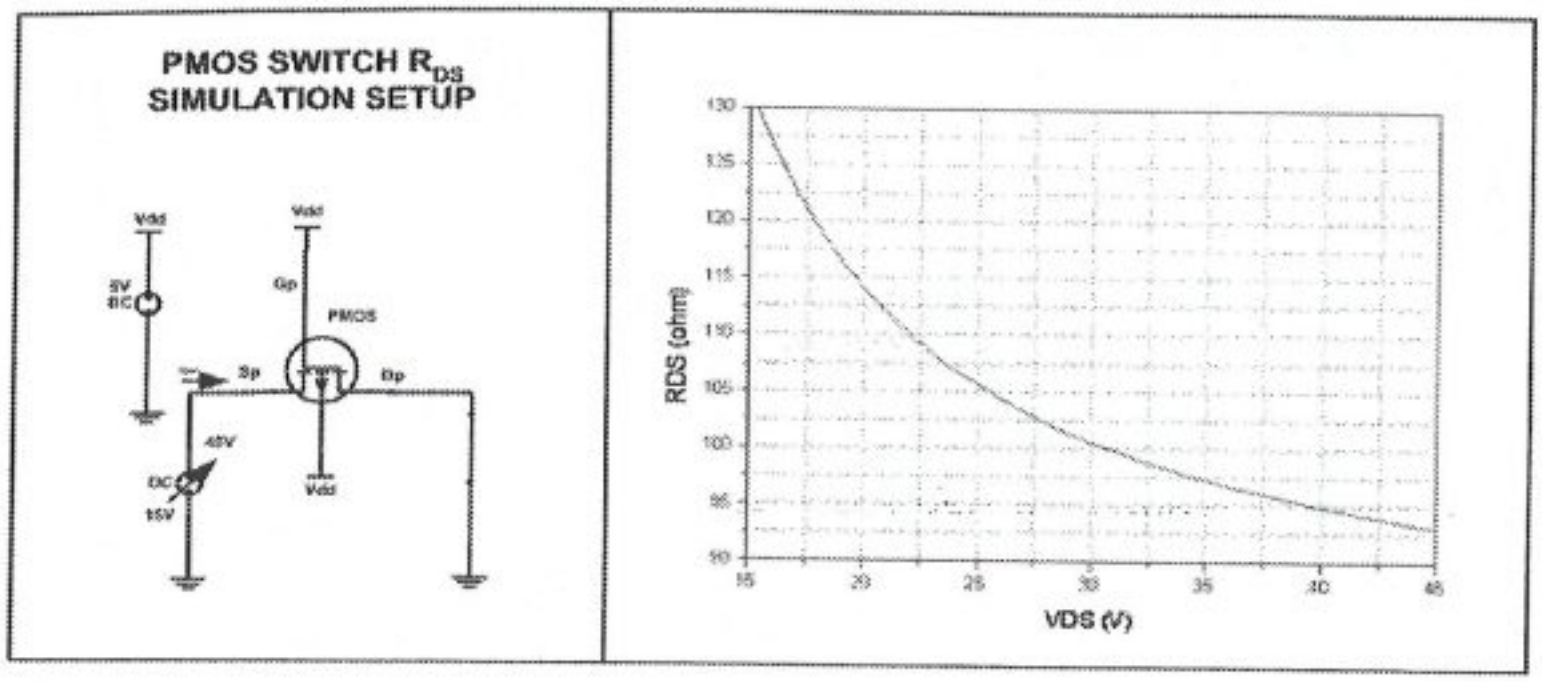


Figure 2.8: Single HVPMOS FET used as switch

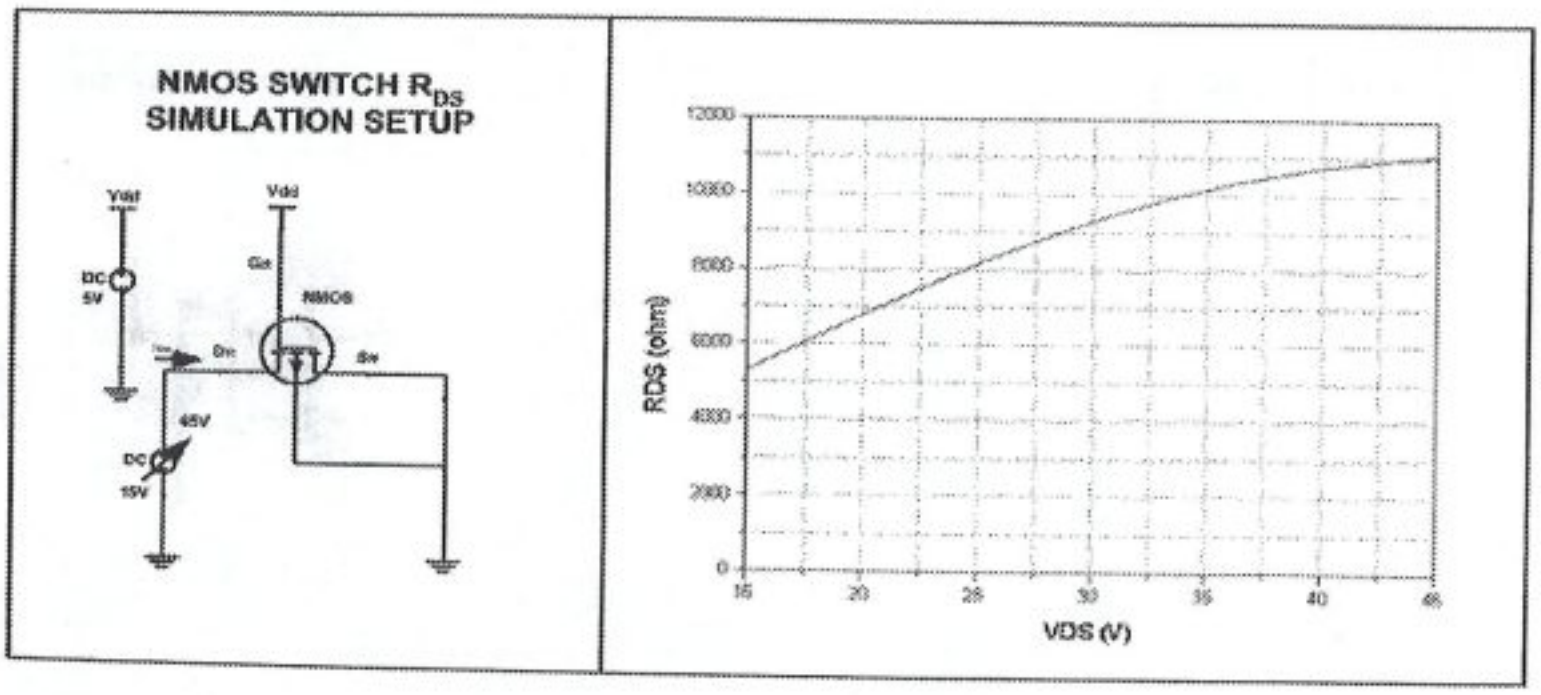


Figure 2.9: Single HVNMOS FET used as switch

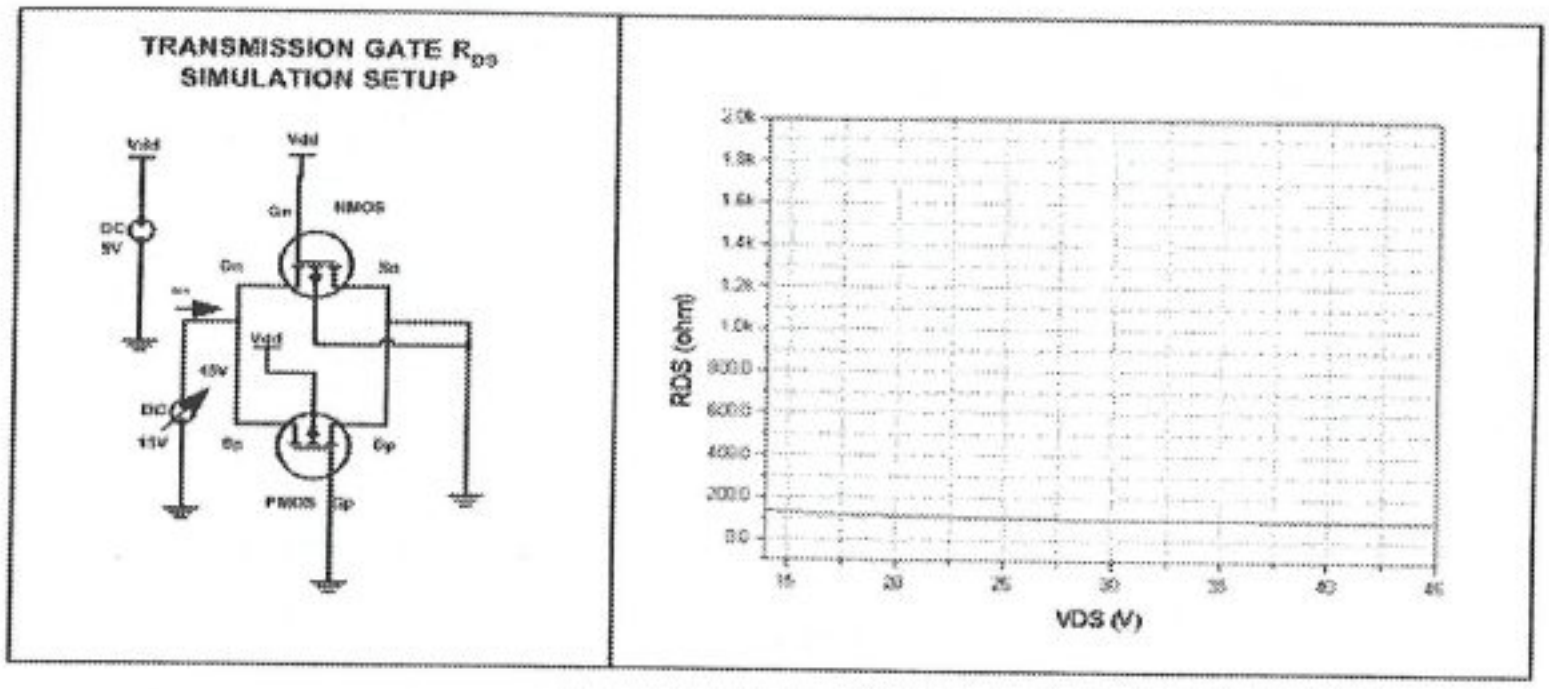


Figure 2.10: HVNMOS and HVPMOS FETs, connected in anti-parallel topology forming a transmission gate

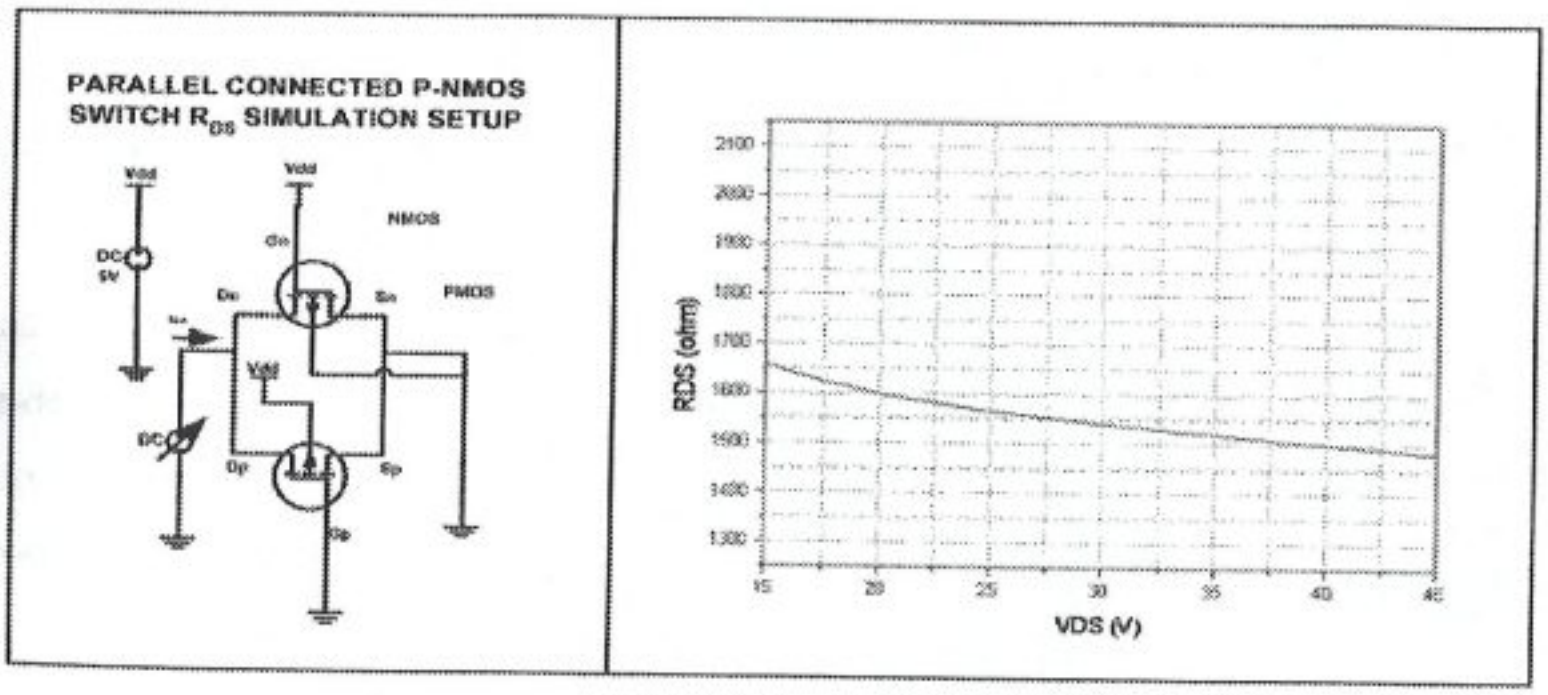


Figure 2.11: HVNMOS and HVPMOS FETs, connected in parallel topology to satisfy SOA requirements

Although transmission gate topology provides the most invariant resistance it could not be used. HVPMOS and HVNMOS transistors are connected in anti-parallel topology (source-drain, drain-source) as shown in figure 2.11 and the technology does not permit more than 5.5 V for V_{GS}, PMOS transistors would fail since their V_{SG} will be around 40 V. If R_{DS} invariance is sacrificed a little for the sake of SOA by connecting HVNMOS and HVPMOS transistors in parallel, acceptable performance could be achieved. Unfortunately other problems associated with the capacitances of the MOSFETs arise then, one of them is the well-known capacitive feedthrough phenomenon in which the high frequency components of the pulse on the edges could easily couple to the inputs of the amplifier through the gate-source and gate-drain capacitances as the name suggests. Also the coupling capacitor, R_{DS} of the switch,bias resistors and the input capacitance of the readout amplifier form a band pass filter that can easily attenuate the echo signal if not adjusted properly. The poles must be located at frequencies lower than 1.5 MHz and higher than 4.5 MHz to allow the passage of all components of the echo, switch transistors and input transistors are empirically adjusted. The problems associated with active protection circuit forced the designer to find a simple and effective solution for protection.

2.2.2 Passive Circuit Approach

Passive circuit approach makes use of the available avalanche diodes in the design libraries that are capable of standing up to typically 50 V in reverse bias. These diodes are used for electrostatic discharge (ESD) protection. Typical ESD protection circuits use the topology given in figure 2.12. Same topology can be used to protect the inputs of the readout amplifier.

The incoming signal will contain large and small signal components. From large signal point of view where $V_{in} >> \frac{kT}{q} = 25\ mV@27^oC$ if the magnitude of incoming signal is larger than the forward voltage drop of the diode, one of the diodes will conduct depending on the polarity of the voltage and eventually the inputs of the readout amplifier will be clamped to vdd or gnd. So the driving pulses will be

absorbed by these diodes. A series connected coupling capacitor that is formed by sandwiching layers that can stand high voltages as high as 50 V reduces the voltage stress on the diodes by blocking DC component of the signal so that 30 V to 45 V pulse on driving side will become 0 V to 15 V pulse on the readout side.

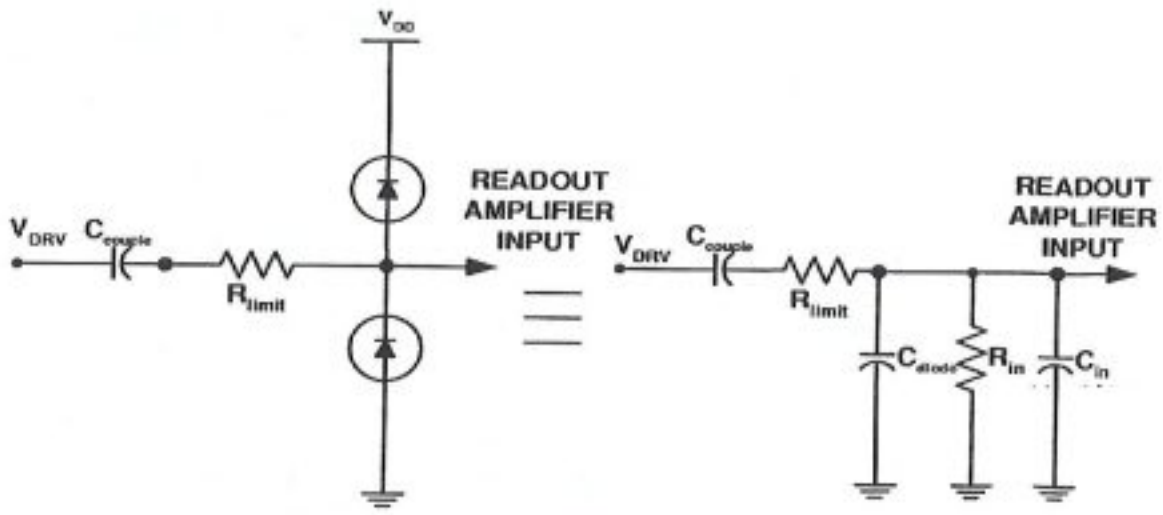


Figure 2.12: Typical ESD protection circuit

From small signal point of view where $V_{in} << \frac{kT}{q} = 25\ mV@27^oC$ coupling capacitor, the current limiting resistor, diode's junction capacitance,bias resistors and input capacitance of the amplifier will form a band pass filter that can attenuate the echo signal unless it is designed properly. Since the dimensions of the diodes are constant, only variable left to designer is the resistances and coupling capacitor. By adjusting the value of the resistance, the 3 dB frequencies of the filter can be set to values that will let all the frequency components of the echo signal within 1.5 MHz-4.5 MHz range. The second order bandpass filter will also be useful by limiting the noise bandwidth at the input of the readout amplifier.

2.3 Design of the Readout Circuit

Low noise OPAMPs are required where a large dynamic range is required. The dynamic range can be expressed as the ratio of signal to noise [29]. Most of the limitations of analog circuits are due to the fact that they operate with electrical variables and simply not with numbers. Therefore, their accuracy is fundamentally limited by noise, offset and distortions [30]. In addition to noise, the linearity of the OPAMP must also be considered. If the OPAMP is nonlinear then a pure sinusoidal

signal will generate harmonics. If the total harmonic distortion (THD) of these harmonics exceeds the noise, then nonlinearity becomes the limiting factor. Sometimes signal to noise plus distortion (SNDR) is used to include both noise and distortion in the dynamic range consideration [29]. In addition to these, power supply injection or charge injection due to switches, digital signals should also be considered. Low noise OPAMPs must have a sufficiently high power supply rejection ratio (PSRR) in order to achieve the desired lower limit of the dynamic range.

2.3.1 The Noise in CMOS Technology

CMOS operational amplifiers typically suffer from high levels of noise, especially at low frequencies. The $1/f$ noise component in a MOSFET is usually quite large due to current flow near the surface and the surface defects [31, 32]. In a typical two stage CMOS OPAMP, the equivalent input noise voltage is usually dominated by the equivalent input noise of the MOS input transistors of the differential input stage. The noise in a MOSFET is modelled as a mean square current generator in the channel as given below

$$i_N^2 = \left(\frac{8kTg_m(1+\eta)}{3} + \frac{K_F I_D}{fC_{ox}L^2}\right)\Delta f \tag{2.18}$$

Dividing by g_m^2 to obtain

$$e_N^2 = \left(\frac{8kT(1+\eta)}{3g_m} + \frac{K_F}{fC_{ox}WLk'_{n,p}}\right)\Delta f \tag{2.19}$$

Where

k: Boltzman Constant

T: Temperature in Kelvin

g_m: transconductance of the transistor

f: frequency

δf: bandwidth

C_ox: Oxide capacitance

W,L: dimensions of the transistor

$k'_{n,p}$: transconductance parameter in saturation

Equation (2.19) is valid for the case where the source of the MOSFET is on AC ground. For other cases equation (2.18) is used or effective g_m is calculated. The

first term in equation (2.19) is the thermal noise component and the second term is the flicker noise component. In many respects thermal noise of a MOSFET is equivalent to the thermal noise of a BJT, but the flicker noise of a MOSFET is much higher than that of a BJT. It can be felt that flicker noise is only important at low frequencies since it varies inversely with frequency. However, the flicker noise is aliased around clock frequencies and therefore becomes significant even at higher frequencies [29]. When MOSFETs are used to build a high frequency voltage controlled oscillator (VCO), the spectral purity of the sinusoid is limited among other things by flicker noise [36].

2.3.2 Noise Minimization Techniques

Minimization of noise had been one of the major issues in design of amplifiers. In multistage amplifiers the noise performance is determined solely by the first stage, since second and other stages' contributions are divided by the gain of the first stage, gain becomes an important parameter. In CMOS technology there are mainly two contributors of noise as shown in equation (2.19): Flicker noise and thermal noise. For flicker noise,there are basically three design approaches:

i) Minimization of the noise contribution of MOSFETs through circuit topology, operating conditions and component selection [29, 33–35]

ii) Use of external means, such as chopper stabilization [37]

iii) Replacement of input MOSFETs by lateral BJT counterparts [31]

2.3.3 Flicker Noise Minimization

The first approach to minimization of $1/f$ noise uses circuit topology and transistor selection: Empirically, PMOS transistors have about two to five times less flicker noise than the NMOS counterparts. It is reported that PMOS transistors exhibit the lowest possible flicker noise for a given gate area. In addition the high input impedance is one of the other advantages of MOSFET inputs. One of the key principles in minimizing flicker noise is to make the first stage gain as large as possible. This means that if the input is a differential amplifier, the source coupled transistors should be PMOS and the gain of the differential amplifier must be

as large as possible. It is found that the lengths of the load transistors should be greater than the lengths of the input transistors to minimize $1/f$ noise [29]. Since $1/f$ noise in a MOSFET is inversely proportional to square root of the gate area $\sqrt{WL}$, the flicker noise in a continuous time CMOS amplifier can be reduced by increasing the gate areas of the transistors, but inevitable penalties are greatly increased area requirements and large input capacitances [33–35].

The second approach is the chopper technique. The input signal is modulated by a square wave signal, mixing it to odd harmonics of f_{chop}. The modulated signal is then amplified and modulated back to baseband. The required hardware is not effective in terms of area.

The third approach utilizes the bulk CMOS compatible lateral BJTs which was first introduced in [31] and used in [32], [34], [35]. AMS 0.8 μm technology uses n-well diffusions in a p-type substrate, and the only available lateral transistors are PNP type as shown in Fig. 2.13. For proper bipolar operation, gate to emitter (source of PMOS) voltage of the lateral PNP (LPNP) transistor must be zero to disable the inherent PMOS transistor depicted in Fig. 2.14. Positive gate bias improves device noise performance by diffusing minority carriers in the base deeper into the n-well and away from surface defects thus reducing the flicker noise. The LPNP has two collectors, lateral and vertical as seen in Fig. 2.14. Total collector current will be their sum. Since lateral operation is desired, minimization of vertical collector current is required. This can be accomplished by connecting the gate of the device to maximum allowable voltage on the chip thereby creating an electrical field beneath the gate that attracts more electrons into the lateral collector.

2.3.4 Thermal Noise Minimization

The choices to reduce the flicker noise will also reduce the thermal noise once the equivalent input noise spectral density is known, the rms value of the noise can be found by integrating the input spectral noise density over the bandwidth. The noise corner where the thermal noise is equal to flicker noise can be found as below

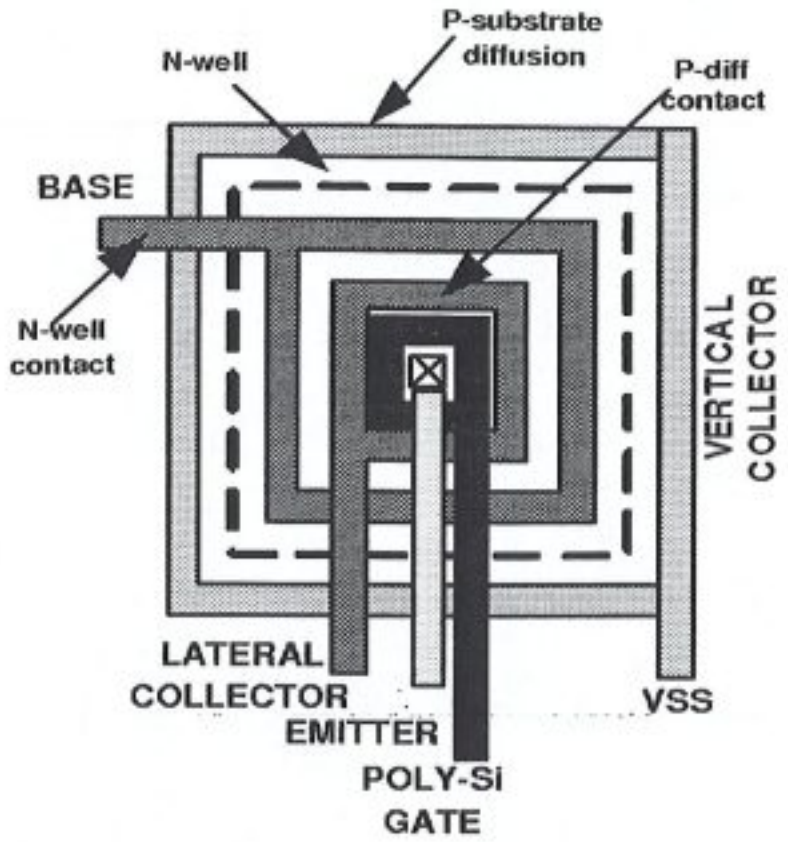


Figure 2.13: Layout of the lateral bipolar transistor

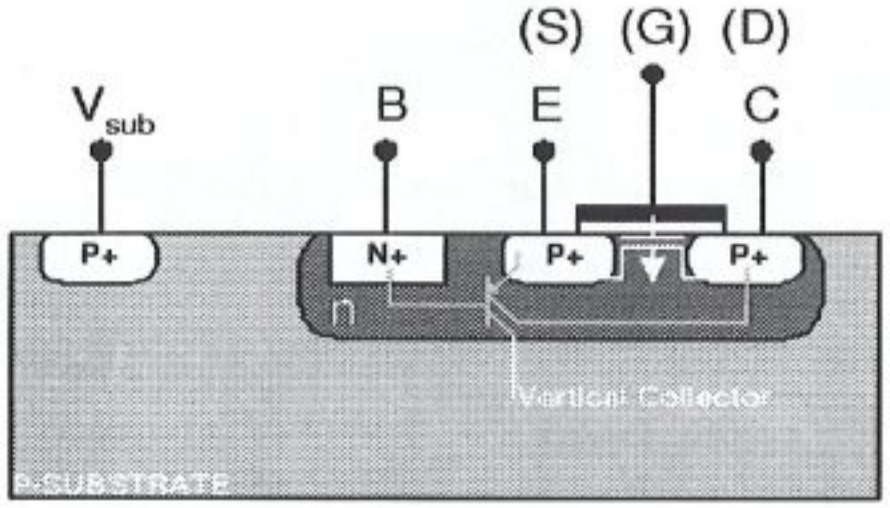


Figure 2.14: Cross sectional view of the lateral bipolar transistor and the PMOS transistor

in equation (2.20) for a single transistor:

$$f_c = \frac{3g_m B_W}{8kT(WL)} \tag{2.20}$$

To reduce thermal noise in OPAMPs g_m is required to be large according to equation (2.19). This can be achieved by high bias current or high aspect ratio (W/L) [29]. If the MOS transistors are deliberately operated near the subthreshold region at a high bias current, matching can be improved as a result of which lowering the total offset voltage of the whole stage as well as a high common mode rejection ratio is ensured. It is a good practice to introduce some voltage gain in the first stage of an amplifier in order to lower the contribution to the total input referred noise

and offset voltage of all subsequent stages. However, high-speed operation implies high frequency poles. This can prohibit the use of active loads because of their high output impedance. Small resistors can be used to introduce low gain in the order of 10 dB without sacrificing noise performance. As a result this design approach allows the reduction of the bias current of the second stage and consequently the total power consumption for a given noise level.

2.3.5 Layout Methods

Careful layout techniques should be used in order to reach good DC performance to minimize the effects of process and temperature gradients as well as mechanical constraints. The large input pair can be drawn in the center of the chip as a cross-coupled quad to minimize lithographic errors. A waffle-iron shape with diagonal metal lines minimizes source and drain access resistances for low noise performance. The overlap of source and drain connections with gate area is also minimized thus reducing the total input parasitic capacitance [34].

2.3.6 The Circuit Topology

The circuit topology to be used in the system has to be simple and must be effective in terms of certain performance parameters, one of which was the low noise operation. Due to strict area limitations two stage, amplifier topology shown in figure 2.15 is chosen.

The CMUT array is intended to be used with digital signal processing blocks. The digital signals can interfere analog signal through the substrate and power supply rails. To prevent this, the power supply rejection ratio (PSRR) of the amplifier must be maximized. The utilization of the cascode current mirror in the first stage, accomplishes high PSRR. Due to the large output resistance of the active load, the pole formed at the output of the first stage is at low frequencies. In addition, common mode rejection ratio is also increased. One of the other advantage is high gain. These parameters are improved by sacrificing the bandwidth by utilizing a cascode current mirror as the load to input transistors. Second stage is a classical common source amplifier, providing additional gain and buffering to the amplified

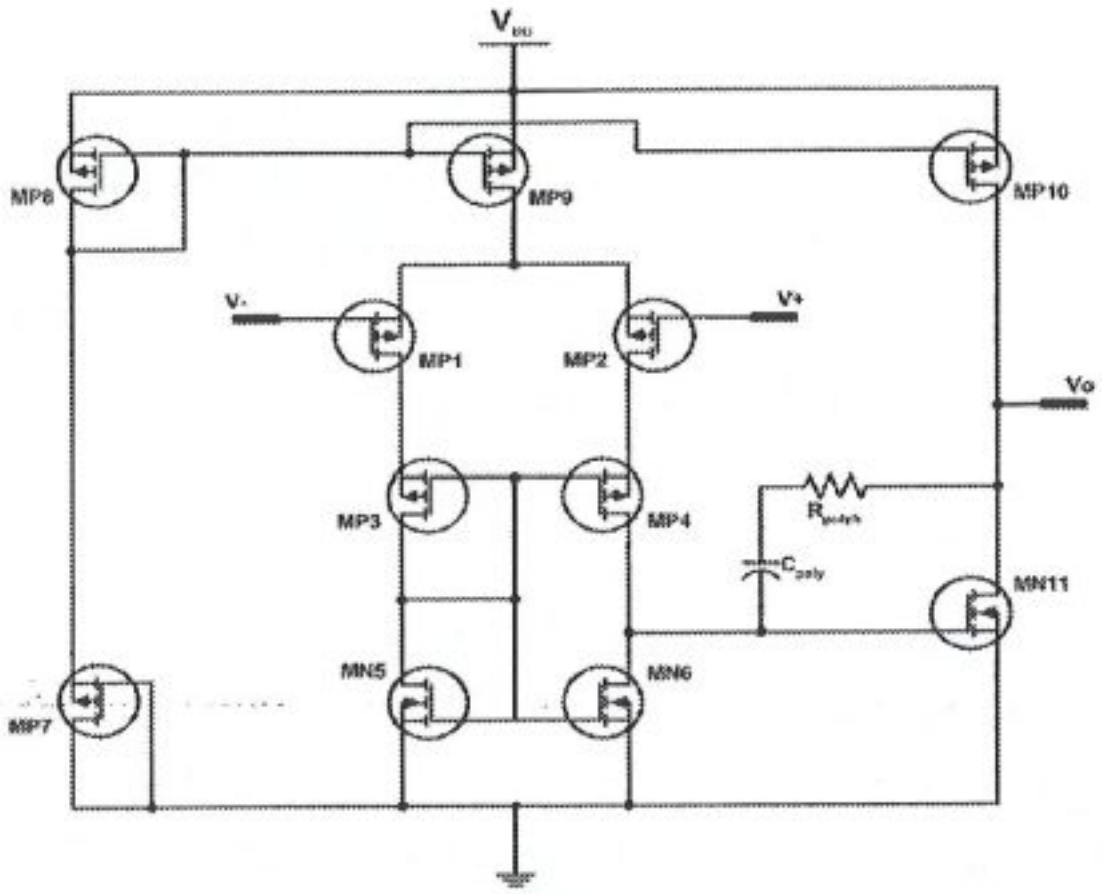


Figure 2.15: Circuit Topology of the readout amplifier

signal. The gain of the first stage is calculated to be

$$A_{v1} = g_{m1,2}R_{out} = g_{m1,2}(r_{o6}//(r_{o4} + r_{o2} + g_{m4}r_{o4}r_{o2})) \cong \tag{2.21}$$

$$= g_{m1,2}(r_{o6}//(g_{m4}r_{o4}r_{o2})) \cong g_{m1,2}r_{o6} \tag{2.22}$$

The cascode topology is empirically adjusted to provide high output resistance and because of this reason the gain is determined by M6's output resistance. For the second stage, the gain is calculated as

$$A_{v2} = g_{m11}(r_{o11}//r_{o10}) \tag{2.23}$$

And for the whole amplifier

$$A_{vo} = A_{v1}A_{v2} = g_{m1,2}g_{m11}r_{o6}(r_{o11}//r_{o10}) \tag{2.24}$$

As will be shown in the next chapter, a generic testbench is designed to obtain the specifications given in table 2.1.

Supply Voltage	5 V
Quiescent Current	132 μA
Power Dissipation	660 μW
Offset Voltage	1.2 μV
Gain Bandwidth Product	11 MHz (10 pF load)
Open Loop Gain	96 dB
Phase Margin	54^o ($C_L \leq 10\ pF$)
Common Mode I/O Range	$0.5 - 4.5\ V$
Common Mode Rejection Ratio	116 dB
+Power Supply Rejection Ratio	120 dB
-Power Supply Rejection Ratio	118 dB
Slew Rate	$7\ V/\mu s$
Equivalent input noise	$< 1.2\ uV/\sqrt{Hz}$@1 Hz
Equivalent input noise over the bandwidth: 1.5-4.5 MHz	20 $nV/\sqrt{Hz}$

Table 2.1: Characteristic parameters of the readout amplifier

2.3.7 Cell Layout

Layout of the cell requires some special approaches, for high voltage transistors their large size results in large C_{gs} values. This can alter the switching characteristics and introduce delay. Because charging and discharging intervals of C_{gs} become comparable to period of trigger signal. In order to minimize the C_{gs} of high voltage transistors source areas are minimized by drawing oval gated transistors with source being at the center. This design approached minimized the delays associated with C_{gs}s. To improve matching of the components resistors are laid out with unit cell approach.

Cell layout, prepared with Cadence Layout XL program, occupies 200 $\mu m \times$ 200 μm area. A special CMUT pad is designed with metal1 as the base and metal2 as the frame connected to metal1 base with vias in order to hold the solder bumps used in flip chip bonding method as seen in figure 2.16.

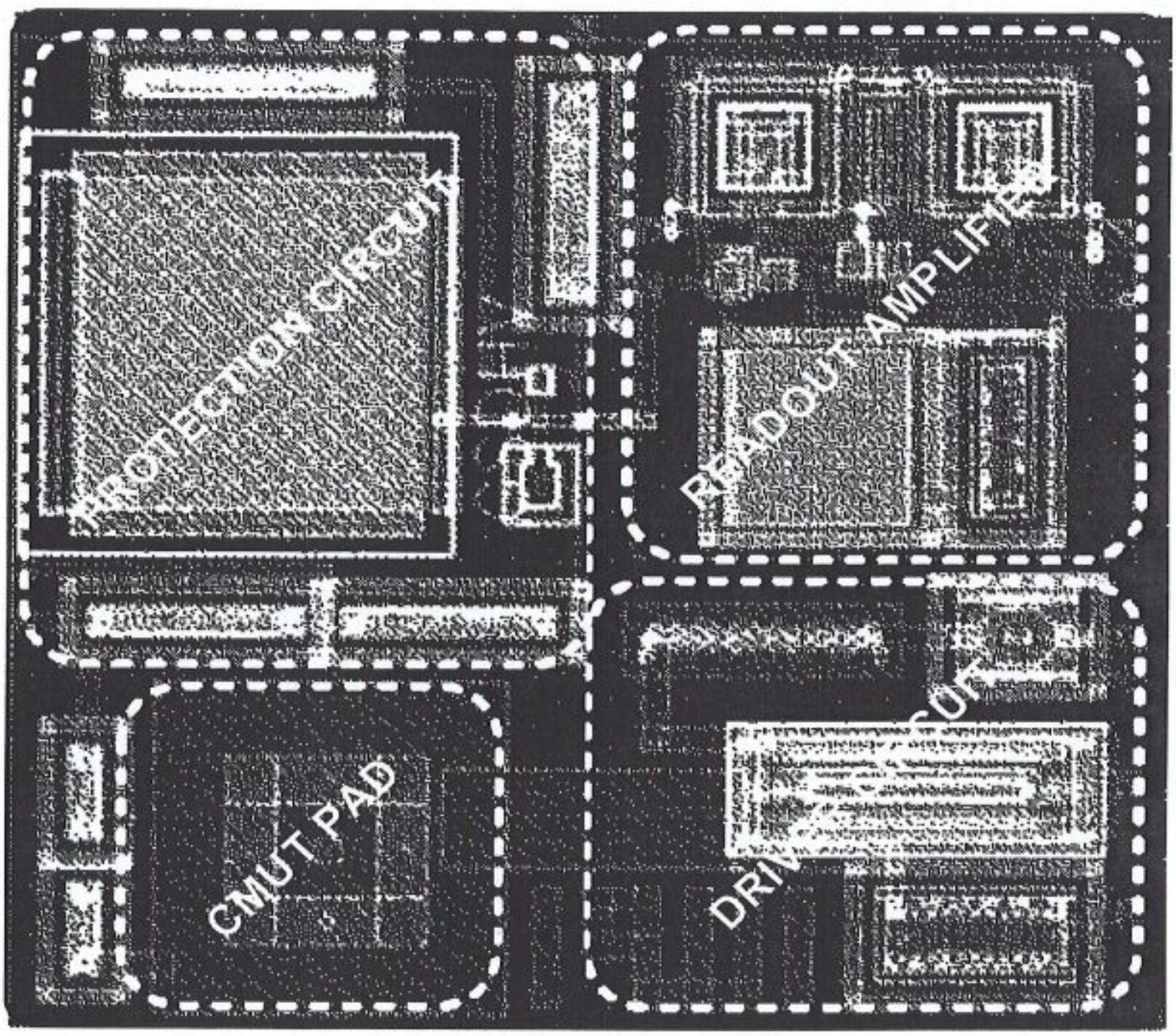


Figure 2.16: Layout of the experimental cell

Chapter 3

SYSTEM VERIFICATION

All system components are designed and tested separately, then circuits combined together to form the front-end cell, tested in time domain and in frequency domain.

3.1 The Driver Circuit

Driver circuit has a trigger input and two outputs to the gates of the HVNMOS and HVPMOS transistors. The simulation setup is given in figure 3.1 and simulation results are shown in figure 3.2. The trigger pulse has 100 ns pulsewidth, 1 ns rise and fall times, 1 μs period. Period is set longer than the pulsewidth to ensure the observation of returning echoes.

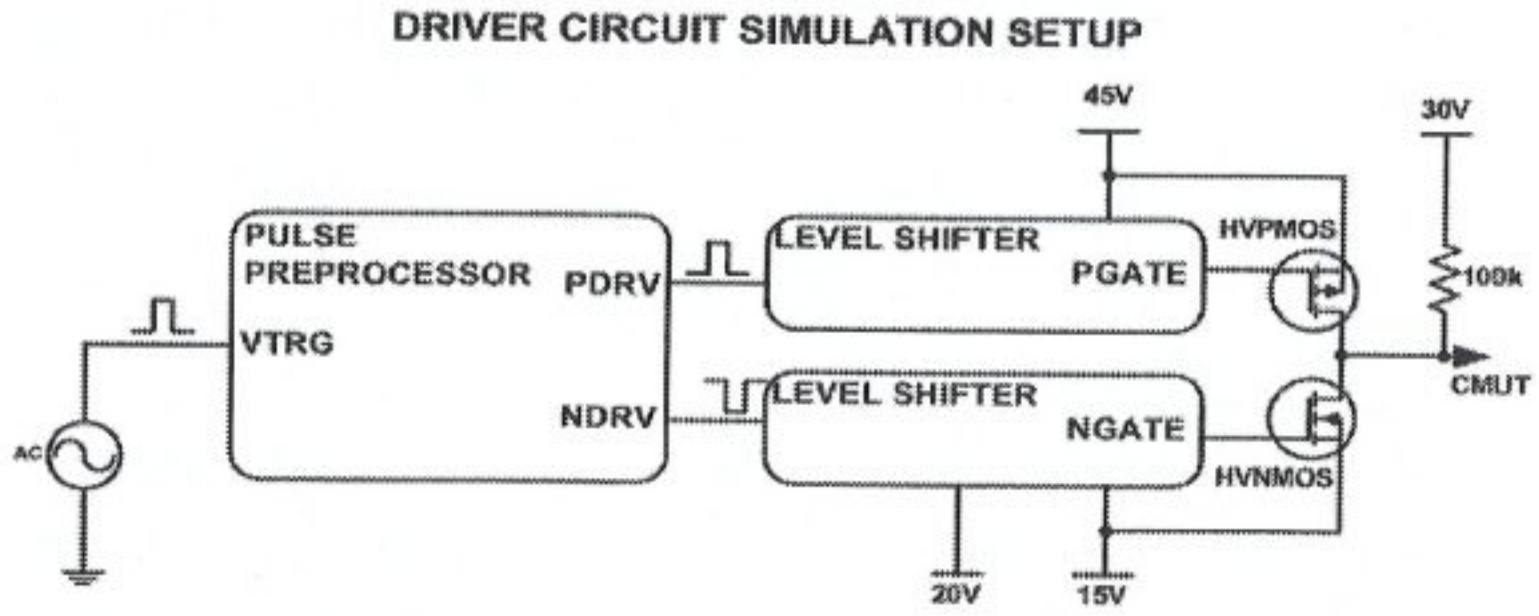


Figure 3.1: Simulation setup for the driver circuit

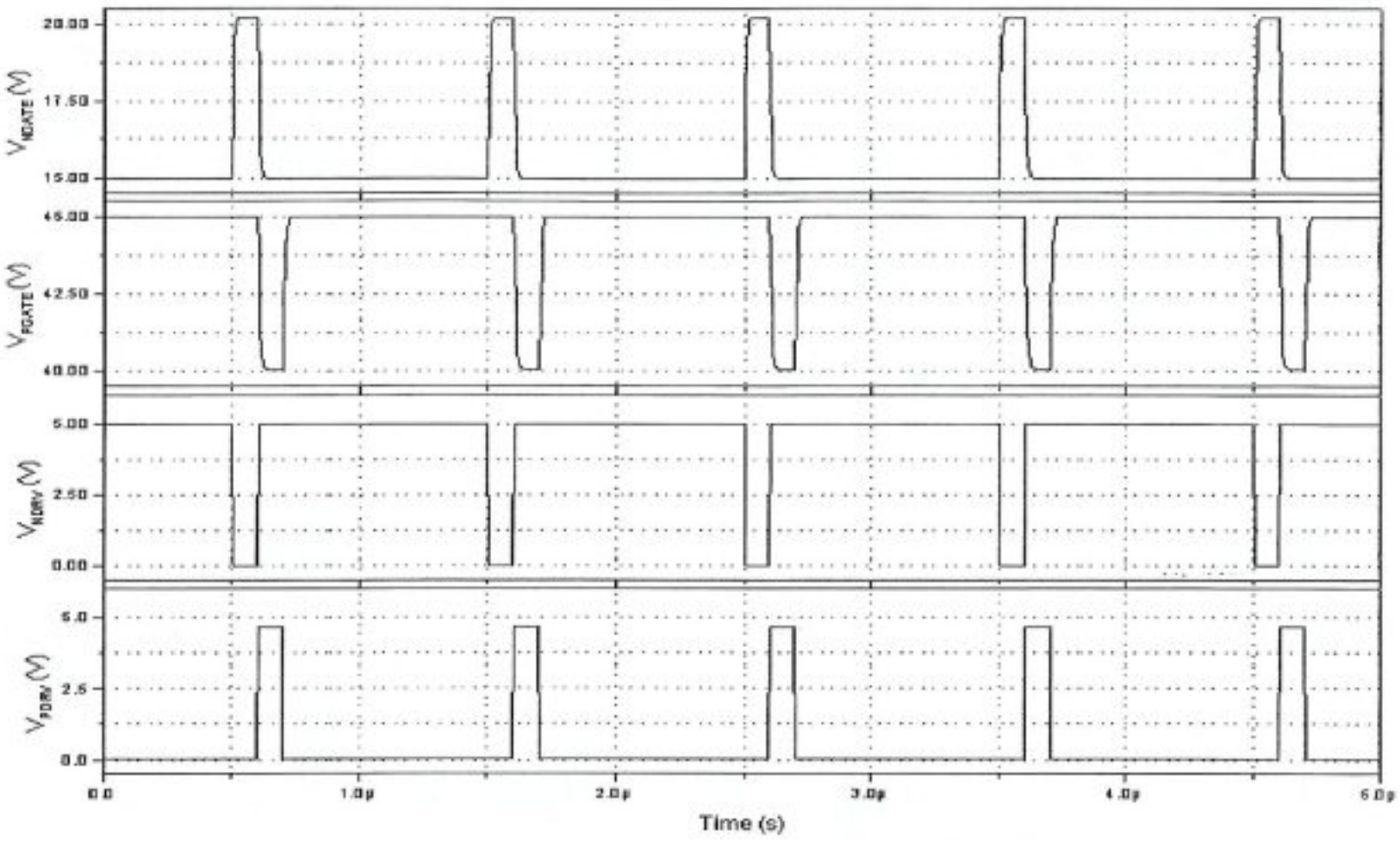


Figure 3.2: Simulation results for the drive circuit

3.2 The Protection Circuit

Protection circuit is the vital part of the system, its malfunction will result in a permanent damage to the readout amplifier, making the cell useless. Because of this reason it was tested fastidiously. The simulation setup shown in figure 3.3 was used for both transient and AC simulations. Results are shown in figure 3.4, it is clearly depicted that incoming signal would pass through the bandpass filter formed by the protection circuit and amplifier input as mentioned in chapter 2. Transient analysis results are shown in figure 3.5. The protection circuit's functionality is verified with the transient analysis.

The DC component of the drive signal V_{drv} is blocked by the coupling capacitor. Coupled signal V_{Co} has 30 V peak to peak amplitude which can easily damage the input transistors of the amplifier, but diodes clamp the excessive voltage to 5 V and GND with respect to signal polarity and protect the amplifier inputs. Small signal components will reach to the amplifier as verified in 3.4 while large signal components are attenuated.

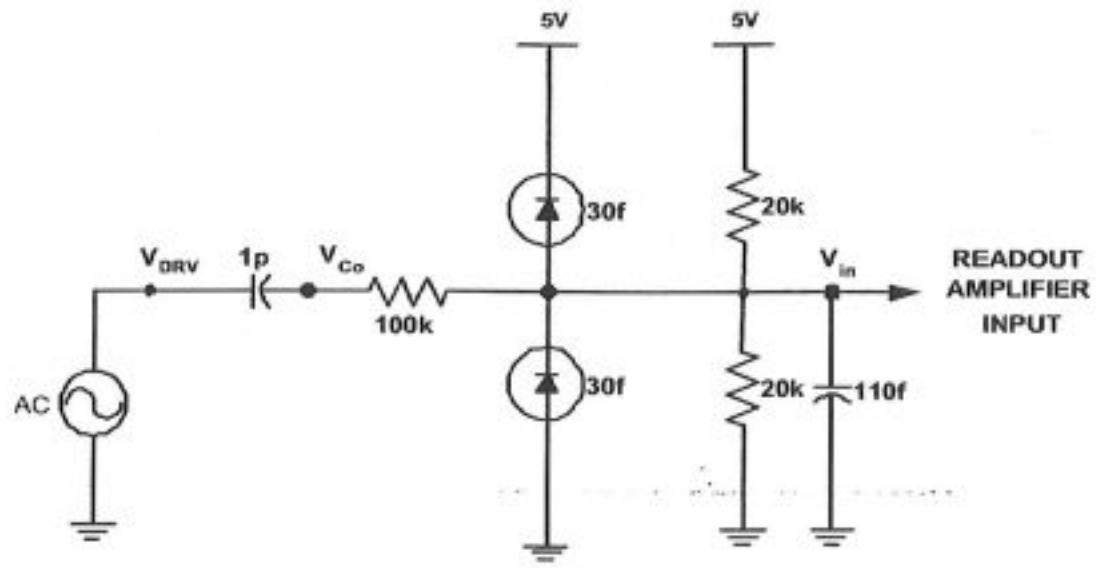


Figure 3.3: Simulation setup for the protection circuit

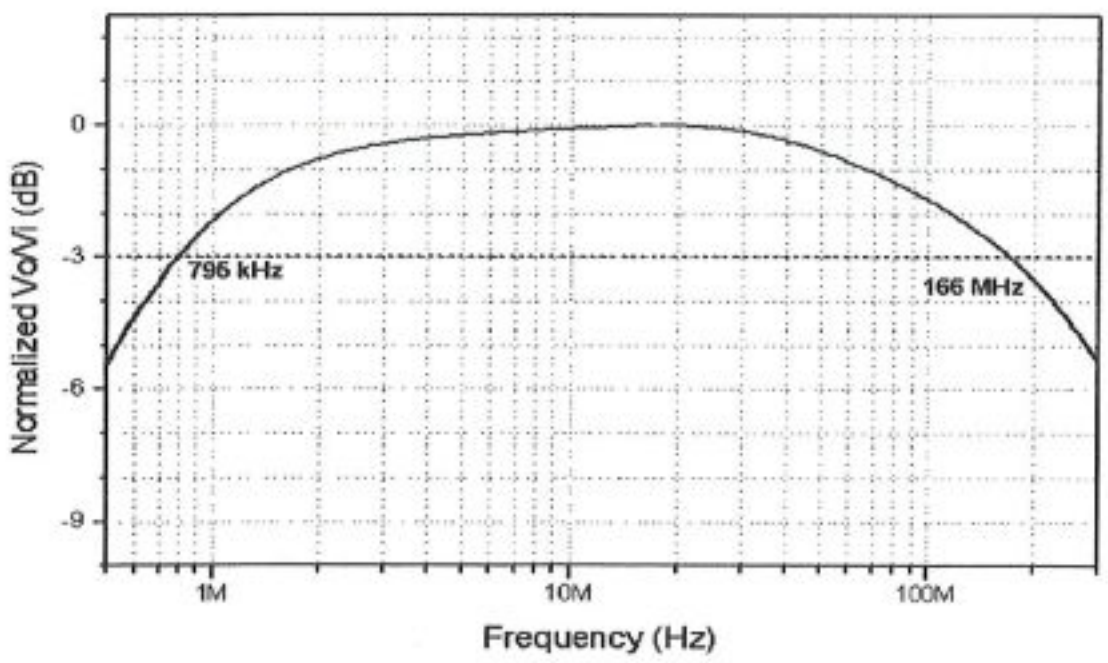


Figure 3.4: AC simulation results for the protection circuit

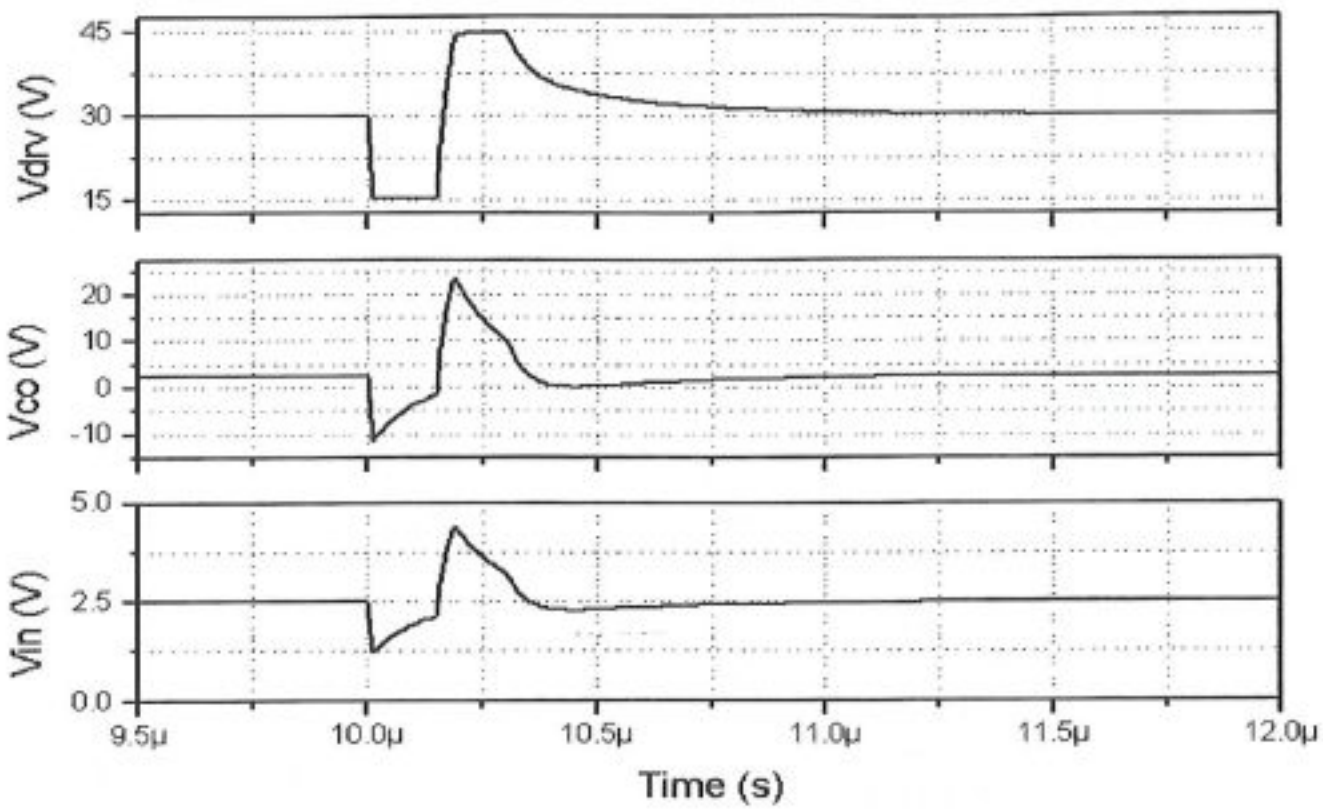


Figure 3.5: Transient simulation result for the protection circuit

3.3 The Readout Circuit

A generic test bench is designed to test any amplifier. Test bench contains the following measurement setups:

1) Offset voltage is shown in figure 3.6

2) Common input - output range is shown in figure 3.7

2) Gain, gain-bandwidth product and phase margin is shown in figure 3.8

3) Common mode rejection ratio (CMRR) is shown in figure 3.9

4) +Power supply rejection ratio (+PSRR) is shown in figure 3.10

5) -Power supply rejection ratio (-PSRR) is shown in figure 3.11

6) Equivalent input noise is shown in figure 3.12

7) Slew rate is shown in figure 3.13

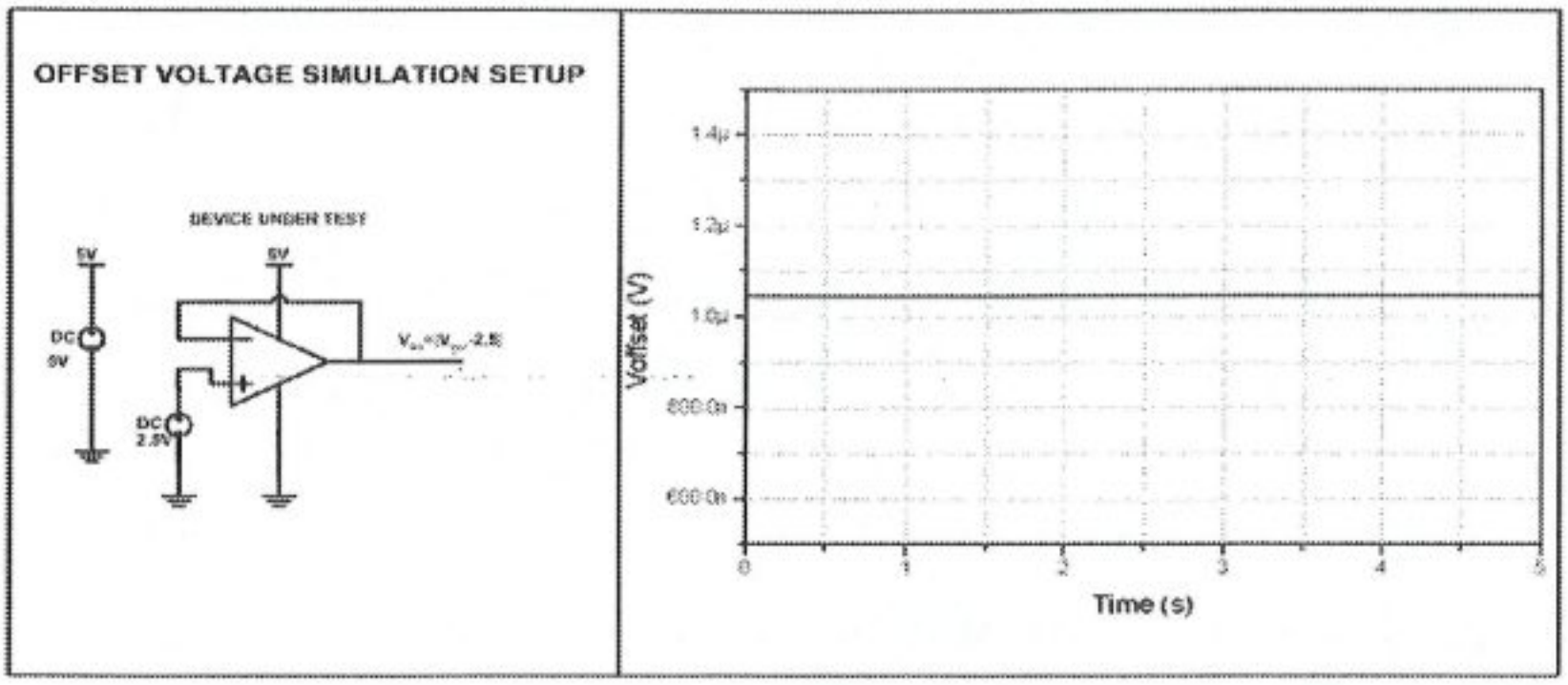


Figure 3.6: Offset voltage simulation setup and results for the readout amplifier

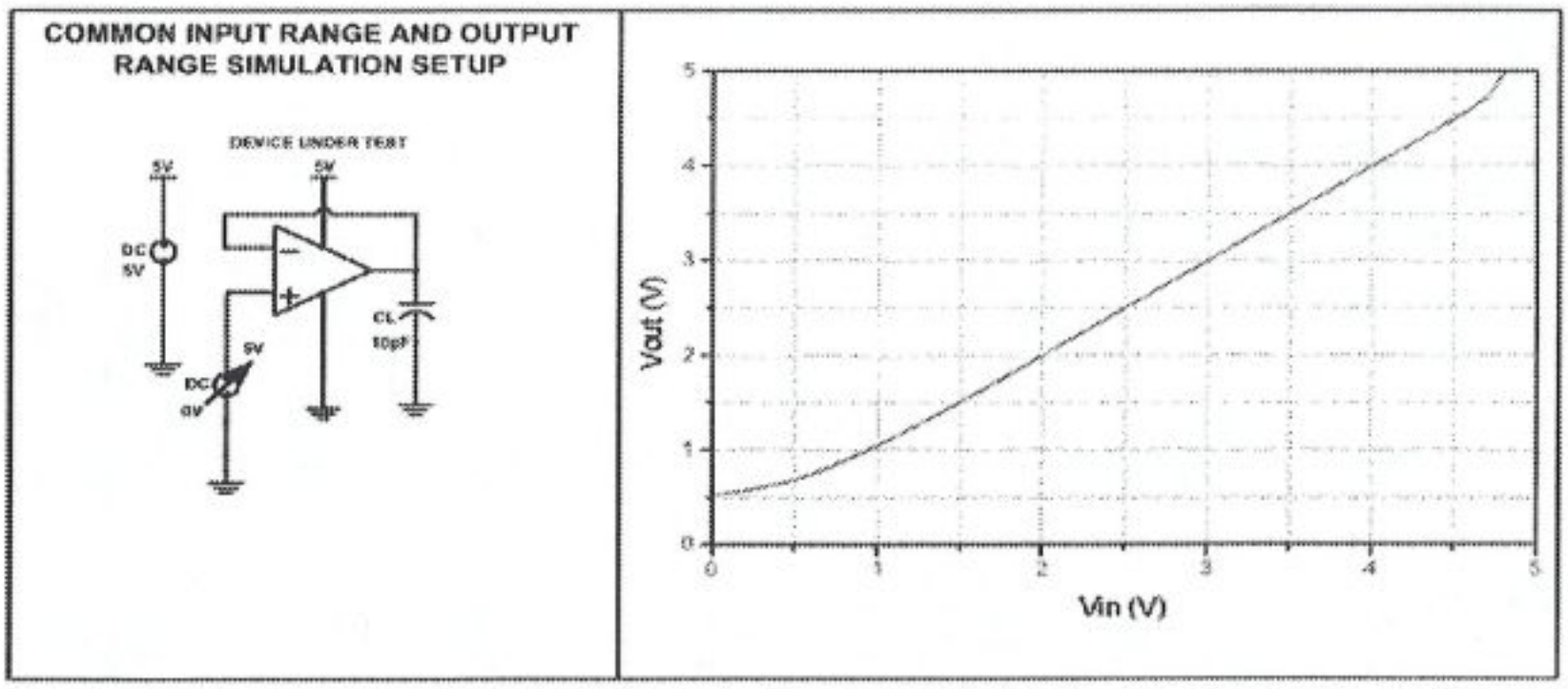


Figure 3.7: Common input output range simulation setup and results for the readout amplifier

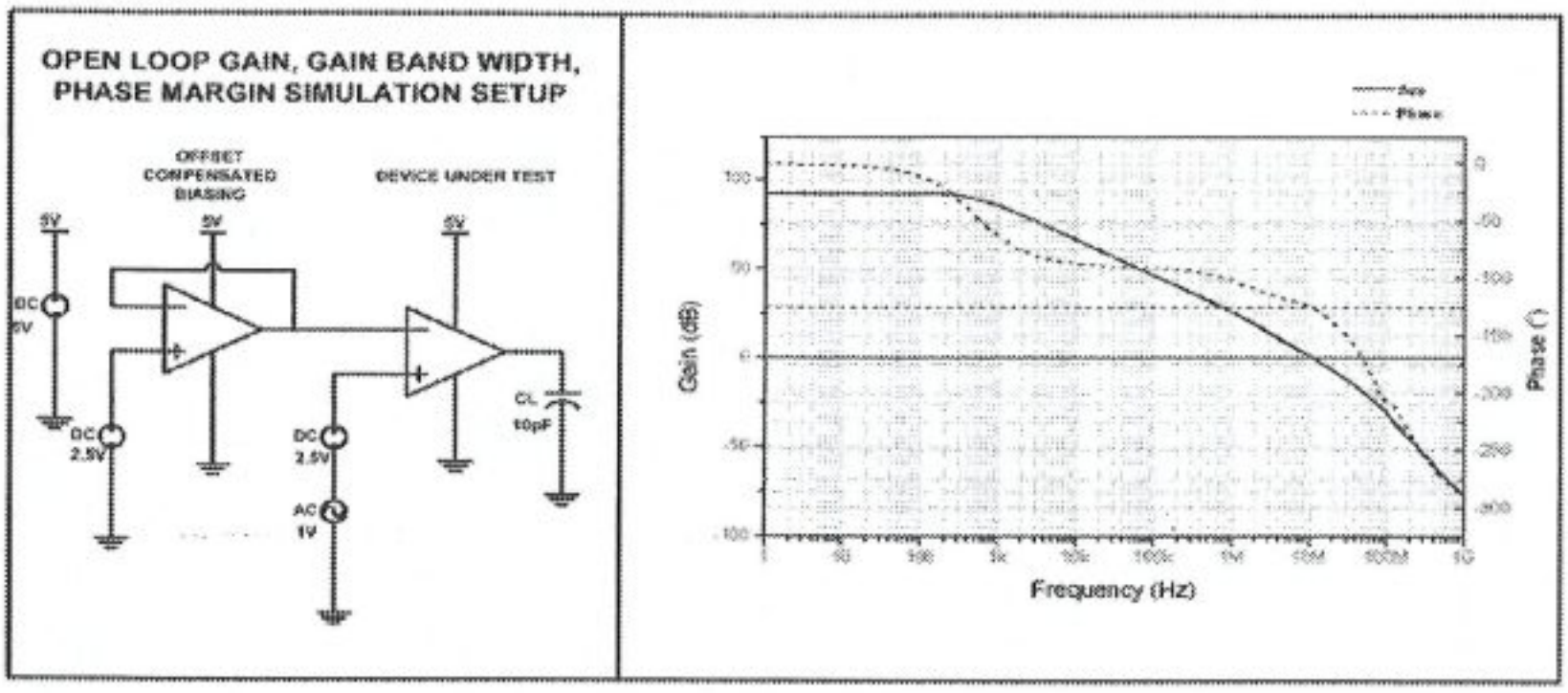


Figure 3.8: Gain, gain-bandwidth product and phase margin simulation setup and results for the readout amplifier

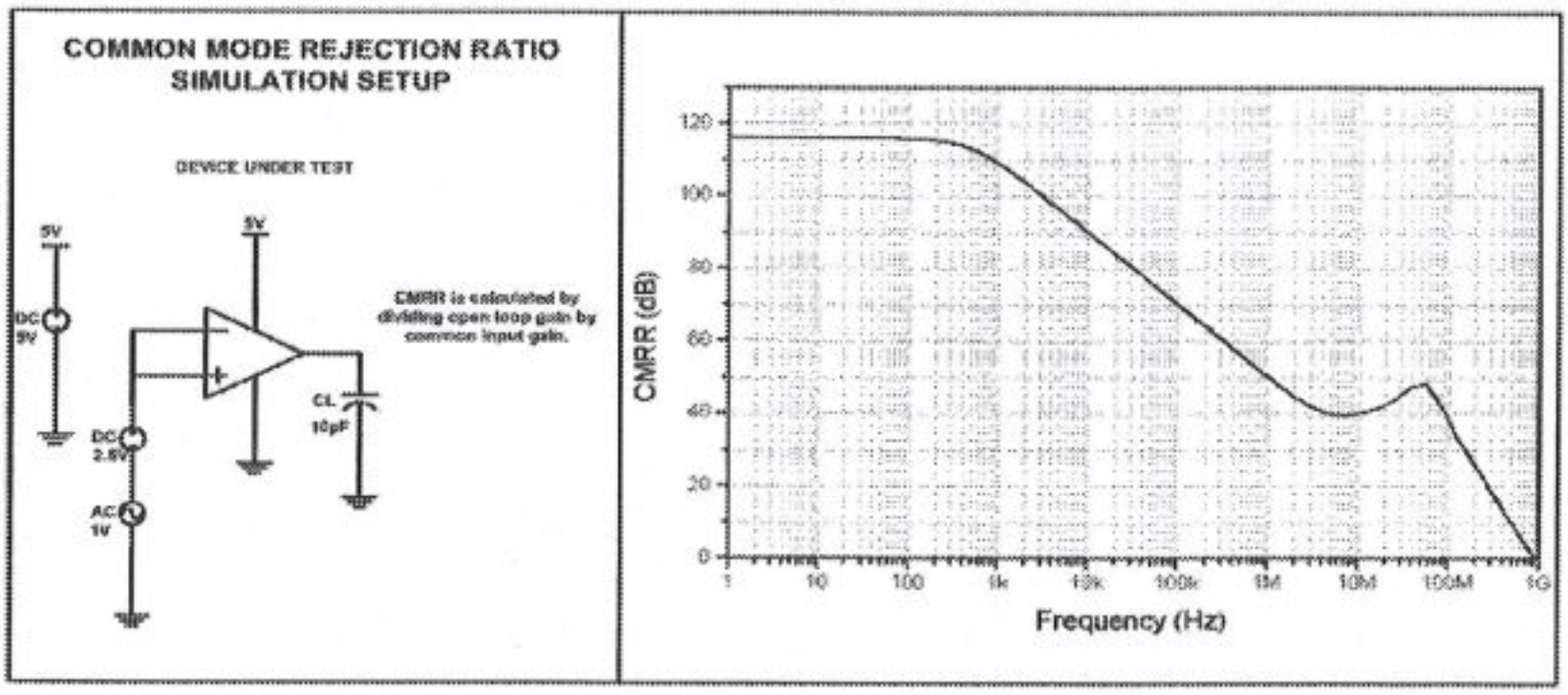


Figure 3.9: Common mode rejection ratio simulation setup and results for the readout amplifier

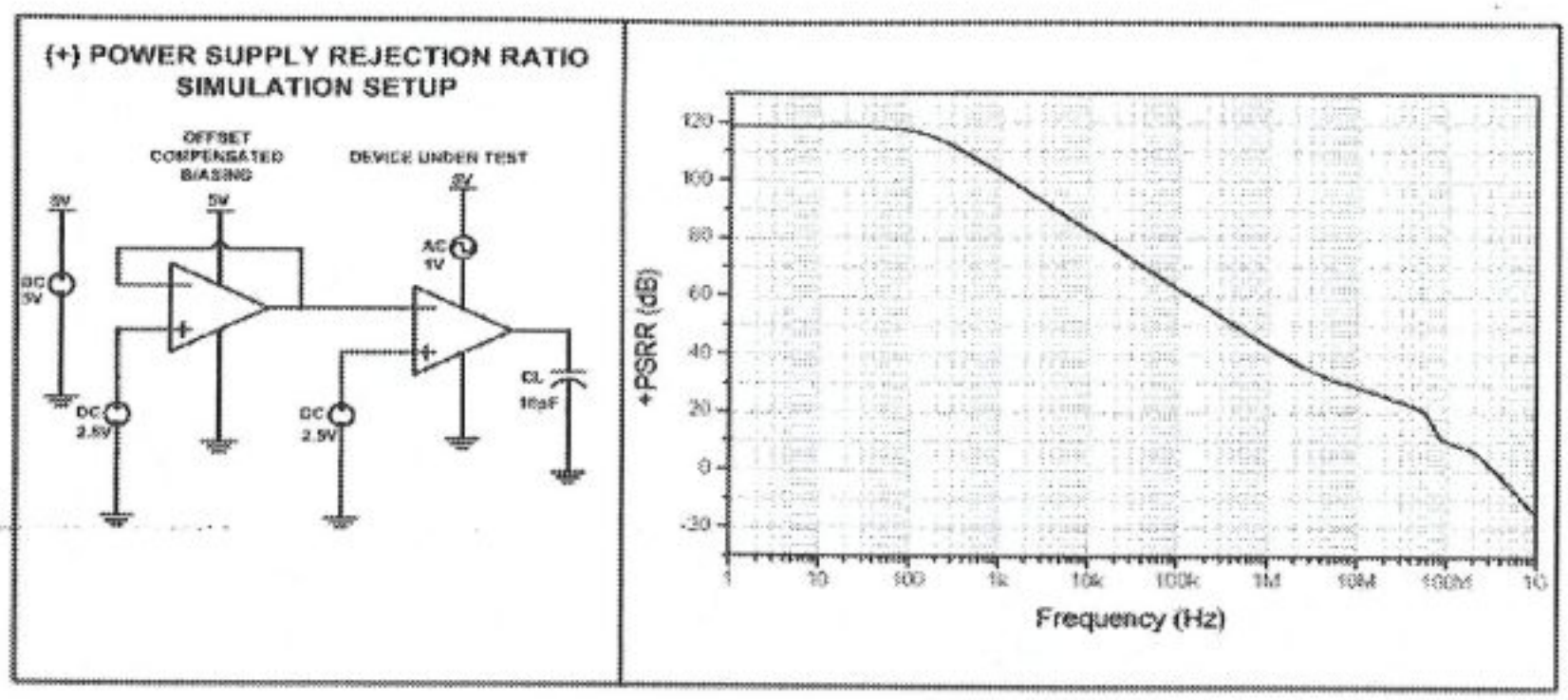


Figure 3.10: +Power supply rejection ratio simulation setup and results for the readout amplifier

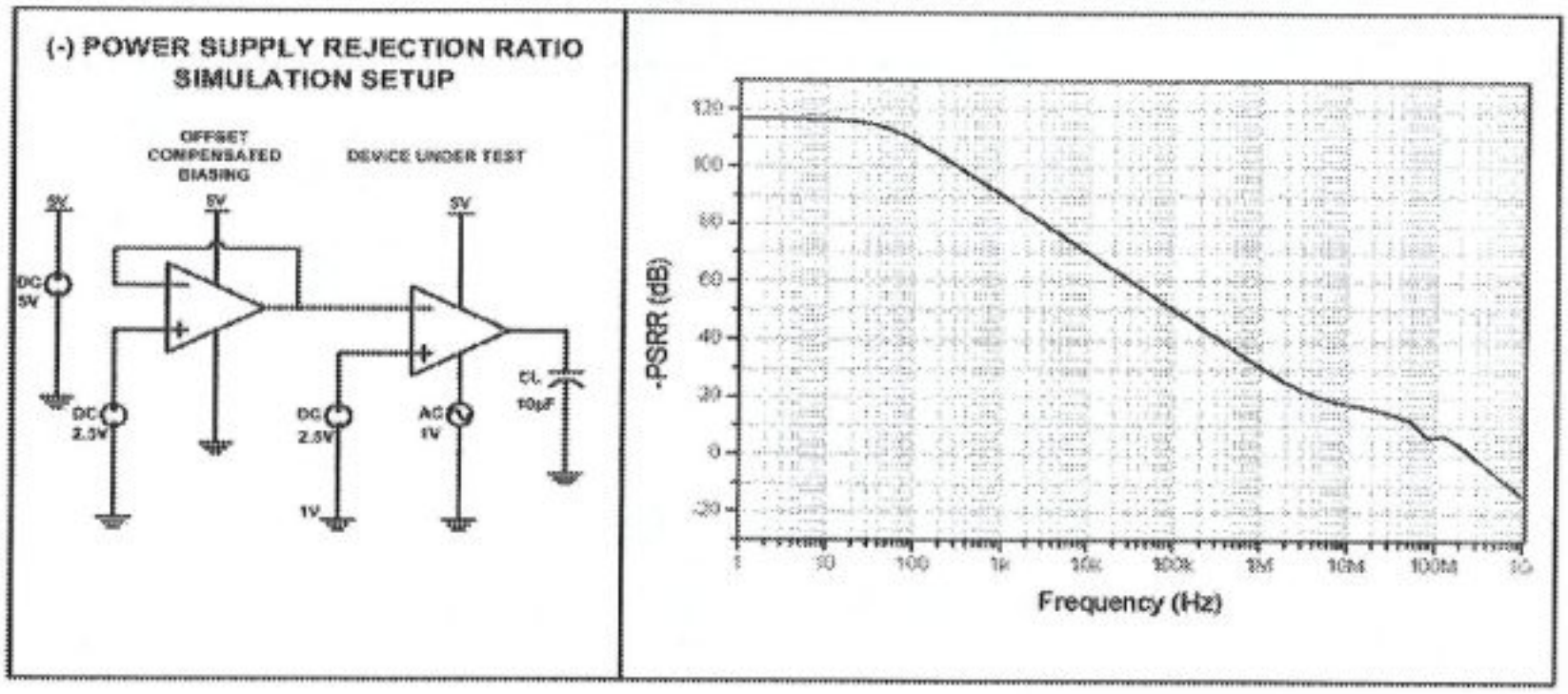


Figure 3.11: -Power supply rejection ratio simulation setup and results for the readout amplifier

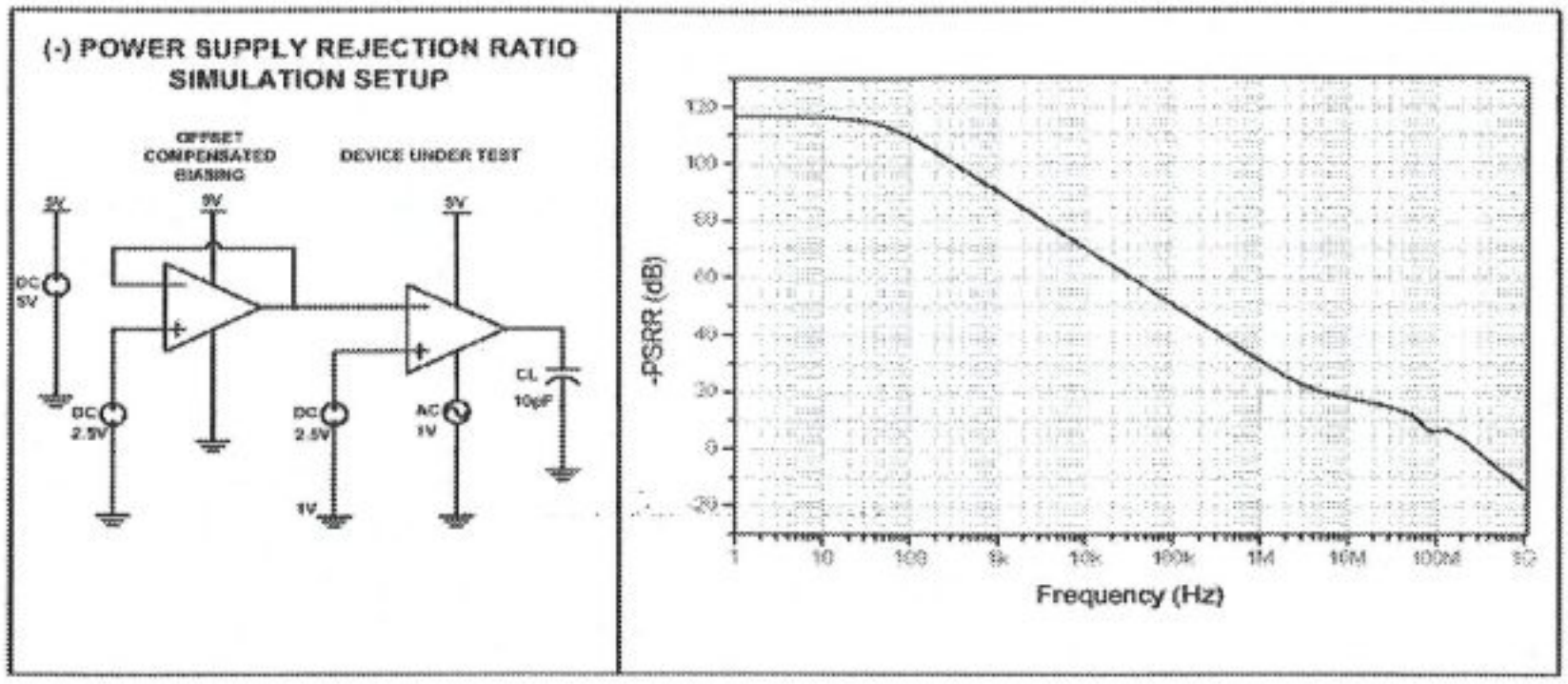


Figure 3.12: Equivalent input noise simulation setup and results for the readout amplifier

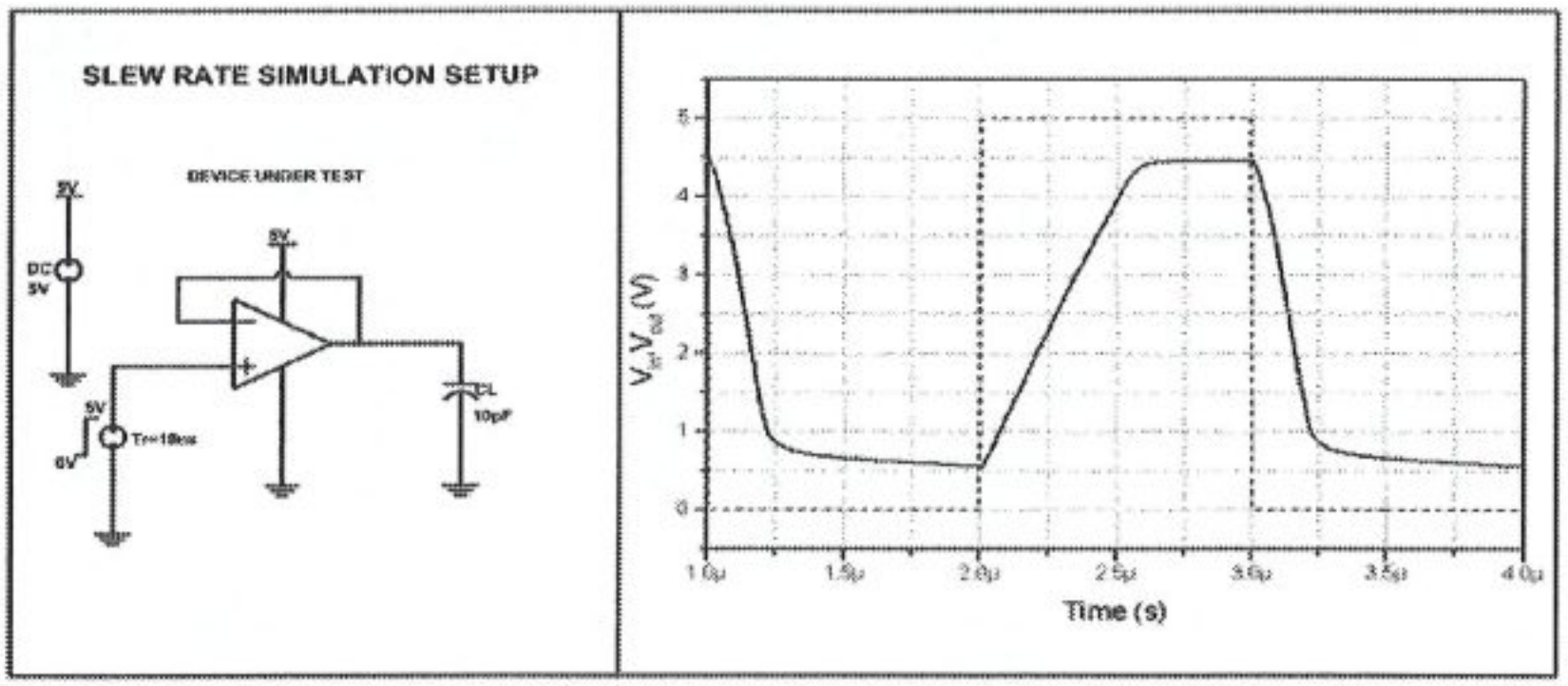


Figure 3.13: Slew Rate simulation setup and results for the readout amplifier

3.4 The Analog Front-End Cell

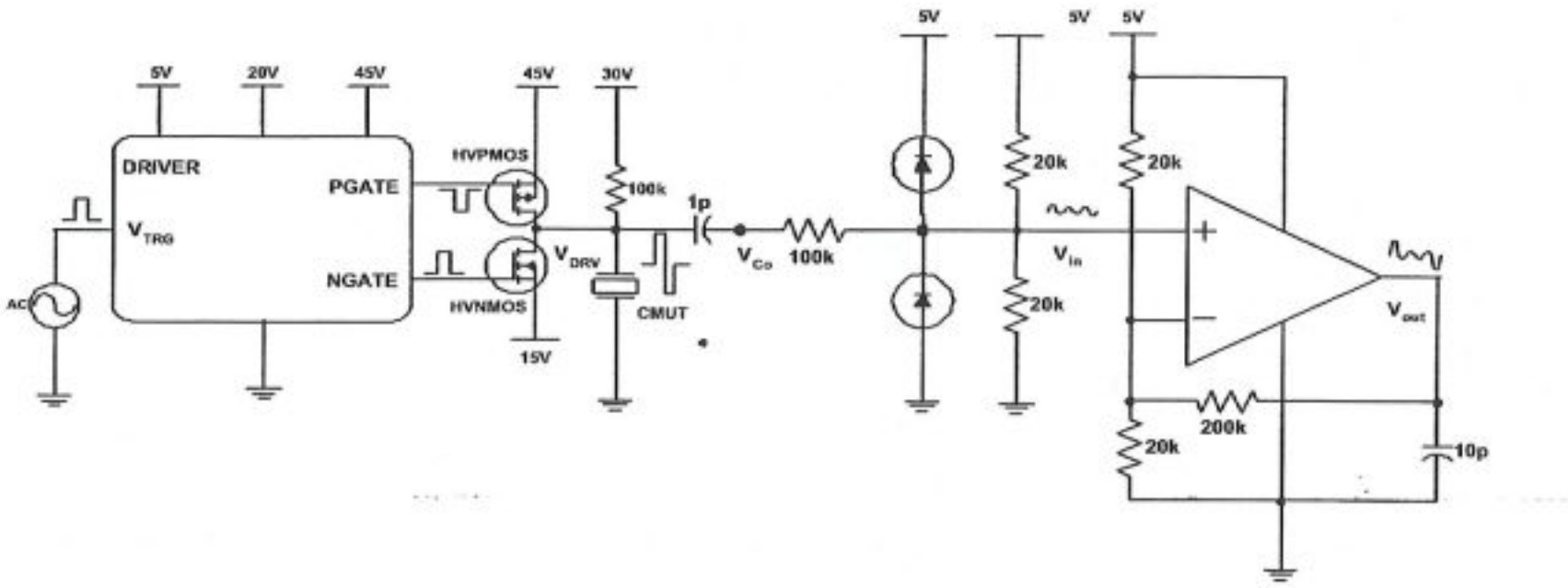


Figure 3.14: Transient simulation setup of the analog front-end cell

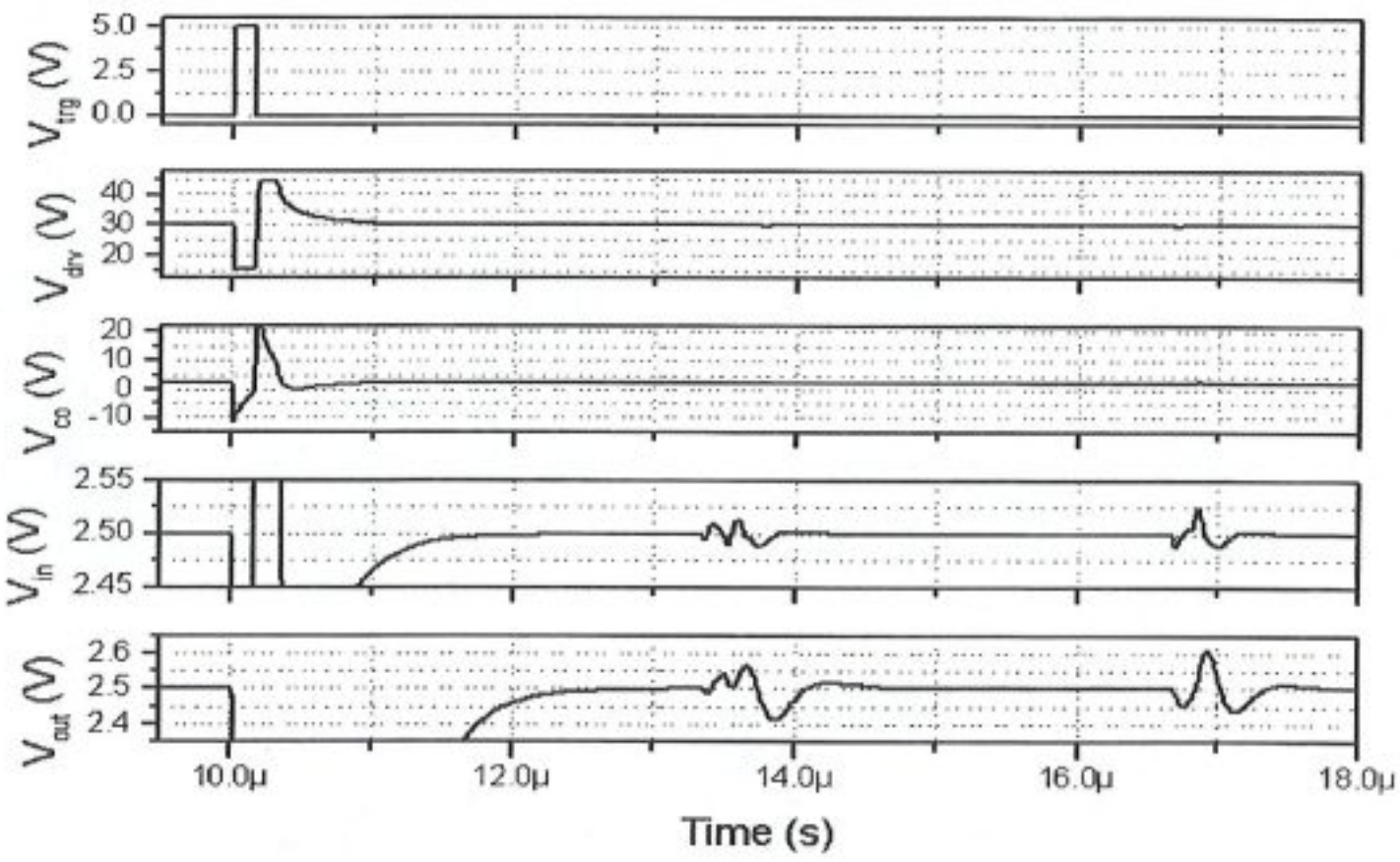
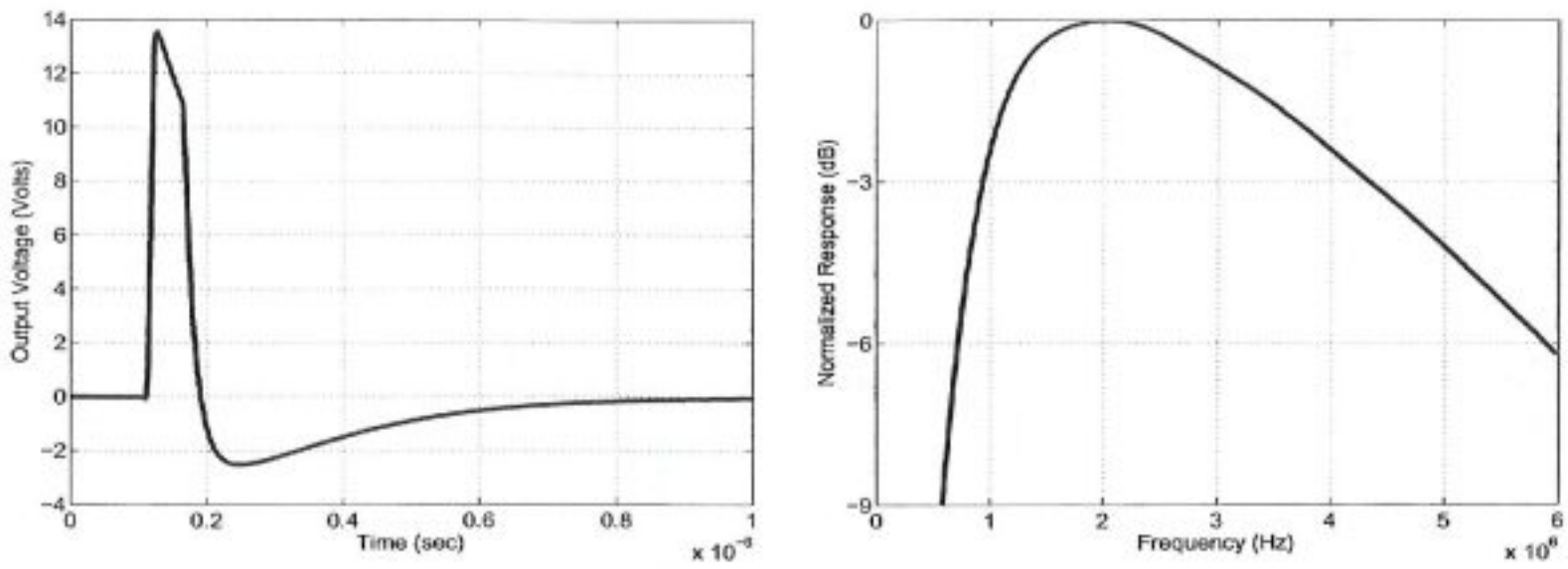


Figure 3.15: Transient simulation results for the system



(a) (b)

Figure 3.16: Output pulse shown in (a) and transmission bandwidth is shown in (b)

The transmission and the reception bandwidths are important characteristics of the system. Following simulations are run to calculate them: In the transmitting mode the driving pulse on the electrical side of the model is measured as observed in figure 3.16 (a) and fast fourier transformation is used to obtain the transmission bandwidth shown in figure 3.16 (b). The transfer ratio n in the Mason's model is calculated to be 9.5795 μN/V. Since the pulse at the electrical end is known, it is possible to obtain the force on the mechanical side by multiplying n with pulse voltage. Then if this force is divided by the total transducer area which is $25\pi r^2 = 34.656\ nm^2$ the output pressure can be obtained. And if it is normalized to the pulse amplitude at the electrical port then 6.9 kPa/V is obtained.

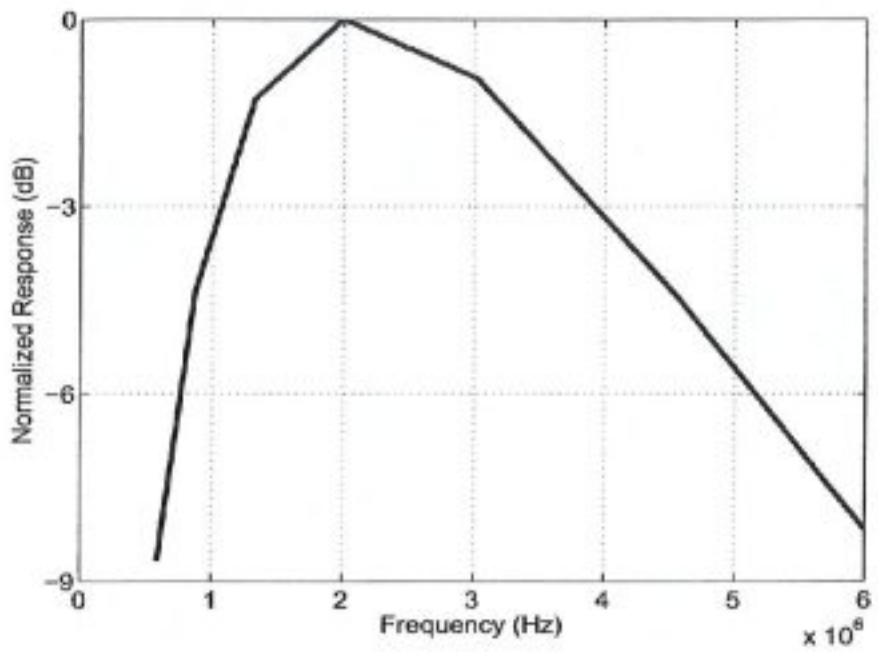


Figure 3.17: Reception bandwidth

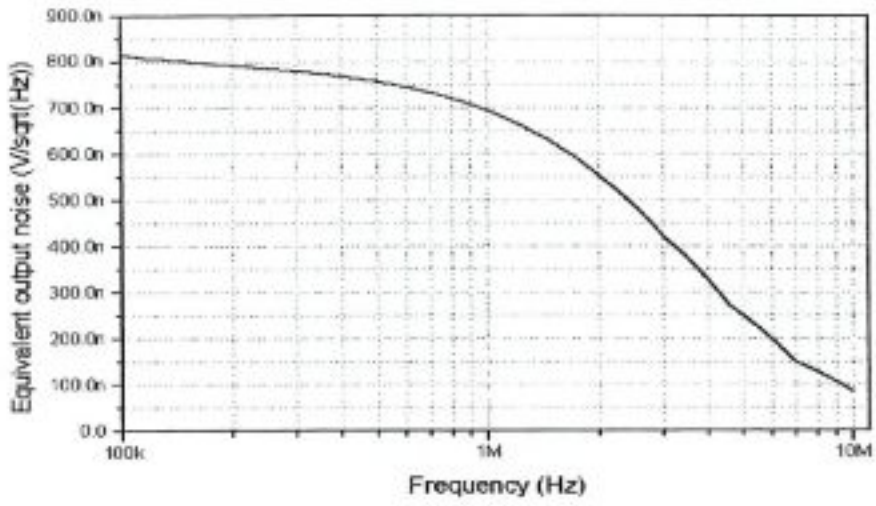


Figure 3.18: Equivalent noise at the input of the CMUT's electrical port

In the reception mode (driver circuit is off), an AC source is connected at the electrical port of the CMUT model the reception bandwidth is obtained by plotting the transfer function from that node to the output of the amplifier by means of AC simulation as depicted in 3.17. And in order to calculate the minimum detectable pressure, a noise simulation is run and the equivalent input noise shown in figure 3.18 is obtained at the electrical port by dividing the equivalent output noise shown in figure 3.19 with the transfer function of the system. It is obvious that if the signal's amplitude is lower than the noise floor, it will not be possible to detect the signal. If the noise floor value is multiplied with n then the minimum detectable force will be calculated and by dividing this value with the area of the transducer $25\pi r^2$, it is possible to obtain the minimum detectable pressure which is $12mPa/\sqrt{(Hz)}$.

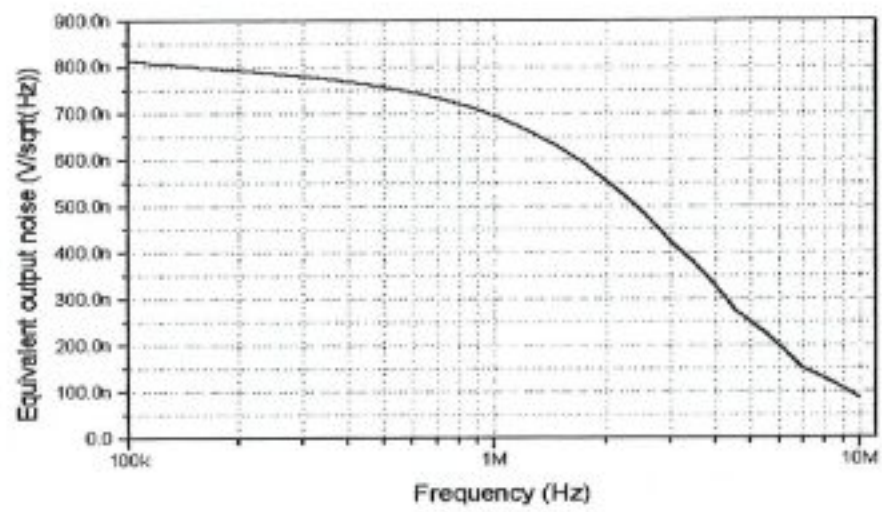


Figure 3.19: Equivalent noise at the output of the readout amplifier

3.5 The Operation of the System

The operation of the system is based on pulse-echo phenomenon and can be divided into two processes: An external trigger pulse starts the transmitting process, the trigger pulse is pre-processed by a logic circuit whose outputs are 180^o out of phase and one pulse width delayed with respect to each other (100 ns) for proper driving of the two high voltage MOSFETs. The outputs are connected to level conversion circuits that convert the 5 V driving logic pulses into properly adjusted voltages that ensure safe operating area constraints of the HVMOSFETs. When HVMOSFETs activated in order, a mono-cycle will be generated at the terminals of the transducer. As the voltage changes abruptly, the transducer consisting of many CMUTs starts to vibrate at the mechanical resonance frequency determined by their dimensions which in turn create acoustic waves coupled into surrounding medium. During the transmitting process the read-out amplifier is protected from the high voltage pulses of the system by the protection circuit. After each driving pulse, the receiving process takes place where the transducer's capacitance is modulated by the absorbed echo signal that causes a voltage between the terminals of the transducer to be induced. Consequently, transducer acts as a small signal source with the high internal impedance formed by CMUT's inherent capacitance which can not directly drive highly capacitive loads as large as 10 pf formed by the metal signal layers in the chip. Echo signal is coupled to readout amplifier through the protection circuit which acts as a band pass filter for the small signal. Then the readout amplifier amplifies the signal to recover the insertion loss and make it easy to process by next stages. A 10 pF load is used to model the parasitic capacitances mentioned above.

Chapter 4

CONCLUSION

A novel analog front-end integrated circuit cell for planar CMUT arrays is introduced in this thesis. Each cell consists of a driver for generating high voltage pulses to drive the CMUT, a connection pad for vertical connection to CMUT by means of flip-chip bonding, a protection circuit to protect the readout amplifier and a low noise readout amplifier to amplify the echo signal. The whole circuit occupies only 200 $\mu m \times 200\ \mu m$ area that corresponds to an operating frequency of approx. 3 MHz with wide bandwidth. A simplified model including the medium that acoustic waves travel is developed from the Mason's classic model. Model parameters are obtained by 3D FEM simulations in ANSYS. Circuit functionality is verified with the post layout simulations in Cadence Spectre simulator. The cell's output pressure is calculated to be 6.9 kPa/V and minimum detectable pressure is obtained as 12 mPa/V. When compared to the other works in the literature, the output pressure is comparable to counterparts' output pressures. In addition, the circuits are not integrated with electronics and use bias voltages as high as 150 V. In the thesis since the bias voltage is limited not only by the process technology but also by the collapse voltage of the CMUT, the output pressure can not be easily increased. The same reason applies to fair low sensitivity of the cell. The overall performance, when the integration advantage is taken into account, is better than many other discrete circuits. The transmission and reception bandwidths are not centered at the operation frequency, but with an acceptable loss they can be utilized. Actually these bandwidths are obtained from the model and real bandwidths can be different due to parasitic effects. In the design, worst case parameters are used to ensure functionality under hard conditions, but in real life it is not always likely

to encounter the worst conditions, at least not all at the same time.

This circuit is only a starting point for an on-chip 3D acoustic imaging system. The system will consist of analog and digital blocks which will occupy vital roles in image reconstruction. 2D arrays of CMUTs provide a unique feature of beam focusing and steering just like in the case of phased array antennas. Without moving the transducer in any direction, only by driving with properly phased signals, X-Y plane scanning and Z-axis focusing can be achieved. Incorporation of digital blocks will yield substrate coupled clock and digital noise signals, thus analog blocks must have high power supply rejection ratios. Digital blocks has to control the driving signals and must evaluate the returning echoes, in order to achieve this, high speed analog to digital converters are required. In addition, image processing and encoding blocks are required. Whatever features are added to the chip, the analog core will remain as the most important part of the design.

An experimental chip that contains 4×4 matrix is designed for test and scheduled for fabrication in October 2004. Because of this reason post layout and post fabrication performances will be compared in the future. This work is expected to be one of the pioneer studies in the volumetric acoustic imaging field.

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