

MINIMISATION OF INSTANTANEOUS TOTAL HARMONIC DISTORTION OF
CURRENTS FOR THREE-PHASE SWITCHING POWER CONVERTERS

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MINIMISATION OF INSTANTANEOUS TOTAL HARMONIC DISTORTION OF
CURRENTS FOR THREE-PHASE SWITCHING POWER CONVERTERS

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ABSTRACT

This work studies an application of the discontinuous control approach to the design of the current control loop in switching power converters and electrical drives.

The role of the current control loop is to generate the switching patterns that will determine the sequence and the duration ON and OFF states of the switches. The reduction of the Instantaneous Total Harmonic Distortion of the currents for 3~Phase Switching Power Converters and 3~Phase Electrical machines is being selected as additional requirement determining the switching matrix operation. The approach is based on the Direct Sliding Mode principle and the unified approach for control of a PWM 3-phase switching matrix with six switches, common for 3-phase inverters, rectifiers as well as 3-phase machines.

Conventional tracking control algorithms may provide the proper selection of switching vector but not the proper timing since switching timing occurs only when the control error is contacted pre-set hysteresis bounds. However this generates significant harmonic distortion especially low order harmonic distortion compared with carrier based algorithms.

The quality of the switching control algorithm is determined by both the proper selection of switching vector and the proper switching timing.

The presented algorithm evaluates harmonic distortion in real time with instantaneous THD definition and sequentially selects two switching vectors in one control period in order to minimize the tracking error and timing is determined according to the THD minimization theorem.

The simulation of the approach is performed on both Boost Rectifier and Buck Inverter, and comparative simulation results with Relay Control approach are given.

ÖZET

Bu çalışmada, 3 fazlı Anahtarlama Güç Çeviricileri ve 3 fazlı Elektrik Makinalarının akımlarındaki, Ani Toplam Harmonik Distorsiyonu azaltacak şekilde kontrol edilebilmesi için gerekli anahtar pozisyonlarının üretilmesine ilişkin, ayrı zamanda bir kontrol yöntemi önerilmektedir. Bu yaklaşım, 6 anahtarlı Darbe Genlik Modülasyonu üreten 3 fazlı anahtarlama matrisinin, tüm 3 fazlı evirici, 3 fazlı doğrultucu ve 3 fazlı elektrik makinaları için tekleştirilmiş modelini ve Direkt Kayan Kipli Denetim ilkesini temel almaktadır.

Klasik izleme algoritmaları, kontrol vektörünün seçimini doğru yapabilirler ve fakat zamanlamasını yapamazlar çünkü anahtarlama zamanı, hatanın daha önceden belirlenmiş histerezis sınırlarına temasıyla gerçekleşmektedir. Fakat bu tip bir yaklaşım, taşıyıcı temelli algoritmalarla kıyaslandığında özellikle düşük dereceden harmonikler yüzünden büyük bir harmonik bozulmaya sebebiyet vermektedir.

Anahtarlama Algoritmasının iyiliği ise hem doğru vektörün seçimi, hem de doğru zamanlamanın yapılmasıyla belirlenmektedir.

Önerilen yaklaşım, Ani Toplam Harmonik Distorsiyon tanımıyla Harmonik distorsiyonu gerçek zamanda hesaplamakta, izleme hatasını minimize edecek şekilde kontrol vektörlerini hesaplamakta, ardından Toplam Harmonik Distorsiyon Minimizasyon ilkesine göre bir kontrol periyodu içinde iki kontrol vektörünün zamanlamasını hesaplamaktadır.

Çalışmada, 3 fazlı Yukarıya doğru doğrultucunun ve 3 fazlı Aşağıya doğru eviricinin önerilen yaklaşımla benzeşimi yapılmış, ve klasik Röle kontrolüyle olan karşılaştırmalı benzeşim sonuçları verilmiştir.

Dedicated to my family

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LIST OF SYMBOLS

sw_j	Binary variable representing the status of j^{th} switch $j=1,2,\dots,6$
U	Control Vector
U_I	First control vector
U_{II}	Second control vector
\vec{u}	Control vector represented in (dq) frames of references
u_j	Control vector component for (abc) frames of references, $j=1,2,3$
u_d	d component Control vector
u_q	q component Control vector
\vec{i}	Inductor currents vector represented in (dq) frames of references
\vec{i}^r	Reference inductor currents vector represented in (dq) frames of references
i_{Lj}	Inductor current vector component in (abc) frames of references $j=1,2,3$
i_{Ld}	d component of Inductor current vector
i_{Lq}	q component of Inductor current vector
i_{gd}	d component of Source current vector
i_{gq}	q component of Source current vector
R	Resistance
L	Inductance
C	Capacitance
V_{Sj}	Input Source Voltage $j=1,2,3$
\vec{v}	AC voltage vector represented in (dq) frames of references
V_O	DC Output voltage
V_{Oj}	Output Voltage vector component in (abc) frames of references $j=1,2,3$
V_{Od}	d component Output Voltage vector
V_{Oq}	q component Output Voltage vector
S	Sliding Mode Manifold

$\vec{\sigma}$	Error Vector
$\vec{\sigma}(0)$	Error vector value at beginning of the control period
$\vec{\sigma}(\tau)$	Error vector value at the end of the control period
\vec{u}_{eq}	Equivalent control vector
\hat{u}_{eq}	Approximated equivalent control vector
τ_{LPF}	Time constant of the Low Pass Filter
V_{DC}	DC Source Voltage
$(\alpha\beta)$	Stationary frame of reference, horizontal axis collinear with phase a base vector
(dq)	Synchronously Rotating frame of reference with the AC side of the converter
T_{abc}^{dq}	Frame transformation matrix, from (abc) frame to (dq) frame
θ_r	Reference angular position
ω_r	Reference angular velocity
\vec{D}	Displacement vector for error
\vec{D}_I	Displacement vector for the first vector
\vec{D}_{II}	Displacement vector for the second vector
τ	Normalized time variable
T	Sampling period of the controller
R_j	RMS value of the jth harmonic
R_1	RMS value of the fundamental harmonic
$A_{abc}^{\alpha\beta}$	Transformation matrix, from (abc) to $(\alpha\beta)$ frame
$A_{\alpha\beta}^{dq}$	Transformation matrix, from $(\alpha\beta)$ to (dq) frame
T_{abc}^{dq}	Transformation matrix, from (abc) to (dq) frame
\vec{x}	System state vector
\vec{x}^r	Reference system state vector
G	Partial derivative of manifold with respect to system state
α	Timing information for Second vector
α^{opt}	Optimum timing information for Second vector
i_d^{ref}	Reference for d component of current

i_q^{ref}	Reference for q component of current
V_o^{ref}	Reference output voltage
v	Quadratic Lypunov function candidate
μ	Positive real number
ϕ^{ref}	Reference angle between d component and q compponent of current
T	Sampling period of the controller
u_{imin}	Lower bound of the control u
u_{imax}	Upper bound of the control u
\vec{H}	Vector valued function
H_d	d component of \vec{H}
H_q	q component of \vec{H}
\vec{f}	Continuous vector valued function
f_d	d component of \vec{f}
f_q	q component of \vec{f}

LIST of ABBREVIATIONS

THD	Total Harmonic Distortion
AC	Alternative Current
DC	Direct Current
EMC	Electromagnetic Compatibility
PWM	Pulse Width Modulation
μ	micro 10^{-6}
m	mili 10^{-3}
k	kilo 10^3
Hz	Hertz (s^{-1})
A	Amper
V	Volt
s	second

1. INTRODUCTION

Switching Power Converters are the main building blocks of UPS, motor drives, active filtering since efficiency and loss requirements dictate the control of power in a switching mode. For all of these applications, high quality AC current tracking with limited ripple is required.

In the Switching Power Converters, the modulation of the power flow between the input side and output side is performed by switching matrix. This switching matrix for the three-phase converters has six switches. The control input for switching power converters is the positions of those switches as a function of time. The vector that has the position information for the switches will be referred as switching vector.

The Pulse Width Modulation (PWM) is mostly used technique, that is varying the duration of pulses with respect to magnitude, frequency or phase of a voltage or current, to form the average of a given reference at the output.

In [1], an algebraic synthesis for PWM methods, which can be the starting point for every PWM method representation, is given. In the work, also, mentioned PWM methods are compared in various aspects i.e harmonic content. It is apparent that switching at a sufficiently high frequency with respect to the modulated function, the ripple and Harmonic Distortion of AC currents can be reduced. But switching frequency can not be increased arbitrarily. Because, first, the switching losses of semiconductor devices increase proportional to the switching frequency. The converter switching losses can be only reduced by the switching frequency of the converter. Second, the regulations regarding electromagnetic compatibility (EMC) are stricter for power conversion equipment operating at switching frequencies higher than 9 kHz [2]. Since high frequency switching generates high frequency harmonics on the currents and voltages, these high frequency harmonics of voltages and currents injected back into the supply system, and coupled electromagnetically are function of the switching transition

times and switching formats in the converter [3]. Third, switches for higher power rated systems (Megawatt) should operate in low frequencies not to cause excessive losses.

Thus, converters should operate at a limited frequency as low as possible. The switching algorithm chosen to meet the closed-loop specifications for the system, should also end up with minimum switching actions, less Total Harmonic Distortion (THD) and regularity in switching.

In [4-5-6-7], the Sliding Mode Control System design for Three Phase Power converters is given. These researches reveal that both the PWM pattern selection and the desired dynamical transients of the closed loop system can be solved together. The scheme evaluates the system's state and explores available control corresponding to the system state.

In [8], keeping the Sliding Mode Approach, the evaluation of system state together with the available controls are considered, and the selection is decided to minimize the switching actions by minimizing the velocity of error.

In [9], which forms the basis of this work, keeping the Sliding Mode approach for converters, the evaluation of controls corresponding to the system state together with the minimization of a cost function, that is Instantaneous Total Harmonic Distortion, is presented.

In [10], for a High-Power drive study, an optimal PWM is studied. Modulation error caused by the conversion of a continuous reference signal into a discrete switching sequence at low switching frequency is compensated by tracking controller which is modifying the switching pattern in real time. Decomposition of the current vector trajectory into its components enables the identification of the instantaneous fundamental current, permitting the implementation of a fast current control system.

In [11], DSP based discrete-time integral-type optimal regulator (handling the processor time lag) is considered for a robust control of an IM drive system composed of a Boost Rectifier and an Inverter. To obtain higher control performance, a DC load current is added from the Inverter side. Deviations in state variables cause stability problems.

Generally, quality of switching control algorithms is determined by both proper selection of switching vector and proper switching timing of switching vector. Conventional tracking control algorithms (hysteresis comparator control, instantaneous space vector control, sliding mode control etc.) may provide proper selection of switching vector, but not proper switching timing since switching timing occurs only

when the control error contacts pre-set hysteresis bounds. It is not reasonable since it generates big harmonic distortion compared with carrier based algorithms and switching frequency varies with different operation points [9].

This work aims to solve the problem of current control of 3~Phase Switching Power Converters satisfying the followings at the same time for given specifications

- Better transient response
- Less ripple
- Less Harmonic Distortion
- Less losses in steady state operation

This work presents a current control scheme based on the work of Chen, Sabanovic, and Ohnishi [9]. The solution is presented for the minimization of THD in currents of 3~Phase switching power converters getting use of the unified description for all 3~Phase switching power converters. This current control approach is based on Sliding Mode Control with a unique correspondence between the state of the system and switching configuration, and evaluates harmonic distortion in real time with Instantaneous Total Harmonic distortion definition as a direct evaluation function. Sliding Mode Control is suggested to have a robust performance against parameter variations and load disturbances without stability problems. In sliding mode, the trajectory of the system is constrained to move on a predetermined manifold in state space. This is accomplished by designing a control law commutating at high frequency among the different possible configurations. Sliding mode not only offers the parameter insensitive features but also gives good system dynamic and static characteristics. Because of the discontinuous control feature of Sliding Mode Control, the chattering can occur in the control system.

Two switching vectors are selected sequentially in one control period according to the error minimization theorem and timing is determined to minimize THD.

2. FUNCTIONAL DESCRIPTION OF 3~PHASE SWITCHING POWER CONVERTERS

2.1 Introduction

The role of the power converter, having matrix-like structure with three legs, is the modulation of the electrical power flow between power sources, acting as a link. Efficient modulation of power flow is realised using switches having zero voltage drop when conducting, and fully blocks the current flow in cut-off region. Generic structure of a 3~Phase Switching Power conversion system is shown in Figure 2.1 .

Rectifiers transform AC power into DC power, and Inverters transform DC power into AC power. In Figure 2.2, the common structures for the switching converters are depicted. These do not represent in any sense all of the 3-phase switching converters but rather the structures with salient properties.

Due to the restriction of Kirchoff's Circuit Law, the nature of sources at input side and output side are different. The role of energy storing elements (L, C) is to balance the power flow between source and sink by temporarily storage and release of energy.

The control of power flow is done by varying the length of time intervals for which the energy storing elements are connected to or disconnected from the energy sources. The control input for these power converters, each having the same switching matrix, is the positions of the switches.

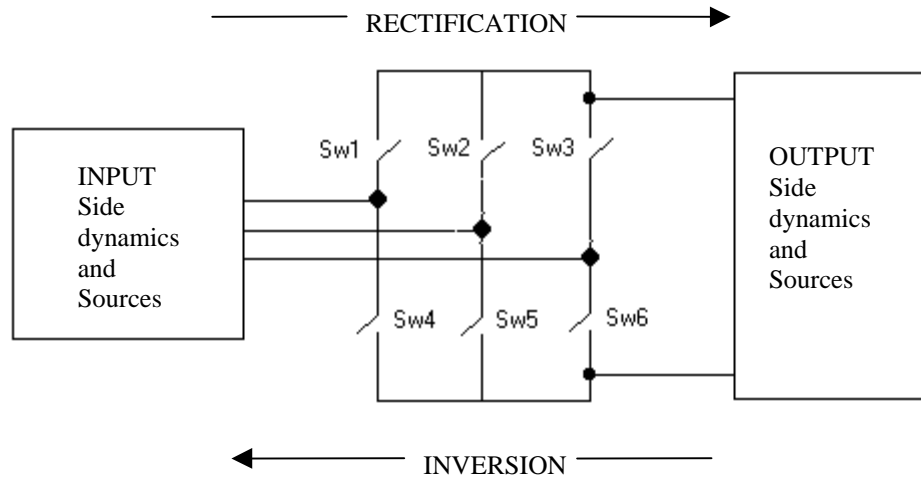


Figure 2.1 Structure of three-phase system

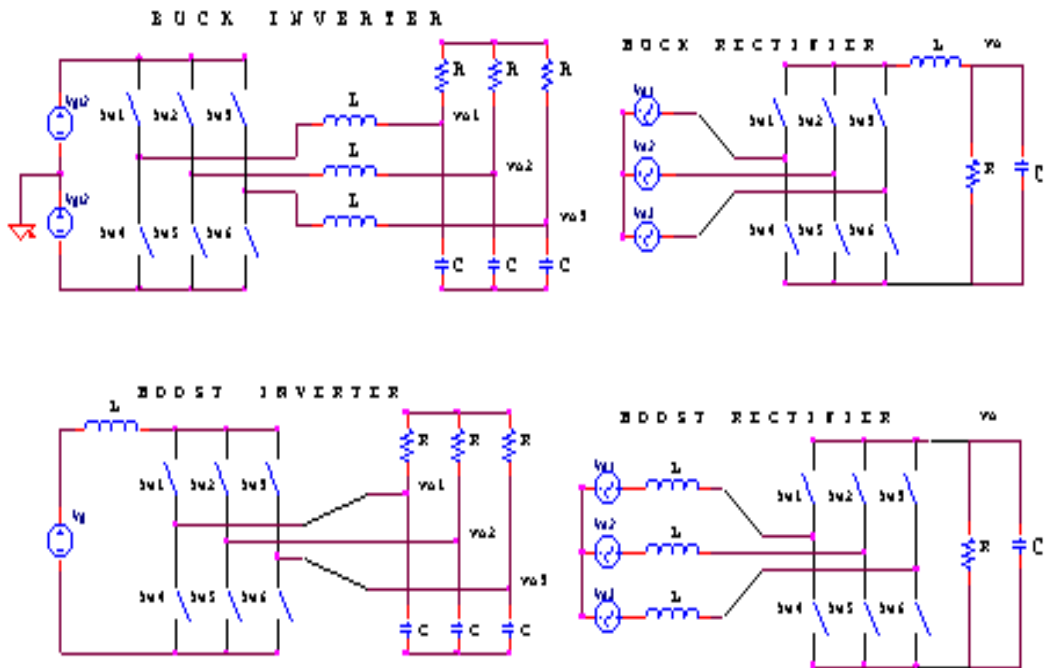


Figure 2.2 Common structures for Switching Power Converters

Switches are operated in such a way that the short circuit of the capacitors and open circuit of the inductor currents are not permitted. These electrical circuit constraints not only limit the number of permissible positions of the switches but also define the number of independent controls, this number being less than the number of switches.

2.2 Definition of Control Vector (Switching Vector) U and Permissible Control Vectors

Let, the vector U represents the states of the switches, which has six elements corresponding to the each switch status (ON-OFF) in the switching matrix.

$U = [sw_1 \ sw_2 \ sw_3 \ sw_4 \ sw_5 \ sw_6]^T$ where sw_i ($i=1,2\dots6$) takes binary values from the set $\{0,1\}$. The value 0 represents the OFF state of the corresponding switch, 1 represents the ON state of the corresponding switch. When the electrical circuit constraints are considered, control vector can be represented with 3 variables as $U = [u_1 \ u_2 \ u_3]^T$ where u_i ($i=1,2,3$) takes values from the set $\{-1,0,1\}$ for Buck Rectifier and Boost Inverter, and u_i ($i=1,2,3$) takes values from the set $\{-1,1\}$ for Buck Inverter and Boost Rectifier. Each component represents the status of the switches at the corresponding leg (each phase) of the switching matrix according to the following:

- the value -1 represents that lower switch is ON, and upper switch is OFF in that leg,
- the value 0 represents that both switches are OFF in that leg,
- the value 1 represents that upper switch is ON and lower switch is OFF in that leg.

The representation of control vector with 3 components, each corresponding to one phase in three-phase system is referred as representation in (abc) frames of references. In the Table 1 and Table 2, the permissible states of the switches are presented above converters.

For the Buck Inverter and the Boost Rectifier, the permissible number of control vectors is 8. All these vectors can be represented with 3 components having values from the set $\{1,-1\}$.

Table 1. Permissible connections for Boost Rectifier & Buck Inverter

Vector	SW1	SW2	SW3	SW4	SW5	SW6
U ₁	ON	OFF	OFF	OFF	ON	ON
U ₂	ON	ON	OFF	OFF	OFF	ON
U ₃	OFF	ON	OFF	ON	OFF	ON
U ₄	OFF	ON	ON	ON	OFF	OFF
U ₅	OFF	OFF	ON	ON	ON	OFF
U ₆	ON	OFF	ON	OFF	ON	OFF
U ₇	ON	ON	ON	OFF	OFF	OFF
U ₈	OFF	OFF	OFF	ON	ON	ON

For the Boost Inverter and the Buck Rectifier the permissible number of control vectors is 9. All these vectors can be represented with 3 components having values from the set $\{1,0,-1\}$.

Table 2. Permissible connections for Boost Inverter & Buck Rectifier

Vector	SW1	SW2	SW3	SW4	SW5	SW6
U ₁	ON	OFF	OFF	OFF	OFF	ON
U ₂	OFF	ON	OFF	OFF	OFF	ON
U ₃	OFF	ON	OFF	ON	OFF	OFF
U ₄	OFF	OFF	ON	ON	OFF	OFF
U ₅	OFF	OFF	ON	OFF	ON	OFF
U ₆	ON	OFF	OFF	OFF	ON	OFF
U ₇	ON	OFF	OFF	OFF	ON	OFF
U ₈	OFF	ON	OFF	OFF	ON	OFF
U ₉	OFF	OFF	ON	OFF	OFF	ON

2.3 Mathematical Model of 3-Phase Switching Power Converters

Derivation of the mathematical models of the switching power converters is out of the scope of this work. Basically, symmetric, balanced three-phase system and ideal switches are assumed. Following the steps at [14], mathematical descriptions of these converters in phase frame, (abc) frames of references, are given in the proceeding parts.

2.3.1 Boost Rectifier Description in Phase (abc) Frame

Boost Rectifier circuit is shown in Figure 2.3. Its mathematical model in Phase frame is as follows:

$$\begin{aligned}
 \frac{d}{dt}V_O &= \frac{1}{2C} [i_{L1}.u_1 + i_{L2}.u_2 + i_{L3}.u_3] - \frac{V_O}{RC} \\
 \frac{d}{dt}i_{L1} &= \frac{1}{L}.V_{s1} - \frac{V_O}{2L} \left(u_1 - \frac{u_1 + u_2 + u_3}{3} \right) \\
 \frac{d}{dt}i_{L2} &= \frac{1}{L}.V_{s2} - \frac{V_O}{2L} \left(u_2 - \frac{u_1 + u_2 + u_3}{3} \right) \\
 \frac{d}{dt}i_{L3} &= \frac{1}{L}.V_{s3} - \frac{V_O}{2L} \left(u_3 - \frac{u_1 + u_2 + u_3}{3} \right)
 \end{aligned} \tag{2.1}$$

Where $u_i = \begin{cases} 1, \text{ when } SW_i \text{ is ON and } SW_{i+3} \text{ is OFF} \\ -1, \text{ when } SW_i \text{ is OFF and } SW_{i+3} \text{ is ON} \end{cases}$

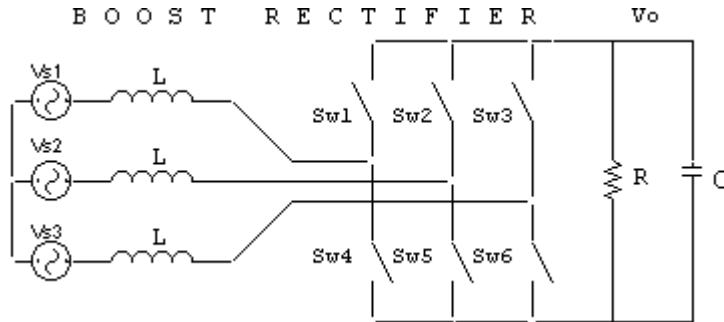


Figure 2.3 Boost Rectifier

V_{s_i} Denotes the 3 phase source voltages, defined as $V_{s_i} = V_g \left[\cos(\theta_r - (i-1)\frac{2\pi}{3}) \right]$,

where $i=1,2,3$

V_o Denotes the output voltage

R, L, C denotes the resistance, inductance, capacitance respectively.

i_{L_i} Denotes the inductor currents where $i=1,2,3$

2.3.2 Buck Inverter Description in Phase (abc) Frame

Buck Inverter circuit is shown in Figure 2.4. Its mathematical model in Phase frame is as follows:

$$\begin{aligned}
 \frac{d}{dt} i_{L1} &= \frac{1}{L} \left[V_{o1} - \frac{V_{o1} + V_{o2} + V_{o3}}{3} \right] - \frac{V_{DC}}{2L} \left[u_1 - \frac{u_1 + u_2 + u_3}{3} \right] \\
 \frac{d}{dt} i_{L2} &= \frac{1}{L} \left[V_{o2} - \frac{V_{o1} + V_{o2} + V_{o3}}{3} \right] - \frac{V_{DC}}{2L} \left[u_2 - \frac{u_1 + u_2 + u_3}{3} \right] \\
 \frac{d}{dt} i_{L3} &= \frac{1}{L} \left[V_{o3} - \frac{V_{o1} + V_{o2} + V_{o3}}{3} \right] - \frac{V_{DC}}{2L} \left[u_3 - \frac{u_1 + u_2 + u_3}{3} \right] \\
 \frac{d}{dt} V_{o1} &= \frac{1}{C} i_{L1} - \frac{1}{RC} V_{o1} \\
 \frac{d}{dt} V_{o2} &= \frac{1}{C} i_{L2} - \frac{1}{RC} V_{o2} \\
 \frac{d}{dt} V_{o3} &= \frac{1}{C} i_{L3} - \frac{1}{RC} V_{o3}
 \end{aligned} \tag{2.2}$$

$$\text{Where } u_i = \begin{cases} 1, \text{ when SW}_i \text{ is ON and SW}_{i+3} \text{ is OFF} \\ -1, \text{ when SW}_i \text{ is OFF and SW}_{i+3} \text{ is ON} \end{cases}$$

V_{DC} Denotes the DC voltage source,

R, L, C denotes the resistance, inductance, capacitance respectively.

i_{L_i} Denotes the inductor currents where subscript $i=1,2,3$

V_{o_i} Denotes the three-phase output voltages

where subscript $i=1,2,3$

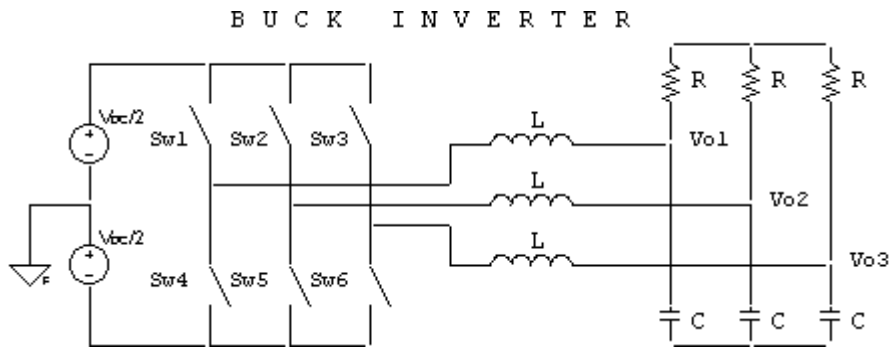


Figure 2.4 Buck Inverter

2.3.3 Buck Rectifier Description in Phase (abc) Frame

Buck Rectifier circuit is shown in Figure 2.5. Its mathematical model in Phase frame is as follows:

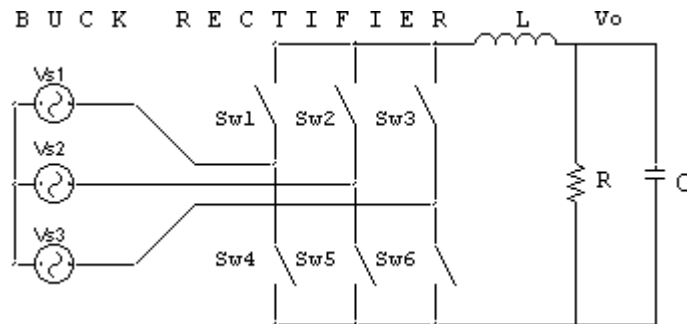


Figure 2.5 Buck Rectifier

$$\begin{aligned} \frac{d}{dt} i_L &= \frac{1}{L} (V_{s1} \cdot u_1 + V_{s2} \cdot u_2 + V_{s3} \cdot u_3) - \frac{V_o}{L} \\ \frac{d}{dt} V_o &= \frac{i_L}{C} - \frac{V_o}{RC} \end{aligned} \tag{2.3}$$

$$\text{Where } u_i = \begin{cases} 1, & \text{when } SW_i \text{ is ON and } SW_{i+3} \text{ is OFF} \\ 0, & \text{when } SW_i \text{ is OFF and } SW_{i+3} \text{ is OFF} \\ -1, & \text{when } SW_i \text{ is OFF and } SW_{i+3} \text{ is ON} \end{cases}$$

R, L, C denotes the resistance, inductance, capacitance respectively.

$$V_{s_i} \quad \text{Denotes the 3 phase source voltages defined as } V_{s_i} = V_g \cdot \left[\cos\left(\theta_r - (i-1)\frac{2\pi}{3}\right) \right],$$

where $i=1,2,3$

i_L Denotes the inductor current

V_o Denotes the output voltage

2.3.4 Boost Inverter Description in Phase (abc) Frame

Boost Inverter circuit is shown in Figure 2.6. Its mathematical model in Phase frame is as follows:

$$\begin{aligned} \frac{d}{dt} i_L &= \frac{V_{DC}}{L} - \frac{V_{O1}u_1 + V_{O2}u_2 + V_{O3}u_3}{L} \\ \frac{d}{dt} V_{O1} &= i_L u_1 - \frac{V_{O1}}{R} + \frac{V_{O1} + V_{O2} + V_{O3}}{3R} \\ \frac{d}{dt} V_{O2} &= i_L u_2 - \frac{V_{O2}}{R} + \frac{V_{O1} + V_{O2} + V_{O3}}{3R} \\ \frac{d}{dt} V_{O3} &= i_L u_3 - \frac{V_{O3}}{R} + \frac{V_{O1} + V_{O2} + V_{O3}}{3R} \end{aligned} \quad (2.4)$$

$$\text{Where } u_i = \begin{cases} 1, & \text{when } SW_i \text{ is ON and } SW_{i+3} \text{ is OFF} \\ 0, & \text{when } SW_i \text{ is OFF and } SW_{i+3} \text{ is OFF} \\ -1, & \text{when } SW_i \text{ is OFF and } SW_{i+3} \text{ is ON} \end{cases}$$

i_L Denotes the inductor current

V_{o_i} Denotes the three-phase output voltages where subscript $i=1,2,3$

R, L, C denotes the resistance, inductance, capacitance respectively.

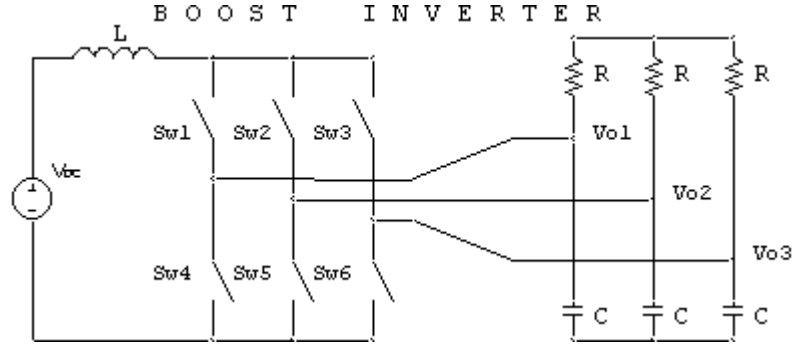


Figure 2.6 Boost Inverter

2.3.5 Synchronously Rotating Frames of References (dq)

Leaning the AC side variables on basis vectors - e_A, e_B, e_C , each shifted with 120° , forming the frame called as (abc) frames of references - the models in (abc) frames of references has the control inputs coupled. So, control system design based on those models is complicated. Transforming the variables and descriptions from (abc) frames of reference to an orthogonal frame, called as $(\alpha\beta)$ frame of reference, horizontal axis (α) collinear with phase A (e_A), will reduce the order, but still the controls will be time varying. To solve the problem of controlling 3~Phase converters, it is convenient to describe the dynamics of the switching converters in the orthogonal frame of references, rotating synchronously related to the AC side of the converter known as (dq) frames of references that serves the controls in the models both decoupled and fixed.

For rectifiers d axis is collinear with the source voltage vector and for inverters the d axis is collinear with the output reference vector. The q axis is perpendicular to the d axis.

The following matrices represent transformations between these frames for a symmetric, balanced three-phase system.

From (abc) to $(\alpha\beta)$ frame, the transformation is given by

$$A_{abc}^{\alpha\beta} = \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \quad (2.5)$$

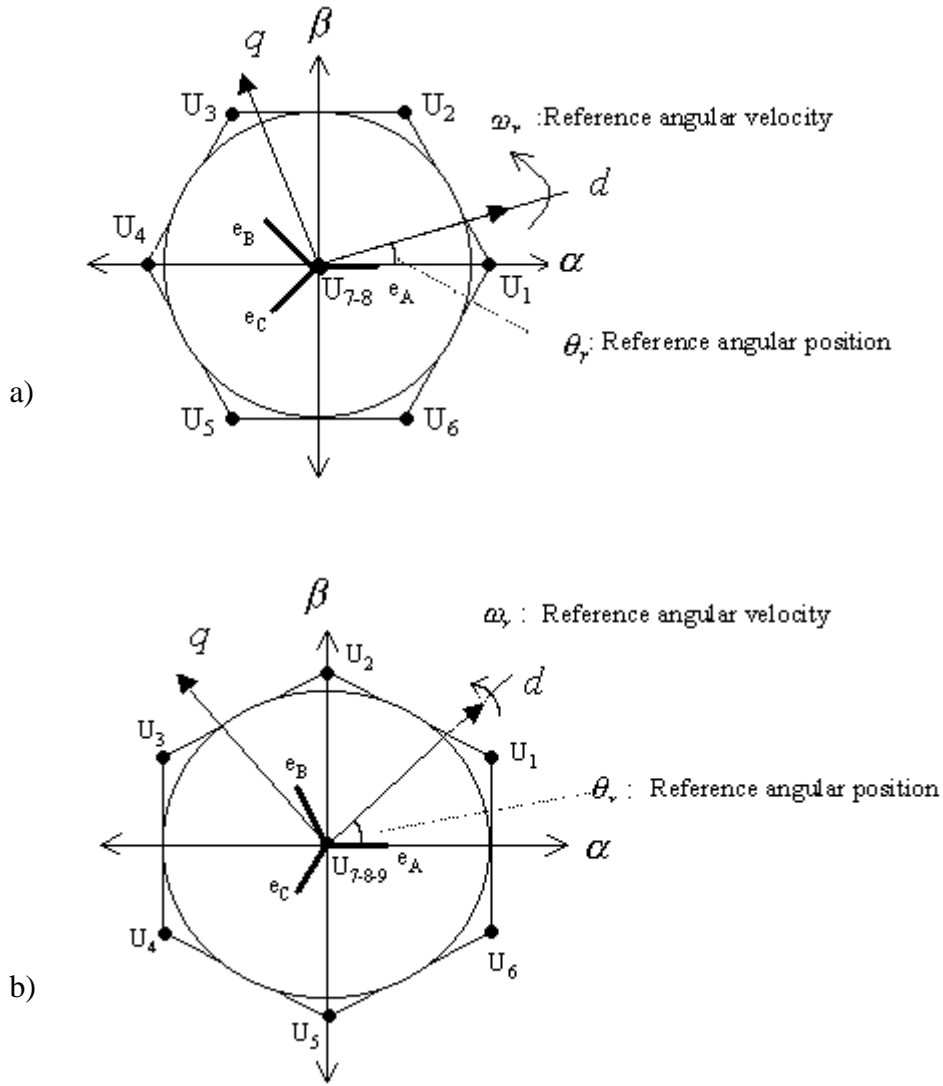


Figure 2.7 Switching vectors a) for Boost Rectifier and Buck Inverter b) for Boost Inverter and Buck Rectifier, in orthogonal frames of references $(\alpha\beta)$, and illustration of Synchronously Rotating (dq) frames of references

From $(\alpha\beta)$ frame to (dq) frame, the transformation is given by

$$A_{\alpha\beta}^{dq} = \begin{bmatrix} \cos\theta_r & \sin\theta_r \\ -\sin\theta_r & \cos\theta_r \end{bmatrix} \quad (2.6)$$

From (abc) to (dq) frame, the transformation is given by

$$T_{abc}^{dq} = A_{\alpha\beta}^{dq} \cdot A_{abc}^{\alpha\beta} = \begin{bmatrix} \cos(\theta_r) & \cos(\theta_r - \frac{2\pi}{3}) & \cos(\theta_r - \frac{4\pi}{3}) \\ -\sin(\theta_r) & -\sin(\theta_r - \frac{2\pi}{3}) & -\sin(\theta_r - \frac{2\pi}{3}) \end{bmatrix} \quad (2.7)$$

where θ_r is the angular position of the (dq) frame of references with respect to orthogonal frame of references. $\theta_r = \omega_r \cdot t$ is the reference angular position and ω_r is the reference angular velocity.

Three phase base vectors, control inputs in (abc) frames and ($\alpha\beta$) frames are shown in Figure 2.7. Also (dq) frames of reference with respect to (abc) and ($\alpha\beta$) frames is shown in Figure 2.7.

2.3.6 Boost Rectifier Description in Synchronously Rotating (dq) Frame

Boost Rectifier description in (dq) orthogonal frame of reference related to the AC side is as follows:

$$\begin{aligned} \frac{dV_O}{dt} &= \frac{-V_O}{RC} + \frac{i_{Ld} \cdot u_d + i_{Lq} \cdot u_q}{2C} \\ \frac{d}{dt} i_{Ld} &= \omega_r \cdot i_{Lq} + \frac{V_{DC}}{L} - \frac{V_O}{2L} u_d \\ \frac{d}{dt} i_{Lq} &= -\omega_r \cdot i_{Ld} - \frac{V_O}{2L} u_q \end{aligned} \quad (2.8)$$

where ω_r is the angular velocity of the AC voltage sources, i_{Ld}, i_{Lq} are the components of inductor current vector and u_d, u_q are the components of control vector, transformed into (dq) frame.

2.3.7 Buck Inverter Description in Synchronously Rotating (dq) Frame

Buck Inverter description in (dq) orthogonal frame of reference related to the AC side is as follows:

$$\begin{aligned}
 \frac{d}{dt}V_{Od} &= \frac{-1}{RC}V_{Od} + \omega_r.V_{Oq} + \frac{1}{C}i_{Ld} \\
 \frac{d}{dt}V_{Oq} &= \frac{-1}{RC}V_{Oq} - \omega_r.V_{Od} + \frac{1}{C}i_{Lq} \\
 \frac{d}{dt}i_{Ld} &= \frac{-1}{L}V_{Od} + \omega_r.i_{Lq} + \frac{V_{DC}}{2L}u_d \\
 \frac{d}{dt}i_{Lq} &= \frac{-1}{L}V_{Oq} - \omega_r.i_{Ld} + \frac{V_{DC}}{2L}u_q
 \end{aligned} \tag{2.9}$$

where ω_r is the angular velocity of the AC side voltage sources. i_{Ld}, i_{Lq} are the components of inductor current vector, V_{Od}, V_{Oq} are components of output voltage vector and u_d, u_q are the components of control vector, transformed into (dq) frame.

2.3.8 Buck Rectifier Description in Synchronously Rotating (dq) Frame

Buck Rectifier description in (dq) orthogonal frame of reference related to the AC side is as follows:

$$\begin{aligned}
 \frac{d}{dt}V_O &= -\frac{V_O}{RC} + \frac{i_L}{C} \\
 \frac{d}{dt}i_L &= -\frac{V_O}{L} + \frac{V_{DC}}{L}u_d \\
 i_{gd} &= i_L.u_d \\
 i_{gq} &= i_L.u_q
 \end{aligned} \tag{2.10}$$

where ω_r is the angular velocity of the AC side voltage sources. i_{gd}, i_{gq} are the components of current vector from the supply, u_d, u_q are the components of control vector, transformed into (dq) frame.

2.3.9 Boost Inverter Description in Synchronously Rotating (dq) Frame

Boost Inverter description in (dq) orthogonal frame of reference related to the AC side is as follows:

$$\begin{aligned}
 \frac{d}{dt}V_{Od} &= -\frac{V_{Od}}{RC} + \omega_r V_{Oq} + \frac{i_L}{C}u_d \\
 \frac{d}{dt}V_{Oq} &= -\frac{V_{Oq}}{RC} - \omega_r V_{Od} + \frac{i_L}{C}u_q \\
 \frac{d}{dt}i_L &= -\frac{V_{Od}}{L}u_d - \frac{V_{Oq}}{L}u_q + \frac{V_{DC}}{L}
 \end{aligned} \tag{2.11}$$

where ω_r is the angular velocity of the AC side voltage outputs, V_{Od}, V_{Oq} are components of output voltage vector and u_d, u_q are the components of control vector, transformed into (dq) frame.

2.3.10 General and Unified Description of 3~Phase Power Converters in Synchronously Rotating (dq) Frame

In order to employ the same control approach for all 3~Phase switching power converters, having the same switching matrix, a unified description is needed. Considering (2.8), (2.9), (2.10), (2.11), general description of three-phase converters can be expressed as:

<p>For Buck Converters</p> $\frac{d}{dt} \vec{v} = \vec{f}_v(v) + B_i \cdot \vec{i}$ $\frac{d}{dt} \vec{i} = \vec{f}_i(v, i) + B_u \cdot \vec{u}$	<p>For Boost Converters</p> $\frac{d}{dt} \vec{v} = \vec{f}_v(v, i) + B_i(u) \cdot \vec{i}$ $\frac{d}{dt} \vec{i} = \vec{f}_i(v, i) + B_u \cdot \vec{u}$	(2.12)
<p>where $\vec{v} = [v_d \ v_q]^T$, $\vec{i} = [i_{ld} \ i_{lq}]^T$, $\vec{u} = [u_d \ u_q]^T$</p>		

Considering (2.12), it can be seen that output voltage is determined by the currents, and currents are determined by the switching vectors. This enables the design of the controller in two steps, namely the current control loop and voltage control loop [7]. First control vector should be selected so that the current tracks its reference. Second, the reference current should be selected so that the voltage tracks its reference. Thus, designing the controller in (dq) frames of references is more convenient.

3. CONTROL OF 3~PHASE SWITCHING POWER CONVERTERS

The control problem for 3~Phase switching power converter system is to find the sequence and the duration of the ON and OFF states for switches so that the desired dynamical specifications are met.

3.1 Sliding Mode Control of Switching Power Converters

Equations describing switching power converters have discontinuous right hand side. In such a system sliding mode motion can result. Recalling equation (2.12), which is also rewritten as (3.1), it is apparent that descriptions of the change of the current of three-phase converters in (dq) frames of references are linear with respect to control input.

$$\begin{array}{ll}
 \text{For Buck Converters:} & \text{For Boost Converters} \\
 \frac{d}{dt} \vec{v} = \vec{f}_v(v) + B_i \cdot \vec{i} & \frac{d}{dt} \vec{v} = \vec{f}_v(v, i) + B_i(u) \cdot \vec{i} \\
 \frac{d}{dt} \vec{i} = \vec{f}_i(v, i) + B_u \cdot \vec{u} & \frac{d}{dt} \vec{i} = \vec{f}_i(v, i) + B_u \cdot \vec{u}
 \end{array} \tag{3.1}$$

where $\vec{v} = [v_d \ v_q]^T$, $\vec{i} = [i_d \ i_q]^T$, $\vec{u} = [u_d \ u_q]^T$.

In Sliding Mode Control, the goal is to force the system error to belong to the predefined manifold in the state space. This manifold is usually defined with the set of the linear or nonlinear functions called as sliding mode functions. In such a system so called sliding mode may occur, exhibiting new type of the motion of the system. Thus, the sliding mode existence conditions and the equations of motion in the sliding mode

should be derived in order to understand the benefits of establishing sliding mode motion in the control system. As shown earlier the switching power converters are described by the following model (2.12). For our explanations of the properties of behavior of the systems with sliding modes we will use a system defined by the following equation:

$$\dot{\bar{x}} = \bar{f}(x, t) + B\bar{u} \quad (3.2)$$

where $\bar{u} = [u_d \ u_q]^T$ is the control-input vector, $\bar{x} = [x_d \ x_q]^T$ system state vector and $\bar{f}(x, t) = [f_d \ f_q]^T$ is a continuous 1x2 vector valued function.

Assuming that the switching manifold is selected as

$$S = \{\bar{x} : \bar{\sigma}(x, t) = G \cdot (\bar{x} - \bar{x}^r) = 0\} \quad (3.3)$$

where \bar{x}^r is the reference vector corresponding to the desired output, and $G = (\partial \bar{\sigma} / \partial \bar{x})$ is a 2x2 matrix, with gradients of functions $\bar{\sigma}_i(x)$, can be regarded as gain.

To study the behavior of the system in sliding mode the projection of the system in the sliding mode manifold should be derived first. For system (3.2), (3.3) this projection has the form as in (3.4). In order to guarantee that system belongs to the sliding manifold the origin of the system (3.4) should be stable and system state should reach that origin from initial state. The origin of (3.4) must be reachable in finite time. From the above explanation the sliding mode may occur only in the origin of the system (3.4) and it shall be treated as the stability in small. Contrarily, the reachability should be analyzed as the stability in large since the initial conditions for the system (3.2) may be far away from the sliding manifold.

The motion of the system on the sliding mode manifold can be derived using the so-called equivalent method. In this method, the control derived from the solution of the equation $\dot{\bar{\sigma}} \Big|_{\bar{u}=\bar{u}_{eq}} = 0$ is put back to the original equations and new set of the equations with $\bar{\sigma} = 0$ represents the dynamical model that governs the behavior of the system in the sliding mode. Assuming the matrix $(G \cdot B)$ has an inverse, equivalent control can be derived as

$$\dot{\vec{\sigma}} = G\vec{f} + GB\vec{u} = 0 \Rightarrow \vec{u} = \vec{u}_{eq} = -(G \cdot B)^{-1} \cdot G\vec{f} \quad (3.4)$$

From a geometrical viewpoint, the equivalent control means replacement of discontinuous control in the intersection of switching surfaces by a continuous control such that state velocity vector lies in the tangential manifold. Putting the equivalent control, in other words, the average of the control, back in the equation results in the motion of the system as $\dot{\vec{x}} = \vec{f}(x) + B \cdot \vec{u}_{eq}$ and the velocity of error can be written as:

$$\dot{\vec{\sigma}} = G \cdot B \cdot (\vec{u} - \vec{u}_{eq}) \quad (3.5)$$

Taking into account the changes in control, we see that, basically it has two components: slow and fast components. The plant under control filters out the high frequency changes and slow change determines the motion in the sliding mode. So, it is reasonable to assume that equivalent control approximates to the slow component of control and can be extracted using a low pass filter.

For the three-phase converters in order to have a better understanding of the switching vector selection approach to be realized, first a conventional method called Relay control will be explained and then presented control strategy will be described in detail.

3.2 Relay Control Approach Vector Selection

For the system that has a $\frac{d\vec{i}}{dt} = \vec{f} + B \cdot \vec{u}$ current loop dynamics, say the manifold is selected as $S = \{i : \vec{\sigma} = \vec{i}^r - \vec{i} = 0\}$, and then choosing a positive definite Lyapunov function candidate as

$$v = \vec{\sigma}^T \cdot \vec{\sigma} / 2 \quad (3.6)$$

Its derivative becomes

$$\dot{v} = \vec{\sigma}^T \cdot \dot{\vec{\sigma}} = \vec{\sigma}^T \cdot \left(\frac{d\vec{i}^r}{dt} - \vec{f} - B\vec{u} \right) \quad (3.7)$$

So, if control is selected as

$$\vec{u} = -\vec{H} \cdot \text{sign}(\vec{\sigma}) \quad (3.8)$$

where $\vec{H} = \begin{bmatrix} H_d & 0 \\ 0 & H_q \end{bmatrix}$, with $\|\vec{\sigma}^T \cdot B \cdot \vec{H}\| > \left\| \vec{\sigma}^T \cdot \left(-\frac{d\vec{i}^r}{dt} + \vec{f} \right) \right\|$, derivative of the

Lypunov function candidate becomes negative that means origin $\sigma = 0$ is stable.

Now having control as:

$$\begin{aligned} u_d &= -H_d \cdot \text{sign}(\sigma_d) \\ u_q &= -H_q \cdot \text{sign}(\sigma_q) \end{aligned} \quad (3.9)$$

in (dq) frames of reference, the back transformation can be of simply the projection to the (abc) frame of references ensuring the signs which is [5]

$$\begin{aligned} \text{sign}(u_1) &= \text{sign}(u_d \cdot \cos(\theta_r) - u_q \cdot \sin(\theta_r)) \\ \text{sign}(u_2) &= \text{sign}(u_d \cdot \cos(\theta_r - \frac{2\pi}{3}) - u_q \cdot \sin(\theta_r - \frac{2\pi}{3})) \\ \text{sign}(u_3) &= \text{sign}(u_d \cdot \cos(\theta_r - \frac{4\pi}{3}) - u_q \cdot \sin(\theta_r - \frac{4\pi}{3})) \end{aligned} \quad (3.10)$$

This back transformation has some drawbacks. The calculated control in $\vec{u} = -\vec{H} \cdot \text{sign}(\vec{\sigma})$ is continuous, it has an amplitude and the direction data in it. But the control specified in (3.10) does not have the corresponding amplitude data. In addition, the exact direction data is not satisfied. Figure 3.1 illustrates the zone in which the theoretical control should exist and applicable controls corresponding to the theoretical control for a particular system state.

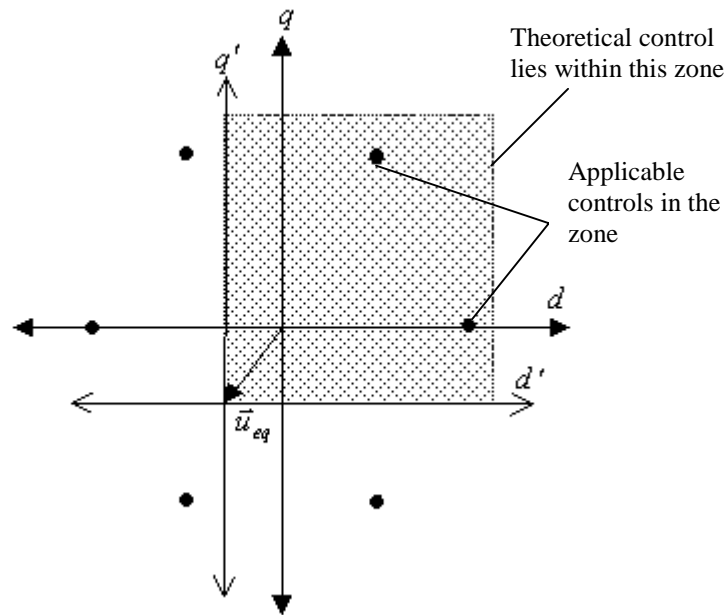


Figure 3.1 Theoretical control and applicable controls for Relay control scheme for a particular system state

Timing of control, that is time instant that the control vector is changed to another is determined whenever the error hits preset error bounds. As mentioned in the introduction chapter, such a conventional tracking control algorithm may provide the proper selection of switching vector but not the proper timing since switching timing occurs only when the control error is contacted pre-set hysteresis bounds. This generates big harmonic distortion, especially in low order harmonics.

Quality of the switching control algorithm is determined by both proper selection of the switching vector and the proper switching timing. Such an approach has been studied in [9], and we will use the basic idea of their study for the realization of the current control loop.

The basic idea of the approach is to evaluate harmonic distortion in real time with instantaneous THD definition and selects necessary sequence of the switching determined according to the THD minimization theorem.

3.3 Description of the THD Minimization Algorithm

This algorithm is applicable for the 3-phase converters current control loop and is intended for discrete-time implementation. Basically, the algorithm calculates 2 vectors for each control period. One of them is targeted to minimize the tracking error at the end of the control period while the other is targeted to improve Instantaneous Total Harmonic Distortion. Thus, the algorithm evaluates harmonic distortion in real time with instantaneous THD definition and sequentially selects two switching vectors in one control period in order to minimize the tracking error and improve Instantaneous Total Harmonic Distortion while timing of the second vector is determined according to the THD minimization theorem.

Error in current is defined as a two-component vector

$$\vec{\sigma} = \vec{i} - \vec{i}^r \quad (3.11)$$

where $\vec{\sigma} = [\sigma_d \quad \sigma_q]^T$, $\vec{i}^T = [i_d \quad i_q]^T$, $\vec{i}^r = [i_d^r \quad i_q^r]^T$, and normalizing the time axis with respect to converters switches switching interval T as:

$$\tau = \frac{t}{T} \quad (3.12)$$

the motion of error in one control period can be written as in (3.13)

$$\vec{\sigma}(\tau) = \vec{\sigma}(0) + \tau \cdot \vec{\sigma} \quad (3.13)$$

In (3.13), $\vec{\sigma}(0)$ denotes the error at the beginning of the switching interval and $\vec{\sigma} = [\dot{\sigma}_d \ \dot{\sigma}_q]^T$ is the velocity of the error vector, assuming the applied vector at $t=kT$ will be fixed during the whole control period T . Real time axis and normalization of time axis both with sampling instances are illustrated in Figure 3.2 .

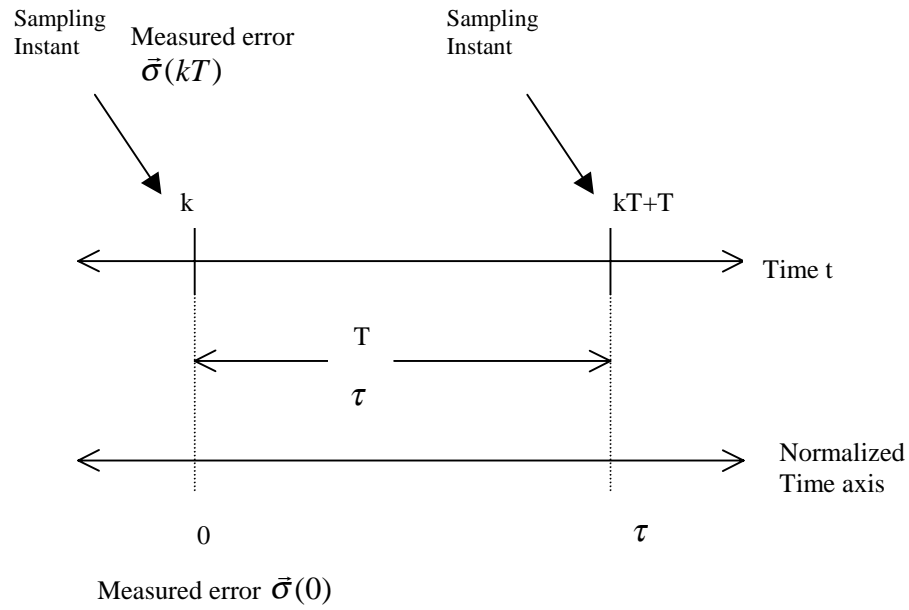


Figure 3.2 Illustration of measurement instances both at real time axis and normalized time axis and calling convention

Let \vec{D}_i be the displacement of the error from $t=kT$ to $t=kT+T$ corresponding to i^{th} control vector which would be on the plant and fixed during the whole control period. Thus it is defined as $\vec{D}_i = \vec{\sigma}_i \tau$ where $\vec{\sigma}_i$ is the velocity of the error corresponding to the i^{th} permissible switching vector. Note that $\vec{\sigma}$ is given by (3.5). The relationship between the permissible switching vectors and velocity of error is shown in Figure 3.3.

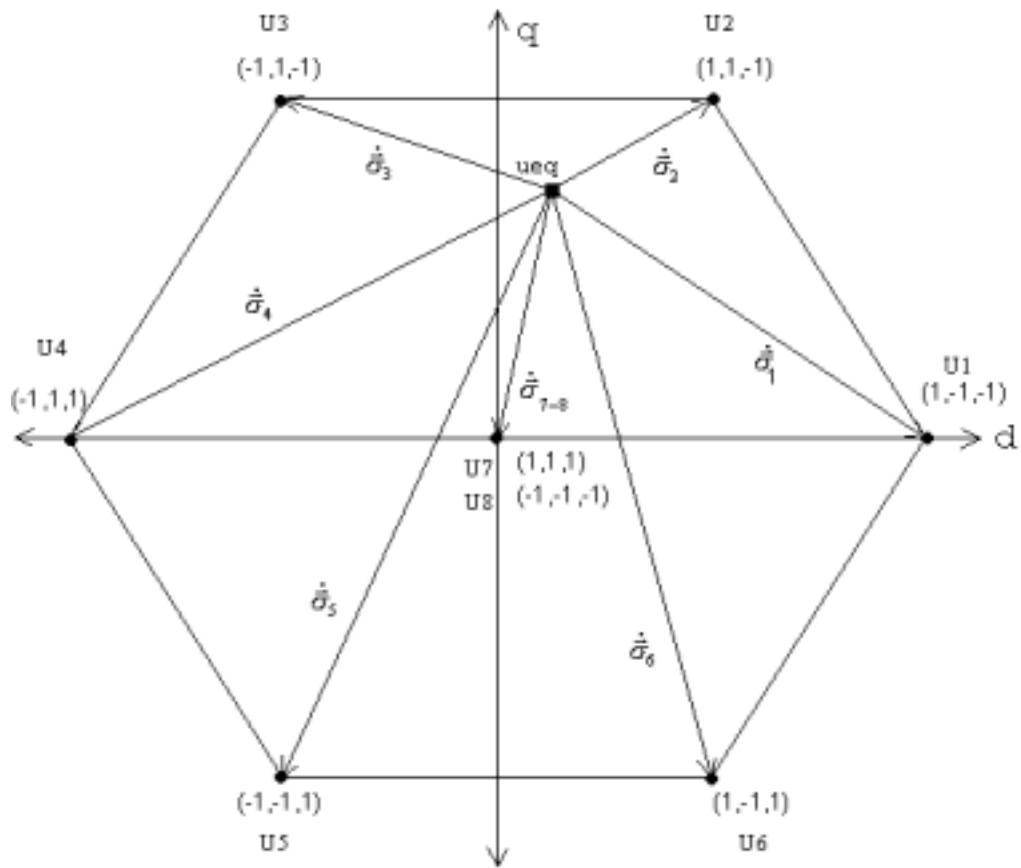


Figure 3.3 Illustration of derivative of error on the possible control vectors

Knowing the velocity of the error corresponding to a certain vector and the initial error, final error, that is the error at the end of the control period, can be calculated corresponding to that particular control vector. In Figure 3.4, if a particular vector will be applied to the plant, error at the end of the control period, that is $\bar{\sigma}(\tau)$, corresponding to the switching vectors is shown .

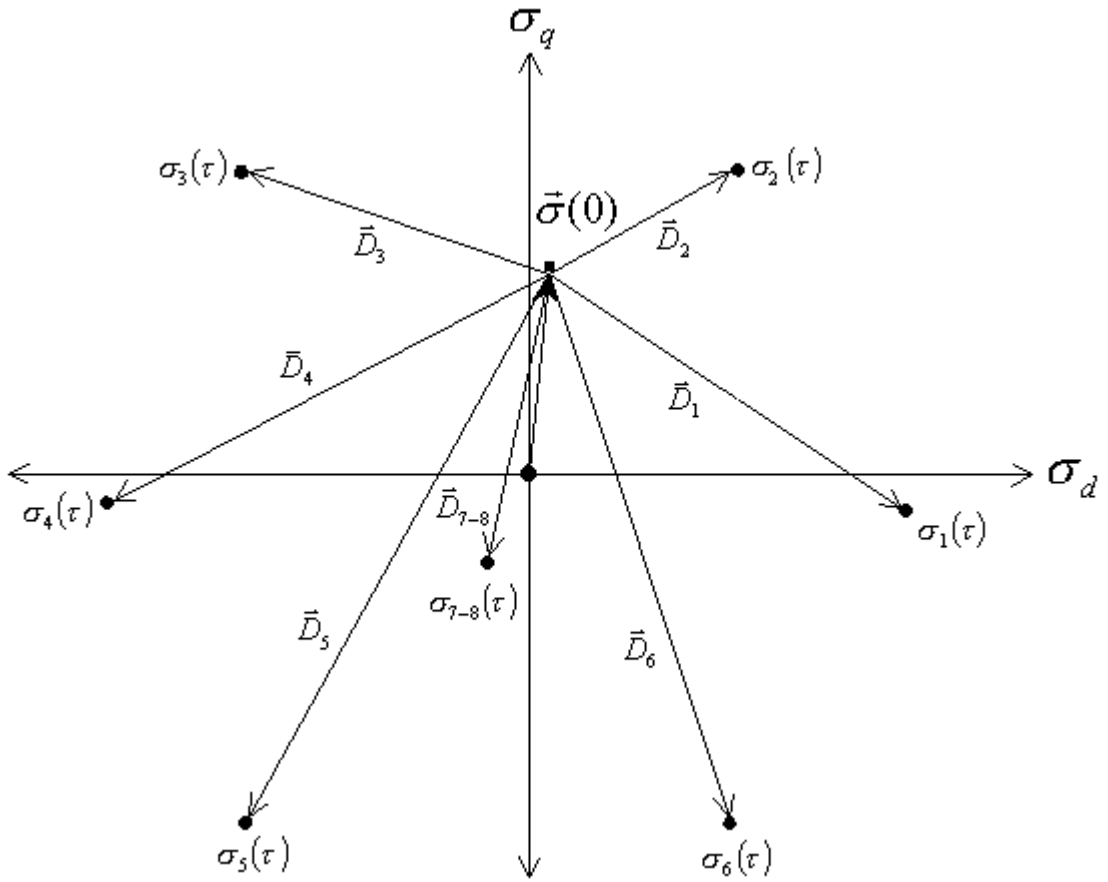


Figure 3.4 Illustration of final errors corresponding to possible vectors for a particular initial error

The vector delivered to the plant at the beginning of every control period, at $t=kT$ (in normalized time $\tau = 0$), targeting to minimize the tracking error at the end of the control period, at $t=kT+T$ (in normalized time $\tau = 1$), will be referred as **First Vector** - U_I . The other vector, targeting minimizing the final error, too, to be delivered to the plant within the control period ($kT, kT+T$) will be referred as **Second vector** - U_{II} . Timing instant for the Second Vector targets to improve the Instantaneous THD.

Generally speaking, some timing instant in normalized time axis, for the second vector will be referred as α . The optimal timing instant, in normalized time axis, which minimizes the Instantaneous THD will be referred as α^{opt} .

3.3.1 Selection of the First Vector

In the selection of the First vector, the main idea is, if the first vector is selected during the full control period, the final error will be minimum. Final error corresponding to i^{th} control vector can be expressed as

$$\|\vec{\sigma}(\tau)\| = \|\vec{\sigma}(0) + \vec{D}_i\| \quad (3.14)$$

Thus, selection of first vector can be expressed as;

$$\text{First vector } U_i = \left\{ U_i \mid \min_i \|\vec{\sigma}(0) + \vec{D}_i\| \right\} \quad (3.15)$$

Selection of First Vector, for an arbitrary initial error, is depicted in Figure 3.5.

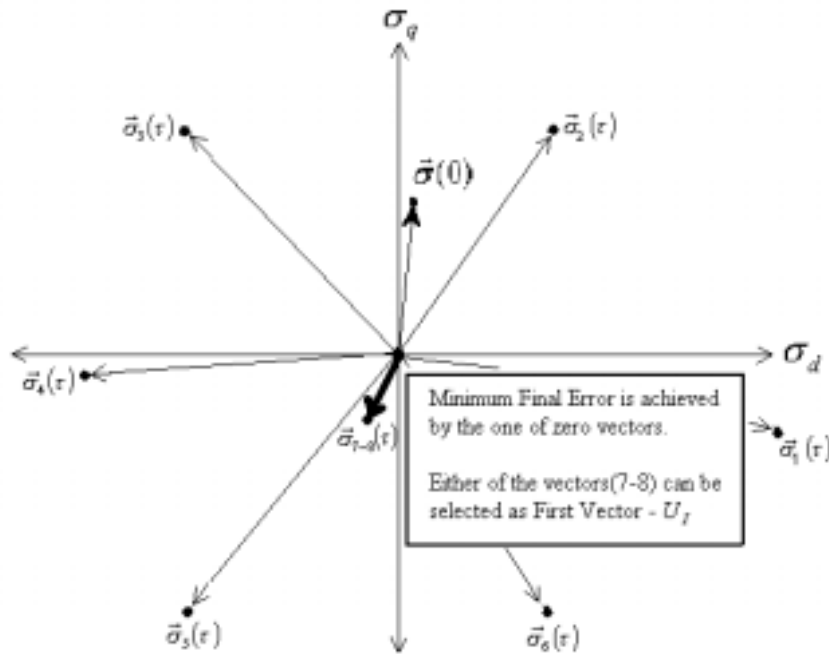


Figure 3.5 Illustration of selection of first vector that causes minimum final error

3.3.2 Selection of the Second Vector

In the selection of the second vector, the governing principle is if the First vector U_I is selected and changed to second vector at some proper timing $\tau = \alpha$, final error, $\sigma(\tau)$, will be nearest to zero.

Selection of Second Vector is illustrated in Figure 3.6. In the figure, two displacement vectors corresponding to the selected vectors, for an arbitrary initial error $\vec{\sigma}(0)$, are shown. If First vector would be applied during the whole control period, the error would come to point K. If Second vector would be applied during the whole control period, the error would come to point L. When the First Vector is applied to the plant, the initial error $\vec{\sigma}(0)$ will move along \vec{D}_I . Before the movement is completed, in other words within the control period, at some time, say time $\tau = \alpha$, if controller jumps to the second vector, the error will move along the line that is parallel to \vec{D}_{II} and will hit to the $\vec{D}_{II} - \vec{D}_I$ at the end of the control period. Thus U_{II} should be selected such that the final error is minimum.

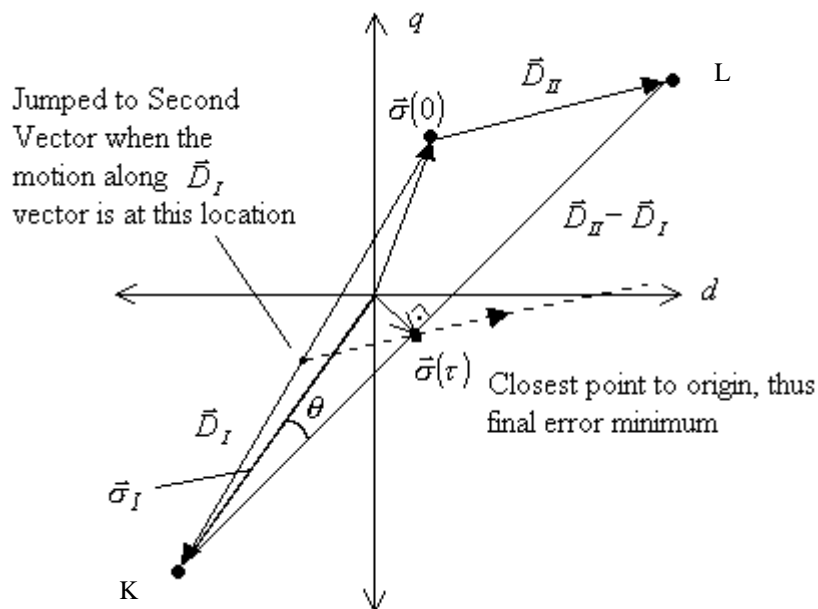


Figure 3.6 Selection of second the vector

Application of the First vector U_I between $[0, \alpha]$ and then jumping to the Second vector for the interval $(\alpha, 1)$, in normalized time, is to be considered. Let \vec{D}_I be the displacement of error within a control period corresponding to the selected first vector. Since the final error will be on the vector $\vec{D}_i - \vec{D}_I$, the closest point is the intersection of the lines from origin to the $\vec{D}_i - \vec{D}_I$ vector which results with the final error

$$\|\vec{\sigma}(\tau)\| = \|\vec{\sigma}_I\| \cdot \sin(\theta) \quad (3.16)$$

Thus the smaller the theta, the smaller the final error. Minimizing θ means minimization of the inner product of the following vectors that is expressed as;

$$\text{Second vector } U_{II} = \left\{ U_i \mid \min_i \left\| \left(\vec{\sigma}(0) + \vec{D}_I \right)^T \cdot \left(\vec{D}_i - \vec{D}_I \right) \right\| \right\} \quad (3.17)$$

At the moment that First vector is selected, Second vector is selected, too.

3.3.3 Selection of Timing

The Selection of timing is determined according to THD minimization. Let \vec{D}_{II} be the displacement of error during the whole control period corresponding to the selected second vector if selected second vector would be applied to the plant during the whole control period.

Instantaneous THD is defined as $\zeta = \int_0^1 \|\vec{\sigma}(\tau)\|^2 d\tau$, and the value of α minimizing ζ is:

$$\alpha^{opt} = \frac{\left(\vec{D}_{II} + 2\vec{\sigma}(0) \right)^T \cdot \left(\vec{D}_{II} - \vec{D}_I \right)}{\left(\vec{D}_{II} - 2\vec{D}_I \right)^T \cdot \left(\vec{D}_{II} - \vec{D}_I \right)} \quad (3.18)$$

If the solution of α^{opt} falls in $0 \sim 1$, then two vectors will be selected during one control period, otherwise, only one vector is selected that excludes useless switching actions.

3.3.4 Obtaining Equivalent Control

Equivalent control is defined as the control, needed to keep the system on the manifold if the system is on the manifold

$$\vec{u}_{eq} = -(G \cdot B)^{-1} \cdot G \cdot \vec{f} \quad (3.19)$$

Equivalent control is used to determine the velocity of error as stated in (3.5), so that the presented algorithm proceeds and selects the control vectors. When (3.19) is considered, over \vec{f} , equivalent control is very dependent on the plant parameters. Not only the change of parameters but also computation is problematic.

On the other hand, taking into account the equivalent control as the slow frequency component of the control, it can be obtained by filtering the control such as

$$\tau_{LPF} \cdot \dot{\hat{u}}_{eq} + \hat{u}_{eq} = \vec{u} \quad (3.20)$$

will converge to equivalent control. Here \hat{u}_{eq} is the approximated equivalent control.

3.3.5 Getting Use of Zero Vectors

There are 2 combination of the switches for Boost Rectifier and Buck Inverter, and 3 vectors for Boost Inverter and Buck Rectifier that result in the zero control vector. Since their values are the same, they cause the same error motion on the plant. Thus this offers an option when a zero vector is selected by the algorithm. The realization of the zero vector shall be selected in such a way that the number of the switches that should change their state should be minimal.

For a Boost Rectifier or a Buck Inverter, application of a zero vector after vector U_3 - that is $(-1, 1, -1)$ - would cause the following actions according to the preferred zero vector.

If U_8 is preferred, that is $(-1,-1,-1)$,

- OFF the upper transistor of the phase b leg of the switching matrix
 - ON the lower transistor of the phase b leg of the switching matrix
- ends up with 2 actions.

On the other hand if U_7 preferred, that is $(1,1,1)$,

- ON the upper transistor of the phase a leg of the switching matrix
 - OFF the lower transistor of the phase a leg of the switching matrix
 - ON the upper transistor of the phase c leg of the switching matrix
 - OFF the upper transistor of the phase c leg of the switching matrix
- ends up with 4 actions.

Thus, preference of the zero vectors, taking into account the previous control vector, reduces the number of switching actions. The look-up tables for zero vector selection is shown in Table 3 and Table 4

Table 3. Zero vector look-up table to reduce the number of switching actions for Boost Rectifier and Buck Inverter

Current Vector on the switching matrix	Zero vector to be applied
U_2 or U_4 or U_6 or U_7	U_7
U_1 or U_3 or U_5 or U_8	U_8

Table 4. Zero vector look-up table to reduce the number of switching actions for Boost Inverter and Buck Rectifier

Current Vector on the switching matrix	Zero vector to be applied
U_1 or U_3 or U_4 or U_6 or U_7	U_7
U_2 or U_3 or U_5 or U_6 or U_8	U_8
U_1 or U_2 or U_4 or U_5 or U_9	U_9

4. SIMULATION RESULTS

Simulations are performed on Boost Rectifier and Buck Inverter. AC current control for these plants is simulated both with THD Minimization algorithm and Relay Control Algorithm. Matlab/Simulink files for all the simulations are in Appendix-A. Results, regarding the dynamic response, steady state ripple, number of switching at steady state, Total harmonic distortion of phase currents, regularity of switching are compared. Also, the Voltage controller is integrated to presented current control scheme and completely controlled plant outputs are observed.

The Total Harmonic Distorsion in phase currents is measured according to

$$THD = \frac{\sqrt{\sum_{j=2}^N R_j^2}}{R_1} \quad (4.1)$$

where R_j is the RMS value of the j^{th} harmonic and R_1 is the RMS value of the fundamental component of the AC side currents.

4.1 Boost Rectifier Simulation

System requirements for a well controlled three-phase Boost Rectifier are

- The output voltage should track its reference value V_o^{ref}
- Input current should be sinusoidal
- The input current phase angle should trace its reference value $\phi^{ref} = \tan^{-1}\left(\frac{i_d^{ref}}{i_q^{ref}}\right)$

Parameters used in Boost Rectifier simulation are shown in Table 5.

Table 5 Parameters for Boost Rectifier

R (Resistance)	L (Inductance)	C (Capacitance)	V _g (Input Voltage Amplitude)	ω (Input Voltage Frequency)
50 Ω	20 mH	700 μ F	10 V	50 Hz

4.1.1 Simulation for Current Control with THD Minimization Algorithm for Boost Rectifier

Simulated system is shown in Figure 4.1. It consists of Boost Rectifier as plant and current controller employing THD Minimization algorithm. Control inputs for the Boost rectifier system is set as d component of current and input currents phase angle that also determines the q component of current.

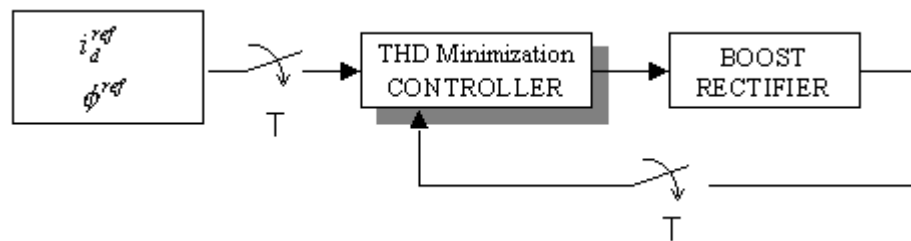


Figure 4.1 Simulation of Current Loop of Boost Rectifier with THD Minimization control scheme

In this simulation, sampling period (T) is set to 50 μ s. We inserted a computational delay of 20 μ s for the controller. Timing scheme used in this simulation is shown in Figure 4.2.

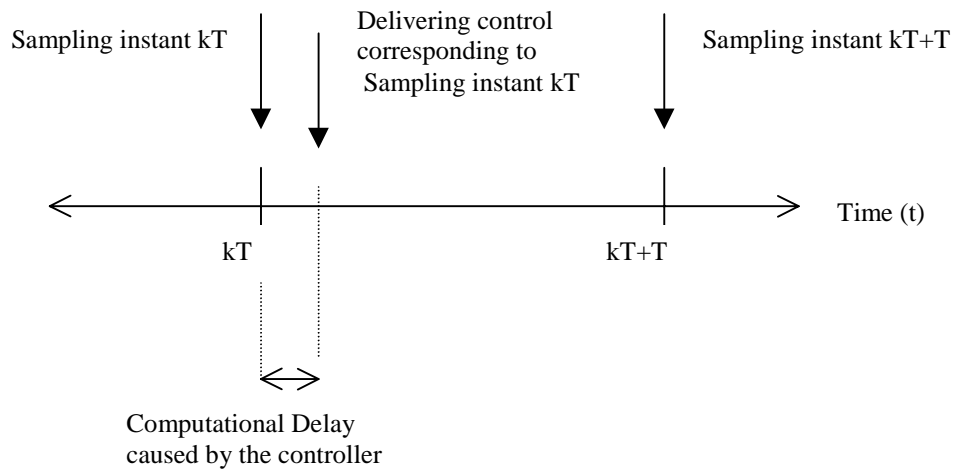


Figure 4.2 Timing scheme of the Boost Rectifier under THD Minimization controller

Current references are given in (dq) frames of references as follows:

The q component of the current is controlled via ϕ^{ref} which is set to 0° degrees until time 0.1 seconds ($t=0.1$ s) to have unity power factor and then changed to 45° degrees. d component of the current is set to 2.5 A until time 0.1 seconds and then changed to 3 A. In Figure 4.3, reference currents, tracking of plant currents and the ripple are shown. Ripple in currents is maximum 50 mA-pp.

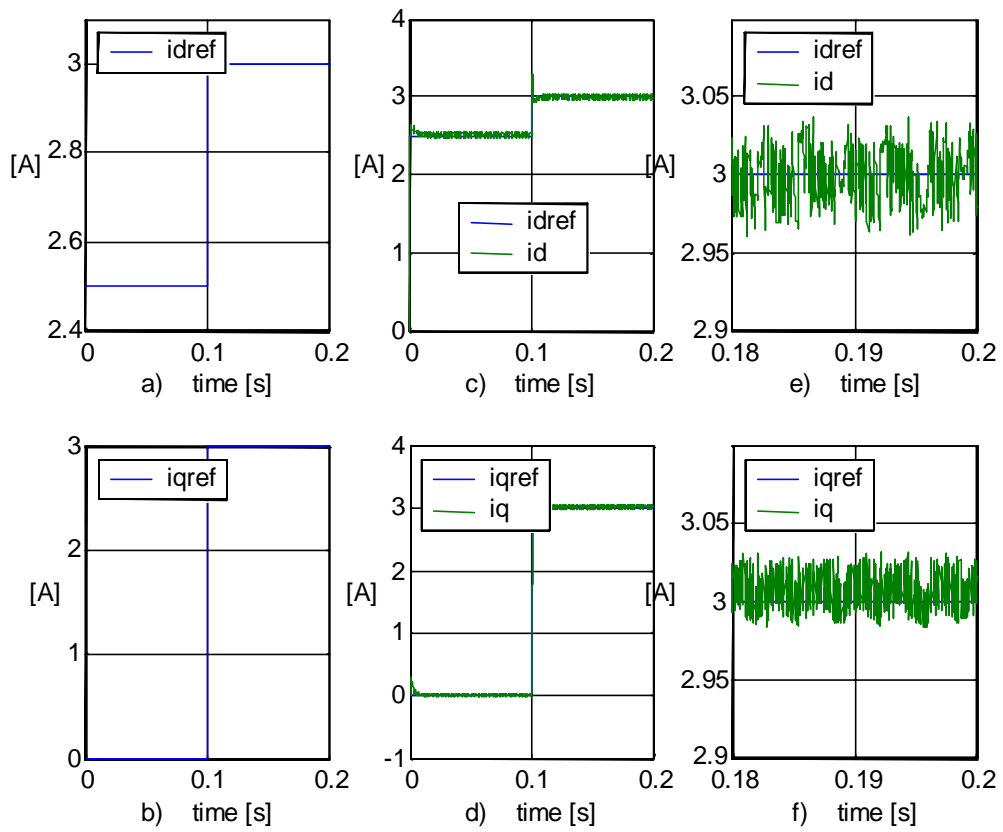


Figure 4.3 a) Reference current d component reference b) Reference current q component reference c) Tracking for d component d) Tracking for q component current e) Ripple for d component f) Ripple for q component of currents in (dq) frame for Boost Rectifier under THD Minimization control scheme

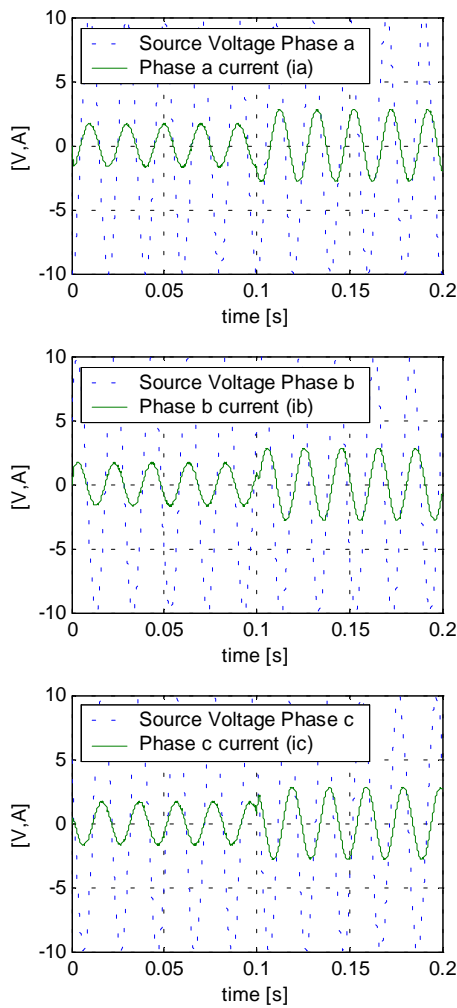


Figure 4.4 Input source voltages and input currents for Boost Rectifier under THD Minimization control scheme

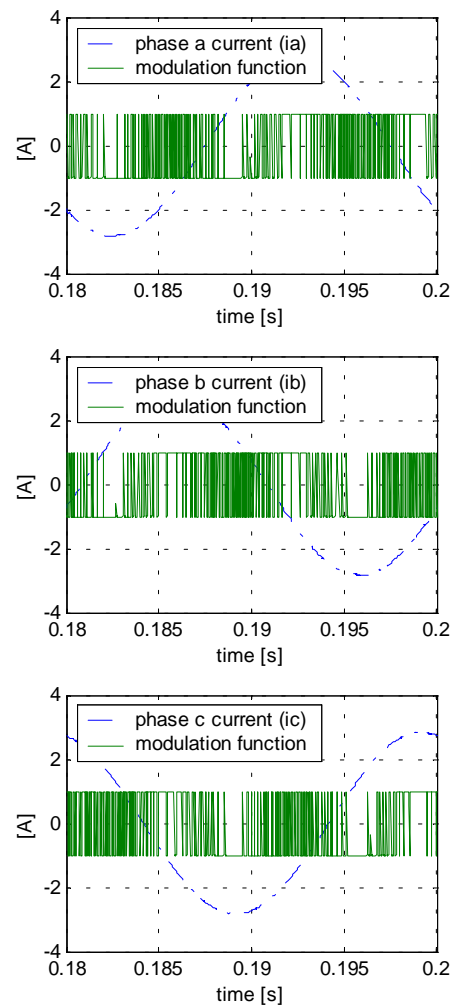


Figure 4.5 Steady state input currents and corresponding modulation functions for one period of input voltage for Boost Rectifier under THD Minimization control scheme

In Figure 4.4, input source voltages and input currents are presented to show the agreement of the change of the angle and the proper sinusoidal waveform of the currents. Since phase angle is changed from 0° degrees to 45° degrees at time 0.1 s, a sharp change in currents is observed at that instant. Before that time ($t=0.1$ s), voltages and currents are in phase as asked, and then shifted for 45° degrees as asked, too. In

Figure 4.5, steady state waveforms of phase current and modulation function of switches are presented for one period of input voltage.

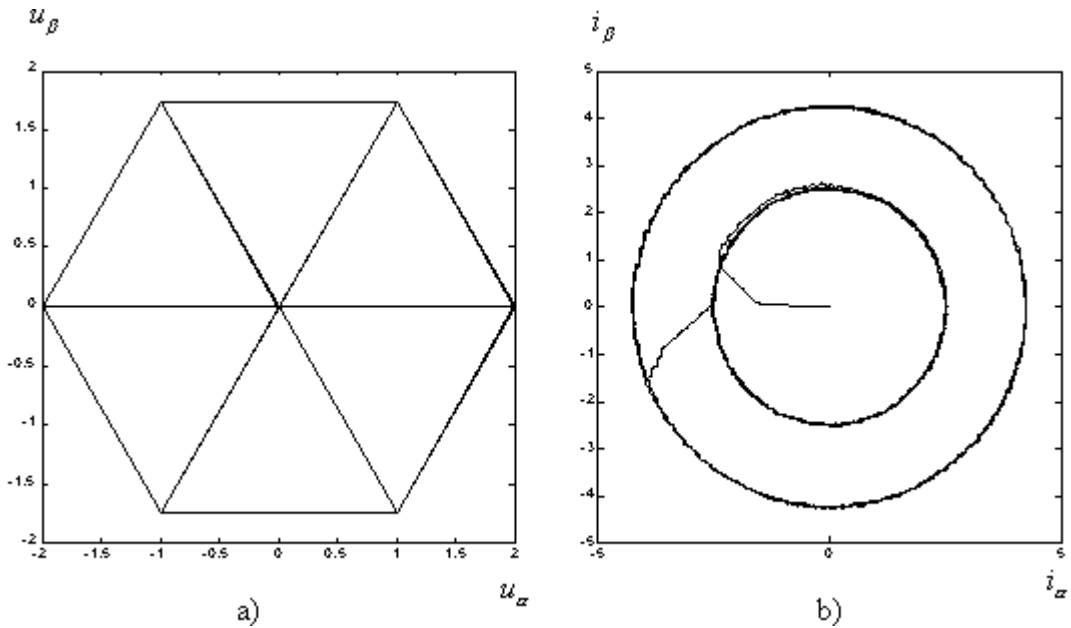


Figure 4.6 a) Control vector shown in $(\alpha\beta)$ frames of references b) Input currents shown in $(\alpha\beta)$ frames of references for Boost Rectifier under THD Minimization control scheme

In Figure 4.6, control vector in $(\alpha\beta)$ frames of references and the input currents in $(\alpha\beta)$ frames are illustrated. Selection of control vectors is regular so higher frequency harmonics and transients are avoided. Input currents shown in $(\alpha\beta)$ frame also verifies the fast dynamic response and small ripple. In Table 6, Total harmonic distortions for input currents are listed.

Table 6. Total harmonic distortions of the phase currents for 50 Hz fundamental Boost Rectifier under THD Minimization controller

	THD
Phase a	0.0086
Phase b	0.0085
Phase c	0.0082

4.1.2 Simulation for Current Control with Relay Controller

This simulation is aimed to see the performance of Relay controller in terms of, ripple of currents, dynamic response, Total Harmonic Distortion, regularity of switching, controller parameters, hysteresis band width, discrete operation with sampling period and carry out a comparison with the THD Minimization algorithm.

Simulated system is shown in Figure 4.7. It consists of Boost Rectifier as plant and current controller employing Relay Control algorithm. Control inputs for the Boost rectifier system is set as d component of current and input currents phase angle that also determines the q component of current.

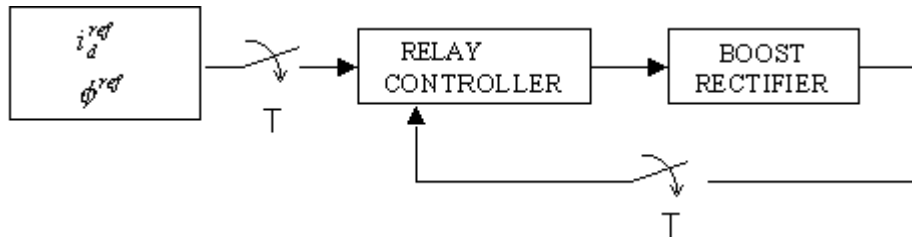


Figure 4.7 Simulation of Current Loop of Boost Rectifier with Relay Control

The ripple for presented algorithm is 50 mA-pp. The hysteresis band width is set to ± 0.05 A. To give the facility of same number of switchings, Sampling Period is set to 25 μ s. In addition, no computational delay is employed for Relay Controller. Timing scheme for this simulation is shown in Figure 4.8.

The same reference current profiles, required from the THD Minimization controller, are asked, q component of the current is controlled via ϕ^{ref} which is set to 0° degrees until time 0.1 s ($t=0.1$ s) to have unity power factor and changed to 45° degrees.

d component is set to 2.5 A and then changed to 3 A at time 0.1 s to illustrate the transients.

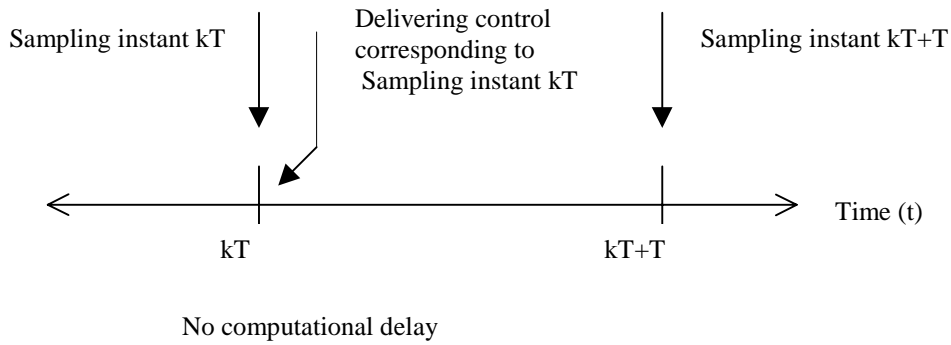


Figure 4.8 Timing scheme of the Relay Controller for Boost Rectifier

In Figure 4.9, reference currents, tracking of plant currents and the ripple are shown. Ripple in currents is 80 mA-pp. Although the relay band is set to 50 mA-pp, the ripple is greater. If Relay Controller would have been operated in continuous time, it would have sustained the ripple exactly the same value set by its hysteresis band. The deviation is caused by the discrete operation of the Relay Controller since it is not designed for discrete-time operation.

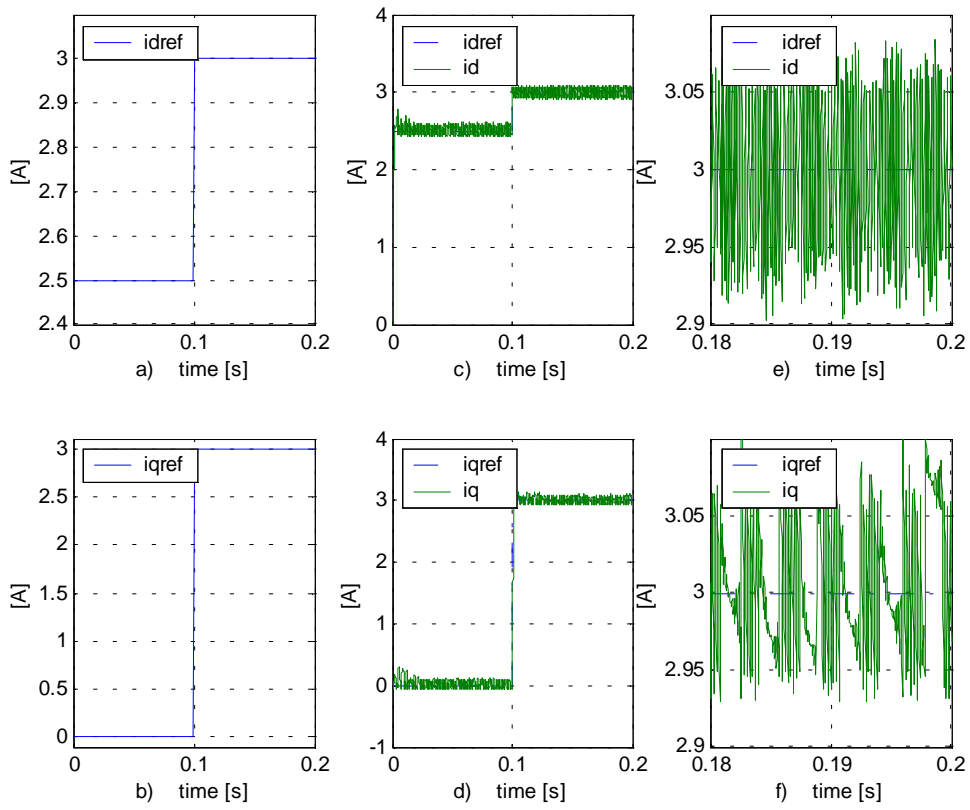


Figure 4.9 a) Reference current d component reference b) Reference current q component reference c) Tracking for d component d) Tracking for q component current e) Ripple for d component f) Ripple for q component of currents in (dq) frame for Boost Rectifier under Relay control scheme

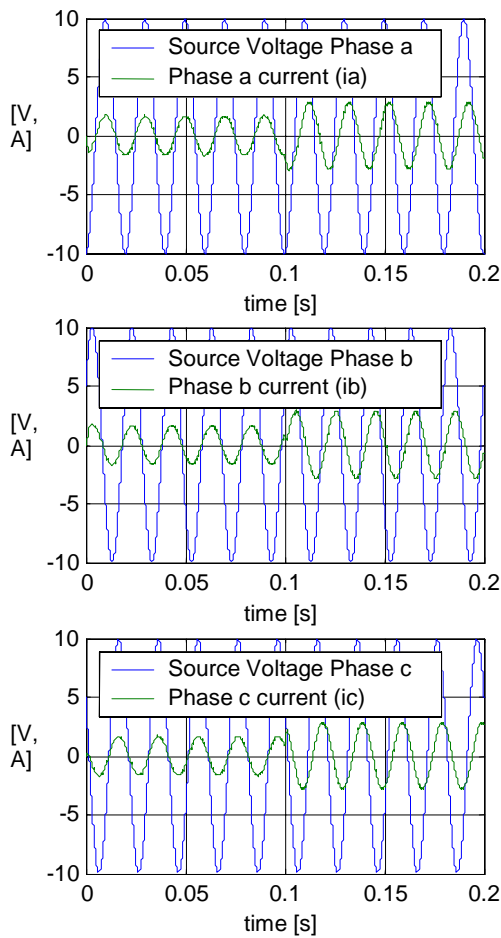


Figure 4.10 Input source voltages and input currents for Boost Rectifier under Relay control scheme

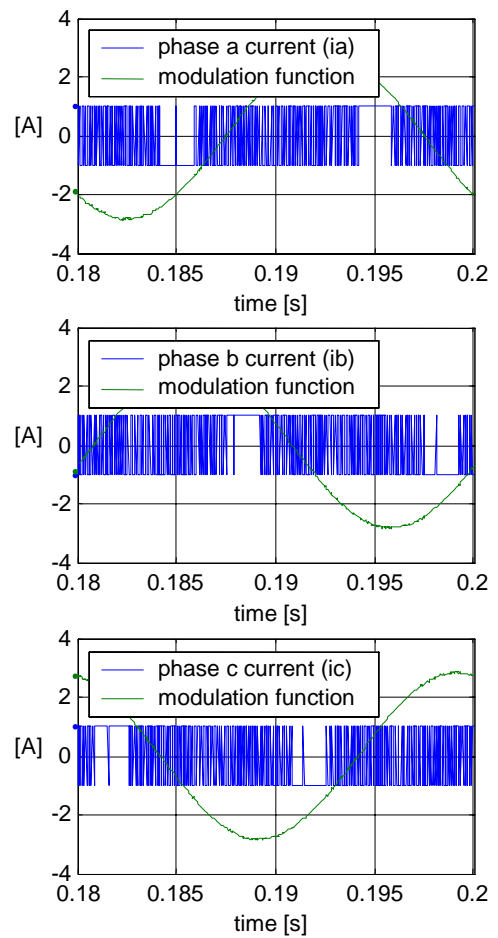


Figure 4.11 Steady state input currents and corresponding modulation functions for one period of input voltage for Boost Rectifier under Relay control scheme

In Figure 4.10, input source voltages and input currents are presented to show the agreement of the change of the angle and the proper sinusoidal waveform of the currents.

In Figure 4.11, steady state waveforms of phase current and modulation function of switches are presented. It is seen that number of switchings are greater than that of THD Minimization algorithm.

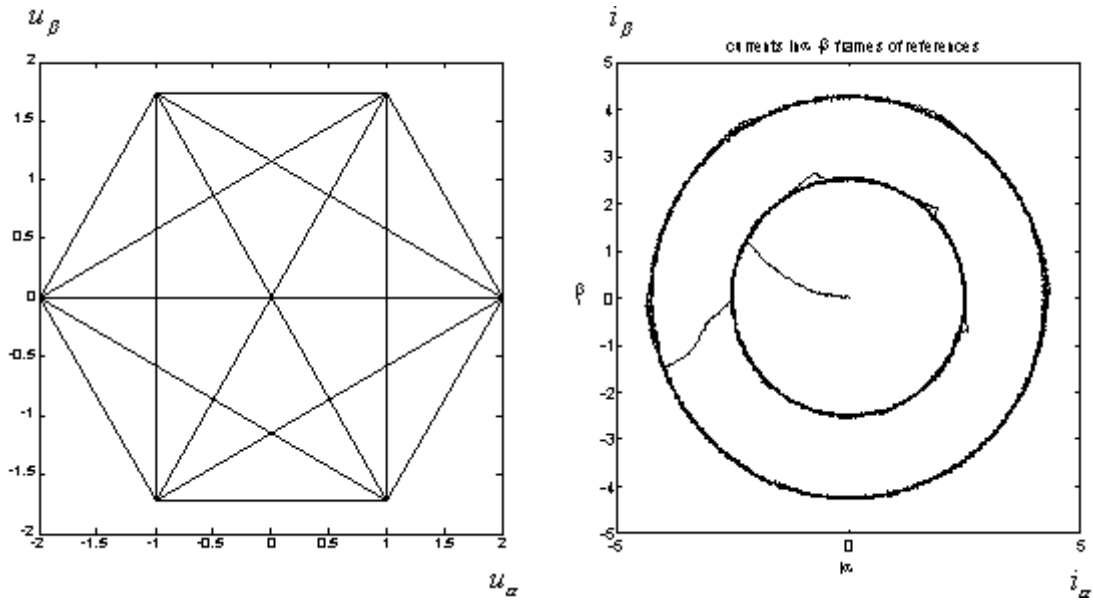


Figure 4.12 a) Control vectors in $(\alpha\beta)$ frame b) Input currents in $(\alpha\beta)$ frame
for Boost Rectifier under Relay control scheme

In Figure 4.12, Modulation functions in $(\alpha\beta)$ frame and input currents are shown in $(\alpha\beta)$ frames of references. Selected switching vectors are not regular that causes undesired high frequency harmonics and transitions at the switches. In Table 7, total harmonic distortions for input currents are listed.

Table 7. Total harmonic distortions of the phase currents for 50 Hz fundamental for Boost Rectifier under Relay control scheme

	THD
Phase a	0.013
Phase b	0.013
Phase c	0.013

4.1.3 Comparison of Relay Control Algorithm and THD Minimization Algorithm on Boost Rectifier

Current loop, with same reference current profiles, is simulated with both Relay Control and THD Minimization control on Boost Rectifier. And results are summarized as follows:

Table 8. Comparison of control algorithm performances for Boost Rectifier based on simulation results

	Relay Control	THD Minimization Control
Sampling Period (T)	25 μ s	50 μ s
Computational Delay	0 s	20 μ s
Ripple in currents	± 40 mA	± 25 mA
Settling time of currents for the step change in reference	2 ms	2 ms
Total Harmonic Distortion at AC currents	0.013	0.0086
Regularity in switching	No	Yes
Number of switchings	More	Less
Computational Load	Less	More

From simulation results, one can easily conclude that, THD Minimization algorithm is functioning correctly. Relay controller has functioned at, not only ideal conditions ,in other words infinite computation speed, but also had the possibility of higher frequency.

Although having more disadvantageous conditions (but closer to real life conditions), THD Minimization algorithm not only succeeds in minimization of Total Harmonic Distorsion but also succeeds in better tracking performance with less number of switching actions.

4.1.4 Voltage Control Design

Continuous nonlinear dynamical system, linear with respect to control

$$\frac{dx}{dt} = f(x,t) + B(x,t)u(x,t) \quad x \in \mathfrak{X}^n, u \in \mathfrak{X}^m \quad (4.2)$$

where all elements of vector f and matrix B are continuous and bounded, and having continuous and bounded first order time derivatives. Rank $B(x,t)=m, \forall x,t>0$ and all components of control input u are bounded by known functions $u_{i\min}$ and $u_{i\max}$. The aim is to stabilize the system motion on the smooth manifold

$$S = \left\{ x : \sigma(x,t) = 0; G(x,t) = \frac{\partial \sigma}{\partial x} \right\} \quad (4.3)$$

where $\sigma \in \mathfrak{X}^m$, and all elements of $\frac{\partial \sigma}{\partial t}$ and G are continuous and bounded and rank $G=m, \forall x,t>0$.

Selecting Lyapunov function candidate in quadratic form

$$v = \frac{\sigma^T \cdot \sigma}{2} \quad (4.4)$$

and putting its derivative into the following form:

$$\frac{dv}{dt} = -\sigma^T \cdot \mu \cdot \sigma \quad (4.5)$$

where $\mu > 0$, will lead to

$$\sigma^T \cdot \frac{d\sigma}{dt} = -\sigma^T \cdot \mu \cdot \sigma \Rightarrow \frac{d\sigma}{dt} + \mu \sigma = 0, \forall \sigma \neq 0 \quad (4.6)$$

On the other hand, using the derivative of the error,

$$\frac{d\sigma}{dt} = G(f + Bu) + \frac{\partial\sigma}{\partial t} \quad (4.7)$$

one ends up with the following control input

$$u(x, t) = -(GB)^{-1} \left(\frac{\partial\sigma}{\partial t} + Gf \right) - (GB)^{-1} \cdot \mu \cdot \sigma \quad (4.8)$$

In continuous time control, if one can calculate and apply this control input to the plant, system motion will move towards the manifold since Lypunov Asymptotic stability conditions are satisfied.

The motion of the system on the manifold can be written using the so-called equivalent control concept. Since u_{eq} is the control needed to keep the motion in the manifold if system states are in the manifold

$$\left. \frac{d\sigma}{dt} \right|_{u=u_{eq}} = G(f + Bu_{eq}) + \frac{\partial\sigma}{\partial t} = 0 \Rightarrow u_{eq} = -(GB)^{-1} \cdot (G \cdot f + \frac{\partial\sigma}{\partial t}) \quad (4.9)$$

So system motion equation on the manifold S is

$$\frac{dx}{dt} = f(x, t) + B(x, t) \cdot u_{eq}(x, t) \quad (4.10)$$

So that (4.8) can be organised as follows:

$$u(x, t) = u_{eq}(x, t) - (GB)^{-1} \mu \sigma \quad (4.11)$$

Organising (4.7) and getting use of (4.9) one has

$$\frac{d\sigma}{dt} = GB(u - u_{eq}) \quad (4.12)$$

which leads to write equivalent control as

$$u_{eq} = u - (G.B)^{-1} \cdot \frac{d\sigma}{dt} \quad (4.13)$$

If we assume that u_{eq} does not change significantly within a control period, then we can have the following approximation for (4.11) as

$$u(kT^+) = u_{eq}(kT^-) - (GB)^{-1} \cdot \mu \cdot \sigma(kT^-) \quad (4.14)$$

which can be rewritten as

$$u(kT^+) = u(kT^-) - (GB)^{-1} \cdot (\dot{\sigma}(kT^-) + \mu \cdot \sigma(kT^-)) \quad (4.15)$$

and the following controller:

$$u(kT^+) = u(kT^-) - (GBT)^{-1} \cdot ((1 + \mu T)\sigma(kT) - \sigma(kT - T)) \quad (4.16)$$

which is very convenient for discrete time realization.[14]

Adopting this idea to voltage control of Buck Converters is straightforward, but adoption to Boost Converters needs more effort. Design for Boost Converters is worked at [4].

For Boost Rectifier, assuming the currents are tracking their references, voltage equation becomes

$$\frac{C}{2} \cdot \frac{dV_o^2}{dt} + \frac{V_o^2}{R} = V_{DC} \cdot i_d^{ref} - \frac{L}{2} \left(\frac{d(i_d^{ref})^2}{dt} + \frac{d(i_q^{ref})^2}{dt} \right) \quad (4.17)$$

This equation can be rewritten as follows; assuming that voltage drop on inductance is small leading to the neglect of the second term on the right hand side

$$\frac{C}{2} \cdot \frac{dV_o^2}{dt} + \frac{V_o^2}{R} = V_{DC} \cdot i_d^{ref} \quad (4.18)$$

This subsystem model obeys to the format in (4.2) with the mapping $V_o^2 = x$ and $i_d^{ref} = u$. Thus ;

$$i_d^{ref}(kT) = i_d^{ref}(kT - T) - (GBT)^{-1}((1 + \mu T)\sigma(kT) - \sigma(kT - T)) \quad (4.20)$$

Since currents should be limited, the controller outputs should be bounded as

$$i_d^{ref}(kT) = \text{sat} \left\{ i_d^{ref}(kT - T) - (GBT)^{-1}((1 + \mu T)\sigma(kT) - \sigma(kT - T)) \right\} \quad (4.21)$$

where $B = \frac{2V_{DC}}{C}$ and T is the sampling period for the controller.

And defining the manifold as

$$S = \left\{ x : \sigma(x, t) = x - x^{ref} = V_o^2 - (V_o^{ref})^2 = 0; G(x, t) = \frac{\partial \sigma}{\partial x} = 1 \right\} \quad (4.22)$$

The controller design is completed. Stability issues and upper bound of the control period for this discrete controller will not be discussed. Just the results at [13] will be satisfied and be employed within the Voltage Loop.

4.1.5 Simulation of THD Minimization Algorithm Combined with Voltage Controller

Simulated system is shown in Figure 4.13. It consists of Boost Rectifier as plant and current controller employing THD Minimization algorithm and voltage controller mentioned in 4.1.4. Control inputs is set as Reference output voltage and input currents phase angle that also determines the q component of current.

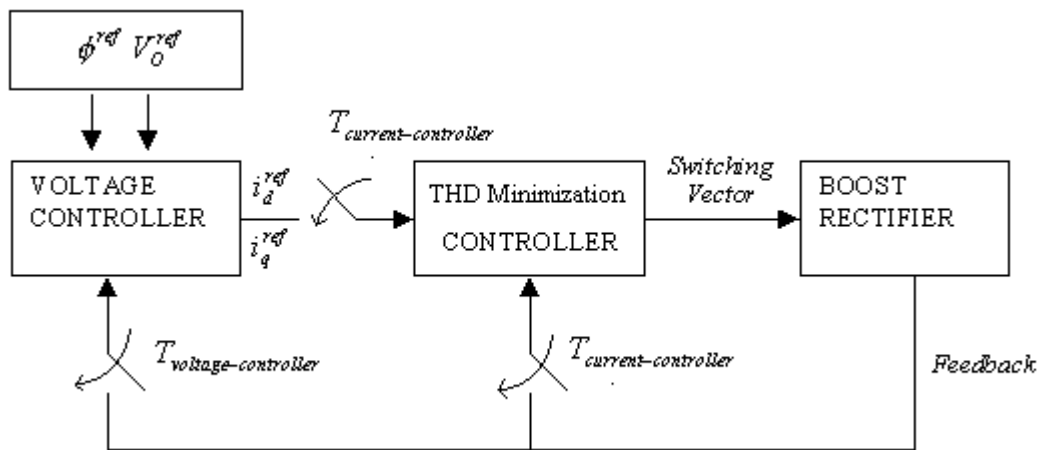


Figure 4.13 Simulation of Boost Rectifier, currents controlled with THD Minimization scheme and voltage controlled by discrete time Sliding Mode Control

Voltage controller structure is out of this work's scope. But for the sake of completeness, the overview is expressed at section 4.1.4. Voltage controller is based on the the extension of continuous Sliding Mode Control to discrete time [14].

In this simulation Voltage loop sampling period is set to 500 μ s and current loop sampling period is set to 50 μ s. Computational delay is set to 25 μ s.

Reference voltage is set to 28 V and changed to 30 V at time 0.2 s. Unity power factor is aimed so the angle is set $\phi^{ref} = 0$. Asked voltage profile and response are shown in Figure 4.14. Ripple at output voltage is ± 0.06 Volts.

In Figure 4.15, input currents and input voltages are shown. They are in phase as asked and currents are clear sinusoids in steady state.

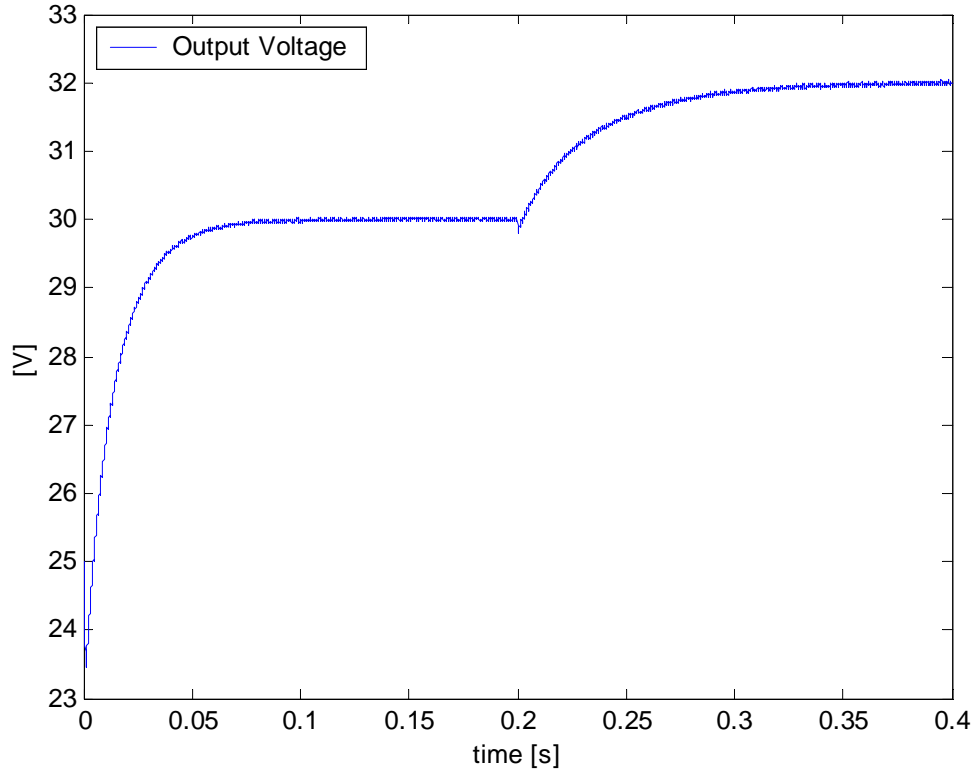


Figure 4.14 Boost rectifier output voltage, currents controlled with presented scheme and voltage controlled by Discrete-Time Sliding Mode Control

In Figure 4.16, in a) control vectors applied to the plant during the simulation, in b) currents in $(\alpha\beta)$ frames and in c) phase a current and corresponding modulation function are shown.

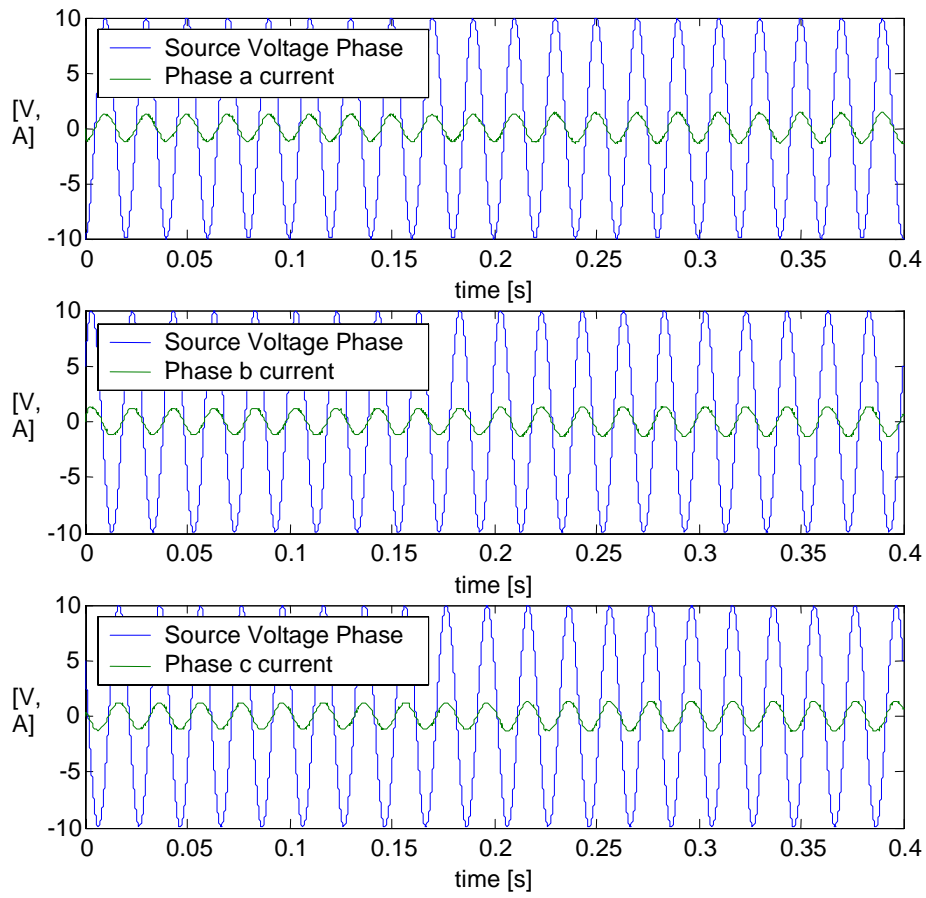
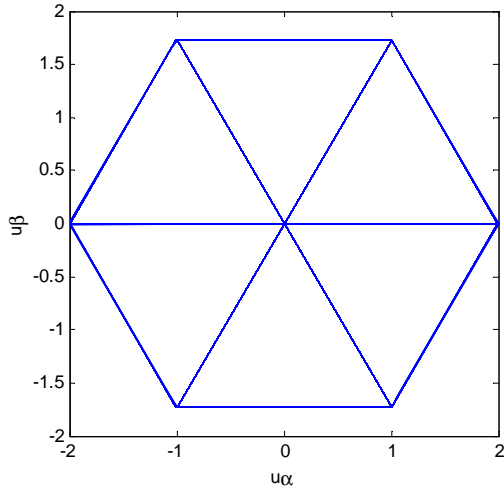
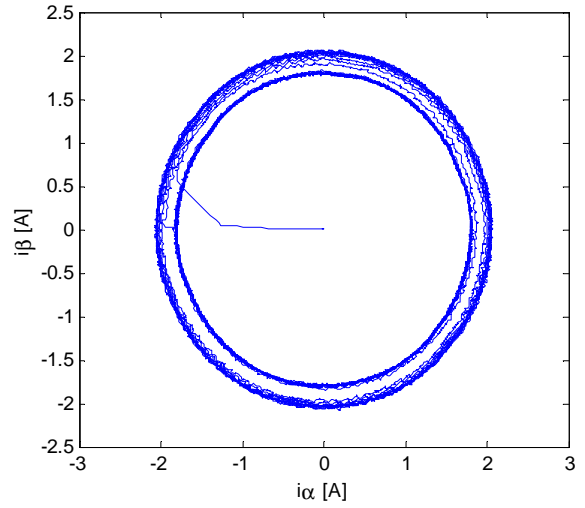


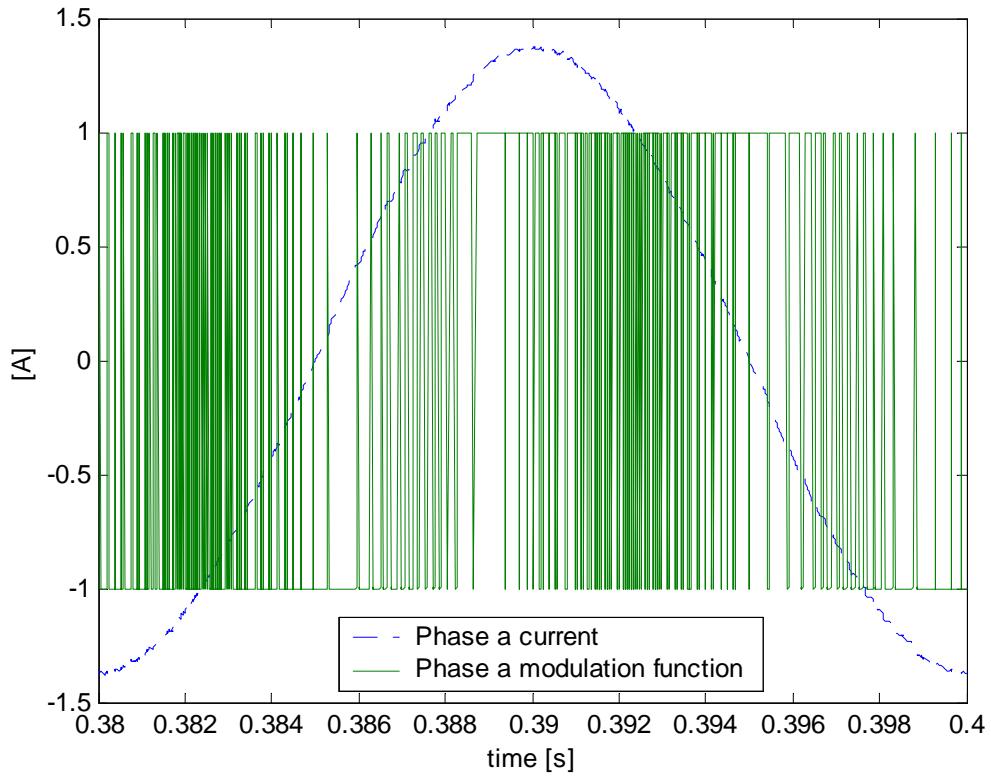
Figure 4.15 Input source voltages and input currents for fully controlled Boost Rectifier



a) Control Vectors in $(\alpha\beta)$ frame



b) Currents in $(\alpha\beta)$ frame



c) Phase a current and corresponding modulation function for one period of input voltage

Figure 4.16 a) Control vectors b) Currents c) Phase a Current and modulation function for completely controlled Boost Rectifier

4.2 Buck Inverter Simulation

Since presented control algorithm is based on the unified description of all 3-Phase Switching power converters, in this part, simulation on an Inverter type converter is performed. on Buck Inverter, current control is simulated both with THD Minimization control scheme and Relay control scheme. System requirements for a well controlled three-phase Buck Inverter are:

- The output voltages should track their reference value, V_o^{ref} , which are supposed to have reference frequency and reference amplitude
- Output currents should be sinusoidal

Parameters used in Buck Inverter simulation are shown in Table 5.

Table 9. Parameters used in Buck Inverter simulation

R (Resistance)	L (Inductance)	C (Capacitance)	Vg (Input Source Voltage)	ω (Output Voltages reference Frequency)
7 Ω	40 mH	30 μ F	300 V	50 Hz

4.2.1 Simulation for Current Control with THD Minimization Algorithm for Buck Inverter

In this simulation, Buck Inverter is simulated with THD Minimization current control scheme. Simulated structure is shown in Figure 4.17. Sampling period of the controller is taken as 50 μ s and, since the controller is the same, computational delay of 20 μ s is reused. Timing scheme used in the simulation is the same as shown in Figure 4.2.

Control inputs for the Buck Inverter system are current references and are set as follows: Until time $t=0.2$ s, d component is set to 3 A. And q component is set to 0 A. Afterwards, d component is set to 0 A and q component is set to 3 A.

In Figure 4.18 a) and b), reference currents in c) and d) actual currents are shown in (dq) frame. Current settling time 1 ms, and peak to peak ripple is 350 mA.

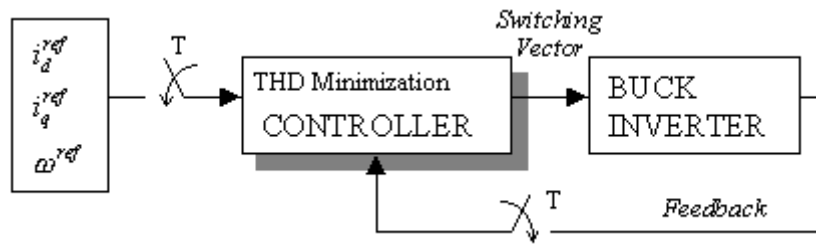


Figure 4.17 Simulation of Current Loop of Buck Inverter with THD Minimization Control scheme

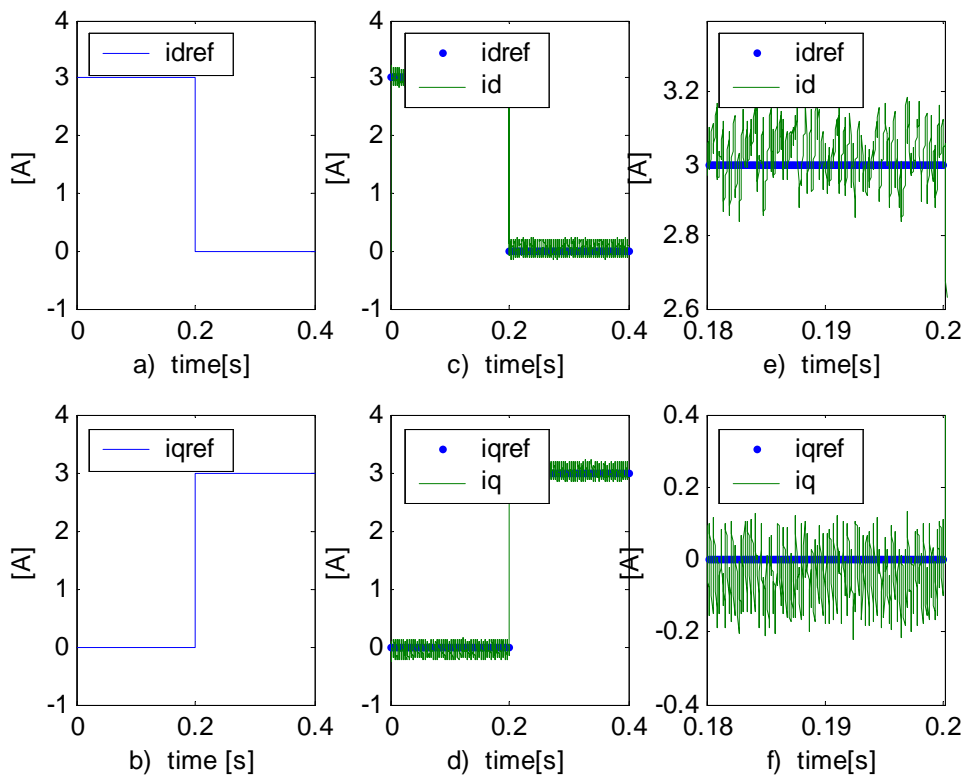


Figure 4.18 a) Reference current d component reference b) Reference current q component reference c) Tracking for d component d) Tracking for q component current e) Ripple for d component f) Ripple for q component of currents in (dq) frame for Buck Inverter under presented control scheme

Settling time for currents is 0.8 ms. Total Harmonic Distortion of the currents is measured as 0.036.

In Figure 4.19, phase currents and voltages are illustrated. They are always in phase since active load is used.

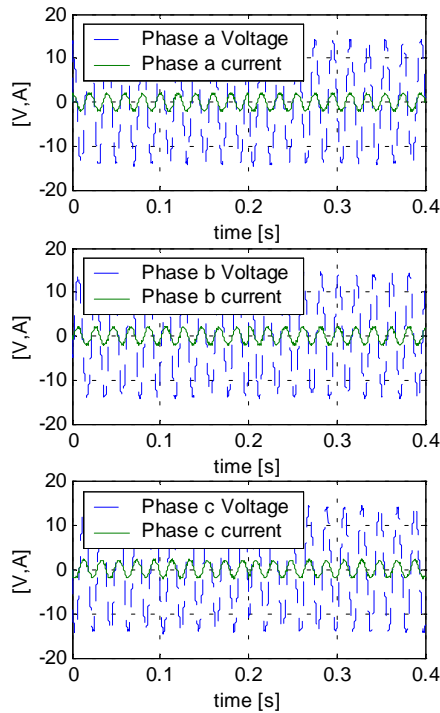


Figure 4.19 Input source voltages and input currents for Buck Inverter under THD Minimization control scheme

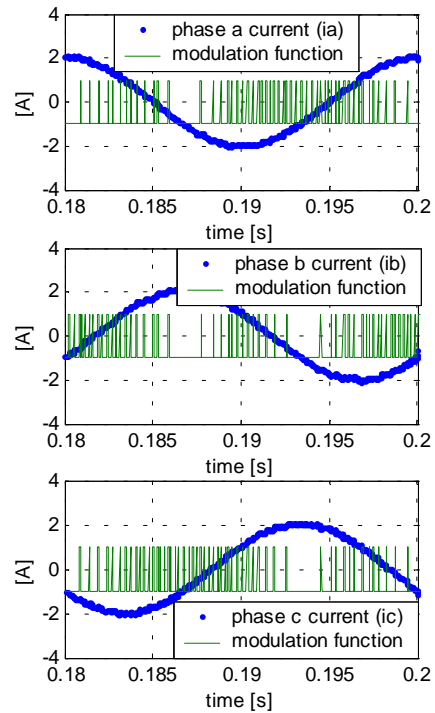


Figure 4.20 Steady state input currents and corresponding modulation functions for one period of output voltages for Buck Inverter under THD Minimization control scheme

In Figure 4.20, phase currents are corresponding modulation functions in steady state for one period of input voltage are shown. In Figure 4.21, input currents are shown in $(\alpha\beta)$ frames of references.

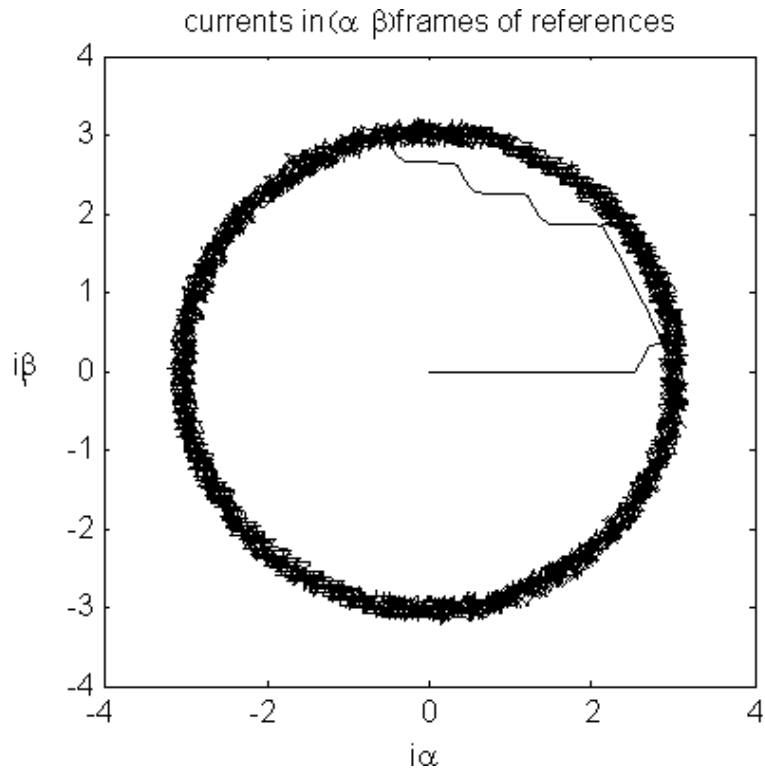


Figure 4.21 Input currents shown in $(\alpha\beta)$ frames of references for Buck Inverter under THD Minimization control scheme

4.2.2 Simulation for Current Control with Relay Controller

This simulation aims to see the performance of Relay controller, ripple of currents, dynamic response, Total Harmonic Distortion, regularity of switching, controller parameters, hysteresis band width, discrete operation with sampling period and carry out a comparison with the THD Minimization algorithm.

Simulated system is shown in Figure 4.22. It consists of Buck Inverter as plant and current controller employing Relay Control algorithm. Control inputs for the Buck Inverter system is set as d and q components of currents and reference frequency for output voltages.

To give the facility of same number of switchings, sampling period is set to 25 μ s. In addition, no computational delay is employed for Relay Controller. Timing scheme for this simulation is as the same shown in Figure 4.8.

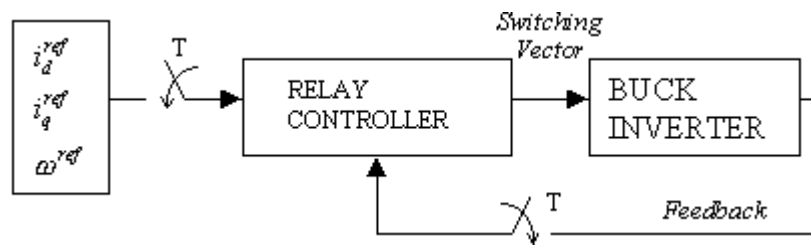


Figure 4.22 Simulation of Buck Inverter, currents controlled with Relay Controller

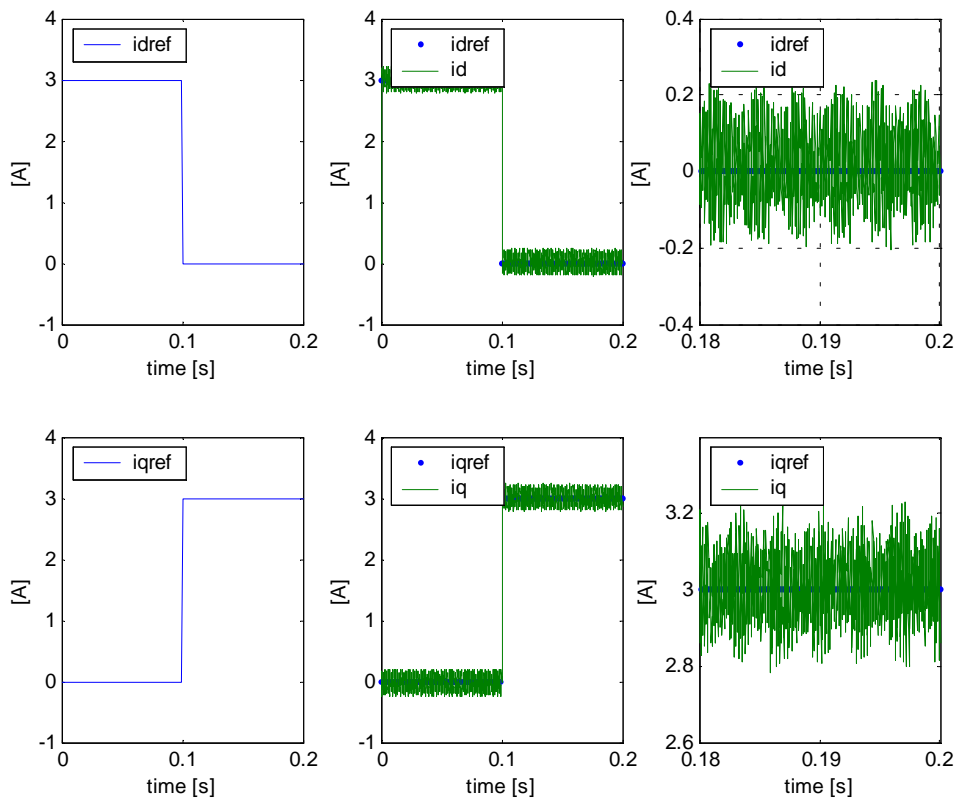


Figure 4.23 Tracking and transients of plant currents in d-q frame for Buck Inverter under Relay control scheme

The same reference current profiles, required from the presented controller, are asked, that is, until time 0.2 s ($t=0.2$ s.), d component is set to 3 A. and q component is set to 0 A. Afterwards, d component is set to 0A and q component is set to 3 A. (Figure 4.23)

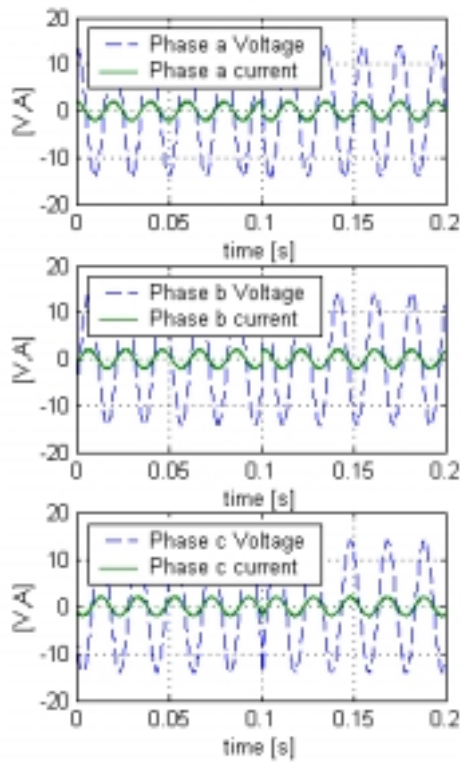


Figure 4.24 Output Phase voltages and output currents for Buck Inverter under Relay control scheme

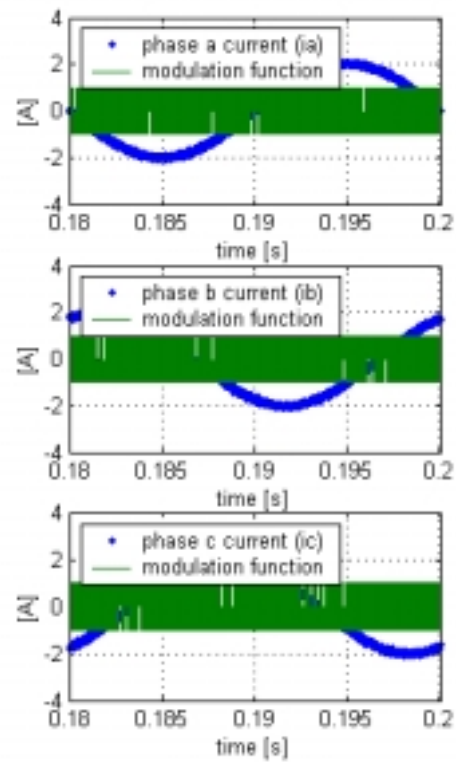


Figure 4.25 Steady state phase currents and corresponding modulation functions for one period of output voltages for Buck Inverter under Relay control scheme

The hysteresis band width is set to ± 0.05 A to have ripple as small as possible, since simple Relay controller operating in discrete time can not avoid ripple extending the hysteresis band. Employing too narrow hysteresis band to avoid excessive ripple causes over-switching.

In Figure 4.23, (dq) reference and actual currents are illustrated and observed that ripple in currents is 450 mA peak-to-peak. Settling time for currents is 1 ms.

In Figure 4.24, output voltages and phase currents are shown. Total Harmonic distortion of the currents are measured as 0.08.

In Figure 4.25, phase currents and corresponding modulation functions for one period of output voltage is shown. The switching frequency is greater than the situation for presented algorithm, which is shown in Figure 4.20.

In Figure 4.26 currents are shown in $(\alpha\beta)$ frames of references. The amount of ripple and deviation of the system state from the reference is observed clearly when compared with the motion obtained with the THD Minimization algorithm (Figure 4.21).

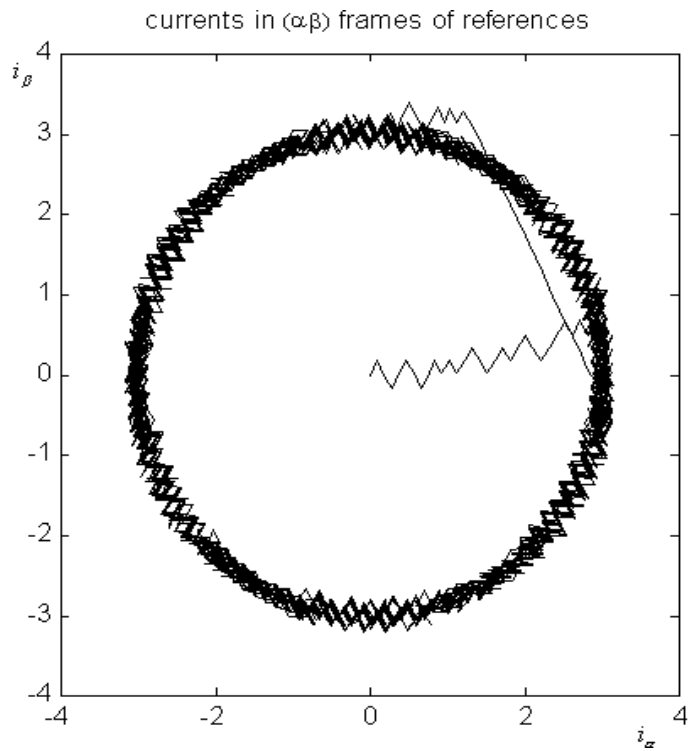


Figure 4.26 Phase currents shown in $(\alpha\beta)$ frames of references for Buck Inverter under Relay control

4.2.3 Comparison of Relay Control Algorithm and THD Minimization Algorithm on Buck Inverter

Current loop, with same reference current profiles, is simulated with both Relay Control and THD Minimization control on Buck Inverter. Results are summarized as follows:

Table 10. Comparison of control algorithm performances for Buck Inverter based on simulation results

	Relay Control	THD Minimization Control
Sampling Period (T)	25 μ s	50 μ s
Computational Delay	0 s	20 μ s
Ripple in currents	± 225 mA	± 175 mA
Settling time of currents for the step change in reference	1 ms	0.8 ms
Total Harmonic Distortion at AC currents	0.08	0.0036
Regularity in switching	No	Yes
Number of switchings	More	Less
Computational Load	Less	More

From simulation results, one can easily conclude that, THD Minimization algorithm is functioning correctly. Relay controller has functioned at, not only ideal conditions ,in other words infinite computation speed, but also had the possibility of higher frequency.

Although having more disadvantageous conditions (but closer to real life conditions), presented algorithm not only succeeds in minimization of Total Harmonic Distorsion but also succeeds in better tracking performance with less number of switching actions.

5. CONCLUSIONS

In this work, a discrete current control scheme is defined for all 3~Phase Switching Power Converters and 3~Phase Electrical machines and verified by simulation.

The presented algorithm is outputting the switching patterns for the switching matrix and is designed to minimize the Instantaneous Total Harmonic Distortion in AC currents.

The algorithm evaluates harmonic distortion in real time with calculation of the instantaneous THD and sequentially selects two switching vectors in one control period in order to minimize the tracking error and timing is determined according to the THD minimization requirements.

Simulation results show that presented method has good performance in the minimization of Total Harmonic Distortion and in current tracking. It has much better dynamic response with less number of switching actions compared with the basic Sliding Mode scheme.

The simulation results are very encouraging, and confirm the theoretical results, further work shall be concentrated on the validation of the algorithm with experiments.

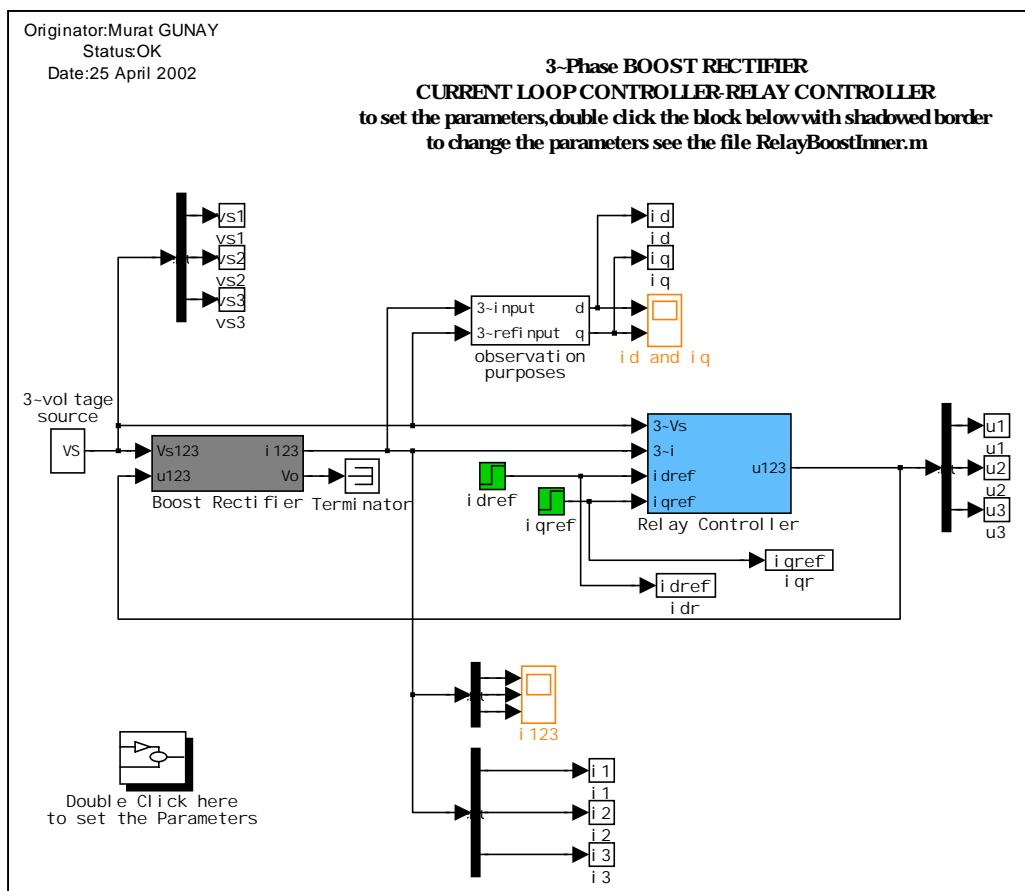
APPENDIX A

APPENDIX B

APPENDIX B.1

BOOST RECTIFIER CURRENT CONTROL WITH RELAY CONTROLLER

Simulink Model File: \Relay_Boost_Inner\Relay_Boost_Inner.mdl



Parameter M file: \Relay_Boost_Inner\RelayBoostInner.m

%Parameters file to be used with Boost Rectifier

%controlled with RELAY CONTROLLER

%Source parameters

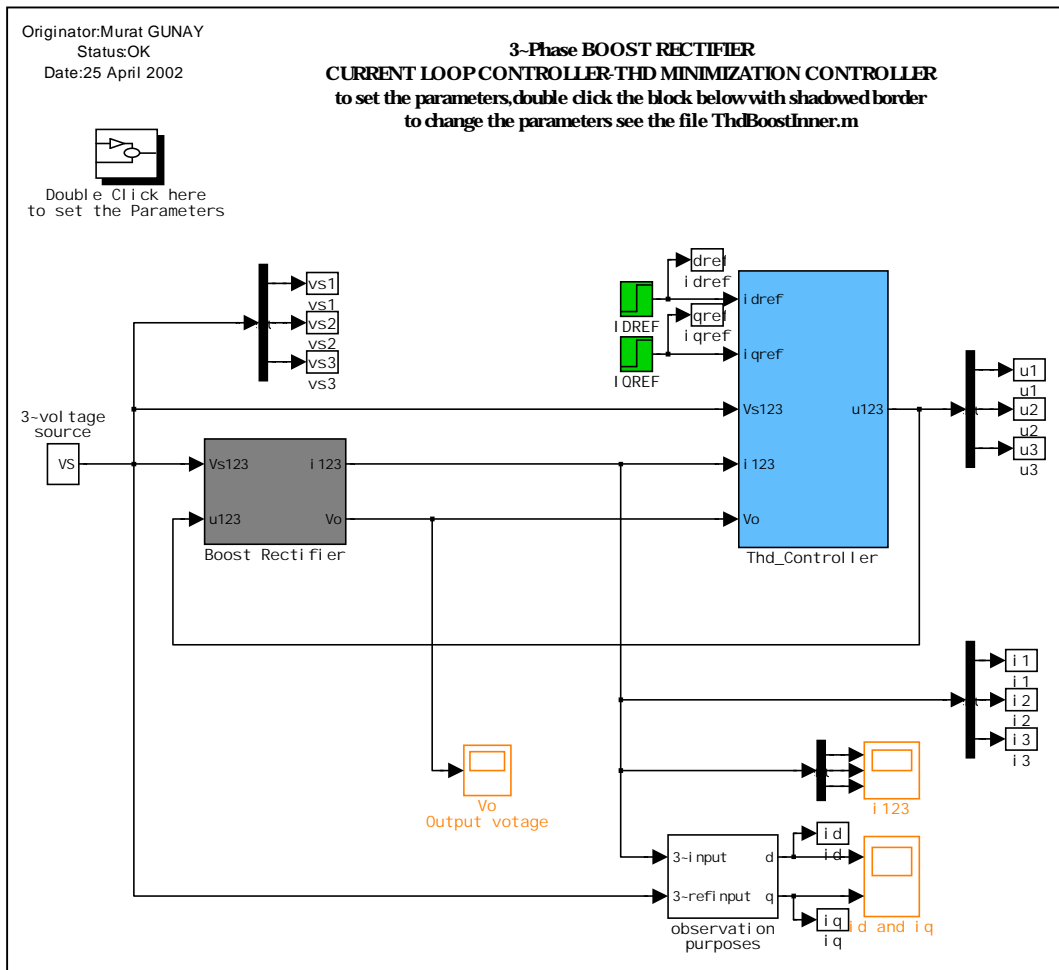
ws=2*pi*50;% source voltage angular frequency[rad/sec]


```
Vg=10; %Source Voltage amplitude
%Plant parameters
R=50; %Resistance [ohms]
L=0.02; %Inductance [Henry]
C=0.0007; %Capacitor [Farads]
IPMAX=50; %max current that plant can allow
IPMIN=-50; %min current that plant can allow
VOPMAX=100; %max voltage that plant can allow
VOPMIN=0; %min voltage that plant can allow
VO_0=25; %initial value of the output voltage
I1_0=0; %initial value of the plant phase a current
I2_0=0; %initial value of the plant phase b current
I3_0=0; %initial value of the plant phase c current
%Relay controller parameters
TS_c=25e-6; %Sampling Period of current loop
bound=0.05;%hystrezis bound --> +-bound
```

APPENDIX B.2

BOOST RECTIFIER CURRENT CONTROL WITH THD MINIMIZATION ALGORITHM

Simulink Model File:\Thd_Boost_Inner\Thd_Boost_Inner.mdl



Parameter M file: \ThdBoostInner.m

```
%Parameters file to be used with Boost Rectifier
%controlled with THD MinimizationController
ws=2*pi*50;%source voltage angular frequency[rad/sec]
Vg=10; %Source Voltage amplitude[V]
```

```

%Plant parameters
R=50;    %Resistance [ohms]
L=0.02;  %Inductance [Henry]
C=0.0007; %Capacitor [Farads]
IPMAX=50; %max current that plant can allow
IPMIN=-50; %min current that plant can allow
VOPMAX=100; %max voltage that plant can allow
VOPMIN=0; %min voltage that plant can allow
VO_0=25; %initial value of the output voltage
I1_0=0; %initial value of the plant phase a current
I2_0=0; %initial value of the plant phase b current
I3_0=0; %initial value of the plant phase c current
%Presented controller parameters
TS_c=50e-6; %Sampling Period of current loop
Compdel=20e-6;%computational delay
%filter parameter
wc=2*pi*20;%filter corner angular frequency

```

S-function file: \Thd_Boost_Inner\thdfboost.c

```

/*=====
==*/

```

```

#define S_FUNCTION_LEVEL 2
#define S_FUNCTION_NAME thdfboost
#include "simstruc.h"
#include "math.h"
#define Rx *mxGetPr(ssGetSFcnParam(S,0)) /*first parameter */
#define Lx *mxGetPr(ssGetSFcnParam(S,1)) /*second parameter*/
#define Cx *mxGetPr(ssGetSFcnParam(S,2)) /*third parameter */
#define Ts *mxGetPr(ssGetSFcnParam(S,3)) /*fourth parameter*/
#define cdel *mxGetPr(ssGetSFcnParam(S,4)) /*fifth parameter */

```

```

/*Friendly access to inputs to S fcn block*/
#define U(element) (*uPtrs[element])

/*****
/*          mdlInitializeSizes          */
*****/
static void mdlInitializeSizes(SimStruct *S)
{

    ssSetNumContStates(S,0);
    ssSetNumDiscStates(S,0);
    if (!ssSetNumInputPorts(S,1)) return;
    ssSetInputPortWidth(S,0,13);          /*input number*/
    ssSetInputPortDirectFeedThrough(S,0,0);
    if (!ssSetNumOutputPorts(S,1)) return;
    ssSetOutputPortWidth(S,0,12);        /*output number*/
    ssSetNumSampleTimes(S,1);
    ssSetNumSFcnParams(S,5);          /*S Fcn parameter number*/
    ssSetNumRWork(S,0);
    ssSetNumIWork(S,0);
    ssSetNumPWork(S,0);
    ssSetNumModes(S,0);
    ssSetNumNonsampledZCs(S,0);
    ssSetOptions(S, SS_OPTION_EXCEPTION_FREE_CODE);
}

/*****
/*          mdlInitializeSampleTimes          */
*****/
static void mdlInitializeSampleTimes(SimStruct *S)
{
    ssSetSampleTime(S,0,CONTINUOUS_SAMPLE_TIME);
    ssSetOffsetTime(S,0,0.0);
}

```

```

/*****
/*          mdlOutputs          */
/*****

static void mdlOutputs(SimStruct *S,int_T tid)
{
    InputRealPtrsType uPtrs = ssGetInputPortRealSignalPtrs(S,0);
    real_T          *y  = ssGetOutputPortRealSignal(S,0);

    int birindex=7; /*index of the first vector selected */
    int ikiindex=7; /*index of the second vector selected*/
    float alpha;    /*timing parameter*/

    int myflag=1;int k;int i;
    float Udq[8][2]; /*Declaration for Udq (Array to store the representations of the
switching vectors in d-q frame) */
    float Pdq[8][2]; /*Declaration for Pdq (Array to store the velocities of the error
corresponding to the switching vectors)*/
    float Ddq[8][2]; /*Declaration for Ddq (Array to store the d-q distances
corresponding to the switching vectors) */
    float canfI[8]; /*Declaration for canfI (Array to store the candidates for the
selection of Fisrt Vector) */
    float canfII[8];
    float dummy_min; /*Declaration for dummy_min (Temporary placeholder for
instantenous min of the candidates)*/
    float pay;float payda; /*Declaration for pay payda (Note that alpha=pay/payda)*/
    float Valfa;float Vbeta; /*Declaration for Valfa Vbeta*/
    float id;float iq; /*Declaration for id iq*/
    float sigmad;float sigmaq; /*Declaration for sigmad sigmaq */
    float u1I;float u2I;float u3I; /*Declaration for u1 u2 u3 related to First Vector*/
    float u1II;float u2II;float u3II; /*Declaration for u1 u2 u3 related to Second Vector*/
    float udI;float uqI; /*Declaration for ud uq related to First Vector*/
    float udII;float uqII; /*Declaration for ud uq related to Second Vector*/

    /* S w i t c h i n g   v e c t o r s   i n   a b c   f r a m e */

```

```

static      int      SW[8][3]={{1,-1,-1},{1,1,-1},{-1,1,-1},{-1,1,1},{-1,-1,1},{1,-
1,1},{1,1,1},{-1,-1,-1}};

int sonvec=7;   /*index of the last vector applied to the plant */
float saat=U(0); /*real time info */

/* substituting inputs */
float idref=U(1);float iqref=U(2);float i1=U(3);float i2=U(4);float i3=U(5);float
Vo=U(6);
float udeq=U(7);float uqe=U(8);float nT=U(9);float V1=U(10);float V2=U(11);float
V3=U(12);
float theta;float GB;float dis1=cdel;float dis2=0;
float pred_d=0;float pred_q=0; /*prediction term for latency*/

if(saat==nT) /*----- sampling instant -----*/
{
    Valpha=V1-0.5*V2-0.5*V3;   /*transformation of source voltages */
    Vbeta=0.5*sqrt(3)*(V2-V3); /*into othgononal alpha-beta frame */
    theta=atan2(Vbeta,Valpha); /*and determining theta */
    id=(i1-0.5*i2-0.5*i3)*cos(theta)+(0.5*sqrt(3)*(i2-i3))*sin(theta);
/*Transformation of measured currents*/
    iq=(i1-0.5*i2-0.5*i3)*(-sin(theta))+(0.5*sqrt(3)*(i2-i3))*cos(theta); /*into the d-q
frame using theta info */
    sigmad=pred_d+id-idref; /*Since we have plant currents in d-q frame and
reference currents coming from voltage controller */
    sigmaq=pred_q+iq-iqref; /*we can determine the error in currents and add
some prediction term to compensates the computation delay*/
    GB=-Vo/(2*Lx); /*Calculation of GB parameter, effecting the velocity of
error */
    for(i=0;i<=7;i++) /*Transformation of switching vectors into d-q frame */
    {
        Udq[i][0]=(SW[i][0]-0.5*SW[i][1]-
0.5*SW[i][2])*cos(theta)+sqrt(3)*0.5*(SW[i][1]-SW[i][2])*sin(theta);

```

```

                                Udq[i][1]=(SW[i][0]-0.5*SW[i][1]-0.5*SW[i][2])*(-
sin(theta))+sqrt(3)*0.5*(SW[i][1]-SW[i][2])*cos(theta);
    }
    for(i=0;i<=7;i++)
    {
        Pdq[i][0]=GB*(Udq[i][0]-udeq);
        Pdq[i][1]=GB*(Udq[i][1]-upeq);
    }
    for(i=0;i<=7;i++)
    {
        Ddq[i][0]=Pdq[i][0]*Ts;
        Ddq[i][1]=Pdq[i][1]*Ts;
    }
    for(i=0;i<=7;i++)
    {
                                                                    canfl[i]=sqrt(
(sigmad+Ddq[i][0])*(sigmad+Ddq[i][0])+(sigmaq+Ddq[i][1])*(sigmaq+Ddq[i][1]) );
    }
    dummy_min=canfl[0];
    k=0;
    for(i=1;i<=7;i++)
    {
        if(dummy_min>canfl[i])
        {
            dummy_min=canfl[i];
            k=i;
        }
    }
    if((k==6) || (k==7))
    {
        if((sonvec==7) || (sonvec==4) || (sonvec==2) ||
(sonvec==0)){k=7;}
        else{k=6;}
    }
}

```

```

    birindex=k;
    for(i=0;i<=7;i++)
    {
        canfII[i]=sqrt( (sigmad + Ddq[birindex][0])* (Ddq[i][0]-
Ddq[birindex][0]) + (sigmaq+Ddq[birindex][1])*(Ddq[i][1]-Ddq[birindex][1]) );
        /*      Sqrt( (sigma_d+DI_d)          *(Di_d-DId)          +
(sigma_q+DI_q)          *(Di_q-DI_q) )          */
    }
    dummy_min=canfII[0];
    k=0;
    for(i=1;i<=7;i++)
    {
        if(dummy_min>canfII[i])
        {
            dummy_min=canfII[i];
            k=i;
        }
    }
    if((k==6) || (k==7))
    {
        if( (birindex==7) || (birindex==4) || (birindex==2) ||
(birindex==0)){k=7;}/*optimization for zero vector */
        else{k=6;}
    }
    ikiindex=k;
    /*****Calculation of
ALPHA *****/
    /*****/
    payda=(Ddq[ikiindex][0]-2*Ddq[birindex][0])*(Ddq[ikiindex][0]-
Ddq[birindex][0]) + (Ddq[ikiindex][1]-2*Ddq[birindex][1])*(Ddq[ikiindex][1]-
Ddq[birindex][1]);
    /* (DII_d-2*DI_d)          *(DII_d-DId)          + (DII_q-
2*DI_q)          *(DII_q-DI_q)          */

```



```

        pay=(Ddq[ikiindex][0]+2*sigmad)*(Ddq[ikiindex][0]-Ddq[birindex][0])
+ (Ddq[ikiindex][1]+2*sigmaq)*(Ddq[ikiindex][1]-Ddq[birindex][1]);
        /* (DII_d+2*sigma_d)      *(DII_d-DI_d)      +
(DII_q+2*sigma_q)      *(DII_q-DI_q)      */
        alpha=pay/(payda+0.000001);
        if(alpha>=0.9||alpha<=0.2)
        { alpha=1000;
        sonvec=birindex;
        dis1=cdel;
        dis2=0;
        myflag=0; }
        else
        { myflag=1;
        sonvec=ikiindex;
        dis1=0;
        dis2=cdel;
        }
        pred_d=Pdq[birindex][0]*dis1+Pdq[ikiindex][0]*dis2; /*Predictions for
d and q components */
        pred_q=Pdq[birindex][1]*dis1+Pdq[ikiindex][1]*dis2; /*Predictions for
d and q components */
        udI=Udq[birindex][0];uqI=Udq[birindex][1];
        udII=Udq[ikiindex][0];uqII=Udq[ikiindex][1];
        u1I=SW[birindex][0];u2I=SW[birindex][1];u3I=SW[birindex][2];
/*output Variables are ok */
        u1II=SW[ikiindex][0];u2II=SW[ikiindex][1];u3II=SW[ikiindex][2];
/*output Variables are ok */
        /*outputs are posted*/
        y[0]=u1I;y[1]=u2I;y[2]=u3I;y[3]=udI;y[4]=uqI; /*First vector related
vars*/
        y[5]=u1II;y[6]=u2II;y[7]=u3II;y[8]=udII;y[9]=uqII; /*Second vector
related vars*/
        y[10]=alpha; /*timing info*/
        y[11]=myflag;

```

```

}/******END OF
SAMPLING INSTANT*****/
}

/*****/
/*          mdlTerminate          */
/*****/

/* Function: mdlTerminate
 * Abstract:
 *   No termination needed, but we are required to have this routine.
 */

static void mdlTerminate(SimStruct *S)
{
}

#ifdef MATLAB_MEX_FILE /* Is this file being compiled as a MEX-file? */
#include "simulink.c" /* MEX-file interface mechanism */
#else
#include "cg_sfun.h" /* Code generation registration function */
#endif

S-function file: S-function file: \Thd_Boost_Inner\myalfa.c

#define S_FUNCTION_LEVEL 2
#define S_FUNCTION_NAME myalfa
#include "simstruc.h"
#include "math.h"
#define Tp *mxGetPr(ssGetSFcnParam(S,0)) /*Sampling Period*/
#define cdel *mxGetPr(ssGetSFcnParam(S,1)) /*Computation delay*/
#define U(element) (*uPtrs[element]) /*Friendly access to inputs to S fcn block*/

/*****/
/*          mdlInitializeSizes          */
/*****/

```

```

/*****/
static void mdlInitializeSizes(SimStruct *S)
{
    ssSetNumContStates(S,0);
    ssSetNumDiscStates(S,0);
    if (!ssSetNumInputPorts(S,1)) return;
    ssSetInputPortWidth(S,0,4);          /*input number*/
    ssSetInputPortDirectFeedThrough(S,0,0);
    if (!ssSetNumOutputPorts(S,1)) return;
    ssSetOutputPortWidth(S,0,1);        /*output number*/
    ssSetNumSampleTimes(S,1);
    ssSetNumSFcnParams(S,2);           /*S Fcn parameter number*/
    ssSetNumRWork(S,0);
    ssSetNumIWork(S,0);
    ssSetNumPWork(S,0);
    ssSetNumModes(S,0);
    ssSetNumNonsampledZCs(S,0);
    ssSetOptions(S, SS_OPTION_EXCEPTION_FREE_CODE);
}
/*****/
/*      mdlInitializeSampleTimes      */
/*****/
static void mdlInitializeSampleTimes(SimStruct *S)
{
    ssSetSampleTime(S,0,CONTINUOUS_SAMPLE_TIME);
    ssSetOffsetTime(S,0,0.0);
}
/*****/
/*      mdlOutputs      */
/*****/
static void mdlOutputs(SimStruct *S,int_T tid)
{
    InputRealPtrsType uPtrs = ssGetInputPortRealSignalPtrs(S,0);
    real_T      *y  = ssGetOutputPortRealSignal(S,0);

```

```

float enb=U(0);float clkreal=U(1);float kT=U(2);float incalpha=U(3);

if(enb==1)
{

    if(clkreal>=(kT+incalpha*Tp))
        {y[0]=0;}
    else{y[0]=1;}
}
else
{
y[0]=1;
}
}

/*****
/*          mdlTerminate          */
*****/

/* Function: mdlTerminate
* Abstract:
*   No termination needed, but we are required to have this routine.
*/

static void mdlTerminate(SimStruct *S)
{
}

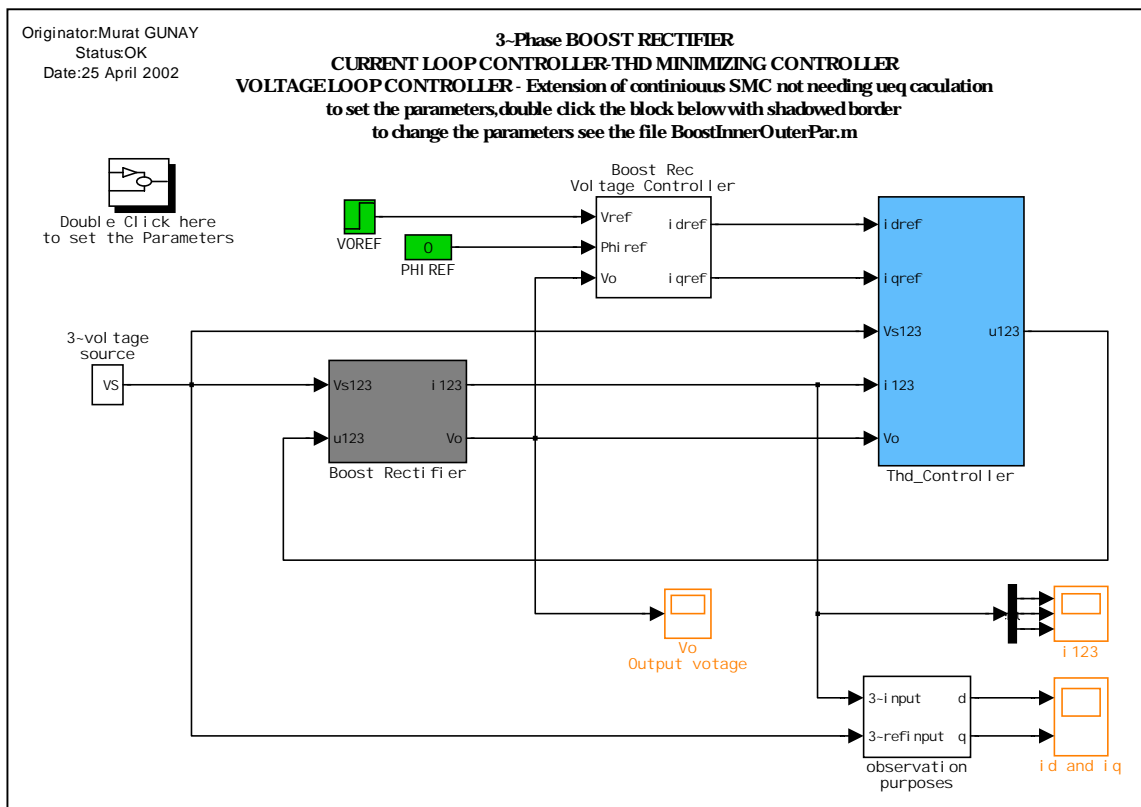
#ifdef MATLAB_MEX_FILE /* Is this file being compiled as a MEX-file? */
#include "simulink.c" /* MEX-file interface mechanism */
#else
#include "cg_sfund.h" /* Code generation registration function */
#endif

```

APPENDIX B.3

BOOST RECTIFIER CURRENT CONTROL WITH THD MINIMIZATION VOLTAGE CONTROLLE WITH DISCRETE TIME SLIDING MODE ALGORITHM

Simulink Model File:\Thd_with_Outer_Loop_Boost\Thd_Boost_Inner.mdl



Parameter M file: \Thd_with_Outer_Loop_Boost\BoostInnerOuterPar.m

%Parameters file to be used with Boost Rectifier

%controlled with Presented Controller

ws=2*pi*50;%source voltage angular frequency[rad/sec]

Vg=10; %Source Voltage amplitude[V]

%Plant parameters

R=50; %Resistance [ohms]

```

L=0.02; %Inductance [Henry]
C=0.0007; %Capacitor [Farads]
IPMAX=50; %max current that plant can allow
IPMIN=-50; %min current that plant can allow
VOPMAX=100;%max voltage that plant can allow
VOPMIN=0; %min voltage that plant can allow
VO_0=25; %initial value of the output voltage
I1_0=0; %initial value of the plant phase a current
I2_0=0; %initial value of the plant phase b current
I3_0=0; %initial value of the plant phase c current
%controller parameters
TS_c=50e-6; %Sampling Period of current loop
Compdel=20e-6;%computational delay
%filter parameters
wc=2*pi*20; %filter corner angular frequency
%Voltage controller
offsetboo=0.0015;%offset for voltage controller
D=500; %convergence rate for voltage controller
TS_v=500e-6; %Voltage Loop Sampling Period
umax=6; %Maximum ref current that voltage controller can allow
errvolzero=1.5; %initial error of voltage

```

S-function file: \Thd_with_Outer_Loop_Boost\myalfa.c

This is the same as *S-function file: \Thd_Boost_Inner\myalfa.c*

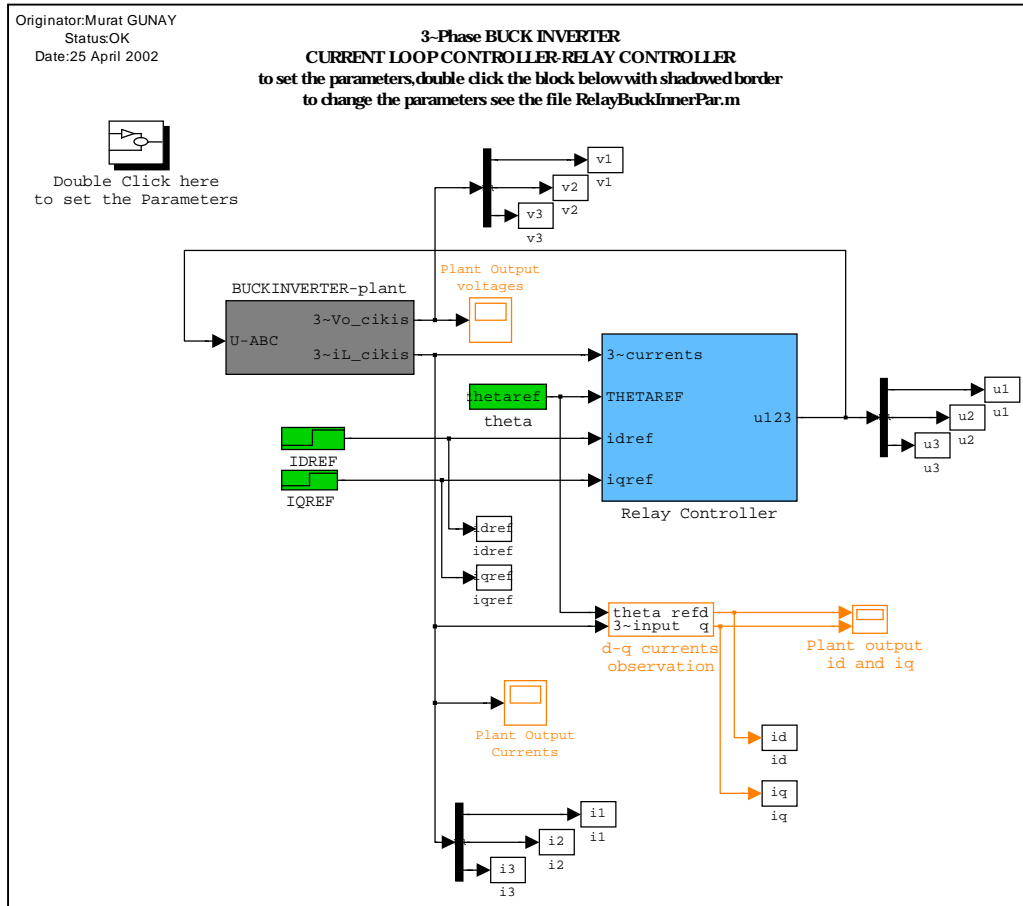
S-function file: \Thd_with_Outer_Loop_Boost\thdfboost.c

This is the same as *S-function file: \Thd_Boost_Inner\thdfboost.c*

APPENDIX B.4

BUCK INVERTER CURRENT CONTROL WITH RELAY CONTROLLER

Simulink Model File: \Relay_Buck_Inner\ Relay_Buck_Inner.mdl



Parameter M file: \Relay_Buck_Inner\ RelayBuckInnerPar.m

%Parameters file to be used with

%Buck Inverter controlled with Relay Controller

wr=2*pi*50;%source voltage angular frequency[rad/sec]

Vg=300;%DC Voltage source [V]

%Plant parameters

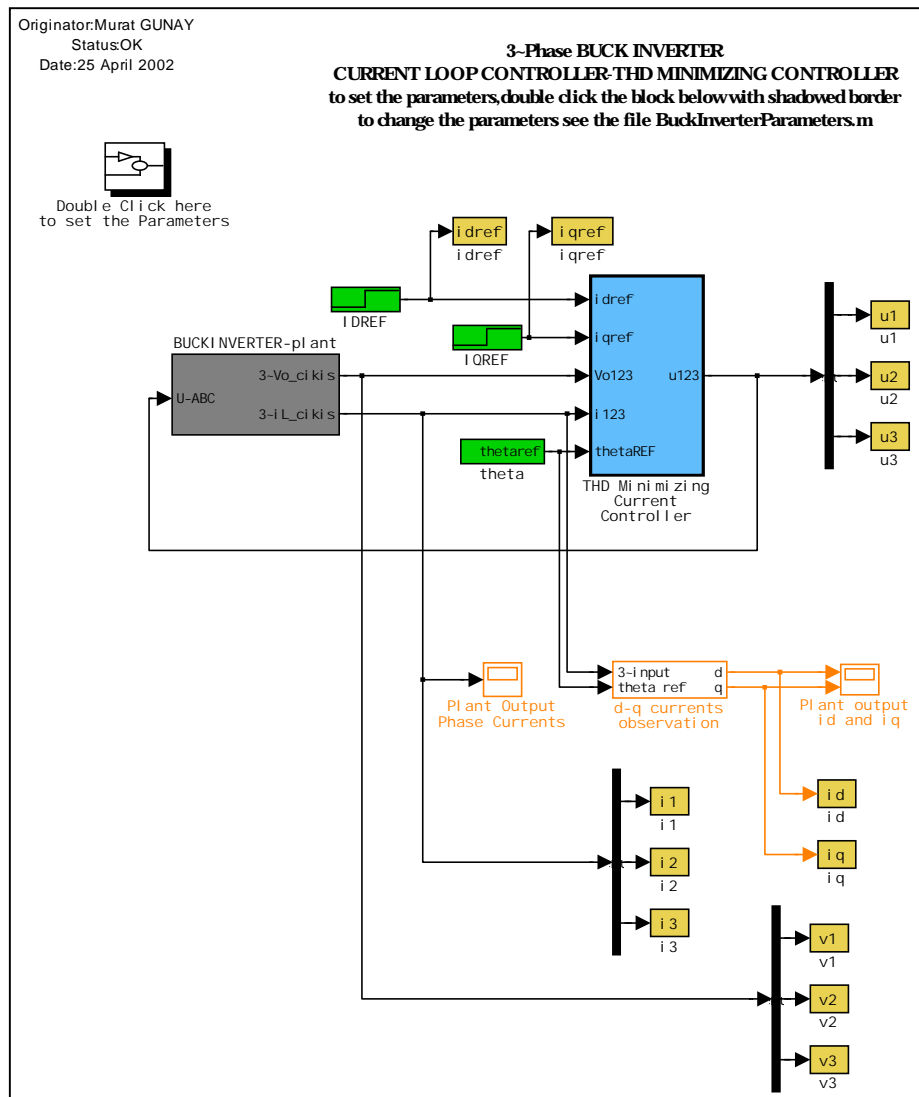
R=7;%resistance [ohms]

L=0.04;% inductance [H]
C=0.00003;% capacitance [F]
IPMAX=50; %max current that plant can allow
IPMIN=-50; %min current that plant can allow
VOPMAX=100; %max voltage that plant can allow
VOPMIN=0; %min voltage that plant can allow
I1_0=0; %initial value of the plant phase a current
I2_0=0; %initial value of the plant phase b current
I3_0=0; %initial value of the plant phase c current
%Relay controller parameters
TS_c=25e-6; %Sampling Period of current loop
bound=0.05;%hystrezis bound --> +-bound

APPENDIX B.5

BUCK INVERTER CURRENT CONTROL WITH THD MINIMIZATION CONTROLLER

Simulink Model File: \Thd_Buck_Inner\Thd_Buck_Inner.mdl



Parameter M file: \Thd_Buck_Inner\BuckInnerParameters.m

%Buck Inverter parameters controlled with presented algorithm

```

%Source parameters
wr=2*pi*50;%reference angular velocity for output voltages
Vg=300; %DC Voltage source Volts
%Plant parameters
R=7; %resistance ohms
L=0.04; %inductance Henry
C=0.00003; %capacitance Farad
%Controller Parameters
TS_c=50e-6; %Current controller sampling period
Compdel=20e-6; %Current controller computational delay
%Filter parameter
fc=2*pi*20; %filter corner frequency

```

S-function file: \Thd_Buck_Inner\thdfbuck.c

```

/*=====
==*/

```

```

#define S_FUNCTION_LEVEL 2
#define S_FUNCTION_NAME thdfbuck
#include "simstruc.h"
#include "math.h"
#define Rx *mxGetPr(ssGetSFcnParam(S,0)) /*first parameter */
#define Lx *mxGetPr(ssGetSFcnParam(S,1)) /*second parameter*/
#define Cx *mxGetPr(ssGetSFcnParam(S,2)) /*third parameter */
#define Ts *mxGetPr(ssGetSFcnParam(S,3)) /*fourth parameter*/
#define cdel *mxGetPr(ssGetSFcnParam(S,4)) /*fifth parameter */
#define Vdc *mxGetPr(ssGetSFcnParam(S,5)) /*sixth parameter */
#define U(element) (*uPtrs[element]) /*Friendly access to inputs to S fcn block*/

```

```

/*****/

```

```

/*          mdlInitializeSizes          */
/*****/
static void mdlInitializeSizes(SimStruct *S)
{
    ssSetNumContStates(S,0);
    ssSetNumDiscStates(S,0);
    if (!ssSetNumInputPorts(S,1)) return;
    ssSetInputPortWidth(S,0,13);          /*input number*/
    ssSetInputPortDirectFeedThrough(S,0,0);
    if (!ssSetNumOutputPorts(S,1)) return;
    ssSetOutputPortWidth(S,0,12);        /*output number*/
    ssSetNumSampleTimes(S,1);
    ssSetNumSFcnParams(S,6);          /*S Fcn parameter number*/
    ssSetNumRWork(S,0);
    ssSetNumIWork(S,0);
    ssSetNumPWork(S,0);
    ssSetNumModes(S,0);
    ssSetNumNonsampledZCs(S,0);
    ssSetOptions(S, SS_OPTION_EXCEPTION_FREE_CODE);
}
/*****/
/*          mdlInitializeSampleTimes          */
/*****/
static void mdlInitializeSampleTimes(SimStruct *S)
{
    ssSetSampleTime(S,0,CONTINUOUS_SAMPLE_TIME);
    ssSetOffsetTime(S,0,0.0);
}
/*****/
/*          mdlOutputs          */
/*****/
static void mdlOutputs(SimStruct *S,int_T tid)
{

```

```

InputRealPtrsType uPtrs = ssGetInputPortRealSignalPtrs(S,0);
real_T      *y  = ssGetOutputPortRealSignal(S,0);

int birindex=7; /*index of the first vector selected */
int ikiindex=7; /*index of the second vector selected*/
float alpha; /*calculated timing information*/
int myflag=1;int k;int i;
float Udq[8][2]; /*Declaration for Udq (Array to store the representations of the
switching vectors in d-q frame) */
float Pdq[8][2]; /*Declaration for Pdq (Array to store the velocities of the error
corresponding to the switching vectors)*/
float Ddq[8][2]; /*Declaration for Ddq (Array to store the d-q distances
conresponding to the switcting vectors) */
float canfI[8]; /*Declaration for canfI (Array to store the candidates for the
selection of Fisrt Vector) */
float canfII[8];
float dummy_min; /*Declaration for dummy_min (Temporary placeholder for
instantenous min of the candidates)*/
float pay;float payda; /*Declaration for pay payda (Note that alpha=pay/payda)*/
float Valfa;float Vbeta; /*Declaration for Valfa Vbeta*/
float id;float iq; /*Declaration for id iq*/
float sigmad;float sigmaq; /*Declaration for sigmad sigmaq */
float u1I;float u2I;float u3I; /*Declaration for u1 u2 u3 for First Vector */
float u1II;float u2II;float u3II; /*Declaration for u1 u2 u3 for Second Vector*/
float udI;float uqI; /*Declaration for ud uq for First Vector */
float udII;float uqII; /*Declaration for ud uq for Second Vector*/

/* S w i t c h i n g   v e c t o r s   i n   a b c   f r a m e */
static int SW[8][3]={{1,-1,-1},{1,1,-1},{-1,1,-1},{-1,1,1},{-1,-1,1},{1,-
1,1},{1,1,1},{-1,-1,-1}};

int sonvec=7; /*index of the last vector applied to the plant */

/*substuting inputs*/

```

```

float saat=U(0);float idref=U(1);float iqref=U(2);float i1=U(3);float i2=U(4);
float i3=U(5);float thetaref=U(6);float udeq=U(7);float uqe=U(8);float nT=U(9);
float V1=U(10);float V2=U(11);float V3=U(12);
float theta;float GB;float dis1=cdel;float dis2=0;
float pred_d=0;float pred_q=0;

if(saat==nT) /*----- s a m p l i n g   i n s t a n t -----*/
{
    theta=thetaref;
    id=(i1-0.5*i2-0.5*i3)*cos(theta)+(0.5*sqrt(3)*(i2-i3))*sin(theta);
/*Transformation of measured currents*/
    iq=(i1-0.5*i2-0.5*i3)*(-sin(theta))+(0.5*sqrt(3)*(i2-i3))*cos(theta); /*into the d-q
frame using theta info */
    sigmad=pred_d+id-idref; /*Since we have plant currents in d-q frame and
reference currents coming from voltage controller */
    sigmaq=pred_q+iq-iqref; /*we can determine the error in currents and add
some prediction term to compensate the computation delay*/
    GB=Vdc/(2*Lx); /*Calculation of GB parameter, effecting the velocity of
error */
    for(i=0;i<=7;i++) /*Transformation of switching vectors into d-q frame */
    {
        Udq[i][0]=(SW[i][0]-0.5*SW[i][1]-
0.5*SW[i][2])*cos(theta)+sqrt(3)*0.5*(SW[i][1]-SW[i][2])*sin(theta);
        Udq[i][1]=(SW[i][0]-0.5*SW[i][1]-0.5*SW[i][2])*(-
sin(theta))+sqrt(3)*0.5*(SW[i][1]-SW[i][2])*cos(theta);
    }
    for(i=0;i<=7;i++)
    {
        Pdq[i][0]=GB*(Udq[i][0]-udeq);
        Pdq[i][1]=GB*(Udq[i][1]-uqe);
    }
    for(i=0;i<=7;i++)
    {
        Ddq[i][0]=Pdq[i][0]*Ts;

```

```

        Ddq[i][1]=Pdq[i][1]*Ts;
    }
    for(i=0;i<=7;i++)
    {
        canfI[i]=sqrt(
(sigmad+Ddq[i][0])*(sigmad+Ddq[i][0])+(sigmaq+Ddq[i][1])*(sigmaq+Ddq[i][1]) );
    }
    dummy_min=canfI[0];
    k=0;
    for(i=1;i<=7;i++)
    {
        if(dummy_min>canfI[i])
        {
            dummy_min=canfI[i];
            k=i;
        }
    }
    if((k==6) || (k==7))
    {
        if((sonvec==7) || (sonvec==4) || (sonvec==2) ||
(sonvec==0)){k=7;}
        else{k=6;}
    }
    birindex=k;
    for(i=0;i<=7;i++)
    {
        canfII[i]=sqrt( (sigmad + Ddq[birindex][0])* (Ddq[i][0]-
Ddq[birindex][0]) + (sigmaq+Ddq[birindex][1])*(Ddq[i][1]-Ddq[birindex][1]) );
        /*      Sqrt( (sigma_d+DI_d)      *(Di_d-DI_d)      +
(sigma_q+DI_q)      *(Di_q-DI_q) )      */
    }
    dummy_min=canfII[0];
    k=0;
    for(i=1;i<=7;i++)

```

```

        {
            if(dummy_min>canfII[i])
            {
                dummy_min=canfII[i];
                k=i;
            }
        }
    if((k==6) || (k==7))
    {
        if( (birindex==7) || (birindex==4) || (birindex==2) ||
(birindex==0)){k=7;}/*optimization for zero vector */
        else{k=6;}
    }
    ikiindex=k;
    /*****Calculation of
ALPHA *****/
    *****/
    payda=(Ddq[ikiindex][0]-2*Ddq[birindex][0])*(Ddq[ikiindex][0]-
Ddq[birindex][0]) + (Ddq[ikiindex][1]-2*Ddq[birindex][1])*(Ddq[ikiindex][1]-
Ddq[birindex][1]);
    /* (DIId-2*DId) * (DIId-DId) + (DIIq-
2*DIq) * (DIIq-DIq) */
    pay=(Ddq[ikiindex][0]+2*sigmad)*(Ddq[ikiindex][0]-
Ddq[birindex][0]) + (Ddq[ikiindex][1]+2*sigmaq)*(Ddq[ikiindex][1]-
Ddq[birindex][1]);
    /* (DIId+2*sigmad) * (DIId-DId) +
(DIIq+2*sigmaq) * (DIIq-DIq) */
    alpha=pay/(payda+0.000001);

    if(alpha>=0.9||alpha<=0.2)
    { alpha=1000;
    sonvec=birindex;

```

```

dis1=cdel;
dis2=0;
    myflag=0;  }
else
{  myflag=1;
    sonvec=ikiindex;
    dis1=0;
    dis2=cdel;
}
pred_d=Pdq[birindex][0]*dis1+Pdq[ikiindex][0]*dis2; /*Predictions for
d and q components */
pred_q=Pdq[birindex][1]*dis1+Pdq[ikiindex][1]*dis2; /*Predictions for
d and q components */
uI=Udq[birindex][0];uqI=Udq[birindex][1];
uII=Udq[ikiindex][0];uqII=Udq[ikiindex][1];
u1I=SW[birindex][0];u2I=SW[birindex][1];u3I=SW[birindex][2];
/*output Variables are ok */
u1II=SW[ikiindex][0];u2II=SW[ikiindex][1];u3II=SW[ikiindex][2];
/*output Variables are ok */

y[0]=u1I;y[1]=u2I;y[2]=u3I;/*switching vector components for First
Vector*/
y[3]=uI;y[4]=uqI; /*d-q components of the First Vector*/
y[5]=u1II;y[6]=u2II;y[7]=u3II;/*switching vector components for
Second Vector*/
y[8]=uII;y[9]=uqII;/*d-q components of the Second Vector*/
y[10]=alpha;y[11]=myflag;
}/******END OF
SAMPLING INSTANT*****/
}
/******
/*          mdlTerminate          */
/******
/* Function: mdlTerminate

```


* Abstract:

* No termination needed, but we are required to have this routine.

*/

```
static void mdlTerminate(SimStruct *S)
```

```
{  
}
```

```
#ifdef MATLAB_MEX_FILE /* Is this file being compiled as a MEX-file? */
```

```
#include "simulink.c" /* MEX-file interface mechanism */
```

```
#else
```

```
#include "cg_sfun.h" /* Code generation registration function */
```

```
#endif
```

S-function file: \Thd_Buck_Inner\myalfa.c

This is the same as used in: *\Thd_Boost_Inner\myalfa.c*

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