Design of a 4.2–5.4 GHz Differential LC VCO Using 0.35 μm SiGe BiCMOS Technology for IEEE 802.11a Applications

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ABSTRACT: In this paper, a 4.2–5.4 GHz, −Gm LC voltage controlled oscillator (VCO) for IEEE 802.11a standard is presented. The circuit is designed with AMS 0.35 μm SiGe BiCMOS process that includes high-speed SiGe Heterojunction Bipolar Transistors (HBTs). According to post-layout simulation results, phase noise is −110.7 dBc/Hz at 1 MHz offset from 5.4 GHz carrier frequency and −113.4 dBc/Hz from 4.2 GHz carrier frequency. A linear, 1200 MHz tuning range is obtained from the simulations, utilizing accumulation-mode varactors. Phase noise was also found to be relatively low because of taking advantage of differential tuning concept. Output power of the fundamental frequency changes between 4.8 dBm and 5.5 dBm depending on the tuning voltage. Based on the simulation results, the circuit draws 2 mA without buffers and 14.5 mA from 2.5 V supply including buffer circuits leading to a total power dissipation of 36.25 mW. The circuit layout occupies an area of 0.6 mm^2 on Si substrate, including DC and RF pads. © 2007 Wiley Periodicals, Inc. Int J RF and Microwave CAE 17: 243–251, 2007.

Keywords: VCO; SiGe; BiCMOS; WLAN; differential tuning; accumulation MOS varactors; RFIC

I. INTRODUCTION

Unlicensed National Information Infrastructure (UNII) band (5–6 GHz) has been authorized in many countries for WLAN high-speed applications. Some of these are the 802.11a and recently developed 802.11n, operating at 5 GHz band with a greater data rate approaching 108 Mbits/s. As the numbers of products grow and the types of the products evolve, high performance oscillators with low phase noise, low power dissipation, satisfactory output power, and tuning range increase their importance in today's wireless applications [1].

Integrated voltage controlled oscillators (VCOs) are one of the important blocks of modern RF transceiver architectures. They are utilized in a number of applications as a source of signal generation [2, 3] and as a part of data or clock recovery systems [4]. Among these applications of VCOs, design for wireless communications has more stringent specifications than for other applications. IEEE 802.11a standard uses orthogonal frequency multiplexing (OFDM) based modulation scheme which is more sensitive to phase noise compared with single carrier modulation schemes. Thus, phase noise is probably the most stringent specification for a wireless VCO. To meet the requirements for IEEE 802.11a standard, the phase noise of the VCO should be lower than −110 dBc/Hz at 1 MHz offset from the carrier frequency [5].

Tuning range is also an important performance parameter and has been a major problem for VCOs in

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CMOS or BiCMOS technologies. Because of the limited tuning range of p-n junction varactors and inversion MOS varactors, accumulation mode is generally preferred [6, 7]. The tuning range of accumulation-mode MOS varactors is proven to be the highest among other varactor types. In addition, the VCO circuit can be tuned more linearly with accumulation-mode MOS varactors [8].

Another issue in VCO design is high varactor sensitivity. A high C_{max}/C_{min} ratio over a low voltage tuning range degrades the phase noise performance [9]. Differential tuning provides a simple but effective solution to avoid the drawbacks of this effect.

Output power and power dissipation are other parameters determining the performance of VCOs. A well-designed VCO should send enough power to its output to drive the mixer and should dissipate the minimum power for a longer battery lifetime.

A VCO meeting the specifications of IEEE 802.11a standard may be implemented utilizing various technologies and topologies. By technology, the combination of the material system and transistor type is meant throughout this paper. Recently published works include realizations with InGaP/GaAs HBT, SiGe BiCMOS, Si CMOS, and Silicon-on-insulator (SOI) CMOS.

A 4.39 GHz cross-coupled VCO realized with InGaP/GaAs technology demonstrates a phase noise of −118 dBc/Hz at 1 MHz offset and its tuning range is 290 MHz [10]. Tuning range is relatively low when compared with standard's 5–6 GHz coverage.

CMOS VCOs with 0.35 μm lithography suffer from relatively poor phase noise performance due to the lateral structure of MOSFETs [11]. Nevertheless, an implementation with 0.25 μm lithography satisfies the IEEE 802.11a phase noise specification [12]. However, tuning range is only 240 MHz and insufficient for a whole coverage of the desired spectrum. A remarkable work accomplished with 0.18 μm CMOS has demonstrated a 780 MHz tuning range and −134 dBc/Hz phase noise at 3 MHz offset, while drawing only 3.5 mA from 1.5 V supply [13]. However, the design is costly when compared to 0.35 μm lithography.

A recent work with SOI CMOS presents a 5.8 GHz VCO implementation with a 2.56 GHz tuning range [9]. A −115 dBc/Hz phase noise at 1 MHz offset is remarkably low when considering the high tuning range. This is accomplished by taking the advantage of SOI substrate and eliminating the varactor sensitivity effect with differential tuning.

Among these realizations, SiGe BiCMOS technology leads others from an application point of view [14, 15]. This is because it combines the cost and integration advantages of Si material system with the performance advantages of SiGe HBTs. High tuning ranges can be obtained utilizing a MOS varactors with C_{max}/C_{min} ratio about 4. In addition, phase noise is expected to be lower due to vertical structure of HBTs. SiGe BiCMOS technology is considered to be a candidate solution for low-noise single-chip RF transceiver designs [16].

SiGe BiCMOS (0.35 μm) is decided as the suitable technology, since it combines the cost and integration advantages of Si with the performance advantages of band-gap engineered SiGe HBTs. With this technology and topology, a low phase noise, high tuning range VCO for 5–6 GHz UNII band applications is designed. The proposed VCO is tunable from 4.2 to 5.4 GHz with a worst case phase noise of −110.7 dBc/Hz at 1 MHz offset from 5.4 GHz carrier. The layout occupies 0.6 mm^2 on Si substrate drawing 14.5 mA from 2.5 V supply including buffers.

The organization of the paper is as follows: Section II develops the VCO design in detail giving the design issues for the core, buffer, and LC tank separately; Section III analyses and discusses the post layout simulation results; Section IV describes the layout design of the circuit and finally Section V concludes the paper.

II. DIFFERENTIAL −GM LC VCO DESIGN

A. Circuit Topology

Considering topologies, RF VCOs can be realized as resonator (LC) based oscillators [17], ring oscillators [18], or multivibrator oscillators [19]. Conceptually, very high tuning ranges can be obtained with multivibrator oscillators. Also, ring oscillator is the simplest topology that is composed of odd numbers of inverter stages and again tuning range can be satisfactory. However, these oscillators, not having inductors, usually have less spectral purity than their LC counterparts. Among the three topologies, LC based oscillators are most prominent ones due to their relatively low phase noise.

Resonator-based VCOs work with the principle of adding negative resistance through feedback to a resonator. By tuning the resonator, the desired frequency range can be covered. Feedback (or negative resistance) is usually provided by using a tapped capacitor and amplifier (Collpitts oscillator) using a tapped inductor and amplifier (Hartley oscillator) or using two amplifiers (−Gm oscillator). Among these, Hartley topology is not usually preferred because of

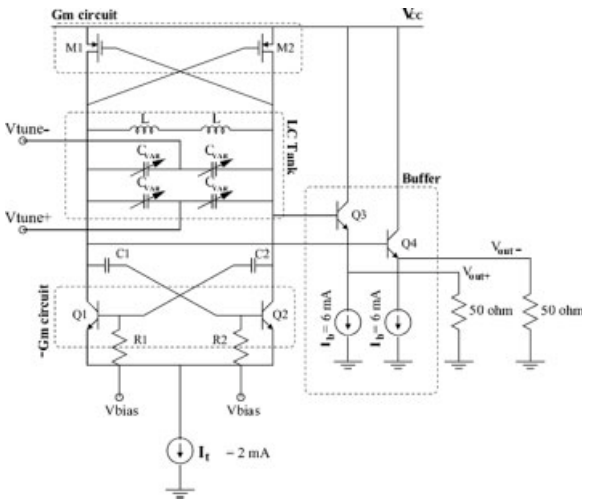

Figure 1. Schematic of the VCO.

the difficulties in IC tapped-inductor implementations. Although there are a number of successful realization with Colpitts configuration, −Gm topology generally results in higher performance in wireless designs [19].

Keeping the stringent phase noise requirement, other performance parameters and topological advantages in mind, differential LC −Gm configuration is chosen in this work. Differential topology is utilized for its additional advantages: First, VCO mostly drives the mixer, most of which is composed of differential Gilbert cell. Another benefit is that it will yield a higher common mode rejection ratio (CMRR), thus higher linearity. Finally, differential topology enhances the output power at the expense of increased power consumption, larger chip area, and increased complexity [20].

The design is classified into three parts as the core, the LC tank, and the buffer, and is discussed in detail below.

B. VCO Core

The technology used in this design is a 0.35 μm four-metal double-poly SiGe BiCMOS process of Austria MicroSystems (AMS) with a thick metal option. It includes high-speed SiGe HBTs with 59 GHz and 63 GHz f_t and f_{max} values, respectively. HBTs with two base contacts are utilized to reduce the base resistance, the critical source of noise in bipolar transistors.

The topology for the VCO is a differential −Gm LC configuration given in Figure 1. It consists of three parts, namely the −Gm circuit (Q1, Q2, M1, and M2), the LC tank (L and C_{var}) and the buffer (Q3 and Q4). The PMOSs together with the npn HBTs in the −Gm part are utilized to obtain additional negative resistance. Also DC level of the oscillation nodes is adjusted by these PMOS devices. This HBT-PMOS cross-coupled pair brings two important improvements over the HBT-only structure: first, it has bigger tank amplitude for a given current reducing the power dissipation; second, it can be optimized to have more symmetrical output wave leading to a better phase noise.

The core of the oscillator benefits from HBT transistors which have the high f_T and f_{max}, lower $1/f$ noise [21], reduced broadband shot noise and thermal noise compared to that of FETs [22] and higher transconductance for a given bias [23]. The HBTs also operate better at lower DC current values providing lower phase noise at lower power dissipation. The VCO illustrated in Figure 1 is operated at the current limited regime in order to reduce power consumption and obtain higher spectral purity [24]. In the current limited regime, the tank amplitude is proportional to the tail current or equivalent parallel tank resistance, while V_{dd} or a change in the operation mode limits it in the voltage-limited regime.

C. LC Tank

The LC tank circuit consists of inductors and varactors. The main difference of the circuit topology from the conventional differential LC tank structure is the differentially tuned accumulation MOS varactors. Differential tuning provides a solution to avoid the drawbacks of high varactor sensitivity (k_v) effect. A high C_{max}/C_{min} ratio over a low voltage tuning range, meaning high varactor sensitivity, degrades the phase noise performance as described by the modified Leeson's Formula [9];

$$L(\Delta f, k_v) = 10\ \log\left\{ \left(\frac{f_0}{2Q\Delta f}\right)^2 \left[\frac{FkT}{2P_s}\left(1+\frac{f_c}{\Delta f}\right)\right] + \left(\frac{k_v v_n}{2k_{LC}\Delta f}\right)^2 \right\} \quad (1)$$

Here, f_o is the frequency of oscillation, Q is the quality factor, Δf is the frequency offset from the carrier, F is the noise factor, k is the Boltzmann's constant, T is the temperature, P_s is the RF power produced by the VCO, f_c is the Flicker noise corner frequency, v_n is the common mode noise voltage and k_{LC} is a constant that is a function of L and C of the resonator.

Utilizing differentially-tuned varactors at the tank circuit enables one to suppress common mode noises,

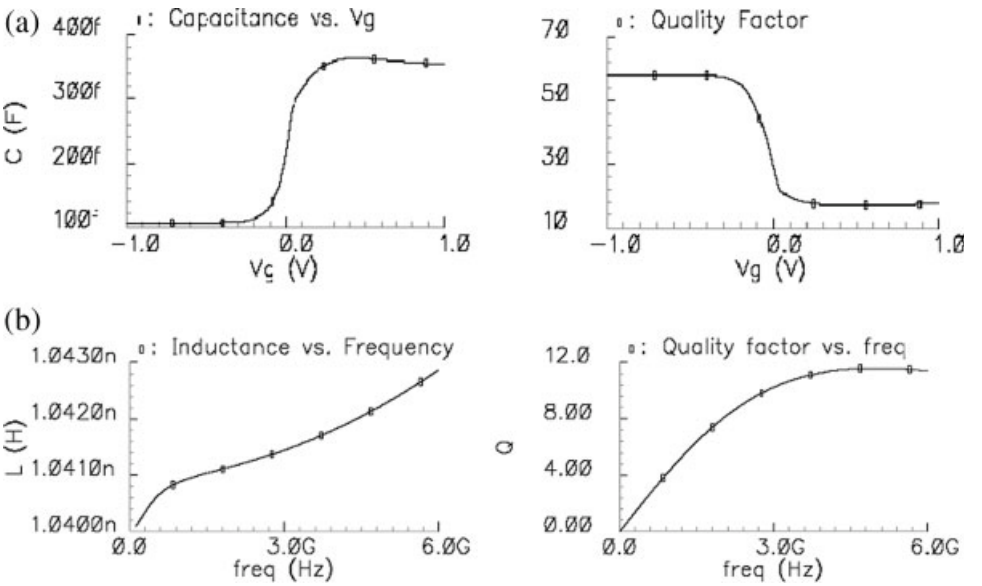

Figure 2. (a) Characteristics of the varactor utilized in the design and (b) characteristics of the inductor utilized in the design.

such as flicker noise from being upconverted to the carrier frequency, resulting in a better phase noise performance.

The elements of LC tank is analyzed individually. The characteristics of a single varactor at 5.4 GHz are shown in Figure 2a. This varactor has a C_{max}/C_{min} about three over a tuning voltage of ± 800 mV. The quality factor has a maximum value of 60 and minimum value of 20, depending on the tuning voltage.

Characteristics of the inductor of the LC tank can be observed in Figure 2b. The inductor is from AMS library and has an inductance value of 1.04 nH with a quality factor of 11.8 at 5 GHz.

The quality factor of the overall tank circuit is determined from the parasitic conductances of capacitance and inductance. Since accumulation mode MOS varactors have relatively higher Q values than on-chip inductors, inductor Q is the main determining factor of the overall Q of the tank circuit.

The utilization of the capacitances C_1 and C_2 is a refinement to the $-$Gm topology and can also be thought as the parts of the LC tank. They are added to the design in order to get larger swings by decoupling the base from the collector. In addition, the center frequency can be fine-tuned without changing the tuning range with C_1 and C_2.

D. Buffer

Buffer is the link between the output stage of the VCO core and the output port. In the design of the buffer two essential criteria needs to be considered. First, it should provide adequate power to the output 50-Ohm termination impedances. Second, it provides adequate isolation between the output and the VCO core. The input impedance of the buffer must be high enough to prevent the measurement equipment from degrading the Q-factor of the LC tank. If we connect the outputs of the core directly to the 50-Ohm ports, the resultant swing reduces considerably, due to the reduction in the parallel tank resistance. Furthermore, the degradation of the output swing may be so high that the circuit does not oscillate.

III. POST-LAYOUT SIMULATION RESULTS

In this design, we mainly aimed for a low phase-noise to meet the phase noise specification of the IEEE 802.11a standard. High and linear tuning range capability is another design target as well as minimized power dissipation and reasonable output power.

Phase noise at a given offset for a linear time variant (LTV) oscillator can be improved by maximizing the Q of the resonator, maximizing the carrier power or minimizing the varactor sensitivity effect, as shown in eq. (1) [9]. Resonator Q is limited by the tank inductance even if buffering prevents the degradation of the resonator Q with its high input impedence. So, highest Q inductor of the library is selected for the design (Fig. 2b). After the values of

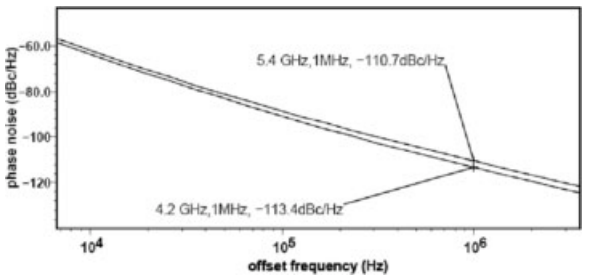

Figure 3. Phase noise of the VCO.

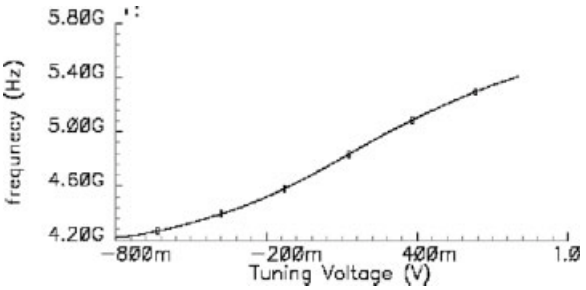

Figure 4. Output frequency vs. differential tuning voltage.

LC tank elements is set, the minimum current for oscillation is calculated and for a safe oscillation, about three times higher current than the minimum current for oscillation is provided by the tail current (for each oscillation node). However, the phase noise is still under demands of the standard with this output power and is increased to four times the minimum current leading to 1 mA from each oscillation branch. One should take into account the trade-off that increasing the carrier power also increases the power dissipation.

Other design strategies for an improved phase noise are minimizing the varactor sensitivity effect and choosing active devices with low $\omega_{1/f}$ frequencies. As briefly explained in Section II, differential tuning of the varactors improves the varactor sensitivity related degradation of the phase noise. Furthermore, HBTs with lower $\omega_{1/f}$ frequencies than MOS counterparts are utilized for a better phase noise.

Phase noise data is sampled for different carrier frequencies (tuning voltages) giving a family of curves between 4.2 GHz and 5.4 GHz. As expected from the oscillator phase noise theory [25], it degrades with the increasing center frequency, so it is lowest for 4.2 GHz and highest for 5.4 GHz. Phase noise simulated at 1 MHz offset from 5.4 GHz carrier is -110.7 dBc/Hz, as illustrated in Figure 3. It is also simulated -113.4 dBc/Hz from 4.2 GHz carrier. Both of these values exceed the phase noise specification of the standard, which is -110 dBc/Hz for the same offset [5]. This also exceeds the phase noise performances of recently published VCOs that are realized with 0.35 μm lithography and similar topology [15, 26].

Frequency tuning is performed by changing differential $V_{\text{tune}(+)}$ and $V_{\text{tune}(-)}$ over a fixed value of 1.2 V which is approximately $V_{CC}/2$. 1.2 V is chosen so as to obtain a higher tuning range. Choosing the zero-tuning voltage at about $V_{CC}/2$ for a differentially-tuned VCO, one is able to get higher voltage headroom for tuning the circuit. In addition, it decreases the oscillator sensitivity. So the effect of high varactor sensitivity, which degrades phase noise, is reduced. This DC value can be easily set by the PMOS transistors. Actually, $V_{\text{tune }(+)} = -V_{\text{tune }(-)} = V_{\text{tune}}$; thus changing V_{tune} from -0.8 V to 0.8 V effectively changes the total voltage from 0.4 V to 2 V. This is the interval where tuning range can be assumed linear. For tuning voltages lower than 0.4 V and higher than 2 V, the linearity of capacitance change in varactors, in other words the linearity of tuning range is degraded. As illustrated in Figure 4, the linearity is not perfect at the corners of the tuning range since the varactor operation region starts to change into accumulation from depletion and the capacitance value converges to the gate-oxide capacitance, C_{ox}.

Output power of an oscillator should be high enough so that it can deliver enough power to the following stage in the transceiver architecture, the mixer. However, it should also be limited not to overload the input of the mixer. After the buffer stage is connected and for 50-Ohm terminations at the output of the buffer, fundamental frequency power is obtained between 4.8 dBm and 5.5 dBm at the corners of the tuning voltage. The differential peak-to-peak voltage swing at the buffer output is 1.2 V. Fundamental output power can be observed in Figure 5. The difference in the power levels for different tuning voltages can be explained as the result of wide

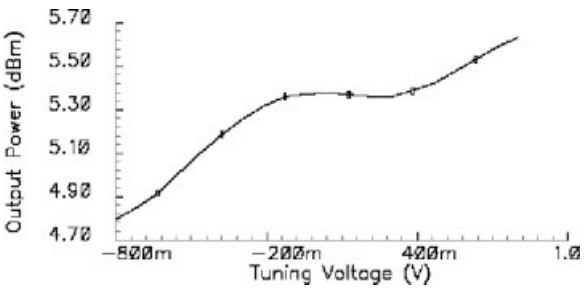

Figure 5. Fundamental frequency output power vs. differential tuning voltage.

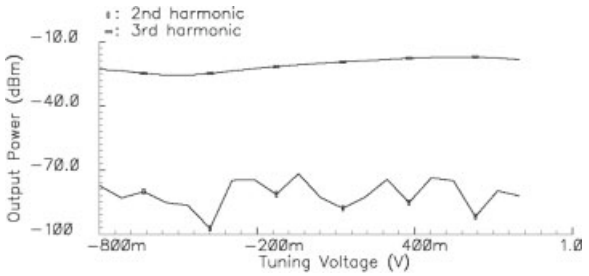

Figure 6. Second and third harmonic output power vs. differential tuning voltage.

frequency coverage. The power levels for the whole tuning range can be equalized; however, this approach is avoided since will increase circuit complexity and power consumption. Second and third harmonic output power need to be suppressed for neat and clear signal at the output. The −82 dBm (87.5 dBc) suppression in the second harmonic is remarkable, as shown in Figure 6. This is due to differential circuit topology that rejects the common mode noise and provides a linear tuning across the covered frequency band. The third harmonic level is also adequately suppressed and has an average of −21 dBm (−26.5 dBc) throughout the 4.2–5.4 GHz band.

Power dissipation is another concern during the design and is minimized with proper DC bias. To minimize the power dissipation and prevent the distortion of the output signal, the HBTs are operated within their current-limited regime instead of voltage-limited regime. For a low 1/*f* noise, the HBTs should be biased at their maximum β. However, this bias is usually below the current where maximum f_t of the transistor is reached. Since, maximum f_t of the HBTs is about 60 GHz, operating frequency of 5 GHz can be reached without the need of biasing at maximum f_t. Hence, the HBTs are biased between maximum β and maximum f_t. The bias point of the HBTs in this design is $f_t \sim 37$ GHz and $\beta \sim 200$. Doing so, high-speed operation as well as low phase noise is aimed. Additionally, increasing the transistor size lowers 1/*f* noise but increases power consumption. The emitter width of the HBTs utilized in the VCO (Q1 and Q2) core is 21.5 μm^2. Buffer HBTs (Q3 and Q4), however, have larger emitter widths of 24 μm^2 for better isolation from the measurement equipment. After the biasing constraints and oscillation condition is taken into account, the VCO core draws 2 mA from current source whereas 12.5 mA is dissipated in the buffer circuitry. Even if some excess current is drawn for oscillation safety, the power dissipated in the oscillator core is lower than previous works realized with SiGe BiCMOS technology and 2.5 V supply voltage [22, 27]. The total current drawn from the 2.5 V supply is 14.5mA, which means a DC power cosumption of 36.25 mW.

Performance summary of the VCO circuit according to the post-layout simulations is given in Table I.

TABLE I. VCO Post Layout Simulation Performance

	VCO Performance
Total current/power dissipation	14.5 mA/36.44 mW
Current/power dissipated (core)	2 mA/5 mW
Output frequency	4.2–5.4 GHz
Phase noise at 1 MHz offset	−113.4 to –110.7 dBc/Hz
Tune voltage range	0.4–2 V
Maximum differential output power	5.5 dBm
Average second harmonic power	−82 dBm (87.5 dBc)
Average third harmonic power	−21 dBm (26.5 dBc)
Supply voltage	2.5 V

IV. LAYOUT DESIGN

The physical layout of the VCO is shown in Figure 7. Some efforts are made to reduce the parasitics as well as the sensitivity to parasitics. The layout is symmetric to minimize the even order distortion of the output waveform. In other words, the VCO circuit is divided into two identical oscillation nodes with inverse phases.

The most critical nodes are the positive and negative oscillation nodes which have to be carefully designed to prevent capacitive and resistive parasitic effects. The connections of these nodes is done by the top metal layer of the process to reduce the capacitance with substrate. Again for the oscillation node, Metal-Insulator-Metal (MIM) capacitances are utilized due to their higher quality factor and linearity. However, this may not bring much improvement

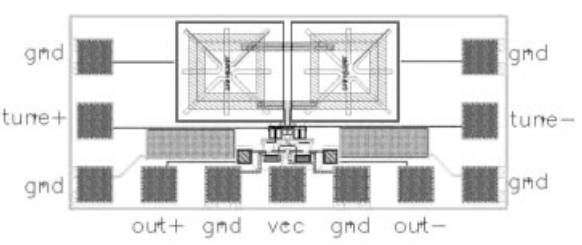

Figure 7. VCO layout.

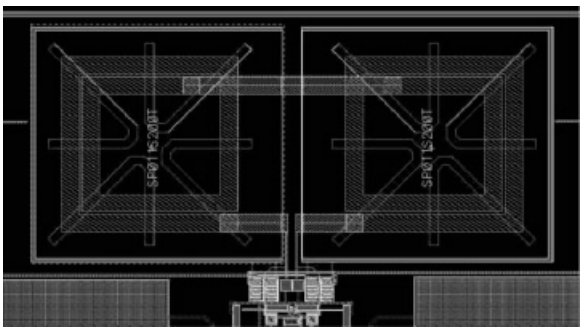

Figure 8. VCO layout detail, inductors.

since the quality factor of the resonator is determined by the inductor. Thinner lower-metal lines are avoided since their current carrying capability is lower than higher-metal lines. Also, thicker lines increases the parasitic capacitance which probably mistune the center frequency. Finally, corners and sharp turns are avoided in the RF path to prevent the degradation of RF signal from these regions.

Delving into more detail, layout can be analyzed in three parts as inductors, varactors and the bias circuitry.

Instead of a single 2.1 nH inductor, two series 1.05 nH inductors are used to keep the circuit symmetry. The unshielded sides are located face-to-face so as to cancel the magnetic effect of each other as shown in Figure 8. The spirals are formed by the thick metal layer of the process which is 2.5 μm wide. With thick metal layer, it is possible to increase the quality factor of the inductor, which is the most critical in the LC tank. The quality factor of the inductor is 11.8 at 5 GHz.

The second part of the layout is formed by the MOS varactors. Its layout is composed of parallel connected small capacitors. The rows and columns can be seen in Figure 9. With a $\pm$ 0.8 V tuning voltage over 1.2 V DC, the each capacitor is tuned from 102 fF to 376 fF leading to a C_{max}/C_{min} ratio of 3.67. The quality factor of the varactors is 20 when its gate-bulk capacitance 102 fF and it is 20 when the capacitance is 376 fF. This change in the varactor quality factor will not citically effect the overall

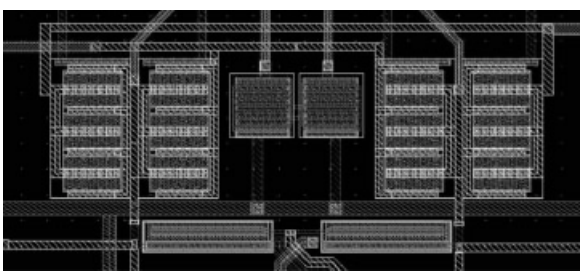

Figure 9. VCO layout detail, varactors.

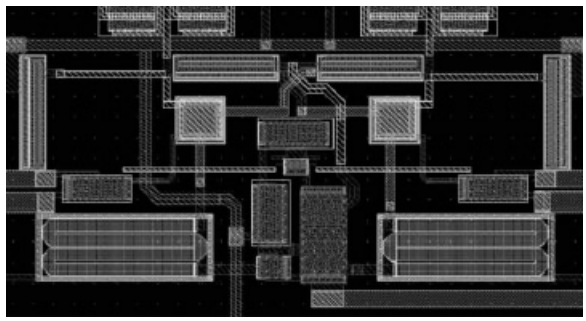

Figure 10. VCO layout detail, bias circuitry.

quality factor of the resonator since it is mainly determined by the inductor.

The third part is the bias circuitry formed by the transistors and resistors. Resistors are formed by the second poly-Si layer of the process and have a resistance of 2.67 kO. The tail current of the LC tank is 2 mA providing 1 mA DC current for each branch. This is about four times the current needed for the startup so as to keep the oscillation safe. Detailed bias circuitry is illustrated in Figure 10.

The whole circuit has dimensions of 1.16×0.52 mm^2 including RF and DC pads occupying an area of 0.6 mm^2 on Si die, as shown in Figure 7.

V. CONCLUSION

An integrated 4.2–5.4 GHz low phase-noise VCO for wireless applications is designed utilizing 0.35 μm SiGe BiCMOS technology. Based on the post layout simulation results, the VCO can be tuned using a DC voltage of 0.4 to 2 V for a bandwidth of 1.2 GHz. The designed and simulated VCO can generate a differential output power of 5.5 dBm with a total power consumption of 36.44 mW including buffers. Typical second and third harmonics levels are simulated to be -82 dBm (87.5 dBc) and -21 dBm (26.5 dBc), respectively. Phase noise of -110.7 to -113.4 dBc, simulated at 1 MHz offset, can be obtained through the frequency of interest, which satisfies the IEEE 802.11a standard requirement.

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REFERENCES

1. A.J. Joseph, D.L. Harame, B. Jagannathan, D. Coolbaugh, D. Ahlgren, J. Magerlein, L. Lanzerotti, N. Feilchenfeld, S. St Onge, J. Dunn, and E. Nowak, Status and direction of communication technologies-SiGe BiCMOS and RF CMOS, Proc IEEE 93 (2005), 1539–1558.
2. H. Moon, K. Sungweon, T.K. Youn, and L. Kwyro, A fully differential LC-VCO using a new varactor control structure, IEEE Microwave Wireless Components Lett 14 (2004), 410–412.
3. M.A. Margarit, D. Shih, P.J. Sullivan, and F. Ortega, A 5-GHz BiCMOS RFIC front-end for IEEE 802.11a/HiperLAN wireless LAN, IEEE J Solid State Circuits 38 (2003), 1284–1287.
4. S.B. Anand and B. Razavi, A CMOS clock recovery circuit for 2.5-Gb/s NRZ data, IEEE J Solid State Circuits (2001) 36, 432–439.
5. IEEE Std. 802.11 Wireless LAN medium access control (MAC) and physical layer (PHY) specifications: High-speed physical layer in the 5 GHz band, IEEE, Sept 1999.
6. De B. Muer, M. Borremans, M. Steyaert, and G. Li Puma, A 2-GHz low-phase-noise integrated LC-VCO set with flicker-noise upconversion minimization, IEEE J Solid-State Circuits (2000) 35, 1034–1038.
7. P. Andreani, A comparison between two 1.8 GHz CMOS VCOs tuned by different varactors, Proceedings of 22nd European Solid-State Circuits Conference (ESSCIRC), Haag, Netherlands, 1998, pp. 380–383.
8. R.L. Bunch and S. Raman, Large-signal analysis of MOS Varactors in CMOS Gm LC VCOs, IEEE J Solid-State Circuits 38 (2003), 1325–1332.
9. N.H.W. Fong, J.-O. Plouchart, J. Zamdmer, L. Duixian, L.F. Wagner, C. Plett, and N.G. Tarr, A 1-V 3.8-5.7-GHz wide-band VCO with differentially tuned accumulation MOS Varactors for common-mode noise rejection in CMOS SOI technology, IEEE Trans Microwave Theory Techniq 51 (2003), 1952–1959.
10. E. Yunseong. E.K. Keechul, and O. Byungdu, Low noise 5 GHz differential VCO using InGaP/GaAs HBT technology, IEEE Microwave Wireless Components Lett 13 (2003), 259–261.
11. C. Lam and B. Razavi, A 2.6-GHz/5.2-GHz frequency synthesizer in 0.4-μm CMOS technology, IEEE J Solid State Circuits 35 (2000), 788–794.
12. S.M. Wu, A 5.8-GHz high efficient, low power, low phase noise CMOS VCO for IEEE 802.11a, Proceedings of the 3rd IEEE International Workshop on System-on-Chip for Real-time Applications, Calgary, Canada, 2003, pp. 127–129.
13. B. Chi and B. Shi, Low power CMOS VCO and its divide-by-2 dividers with quadrature outputs for 5GHz/2.5GHz WLAN transceivers, IEEE 2002 International Conference on Communications, Circuits and Systems and West Sino Expositions, Chengdu, China, pp. 525–528.
14. L. Dermentzoglu, G. Kamoulakos, and A. Arapoyanni, An Extra Low noise 1.8 GHZ voltage controlled oscillator in 0.35 SiGe BiCMOS technology, IEEE 9th International Conference on Electronics, Circuits and Systems, Dubrovnik, Croatia, 2002, pp. 89–92.
15. G.K. Young, S.K. Hyun, H.B. Jung, H.O. Jae, and W.K. Chang, Fully integrated differential VCO with buffer amplifier using 0.35 μm SiGe BiCMOS for C-Band wireless RF transceiver, Proceedings of the IEEE Radio and Wireless Conference, Boston, MA, 2003, pp. 297–300.
16. M. Feng, S. Shyh-Chiang, D.C. Caruth, and J.-J. Huang, Device technologies for RF front-end circuits in next-generation wireless communications, Proc IEEE 92 (2004), 354–375.
17. H. Shin, X. Zhiwei, and M.F. Chang, A 1.8-V 6/9-GHz reconfigurable dual-band quadrature LC VCO in SiGe BiCMOS Technology, IEEE J Solid-State Circuits 38 (2003), 1028–1032.
18. Y.U. Yim, J.F. McDonald, and R.P. Kraft, 12–23 GHz ultra wide tuning range voltage-controlled ring oscillator with hybrid control schemes, Proceedings of IEEE Computer Society Annual Symposium on VLSI, Tampa, FL, 2005, pp. 278–279.
19. J. Rogers and C. Plett, Radio frequency integrated circuit design, Artech House, Boston, 2003.
20. A. Hajimiri and T.H. Lee, Design issues in CMOS differential LC oscillators, IEEE J Solid-State Circuits 34 (1999), 717–724.
21. D. Greenberg, S. Sweeney, C. LaMothe, K. Jenkins, D. Friedman, B. Martin Jr, G. Freeman, D. Ahlgren, S. Subbanna, and A. Joseph, Noise performance and considerations for integrated RF/analog/mixed-signal design in a high-performance SiGe BiCMOS technology, In the Proceedings of 2001 IEEE International Electron Devices Meeting (IEDM) Technical Digest, 2001, pp. 22.1.1–22.1.4.
22. D.I. Sanderson, 5–6 GHz Silicon-Germanium VCO with tunable polyphase outputs, M.Sc. Thesis, Virginia Polytechnic Institute and State University, Blacksburg, Virginia, May 2003.
23. E. Abou-Allam, T. Manku, M. Ting, and M.S. Obrecht, Impact of technology scaling on CMOS RF devices and circuits, In the Proceedings of 2000 IEEE Custom Integrated Circuits Conference (CICC), Orlando, FL, 2000, pp. 361–364.
24. D. Ham and Ali Hajimiri, Concepts and methods in optimization of integrated LC VCOs, IEEE J Solid-State Circuits, (2001) 36, 896–909.
25. A. Hajimiri and T. Lee, The design of low noise oscillators, Kluwer Academic, 2004.
26. A.H. Mostafa, CMOS 5-10 GHz oscillators for low voltage RF Applications, Proceedings of 43rd IEEE Midwest Symposium on Circuits and Systems, Lansing MI, 2000, vol. 1, pp. 478–481.
27. M. Chu, D.J. Allstot, J.M. Huard, and K.Y. Wong, NSGA-based parasitic aware optimization of a 5GHz low-noise VCO, Proceedings of the IEEE Asia and South Pacific Design and Automation Conference, Yokohama, Japan, 2004, pp. 169–174.

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