A WIDEBAND SINGLE-CHANNEL RECEIVER FRONT-END FOR C/X/KU/KA-BAND SATCOM SYSTEMS

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A WIDEBAND SINGLE-CHANNEL RECEIVER FRONT-END FOR C/X/KU/KA-BAND SATCOM SYSTEMS

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ABSTRACT

A WIDEBAND SINGLE-CHANNEL RECEIVER FRONT-END FOR C/X/KU/KA-BAND SATCOM SYSTEMS

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This thesis focuses on the design and implementation of a radio frequency (RF) integrated receiver for satellite communication (SATCOM). Increasing the bandwidth is one of the key enablers to achieve higher data rates. In mm-wave, a larger bandwidth can be allocated. Since Low-Earth orbit (LEO) SATCOM systems are promising for global connectivity and internet coverage, these SATCOM applications have gathered attention recently. Currently licensed frequency bands for SATCOM reception are C-, X-, Ku-, and Ka-bands. A wideband receiver RF module that covers these SATCOM bands would be cost-efficient. On the other hand, due to orbiting around Earth at more than 200 km altitudes and utilizing mm-wave, the atmospheric path loss is increased. To compensate for increased path loss, one can employ MIMO arrays.

This thesis presents two separate single-channel receiver-ICs for SATCOM applications. The first receiver includes a low-noise amplifier (LNA) and a phase shifter. The designed receiver achieved a 6-bit phase resolution over a bandwidth of 5.7-25 GHz. The first receiver exhibits a peak output referred the third-order intercept point (OIP3) and input referred 1-dB compression point (IP_{1dB}) of -22 dBm and -23.4 dBm, respectively, thanks to the post-distortion technique employed in the LNA. The second receiver is based on sub-blocks: an LNA, a phase shifter-attenuator, and a variable gain amplifier (VGA). The same post-distortion method is applied in the LNA. A passive vector sum phase shifter topology is adopted to enhance linearity performance. The phase shifter architecture is based on a novel close-loop voltage variable attenuator (VVA). The proposed VVA enables to achieve

both phase and amplitude control functionality in a single block with low RMS phase and amplitude error. Also, a quadrature hybrid coupler is utilized with a 1^{st}-order polyphase filter (PPF) to obtain 6-bit phase resolution over a wide bandwidth. The VGA is based on a distributed amplifier topology with an RC-feedback to obtain wideband low amplitude error. The second receiver achieves a gain of 25 dB, a minimum noise figure (NF) of 2.7 dB, and -23 dBm IP_{1dB} over a wide frequency range of 7-26.4 GHz, which covers multiple licensed frequency bands for SATCOM reception. The second receiver provides 6-bit phase resolution with 5.6° RMS phase error and 36-dB attenuation range.To the best of the authors' knowledge, this receiver achieved the highest attenuation range and highest linearity that supports the multiple licensed frequency bands for SATCOM reception thanks to passive vector sum with the proposed VVA and the post-distortion method applied in the LNA.

ÖZET

C/X/KU/KA-BANT SATCOM SİSTEMLERİ İÇİN GENİŞ BANT TEK KANALLI ALICI ÖN UCU

TAHSIN ALPER ÖZKAN

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Tez Danışmanı: Prof. Dr. Yaşar Gürbüz

Anahtar Kelimeler: SATCOM, alıcı, hüzmeleme, faz dizileri, SiGe BiCMOS

Bu tez, uydu haberleşmesi (SATCOM) için bir radyo frekansı (RF) entegre alıcının tasarımı ve uygulamasına odaklanmaktadır. Bant genişliğinin artırılması, daha yüksek veri hızlarına ulaşmanın temel unsurlarından biridir. mm dalga boylarında daha büyük bir bant genişliği tahsis edilebilir. Alçak Dünya yörüngesi (LEO) SATCOM sistemleri küresel bağlantı ve internet kapsamı için umut vaat ettiğinden, bu SATCOM uygulamaları son zamanlarda dikkat çekmektedir. Şu anda lisanslı SATCOM yayın frekans bantları C, X, Ku ve Ka bantlarıdır. Bu SATCOM bantlarını kapsayan geniş bantlı bir alıcı RF modülü uygun maliyetli olacaktır. Öte yandan, Dünya etrafında 200 km'den fazla irtifada yörüngede olması ve mm dalga boylarını kullanması nedeniyle atmosferik yol kaybı artmaktadır. Artan yol kaybını telafi etmek için MIMO dizileri kullanılabilir.

Bu tez, SATCOM uygulamaları için iki ayrı tek kanallı alıcı-IC sunmaktadır. İlk alıcı, düşük gürültülü bir yükselteç (LNA) ve bir faz kaydırıcı içerir. Tasarlanan alıcı, 5,7-25 GHz bant genişliği üzerinde 6 bit faz çözünürlüğü elde etti. İlk alıcı, LNA'da kullanılan bozulma sonrası tekniği sayesinde, üçüncü dereceden kesme noktasına (OIP3) referanslı tepe çıkışı (-22 dBm) ve 1 dB sıkıştırma noktasına (IP1dB) referanslı girişte sırasıyla -23,4 dBm'lik bir tepe çıkışı sergiledi. İkinci alıcı, alt bloklara dayanmaktadır: bir LNA, bir faz kaydırıcı-zayıflatıcı ve bir değişken kazançlı amplifikatör (VGA). Aynı bozulma sonrası yöntemi LNA'da da uygulandı. Doğrusallık performansını artırmak için pasif vektör toplamı faz kaydırıcı topolojisi benimsenmiştir. Faz kaydırıcı mimarisi, yeni bir kapalı çevrim gerilim kontrollü zayıflatıcıya (VVA) dayanmaktadır. Önerilen VVA, düşük RMS faz ve genlik hatası ile tek

bir blok içinde hem faz hem de genlik kontrol işlevselliğini gerçekleştirmeye olanak tanımıştır. Ayrıca, geniş bir bant genişliği üzerinde 6 bit faz çözünürlüğü elde etmek için bir-dereceli çok fazlı filtre (PPF) ile bir kareel hibrit kuplör kullanılmıştır. VGA, geniş bant düşük genlik hatası elde etmek için RC geri beslemeli dağıtılmış bir amplifikatör topolojisine dayanmaktadır. İkinci alıcı, SATCOM alımı için birden fazla lisanslı frekans bandını kapsayan 7-26,4 GHz geniş bir frekans aralığında 25 dB'lik bir kazanç, 2,7 dB'lik minimum gürültü değeri (NF) ve -23 dBm IP_{1dB} elde ediyor. İkinci alıcı, 5.6° RMS faz hatası ile 6 bit faz çözünürlüğü ve 36 dB zayıflatma aralığı sağlamaktadır. Yazarların bilgi birikimine göre, bu alıcı; LNA'da uygulanan bozulma sonrası yöntemi, ve önerilen VVA'nın kullanıldığı pasif vektör toplamı metotları sayesinde, SATCOM alımı için birden fazla lisanslı frekans bandını destekleyen en yüksek zayıflatma aralığını ve en yüksek doğrusallığı elde etmiştir.

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Eşime ve aileme...
To my wife and my family...

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MIMO Multiple-Input-Multiple-Output 3

NF Noise Figure 5

Opamp Operational Amplifier 40

PPF Poly-Phase Filters 38

QAF Quadrature All-Pass Filter 35

RF Radio Frequency 9

RMS Root Mean Square 17

SATCOM Satellite Communication 4

SLL Side-Lobe Level 16

SMS Short Message Service 1

SoC System-on-Chip 6

SOLT Short-Open-Load-Thru 28

SPI Serial-to-Parallel Interface 55

T/R Transmit/Receive 14

TTD True-Time Delay 20

TUBITAK Turkish Scientific and Technology Research Institution viii

UHD Ultra High Definition 1

VGA Variable Gain Amplifier 14

VVA Voltage-Variable Attenuator 19

1. INTRODUCTION

Since the invention of cell phones, successive generations of wireless communication technologies has been part of our daily life. Each successive generation has consistently aimed for, and achieved, higher data rates, as illustrated in Fig. 1.1 (Al Mtawa, Haque & Bitar, 2019). These enhanced data rates have opened up the way for more sophisticated and high-quality applications. For instance, the 2G introduced short message service (SMS) whereas video call was enabled with the 3G. As a consequence, the expected application domains for subsequent generations have become significant drivers for technological advancements. For context, current high-definition (HD) video streaming demands bandwidths between 1-5 Mbps, but it's projected that 16K high-definition streaming will require a much more high data rate of 100-500 Mbps (Clemm, Vega, Ravuri, Wauters & Turck, 2020). Sectors such as healthcare, immersive Ultra High Definition (UHD) and three-dimensional (3D) video services, augmented reality, and smart homes highlight the transformative potential of 5G technology (Xiang, Zheng & Shen, 2016; Yifei & Longming, 2014). On top of the growing bandwidth demand, the number of internet users has been gradually increasing from 1 billion (16% of internet users) in 2005 to 5.5 billions (68% of internet users) in 2024 as shown in 1.2.

Cellular Network Technology		Theoretical Bandwidth	Practical Bandwidth
2G	GPRS	50 kbps	40 kbps
	EDGE	1 Mbps	500 kbps
3G	WCDMA	384 kbps	
	HSPA	7.2 Mbps	4.3 Mbps
	HSPA+[3]	21.6 Mbps	7.3 Mbps
4G	LTE	150 Mbps	18.6 Mbps downlink; 9 Mbps for upload
	LTE-A	1 Gbps	30 Mbps downlink; 10 Mbps for upload
	LTE-A Pro	3 Gbps	
5G		20 Gbps	

Figure 1.1 Cellular-technology generations in the world-wide market in the past decades (Al Mtawa et al., 2019)

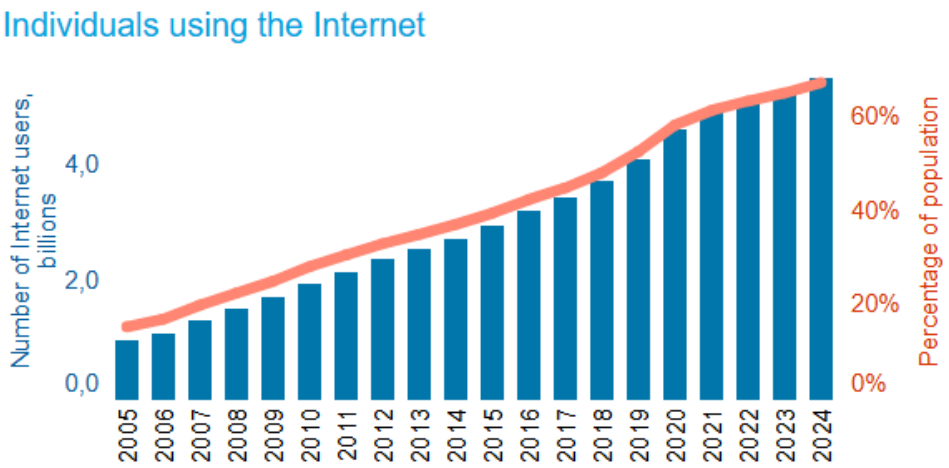

Figure 1.2 The number of people using internet in 2005-2024 (ITU, 2025)

The 4G cellular communication systems operates below 6 GHz where the frequency spectrum is excessively dense (Rappaport, Xing, Kanhere, Ju, Madanayake, Mandal, Alkhateeb & Trichopoulos, 2019). To accommodate the requirements of the aforementioned applications and to establish the necessary infrastructure for these domains, the International Telecommunication Union Radiocommunication (ITU-R) has delineated specific criteria. As illustrated in Fig. 1.3, these specifications include: peak data rates of up to 20 Gb/s; a user-experienced data rate of 100 Mb/s; a spectral efficiency threefold that of IMT-Advanced; network energy efficiency improved by a factor of 100 compared to IMT-Advanced; support for mobility speeds up to 500 km/h; nearly 1 million simultaneous connections per km^2; an area traffic capacity close to 10 $Mbit/s/m^2$; and an end-to-end latency of less than 1 ms (ITU-R-M.2083-0, 2015; Navarro-Ortiz, Romero-Diaz, Sendra, Ameigeiras, Ramos-Munoz & Lopez-Soler, 2020).

Shannon's theorem formulates the maximum achievable data rate for a given bandwidth, B, received signal power, S, noise power, N, and temperature, T as in equation (1.1) (Shannon, 1948).

$$C = B \cdot \log(1 + S/N) \quad \text{where } N = kTB \tag{1.1}$$

To enhance channel capacity, it is imperative to enlarge the bandwidth, despite the resultant rise in noise levels. Conversely, as indicated by the received signal power, P_R, formula in equation (1.2), the power decreases with increasing signal frequency, primarily due to the escalation of free space path loss (FSPL) in the transmission

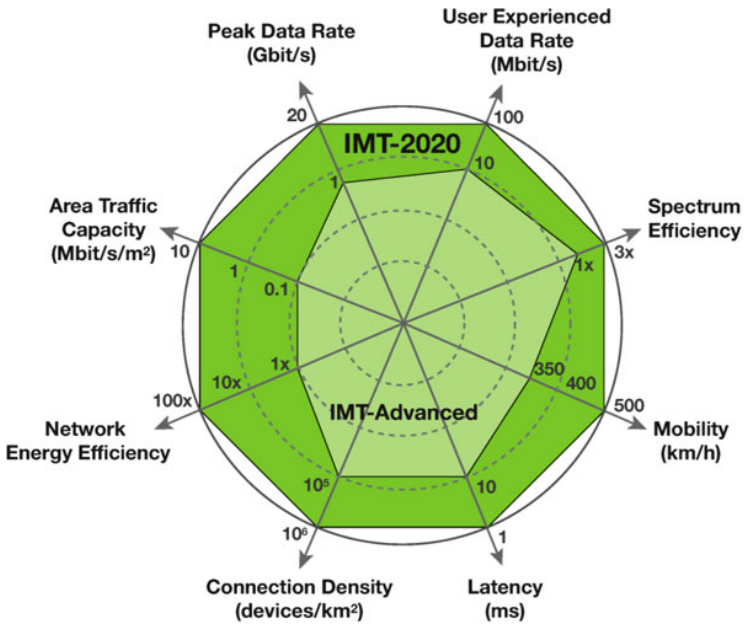

Figure 1.3 IMT-2020 specifications (ITU-R-M.2083-0, 2015)

medium.

$$P_R[dB] = P_T[dB] + G_T[dB] + G_R[dB] - FSPL[dB] \quad (1.2)$$
$$where\ FSPL = \left(\frac{4\pi df}{c}\right)^2$$

P_T, G_T, G_R, c, and d are the transmitted signal power, transmitter antenna gain, receiver antenna gain, speed of light, and communication distance, respectively (Balanis, 2016). Thus, when leveraging millimeter waves (mm-waves) to exploit larger bandwidths, one must address the associated rise in attenuation. Strategies such as beamforming and the employment of multiple-input-multiple-output (MIMO), and phased arrays are essential to counteract this heightened attenuation.

1.1 Satellite Communication Systems

Another key aspect in communication systems is the covered area by these systems. Only 6% percent of global coverage is provided by terrestrial communication systems (You, Zhu, Qiang, Tsinos, Wang, Gao & Ottersten, 2024). Terrestrial networks fall

short in global coverage since the establishment of communication in environmentally challenging locations such as poles and ocean is extremely hard for terrestrial communication systems. On the other hand, satellite communication (SATCOM) systems offer longer communication distance which enables broader coverage compared to terrestrial networks. The effect of geographical conditions on the communication links in SATCOM is less than terrestrial networks. Moreover, satellite systems has and advantage to support communication links when the communication terminals or targets moves with high speed (You et al., 2024).

Satellites have long been employed to establish communication links between various locations on Earth. SATCOM facilitates global connectivity, particularly in remote and under-served regions. One of its primary application domains is telecommunications, where SATCOM enables services such as broadcast satellite television and radio, as well as internet access in rural areas. Low Earth Orbit (LEO) satellites operate at altitudes ranging from 200 to 2000 km. Due to their lower orbital altitude compared to Medium Earth Orbit (MEO) or Geostationary Earth Orbit (GEO) satellites, LEO systems experience reduced latency and path loss (You et al., 2024). SATCOM is also employed in secure communications for defense purposes, as well as in remote monitoring and navigation systems.

Notable LEO satellite constellations designed for telecommunications include TeleSat, Amazon Kuiper, Starlink, and OneWeb. Among these, OneWeb and Starlink utilize carrier frequencies of 12 GHz and 14 GHz for downlink and uplink, respectively, while Amazon Kuiper employs 20 GHz for downlink and 29 GHz for uplink (Lin, Cioni, Charbit, Chuberre, Hellsten & Boutillon, 2021). In addition, other frequency bands such as C-band (4–8 GHz), X-band (8–12 GHz), and Ku-band (12–18 GHz) are commonly used for applications including continuous satellite television broadcasting, weather monitoring, and air traffic control.

Electronically scanned phased arrays are generally more suitable for SATCOM applications than mechanically steered systems, as they enable low-latency communication with a compact and lightweight form factor. Another key advantage of phased arrays is their wide bandwidth, which allows coverage across the C-, X-, Ku-, and Ka-bands employed in SATCOM systems. Previously reported wideband integrated circuits (ICs), such as those in (Hu, Kazan & Rebeiz, 2023; Mondal, Singh, Hussein & Paramesh, 2018), have played a critical role in enabling these systems. Fig. 1.4 illustrates a LEO satellite system employing massive MIMO (You et al., 2024).

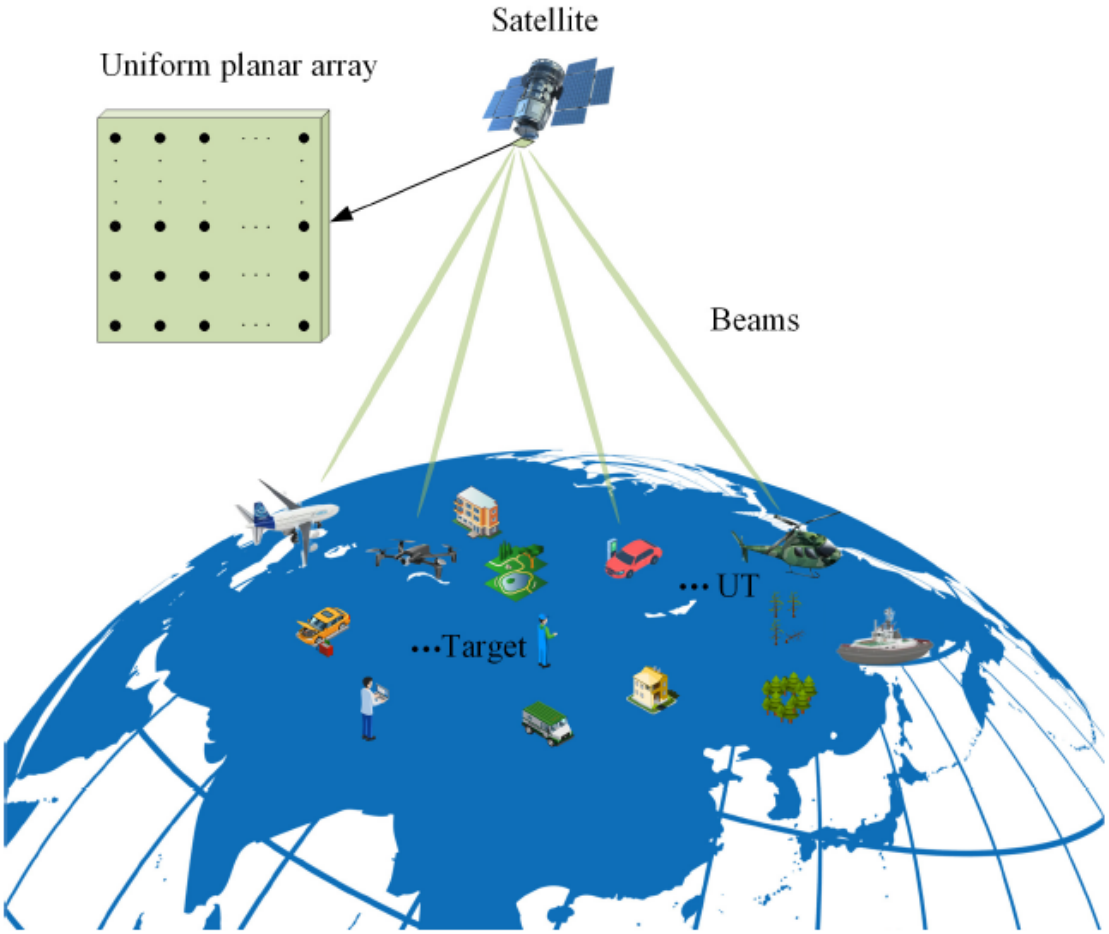

Figure 1.4 A LEO satellite system with a massive MIMO (You et al., 2024)

1.2 SiGe BiCMOS Technology

IC designs are predominantly based on three major technology platforms: III-V technologies (such as gallium arsenide (GaAs) and indium phosphide (InP)), CMOS technologies, and SiGe BiCMOS technology. III-V technologies offer distinct advantages over the others in terms of higher gain, lower noise figure (NF), and increased output power—parameters that are crucial for RF IC front-ends. For example, GaAs and GaN devices are employed in current E-band transceivers due to their ability to deliver the high output power and linearity required for mobile backhaul systems targeting ranges exceeding 2 km (Preez, Sinha & Sengupta, 2023). Despite their superior performance, III-V technologies suffer from higher defect densities and a greater susceptibility to physical damage, which complicates the fabrication process. Additionally, they are characterized by low yield rates (Cressler & Niu, 2003). These challenges significantly escalate production costs. Consequently, their high cost limits their applicability in industries that demand large-scale manufac-

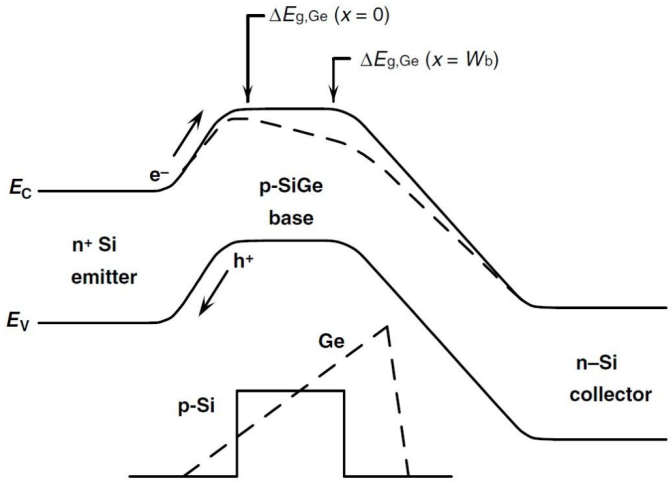

Figure 1.5 The representation of the energy band diagram of SiGe HBT (top) and Si BJT (bottom) (Cressler, 2007)

turing. Furthermore, integration of III-V technologies with other platforms is not feasible, necessitating the design of each sub-block on separate ICs to achieve adequate system-level performance. Nevertheless, their high output power makes them suitable for high-power applications, such as base stations.

Si is one of the most abundant elements on Earth. The ability to produce defect-free, large-diameter Si wafers contributes to a higher number of ICs per wafer. Owing to these attributes, CMOS technologies offer the lowest cost among the available semiconductor technologies (Cressler & Niu, 2003). In recent years, significant advancements in CMOS technologies—particularly in RF performance metrics such as f_T, f_{max}, and NF_{min}—coupled with improvements in digital circuitry, including digital signal processing and data converters, have enabled the development of System-on-Chip (SoC) solutions based on single-chip architectures for complex transceivers (Preez et al., 2023). However, these technologies are subject to considerable process variations. Specifically, MOS devices are well known for their modeling challenges (Preez et al., 2023). Variations in parasitic capacitance and resistance can alter circuit performance, thereby introducing reliability concerns for these technologies.

SiGe BiCMOS technology emerged as an enhancement to Si-based technologies through the application of bandgap engineering. In this process, a SiGe alloy is grown epitaxially. The bandgap energies of Si and Ge are 1.12 eV and 0.66 eV, respectively. Increasing the Ge content leads to a reduction in the bandgap energy of the alloy. A smaller bandgap enhances electron injection efficiency within the device, thereby resulting in a higher current gain, denoted as Beta. Furthermore, the Ge composition is introduced in a graded profile, as illustrated in Fig. 1.5, rather than being kept constant. This graded profile creates a built-in electric field

that accelerates minority carriers in the base region, effectively reducing their base transit time, τ_b.

Although forming a graded SiGe alloy in the base region increases fabrication complexity and cost, the overall manufacturing expense remains significantly lower than that of III-V technologies. Unlike III-V technologies, SiGe processes are not hindered by low yield, and they exhibit greater resilience to process variations than CMOS technologies. The performance characteristics of SiGe technology rival those of III-V technologies. The impact of these enhancements on a pure Si wafer is reflected in performance metrics such as f_T, f_{max}, and NF_{min}. The parameters f_T and f_{max} are critical figures of merit that define the frequency limits of an electronic device. Specifically, f_T denotes the frequency at which the short-circuit current gain drops to unity. The expression for f_T is provided in equation (1.3), where τ_b and τ_c represent the base and collector transit times, g_m is the transconductance of the device, C_π and C_μ are the base-emitter and base-collector capacitances, respectively, and r_e and r_c denote the emitter and collector resistances (Cressler, 2007). While f_T can be adjusted during the design phase—since g_m and the capacitances are dependent on biasing conditions and device dimensions—the transit times are inherently determined by the fabrication process. The reduced base transit time resulting from graded Ge doping directly contributes to an increase in f_T, as indicated by equation (1.3).

$$f_T = \frac{1}{2\pi}\left(\tau_b + \tau_c + \frac{1}{g_m}\left(C_\pi + C_\mu\right) + \left(r_e + r_c\right)C_\mu\right)^{-1} \tag{1.3}$$

The other critical frequency parameter, f_{max}, represents the maximum oscillation frequency. Its formulation is given in equation (1.4), where r_b denotes the intrinsic base resistance. An enhancement in f_T directly contributes to an increase in f_{max}, as the two are proportionally related. By adjusting the Ge grading profile within the base region, higher doping concentrations can be achieved. This modification leads to a reduction in the intrinsic base resistance, thereby enabling higher values of f_{max} without compromising current gain.

Conversely, in conventional Si BJTs, reducing the intrinsic base resistance can also be achieved by increasing the doping concentration in the base region. However, this approach comes at the cost of diminished current gain. Therefore, SiGe technology offers a favorable trade-off by enabling lower base resistance while preserving performance metrics critical to high-frequency operation.

$$f_{max} = \sqrt{\frac{f_T}{8\pi C_\mu r_b}} \tag{1.4}$$

The last of the previously mentioned figures of merit is the minimum achievable noise figure, NF_{min}. Its analytical expression is provided in equation (1.5), where β_{DC} denotes the DC current gain, J_c is the collector current density, and n represents the emitter-base junction ideality factor. Similar to the case of f_T, the designer retains a degree of control over NF_{min} by adjusting parameters such as J_c and β_{DC}. However, intrinsic resistances and the threshold voltage are determined by the fabrication process and are therefore beyond the designer's control.

A key advantage of SiGe HBTs over conventional Si BJTs is the ability to reduce the intrinsic base resistance, r_b, without degrading the current gain. This reduction leads to an improvement in NF_{min}. Moreover, it is generally observed that an increase in f_T contributes to a corresponding decrease in NF_{min}.

$$NF_{min} = 1 + \frac{n}{\beta_{DC}} + \sqrt{\frac{2J_c}{V_t}(r_e + r_b)\left(\frac{f^2}{f_t^2} + \frac{1}{\beta_{DC}}\right) + \frac{n^2}{\beta_{DC}}} \tag{1.5}$$

Table 1.1 Performance comparison of numerous device technologies for radio frequency integrated circuits (Preez et al., 2023)

Technology	IC Cost	Integration	RF Performance	Target products
GaAs pHEMT / mHEMT	High RF modules; requires multi-chip approach	Poor	Excellent, preferred for many RF applications	PA, LNA, complete RF modules
GaN HEMT	Relatively new technology	Poor	Higher P_{sat} but worse linearity vs. GaAs	Future PA, LNA
InP pHEMT	Generally more than GaAs competitors	Poor, RF circuits are highly complex	Better f_T, f_{max} versus GaAs	Defense systems
SiGe	Lower, function of production volume, comparable cost for small-volume production	Good, but not suited for A/D and baseband integration within SoCs	High f_T, f_{max}, decent phase noise performance & low-loss BEOL[3] layer stackup	Medium to high-power mm-wave transceivers ICs
SiGe BiCMOS	Lower than competitors, but depending on production volume; SoCs result in good yield	Excellent integration with wide range of logic, good power consumption for A/D and D/A converters	High f_T, f_{max}, decent phase noise performance & low-loss BEOL layer stackup	Medium to high-power mm-wave transceivers, can readily integrate with PLLs and A/D converters
RF CMOS	Mm-wave expansion of digital CMOS, requires advanced lithography and costly NRE	Facilitates high-density digital circuitry integrated with RF; SoC integration possible with digital baseband and memory blocks	Transistor f_T, f_{max} can reach mm-wave operation, but requires low breakdown voltages and miniaturized nodes	Transceivers with A/D, PLL, amplifier blocks with digital control, well-suited for lower-performance applications
CMOS FDSOI	Lowest supply voltage and power consumption	Can integrate with high-density mixed-signal SoCs, relatively low power requirement for crossing chip boundaries	Substrate engineering can substantially improve RF performance; high f_T, f_{max}, good isolation and linearity	Very high-speed mixed-signal blocks (e.g., SerDes)

A relative performance comparison of various IC technologies is provided in Table 1.1. In summary, III-V technologies demonstrate superior performance characteristics compared to other platforms; however, their high fabrication costs and

low yield rates constrain their use to application-specific designs, such as power amplifiers requiring high output power or low-noise amplifiers (LNAs) demanding extremely low NF. Despite significant advancements in CMOS technology, process variability remains a fundamental limitation. Moreover, operating at large level of V_{DS} might lead to a degradation in threshold voltage and transconductance. SiGe HBTs, by contrast, offer higher transconductance, improved 1/f noise characteristics, and greater output power, along with slightly enhanced efficiency relative to MOS devices. RF IC front-ends implemented in SiGe BiCMOS technology present a cost-effective and highly integrable solution, while delivering performance metrics that are comparable to those achieved with III-V technologies.

1.2.0.1 IHP 0.13 μm SiGe BiCMOS (SG13S) Tehcnology

In this thesis work, IHP Microelectronics 0.13 μm SG13S technology process was preferred. It is reported that IHP's 0.13 μm SiGe BiCMOS technology provides HBTs with f_t/f_{max} of 250/340 GHz and BV_{CEO} of 1.7 V. The cross-section of the SG13S process is illustrated in Fig. 1.6. The process consists of five thin (M1-M5) and two thick metal (TM1-TM2) layers. The thick metal layers are located at the top. TM1 and TM2 are generally used to implement high quality-factor inductors and low loss transmission lines. The metal-insulator-metal (MIM) capacitor resides between TM1 and M5. The process offers three different polysilicon resistors (rsil, rppd and rhigh).

1.3 Thesis Overview

This thesis aims to design and implement a radio frequency (RF) receiver for SATCOM applications. Increasing the bandwidth is one of the key enablers to achieve higher data rates. In mm-wave, a larger bandwidth can be allocated. Since LEO SATCOM systems are promising for global connectivity and internet coverage, these SATCOM applications have gathered attention recently. Currently licensed frequency bands for SATCOM reception are C-, X-, Ku-, and Ka-bands. A wideband receiver RF module that covers these SATCOM bands would be cost-efficient. On the other hand, due to orbiting around Earth at more than 200 km altitudes and uti-

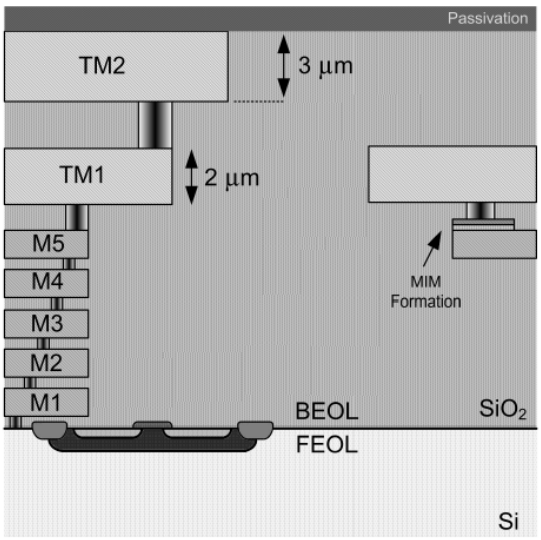

Figure 1.6 The cross-section of IHP's 0.13 μm SiGe BiCMOS SG13S technology (Özkan, 2020)

lizing mm-wave, the atmospheric path loss is increased. To compensate for increased path loss, one can employ MIMO arrays. In this thesis, two separate single-channel receiver-ICs for SATCOM applications are presented.

The first receiver consists of an LNA and a 6-bit phase shifter. The designed LNA comprises three stages. The first two stages are single-ended, while the third stage is differential since a passive balun is placed between the second and third stages. Each stage in the designed LNA employs a series RL-loaded cascode topology, which enables flat gain across a wide bandwidth. The last stage of the LNA employs a post-distortion method to enhance IIP3 linearity performance. The phase shifter is based on a passive vector-sum phase shifter topology to achieve high linearity. Analog-controlled voltage variable attenuators with a closed-loop for attenuation control are utilized in weighting the quadrature signals. A wideband Wilkinson power divider is finalized by summing the weighted vectors. In the second receiver, the phase shifter adopts a differential hybrid coupler and 1^{st}-order polyphase filter to enlarge the bandwidth. Also, an RC attenuation compensation network is utilized in the attenuators to reduce amplitude errors in the high attenuation states. The control of the attenuators is switched to digital inputs by employing a 22-bit serial-to-peripheral interface, level shifters, and two 10-bit DACs. Finally, a distributed amplifier-based VGA is introduced in the second receiver as the last stage. The VGA employs RC-feedback to widen the frequency range. The system level schematic simulations of the receiver is presented by connecting the LNA, phase shifter-attenuator, and VGA in that order in ADS environment.

1.4 Thesis Organization

The rest of this thesis is organized as follows: Chapter 2 provides fundamental information about phased arrays. Amplitude and phase control blocks in phased arrays are briefly explained with various topologies. The working principle and design vector-sum phase shifter topology are analyzed with the inductance equations. The chapter is followed by a presentation of the current state-of-the-art in wideband receiver ICs.

Chapter 3 contains the analysis, design, simulation and measurements of both wideband receivers for SATCOM applications. This chapter begins with the design procedure of each sub-block; the LNA and phase shifter. After the design procedure, the measurement results are provided for each sub-block. The first receiver, the combination of the LNA and phase shifter, is presented and the measurement results are shown as well. Also, Chapter 3 also covers the design revisions in the LNA and phase shifter in the second receiver, and simulations of each sub-block in the second receiver. Finally, chapter 3 will is concluded with the system level simulations of the second receiver.

The last chapter of this dissertation will summarize the findings and the impacts of the presented works. Moreover, this chapter also opens up a discussion on the limitations and possible solutions to these limitations. A list of future work finalizes the thesis.

2. BACKGROUND

2.1 Phased Arrays

A single antenna element operates with a low-directivity characteristic, resulting in omnidirectional radiation with a wide beam. Low directivity leads to lower antenna gain, which affects the link budget. Considering the increased path loss in mm-wave frequencies, high directivity should be required. When multiple antenna elements are arranged in an array configuration, the overall radiation pattern becomes significantly more directive, leading to a narrower main beam. By appropriately controlling the phase of each radiating element—such as by applying a constant phase taper between adjacent elements—the main beam can be electronically steered away from the broadside (normal) direction.

2.1.1 Operating Principle

Phased arrays have been employed across various domains, including medical applications (Bucci, Crocco, Scapaticci & Bellizzi, 2016) and automotive radars (Ku, Schmalenberg, Inac, Gurbuz, Lee, Shiozaki & Rebeiz, 2014). By utilizing multiple antenna elements, both the transmitter and receiver antenna gain can be enhanced. Consequently, the attenuation associated with mm-wave usage can be counterbalanced, enabling the establishment of extended communication links.

Fig. 2.1 separately illustrates phased array systems in both transmission and reception. The signal intended for transmission, denoted as $S(t)$, is expressed in Eq.(2.1), where $v(t)$ and $\phi(t)$ symbolize the baseband signal modulating the carrier signal.

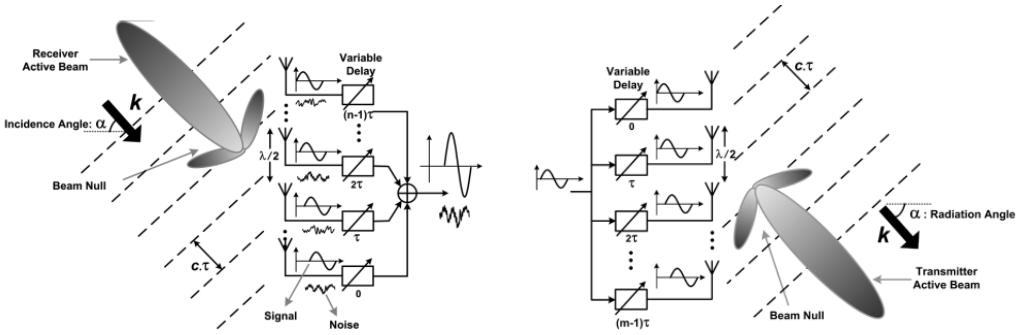

Figure 2.1 The operating principle of phased array in reception (left) in transmission (right) (Hajimiri, Hashemi, Natarajan, Guan & Komijani, 2005)

Here, τ represents the time delay between successive elements (Natarajan, Komijani & Hajimiri, 2005). Under the narrow-band approximation, it's posited that phase shifts can substitute for time delays. This leads to more compact designs since time delay circuits occupy more area.

$$S(t) = \sum_{n=0}^{n-1} v(t - k\tau) cos\Big(\omega_{RF} t + \phi(t - k\tau)\Big) \tag{2.1}$$

As equation (2.1) indicates the beam direction or angle is controlled by the phase of each element. The incremental phase shift between each element in an array along with the distance between the elements determines the angle between the main beam and the elements. To obtain the highest possible directivity, the distance between radiating antenna elements should be $\lambda/2$.

2.1.2 Phased Array Architectures

Phased arrays have been classified as active and passive depending on whether each element has its own RF chain or not. In passive phased arrays, each element has only its phase shifter as shown in Fig. 2.2a. The transmitter and receiver utilize separate central amplifiers. Due to losses in the feed network and phase shifter, the central amplifier in the transmitter must provide very high output power, and the central amplifier in the transmitter must perform high gain while introducing very low noise. Most of the passive phased arrays do not offer amplitude control (Parker & Zimmermann, 2002). Active phased arrays contain an RF chain for each antenna element. The RF chain includes an LNA, a PA, a phase shifter, RF switches, and a

variable gain amplifier (VGA)/attenuator. An example of a transmit/receive (T/R) module is presented in Fig. 2.2b.

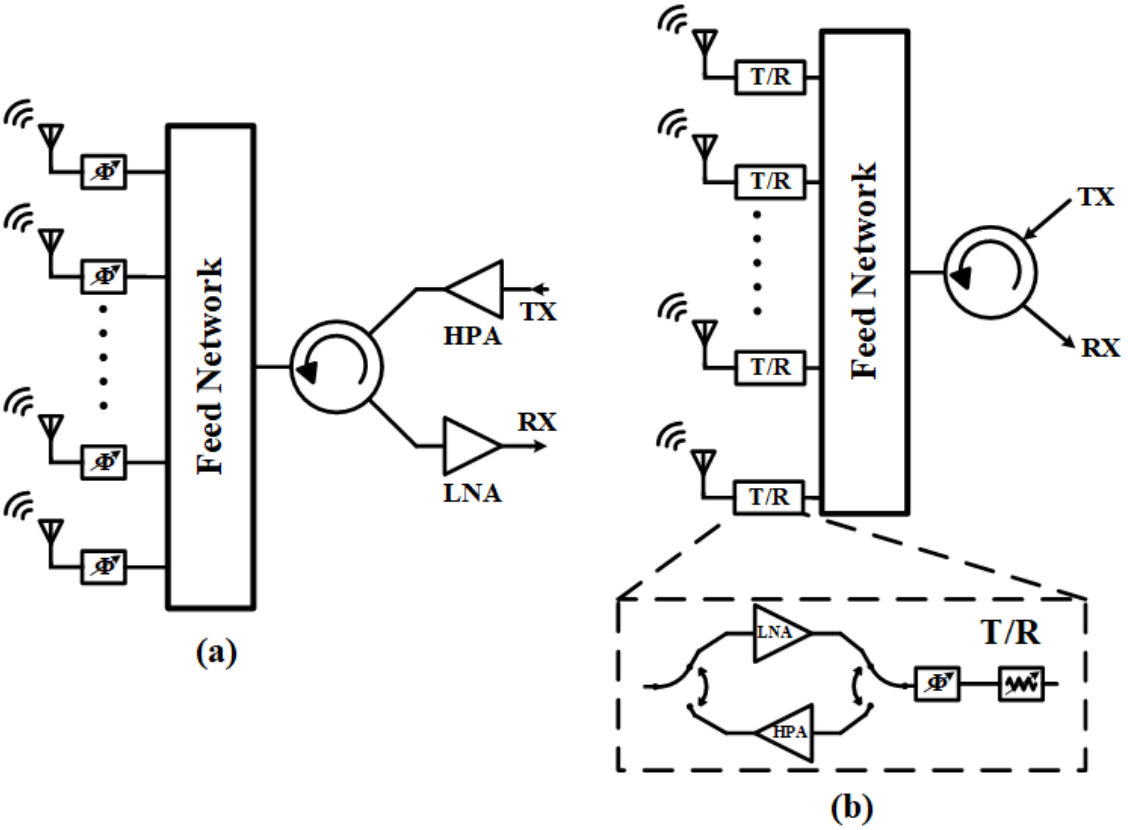

Figure 2.2 (a) Passive and (b) active phased array architectures

The main advantage of passive phased arrays is very low power consumption compared to active phased arrays since there are only central amplifiers. Architectural simplicity makes passive phased arrays less expensive. On the other hand, active phased arrays offer better performance in terms of high gain and output power, lower NF. Due to element-wise amplitude and phase control in active phased arrays, beam steering is more precise. Another advantage of active phased arrays is the scalability. We can increase the number of antenna element since each element has its own RF chain. However, passive phased arrays suffer from increased losses introduced by the feed network as the number of element increased.

Controlling the phase and amplitude of each element for the beam direction or angle is referred as beamforming. Phased arrays are also classified with respect to their beamforming methodology. The beamforming in phased arrays is divided into analog or digital depending on where the phase and amplitude of an element is controlled. In the digital beamformers, the phase shift is determined at the baseband whereas the analog beamformers gives phase shift in the transmitter/receiver (transceiver) part as shown in Fig. 2.3. In digital beamforming, each transceiver element has its

own mixer and Analog-to-Digital converters (ADCs). Since the signal combining comes after ADCs, the ADCs must have high linearity (Kalyoncu, 2019). The high linearity requirement increases the power consumption dramatically. On the other hand, more precise control over phase and amplitude can be achieved at the baseband compared to in the RF path (Yang, Yu, Lan, Zhang, Zhou & Hong, 2018; Zhang, Wu & Fang, 2011). Analog beamformers offer lower power consumption by leveraging the employment of one ADC after signal combining. Moreover, the phase shifter in RF domain brings either high loss or low linearity performance depending on the phase shifter topology. Analog beamformers do not support multiple beams so, the number of users are limited. Unlike analog beamformers, digital beamformers can support multiple beams at a time. As a result, digital beamformers can support any number of user terminal, only limited by the number of elements in array. A third beamforming option exists as the hybrid beamforming which combines narrow beams shape of analog beamforming for longer distance with simplicity in design and performance of digital beamforming (Li, Wang, Li, Liu & Zhou, 2019; Maneiro-Catoira, Brégains, García-Naya & Castedo, 2018; Roth, Pirzadeh, Swindlehurst & Nossek, 2018).

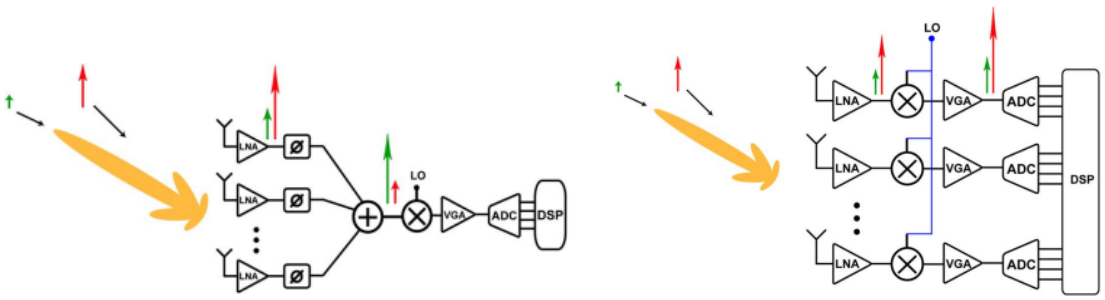

Figure 2.3 Beamformers, analog beamformer (left) digital beamformer (right) (Puglielli, Townley, LaCaille, Milovanović, Lu, Trotskovsky, Whitcombe, Narevsky, Wright, Courtade, Alon, Nikolić & Niknejad, 2016)

There are several phase shifting methods in beamformers as shown in Fig. 2.4. LO phase shifting is a phase shifting that the phase shifting occurs in LO path. In RF and IF phase shifting, the phase shifting is performed before and after the downconversion in a receiver chain, respectively. In digital phase shifting, digital signal processing or ADC/DAC are responsible for phase shifting on digital I/Q samples. Among the phase shifting methods, contemporary phased arrays have been employed RF phase shifting since single mixer employed in RF phase shifting removes complex LO feed networks and degradation due to these feed networks (Kalyoncu, 2019).

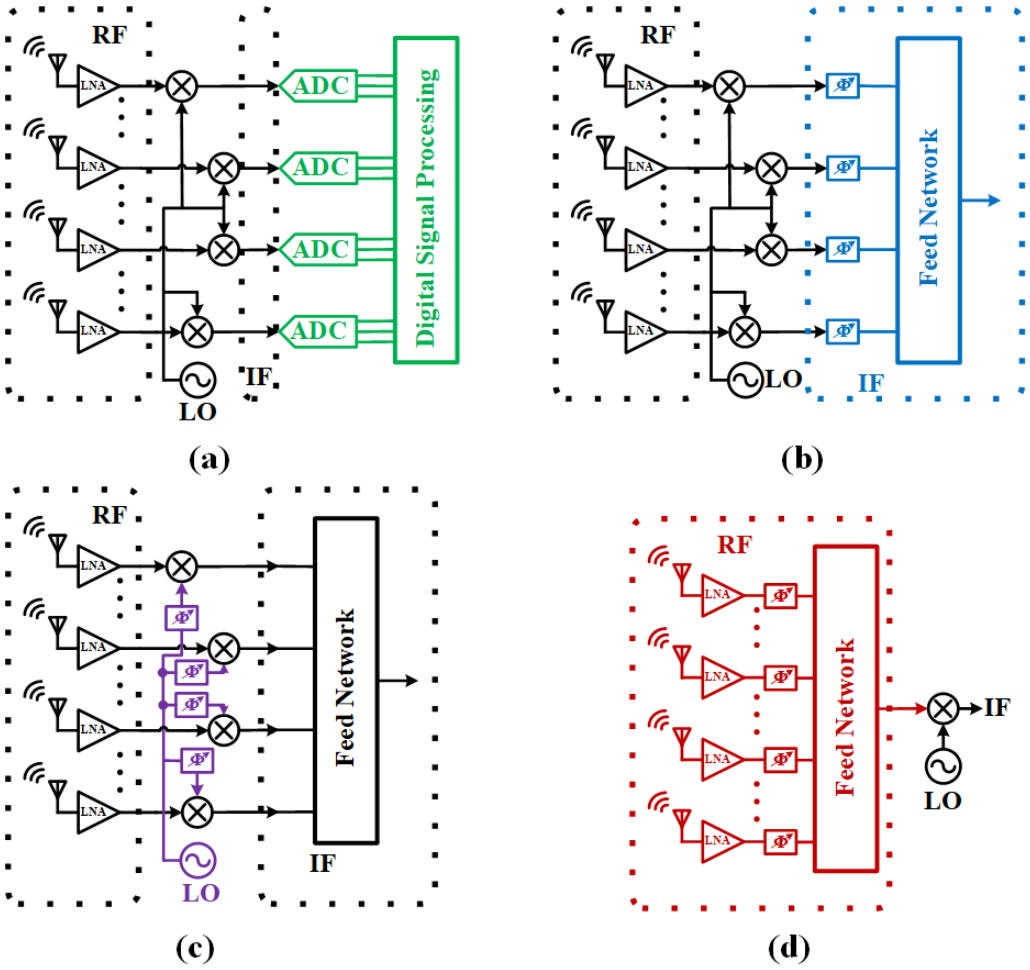

Figure 2.4 RF phase shifting methods (a) digital, (b) IF, (c) LO, and (d) RF

2.2 Phase and Amplitude Control Blocks

Beamforming has been a focal point of research over the years, especially given its significant role in fulfilling the high standards of 5G applications. As underscored by equation 2.1, the precise control of phase and amplitude is essential for the constructive combination of incoming signals and for steering the beam direction. Furthermore, the suppression of the side-lobe level (SLL) is intricately linked to phase resolutions. Figure 2.5 elucidates that with increased phase resolution, there is a concomitant decrease in SLL. Another critical insight derived from Fig. 2.5 is the inverse relationship between phase resolution and the required number of antennas for achieving a target SLL. A finer phase resolution implies fewer necessary antennas, consequently leading to reductions in system size and cost (Mailloux, 2017). Along with the phase resolution, the resolution of the amplitude control should be high to adjust the SLL and null points in the beamforming (Roques, Cazaux & Pouysegur,

1990; Walker, 1994). Therefore, amplitude and phase control blocks are crucial for beamforming.

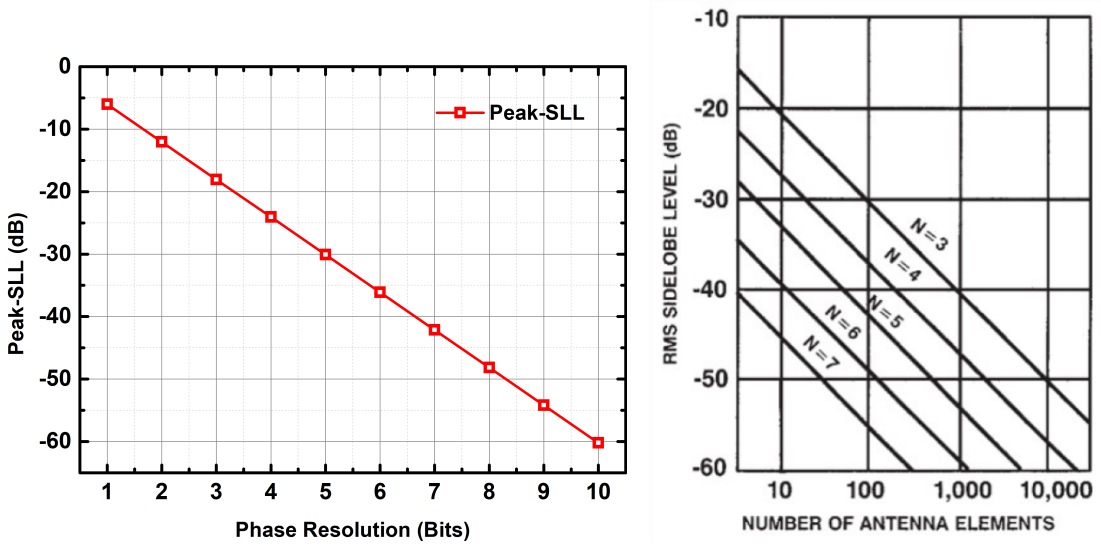

Figure 2.5 Peak SLL due to N bits of quantization with respect to the number of phase control bits (left) and required antenna number to reach the same RMS side-lobe level with different phase resolutions (right) (Mailloux, 2017)

2.2.1 Attenuators and VGAs

VGAs and attenuators are employed in transceivers for amplitude control purposes. The main objective of these amplitude control blocks is to adjust the signal's power level by introducing the same phase shift. However, the amplitude control blocks insert different phase shifts across different amplitude levels due to parasitic effects in the transistors and layouts. Similarly, the amplitude levels vary with the frequency. Root mean square (RMS) amplitude and phase errors are parameters of an amplitude control block utilized to show error performance. RMS amplitude and phase error formulas are given in (2.2) and (2.3), respectively.

$$RMS-Amplitude\ Error(f)=\sqrt{\frac{1}{N}\sum_{n=1}^{N}\left(\Delta\Phi_n(f)\right)^2} \tag{2.2}$$

$$RMS-Phase\ Error(f)=\sqrt{\frac{1}{N}\sum_{n=1}^{N}\left(\Delta\epsilon_n(f)\right)^2} \tag{2.3}$$

VGAs can provide gain to compensate the losses of other blocks in the transmitter or receiver chain. The cost of gain that VGA brings is the deterioration in linearity. On the other hand, attenuators, often being passive structures, inherently possess a higher power handling capability. A noteworthy advantage of attenuators is their zero DC power consumption, which can significantly relax the other sub-blocks specifications. Furthermore, attenuators can operate over expansive bandwidths, often exceeding 10 GHz (Kandis, Burak, Kana, Yazici & Gurbuz, 2022; Ku & Hong, 2010; Song, Cho & Cressler, 2018). The attenuation range of attenuators is larger than VGAs since the large phase variation in low gain settings occurs in VGAs.

Attenuators can be classified as digital or analog controlled attenuators. The former is commonly realized using switched-Π/T type resistive networks, as depicted in Fig. 2.6 (Kandis et al., 2022; Ku & Hong, 2010; Song et al., 2018; Yuan, Mu & Guo, 2018). One significant advantage of digitally-controlled attenuators is their independence from ADCs for operation.

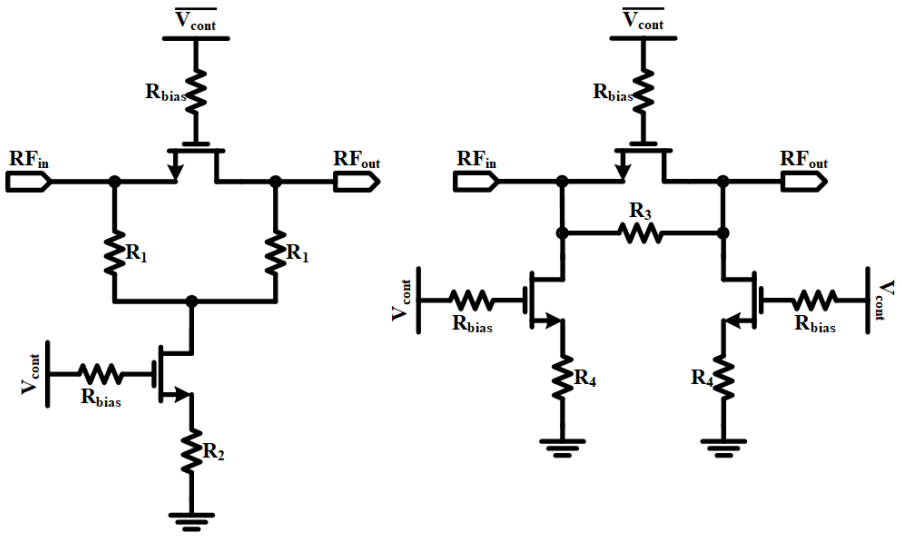

Figure 2.6 Attenuator networks

The operation principle of digital-step attenuator is the selection between reference path and lossy path. When Q1 is ON and Q2 is OFF in Fig. 2.6, Q1 provides a direct connection between RF_{in} and RF_{out}, constituting the reference path. Conversely, when Q2 is ON and Q1 is OFF, the T-type resistive network occurs between RF_{in} and RF_{out}, delineating the lossy path.

The bandwidth of these attenuators is largely dependent on the parasitic capacitance of the OFF-state switches. Concurrently, the loss experienced in the reference path, commonly termed insertion loss (IL), hinges on the R_{ON} resistance of the series switch. In large attenuation networks, the phase variation becomes significant. To counteract this, R-L-R low pass network is employed as in (Kandis et al., 2022).

To increase attenuation range, the number of utilized networks should be increased which causes higher IL and larger area. The study presented in (Kandis et al., 2022) details a 6-bit, 24 dB digital step attenuator designed using 130nm SiGe BiCMOS technology. It operates over a frequency range from DC to 25 GHz, and the input 1-dB compression point (IP_{1dB}) for this attenuator exceeds 20 dBm. The RMS phase error is 2.4°. Nevertheless, it exhibits an insertion loss greater than 9 dB, and its overall area measures 1.1 mm^2. Another digital step attenuator reported in (Yuan et al., 2018) has 31.5 dB attenuation range and 0.5 dB resolution. This work introduces two separate attenuators tailored for specific frequency bands: one covering the 15-18 GHz range and the other spanning 19-24 GHz. Combined, these attenuators occupy a total area of 1.07 mm^2.

In prevalent analog-controlled attenuators, the resistance elements within the resistive Π/T-type networks are supplanted with NMOS devices. This design allows for control over attenuation by modulating the gate voltage, which in turn adjusts the channel resistance of the NMOS devices, as expressed in equation (2.4) (Dogan, Meyer & Niknejad, 2004,0). A distinct advantage of analog-controlled attenuators is their compactness, stemming from a compact design featuring merely three transistors. This simplicity also facilitates a straightforward design methodology. However, a notable drawback is their dependency on ADCs for system integration, a requirement not present in digital-step attenuators.

$$R_{channel} = \frac{1}{\mu_{n,p} C_{ox} \frac{W}{L} \left(V_{|GS|} - V_T \right)} \tag{2.4}$$

(Dogan et al., 2005) reported a voltage variable attenuator (VVA) which has 42 dB attenuation range and 0.9-3.5 dB insertion loss. Fig. 2.7 demonstrates the schematics of conventional VVAs. $IP1_{dB}$ of this VVA is measured at 2.5 dBm while occupying 0.7 mm^2. The operation frequency is DC-2.5 GHz. A VVA operates DC to 10 GHz (Dogan et al., 2004). The insertion loss is 0.8-3 dB and the attenuation range is 35 dB. $IP1_{dB}$ is measured at 5 dBm while occupying 0.29 mm^2. Another VVA is presented in (Wagner, Mayer, Wickert, Wolf, Joram, Strobel & Ellinger, 2013) with different topology. In this topology, input and output are differential signals. By adjusting channel resistances of the series and shunt devices, the attenuation is controlled. The purpose of the series devices is as the same as in Π/T-type networks whereas shunt devices determine the controlled leakage between the differential signals. The work in (Wagner et al., 2013) reported 3.6 dB insertion loss and 51.7 dB maximum attenuation. The phase variation is measured as 4°. The

total area is 0.7 mm^2. However, this topology requires one balun at each input and output port to convert differential to single-ended for single-ended designs.

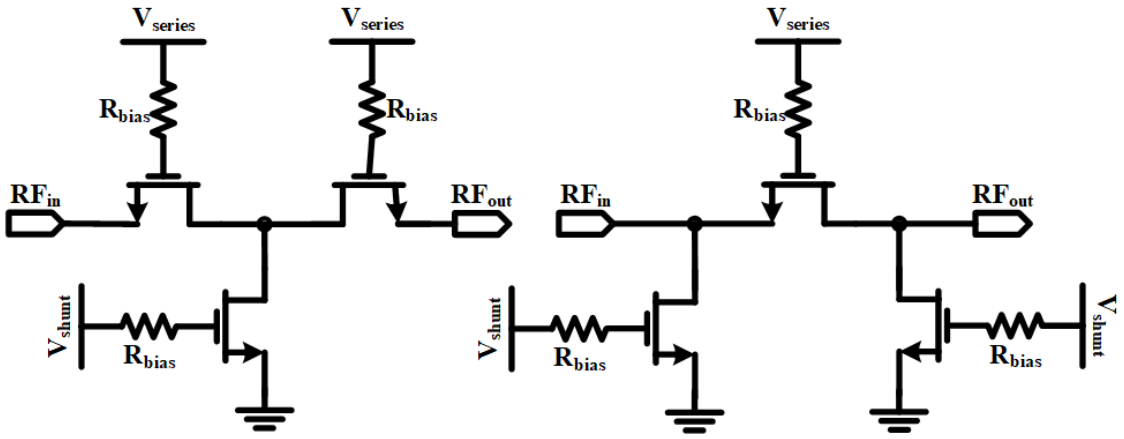

Figure 2.7 The schematics of conventional VVAs

2.2.2 Phase Shifters

Phase control in communication systems typically relies on two primary components: true-time delay (TTD) circuits and phase shifters. TTDs are particularly suited for wideband systems as they avoid the beam-squint phenomenon (Ma, Leenaerts & Baltus, 2015). However, these circuits come with inherent drawbacks: they consume substantial area and introduce significant losses in the RF path. Due to these drawbacks, phase shifters often emerge as the more favorable choice over TTDs in many applications.

The main objective of these phase control blocks is to adjust the signal's inserted phase by the circuit without affecting the amplitude level of the input signal. However, the phase control blocks lead to variations in the signal's power across different phase states. Similarly, the inserted phases vary with the frequency. Similar to the amplitude control blocks, RMS amplitude and phase errors are parameters of a phase control block utilized to show error performance. RMS amplitude and phase error formulas are given in (2.2) and (2.3), respectively.

Phase shifters are classified into two categories in terms of DC power consumption: passive or active phase shifters. Former leveraging zero power consumption. Due to being passive structures, passive phase shifters have the capability to handle high powers. However, they introduce high loss and occupy large area which increases the cost of the system. Similar to digital step attenuators, higher phase resolution

requires additional networks which increase overall area.

In the literature, several passive phase shifter works have been reported (Basaligheh, Saffari, Rasti Boroujeni, Filanovsky & Moez, 2020; Calışkan, Yazici & Gurbuz, 2021; Garg & Natarajan, 2017; Gong, Cho & Cressler, 2017; Gul, Duong, Kim & Lee, 2013). The schematics of some passive phase shifter topologies are illustrated in Fig. 2.8. (Gul et al., 2013) employs switch-line topology which the phase shift depends on the length difference between the reference line and longer line. In this work, 2-bit switch-line phase shifter with the minimum insertion loss of 8.2 dB is presented between 57-64 GHz in 130 nm CMOS technology. Another passive phase shifter topology is switched-filter type which replaces transmission line in switch-line topology with the high-pass and low-pass filters. The phase shifter design in (Calışkan et al., 2021), implemented in 130 nm SiGe BiCMOS technology, integrated with an all-pass network, spans frequencies from 6-25 GHz and occupies 0.48 mm^2. However, this design suffers a considerable loss of 20.4 dB. To mitigate this pronounced loss, (Gong et al., 2017) replaced the switches with active switches and obtained 11.5 dB gain, albeit at the expense of heightened power consumption of 195 mW. This phase shifter is also realized in 130 nm SiGe BiCMOS technology. In reflection-type passive phase shifters, phase modulation is achieved by modulating the load impedances of the coupler, as detailed in (Basaligheh et al., 2020; Garg & Natarajan, 2017) which are implemented in 65 nm CMOS.

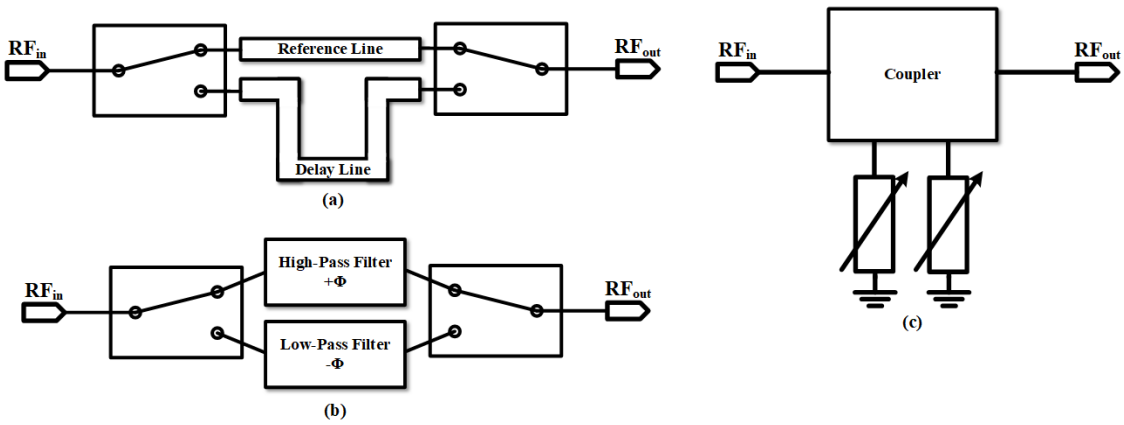

Figure 2.8 The schematics of passive phase shifters: Switched-line (a), Switched-filter (b) and Reflection-type (c) phase shifters

Active phase shifters provide the benefit of high phase resolution while also offering gain, thereby easing the performance requirements of other subsystems in terms of gain, noise etc. Moreover, they can be realized in a compact area. The vector-sum phase shifter topology is predominantly favored for active phase shifters. As depicted in Fig. 2.9, firstly, the single-ended input is converted to differential signals which are fed to I/Q generation network. I/Q network generates four different signals

that are 90° apart from each other. In the final stage, the two of these signals are combined with different weights controlled by the VGAs to obtain desired phase shift. Since the VGAs are analog-controlled, additional control circuit is required.

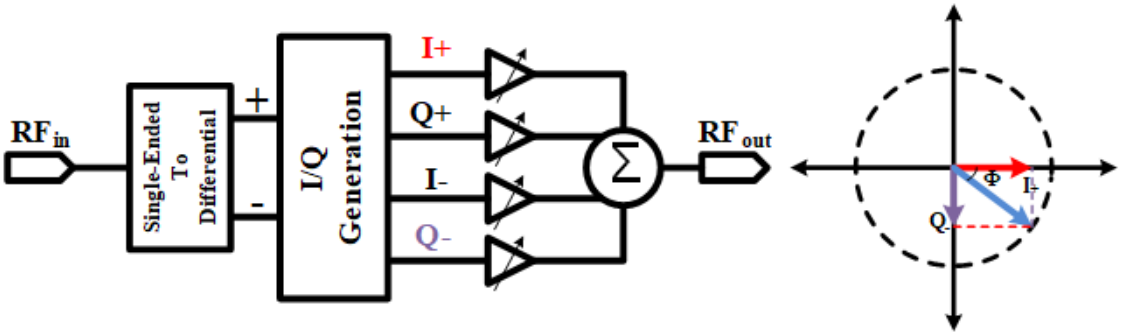

Figure 2.9 The block diagram of the vector sum phase shifter

There has been reported various active phase shifters in the literature (Cetindogan, Ozeren, Ustundag, Kaynak & Gurbuz, 2016; Kalyoncu, 2019; Kalyoncu, Ozeren, Burak, Ceylan & Gurbuz, 2019). (Cetindogan et al., 2016) achieved 6-bit phase resolution between 9.6-11.7 GHz with RMS phase error lower than 2.8°. Overall insertion loss is 2.5 dB while $IP1_{dB}$ is -11 dBm. This phase shifter is implemented in 0.25 μm SiGe BiCMOS technology.

2.3 Existing Literature in Phased Array Systems for Satellite Communications

There has been substantial amount of work on phased arrays in SATCOM bands both in academia. (Liu, Li, Li, Deng, Li, Liu & Xiong, 2016) demonstrated a phased array transceiver that operates at X-band, one of the licensed SATCOM bands. In receiver side, the transceiver achieves a gain of 25 dB, an NF of 3 dB, an IP_{1dB} of -18 dBm, an rms phase error less than 3.8° with 5-bit phase resolution, and an rms gain error less than 1.2 dB in the frequency range between 9-11 GHz while consuming 352 mW DC power. A 25-30 GHz receiver was realized in 65-nm CMOS technogy (Mondal et al., 2018). The receiver provides 34 dB gain, 7.3 dB minimum NF, -29 dBm IP_{1dB} with 27.5 mW DC power consumption. (Xie, Feng, Huang, Zhang, Zhao, Liu, Liu, Li & Wu, 2025) implemented RF phased array receiver front-end in Ku-band for SATCOM applications. 8-channel 64-beam receiver achieves 24.5 dB peak gain within the frequency range of 10-15 GHz. The receiver's amplitude control range is 23.5 dB, exhibiting amplitude control step of 0.5 dB. IP_{1dB} of -15.8

dBm is obtained while consuming 465 mW. SATCOM phased arrays has not been a focus in only academia, but also in industry. Axiro F6212 is a Ka-band 16-channel RX active beamforming IC module that operates at 17.7-21.2 GHz, providing 28 dB gain with 26 dB gain control and 0.45 dB gain steps (Renesas Electronics (Axiro), 2025). Phase resolution is 6-bit.

(Sayginer & Rebeiz, 2016) and (Hu et al., 2023) demonstrate wideband operation that covers multiple SATCOM bands in a single IC, which eventually reduce the cost of IC. (Sayginer & Rebeiz, 2016) is an 8-element phased array receiver which operates in 2-16 GHz. In this frequency range, a channel in the receiver performs 4-bit phase control, 3-bit amplitude control with 8 dB, -20 dBm IP_{1dB}, 11.5 minimum NF while consuming 250 mW DC power. This works utilizes QPSK modulation to achieve 122.9-Mbaud with an EVM of 6.3%. (Hu et al., 2023) achieves to operate between 3.1-25.5 GHz, covering C-, X-, Ku-, Ka-bands which are the licensed for SATCOM applications. The receiver consists of 16 channels, providing a peak gain of 26.6 dB, an NF of 2-2.4 dB. IP_{1dB} performance of this receiver is -50 dBm. The amplitude control range is 25 dB while phase resolution is 5-bit with calibration. DC power consumption per channel is 112.5 mW. This work achieves 16-QAM 400-MBaud modulation with an EVM of 1.13-2.35%.

3. WIDEBAND SINGLE-CHANNEL RECEIVER FRONT-ENDS FOR C/X/Ku/Ka-BAND SATCOM SYSTEMS

In this chapter, the design, implementation and measurement of each block in the wideband SATCOM receivers. There are two different versions of the single-channel receivers. The first single-channel receiver consists of an LNA and a phase shifter. The design steps, simulation results and measurement results of each block, and the simulation and measurement results of the first receiver channel are provided in this chapter. The second receiver contains the updated block versions of the previous channel along with an additional VGA to increase the amplitude control range and relax the specifications of the phase shifter block. The design steps, simulation results and measurement results of each block in the second receiver channel, and system level simulation results for the second receiver channel are provided in this chapter. Finally, the comparison with similar works from the literature is presented.

3.1 Receiver with LNA and Phase Shifter

During the design of a receiver system, key performance metrics include noise figure (NF), gain, linearity, bandwidth, and power consumption. The noise performance of a receiver is critical for maintaining signal sensitivity. In other words, NF is a key performance parameter due to the extremely low power levels of the received signal. As defined by the NF equation given in (3.1), even a small amount of added noise power can render the signal undetectable (Pozar, 2011).

$$F_{total} = F_1 + \frac{F_2}{G_1} + \frac{F_3}{G_1 G_2} ... \tag{3.1}$$

In this equation, F represents the noise factor, G represents the gain of each stage, and N denotes the noise power (including both added and initial contributions). In receiver architectures, the order of sub-blocks plays a crucial role in the overall NF performance of the system. The noise contribution of each sub-block, along with the total noise figure of the receiver system, can be calculated using the equation in (3.1). According to this relationship, the first sub-block in the receiver chain must exhibit very low noise and high gain to suppress the noise contributions of subsequent stages. Therefore, in many receiver systems, a high-gain LNA is positioned as the first block in the chain to achieve improved noise performance and gain. To support the intended number of users and to enable SATCOM applications within the target frequency band, appropriate bandwidth—especially the 3-dB bandwidth—is a critical design parameter. The designed system includes an LNA and a phase shifter as shown in Fig. 3.1. With this sub-block order, the receiver prioritizes NF performance over linearity.

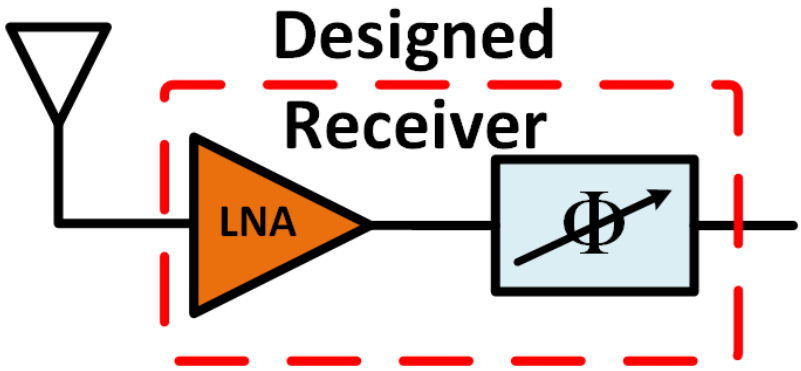

Figure 3.1 The block diagram of the first receiver chain

3.1.1 Low Noise Amplifier

One of the critical blocks used in the receiver system is the low-noise amplifier (LNA). As the first sub-block in the receiver chain, the noise contribution of the LNA is directly added to the overall system noise factor. Therefore, the LNA serves as one of the most critical components in achieving low-noise performance in the receiver. In addition, as the primary gain block within the receiver chain, the LNA amplifies the signal received from the antenna to compensate for losses introduced by subsequent blocks such as attenuators, phase shifters, and mixers. Furthermore, in the presence of strong interfering signals from adjacent channels, the LNA must be capable of linearly amplifying the desired signal without introducing distortion.

It must preserve signal integrity throughout the receiver chain to ensure robustness against data leakage from nearby channels. Consequently, linearity is a vital parameter for optimizing communication quality and reliability and should be considered alongside NF and gain.

In the literature, common-emitter (CE) and cascode topologies have been widely employed in Si-based LNA designs. CE topology can offer lower NF than cascode topology with lower DC power consumption. However, limited available gain from one stage CE necessitates the use of multiple CE stages to obtain the high-gain goal expected from LNA. In CE topology, the feedback mechanism that arises from the collector-base capacitance degrades the stability of the amplifier. On the other hand, the effect of this capacitance is diminished in the cascode topology due to the common-base (CB) part. Cascode topology offers more gain and higher output power at the cost of higher DC power consumption. Considering these trade-offs among the topologies and expectations from the LNA block, the design of the amplification stages is based on a cascode topology. To achieve high gain in a wideband, the LNA is determined to consist of three stages.

As mentioned before, the linearity of an LNA is crucial for the receiver since the LNA must amplify the received signal without distorting it when a strong interferer exists. One of the linearity performance parameters is the referred third-order intercept point (IIP3). Due to the non-linear nature of amplifiers, the amplifier generates inter-modulation products when there are more than two input signals. If these input signals are close in frequency, their third-order inter-modulation (IM3) product resides in the operation band. IIP3 indicates the relationship between signal power at the fundamental tone and IM3 products. To suppress the output power generated by third-order IM3 products, an additional nonlinear circuit, referred to as an auxiliary circuit, is introduced into the amplifier. This auxiliary path is designed to generate out-of-phase IM3 components with the output signal in the main path. As a result, the sum of the outputs of auxiliary and main paths at the output leads to a reduced IM3 magnitude compared to that generated by the main amplifier alone. This method is referred to as post-distortion.

One variant of the post-distortion method utilizes a diode-connected auxiliary element at the output of the first stage of a cascode amplifier. This element injects a third-order component out of phase with the undesired IM3 product at an intermediate node, thereby facilitating cancellation. This method introduces additional loss and a rise in NF due to the reduced output impedance of the first amplifier stage. On the other hand, enhanced IP3 performance across a wide bandwidth is achievable using the diode-connected auxiliary structure. In (Kim, Aparin, Barnett

& Persico, 2006), the active post-distortion with auxiliary device demonstrated up to 20 dB IIP3 enhancement when the post-distortion method was employed. Another study reported an IIP3 as high as 14.1 dBm using a similar approach (Zhang, Fan & Sinencio, 2009). In this LNA design, a diode-connected post distortion method is employed for IIP3 improvement. To demonstrate the IIP3 improvement in SiGe BiCMOs technology clearly, two separate two-stage cascode LNAs were fabricated; one without the post-distortion method and the other with the post-distortion method. To achieve high gain in the receiver, an additional stage was implemented as the first stage. Since the fabricated LNA to showcase post-distortion method is a two-stage amplifier, this design is explained in this part of the thesis. The design steps of the first stage is similar to the second stage. The LNAs were designed with the contributions from M. Emre Çakır.

The second stage is designed using a simultaneous noise and power matching technique. The design process begins with selecting the collector current for a unit device (with emitter length (l_e = 0.84 μm) and emitter width (w_e = 0.12 μm) that minimizes the minimum NF, NF_{min}. Once the optimal collector current for the unit device is identified, the number of transistors is determined such that the resulting optimal source resistance for noise matching aligns with the standard system impedance of 50 Ω. An emitter inductor is introduced to ensure that the real part of the input impedance matches 50Ω, thereby satisfying both noise and power matching requirements.

To achieve the target bandwidth, an RC feedback technique was implemented in each stage. RC feedback contributes to flattening and enhances both input and output impedance matching. However, its drawbacks include a reduction in gain and reverse isolation, along with an increase in NF. In (Hu, Li, Kazan & Rebeiz, 2024), staggered tuning and series R–L load techniques were compared as alternative bandwidth extension methods. In multistage amplifier architectures, staggered tuning involves assigning the peak gain of each stage to different frequencies, thereby broadening the overall bandwidth. According to (Hu et al., 2024), the primary limitations of staggered tuning are the requirement for large load inductors at lower frequencies and the variation of NF across the frequency band. On the other hand, the series R–L load technique offers a frequency-independent, flat gain response, avoiding the multiple gain peaks characteristic of staggered tuning. Consequently, the series R–L load technique was also adopted in this design to extend the bandwidth while mitigating the limitations associated with staggered tuning.

Another key point in the design of this LNA is the single-ended to differential conversion. Generally, this conversion takes place in the phase shifter as mentioned

before. However, a passive balun that operates in a wide bandwidth is challenging to design. To relax the phase shifter design, a passive balun is integrated into the LNA design at the interstage. The balun is a part of the matching network between the second and third stages. The schematic of the designed LNA is shown in Fig. 3.2. The post-layout electromagnetic simulations of designed LNA were conducted in Keysight ADS Momentum. The designed LNA with and without post-distortion method occupy 0.86 mm^2 (1.31 mm $\times$ 0.65 mm) while 52.9 mW DC power consumption.

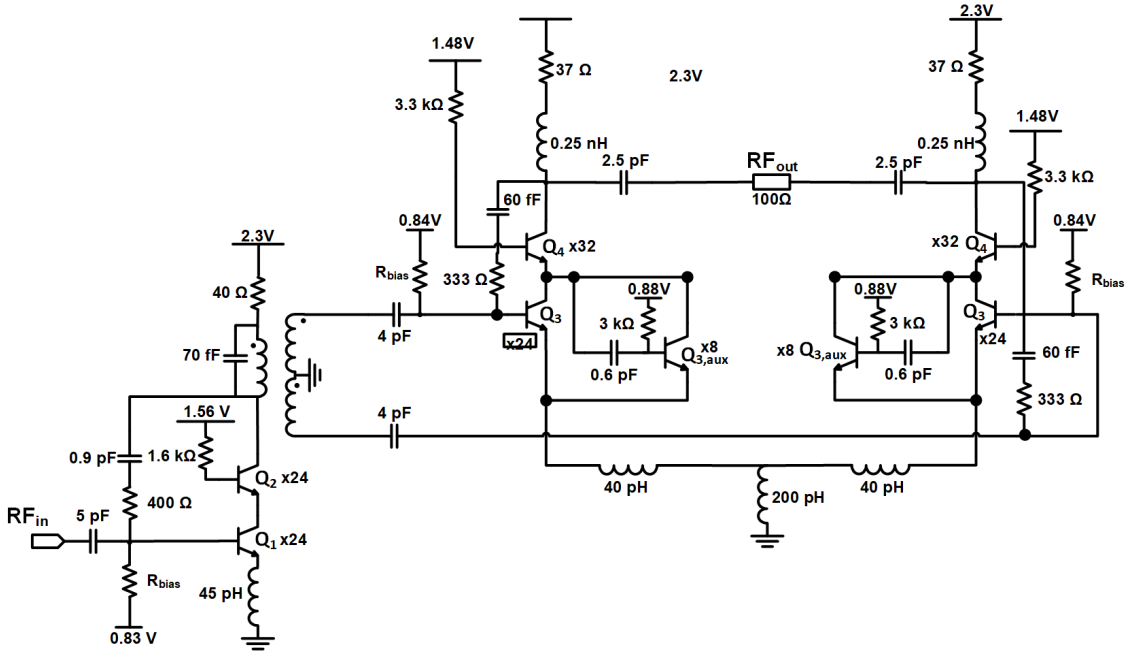

Figure 3.2 The schematic of the designed LNA

Pad-to-pad measurements setup for S-parameter measurements is shown in Fig. 3.3. During the S-parameter measurements, a Keysight N5224A network analyzer was utilized with the 100-μm Picoprobe GSG RF probes. In order to move the reference planes to the probe tips, short-open-load-thru (SOLT) calibration was performed using the Picoprobe CS-5 substrate calibration kit. The power level of the network analyzer was set to -30 dBm to avoid operating in compression.

S-parameter measurements are demonstrated in Fig. 3.5 and Fig. 3.6. The measurement results indicate that both input and output return losses are better than 8 dB in the frequency range of 1-25 GHz. The LNA without the post-distortion method provides 18 dB gain, whereas the other LNA has 17 dB gain.

Pad-to-pad measurement setups for linearity and NF characterization are illustrated in Fig. 3.4. The linearity performance of the fabricated chips was characterized using 100-μm Picoprobe GSG RF probes, using a Keysight E8257D and E8567D signal generators and a Keysight E4448A spectrum analyzer. To account for the insertion

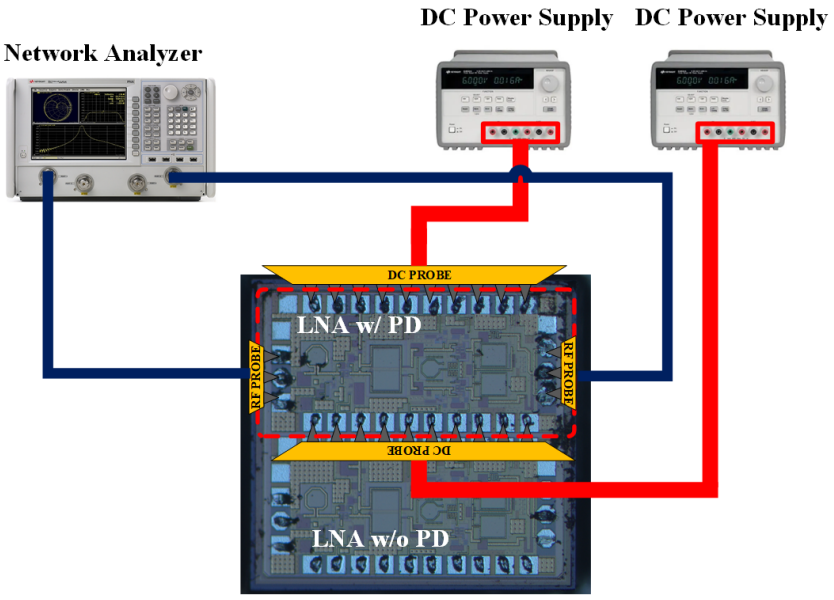

Figure 3.3 The S-parameter measurement setups for the designed LNA

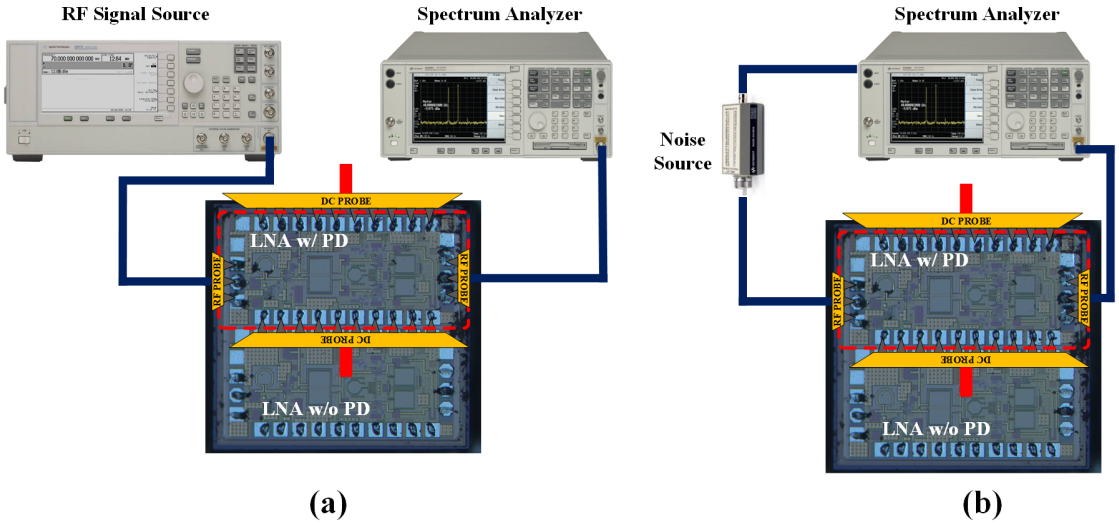

Figure 3.4 The measurement setups for the designed LNA: (a) Linearity and (b) NF

loss introduced by RF cables and probes, thru-line calibration measurements were performed using the Picoprobe CS-5 substrate calibration kit.

The NF measurement results are presented in Fig. 3.7. A 0.2 dB increase in NF is observed when comparing the two configurations: the LNA without post-distortion exhibits an NF of 2.6 dB, while the LNA with post-distortion demonstrates an NF of 2.8 dB. Linearity measurement results, shown in Fig. 3.8, indicate that the LNA employing post-distortion achieves an IP_{1dB} of -15 dBm, in contrast to -19 dBm for the LNA without post-distortion—representing a 4 dB improvement.

IIP3 measurements show that the post-distortion technique enhances IIP3 from -6.2 dBm to -2.7 dBm, yielding a 3.5 dB improvement. Overall, the measurement results

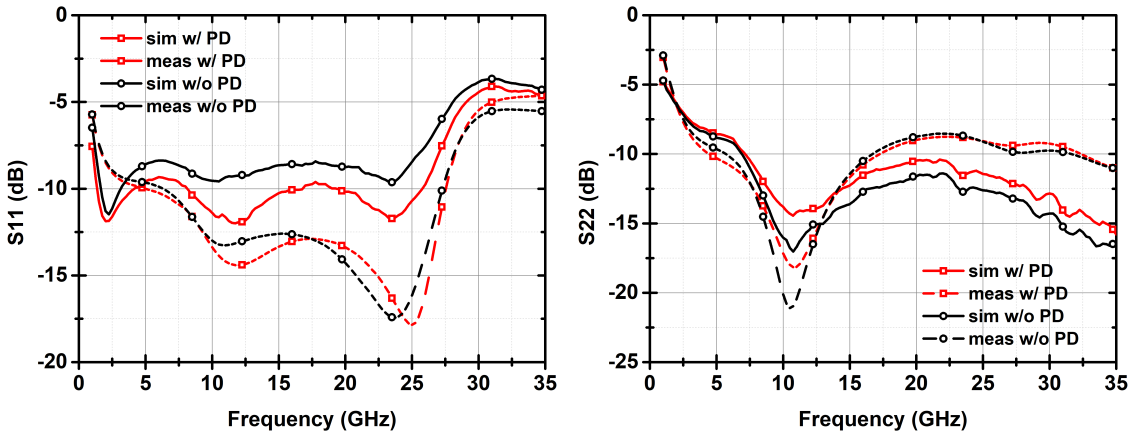

Figure 3.5 The measured input and output matchings of the designed LNA: (left) S11 and (right) S22

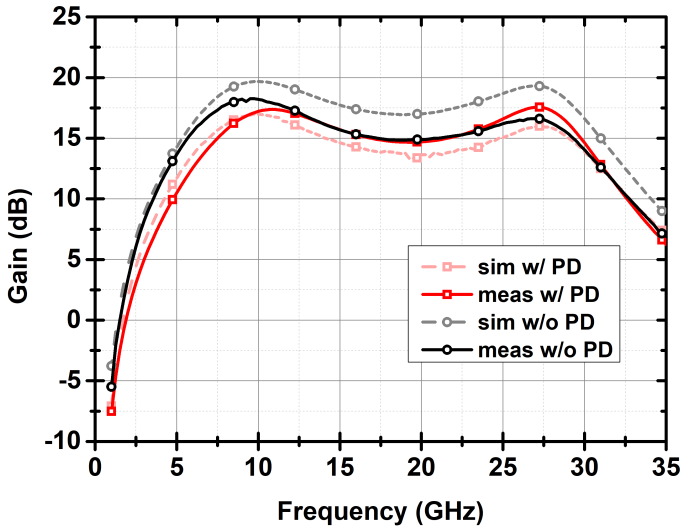

Figure 3.6 The measured gain of the designed LNA

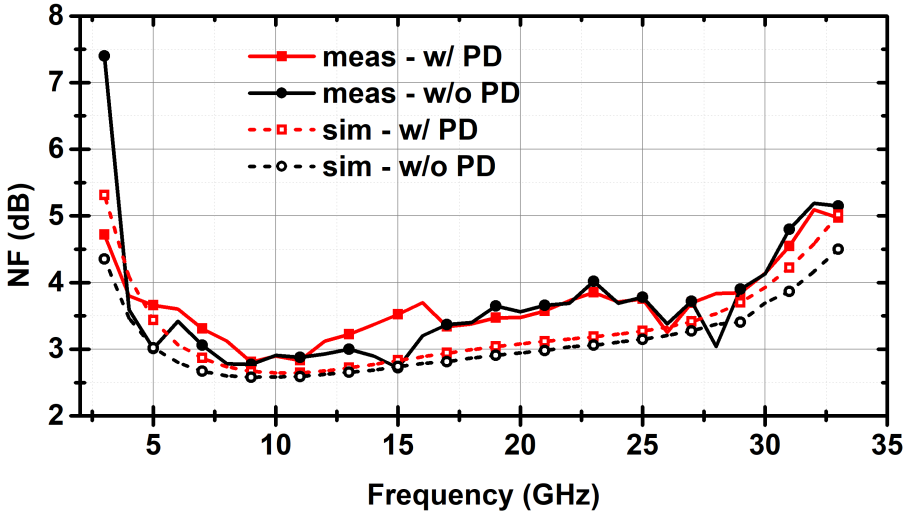

Figure 3.7 The NF simulation and measurement results of the designed LNA

are consistent with simulation data, confirming that the post-distortion method effectively enhances the linearity performance of the LNA.

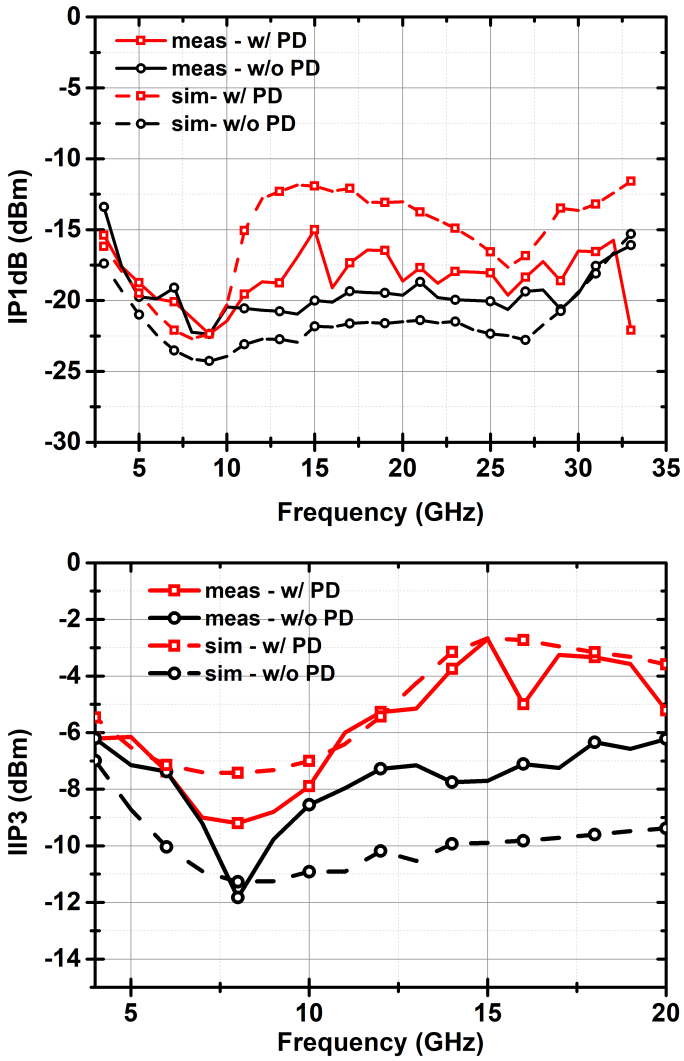

Figure 3.8 The linearity simulation and measurement results of the designed LNA: (top) IP1dB and (bottom) IIP3

$$FoM_1 = \frac{Gain}{F-1} \cdot \frac{IP_{1dB}(mW)}{P_{dc}(mW)} \cdot 10 \tag{3.2}$$

$$FoM_2 = \frac{Gain}{F-1} \cdot \frac{IIP3(mW)}{P_{dc}(mW)} \cdot 10 \tag{3.3}$$

Table 3.1 demonstrates the comparison of the designed LNA with the Si-based wideband LNA works (Gurol, Ozboz, Ozkan, Kalyoncu & Gurbuz, 2024; Hu et al., 2024; Saha, Shankar, Schmid, Mills & Cressler, 2012; Wang, Chen, Hou, Zhou, Chen,

Wang, Xu & Hong, 2024; Zhang, Li, Ye, Li & Ren, 2011). Among the compared works, the highest gain is observed in (Wang et al., 2024). This work has higher power consumption and lower IIP3 performance. (Gurol et al., 2024) achieves the highest IIP3 of among the compared works in a narrower bandwidth with lower gain. The designed LNA achieves high gain, wide bandwidth with a high linearity performance. Moreover, the designed LNA performs single-ended to differential conversion different than the comprared works.

Table 3.1 Comparison with the Si-based wideband LNA works

Reference	**(Gurol et al., 2024)**	**(Wang et al., 2024)**	**(Zhang et al., 2011)**	**(Saha et al., 2012)**	**(Hu et al., 2024)**	**This Work w/ PD**
Technology	0.13 μm SOI CMOS	0.13 μm SiGe BiCMOS	0.13 μm SiGe BiCMOS	0.13 μm SiGe BiCMOS	90 mm SiGe BiCMOS	**0.13 μm SiGe BiCMOS**
NF	3.07 dB	1.4–4.3 dB	2.8 dB	4.5–6.5 dB	1.8–2.2 dB (2–20 GHz)	**2.8–4 dB (3–29.5 GHz)**
IP$_{1dB}$ (@ f$_{center}$)	-10 dBm	-18 dBm	NA	-5.6 dBm	-20 to -15 dBm	**-15 dBm**
Gain	13.2 dB	27 dB	16.3 dB	9 dB	20 dB	**18 dB**
3dB BW	22–28 GHz	1–27 GHz	1–10 GHz	3–26 GHz	1.6–24 GHz	**6–30 GHz**
Power	32.67 mW	85 mW	23 mW	33 mW	29 mW	**52 mW**
IIP3	6 dBm	-5 dBm	-3.2 dBm	5.8 dBm	-	**-2.5 dBm**
Core Area	0.61 mm^2	0.27 mm^2	0.33 mm^2	0.35 mm^2	0.21 mm^2 *	**0.37 mm^2**
FoM1 & FoM2	0.12 & 0.467	0.1810 & 0.055	- & 1.6	0.048 & 0.67	0.078 & -	**0.05* & 0.9**

***** : Estimated from figure

3.1.2 Passive Vector-Sum Phase Shifter

Phase shifter topologies have been discussed in the previous chapter. Vector modulator type phase shifters have the advantages of high phase resolution within a compact area and bandwidth. Thus, vector modulator topology was selected to cover SATCOM bands. The traditional design approach for vector-modulators predominantly uses VGAs to adjust the magnitude of the vectors. While VGAs are beneficial in terms of providing gain, they come with their own set of challenges, particularly when it comes to maintaining linearity. Another limiting factor of VGAs is their inherent DC power consumption. Low linearity and high DC power consumption increase the burden of the phase shifter for system performance. For instance, the DC power budget of VGAs, eventually phase shifters, can be used in a power amplifier to obtain higher output power at the end of the transmitter chain, assuming the transmitter chain has sufficient gain. In a receiver, a phase shifter can be a bottleneck for linearity due to VGAs.

Given these limitations, a shift in design strategy has been observed where VGAs are replaced with VVAs in vector-modulators, as referenced in (Gao & Zhao, 2021). The introduction of VVAs not only addresses the linearity issues associated with VGAs but also provides an advantage in terms of no power consumption due to their typically passive nature. Additionally, the design with VVAs helps for more compact configurations, further adding to the benefits of this approach in the quest for cost-effective and efficient RF circuits.

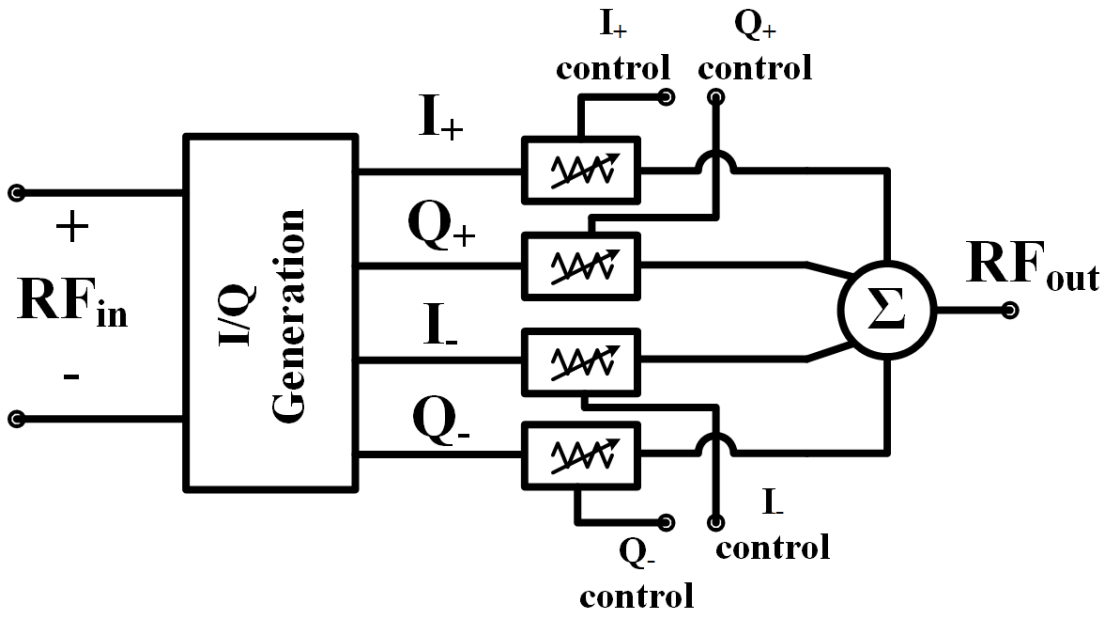

Figure 3.9 The block diagram of the phase shifter

The proposed vector-modulator phase shifter can be divided into three parts as shown in Fig. 3.9: differential and quadrature signal generations, vector modulator, and vector combination. The single-ended to differential conversion or differential signal generation was integrated into the LNA as explained in the LNA design. The next part is the generation of I and Q signals, which are 90° apart from each other. A quadrature all-pass filter (QAF) was employed for I/Q generation since wideband performance can be obtained with QAF. The final stage is the weighted combination of I and Q signals. The weights are the amplitudes of each signal determined by a VVA. Therefore, there are four VVAs in total, one VVA for each I and Q signal. The weighted I/Q signals are combined in the final part.

3.1.2.1 I/Q Signal Requirements

For simplicity, it is assumed that the input signal has a magnitude of 1V and a phase of 0°. The first stage performs a single-ended to differential conversion, commonly referred to as a balanced-to-unbalanced (balun) transformation. Due to layout asymmetry and parasitic effects, baluns are unable to perfectly convert the input signal into two equal-amplitude, out-of-phase signals. To simplify the analysis, the phase and amplitude errors are reflected on the "minus" line as $\Delta\theta_{balun}$ and $|\Delta\varepsilon_{balun}|$ in (3.4) and (3.5), respectively. Additionally, the balun introduces insertion loss of more than 1dB in addition to the 3dB division loss (Shin, Kim, Kang & Rebeiz, 2013). Consequently, the voltage gain of the balun is represented by A_{balun} in (3.4) and (3.5). The output signals of the balun are depicted in Fig. 3.10.a.

$$v_+ = |A_{balun}|\angle 0^\circ \tag{3.4}$$

$$v_- = |A_{balun} + \Delta\varepsilon_{balun}|\angle(180^\circ + \Delta\theta_{balun}) \tag{3.5}$$

Two out-of-phase signals obtained from (3.4) and (3.5) are input into an I/Q generation network to produce quadrature signals. The I/Q network generates ±45° phase-shifted versions of both input signals, resulting in outputs that are separated by 90°. Furthermore, the phase and amplitude errors are reduced by half during the I/Q generation process (Singhal & Hasan, 2022). Most I/Q generation networks

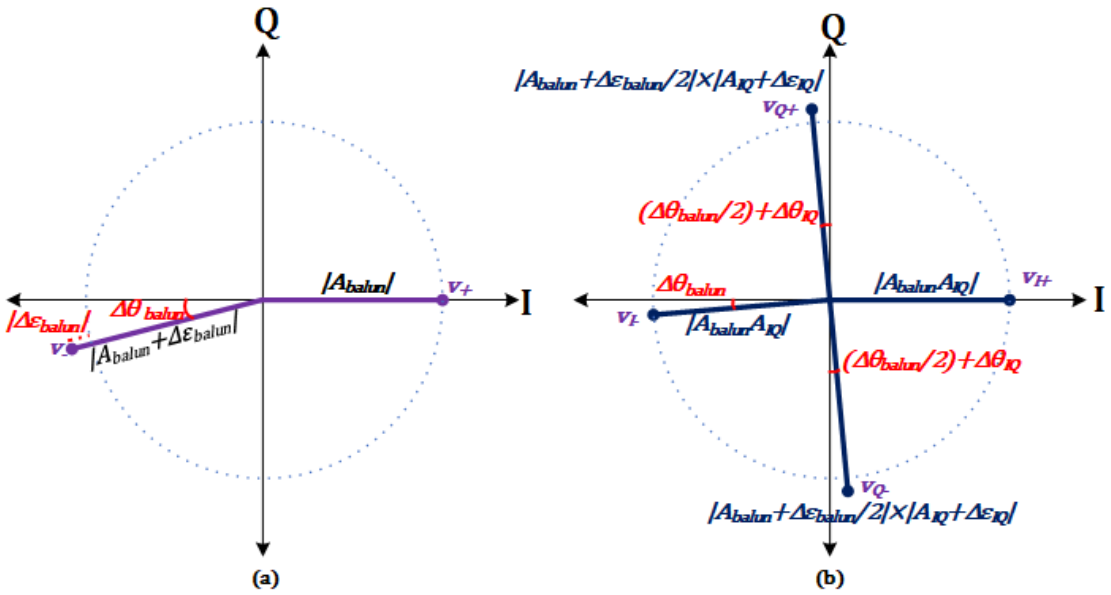

Figure 3.10 Signals after (a) balun (b) I/Q generation networks

exhibit negligible phase and amplitude errors at the center frequency. However, the frequency response of these networks limits the bandwidth, causing increased phase and amplitude errors as the frequency deviates from the center frequency. Consequently, the phase and amplitude errors introduced by the I/Q network are denoted as $\Delta\theta_{IQ}$ and A_{IQ}, respectively. It is important to note that the I_+ and I_- paths are identical, meaning their relative phase difference is unaffected by the errors in the network. The resulting quadrature signals are described in (3.6)-(3.9). The output signals of the I/Q network are shown in Fig. 3.10.b.

$$v_{I+} = |A_{balun} \times A_{IQ}|\angle 0^\circ \tag{3.6}$$

$$v_{I-} = |A_{balun} \times A_{IQ}|\angle(180^\circ + \Delta\theta_{balun}) \tag{3.7}$$

$$v_{Q+} = |A_{IQ} + \Delta\varepsilon_{IQ}| \times |A_{balun} + \frac{\Delta\varepsilon_{balun}}{2}|\angle(90^\circ + \frac{\Delta\theta_{balun}}{2} + \Delta\theta_{IQ}) \tag{3.8}$$

$$v_{Q-} = |A_{IQ} + \Delta\varepsilon_{IQ}| \times |A_{balun} + \frac{\Delta\varepsilon_{balun}}{2}|\angle(270^\circ + \frac{\Delta\theta_{balun}}{2} + \Delta\theta_{IQ}) \tag{3.9}$$

Finally, the quadrature signals are summed with different ratios in the last stage. The output signal is obtained as in (3.10). For simplicity, the phase and amplitude errors in the quadrature signals, along with the error arising from the amplitude weightings, are approximated to cumulative errors, $\Delta\theta_{Total}$ and $\Delta\varepsilon_{Total}$ in (3.10).

$$v_{out} = |A_{I,n}| \times v_{I\pm} + |A_{Q,n}| \times v_{Q\pm} \approx \pm|A_{I,n}| \times |A_{balun} \times A_{IQ}|\angle 0^\circ \pm|A_{Q,n}| \times |A_{balun} \times A_{IQ} + \Delta\varepsilon_{Total}|\angle(90^\circ + \Delta\theta_{Total}) \tag{3.10}$$

$$\Delta\theta_{Total} = \frac{\Delta\theta_{balun}}{2} + \Delta\theta_{IQ} + \Delta\theta_{weight,n} \tag{3.11}$$

$$\Delta\varepsilon_{Total} = \left((|A_{balun}| \times \Delta\varepsilon_{IQ}) + (\frac{\Delta\varepsilon_{balun}}{2} \times |A_{IQ}|) + (\frac{\Delta\varepsilon_{balun}}{2} \times \Delta\varepsilon_{IQ})\right) \times \Delta\varepsilon_{weigth,n} \tag{3.12}$$

where n is the state-number among the 2^N states for an N-bit phase shifter, and $|A_{I,n}|$ and $|A_{Q,n}|$ are the corresponding weights of the IQ signals. By utilizing amplitude and phase errors in (3.12) and (3.11), we can calculate output phase and amplitude errors at any given phase state as in (3.13) and (3.14), respectively (Kim, Kang, Koh & Rebeiz, 2012).

$$\theta_{Error,n} = \tan^{-1}\frac{|A_{Q,n}|}{|A_{I,n}|} - \tan^{-1}\left(\frac{|A_{Q,n}|\Delta\varepsilon_{Total}cos(\Delta\theta_{Total})}{|A_{I,n}| - |A_{Q,n}|\Delta\varepsilon_{Total}sin(\Delta\theta_{Total})}\right) \tag{3.13}$$

$$\varepsilon_{Error,n} = \frac{1 + (\frac{|A_{Q,n}|}{|A_{I,n}|}\Delta\varepsilon_{Total})^2 - 2\frac{|A_{Q,n}|}{|A_{I,n}|}\Delta\varepsilon sin(\Delta\theta_{Total})}{1 + (\frac{|A_{Q,n}|}{|A_{I,n}|})^2} \tag{3.14}$$

To achieve N-bit phase resolution without any overlapped phase-states, the maximum phase error at any state should be smaller than half of the least-significant bit (LSB). This error margin can be calculated as $360^\circ/2^{N+1}$. By utilizing (3.13), different phase and amplitude errors have been analyzed to determine phase resolution for each error combination. The amplitude error is constrained to ±10 dB, and the

phase error is limited to ±30°. For each combination of phase and amplitude error within these ranges, the output phase error is calculated and compared to half of the LSB for different bit resolutions. Following these comparisons, the phase resolution limits for various phase and amplitude errors are identified and illustrated in Fig. 3.11.

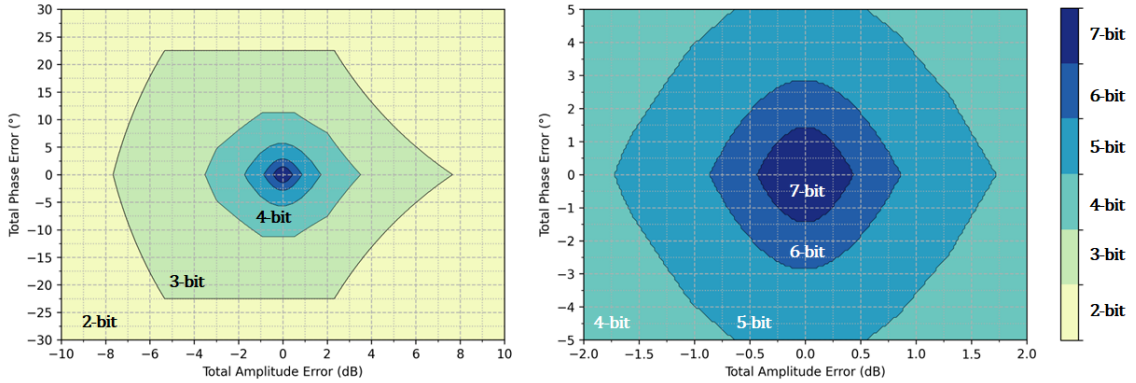

Figure 3.11 Bit resolution regions for different phase and amplitude errors

For instance, when $\Delta\theta_{Total}$ is 5° and $\Delta\varepsilon_{Total}$ is -4 dB, the maximum calculated phase error across all phase states is 15.2°. This value is less than half of the LSB for a 3-bit phase resolution ($360°/2^{3+1} = 22.5°$) but exceeds the limit for a 4-bit phase resolution ($360°/2^{4+1} = 11.25°$). Consequently, it falls within the 3-bit phase resolution region.

3.1.2.2 Quadrature All-Pass Filter Design

There have been various works on quadrature signal generation in literature (Hu et al., 2023; Kim et al., 2012; Kulkarni, Zhao & Reynaert, 2013). (Kulkarni et al., 2013) utilizes poly-phase filters (PPF) to obtain low phase error in a wide bandwidth. In PPFs, the bandwidth of the quadrature phase difference depends on the order of the network. In other words, the bandwidth can be expanded by adding another RC section to the filter. However, each RC section inserts an additional 3-dB loss. (Kim et al., 2012) employs QAF to generate I/Q signals. The performance of QAF is comparable with 2^{nd}-order poly-phase filters (PPF) in terms of phase and amplitude imbalance due to its second-order frequency response. QAF has superiority over PPF since QAF leads to lower losses than PPF. The bandwidth of a QAF can be widened by reducing the quality factor of the network (Kim et al., 2012). The drawback of QAF is the area due to the inductors in QAF. The center frequency of QAF is determined by $\omega_0 = 1/\sqrt{L_1 C_1}$. R_1, R_2, and R_3 are de-Q resistors employed

to enhance the bandwidth with the cost of increased insertion loss. L_2 and C_2 make final adjustments in the phase response. The schematic of QAF is demonstrated in Fig. 3.12. The resistors were realized with five parallel R_{poly} resistors, which provide almost constant resistance over a wide temperature range.

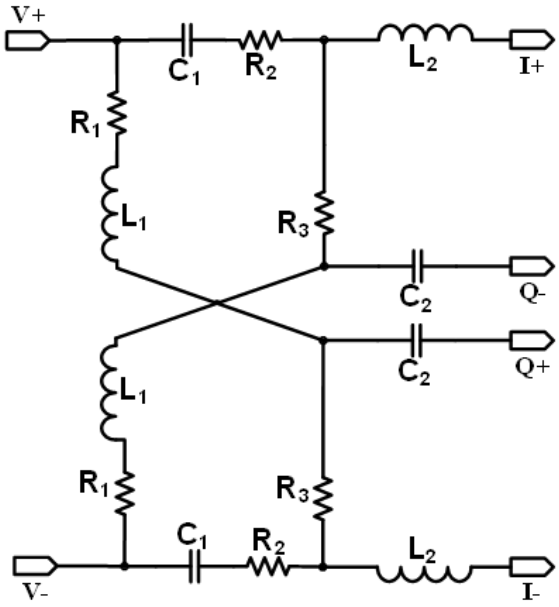

Figure 3.12 The schematic of QAF

Fig. 3.13 presents the simulation results of the designed QAF. The QAF has an insertion loss lower than 16 dB between 5 and 30 GHz. Phase and amplitude imbalance between I/Q signals is lower than approximately 2° and 1 dB, respectively.

3.1.3 Voltage Variable Attenuator

VVA has a significant role in the phase shifter architecture since the summation weights of the I/Q vectors are determined by the VVA. The amplitude range and resolution of VVA are crucial. The attenuation of devices in the circuit may vary with temperature. The performance of VVA should not change drastically with the temperature.

Conventional VVAs are typically designed with two separate control voltages—one for the series device and the other for the shunt device as shown in Fig. 2.7. This conventional design strategy introduces challenges in achieving both the desired level of attenuation and simultaneously ensuring that the input/output remains matched to a standard impedance of 50Ω.

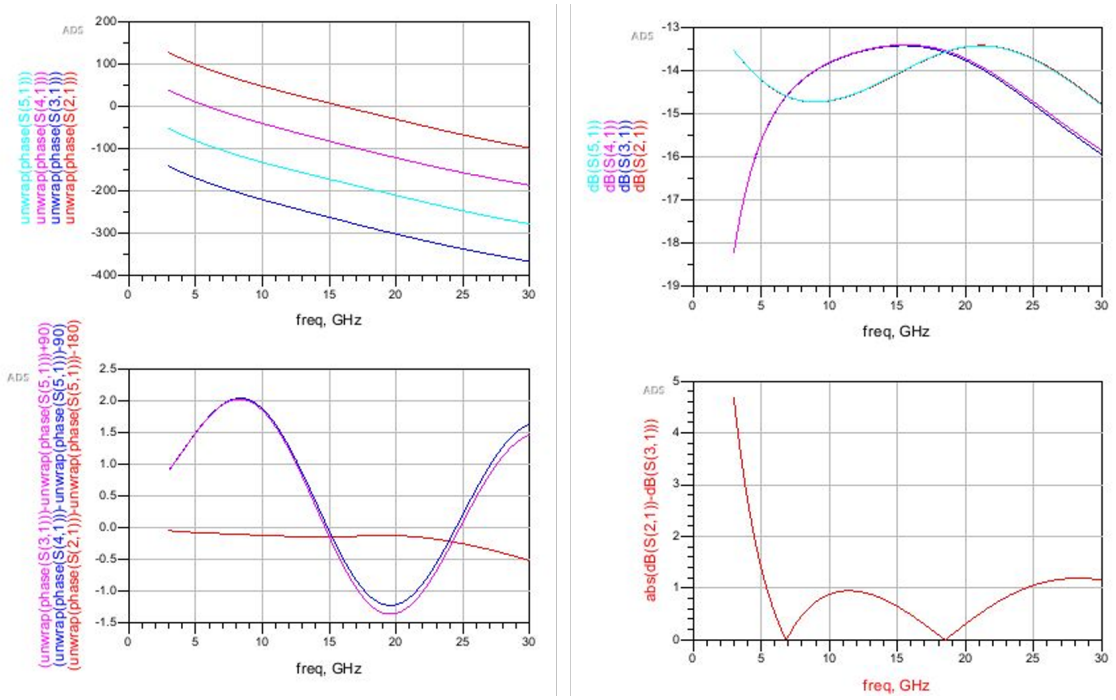

Figure 3.13 The simulation results of QAF

Considering these challenges, a VVA with close-loop controls was proposed to control amplitude in the phase shifter architecture. To simplify this control mechanisms and solve existing problems related to conventional VVA,a close-loops approach can be used for the VVA. As a drawback, a close-loop approach will reduce the possibility to find the optimum point that can be obtained by external voltage controls. In other words, when the comparison conditions in the close-loops are met, the iterations in the loops will stop and the optimum point for the conditions would have been missed. The schematic of the proposed close-loop VVA is demonstrated in Fig. 3.14. There are two close-loops in the VVA: one for the determination of the attenuation, the attenuation loop, and the other for the matching, the matching loop. A close-loop is divided into two segments: the main attenuator and a replica attenuator. The main attenuator is shared between two close-loops.

In the attenuation loop, the control voltage of the series devices, V_{series}, is determined. Instead of a replica attenuator, a copy of the series device is placed series to R_2. The channel resistance of the copy series device is referred as R_{series}. The voltage division between R_{series} and R_2 generates a voltage at the positive input of the operational amplifier (Opamp). The voltage at the negative input is determined by the voltage division between R_2 and R_3. R_3 is controlled externally to obtain the desired attenuation. Since the voltage at the negative input is fixed, the Opamp generates an output voltage to reduce the voltage difference between its inputs. By this way, V_{series} is determined by the loop. Another advantage of

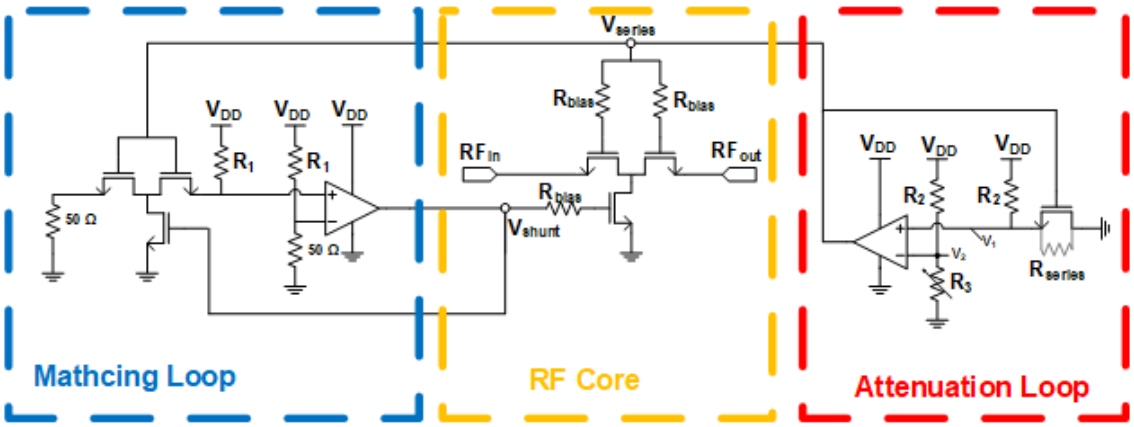

Figure 3.14 The proposed closed-loop VVA

this attenuation loop is that the attenuation is constant with varying temperature since the attenuation is determined with the ratio between R_2 and R_{series} and the ratio is not related to the temperature. The process variations will be covered in the design phase. These close-loop configurations, therefore, provide a self-calibrating mechanism that eliminates the need for manually adjusting the two control voltages.

In the loop, an external voltage is directly applied to the negative input instead of utilizing R_3 to reduce the complexity of controlling R_3. Also, the external voltage can be generated after a DAC for digital-control purpose.

In the matching loop, a 50Ω resistor is placed at the far end of the replica attenuator, which transforms the 50Ω resistance to another value. This transformed resistance generates a voltage at the positive input of the Opamp, which is proportional to R_1 and the transformed resistance value. The negative input of the Opamp is set to a specific value due to the voltage division between R_1 and the 50Ω resistor. The Opamp generates an output voltage to reduce the voltage difference between its inputs. As a result, the voltage at the positive input converges to the fixed voltage at the negative input terminal. Through this process, V_{shunt} is determined by the loop based on the given series device voltages.

As mentioned before, since the blocks prior to passive structures, the linearity bottleneck in the phase shifter is the VVA. The linearity of the VVA can be enhanced by stacking the devices. With the stacking, the voltage swing of a signal will be distributed among the stacked devices, thus, overall voltage swing can be increased, so the input power. By this way, the power handling capability of the VVA is improved.

3.1.3.1 The Design of Opamp

In this phase shifter architecture, Opamp plays a crucial role in the feedback loops to control voltage-variable attenuator (VVA) as depicted in Fig. 3.14. Negative input of the Opamp is connected to a reference circuit. The reference circuit can be a voltage source as in the attenuation loop or a resistor as in the matching loop. Positive input is connected to a replica network. The output of the Opamp is used to control the replica network by making voltages sensed at the inputs of the Opamp closer. This control becomes more precise as the common mode rejection ratio (CMRR) of the Opamp is higher. One way to increase CMRR is to obtain higher differential gain from the Opamp. To increase the gain, length of transistors are set to 1μm. To avoid instability issues, RC-compensated two-stage Opamp topology is selected as shown in Fig. 3.15.a. Output voltage range is increased to 3.3 V by utilizing high voltage MOSFETs. Fig. 3.15.b also illustrates the layout of the Opamp.

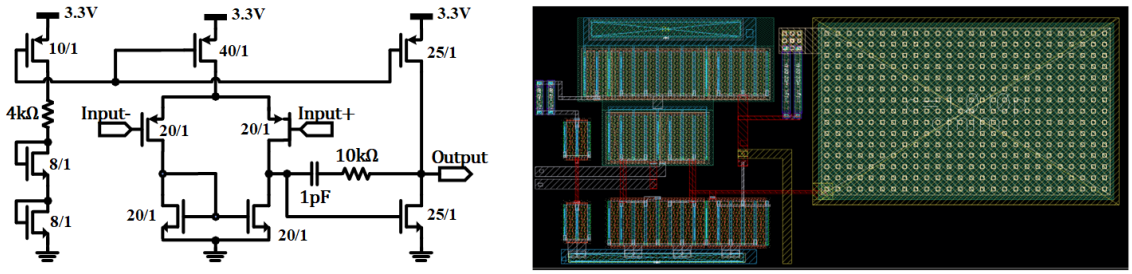

Figure 3.15 (a) Schematic and (b) layout of the designed Opamp

The designed Opamp draws 249 μA current from 3.3 V voltage supply. Post-layout simulations indicate that the designed Opamp provides 63.1 dB gain with a 3-dB bandwidth of 25.49 kHz as demonstrated in Fig. 3.16. The phase margin is 58° Common-mode gain is -11 dB and CMRR is approximately 74 dB. The simulated slew rate for a 2 pF load capacitance is 11.43 V/μs.

3.1.3.2 Attenuator Core

The VVA design proceeds with the determination of device sizes. We can represent series transistor as R_{series} and shunt transistor as R_{shunt}. The relationships between these resistances and attenuation for a T-type attenuation network are given in (3.15) while keeping the resistance seen from the input or output as 50 Ω.

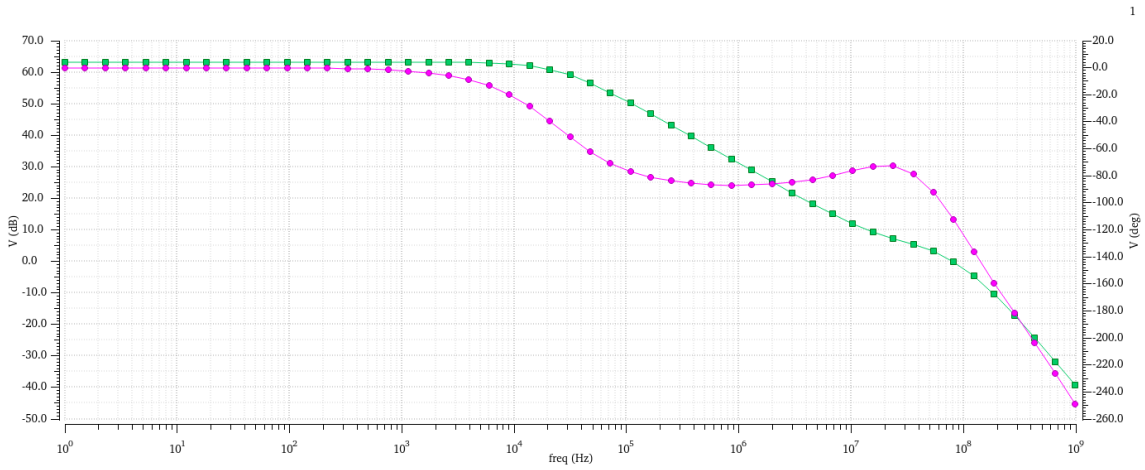

Figure 3.16 The simulation results of the designed Opamp

$$R_{series} = Z_0 \times \frac{10^{Att(dB)/10} - 1}{10^{Att(dB)/10} + 1} \quad and \quad R_{shunt} = 2Z_0 \times \frac{10^{Att(dB)/10}}{10^{Att(dB)/10} - 1} \tag{3.15}$$

These equation indicate that R_{series} increases up to 48 Ω and R_{shunt} decreases from approximately 5 kΩ. To reduce the insertion loss (IL) of the attenuator, the series device should be large, and the shunt device should be small. On the other hand, a large attenuation range requires larger shunt devices. Also, larger devices lead to higher parasitic capacitances, which deviate impedance matching from 50 Ω. Considering these trade-offs, the series device size is selected as 65μm/130nm and the shunt device is selected as 35μm/130nm.

To increase linearity, two-stack shunt devices are used. Also, two T-type VVAs are cascaded to achieve a 32 dB attenuation range. Gates are biased through 20 kΩ. The same T-type VVA is copied in the matching loop. A five-stack of series devices is used in the attenuation loop for better control in the attenuation range. The designed VVA is shown in Fig. 3.17. VVA core occupies 77μm $times$67μm without including Op-amps.

The post-layout simulations indicate that the IL of the designed VVA is between 4-7 dB in a 1-30 GHz bandwidth while providing approximately 40 dB attenuation range. Fig. 3.18 shows the attenuation at different temperatures. -40°C, 27°C, and 100°C temperatures are represented with red, yellow, and green traces in all graphs. The IP_{1dB} of the designed VVA is higher than 15 dBm at the reference state.

Pad-to-pad measurements setups for linearity and S-parameter measurements are shown in Fig. 3.19. The linearity performance of the chips was measured with 100-μm Picoprobe GSG RF probes, employing a Keysight E8257D signal generator

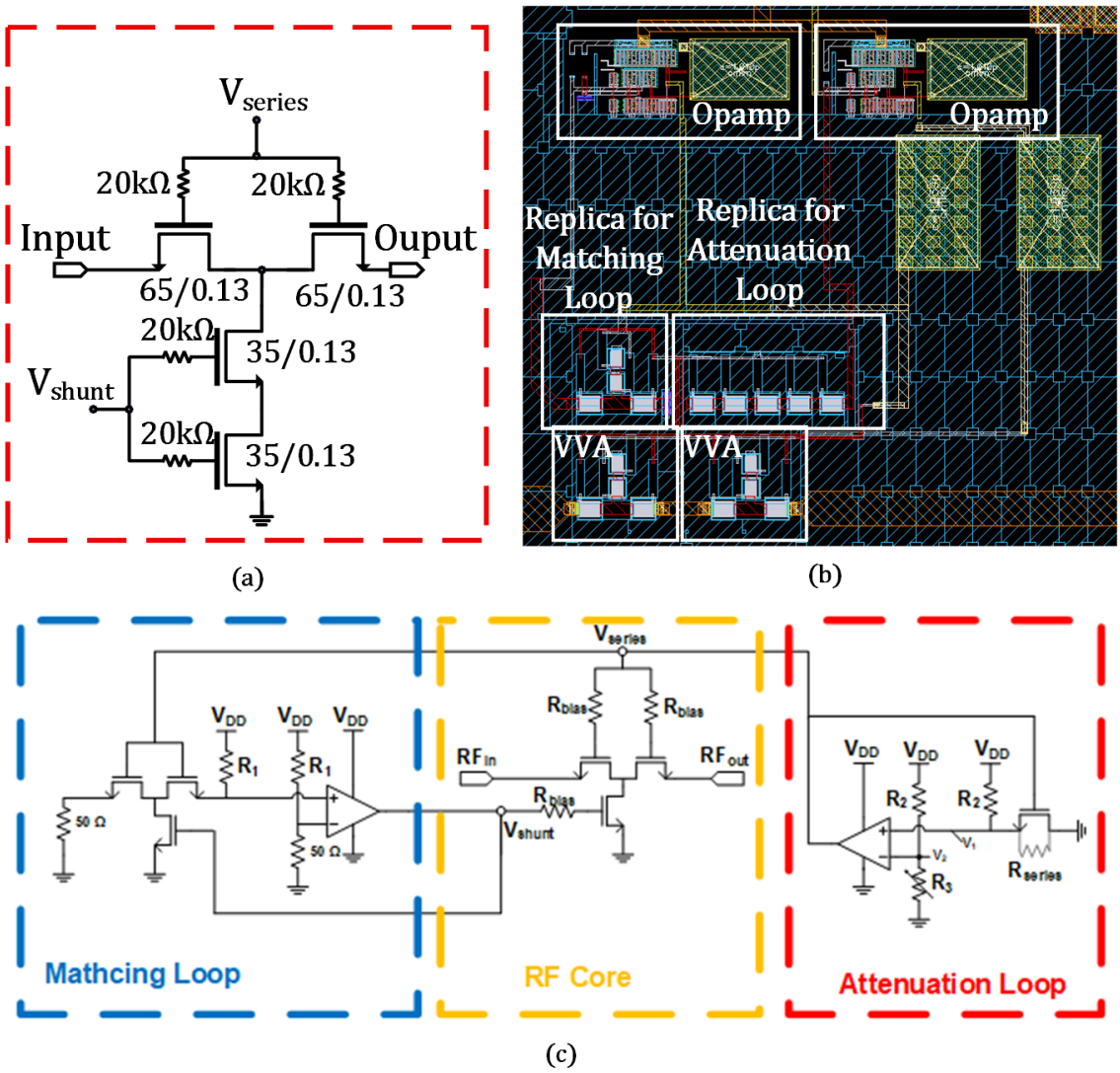

Figure 3.17 The designed closed-loop VVA: (a) attenuation core, (b) the layout of the close-loop VVA, (c) the schematic of the proposed close-loop VVA

and Keysight E4448A spectrum analyzer. To quantify the loss that arises from the RF cables and probes, thru line measurements were conducted on the Picoprobe CS-5 substrate calibration kit. During the S-parameter measurements, a Keysight N5224A network analyzer was utilized with the same probes. In order to move the reference planes to the probe tips, short-open-load-thru (SOLT) calibration was performed using the impedance standard substrate CS-5.

The linearity measurements were planned before S-parameter measurements to find the linear operation region of the VVA. During the linearity measurement, the input power was swept from -10 dBm to 16 dBm at different frequencies between 1 GHz and 30 GHz. After excluding the cable and probe losses, IP_{1dB} of the VVA varies between 9 and 15 dBm as shown in Fig. 3.20.

In order not to cause gain compression in the S-parameter measurements of the VVA,

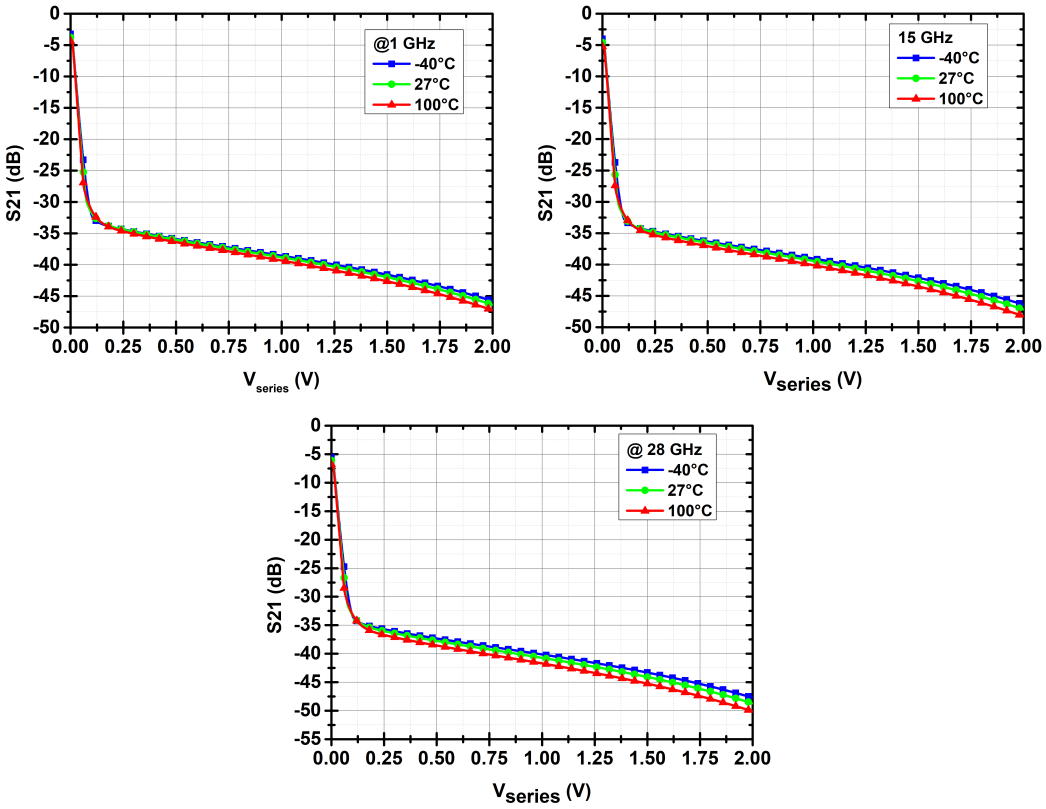

Figure 3.18 Attenuation of VVA at different temperatures (top left) at 1 GHz, (top right) at 15 GHz, and (bottom) at 28 GHz

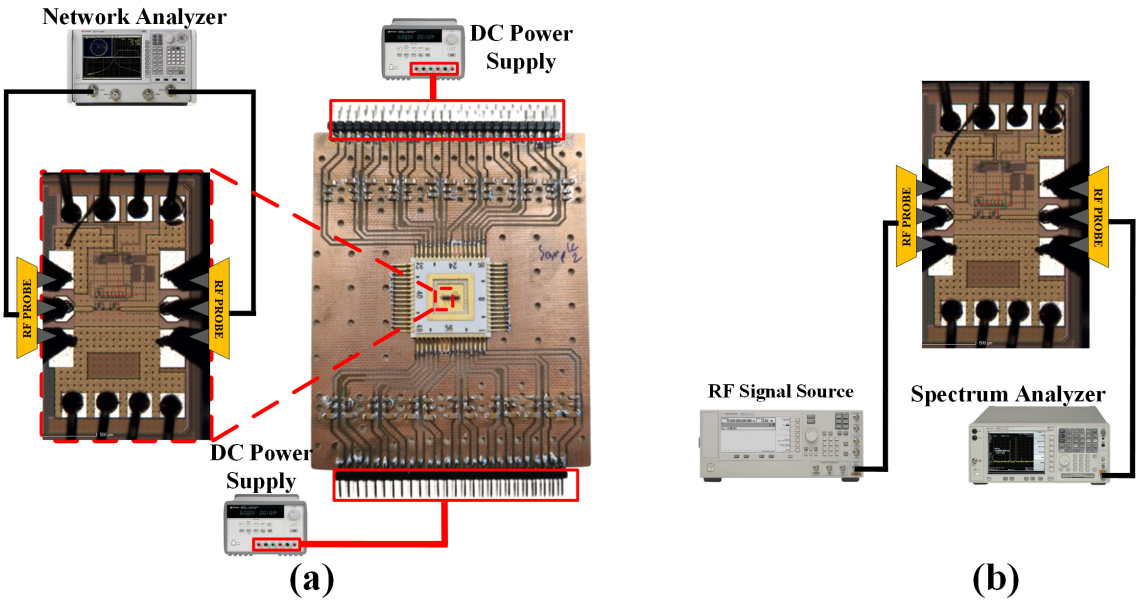

Figure 3.19 The measurement setups of VVA: (a) S-parameter and (b) IP_{1dB}

the input power was set to -5 dBm for the S-parameter measurements. The attenuation was adjusted via changing V_{DD}. The S-parameters were measured between 1 GHz and 34 GHz with 0.5 dB attenuation steps. The S-parameter measurement

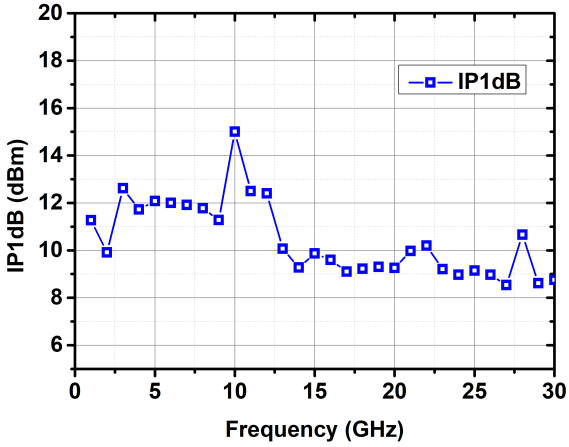

Figure 3.20 The linearity measurements of VVA

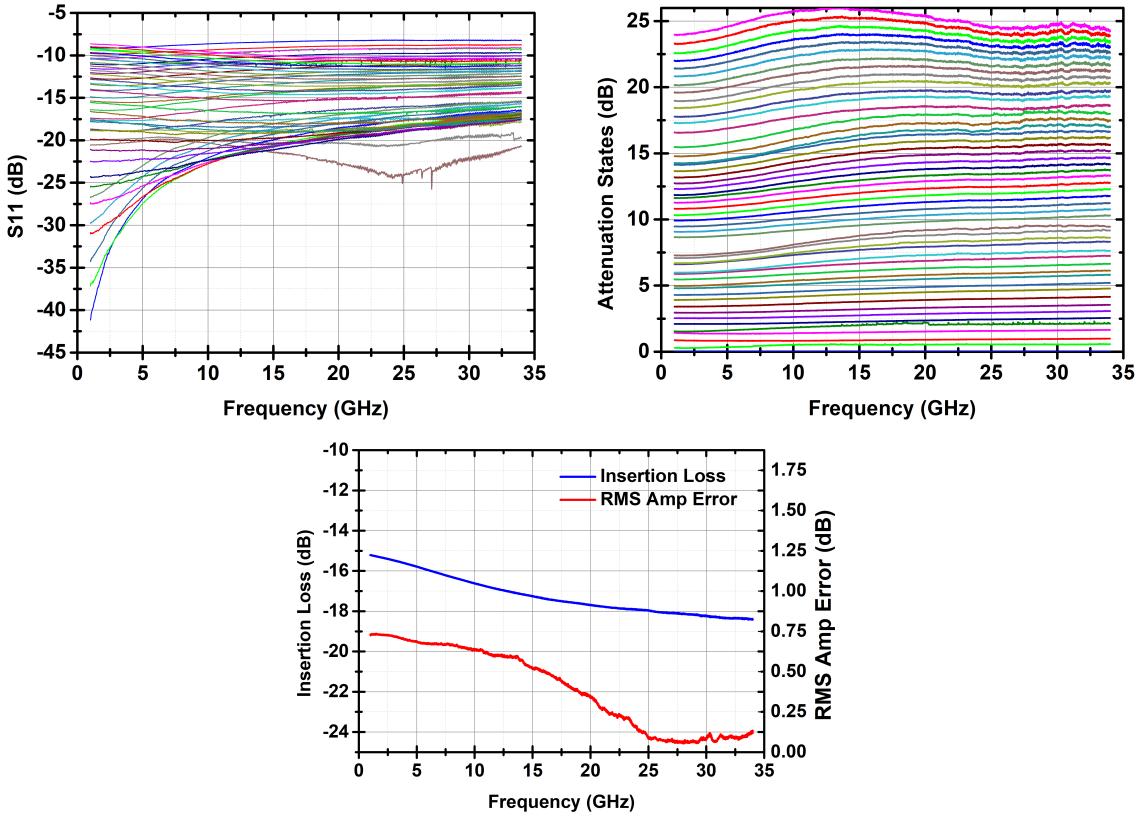

Figure 3.21 The S-parameter measurement results of VVA

results are presented in Fig. 3.21. The VVA has a minimum insertion loss of 15 dB, which is 14 dB higher than the simulations. The VVA achieves a 23 dB attenuation range with a 0.5 dB amplitude step. The RMS amplitude error is lower than 0.5 dB between 15 GHz and 35 GHz.

3.1.3.3 Power Combiner Design

Each I/Q signal generated by QAF goes through a VVA to change the amplitude of the signal. After weighting, two I/Q signals must be summed in the final stage to obtain the target phase shift. One option to combine weighted I/Q signals is a T-junction, which is basically a direct connection between four signals. Low isolation between ports of a T-junction leads to low output impedance. Also, due to low isolation, VVAs load each other and affect each other's attenuation slightly. Thus, the phase shift deviates from the target. To overcome the isolation problem, a Wilkinson power combiner is chosen in the summation network. Multi-section Wilkinson power combiners are promising for wideband operations (Hu et al., 2023). The disadvantage of the multi-section Wilkinson power combiner is large-area occupation due to multiple $\lambda/4$ transmission lines. To reduce the area, T-coils are utilized instead of quarter-wave transmission lines (Lin & Lee, 2012). The schematic of the T-coil-based multi-section Wilkinson power combiner is shown in Fig. 3.22

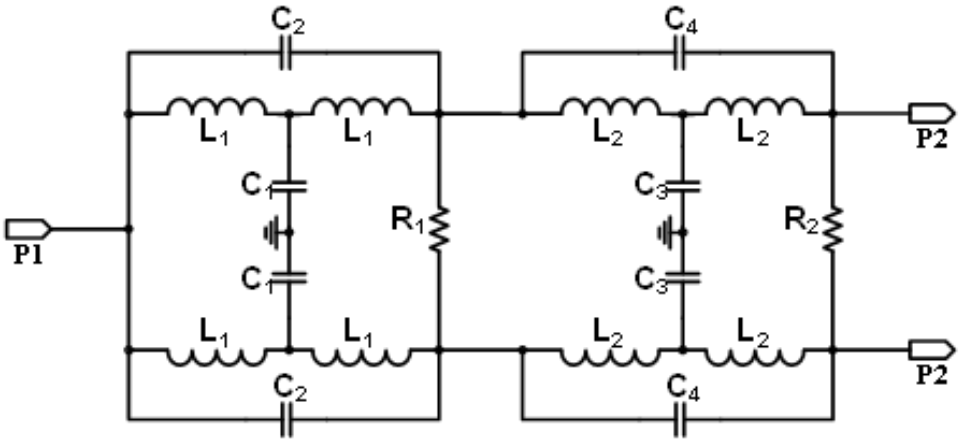

Figure 3.22 The schematic of power combiner

Simulation results are presented in Fig. 3.23. Simulation results indicate that all three ports have return losses better than 10 dB in the 3 - 30 GHz bandwidth. Amplitude imbalance is lower than 1 dB up to 20 GHz, while insertion loss is lower than 4.5 dB.

3.1.3.4 Measurement Results of The Phase Shifter

Pad-to-pad measurements setup for S-parameter measurements is shown in Fig. 3.24. During the S-parameter measurements, a Keysight N5224A network analyzer was utilized with the 100-μm Picoprobe GSG RF probes. In order to move the reference planes to the probe tips, short-open-load-thru (SOLT) calibration was performed using the Picoprobe CS-5 substrate calibration kit.

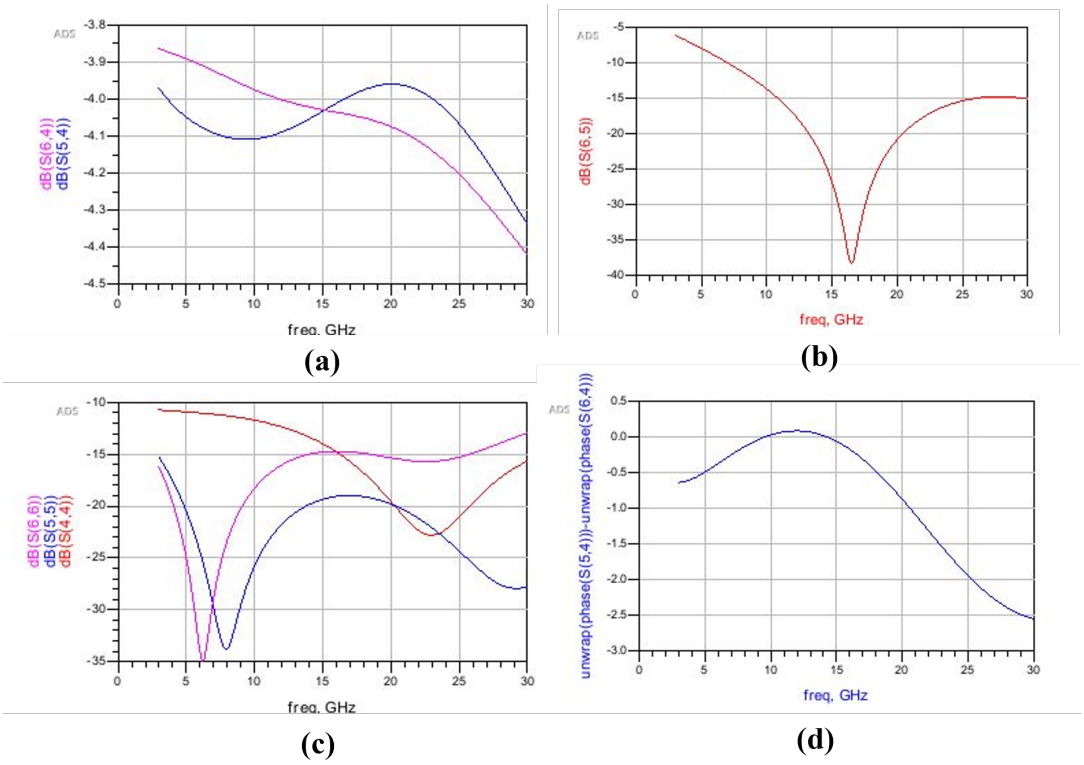

Figure 3.23 The simulation results of power combiner. (a) insertion loss (b) isolation (c) return losses (d) amplitude imbalance

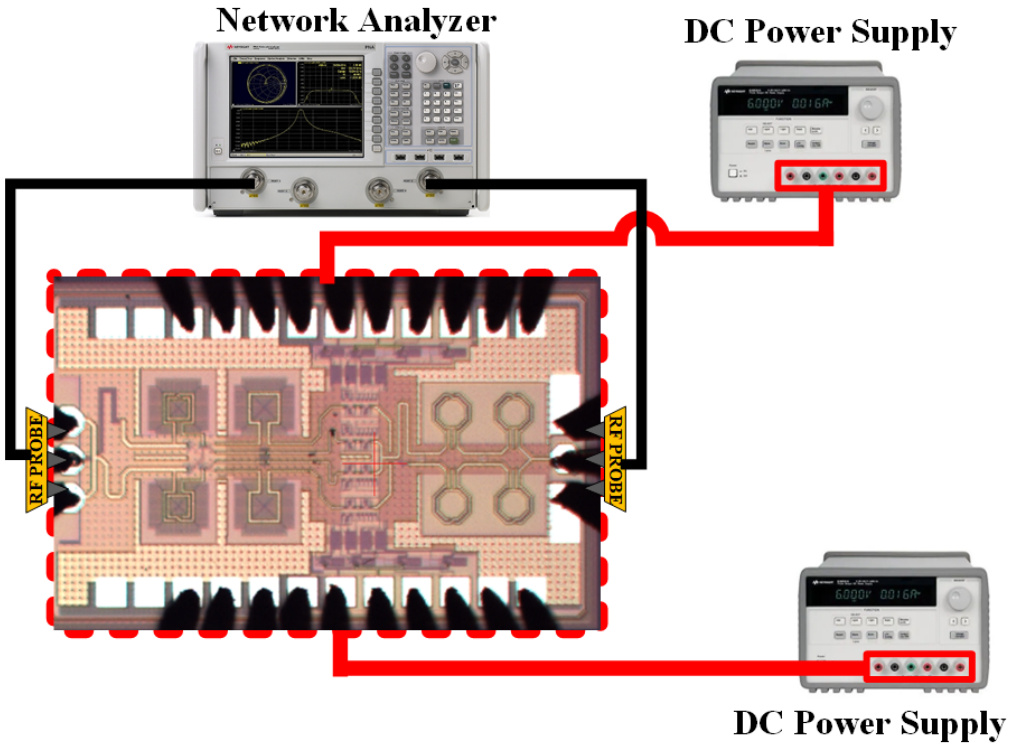

Figure 3.24 The measurement setup of the designed phase shifter with QAF

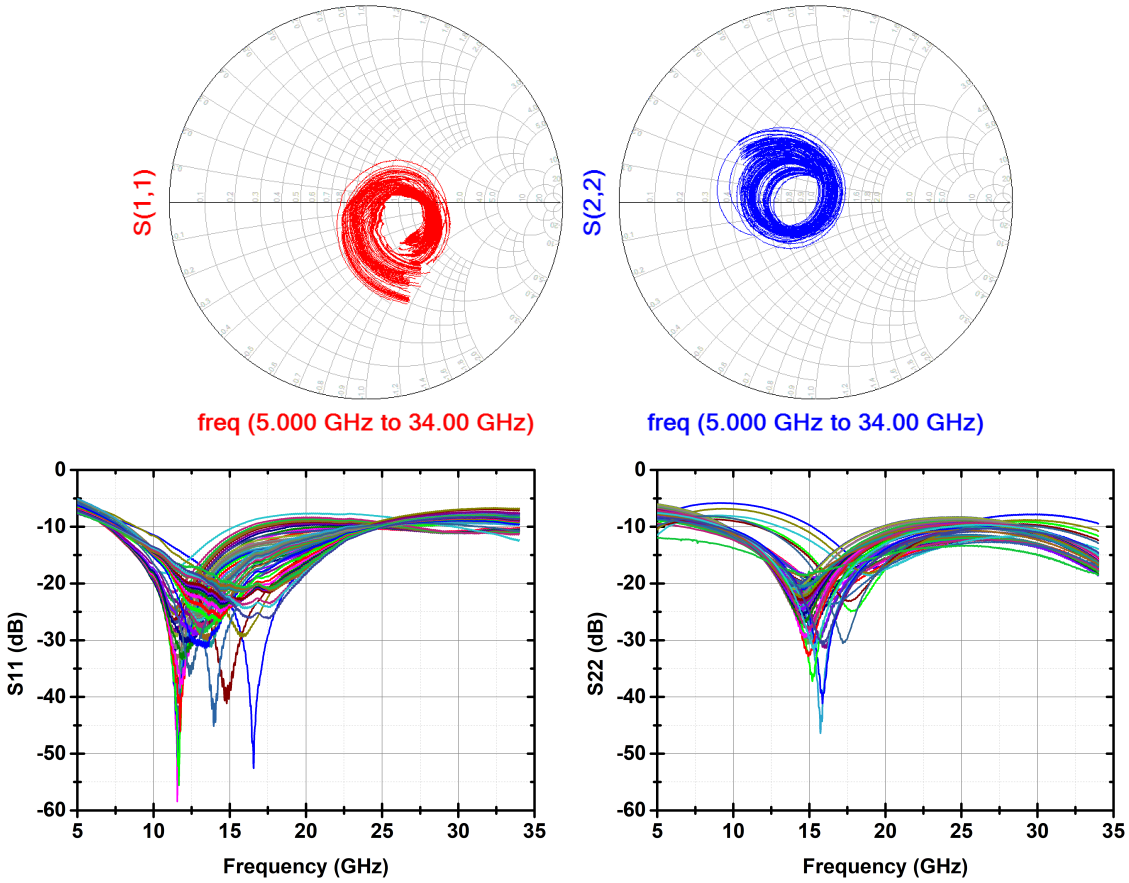

Figure 3.25 The input and output matchings of phase shifter

In order not to cause gain compression in the S-parameter measurements of the phase shifter, the input power was set to -5 dBm for the S-parameter measurements. The target phase state was adjusted via $V_{control}$ supply of the necessary $I_{+/-}/Q_{+/-}$ paths. For instance, -45° phase state can be obtained by adjusting the $V_{control}$ of the attenuators on the I_+ and Q_- paths. The S-parameter measurements were taken to lower phase error at different frequencies to widen the phase-control bandwidth as shown in Fig. 3.25.

The S-parameters were measured between 5 GHz and 34 GHz with 5.625° phase steps. The input and output matching measurement results are presented in Fig. 3.25. Excluding a few states, both input and output matchings are better than -10 dB in the frequency of interest. The phase states are demonstrated in Fig. 3.26. Fig. 3.27 demonstrates the rms phase error for the three sets of selected states; ie, one set is selected to lower the rms phase error at 8 GHz, the another one is for 15 GHz, and the last one is for 22 GHz. The phase shifter achieves a 360° phase span with 6-bit phase resolution between 5.7 and 25 GHz. The RMS phase error is lower than 6° between 5.7 GHz and 25 GHz. Fig. 3.28 shows the amplitude response of the phase shifter for different states across the frequency band. The phase shifter

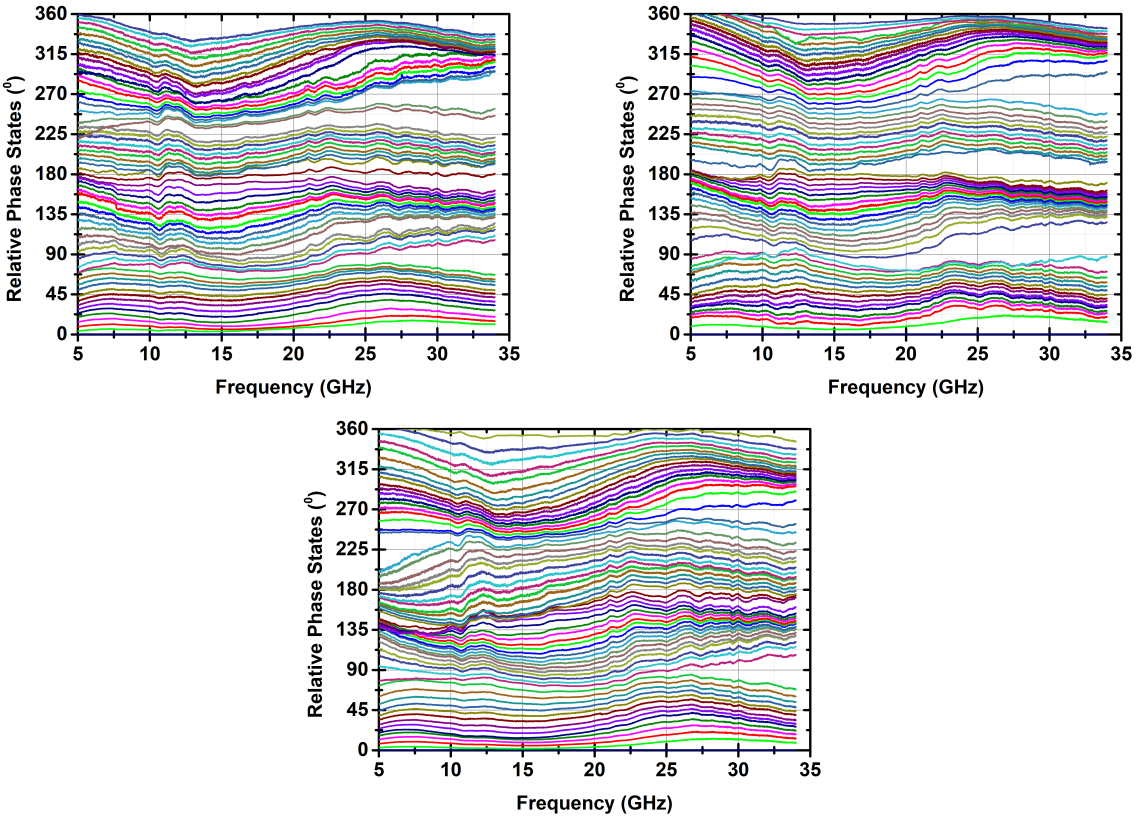

Figure 3.26 The relative phase states of the quadrature based phase shifter selected for different center frequencies: 8 GHz (top left), 15 GHz (right top) and 22 GHz (bottom)

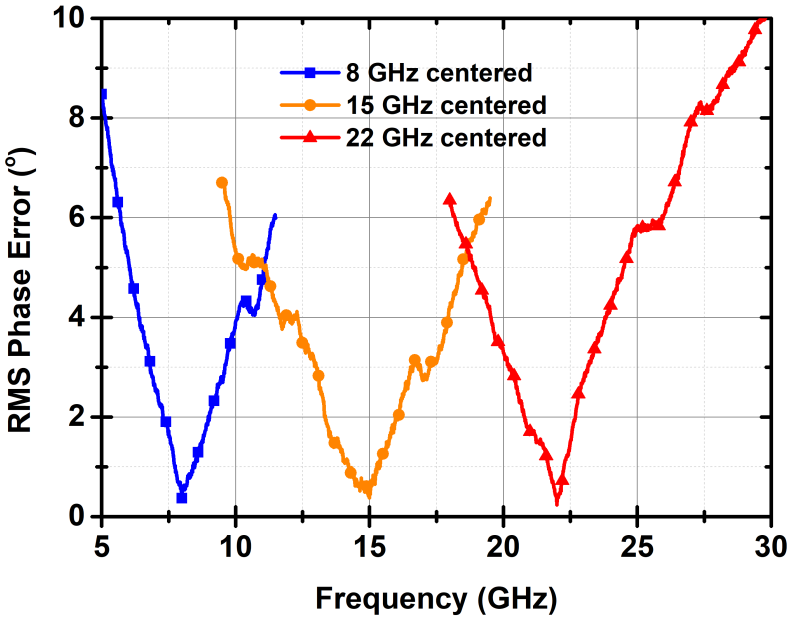

Figure 3.27 RMS phase error of the quadrature based phase shifter

has an average insertion loss of 29 dB due to increased insertion loss of VVA.

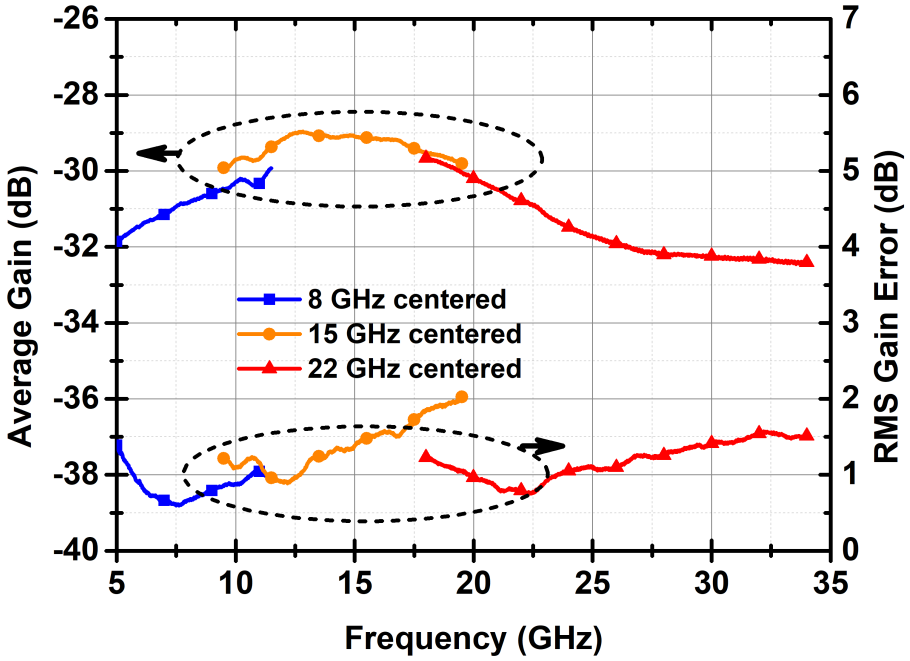

Figure 3.28 The amplitude response of the quadrature based phase shifter

3.1.4 Receiver Measurements

The designed LNA and phase shifter combined with the order in Fig. 3.1. The LNA is responsible for increasing amplitude of the received signal by adding minimal noise whereas the phase shifter inserts controlled phase shift. The receiver is realized in IHP's SG13S 0.13 μm SiGe BiCMOS technology. The die photo of the receiver is shown in Fig. 3.29. The receiver occupies 2.16 mm^2 (2.55 mm $\times$ 0.85 mm), including pads. The receiver die is packaged via bond-wires to carrier. The receiver draws 29 mA current from 2.3 V, consuming a DC power of 66 mW. NF, IP_{1dB}, phase response, IIP3 and gain are significant parameters for the receiver.

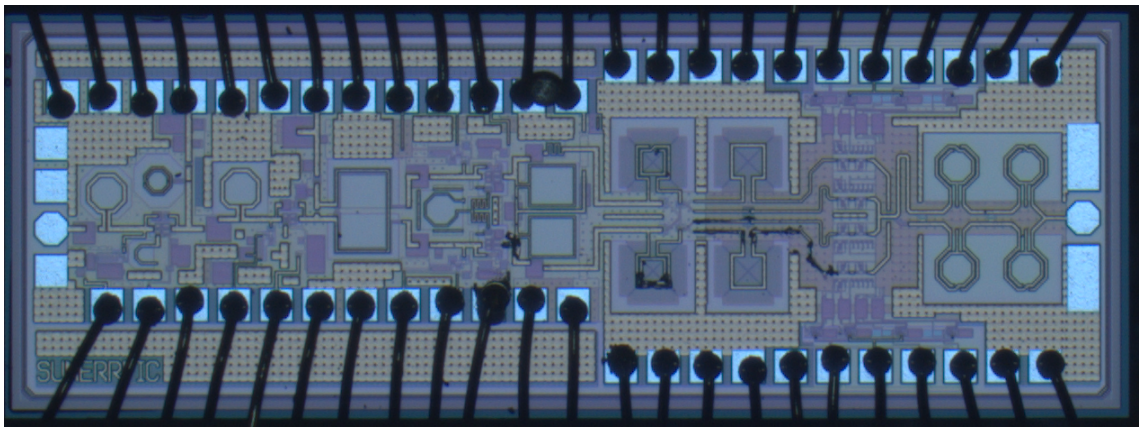

Figure 3.29 The micrograph of the receiver

Pad-to-pad measurements setup for S-parameter measurements are similar to phase

shifter or LNA measurement setup. During the S-parameter measurements, a Keysight N5224A network analyzer was utilized with the 100-μm Picoprobe GSG RF probes. SOLT calibration was performed using the Picoprobe CS-5 substrate calibration kit. In order not to cause gain compression in the S-parameter measurements of the phase shifter, the input power was set to -45 dBm for the S-parameter measurements. The target phase state was adjusted via $V_{control}$ supply of the necessary $I_{+/-}/Q_{+/-}$ paths. For instance, -45° phase state can be obtained by adjusting the $V_{control}$ of the attenuators on the I_+ and Q_- paths. The S-parameter measurements were taken to lower phase error at different frequencies to widen the phase-control bandwidth as shown in Fig. 3.30. The measurement results show that 3-dB bandwidth of the receiver is 18.36 GHz, from 6.84 GHz to 25.2 GHz. The measured peak gain is -2.1 dB at 12.2 GHz.

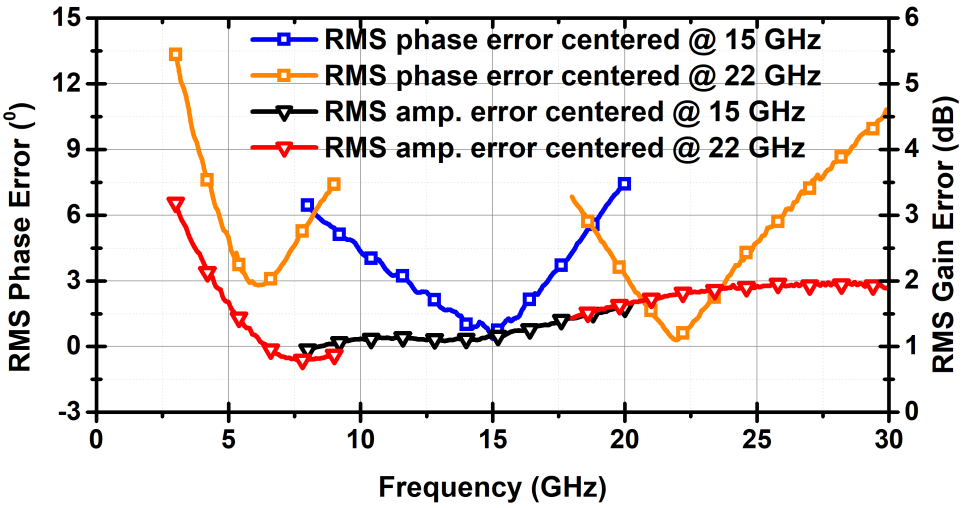

Figure 3.30 RMS gain and phase errors of the receiver

Pad-to-pad measurement setups for linearity and NF measurements are similar to LNA measurement setup. The linearity performance of the fabricated chips was characterized using 100-μm Picoprobe GSG RF probes, using a Keysight E8257D and E8567D signal generators, and a Keysight E4448A spectrum analyzer. Measured thru-cable losses are excluded from the results. The results of the NF measurements are presented in Fig. 3.31. Linearity measurement results for different auxiliary voltage of the post-distortion circuit, also shown in Fig. 3.32 and Fig. 3.33, indicate that the receiver with post-distortion achieves the maximum IP_{1dB} of -23.4 dBm at 23 GHz, compared to -24.9 dBm for the receiver without post-distortion at the same frequency—representing a 1.5 dB improvement. The maximum difference in IP_{1dB} between with and without post-distortion is obtained as 6 dB at 16 GHz. IIP3 measurements reveal that the post-distortion technique enhances IIP3 from -22 dBm to -19.8, corresponding to a 2.2 dB improvement. Overall, the measurement results are confirming that the post-distortion method effectively improves the linearity

performance of the receiver.

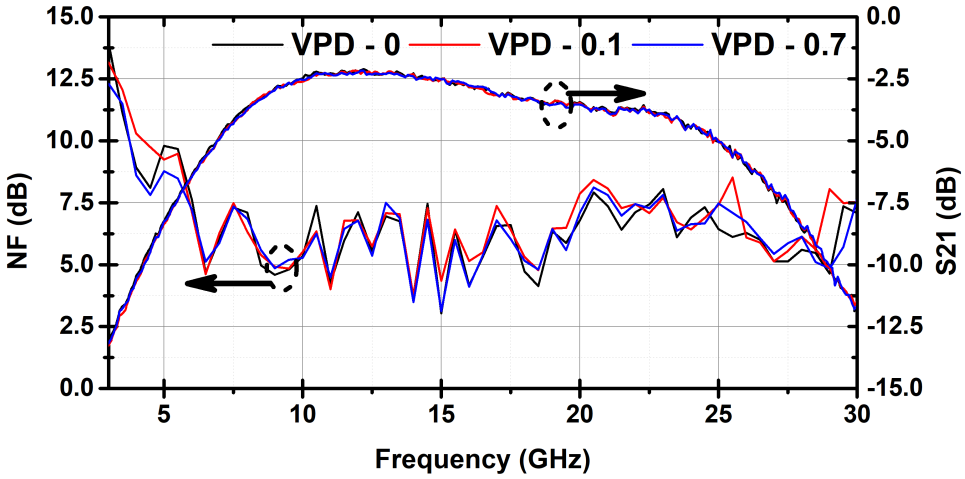

Figure 3.31 The NF and gain performance of the receiver

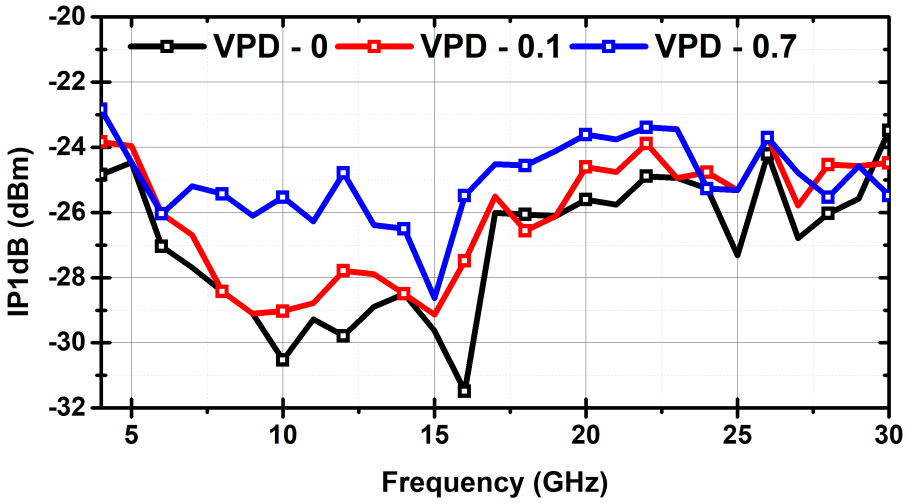

Figure 3.32 The IP_{1dB} of the receiver

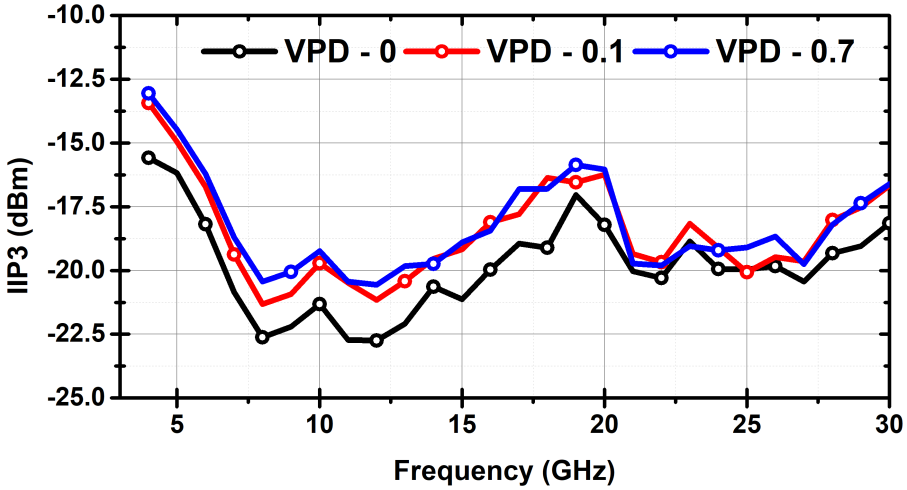

Figure 3.33 The IIP3 of the receiver

3.2 A Wideband Single-Channel Receiver Front-End For

C/X/Ku/Ka-Band SATCOM System

The implemented first receiver operates over a 3-dB bandwidth of 8–29 GHz. The phase control mechanism provides a 6-bit resolution across this frequency range. The use of analog control in the phase shifter enables broader phase control bandwidth by allowing different phase states to be optimized for distinct frequency sub-bands. Since a digital control is demanded for a phase shifter in a system-level operation, it would be beneficial to improve the phase control bandwidth of the phase shifter.

Additionally, as indicated by (3.1), the insertion loss of the phase shifter contributes significantly to the overall NF of the receiver. Due to the relatively high loss introduced by the phase shifter, the gain provided by the LNA is insufficient to adequately suppress its noise contribution. This highlights the need for further optimization to reduce the insertion loss of the phase shifter. In parallel, increasing the gain of the LNA would also be beneficial in minimizing the overall system NF. Finally, the inclusion of an amplitude control block is essential for suppressing SLL in phased array systems, which is a critical requirement for maintaining radiation pattern integrity.

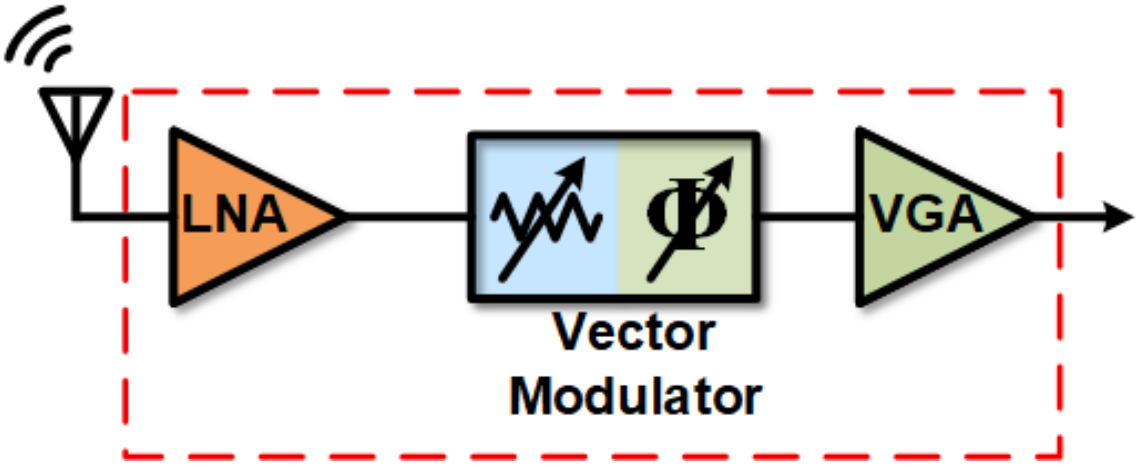

Figure 3.34 The block diagram of the second receiver chain

To improve gain, NF, phase error bandwidth, and include an amplitude control block, another receiver has been designed with improved sub-blocks. The second receiver is shown in Fig. 3.34, including a VGA as an amplitude control block. With the addition of VGA, the total gain of the receiver increased. LNA is based on the same topology, a three-stage cascode topology. After the second stage of the LNA, a passive balun divides the input signal into two differential signals. As a result, the third stage is differentially designed. In the phase shifter architecture, the I/Q network in the phase shifter is reworked to improve phase error and loss. Since

high-attenuation states vary with the frequency, an attenuation flatness circuit is implemented in the vector weighting part. Utilizing the proposed close-loop VVA, the phase shifter can provide the both attenuation and phase control functionality. Finally, the analog control of the phase shifter is changed to digital control by employing a serial-to-parallel interface (SPI) and a voltage digital-to-analog converter.

The ordering of blocks in the second receiver chain is determined based on the NF and linearity performance requirements of the overall receiver. The LNA is positioned as the first block to minimize the impact of noise introduced by subsequent stages, as it provides the lowest NF in the chain. If a VGA were placed as the second stage, the IP_{1dB} of the receiver would be limited to approximately -40 dBm, thereby significantly reducing the receiver's dynamic range. To avoid this limitation, a phase shifter is selected as the second block in the chain, preserving both linearity and dynamic range.

3.2.1 Low Noise Amplifier

As previously discussed, the LNA is one of the most critical components in the receiver chain. Being the first sub-block, the LNA's noise contribution is directly added to the overall system noise factor, making it a key determinant of the receiver's noise performance. As such, the LNA plays a pivotal role in enabling low-noise operation. Furthermore, serving as the primary gain stage, the LNA amplifies the weak signal received from the antenna to compensate for losses introduced by subsequent components such as attenuators and phase shifters.

While the noise figure of the LNA critically influences the minimum detectable signal level of the receiver, its linearity performance determines the upper limit of the acceptable input power level. Therefore, to maintain both sensitivity and dynamic range, the LNA must exhibit not only low noise but also high linearity.

In consideration of the insertion loss introduced by the phase shifter in the preceding receiver stage, the LNA is designed to achieve a gain exceeding 25 dB, while maintaining the NF as low as possible. To meet the high gain requirement, a three-stage LNA architecture is adopted. Since the CE topology is insufficient for achieving both high gain and stability, each stage is implemented using a cascode configuration.

Another critical design parameter is bandwidth. Staggered tuning is an effective technique for multi-stage amplifiers, wherein the gain peaks of individual stages are intentionally offset in frequency to achieve a broader bandwidth. This approach en-

ables the amplifier to maintain a relatively uniform gain across the desired frequency range. However, it often results in degraded noise performance over frequency (Hu et al., 2024). To address this limitation, RC feedback and series R–L load techniques are employed to maintain high gain within the targeted frequency band while preserving acceptable noise characteristics.

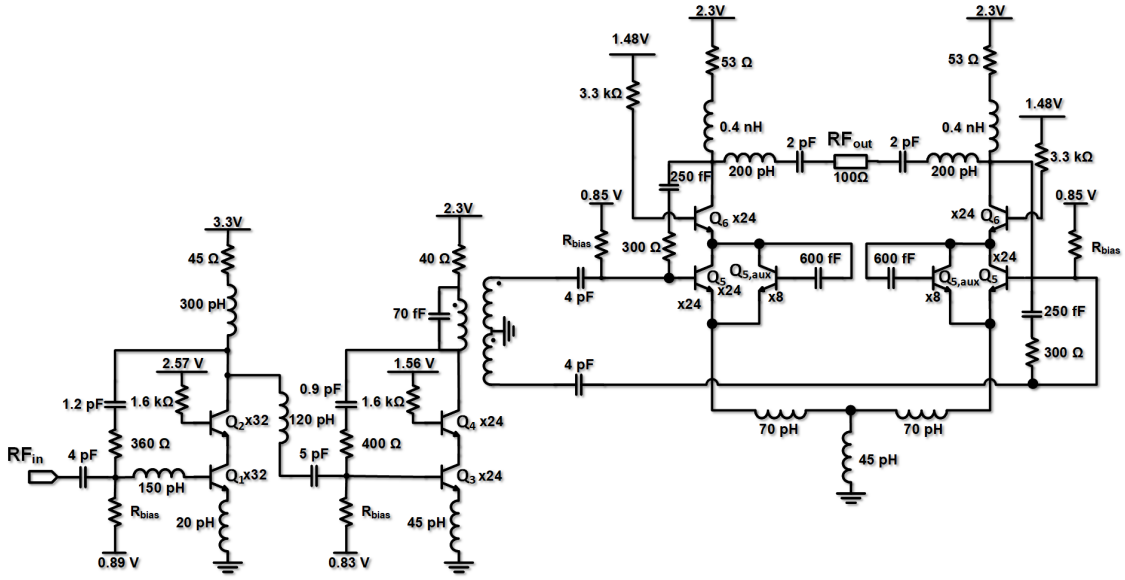

Figure 3.35 The schematic of the designed LNA

In the first two stages, the simultaneous noise and power matching technique is employed to achieve a NF close to the minimum noise figure, NF_{min}. This approach begins with determining the collector current density of the transistors to minimize NF_{min}. Once the optimal current density is selected, the transistors are appropriately sized to ensure that the optimum source resistance for noise matching corresponds to 50 Ω. Emitter degeneration inductance is introduced to adjust the real part of the input impedance to match 50 Ω. Additionally, RC feedback and series R–L load networks are incorporated into both the input and output matching networks to enhance bandwidth, ensuring wideband performance. Lastly, similar to previously designed LNA, the last stage employs the diode-connected post-distortion method. The post-distortion circuitry is turned on by biasing the auxiliary devices. The schematic of the designed LNA is shown in Fig. 3.35. Fig. 3.36 presents the layout of the LNA taped-out.

The post-layout electromagnetic simulations of designed LNA were conducted in Keysight ADS Momentum. The LNA was realized with contributions from M. Kaan Lermi. The layout occupies an area of 0.78 mm^2 (1.58 mm × 0.49 mm), and the DC power consumption is 63.4 mW.

Fig. 3.37 presents the input and output matching characteristics when the post-

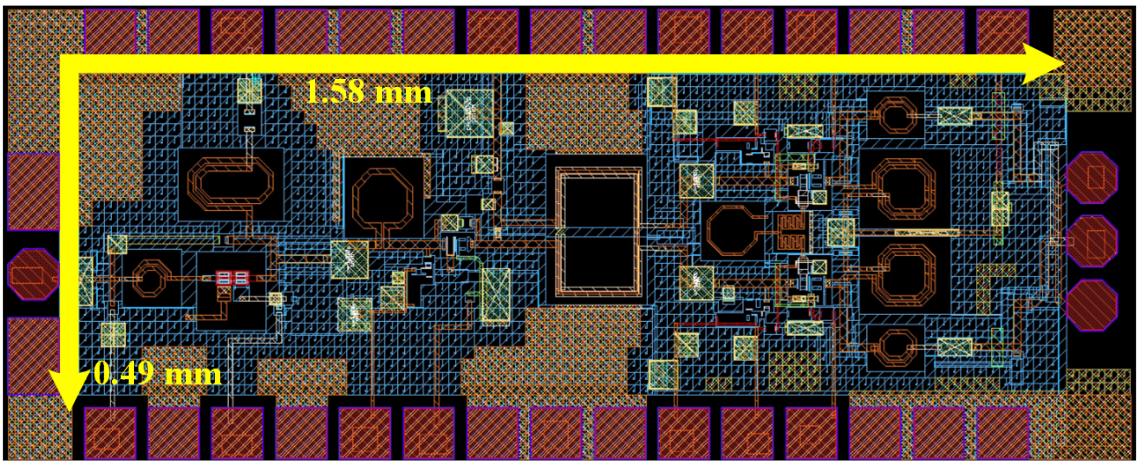

Figure 3.36 The layout of the designed LNA

distortion circuitry is activated. The input return loss remains above 10 dB over the 1.3–35 GHz range for both configurations. The output return loss is above 10 dB from 2.3 GHz to 26.5 GHz. Simulated K-factor results in Fig. 3.38 show that the LNA is unconditionally stable in the frequency of interest.

Fig. 3.39 illustrates the gain and NF performance. The amplifier achieves a peak gain of 30.5 dB, with a 3-dB bandwidth extending from 6.2 GHz to 29.1 GHz. The simulation results indicate that a minimum NF of 2.2 dB is observed at 5.5 GHz. The NF of the LNA is below 3.1 dB in the 3-dB bandwidth.

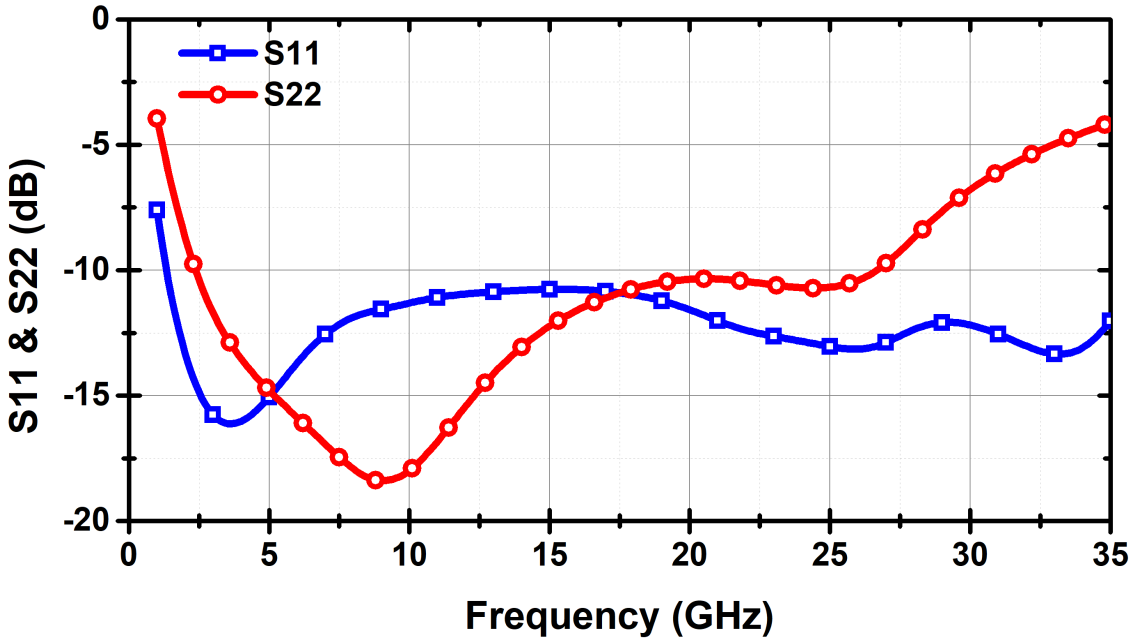

Figure 3.37 The input and output matchings of the designed LNA

The simulated IP_{1dB} and IIP3 for the LNA with and without the post-distortion technique are presented in Fig. 3.40. The results indicate that, when post-distortion

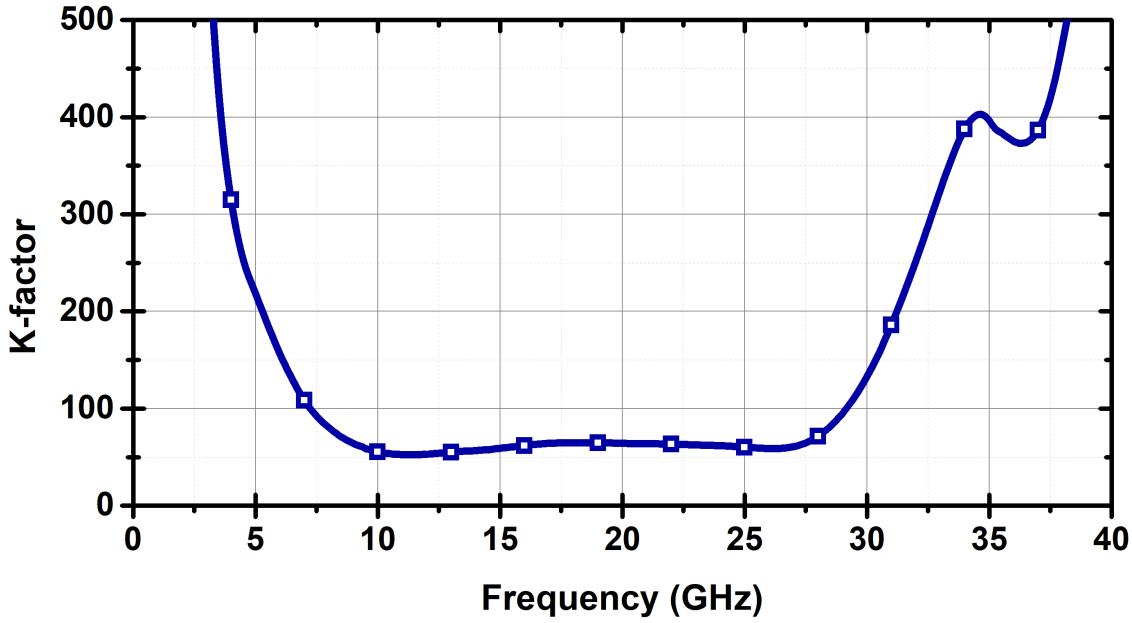

Figure 3.38 Simulated K-factor results for the stability of the LNA

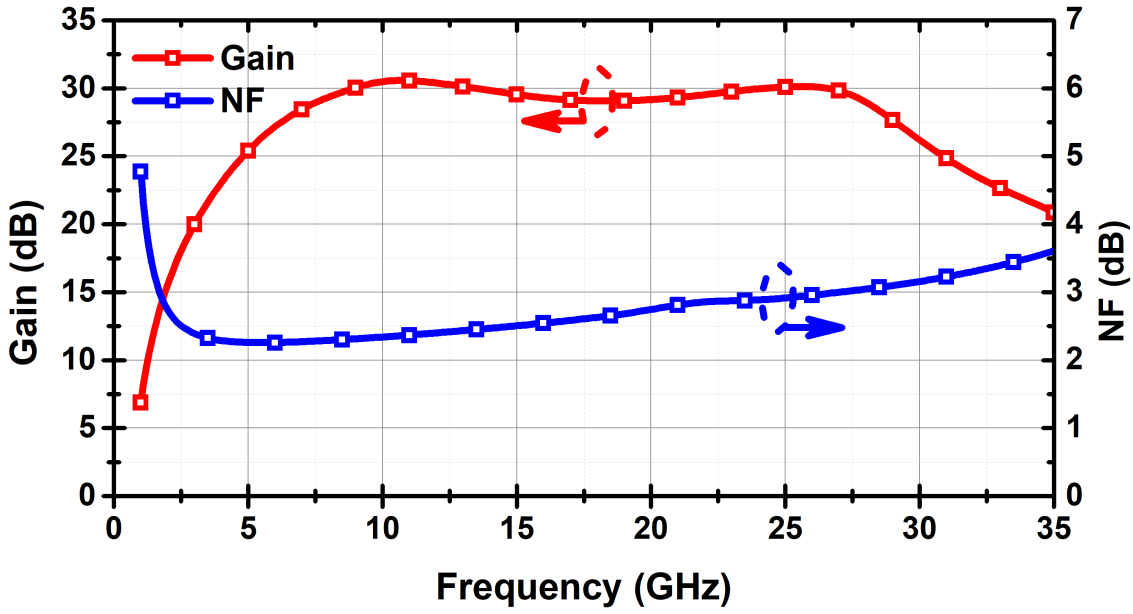

Figure 3.39 The gain and NF performance of the designed LNA

is employed, the IP_{1dB} varies between -35 dBm and -20 dBm across the operating bandwidth. In contrast, without post-distortion, the IP_{1dB} ranges from -36 dBm to -25 dBm. Within the 3-dB bandwidth, the maximum IIP3 reaches -15.5 dBm with post-distortion, compared to -19.5 dBm without post-distortion.

3.2.2 Passive Vector-Sum Phase Shifter

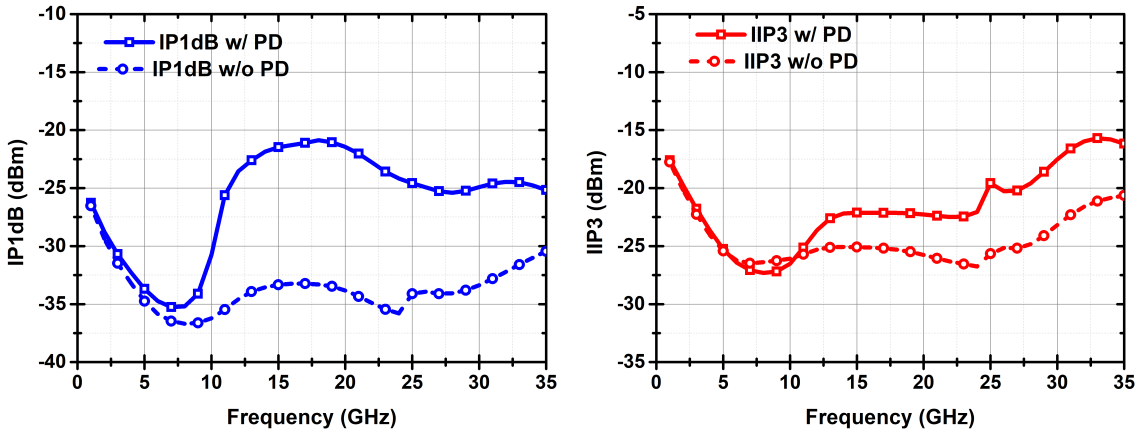

Figure 3.40 The IP_{1dB} (left) and IIP3 (right) of the designed LNA

The phase shifter in the first receiver employs a QAF as an I/Q generation network. The QAF network was chosen since it performs lower loss than 2^{nd}-order PPF, which has similar phase variation to QAF. However, the QAF network's amplitude error limits the operation bandwidth. The loss of the phase shifter should be reduced to lower the overall NF of the receiver. Considering the measurement results, the phase shifter was planned to be redesigned with the same passive vector-sum architecture. The schematic of the designed coupler based phase shifter is depicted in Fig.3.41.

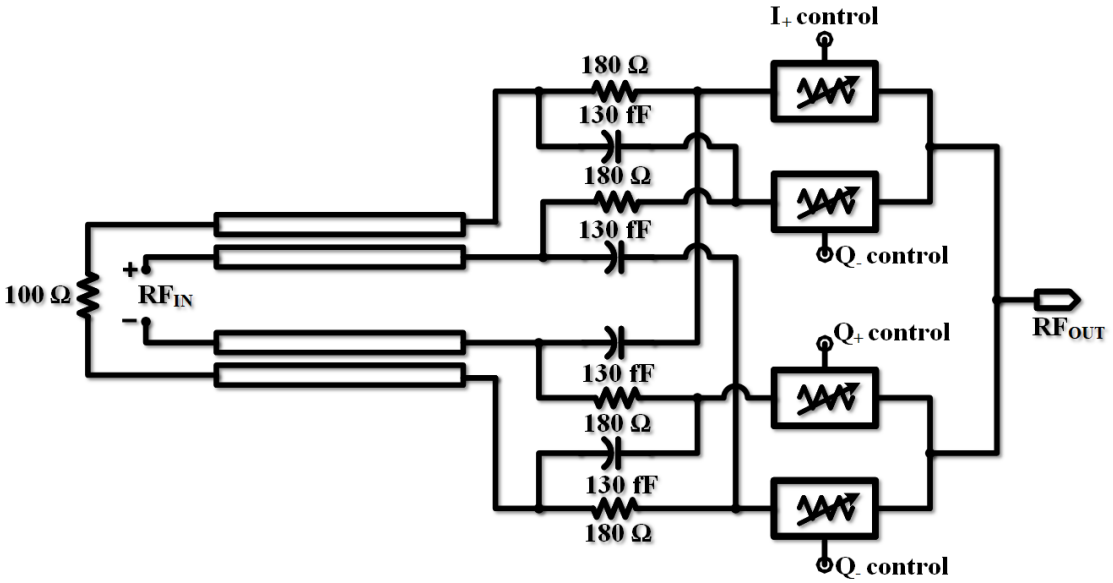

Figure 3.41 The schematic of the designed coupler based phase shifter

There have been various methods to generate I/Q signals in literature (Hu et al., 2024; Kalyoncu, Burak, Kaynak & Gurbuz, 2019; Kulkarni et al., 2013). PPF and QAF were discussed in the previous sections. Another method used for I/Q generation is a lumped component implementation of coupler (Frye, Kapur & Melville, 2003). In this work, a quadrature hybrid coupler was modeled with lumped com-

ponents to reduce the area of the coupler. Another advantage of this topology is lower loss. However, this area and loss reduction has a drawback of higher phase and amplitude error in a wide bandwidth. (Qunaj & Reynaert, 2021) employs a quadrature hybrid coupler to achieve low phase error in a wideband. Therefore, a quadrature hybrid coupler is employed in this phase shifter design. The designed quadrature hybrid coupler achieves excellent phase response and matching over an approximately 100% fractional bandwidth. Since the target SATCOM bands require more than the bandwidth of coupler, an RC-PPF is cascaded to further enlarge the bandwidth. The 3D view, and the phase and amplitude error of I/Q generation network are depicted in Fig. 3.42. I/Q network achieves ±2° phase error within the frequemcy band.

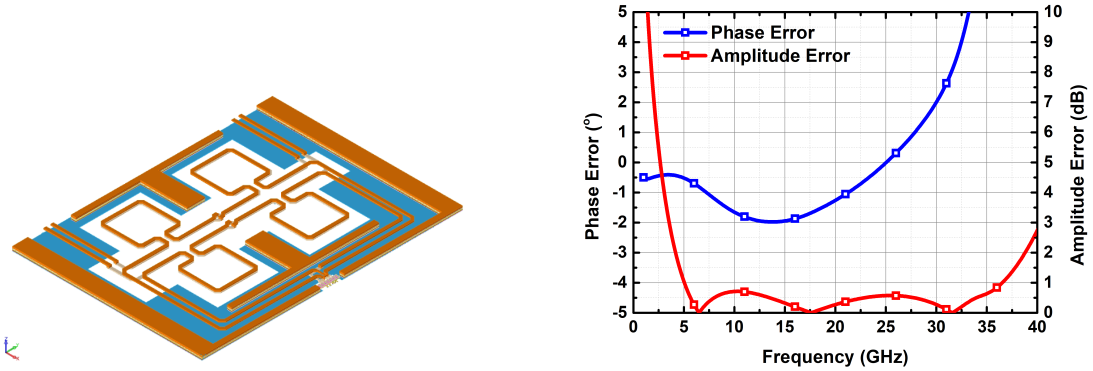

Figure 3.42 The 3D view (left), and the phase and amplitude errors (right) of I/Q generation network

3.2.2.1 VVA and Attenuation Flatness Circuitry

The design of the VVA was discussed in Section 3.1.3.2. To reduce insertion loss, the architecture was reduced to a single T-type VVA configuration, rather than cascading two VVA stages. Additionally, the sizes of the series transistors were increased to 100 μm to further minimize loss. To extend the control voltage range, a single MOS transistor—sized at 100 μm width and 0.65 μm length—is incorporated into the attenuation loop, along with a 1 kΩ comparison resistor.

In the T-type VVA, high attenuation states make series devices get close to the off-state. This leads to a change in the input impedance and degrades the phase and amplitude of the I/Q signals. To prevent this degradation in the input impedance of the VVA, another two-stack shunt devices are implemented at the input side. In this way, VVA can present 50 Ω in high attenuation states, too. The schematic of

the designed VVA is depicted in Fig. 3.43.

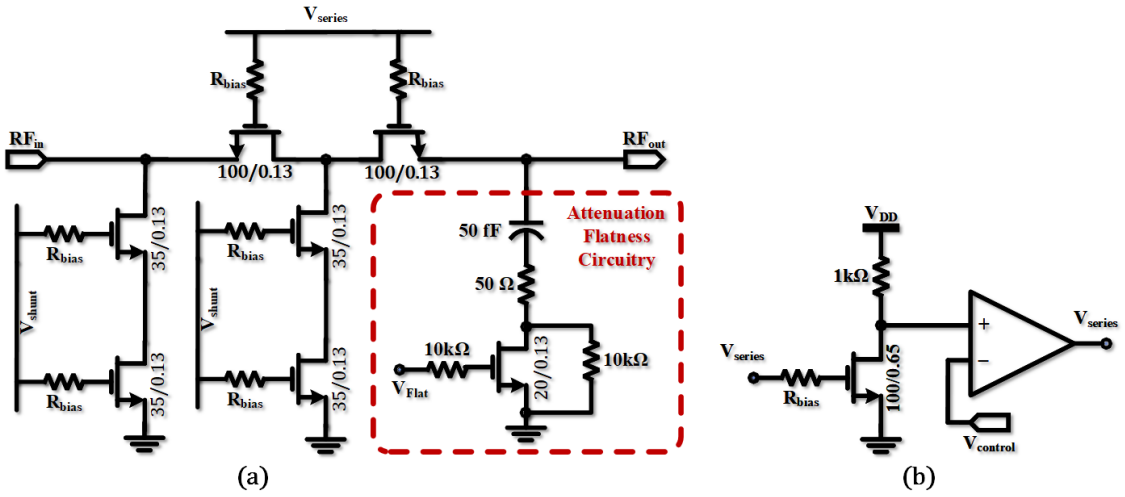

Figure 3.43 The schematic of the designed VVA: (a) VVA core, (b) attenuation loop

Another key point in a VVA is that the attenuation decreases as the frequency increases since the off-state capacitance becomes more effective than the off-state resistance. (Zhang, Li, Gao, Li, Wang, Kuan, Song, Yu, Gu & Xu, 2021) utilizes a capacitive compensation method to generate poles and zeros to cancel out existing poles. In our VVA design, a series RC network with a switch is inserted as a shunt component. As the attenuation increases, the switch will be turned on by an external control. In this way, the decrease in the loss with the increased frequency will be canceled out with the additional circuitry. The effect of the attenuation compensation circuitry on the 23-dB attenuation state is illustrated in Fig. 3.44. The reference state has a decreasing behavior, but 23 dB attenuation state has the opposite. When the switch in the compensation circuitry is turned on, more flat attenuation response can be obtained. As a results, the amplitude error is reduced.

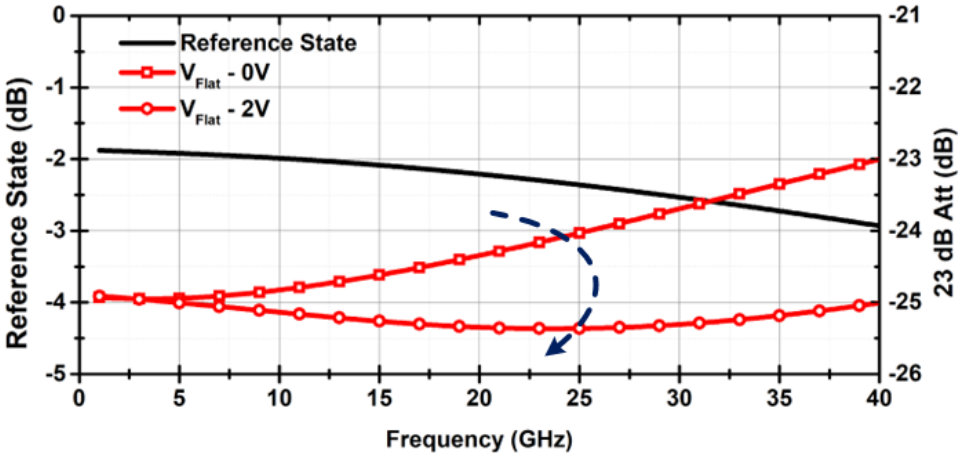

Figure 3.44 The effect of the attenuation compensation circuitry on the 23-dB attenuation state

3.2.2.2 Voltage DAC

The previous version of the phase shifter was controlled using four analog voltages. In contrast, most phase shifters used in phased array systems operate with digital control inputs. To bridge this interface, digital control signals are converted into analog control voltages for the attenuators via two voltage DACs, one for each of the I and Q signal paths.

To enable high-precision control, a 10-bit DAC based on the R-2R ladder topology is implemented using 0.13 μm SiGe BiCMOS technology. The output of the DAC is buffered using a custom-designed Opamp to ensure drive strength and signal integrity. The schematic of the implemented DAC is shown in Fig. 3.45. Since the control voltage range of the coupler-based phase shifter extends up to 3.3 V, the DAC supply voltage V_{DD} is accordingly set to 3.3 V.

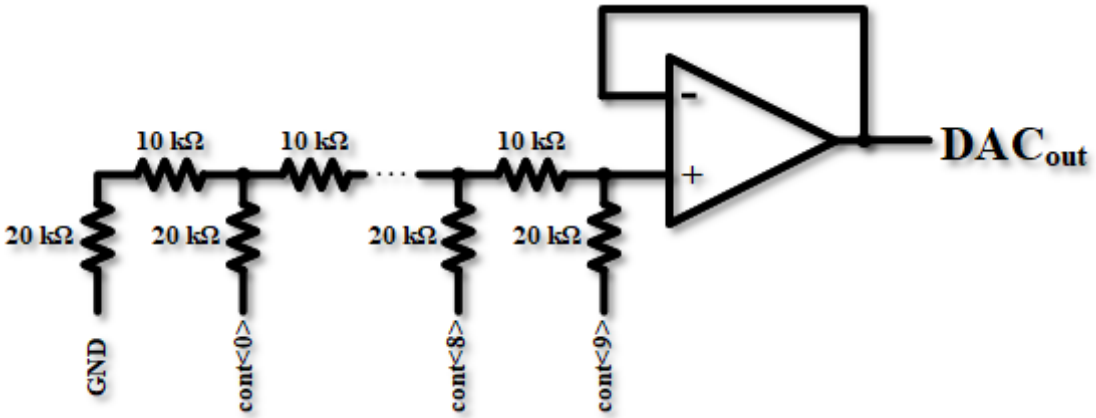

Figure 3.45 The schematic of 10-bit R-2R DAC

3.2.2.3 SPI

A digital control circuit is required to manage the 22-bit digital control inputs of the phase shifter. Without such a circuit, these 22-bit inputs would need to be provided directly through pads, significantly increasing both layout complexity and area. To address this, an SPI is implemented using IHP's 0.13 μm SiGe BiCMOS digital standard cell library. The layout of the SPI is shown in Fig. 3.46, occupying a core area of 108 μm $\times$ 50 μm.

The SPI operates using an asynchronous serial communication protocol and is triggered on the rising edge of the clock signal. The SPI interface includes data, load,

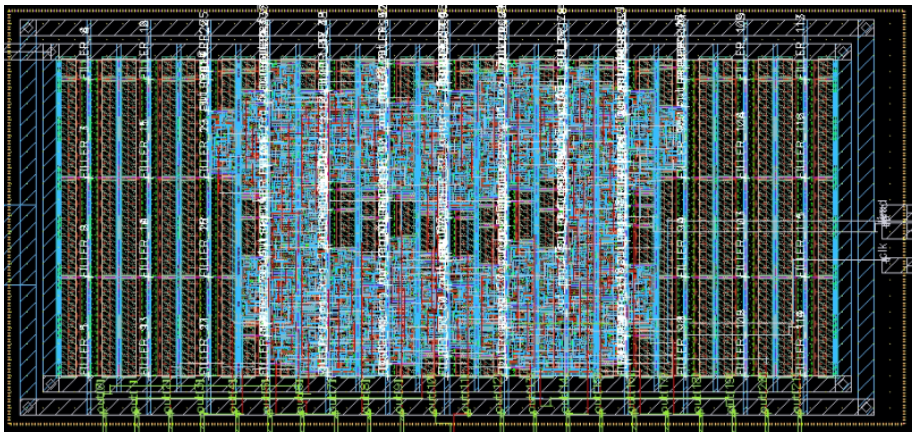

Figure 3.46 The layout of the designed SPI

clock, and reset inputs. When the load signal remains high for 22 clock cycles, the 22-bit serial data is transferred into the output registers. A timing diagram illustrating the operational behavior of the SPI is provided in Fig. 3.47.

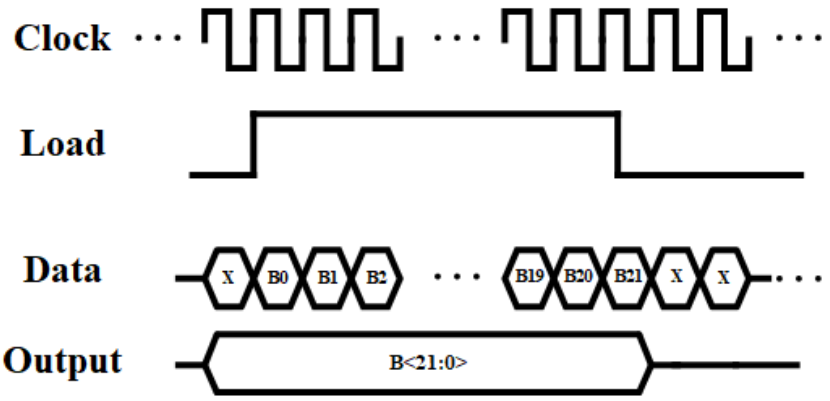

Figure 3.47 An example for SPI timing diagram

The digital standard library operates at a supply voltage of V_{DD} = 1.2 V. To accommodate 3.3 V digital input signals, level shifters—shown in Fig. 3.48 are used to convert 1.2 V logic levels to 3.3 V. The combined layout of the DAC and level shifters is presented in Fig. 3.49, occupying a core area of 104 μm × 40 μm.

Post-layout EM simulations of the designed coupler based phase shifter were performed using Keysight ADS Momentum. The layout of the phase shifter is shown in Fig. 3.50, and it occupies a core area of 0.6 mm^2 (0.78 mm × 0.78). The The DC power consumption of the control circuitry is 12 mW.

Fig. 3.51 illustrates the phase control performance with additional 10 dB attenuation control. Without attenuation, the phase shifter exhibits an average loss of 15 dB across different phase states, with a 3-dB bandwidth extending from 2.5 GHz to 32 GHz. With 10 dB attenuation, the phase shifter exhibits an average loss of 25 dB across different phase states, with a 3-dB bandwidth extending from 2.5 GHz

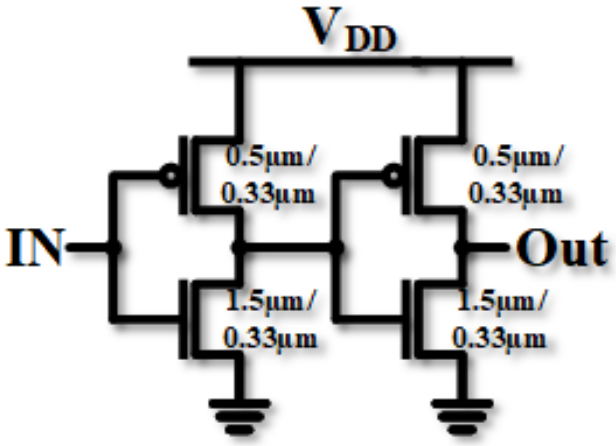

Figure 3.48 The schematic of a level shifter

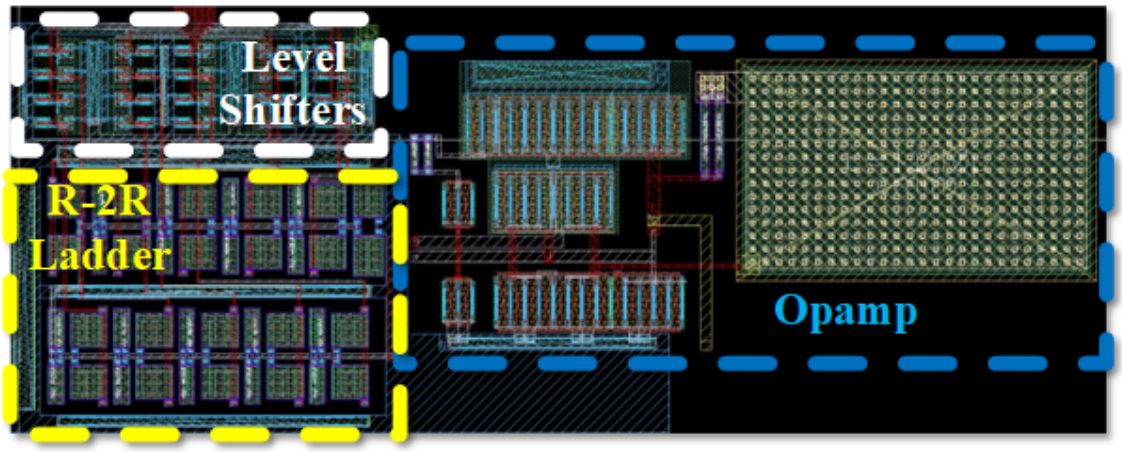

Figure 3.49 Combined layout of the DAC and level shifters

to 28 GHz. The designed phase shifter achieves a phase control range of 360° with 5.625 dB phase steps. Fig. 3.53 demonstrates RMS amplitude and phase errors with and without 10 dB attenuation. The RMS phase error is lower than 5.6° in the frequency range of 4.7-33 GHz for both cases. For the same frequency range, the RMS amplitude error is lower than 1 dB. Finally, Fig. 3.52 shows the simulated IP_{1dB} results of the phase shifter at the reference state. The phase shifter achieves the minimum IP_{1dB} of 19 dB, which showcases highly linear operation.

Table 3.2 presents a comparison between the proposed LNA and a previously reported wideband Si-based VGA designs (Calışkan et al., 2021; Gao & Zhao, 2021; Hu et al., 2024; Jung & Min, 2020). Among the referenced works, the highest gain of 1.2 dB is reported in (Hu et al., 2024) over a wide bandwidth of 5–21 GHz; however, this design exhibits higher power consumption and inferior IP_{1dB} performance. The design in (Gao & Zhao, 2021) achieves the lowest RMS phase error among the compared works but operates over a narrower bandwidth of 19–23 GHz. The proposed

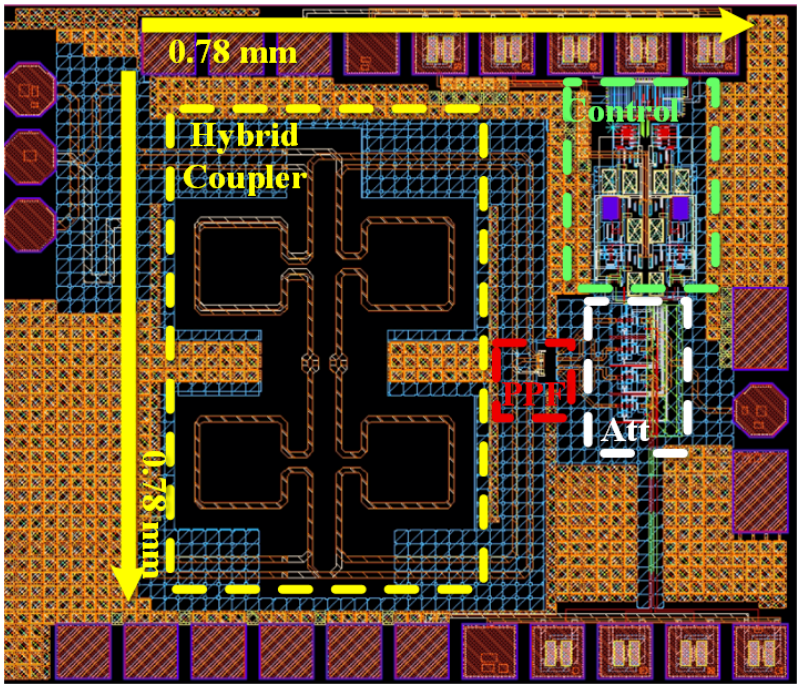

Figure 3.50 The layout of the designed coupler based phase shifter

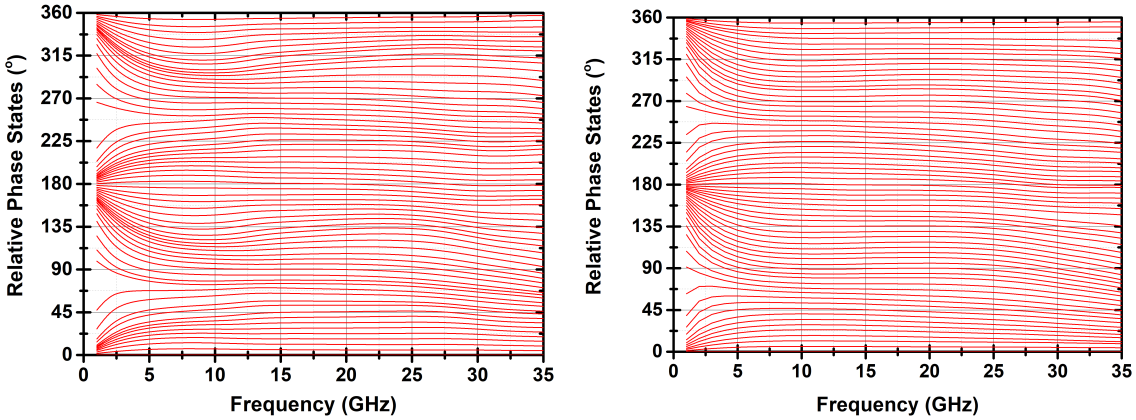

Figure 3.51 The relative phase states of the designed coupler based phase shifter at reference amplitude level (left) and with 10 dB attenuation (right)

coupler-based phase shifter offers a high IP_{1dB}, wide bandwidth, and high phase resolution. To the best of the authors' knowledge, the phase shifter achieves 6-bit phase resolution with the widest frequency range among the passive phase shifters. These advantages are attributed to its passive architecture, attenuation flatness circuitry in the proposed VVAs, and the low phase error inherent in the coupler–PPF-based I/Q generation network.

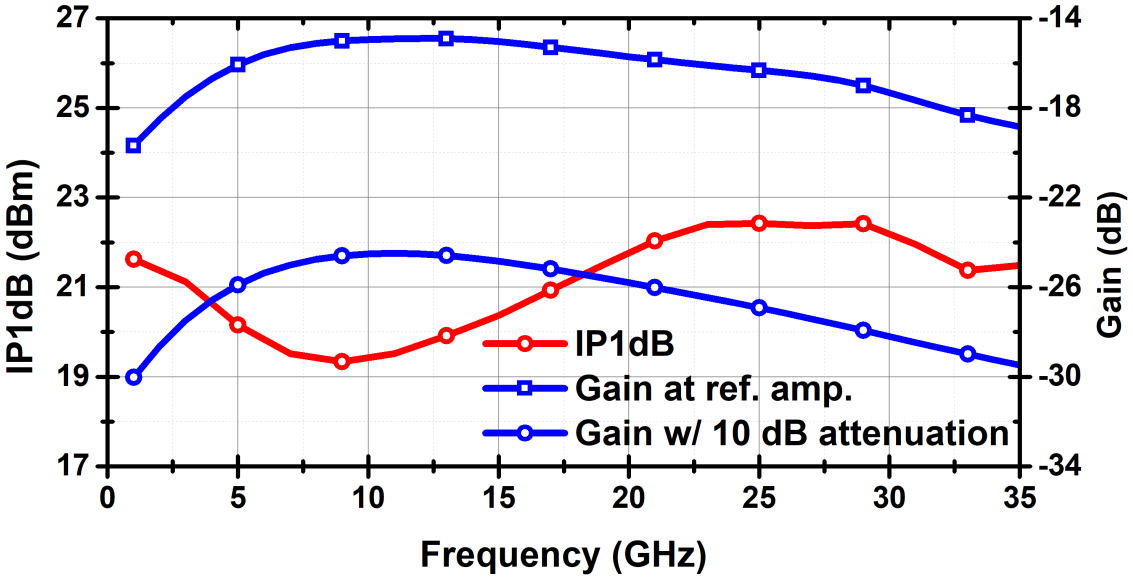

Figure 3.52 Inserted gain at reference amplitude level and with 10 dB attenuation, and IP_{1dB} of the designed coupler based phase shifter

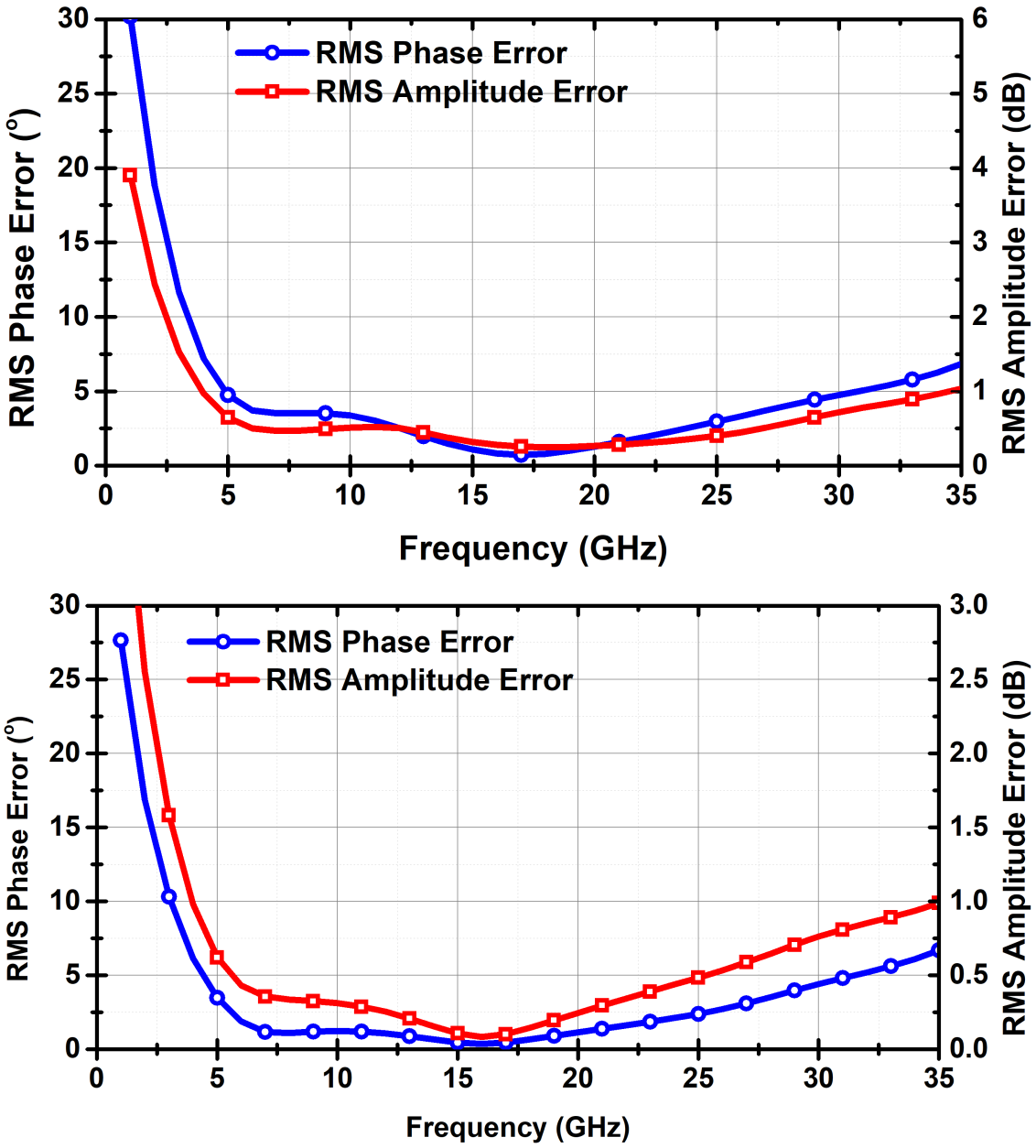

Figure 3.53 RMS phase and amplitude errors of the designed coupler based phase shifter at reference amplitude level (top) and with 10 dB attenuation (bottom)

Table 3.2 Comparison of the designed phase shifter with the state-of-the-art

Reference	**(Gao & Zhao, 2021)**	**(Jung & Min, 2020)**	**(Calışkan et al., 2021)**	**(Hu et al., 2024)**	**This Work****
Technology	65 nm CMOS	28 nm CMOS	130 nm SiGe BiCMOS	90 nm SiGe BiCMOS	**130 nm SiGe BiCMOS**
IP1dB (dBm)	-	-	>12	-11.5	**>19**
Gain (dB)	-11.5	-12.8	-20.4	1.2	**-15**
Bandwidth (GHz)	19–23	29–37	4–26	5–21	**4.7–32**
RMS Phase Error (°)	<2	<8.8	<5.6	<4.1	**<5.6**
RMS Amplitude Error (dB)	<0.38	-	<1.2	<1.6	**<1**
Area (mm^2)	0.64	0.08	0.45	-	**0.63***
Power Consumption	0	0	0	41 mW	**12 mW**

*: Excluding pads **: Post-layout simulation results

3.2.3 Variable Gain Amplifier

VGAs are an amplitude control block that provides gain while adjusting the gain level. There have been various works on VGAs in mm-waves (Altintas, Ozkan, Burak, Yazici & Gurbuz, 2024; Lee, Park & Hong, 2019; Padovan, Tiebout, Neviani & Bevilacqua, 2016; Sadhu, Bulzacchelli & Valdes-Garcia, 2016; Siao, Kao & Wang, 2014; Tsai & Lin, 2019). Fig. 3.54 shows the schematic of a conventional current-steering VGA. The main signal path is through Q1 and Q2, where Q3 enables the gain control functionality. The current passing through Q3 is controlled via its base voltage, $V_{control}$. As the collector current of Q3 increases, Q2's collector current decreases. In other words, Q3 steers current from Q2. This current-steering reduces the transconductance of Q2. As a result, the gain in the signal path decreases.

Wideband gain control is challenging when using current-steering topologies. To address this limitation, a distributed amplifier topology is adopted to enable multi-band operation. Distributed amplifiers are commonly employed in wideband power amplifier designs due to their inherent bandwidth advantages. In this topology, the input signal is successively amplified by multiple identical gain stages, and the amplified signals are linearly combined at the output.

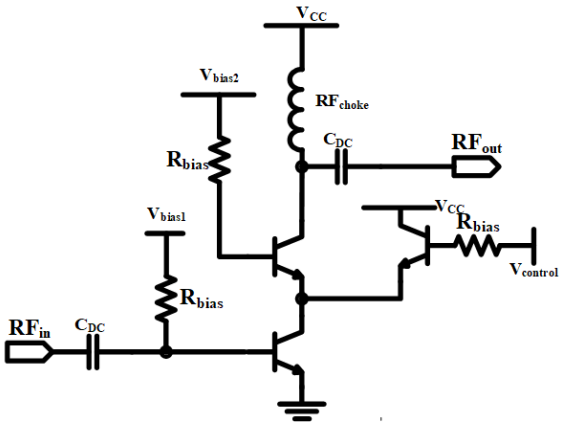

Figure 3.54 The schematic of conventional current-steering VGA

Although comparable overall gain can be achieved using a single-stage amplifier, the gain–bandwidth product is typically lower than that of a distributed amplifier. In contrast, distributed architectures enhance bandwidth by increasing the number of amplification stages. Another advantage of increasing the number of stages in distributed amplifiers is that output power handling is increased. However, because the output summing network utilizes either transmission lines or artificial transmission lines, the associated insertion loss and layout area of the summing network tend to increase as well.

Considering the trade-offs among area, insertion loss, gain, and bandwidth, VGA is implemented using a two-section distributed amplifier topology. Gain control is achieved through a current-steering mechanism by adjusting the base bias of the active devices. To further enhance the bandwidth, RC feedback is incorporated into each stage—similar to the approach employed in the LNA design. The schematic of the designed VGA is shown in Fig. 3.55.

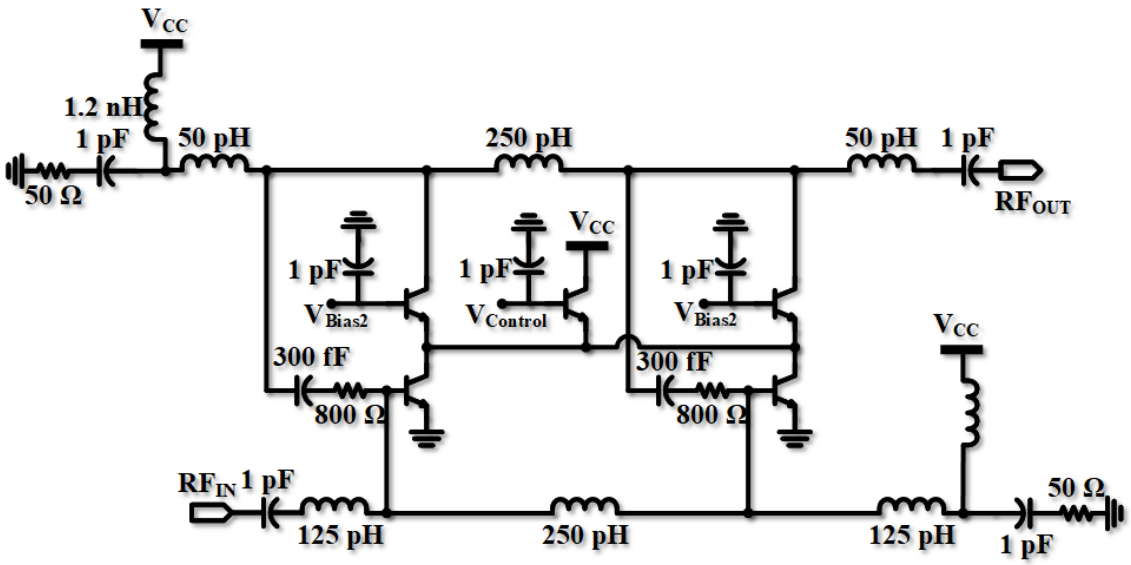

Figure 3.55 The schematic of the designed VGA

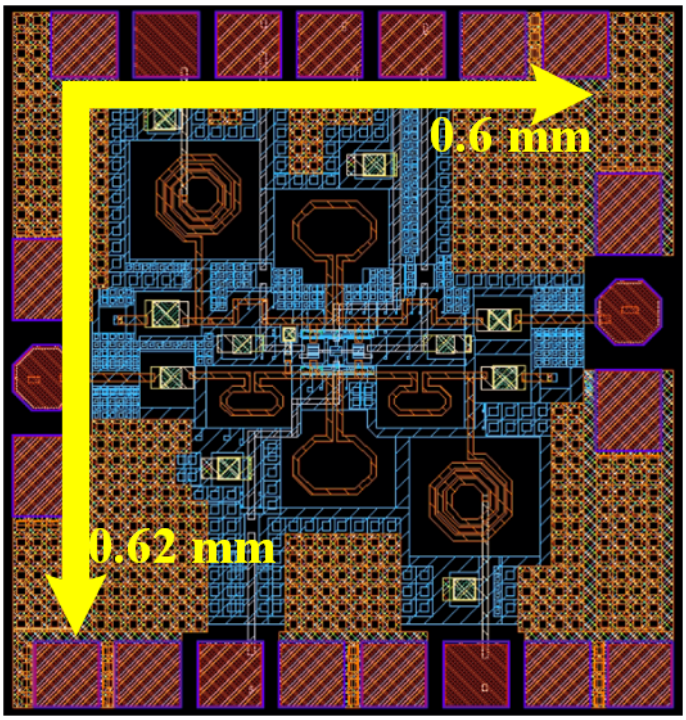

Figure 3.56 The layout of the designed VGA

Post-layout EM simulations of the designed VGA were performed using Keysight

ADS Momentum. The VGA was realized with contributions from Alp Bilgin. The layout of the VGA is shown in Fig. 3.56, and it occupies a core area of 0.38 mm^2 (0.6 mm $\times$ 0.62). The DC power consumption is 54 mW.

Fig. 3.57 illustrates the input and output matching characteristics. The input return loss remains better than 10 dB across the 3.4–35 GHz frequency range, while the output return loss remains better than 10 dB from 5.4 GHz to 35 GHz. Simulated K-factor results in Fig. 3.58 show that the VGA is unconditionally stable in the frequency of interest.

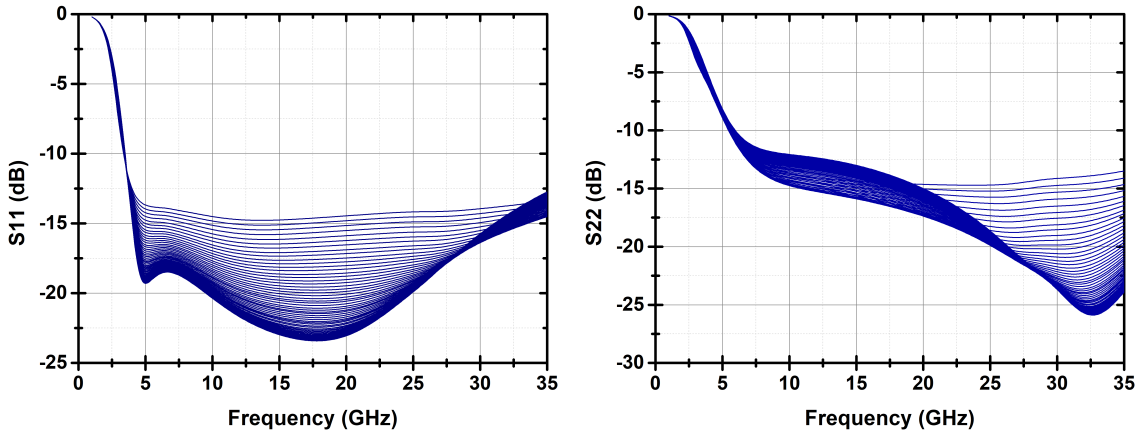

Figure 3.57 The input (left) and output (right) matchings of VGA

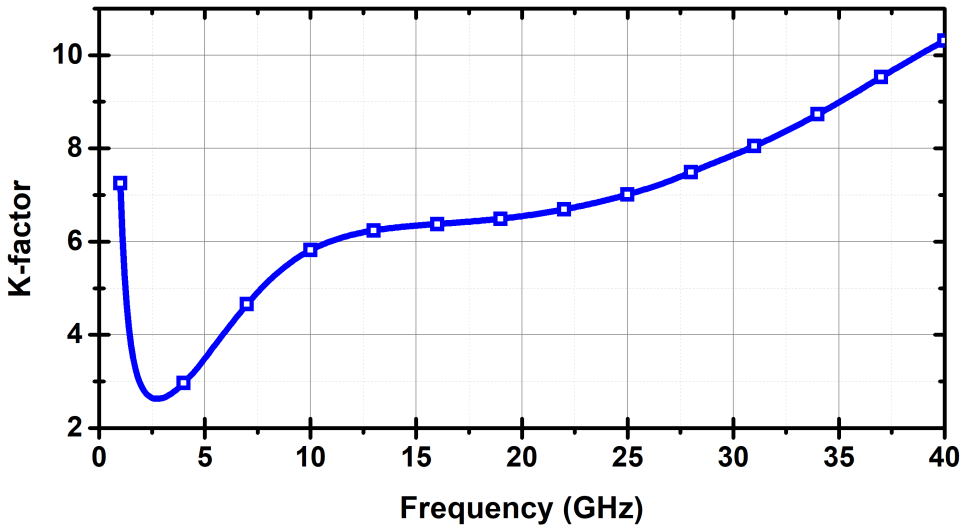

Figure 3.58 Simulated K-factor for the stability of the VGA

Fig. 3.59 illustrates the gain control performance. At the reference state, the amplifier achieves a peak gain of 13.5 dB, with a 3-dB bandwidth extending from 2.9 GHz to 35 GHz. The designed VGA achieves a gain control range of 25 dB with 0.5 dB attenuation steps. Fig. 3.60 demonstrates RMS amplitude and phase errors. RMS amplitude error is lower than 0.2 dB across the 3-dB bandwidth. RMS phase error

is lower than 0.2 dB across the 3-dB bandwidth. For the same frequency range, the RMS phase error is lower than 5.6°. Finally, Fig. 3.61 shows the simulated IP_{1dB} results of VGA.

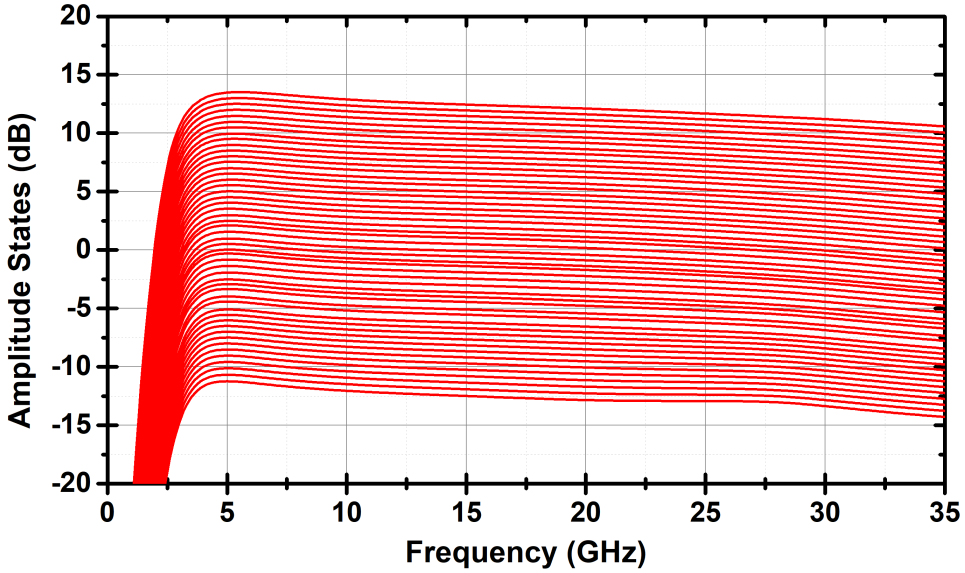

Figure 3.59 The amplitude states of the designed VGA

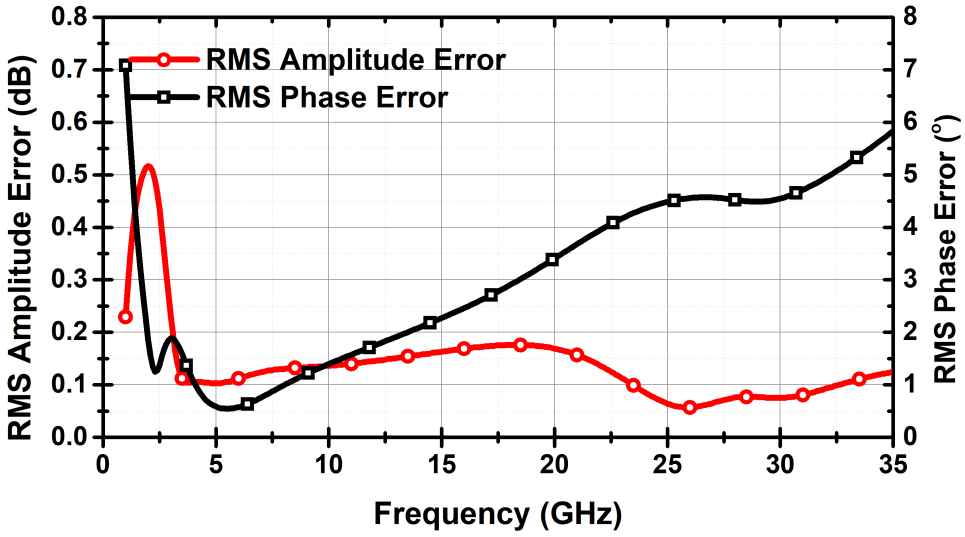

Figure 3.60 RMS amplitude and phase errors of the designed VGA

Table 3.3 presents a comparison between the proposed VGA and a previously reported wideband Si-based VGA designs (Altintas et al., 2024; Chiu, Wang & Wang, 2021; Chiu et al., 2021). Among the referenced works, the highest gain of 21 dB is reported in (Chiu et al., 2021) over a wide bandwidth of 4–43 GHz; however, this design exhibits lower IP_{1dB} performance. The design in (Altintas et al., 2024) achieves the lowest RMS phase error among the compared works but operates over a narrower bandwidth of 8-18 GHz. The proposed VGA offers a high gain, wide bandwidth, and large gain control range.

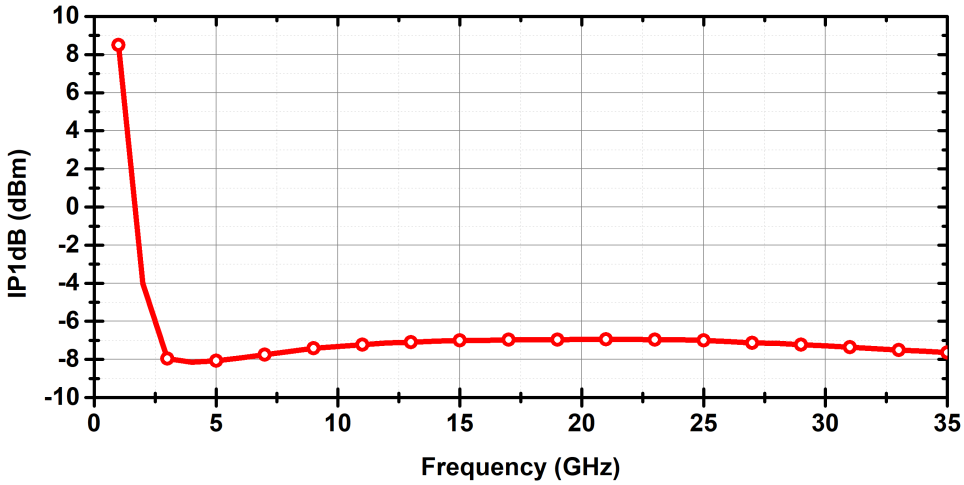

Figure 3.61 The IP_{1dB} of the designed VGA

Table 3.3 Comparison of the designed VGA with the state-of-the-art

	This work**	**(Chiu et al., 2021)**	**(Meng, Yu, Xiao, Zhao, Wu, Liu & Kang, 2025)**	**(Altintas et al., 2024)**
Technology	**130 nm SiGe BiCMOS**	90 nm CMOS	65 nm CMOS	130 nm SiGe BiCMOS
Topology	**VGDA**	VGDA	VGPA	Current Steering VGA
Peak Gain (dB)	**13.2**	21 dB	14.4	13.2
Gain Control Range (dB)	**26****	18 dB	12.8	16
NF (dB)	**5.8 - 6.2**	4.5 - 9.2	5 - 7	1.93 - 2.7 *
Bandwidth (GHz)	**3 - 35+**	4 - 43	22.6 - 37	8 - 18
IP1dB (dBm)	**-8**	-18 to -17 *	- 0.8	3.9
RMS Phase Error (°)	**< 4.7 @ 30 GHz**	-	< 4.8	< 4.3
RMS Amplitude Error (dB)	**0.05 - 0.17**	-	-	0.26
P_{DC} (mW)	**54**	33	126	24
Area (mm^2)	**0.36 mm^2 #**	0.721 mm^2	0.11 mm^2 #	0.58

*: Estimated from figure #: Core area **: Post-layout simulation results

3.2.4 Receiver Simulations

The second receiver includes an LNA, a phase shifter–attenuator block, and a VGA, as illustrated in Fig. 3.34. Post-layout electromagnetic simulations for each individual block were performed using Keysight ADS Momentum. These simulations were then integrated within the ADS environment to evaluate the overall receiver chain performance in terms of noise performance, linearity, and S-parameters. The simulations were conducted with the post-distortion circuitry enabled, as its effectiveness had already been demonstrated in the performance results of the designed LNA. The complete receiver channel occupies a core area of 2.4 mm^2 (3 mm × 0.8 mm).

The simulated input and output matchings of the receiver are presented in Fig. 3.62. The input return loss is higher than 10 dB 1.3–35 GHz range. the output return loss remains better than 10 dB from 5.4 GHz to 35 GHz.

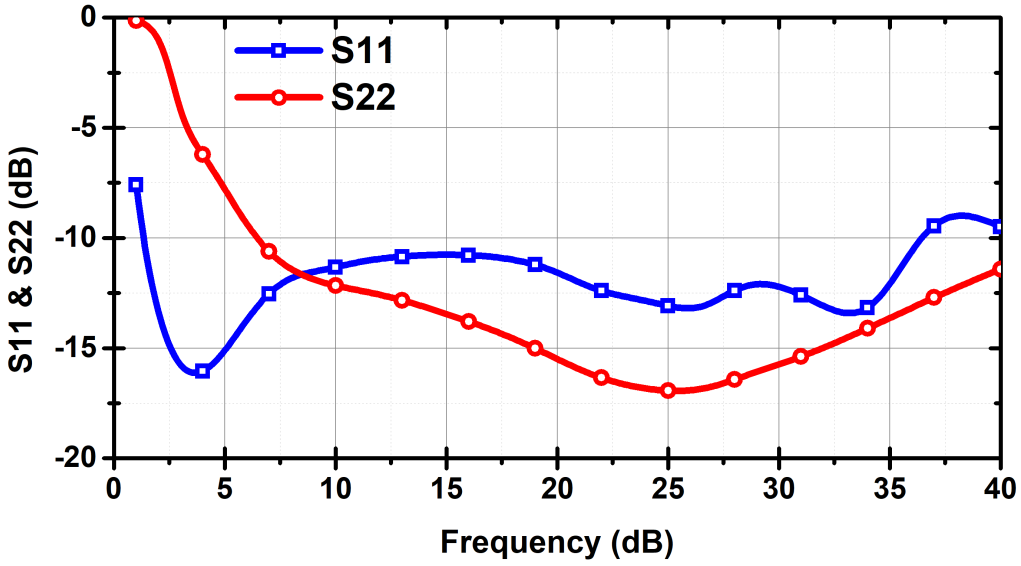

Figure 3.62 The simulated input and output matchings of the wideband receiver

The simulated gain and NF performance of the receiver are presented in Fig. 3.64. The receiver achieves a peak gain of 28.8 dB, with a 3-dB bandwidth spanning from 7 GHz to 26.4 GHz. Within the 4.5–30.2 GHz range, the gain remains above 20 dB.

The simulation results indicate a minimum NF of 2.57 dB at 10.3 GHz, representing approximately a 0.3 dB increase compared to the standalone LNA. This degradation is attributed to the insertion loss of the phase shifter and the moderate NF performance of the VGA (approximately 6 dB). Simulated K-factor results in Fig. 3.63 show that the VGA is unconditionally stable in the frequency of interest. The simulated NF is 2.8 dB at 7 GHz and 3.3 dB at 26.4 GHz, indicating that the NF

remains below 3.3 dB within the 3-dB bandwidth. The maximum NF across the 4.5–30.2 GHz frequency range is 4.2 dB, observed at the upper end of the spectrum.

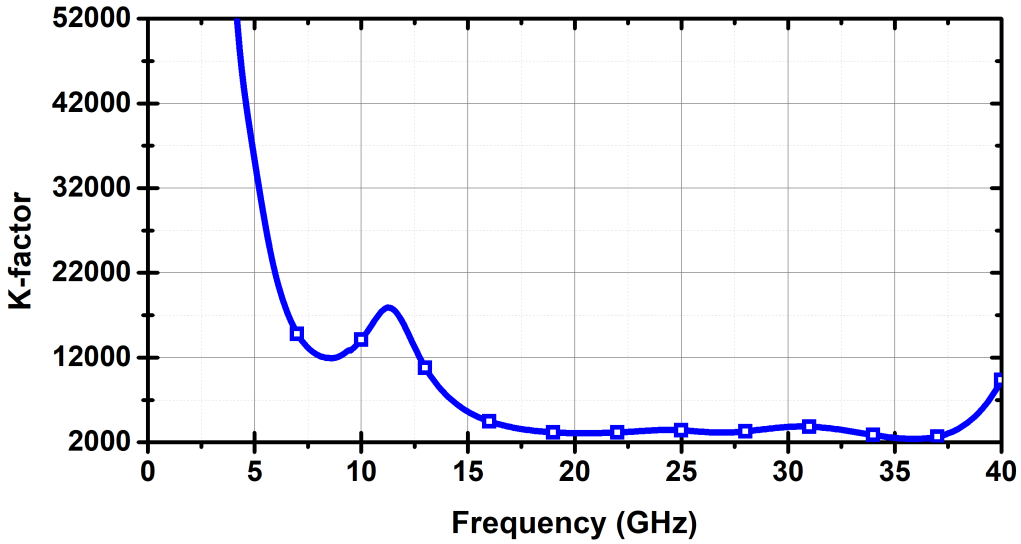

Figure 3.63 Simulated K-factor for the stability of the second receiver

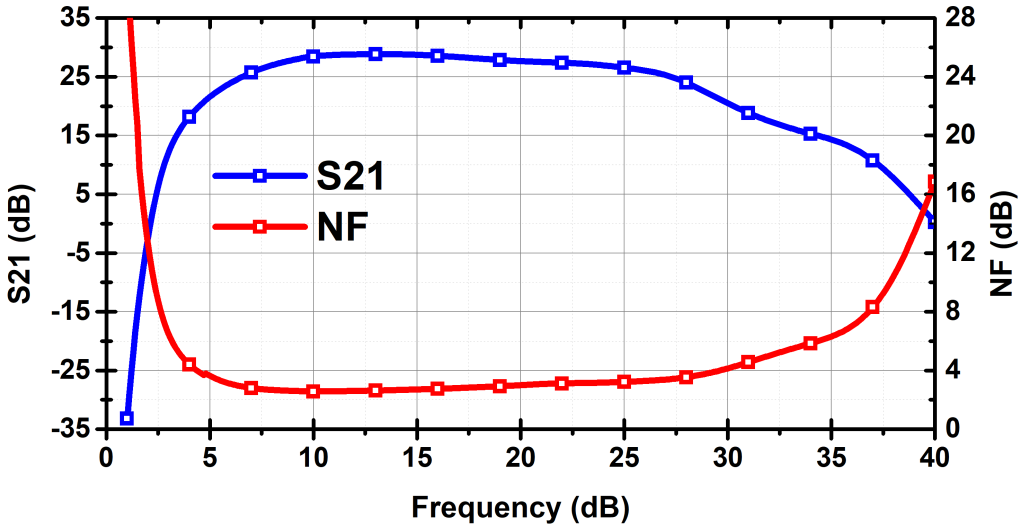

Figure 3.64 The simulated gain and NF of the wideband receiver

The IP_{1dB} and IIP3 of the receiver are shown in Fig. 3.65. The results indicate that, with the post-distortion technique enabled, the IP_{1dB} ranges from -35 dBm to -23 dBm across the operating bandwidth. The IIP3 varies between -25 dBm and -12. dBm, demonstrating highly linear behavior throughout the band.

Fig. 3.66 demonstrates the simulated amplitude states relative to the highest gain configuration. The receiver achieves an overall amplitude control range of 36 dB with a fine resolution of 0.5 dB. Of this total range, 26 dB is provided by the VGA, while the remaining 10 dB is contributed by the coupler-based phase shifter. Fig. 3.68 depicts the simulated phase states with respect to the reference state. Overall

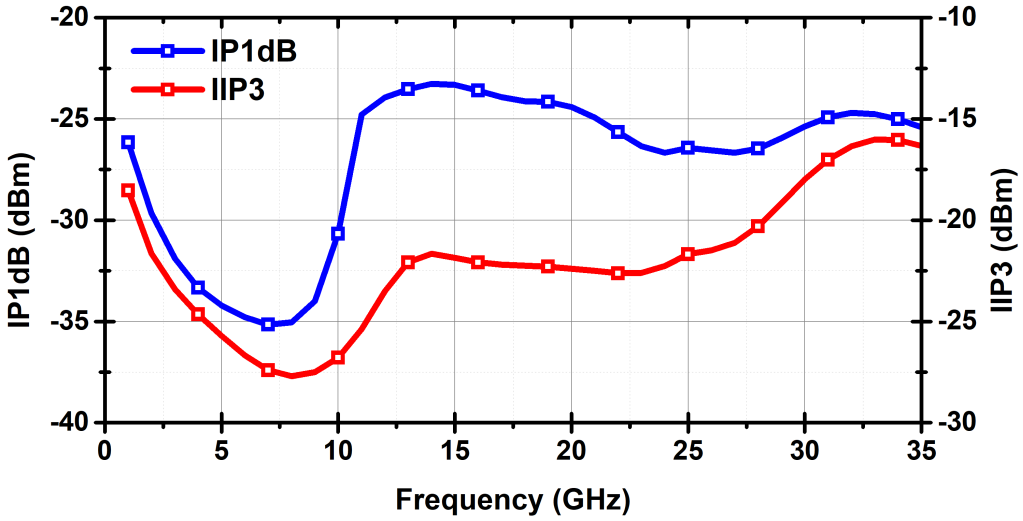

Figure 3.65 The simulated IP_{1dB} and IIP3 of the wideband receiver

phase range of the receiver is 360° with 5.6° phase resolution.

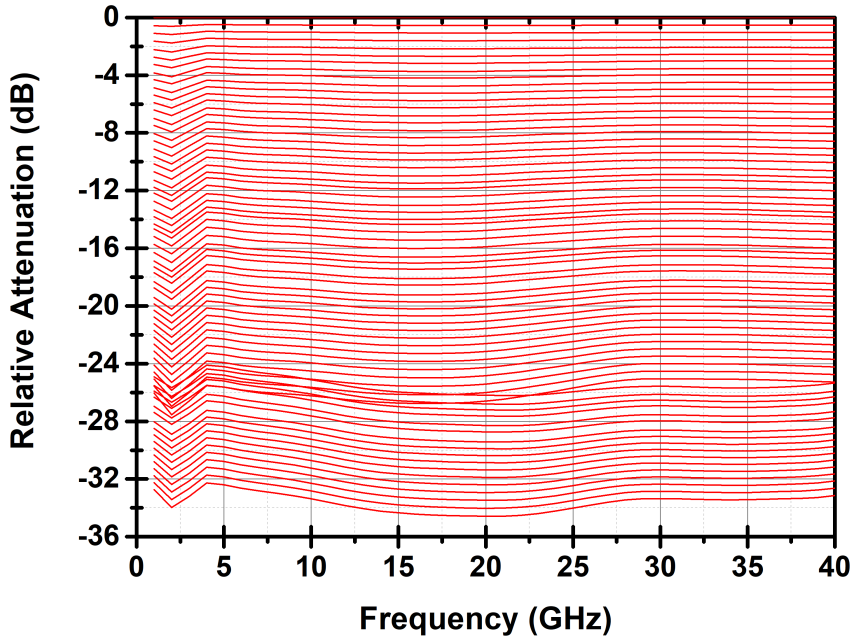

Figure 3.66 The simulated relative attenuation states of the wideband receiver

Fig. 3.68 demonstrates the simulated RMS amplitude and phase errors. The simulated RMS amplitude error is lower than 0.35 dB while the simulated RMS phase error is lower than 5.6° in the 3-dB bandwidth. These values are attributed to coupler based topology, proposed VVA in phase shifter-attenuator, and distributed VGA with an RC-feedback.

Fig. 3.69 shows the average group delay and their average variation among different 64-phase states. The average group delay variation among the phase states is below 4 ps in the 3-dB bandwidth since the second receiver achieves flat phase response in

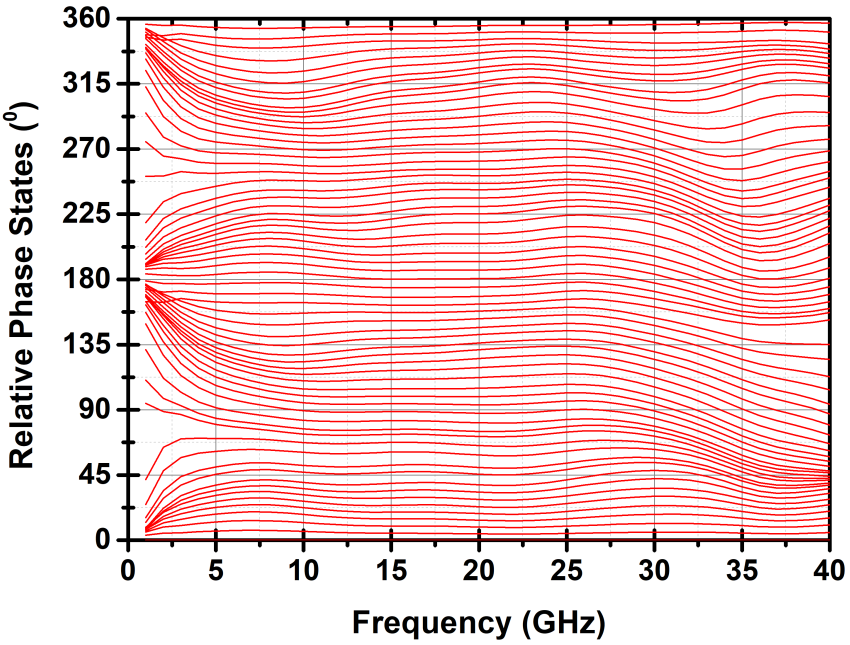

Figure 3.67 The simulated relative phase states of the wideband receiver

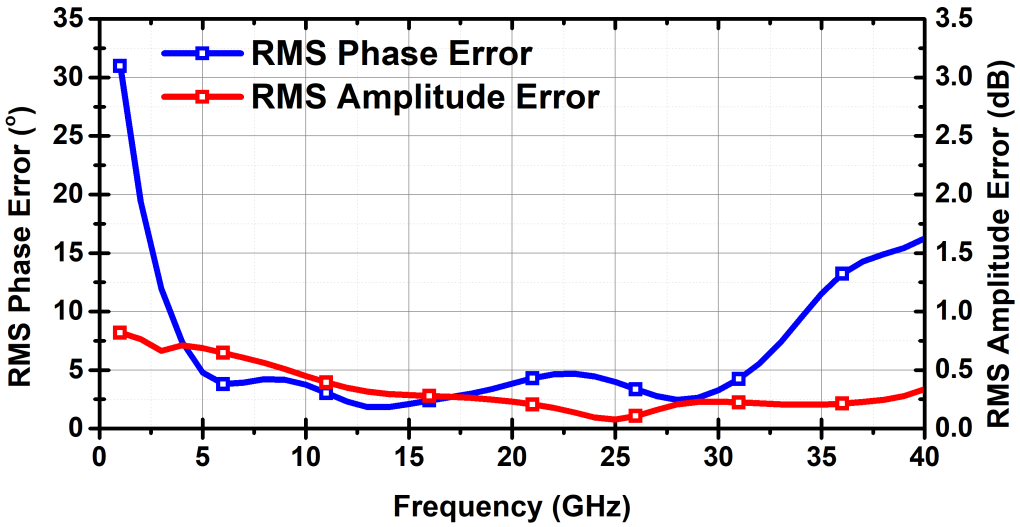

Figure 3.68 The simulated RMS phase and amplitude errors of the wideband receiver

the 3-dB bandwidth.

Table 3.4 presents a comparison between the proposed receiver and a previously reported wideband Si-based receiver that operates in different SATCOM reception bands. (Alhamed et al., 2023; Hu et al., 2024; Lee et al., 2024; Liu et al., 2016; Mondal et al., 2018). Among the referenced works, the highest gain of 34 dB is reported in (Mondal et al., 2018) over a bandwidth of 25-30 GHz; however, this design does not support amplitude control. The design in (Alhamed et al., 2023) achieves the largest bandwidth among the compared works, but the referred linearity performance is around -50 dBm. The proposed receiver offers a high gain, wide

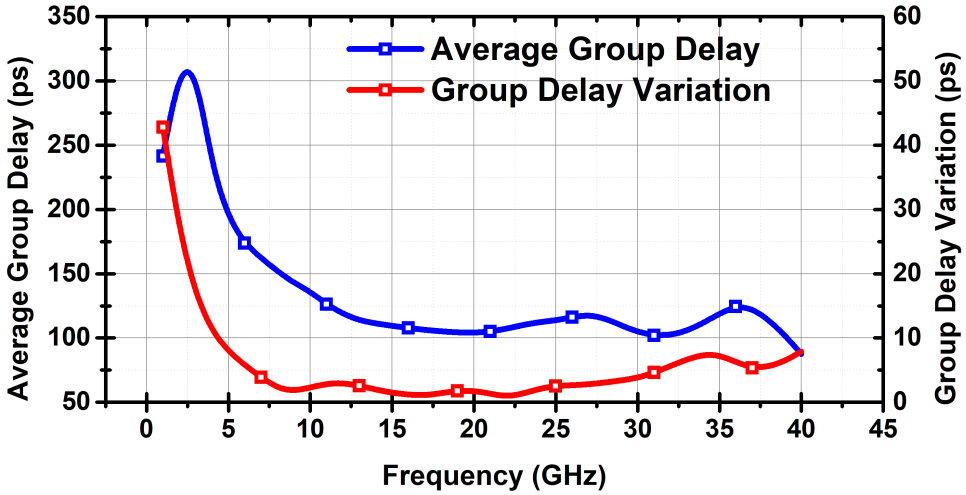

Figure 3.69 The simulated average group delays of 64-phase states, and average group delay variation among 64 phase states

bandwidth, and large gain control range with good phase and amplitude resolution. Due to the distance in the SATCOM and path loss, the IP_{1dB} of our receiver is sufficient to support SATCOM applications thanks to the employed post-distortion method.

Table 3.4 Performance comparison of state-of-the-art beamformers in SATCOM bands

Reference	This Work**	(Hu et al., 2024)	(Alhamed, Gültepe & Rebeiz, 2023)	(Lee, Ozdag, Plouchart, Valdes-Garcia & Sadhu, 2024)	(Liu et al., 2016)	(Mondal et al., 2018)
Technology	**130 nm SiGe BiCMOS**	90 nm SiGe BiCMOS	180 nm SiGe BiCMOS	130 nm SiGe BiCMOS	130 nm SiGe BiCMOS	65 nm CMOS
Architecture	**RX**	RX	4x1 RX	TRX	TRX	RX
Peak Gain (dB)	**25**	26.6	22	19.5	25	34
NF (dB)	**2.7 – 3.8**	2-2.4	4.7 – 6.2	2.8 – 3.1 dB	3	7.3
Bandwidth (GHz)	**7 – 26.4**	3.1 - 25.5	15 – 57	24 – 30	9 - 11	25 - 30
IP_{1dB} (dBm)	**–35 to -23**	-50	–28	–31.2	-18	-29
Gain Control Range (dB)	**36**	25	18	8	-	-
RMS Phase Error (°)	**< 5.6**	< 5.6	< 3.6	< 0.8	< 3.8	-
RMS Amplitude Error (dB)	**< 0.35 dB**	< 1	< 1.1	< 0.5	1.2	-
P_{DC} (mW)	**150**	112.5	200	48	352	425
Area/Channel (mm^2)	**2.4**	0.9	0.8*	1.26	15.6#	0.77

*: Estimated from figure **: Simulation

4. CONCLUSION AND FUTURE WORK

4.1 Summary of Work

SATCOM enables global connectivity and broadband internet coverage, playing a key role in delivering high-speed communication to users worldwide. In addition to providing global connectivity, the growing demand for higher data rates and cost-efficient communication solutions is driving the need for increased bandwidth utilization. To meet these requirements, SATCOM systems can leverage the wide bandwidth available in the mm-wave spectrum, along with phased array transceivers, to support high data rate transmission.

In this thesis, a wideband receiver covering C-, X-, Ku-, Ka-bands licensed for SATCOM reception is designed and implemented in 0.13 μm SiGe BiCMOS technology. The receiver incorporates a three-stage cascode LNA providing single-ended to differential conversion, a passive vector sum phase shifter with amplitude control, and a VGA based on a distributed amplifier topology to meet the bandwidth target. To the best of the authors' knowledge, this is the first implementation of the passive vector-sum phase shifter that provides both amplitude and phase control functionality in a single block. This multi-functionality attributes to the proposed closed-loop VVA. A minimum NF of 2.8 dB is achieved with -23 dBm input power capability in a 116% fractional bandwidth. Low NF is crucial in determining the minimum detectable signal level in SATCOM terminals. 6-bit phase resolution and 36 dB amplitude control range with 0.5 dB steps are significantly beneficial in suppressing side lobes in a phased array system. Since the receiver is implemented in SiGe BiCMOS technology, the receiver offers a low-cost design compared to counterparts in III-V technologies. Therefore, this design is very promising and a good candidate to be an element in the phased array receivers for SATCOM applications.

4.2 Future Work

In the short term, the sub-blocks in the wideband receiver, were taped out for fabrication, will be subject to measurements. Hence, the measurement schemes are going to be prepared. PCB boards for each die to be measured are going to be designed and fabricated to feed the supply voltages. Furthermore, a transmitter version of the receiver has been undergoing development in 0.13 μm SiGe BiCMOS technology, and will be taped out for fabrication.

There are several design points that can be focused on to enhance the performance of the presented receiver. First of all, the control of VGA can be changed to digital control rather than analog voltage in order to reduce the system-level complexity in a phased array. Another aspect to be improved is the area of the phase shifter. The area occupied by the quadrature hybrid coupler can be reduced by implementing it with lumped components. Furthermore, employing an active balun instead of the passive balun in the LNA can increase the overall receiver gain and improve the gain flatness.

In the long term, the designed receiver and transmitter in the short-term goals can be implemented in four-channel transmitter and receiver chips. These chips will be connected to an antenna to evaluate in a communication scheme. These measurements will be proof that the transmitter and receiver are promising candidates to be utilized in a LEO for SATCOM.

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APPENDIX

List of Publications

During my post-graduate period, I was the author and co-author of seven journal papers and six conference papers. Moreover, we already submitted two journal papers and we plan to submit one journal paper in a short term. You can find the list of publications during my post-graduate period in Sabanci University with SUMER group under the supervision of Prof. Yasar GÜRBÜZ below.

Journals

A. B. Ozdol, T. A. Ozkan, H. Kaya, M. E. Cakir, I. Kalyoncu and Y. Gurbuz, "Highly Linear Wideband Low-Noise Amplifiers for Sub-6 GHz Using Cascode and Diode-Connected Postdistortion Circuits," in IEEE Transactions on Microwave Theory and Techniques, doi: 10.1109/TMTT.2025.3558333.

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S. Firouz, T. A. Ozkan, N. K. Veziroglu, O. Ceylan, C. Carta, and Y. Gurbuz, "Design of a Low-Phase-Noise Integer-N PLL Employing a Cross-Coupled VCO with a Decoupled Tank and LC Tail Filter for 5G Applications in 130nm BiCMOS Technology" (Submitted to IEEE Transactions on Circuits and Systems - I: Regular Papers)

M. E. Cakir, T. A. Ozkan, C. Carta, and Y. Gurbuz, "A Wideband Low Noise Amplifier with Diode Connected Post-Distortion in 130 nm SiGe BiCMOS for SATCOM Applications" (Soon to be submitted)