ULTRA-WIDEBAND POWER AND LOW NOISE DISTRIBUTED AMPLIFIERS WITH AREA REDUCTION METHODS

by
SELİM ARAS YAĞMURLU

Submitted to the Graduate School of Engineering and Natural Sciences
in partial fulfilment of
the requirements for the degree of Master of Science

Sabancı University
June 2025

ULTRA-WIDEBAND POWER AND LOW NOISE DISTRIBUTED AMPLIFIERS WITH AREA REDUCTION METHODS

Approved by:

Asst. Prof. KORKUT KAAN TOKGÖZ .....
(Thesis Supervisor)

Prof. İBRAHİM TEKİN .....

Assoc. Prof. MUSTAFA BERKE YELTEN .....

Date of Approval: July 16, 2025

ABSTRACT

ULTRA-WIDEBAND POWER AND LOW NOISE DISTRIBUTED AMPLIFIERS WITH AREA REDUCTION METHODS

SELİM ARAS YAĞMURLU

Electronics Engineering, M.Sc. Thesis, July 2025

Thesis Supervisor: Asst. Prof. Korkut Kaan Tokgöz

Keywords: ultra-wideband, distributed amplifiers, transconductance optimization, area reduction, CMOS, low-noise amplifier, power amplifier

Ultra-wideband (UWB) amplifiers are essential components of communication systems, radar, and fiber-optic technologies that require a wide bandwidth and minimal latency. Distributed amplifiers (DAs) effectively manage parasitic capacitances through artificial transmission-line structures, offering inherent broadband performance. However, conventional DAs typically consume large silicon areas due to numerous stages and extensive interconnections, and passives.This thesis introduces increased transconductance bandwidth with a fully-shunt peaking method in cascode and compact inductor-based area reduction methods with decreased quality factor optimization for distributed power amplifiers (DPA) and distributed low-noise amplifiers (DLNA). The proposed DPA achieves an average 13.75 dB gain and stable output power with average of 13.69 dBm across a minimum 70 GHz bandwidth. The DLNA has a noise figure below 6 dB with an average gain of 13.6 dB within the same frequency range. Both designs, implemented in TSMC's 65-nm bulk CMOS technology, outperform literature in noise figure, gain, and output power.

ÖZET

ALAN AZALTMA YÖNTEMLERİYLE ULTRA GENİŞ BANT GÜÇ VE DÜŞÜK GÜRÜLTÜLÜ DAĞITILMIŞ YÜKSELTEÇLER

SELİM ARAS YAĞMURLU

Elektronik Mühendisliği, Yüksek Lisans Tezi, Temmuz 2025

Tez Danışmanı: Dr. Öğr. Üyesi Korkut Kaan Tokgöz

Anahtar Kelimeler: ultra-geniş bant, dağıtık amplifikatörler, alan azaltma teknikleri, CMOS, düşük gürültülü amplifikatör, güç amplifikatörü

Ultra geniş bant (UWB) amplifikatörler, geniş bant genişliği ve minimum gecikme gerektiren iletişim sistemleri, radar ve fiber optik teknolojilerinin temel bileşenleridir. Dağıtık amplifikatörler (DA'lar), yapay iletim hattı yapıları aracılığıyla parazitik kapasitansları etkili bir şekilde yöneterek doğal geniş bant performansı sunmaktadır. Ancak, geleneksel DA'lar, çok sayıda kademe, kapsamlı ara bağlantılar ve pasifler nedeniyle genellikle geniş silikon alanları tüketmektedir. Bu tez, kaskod ve kompakt indüktör tabanlı alan azaltma yöntemlerinde tam şönt tepe yöntemi ile artırılmış transkondüktans bant genişliğini, dağıtılmış güç amplifikatörleri (DPA) ve dağıtılmış düşük gürültülü amplifikatörler (DLNA) için azaltılmış kalite faktörü optimizasyonuyla sunmaktadır. Önerilen DPA, minimum 70 GHz bant genişliğinde ortalama 13,75 dB kazanç ve ortalama 13,69 dBm kararlı çıkış gücü sağlamaktadır. DLNA, aynı frekans aralığında ortalama 13,6 dB kazançla 6 dB'nin altında bir gürültü değerine sahiptir. TSMC'nin 65 nm toplu CMOS teknolojisinde uygulanan her iki tasarım da gürültü figürü, kazanç ve çıkış gücü açısından literatürden daha iyi sonuçlanmıştır.

ACKNOWLEDGEMENTS

This thesis was supported by the Scientific and Technological Research Council of Turkey (TÜBİTAK) under Grant No. 121C073, titled "Development of Critical Building Blocks for mm-Wave and sub-THz Front-End Transceivers on CMOS Towards 1 Tbps Wireless Communications."

First and foremost, I would like to express my sincere gratitude to my supervisor, Asst. Prof. Dr. Korkut Kaan Tokgöz, for his continuous guidance and support throughout my academic journey. His mentorship - extending from my undergraduate years into my master's studies - has profoundly shaped both my technical expertise and personal development.

I also wish to thank the members of my thesis committee, Prof. İbrahim Tekin and Assoc. Prof. Dr. Mustafa Berke Yelten, for their valuable time, insightful comments, and constructive feedback, all of which significantly contributed to the improvement of this work.

I am deeply grateful to my friends Helin, Sinan, Batu, İrem, Ekin, Bartu, Ege, Erkin, Efe, and many others, for their enduring friendship and the countless shared experiences that made my university life meaningful.

Lastly, I would like to thank my parents, Aslı and Fırat for their unwavering support, love, and encouragement throughout this journey. Their sacrifices and constant presence - both mentally and physically - have been instrumental in helping me move forward in life and complete this thesis.

In memory of my grandfather, Kurtul Tülüveli, who instilled in me the passion for learning and the joy of teaching.
Bana hem öğrenmeyi hem de öğretmeyi sevdiren kıymetli dedem Kurtul Tülüveli'ye, sevgi ve özlemle...

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

1. INTRODUCTION

1.1 Need for Ultra-Wideband Amplifiers

The need for higher data transfer rates is driving continuous innovation in communication systems. According to the Shannon–Hartley theorem, channel capacity is governed by three parameters, which are bandwidth, signal power, and noise level. Especially in scenarios where the available power or noise figure is already near its practical limit, widening the bandwidth becomes the most direct and effective means of boosting capacity, as expressed in Eq. 1.1.

$$C = B \log_2\left(1 + \frac{S}{N}\right) \tag{1.1}$$

High-frequency wireless technologies are now commonly used in millimeter-wave communication, automotive radar, and fiber-optic systems. These applications demand ultra-wideband (UWB) amplifiers that operate across tens of gigahertz while maintaining stable gain, either high output power or low noise, and minimal latency.

These parameters are controlled mainly by two important amplifiers, which are low-noise and power amplifiers (PA). On the receiver side, the low noise amplifier (LNA) amplifies weak incoming signals while minimizing added noise. This reduces the overall noise of the entire path, making the signal-to-noise ratio lower. On the transmit side, the power amplifier (PA) amplifies the amplified signal to a maximum reachable output power, which is controlled by the PA's Saturated Output Power Psat. PAs are used as the final stage before the antenna, while the form of the signal does not affect.

However, most of the PA and LNA designs often do not deliver UWB flat gain

and matching. This makes the traditional amplifier topologies not usable in these bandwidths. Moreover, as operating bandwidth increases, parasitic effects and gain-bandwidth limitations become more dominant, making conventional solutions insufficient for UWB applications. This makes the researchers search for possible solutions for UWB coverage.

1.2 Ultra-Wideband Amplifiers and Topologies

1.2.1 What is Ultra-Wideband Amplifier?

As the name implies, ultra-wideband (UWB) amplifiers are designed to operate in an extensive frequency range. According to the literature Yang & Giannakis (2004) and the Federal Communications Commission (FCC) Federal Communications Commission (2002) in the United States, a signal is classified as a UWB, if it satisfies one of the following criteria: greater than 500 to 1500 MHz of bandwidth or a fractional bandwidth(FBW) of greater than 20-25% which fractional bandwidth is calculated according to Eq.1.2.

$$\mathrm{FBW}_{\%} = \left(\frac{2(f_H - f_L)}{f_H + f_L}\right) \times 100 \geq 25\% \tag{1.2}$$

In this thesis, the designed amplifiers are expected to work minimum in the range of 1 GHz to 71 GHz, resulting in a 70 GHz bandwidth. This large bandwidth results in an FBW of 194%. This FBW value exceeds the minimum requirement presented by the FCC and the literature for UWB systems. This much bandwidth also shows the design's goal of high-speed data transfer across a wide frequency range. Traditional amplifier topologies commonly fail to meet these requirements due to the limited FBW designs.

1.2.2 Various Ultra-Wideband Amplifier Topologies

To solve the limitations that were presented previously, UWB amplifier designs must be used, and they are expected to be able to work in broadband or have higher FBW inherently. Among various topologies that have large bandwidth, the resistive-feedback amplifier, filter-match amplifier, and distributed amplifier emerge as an effective solution to these problems.

1.2.2.1 Resistive-Feedback Amplifier

Resistive feedback is a method that is commonly used to extend bandwidth and better impedance matching over larger bandwidths. The topology consists of a resistor that connects a resistor to the input and output nodes, creating a feedback loop which is shown in Figure 1.1. In the literature, it is even suggested to put a degeneration resistor to even enhance gain flatness and linearity (Lee, 2003).

$$Z_{\text{in}} = \frac{R_F}{1+g_m R_L}, \quad Z_{\text{out}} = \frac{R_F}{1+g_m R_S} \tag{1.3}$$

In implementations of resistive-feedback input and output impedance can be calculated using Eq. 1.3. This enables only 4-parameter control for matching, resulting in simultaneous matching to $50\,\Omega$ by selecting appropriate values for R_F, R_L, and R_S based on the transistor's transconductance (g_m).

In the literature, resistive feedback loops are used multiple times back-to-back to build a design without inductors that is LNA in Silicon-Germanium (SiGe). It has a 20 dB gain and 7 GHz bandwidth with a noise of 3 dB to 4 dB, while without the inductors, significantly reduced area (Lee & Cressler, 2005).

1.2.2.2 Filter-Match Amplifier

The filter-match amplifier is one of the designs that can enable UWB amplification. It can use the input capacitance of a transistor or an external capacitor together with an inductor to create an LC band-pass filter (Ismail & Abidi, 2004). This allows the amplifier to have a wide impedance matching. However, the filters' inherent low-frequency blocking capability is not suitable for down to direct current (DC)

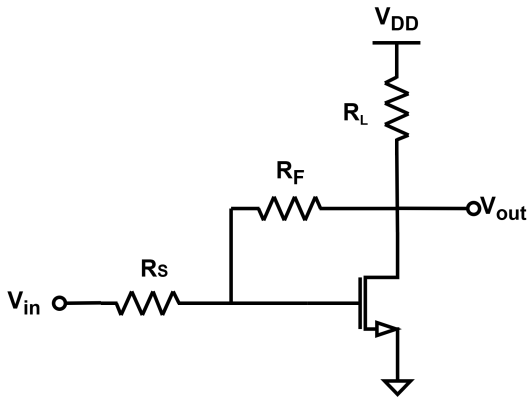

Figure 1.1 Common-source amplifier with resistive feedback.

applications.

In the literature, filter-match amplifiers are commonly found in 3 GHz to 10 GHz (Bevilacqua & Niknejad, 2004; Ismail & Abidi, 2004). Peaking inductors can be added to boost the effective bandwidth and help extend bandwidth beyond the unity gain frequency (Bevilacqua & Niknejad, 2004). Compared to resistive-feedback amplifiers, this topology is less area efficient due to the usage of an inductor in the band-pass filter. But, it has a comparable power consumption to the resistive-feedback amplifier. These techniques are shown in UWB LNAs using both ladder-type and shunt-feedback structures, each with different trade-offs between area and gain flatness (Bevilacqua & Niknejad, 2004; Ismail & Abidi, 2004).

In these conventional lumped amplifiers (filter-match and resistive-feedback amplifiers), the gain bandwidth product (GBP) is constrained by the parasitic capacitances of the active devices. This leads to the classical trade-off where increasing voltage gain A_v typically decreases the -3 dB bandwidth $f_{-3\text{dB}}$, since their product remains nearly constant, as expressed in Eq. 1.4:

$$\text{GBP} = A_v \cdot f_{-3\text{dB}} \tag{1.4}$$

1.2.2.3 Distributed Amplifier

Distributed amplifier (DA) takes a completely different approach from the other UWB or broadband amplifier topologies. The main difference between it and the

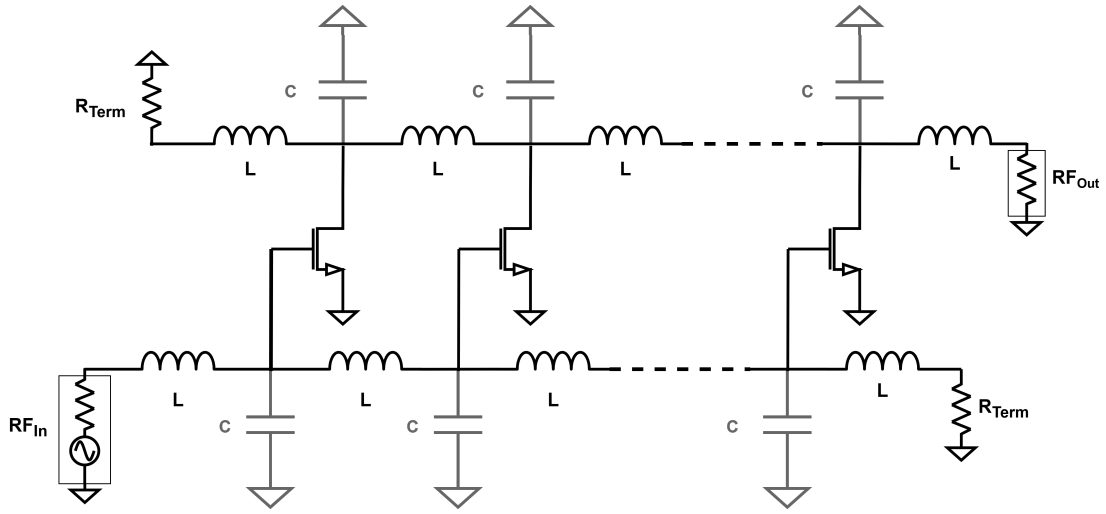

Figure 1.2 Distributed amplifier in the form of LC ladders.

other topologies is in distributed amplifiers instead of cascading transistors to increase the gain-bandwidth product, which places the transistors in parallel to each other. Then connects each transistor's gate and drain with inductors to form artificial transmission lines(ATLs). These LC ladders, as shown in Figure 1.2, allow the parasitic capacitance of transistors to be absorbed and allow the signal to propagate inside the created ATLs. Each stage produces an amplified signal, and these signals combine at the output which resulting in a higher gain. This parallel structure of a distributed amplifier helps to distribute gain across stages and enables wider bandwidths. Therefore, distributed amplifiers can surpass the gain-bandwidth limitation.

Normally, in a transistor, the gain-bandwidth is limited by the unity-gain. In a single transistor, if the width is doubled gain should be increased, but the bandwidth should drop due to higher output capacitance. However, in DAs, gain can be increased by adding more stages and without ht affecting the bandwidth, because the output capacitance of each stage is separated stage by stage. In DAs, trade is mainly between the delay to gain, which is inversely proportional to each other, because to increase gain, more stages need to be added, but this increases the number of stages delays to each other, but the frequency stays flat. The matching is controlled by terminating input and output lines with resistances that make matching automatic.

As every topology has drawbacks, distributed amplifiers have their drawbacks, too. First, half of the output power is lost to the output termination resistor. This also reduces the efficiency significantly. The area and power consumption are high due to the number of stages, increasing them by a 5 to 10 times increase in power consumption (Bevilacqua & Niknejad, 2004). The area is larger due to the use of lots of inductors, which cover most of the area. Noise figure is around 3 dB at low frequency due to the termination resistance at the input ATL. However, these

negative effects do not affect its usability due to its benefits.

1.3 Motivation

In millimeter-wave communication links, multi-purpose wireless communication, ultra-wideband communication, fiber-optic systems ultra-wideband (UWB) amplifiers are required in both the transmit and receive chains to cover tens of gigahertz while maintaining minimal latency and distortion. Among the available UWB topologies, the distributed amplifier (DA) is particularly well suited for bandwidths up to 70 GHz. This is due to its ATL structure, which absorbs parasitic capacitances along the line, resulting in minimal impact on bandwidth. In addition, the integrated termination resistor enables the design to achieve broadband matching inherently.

The main drawback of the DA, however, is its large area consumption. Each added stage, along with its ATL section, significantly increases the layout size, often exceeding 0.5 mm^2 in 65-nm Complementary metal–oxide–semiconductor (CMOS). This becomes a major constraint in multi-amplifier systems where multiple circuits must share a single die, especially in research applications where silicon area is a limited and costly resource.

This thesis, therefore, focuses on realizing area-efficient DAs while maintaining state-of-the-art performance. In the PA path, the goal is to achieve a maximum gain of 15 dB and stable output power above 13 dBm across a minimum bandwidth of 70 GHz, all within the smallest possible area. In the LNA path, the target is to maintain a flat noise figure below 6 dB and a peak gain of 15 dB over at least the same bandwidth, again with aggressive area reduction. Across both paths, the area optimization is driven by reducing passive components' area usage, either in the form of more compact transmission lines or optimized inductor structures.

All circuits are realized in TSMC 65-nm bulk CMOS and are designed to outperform recent literature in noise figure (NF), total transconductance (G_m), output 1-dB compression point($OP_{1\mathrm{dB}}$), and expected layout footprint. The ensuing chapters detail the underlying theory, the proposed area-reduction techniques, and the experimental validation of these claims.

1.4 Thesis Organization

The thesis organization follows:

The remainder of this thesis is organized as follows:

- Chapter 2 provides a comprehensive background on distributed amplifiers. It begins by explaining their operational principles and then discusses key performance limitations, such as gain-delay trade-offs, noise behavior, and distortion mechanisms. Various distributed amplifier (DA) topologies are reviewed, including cascode, inductive peaking, tapered, and feedback-based designs. The chapter concludes by introducing area reduction methods, focusing on slow-wave transmission lines, inductor different shapes and stacked inductor strategies.

- Chapter 3 presents the design and analysis of the proposed distributed power amplifier (DPA). Design considerations and theoretical formulations are detailed, including Class-A operation and G_m peaking. The proposed design methodology is described, followed by the simulation results at the schematic level and the EM simulated inductor schematic. The performance is then benchmarked against state-of-the-art designs in the literature.

- Chapter 4 focuses on the development of the distributed low noise amplifier (DLNA). Design aspects specific to low-noise performance are discussed, supported by theoretical noise figure calculations and transconductance optimization. The chapter also details the applied area reduction techniques and includes both schematic and layout-level simulations. A comparative evaluation with prior work concludes the chapter.

- Chapter 5 summarizes the contributions of the thesis. It highlights the key achievements, discusses limitations, and proposes directions for future research in ultra-wideband amplifier design.

2. BACKGROUND

2.1 Overview of Distributed Amplifiers

The topology of distributed amplification dates back to Percival's patent in 1936 (Percival, 1937), but it was perfected and published in the scientific community by Ginzton in 1948 (Ginzton, Hewlett, Jasberg & Noe, 1948). This approach was considered a solution for achieving wide-band amplification with vacuum tube technology, which is the most common amplifier technology. Since then, distributed amplifiers (DAs) have become a fundamental wideband amplifier architecture because they can surpass the intrinsic gain-bandwidth limitation of individual transistors. During the past decades, advances in IC interconnects, passive components, and transistor technologies have enabled compact, fully integrated ultra-wideband amplifiers operating well into the sub-terahertz range.

This chapter begins by introducing the operational principles of the distributed amplifier, focusing on the theoretical basis of its design. It then presents the conventional DA architecture, followed by an analysis of performance limitations and trade-offs. Next, the chapter surveys several DA topologies and highlights their respective advantages and limitations. Finally, this chapter concludes with a detailed examination of area reduction techniques for reducing areas occupied by the passive devices.

2.1.1 Operation Principles

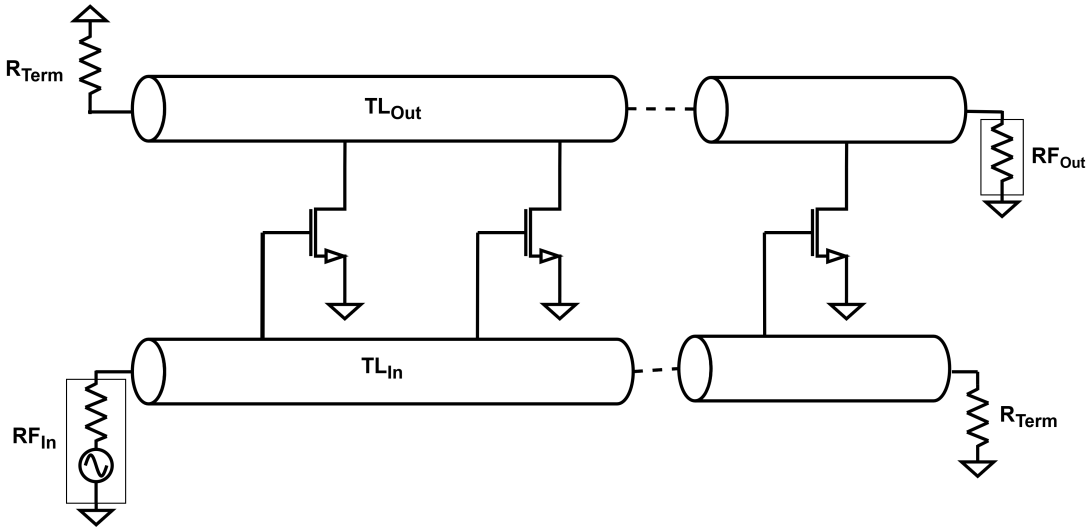

Figure 2.1 Distributed amplifier with transmission line.

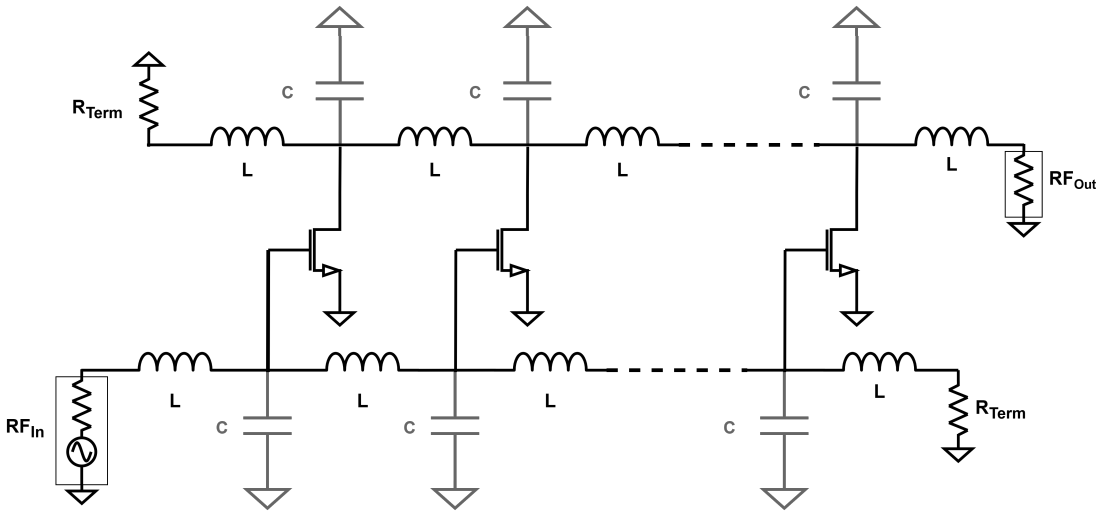

Figure 2.2 Distributed amplifier with lumped elements.

In distributed amplifiers, transconductive stages (gain cells) are arranged in parallel. These stages are made up of transistors, and before integrated circuits (IC), vacuum tubes were used as amplifiers. These stages are interconnected to each other either by ATLs or inductors at their input and output lines, shown in Figure 2.2 and Figure 2.1. In this topology, the input signal propagates along the gate line. The input wave then reaches each gain-cell gate after a fixed delay introduced by the preceding line section. Each delay section lies between adjacent gain cells, and the gate line is terminated by a resistor at its far end.

As the input signal moves along the gate lines, it sequentially activates the gain cells one by one. In the same sequential order, each activated gain cell creates an output current into the drain line. Equal per-section delays keep all drain currents in phase, so they combine coherently at the output..

Meanwhile, backward propagating signals are also generated, as depicted in Figure 2.3. Half of the signal propagates toward the output, while the other half moves in the reverse direction. As shown in Figures 2.2 and 2.1, a termination resistor at the drain line absorbs the backward-traveling wave and eliminates reflections or unwanted feedback.

Because the output signals from each gain cell add linearly, the total voltage gain scales approximately with the number of active stages. The fundamental gain expression of an ideal distributed amplifier is given in Eq. 2.1.

$$A_v(w) = \frac{1}{2} N g_m(w) Z_0 \quad \text{(Razavi, 2002)} \tag{2.1}$$

Eq. 2.1 assumes the gain expression for an ideal, lossless distributed amplifier in which each gain stage contributes equally to the output signal. The transconductance of each gain stage is denoted by g_m, the characteristic impedance (Z_0) of the ATLs, and the number of gain cells by N. The formula makes the assumptions that there are no losses in the active devices or ATLs, and that the propagation delay between the gate and drain lines is exactly equal. Under such conditions, the voltage contribution from each gain cell arrives in phase and adds coherently at the output, resulting in a total gain that scales linearly with N.

However, because real transmission lines have conductor and dielectric losses, Eq. 2.1 overestimates gain in practical designs. In actual designs, it is impossible to create lossless elements due to parasitic losses, resistances, and dielectric losses, and limited quality factor (Q) that all degrade the signal while propagating.

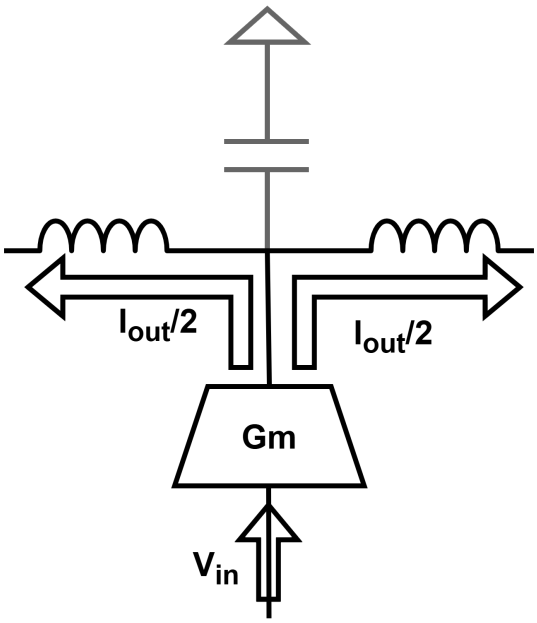

Figure 2.3 Output current after each gain-cell.

Two main implementation strategies are commonly used: transmission-line-based and lumped-element-based distributed amplifiers. Among these, transmission-line-based designs are more prevalent in DA applications, as they allow wider response and better DC behavior. Transmission lines are basically periodic LC sections that approximate the behavior of a continuous flow.

In transmission-line implementations, the attenuation constant αquantifies the exponential decay of signal amplitude per unit length caused by conductor and dielectric losses. As input and output signals propagate through the gate and drain lines, they experience signal degradation. This signal degradation is significantly increasing with the frequency f and propagation distance l_u. The resulting voltage gain of a distributed amplifier with lossy transmission lines is given by the expression in Eq. 2.2, which incorporates these loss mechanisms by including α, n, and l_u to quantify the cumulative attenuation effect across all stages.

$$A_v(w) \approx \left(1 - \frac{\alpha(w) n l_u}{2}\right) \cdot \frac{n g_m(w) Z_0}{2} \quad (Razavi,\ 2002) \tag{2.2}$$

A power gain approximation for transmission-line-based DAs was first presented in 1982 (Ayasli, Mozzi, Vorhaus, Reynolds & Pucel, 1982). By applying the same parameters as defined in Eq. 2.2, this approximation captures the non-linear effect of signal loss along the gate line. It provides an estimated value for practical power

gain and shows that, unlike voltage gain, the power gain does not increase linearly with stage number. Instead, it reflects the attenuation impact more accurately, especially at higher frequencies or when more stages are added.

$$G \approx \frac{g_m^2 n^2 Z_0^2}{4}\left(1-\frac{\alpha_g l_g n}{2}+\frac{\alpha_g^2 l_g^2 n^2}{6}\right)^2 \quad (Ayasliet\ al.,\ 1982) \tag{2.3}$$

Depending on the frequency range that the design is intended to work in, the transmission lines might be too long, and the length increase is not area efficient. As discussed previously, the main problem of DA is area consumption, and designs do not want a large area with the combination of transmission lines, high attenuation at low frequencies compared to an inductor. Inductors become a feasible solution below 100 GHz. As a result, designers can adopt lumped-element equivalents of transmission lines using inductors and parasitic capacitors for wave propagation. In this method due to per node capacitance is controlled by the parasitic capacitances of the transistor and inductor. The drain and gate line inductors need to use different inductance values to optimize delay to increase gain, in which literature examples use different inductance values for gate and drain lines(Tarar, Qayyum, Ali & Negra, 2024). As a result, the combination can behave like ATLs that replicate the behavior of transmission lines by segmenting them into cascaded LC sections, which can be seen in Figure 2.2. The shaded areas in the figure represent the aggregated parasitic components.

In lumped DA design, a significant portion of the shunt capacitance arises from the transistor gate-source capacitance C_{gs}, which is inherent to each gain cell. Similarly, the inductance L may be realized using compact integrated inductors. Thus, the total per-section capacitance and inductance are defined by both passive devices(inductors or TLs) and the active device parasitic.

The characteristic impedance of the gate line Z_g, which determines signal matching and power division, can be expressed in Eq. 2.4.

$$Z_g = \sqrt{\frac{L_g}{C_g+\frac{nC_{gs}}{l_g}}} \quad (Razavi,\ 2002) \tag{2.4}$$

Here, L_g is the series gate inductance per section of transmission line or inductor, C_g is the added lumped capacitance from either transmission line or inductor, C_{gs} is the intrinsic gate-source capacitance of the transistor which related to its size,

and l_g is the physical length of the gate delay section. This equation reflects how the characteristic impedance of the gate line is influenced not only by the designed passive values but also by transistor parasitics.

The values of L and C used in gain expressions are similarly derived based on transmission line principles. The per-section values are selected to meet the desired Z_0 and time delay t_d, following the classic relations in Eq. 2.5.

$$Z_0 = \sqrt{\frac{L}{C}}, \quad t_d = \sqrt{LC} \tag{2.5}$$

Solving these equations simultaneously allows the designer to extract appropriate values for L and C for each delay section:

$$L = t_d Z_0, \quad C = \frac{t_d}{Z_0} \tag{2.6}$$

Once extracted, these values can be adjusted, ensuring that the ATL maintains both the desired impedance and the appropriate propagation delay per section. Ultimately, the interaction between the capacitances of the active device and the passive layout choices dictates the true behavior of the lumped transmission structure. Also, Eq.2.6 shows an important perspective to increase the Z_0 which is linked to the t_d, L needed to increase this creates a relationship of delay to gain which will be talked about in later chapters.

Although this approach enables compact implementation, it introduces non-negligible loss mechanisms due to finite inductor quality factor Q_L. Each inductor adds resistive loss, which causes signal degradation at every stage. The Q is defined as Eq. 2.7, where R is the series resistance of the inductor:

$$Q_L(\omega) = \frac{\omega L}{R} \tag{2.7}$$

Unlike TL-based models, which treat loss as a continuous parameter α, lumped-element lines incur discrete stage-by-stage losses. This cannot be modeled with a global line loss. Instead, the gain reduction compounds at each stage as a result of this resistive loading. The correct gain expression is shown in Eq. 2.8:

$$A_v(\omega) \approx \frac{n g_m(\omega) Z_0}{2} \cdot \left(\frac{Q_L}{\sqrt{Q_L^2 + 1}} \right)^n \tag{2.8}$$

This expression captures how the signal weakens in stages as a function of Q_L. For example, even with $Q_L = 10$, total gain drops by more than 5% for 10 stages. This effect gets worse as n increases. Therefore, choosing an appropriate Q_L is not critical as values between 8 and 15 are typically enough to keep gain degradation minimal while still enabling compact inductor designs.

Finally, a critical factor in achieving effective signal transfer and broadband performance in distributed amplifiers is impedance matching. Both the gate and drain lines must be terminated with resistive loads matched to the line's Z_0. These terminations prevent the reflection of backward-propagating signals, which would otherwise interfere destructively with forward signals and introduce frequency-dependent standing waves. Proper impedance matching ensures clean summation of output signals, wideband frequency response, and stable operation without external tuning networks, a fundamental advantage of distributed amplifier topologies.

2.2 Performance Limitations and Trade-Offs

2.2.1 Number of Stages vs. Delay and Gain

Many gain cells are used in a distributed amplifier. Each cell gives a small voltage step, A_{cell}, that is less than what one LC-matched stage can give. The total gain goes up with the number of stages, N, because the drain currents add in phase.

$$A_v(N) = N\, A_{\text{cell}} \tag{2.9}$$

Every gate–drain section adds the same electrical delay, τ. The longest signal path—starting at the first cell—therefore extends by roughly $N\tau$.

$$\tau_{\text{total}} \approx N\,\tau \tag{2.10}$$

For a single cell, the upper 3-dB point is set by its RC pole.

$$\text{BW}_{\text{cell}} \approx \frac{1}{2\pi R C_{\text{eff}}} \tag{2.11}$$

In a full DA, the real bandwidth limit comes from the ATL, because the gate and drain parasitics are spread along the line instead of being lumped at one node. With inductance L' and capacitance C' per unit length, line length l, and extra shunt term $C_{\text{in,out}}$, the cut-off is Eq.2.12

$$f_{\text{cutoff}} = \frac{1}{\pi\sqrt{L'l\,(C'l + C_{\text{in,out}})}} \tag{2.12}$$

Gain and delay rise together, so their ratio is independent of stage count.

$$\frac{A_v(N)}{\tau_{\text{total}}} = \frac{A_{\text{cell}}}{\tau} \tag{2.13}$$

More stages, therefore, give higher gain and longer delay, while usable bandwidth stays almost the same, so long as the transistor f_T is comfortably above the line cut-off.

$$\boxed{\text{Gain} \uparrow,\ \text{Delay} \uparrow,\ \text{Bandwidth} \approx \text{constant}} \tag{2.14}$$

2.2.2 Noise

In distributed amplifiers, noise sources are typically grouped into two categories, which are transistor noise and thermal noise generated by passive components such

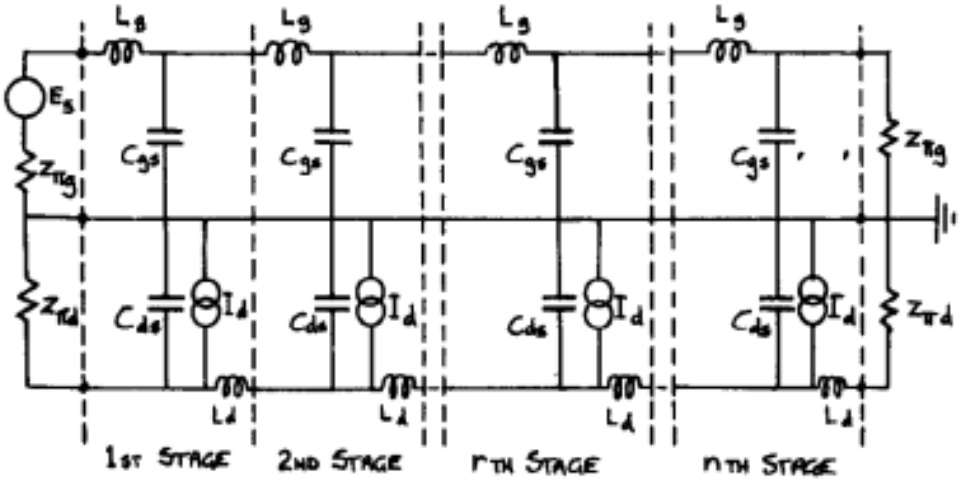

Figure 2.4 MESFET distributed amplifier model for noise analysis.(Aitchison, 1985)

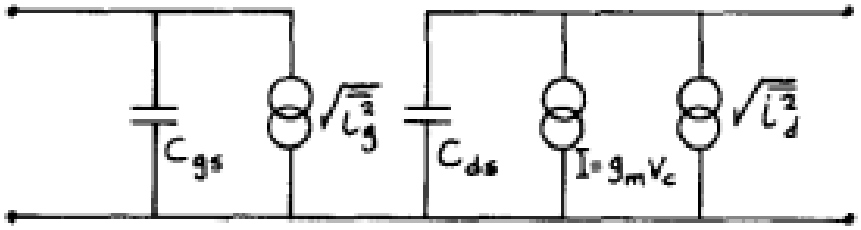

Figure 2.5 MESFET small signal model for noise analysis.(Aitchison, 1985)

as termination resistors. Transistors contribute drain noise, gate-induced noise, flicker noise, and, in some cases, popcorn noise, which is more common in junction-based devices(Lee, 2003).

In 1985, Aitchison calculated the intrinsic noise of metal–semiconductor field-effect transistor(MESFET) based distributed amplifiers, and he defined four noise sources for it, which can be seen in Fig. 2.4 and 2.5. These are gate-source impedance noise, gate load termination resistance, drain load resistance, and internal noises from transistors. Also, in calculations of lossless transmission lines or passives, it is assumed that perfect matching and per-section delay on gate and drain lines ($\beta_g = \beta_d = \beta$) can be used to find reverse and forward power gain calculations.

The forward and reverse available power gains under ideal matching are defined, respectively, as:

$$G_f = \frac{n^2 g_m^2 Z_{\pi g} Z_{\pi d}}{4} \quad (Aitchison,\ 1985) \tag{2.15}$$

$$G_r = \frac{g_m^2 Z_{\pi d} Z_{\pi g}}{4} \left(\frac{\sin n\beta}{\sin \beta} \right)^2 \quad (Aitchison,\ 1985) \tag{2.16}$$

Unlike lumped amplifiers, the repeating structure of distributed amplifiers allows noise from one transistor to propagate both forward and backward through the transmission line network. As a result, accurate noise analysis must include forward and reverse gain, as shown in Eq. 2.15 and Eq. 2.16.

The total noise factor was derived by summing the available noise powers from four main sources, which are source resistance, input termination resistor, drain termination resistor, and gate/drain noise. The final expression of Aitchison's for noise factor F is given by Eq.2.17.

$$F = 1 + \left(\frac{\sin N\beta}{N \sin \beta} \right)^2 + \frac{4}{N^2 g_m^2 Z_{\pi g} Z_{\pi d}} + \frac{Z_{\pi g} \omega^2 C_{gs}^2 R}{N g_m} \sum_{r=1}^{N} f(r,\beta) + \frac{4P}{N g_m Z_{\pi g}} \tag{2.17}$$

The phase shift per section β and the cutoff frequency ω_c of the LC ladder are defined as:

$$\beta = 2 \sin^{-1} \left(\frac{\omega}{\omega_c} \right) \tag{2.18}$$

$$\omega_c^2 = \frac{4}{LC} \tag{2.19}$$

The characteristic impedances of the drain ladder and gate ladder are $Z_{\pi d}$ and $Z_{\pi g}$, respectively, in Eq. 2.17. The gate-source capacitance is denoted by C_{gs}, the gate resistance by R, and the drain noise factor by P. Each gain cell's positional noise contribution is taken into account by the function $f(r,\beta)$, which has the following definition:

$$f(r,\beta) = ((N - r + 1)^2 + \frac{\sin(r-1)\beta}{\sin \beta})^2 + \frac{2(N - r + 1) \sin(r-1)\beta \cos(r\beta)}{\sin \beta} \tag{2.20}$$

Each term in Eq. 2.17 represents a different noise source in the distributed amplifier. The first one is the basic thermal noise from the source, which is always there, no matter what kind of amplifier you're using. The second term comes from the gate termination resistor, and it follows a sinusoidal shape, and it's important at low frequencies but fades out as frequency increases. The third one is the noise from the drain termination on the left-hand side, but since it does not get amplified, it is usually very small. The fourth term is from gate-induced noise in the transistors, and this one becomes more significant at high frequencies. The last term is the noise coming from the drain side of the transistors, and it's scaled by a factor P depending on the device.

However, the Aitchison model has key flaws. He assumed that the noise power spectral density is simply the squared magnitude of the Fourier transform of the noise current, which is not valid for random processes. This leads to inaccurate results, especially at high frequencies. He also ignores the partial correlation between gate-induced and channel noise.

Heydari fixes both issues. He calculates the autocorrelation of the output noise and then applies the Fourier transform to get the correct power spectral density. His model includes all major noise sources, including gate and drain termination noise, gate-induced noise (with correlation), channel noise, and flicker noise. It also handles forward and backward noise propagation more rigorously (Heydari, 2007).

The total noise factor he derives is the following:

$$F_{\text{tot}} = 1 + F_{\text{flicker}} + \frac{1}{(N g_m Z_T)^2} + \left(\frac{\sin N\beta}{N \sin \beta}\right)^2$$
$$+ \frac{\gamma}{N g_m Z_T}\left(1 + \frac{2N^2+1}{3}\left|\frac{\kappa_c}{c}\right|^2\left[(\omega\tau_{GS})^2 + 2N\kappa_c(\omega\tau_{GS})\right]\right) \quad (Heydari,\ 2007) \tag{2.21}$$

Compared to Eq. 2.17, this expression is more accurate and includes real CMOS effects like correlated noise and flicker. It's also validated by measurements, making it more reliable for design.

2.2.3 Linearity

Linearity is a critical performance criterion in distributed amplifiers (DAs), especially for ultra-wideband systems where signal distortion directly impacts system fidelity. Among various nonlinearity metrics, third-order intermodulation distortion (IM3) is particularly important due to its proximity to the desired signal band in two-tone tests. In DAs, the dominant source of non-linearity is the higher-order behavior of the transistor transconductance, particularly the third-order coefficient g_{m3}.

Unlike cascaded amplifier topologies, where additional stages tend to degrade linearity at constant output power, distributed amplifiers benefit from improved linearity as the number of stages increases. This improvement stems from the coherent summation of fundamental tones across stages, while the intermodulation components add incoherently. As a result, the carrier-to-intermodulation power ratio (C/IM3) increases significantly with stage count, making DAs inherently more linear under large-signal conditions. This behavior is quantitatively described by the following expression derived in (Aitchison & Mbabele, 2001):

$$\frac{C}{\text{IM3}} = \left(\frac{g_{m1}^3}{3k^2 g_{m3}}\right)^2 n^4 e^{-2n\alpha_d} \tag{2.22}$$

Here, g_{m1} and g_{m3} are the first- and third-order transconductance coefficients, k is a constant determined by bias and input amplitude, n is the number of stages, and α_d denotes the drain line attenuation in nepers per section. As seen in Eq. 2.23, the linearity improves with n^4, but is counteracted by the exponential decay introduced by line losses. However, simulations on the paper proved that the number of stages improves significantly the linearity. In five stage one compared to the one staged distributed amplifier improvement is 25 dB which a significant linearity improvement.

Linearity is a key requirement for distributed amplifiers (DAs), especially in ultra-wideband designs where intermodulation products fall inside the signal band and cannot be filtered. The dominant nonlinearity in DAs stems from the device transconductance, with the cubic term g_{m3} driving IM3 in two-tone tests. Unlike cascaded topologies—where adding stages typically hurts linearity at a fixed output level—DAs improve with stage count because fundamentals add coherently while IM3 terms add incoherently. As a result, the carrier-to-IM3 ratio rises sharply with n; for example, in literature reports roughly a 25 dB improvement going from a single-stage to a five-stage DA (Aitchison & Mbabele, 2001). This behavior is

captured by the expression derived in 2.23

$$\frac{C}{\text{IM3}} = \left(\frac{g_{m1}^3}{3k^2 g_{m3}}\right)^2 n^4 e^{-2n\alpha_d}, (Aitchison\&Mbabele,\ 2001) \tag{2.23}$$

where g_{m1} and g_{m3} are the first- and third-order transconductance coefficients, k is a scaling constant set by bias and input amplitude, n is the number of stages, and α_d is the drain-line attenuation per section (nepers). As seen in Eq. 2.23, linearity improves with n^4 but is penalized by the exponential loss term $e^{-2n\alpha_d}$ however the effect of loss term do not match the improvement of stages.

2.3 Distributed Amplifier Topologies

In this part of the chapter, distributed amplifier topologies will be discussed, along with their pros and cons.

2.3.1 Conventional Distributed Amplifier

Distributed amplifiers, as covered in the previous section, allow constructive signal propagation across multiple parallel gain paths, thereby overcoming the gain-bandwidth product limitation of individual transistors. Figure 2.6 depicts a typical conventional distributed amplifier; the number of parallel cells can change based on the desired performance. Each G_m cell in a conventional architecture has only one active stage, usually a common-source transistor. These G_m cells are connected by transmission lines or inductors, which, when combined with the G_m cell's inherent parasitic capacitances, create ATLs. Broadband operation is made possible by these ATLs, which facilitate synchronized wave propagation along the gate and drain networks. Examples of this conventional or common source DA on Gallium Nitride (GaN) (Hu, Zhang & Ma, 2022) and bulk CMOS (Tsai, Wang, Kuan & Chang, 2005) technologies can be found in the literature.

The ideal voltage gain of a conventional DA, with the assumption of lossless ATL and matched termination, can be seen in Eq. 2.24.

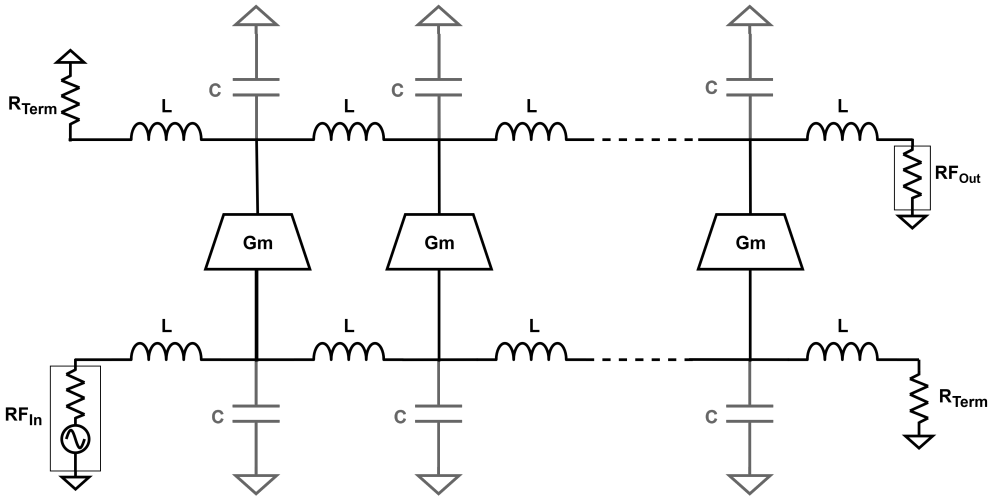

Figure 2.6 Conventional distributed amplifier with gain cell as Gm (transconductance).

$$A_v(w) = \frac{1}{2} N G_m(w) Z_0 \quad \text{(Razavi, 2002)} \tag{2.24}$$

N is the number of gain stages, Z_0 is the characteristic impedance, and $G_m(\omega)$ is each cell's effective transconductance. Because of the traveling-wave nature of the signal, only half of its power reaches the load, which results in the $\frac{1}{2}$ factor.

2.3.2 Cascode Distributed Amplifiers

Cascode distributed amplifier is the most widely used architecture in G_m cell design (El-Chaar, Vincent, Arnould, de Souza, Bourdel & Podevin, 2022). It uses stacked transistors in each G_m cell to improve gain and high-frequency stability. By replacing a single common-source stage with a common-source stage stacked with a common-gate transistor. It can be seen in Fig. 2.7. This structure can suppress the Miller effect (Fang, Levy & Buckwalter, 2016), increase output resistance (Fang et al., 2016; Wu, Kao & Chu, 2022), enhance gain (El-Aassar & Rebeiz, 2019a), and improve reverse isolation (El-Chaar et al., 2022), making it more suitable for distributed amplifier implementations.

In the literature, this method has been applied to nearly all popular integrated circuit (IC) technologies. Depending on the process, multi-stack configurations can also be used. These include double-stacked (Arbabian & Niknejad, 2009), triple-

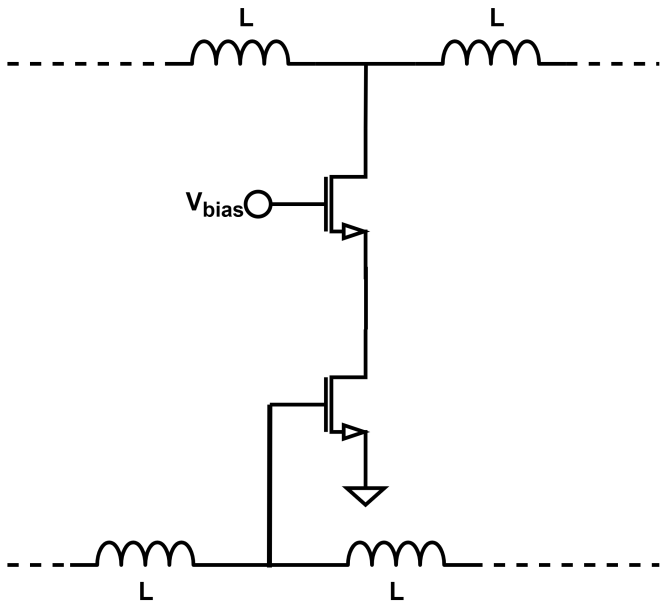

Figure 2.7 Cascode distributed amplifier.

stacked (Feng et al., 2017; Testa, Belfiore, Paulo, Carta & Ellinger, 2015), and even quadruple-stacked designs (El-Aassar & Rebeiz, 2019a,2). Cascode DAs have been demonstrated across various technologies, including bulk CMOS (Arbabian & Niknejad, 2009; Feng et al., 2017; Jahanian & Heydari, 2012), silicon-on-insulator (SOI) CMOS (El-Aassar & Rebeiz, 2019b,2), Indium Phosphide (InP) heterojunction bipolar transistor (HBT) (Nguyen, Cui, Nguyen, Stameroff & Pham, 2023), SiGe Bipolar CMOS(BiCMOS) (Testa et al., 2015), and Gallium arsenide (GaAs) (Hu, Ma, Xie, Liu & Feng, 2024).

However, cascode structures introduce increased power consumption, voltage headroom requirements, and layout complexity, especially in low-voltage technologies.

2.3.3 Inductive Peaking Techniques

In the literature, there are two types of inductive peaking techniques, which are interstage inductive peaking and gate inductive peaking. The interstage method is most commonly used among the peaking methods. It is used in cascode topologies between common-source and common-gate transistors. This methodology focuses on the isolation of internal capacitance in that node and affects the response of G_m cells by increasing its effect at higher frequencies where transconductance usually drops. Heydari et al. (Heydari & Safiallah, 2023) showed that a simple interstage

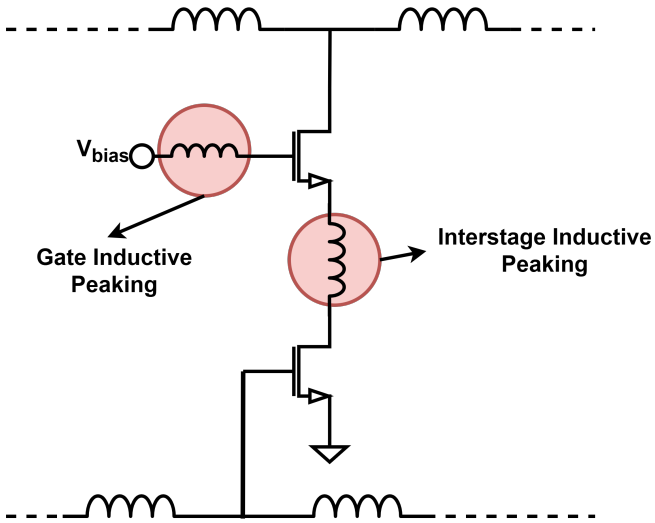

Figure 2.8 Cascode distributed amplifier with inductive peaking in circular.

inductor can increase the bandwidth of a cascode stage by several gigahertz. Even in multiple stacked cascode amplifiers, the increased number of inter-stage peaking has an increasing effect on the G_m (Testa et al., 2015).

Gate inductive peaking is another way to do transconductance peaking in higher frequencies. In this method, an inductor is placed in the gate of the common gate transistor in Fig. 2.8. As previously discussed, the main problem of the transconductance drop is the capacitances, and this gate inductor can be able to pull the second gm peaking that is in the sub-terahertz region, which can be seen in Fig. 2.9. This way, bandwidth is increased significantly (Feng et al., 2017)

However, increased transconductance from the inductive peaking may result in instability (Kim, 2019). Therefore, the designs should be checked for perfect stability. Also, a major problem arises with peaking, which is the increased area usage from the inductors.

2.3.4 Tapered Structures

In a distributed amplifier, half of the drain current from every G_m cell flows into the drain termination, reducing the available output power by approximately 3 dB. This will significantly reduce the overall efficiency, especially in highly efficient designs. However, that termination resistor simplifies the design by improving stability and eliminating reflections.

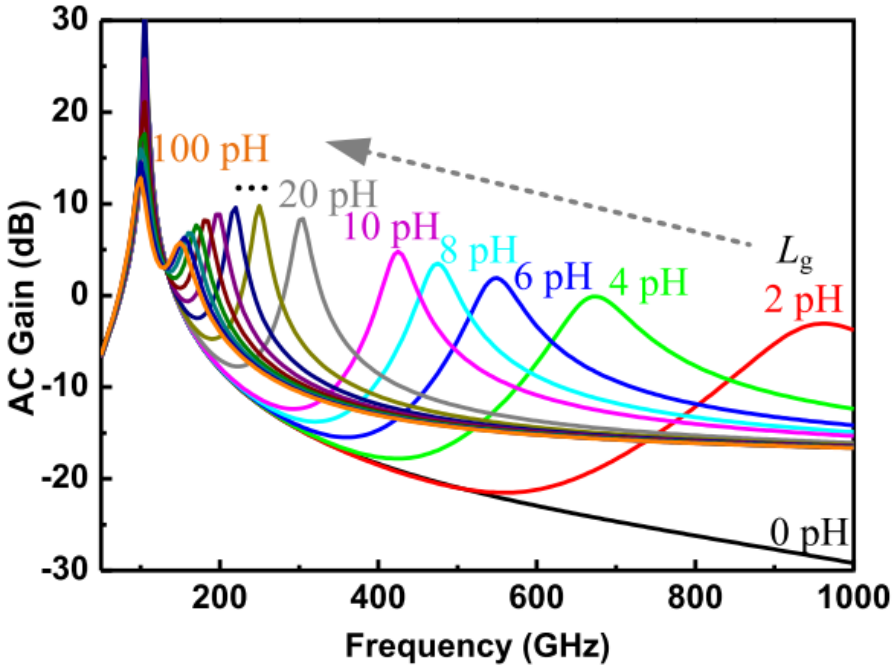

Figure 2.9 Effect of gate peaking in various technologies (Feng et al., 2017).

If the design is transmission line-based, this lost current can be saved using tapering the drain transmission line. Instead of using a uniform Z_0 transmission line, tapered structures gradually reduce the impedance stage by stage toward the output. When properly designed, this allows the reverse wave from each cell to be canceled by the left-going wave of the next cell (Ginzton et al., 1948). A commonly used tapering strategy scales the impedance of each drain section inversely with its position, as shown in Eq. 2.25. The schematic design of tapering can be seen in 2.10.

$$Z_k = \frac{Z_0}{k} \tag{2.25}$$

This method is implemented in a cascaded CMOS distributed amplifier using tapered interstage lines. Their results show a gain improvement of more than 6 dB compared to flat-line designs. As the tapering factor increases, gain and efficiency also improve. This method also increases bandwidth with an increase in the tapering coefficient of the design (Tarar et al., 2024).

Tapering helps eliminate the power reduction in internal terminations, but it requires careful design steps due to different transmission lines needed to design, layout parasitics, and loading. The advantageous parts of tapering are only achieved when these factors are well-optimized.

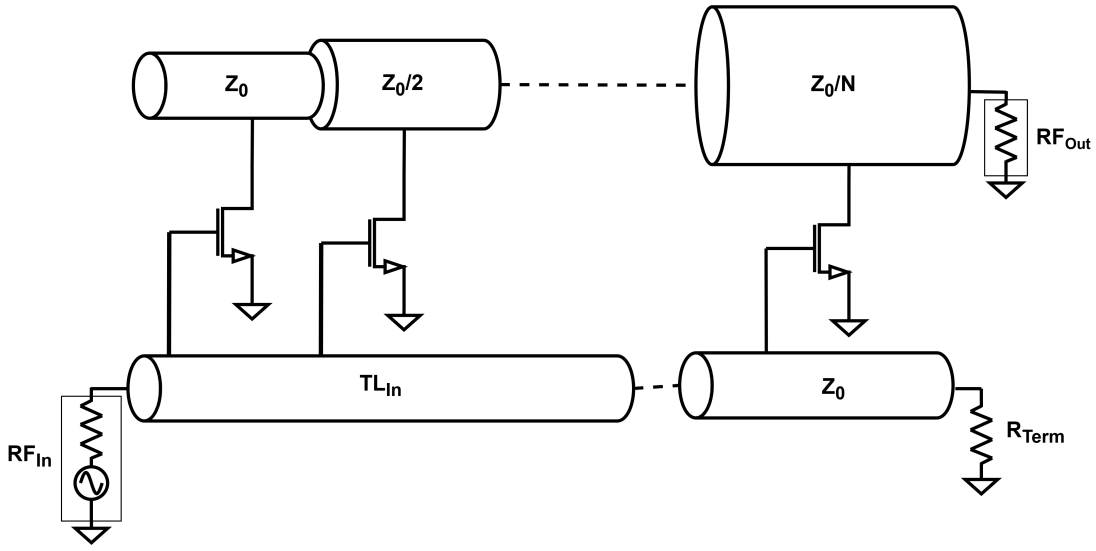

Figure 2.10 Tapered DA

2.3.5 Feedback-based distribute amplifiers

In distributed amplifiers, signal loss at higher frequencies is one of the main limitations that reduces gain. Since extending bandwidth is a key goal, many studies focus on compensating for this loss. Common approaches are to either increase the effective transconductance or boost the signal directly through feedback. This has led to two main feedback techniques: intra-stack coupling and ATL coupling.

The first method, intra-stack coupling, is shown in Fig. 2.11. In this structure, the gate peaking inductor and the interstage inductor within the cascode G_m cell are coupled. This coupling method helps recover the power of the lost signal due to parasitic capacitance at the cascode node and effectively boosts the transconductance G_m at higher frequencies (El-Aassar & Rebeiz, 2020a; Lee, Park, Choi, Liu & Wang, 2023). This boosting is done by changing the common gate amplifier to work as a common source amplifier and adding a boost to the design. However, since this is a form of positive feedback, it can reduce the stability of the system, so the design must be carefully checked for stability parameters.

The second feedback method, shown in Fig. 2.12, couples the ATLs, inductor or transmission line based, to the gate and drain. This technique focuses on loss along the gate line at higher frequencies. As the signal propagates in the gate line, it weakens due to lossy behavior in the ATL at the higher frequencies. By introducing coupling between the gate and drain lines, this method aims to reinforce the input signal that moves on the gate line and improve gain in the later stages by increasing the signal from the train line of the amplifier (Hsiao, Su & Hsu, 2013; Lee et al.,

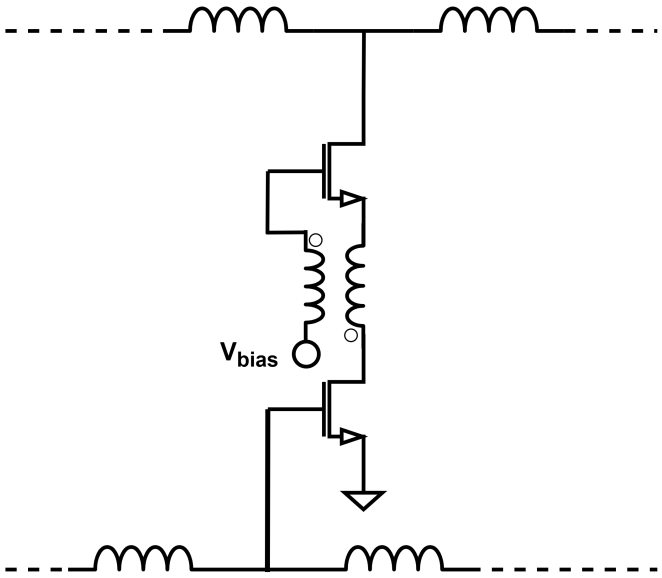

Figure 2.11 Intra-stack coupling gain cell

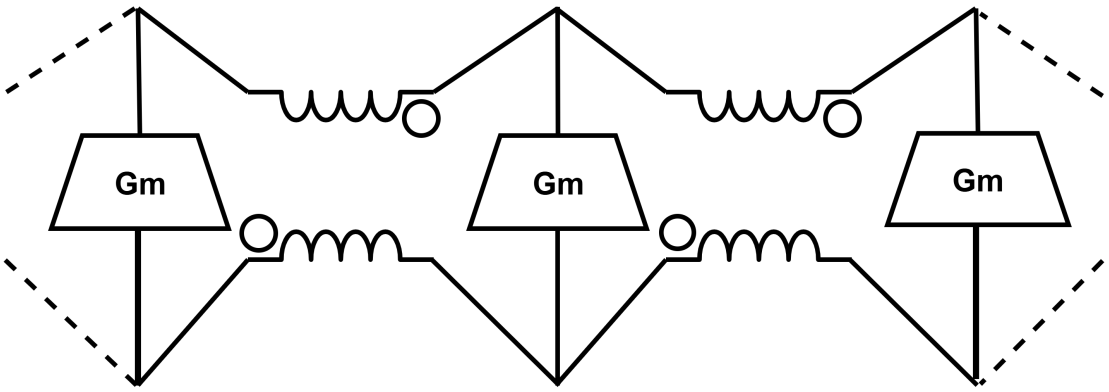

Figure 2.12 Drain-gate line coupling

2023).

2.4 Area Reduction Techniques

Distributed amplifier for UWB applications presents a major problem, which is the on-chip passive components, especially inductors and transmission lines. They are the major area consumers in our chip area. Since distributed amplifier topology inherently relies on multiple stages of lumped inductors or transmission lines to create ATLs, reduction techniques for these passives are essential for efficient area

consumption. In this section, we will be introducing key passive area reduction methods, which are slow-wave transmission lines and different shaped, lower Q, irregular layout, and stacked inductors.

2.4.1 Slow-Wave Transmission Lines

Slow-wave transmission lines (SWTL) are used to reduce the physical length of ATLs by increasing the propagation constant β, allowing a more compact design for distributed amplifiers. This is done by increasing the effective dielectric constant ε_{eff} by adding capacitive loaded structures, such as floating slot-type metals placed beneath the signal line which basically act like bumbs and slows down wave velocity and reduce the wave length.

The phase velocity v_p and effective dielectric constant ε_{eff} are related as shown in Eq. 2.26. For quasi-TEM transmission lines, ε_{eff} can also be derived from the inductance and capacitance per unit length as given in Eq. 2.27. These equations show that by increasing capacitance directly, the wave velocity can be reduced.

$$v_p = \frac{c}{\sqrt{\varepsilon_{\text{eff}}}} \tag{2.26}$$

$$\varepsilon_{\text{eff}} = \frac{L'C'}{\mu_0 \varepsilon_0} \tag{2.27}$$

Figure 2.13 shows a conventional coplanar waveguide (CPW) transmission line. While it offers simplicity, it occupies a relatively large footprint for a given electrical length due to its limited ε_{eff}. In contrast, the slow-wave transmission line structure shown in Fig. 2.14 incorporates patterned slot-type floating metals to enhance the capacitive effect and compress the line length.

To evaluate the effectiveness of the proposed structure, in paper four, SWTL variants were designed by adjusting the slot length and spacing while keeping the CPW width and gap constant (Yağmurlu & Tokgöz, 2024). Compared to a conventional CPW, the best-performing slow-wave structure exhibited approximately twice the effective dielectric constant and significantly higher propagation constant, which resulted in nearly 30% reduction in physical length. Although the loss slightly increased, the

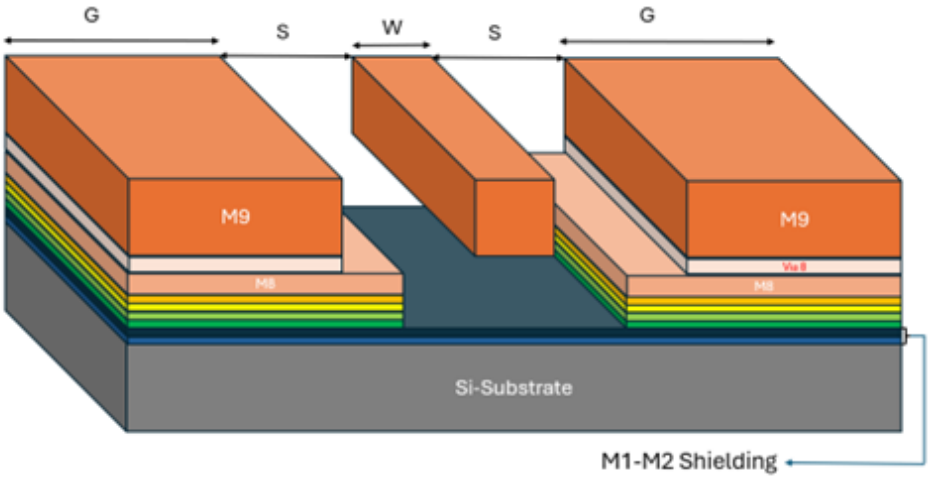

Figure 2.13 Conventional CPW transmission line (Yağmurlu & Tokgöz, 2024).

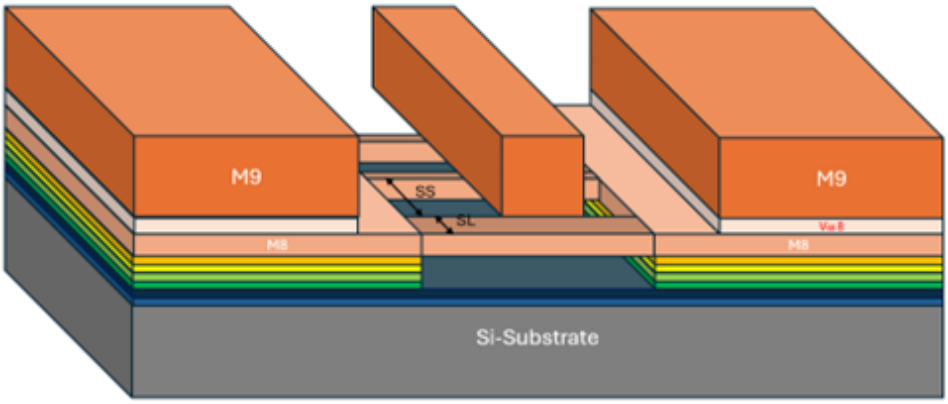

Figure 2.14 Slow-wave transmission line (SWTL) with floating slot-type metal structure (Yağmurlu & Tokgöz, 2024).

compactness and improved phase delay make the SWTL a more efficient option for mmWave distributed amplifier designs (Yağmurlu & Tokgöz, 2024).

2.4.2 Inductor Design Strategies

On-chip spiral inductors are another key area in RF integrated design. Therefore, there are lots of design strategies that aim to maximize inductance per area or otherwise reduce the inductor size. As previously discussed in CMOS DAs, it is common to use a lumped inductor for high inductance needed ATL designs, or it can be used as a peaking inductor. This widespread use led the researchers to look for minimization methods and which is crucial for designs. In this part of the thesis, we are going to review some approaches for inductors, shapes of inductors, accepting lower Q in-

ductors for size benefits, employing irregular layout, and stacking inductors. Each of the methodology provide an area of saving but with an impact on performance.

2.4.2.1 Different Shapes

The geometry of an on-chip spiral inductor influences performance and area. In the literature most commonly used shapes are square, octagonal, and circular spirals. The general rule of thumb is that if a spiral inductor is more symmetric and has a round shape, it has higher Q, while more cornered designs provide higher inductance per area.

A square spiral utilizes nearly 100% of its bounding box, while an octagonal spiral typically covers about 82–83%, and a circular spiral only about 79% (Chen & Liou, 2004). Although circular spirals offer the lowest series resistance due to the lowest distance between ports and the highest Q, they leave considerably unused area than standard rectangular layouts. While square spirals maximize inductance density, but suffer from increased resistance due to sharp corners and longer metal paths. Octagonal spirals are easier to implement than true circles, consume slightly less area than circular spirals, and only marginally compromise on Q-factor (Chen & Hsu, 2022). Also, it is important to note that in IC design, most of the technologies only offer 45 degree angle lines and 90 degree lines for drawing, which makes circular impossible to design while making an octagon, all of which are closest to a circle get their advantage.

2.4.2.2 Stacked Inductors

Stacked inductors are spiral inductors built across multiple metal layers to save area. Instead of the usual single layered inductor design, in this method parallel multiple inductors across different layers and connects to each other. In designs, usually the area below the inductors is unused, therefor stacking inductors in this way, the bottom of the inductors can be used. However, this stacking comes with the disadvantage of increased resistance due to increased line length. Thus, stacked inductors typically have a lower Q with compact designs.

In the literature, examples of stacked inductors can be seen using a 180-nm CMOS

process with four to six layer stacking. It can be seen from the results that when the stacking number increases, the inductance increases significantly. However, it reduces the Q (Yin, Xie, Kang, Shi, Mao & Sun, 2008). This is expected due to increased line length, as a result, resistivity increases worst metalizations are used, which are thinner than the top metals. Also, self-resonant frequency must be considered in design, since stacking leads to a decrease in results. (Yin et al., 2008).

3. DISTRIBUTED POWER AMPLIFIER

Distributed power amplifier (DPA) simultaneously deliver wide bandwidth and high output power, and their stage count scales with the required performance. In this work, a DPA is designed as the final stage of a transmitter. The focus is on achieving wideband gain and wideband high output power, with a compact layout using area reduction methods. The design steps, performance targets, and key trade-offs are presented in this chapter.

3.1 Design Considerations of the Power Amplifier

DAs are common in ultra-wideband applications, as previously discussed. Most of the DAs are not optimized for high output power and efficiency, which makes them unsuitable for power applications. In the literature, DPAs have been implemented using various technologies, including bulk CMOS (Kim, 2019; Tarar et al., 2024), SOI CMOS (Celik & Reynaert, 2021; El-Aassar & Rebeiz, 2019a,1,2,2), and SiGe BiCMOS (Fang et al., 2016). In this design, the DPA is intended to serve as the output stage of a transmitter. Unlike regular DAs, their designs mostly focused on producing higher output power. To achieve it, most of the time output is not matched to 50 Ω, but to a load optimized for maximum power transfer.

Area reduction is a key goal of this thesis. Therefore, to achieve this, vertically stacked and shape-optimized inductors are used to minimize layout size, accepting a lower Q as a trade-off. This enables a more compact design.

Gain cells are biased in Class-A to ensure high linearity and sufficient gain, which is the most common practice in DPAs. Input matching and unconditional stability are maintained across the entire 70 GHz bandwidth.

Recent works based on bulk CMOS, SOI CMOS, and SiGe technologies report out-

put power levels around 14 dBm and average gains of approximately 15 dB. It is worth noting that CMOS SOI-based designs benefit from higher supply voltages (e.g., 4.4 V), which contribute to improved output power and gain. In some cases, cascaded stages are also used to achieve higher gain. This work aims to exceed those performance metrics while maintaining a compact and wideband DPA architecture.

3.2 Methodology and Theoretical Calculations

3.2.1 Class-A Power Amplifier

The DPA is biased in *Class-A* to lock in linear gain over the entire band. Figure 3.1 confirms that V_{DS} and I_{DS} swing from 0 to $2V_{DC}$ and 0 to $2I_{DC}$, occupying the full 360° conduction angle. Guided by the $I_D{-}V_{GS}$ curve of the **TSMC 65-nm CMOS** process (Fig. 3.2), the gate bias is set above 0.5 V, keeping the device in saturation so distortion stays minimal while high-frequency gain remains usable. Class-A's ideal drain efficiency peaks at 50 % (Lee, 2003); although practical figures are lower, the wide linear region it delivers is indispensable for ultra-wideband DPAs.

3.2.2 G_m Peaking

Ultra-wideband DAs suffer from gain reduction at higher frequencies due to the roll-off in the transistor's transconductance, g_m. This degradation becomes significant when parasitic capacitances dominate the frequency response. To solve this problem, peaking techniques such as interstage inductive peaking and gate inductive peaking have been proposed and widely adopted in DAs. These techniques operate by introducing inductors to resonate with the parasitic capacitances, thereby flattening or boosting the frequency response. To quantitatively evaluate their effect, the frequency-dependent $G_m(s)$ of various cascode topologies is analyzed in the next paragraphs.

To begin the analysis, small-signal equivalent circuits are drawn for three different

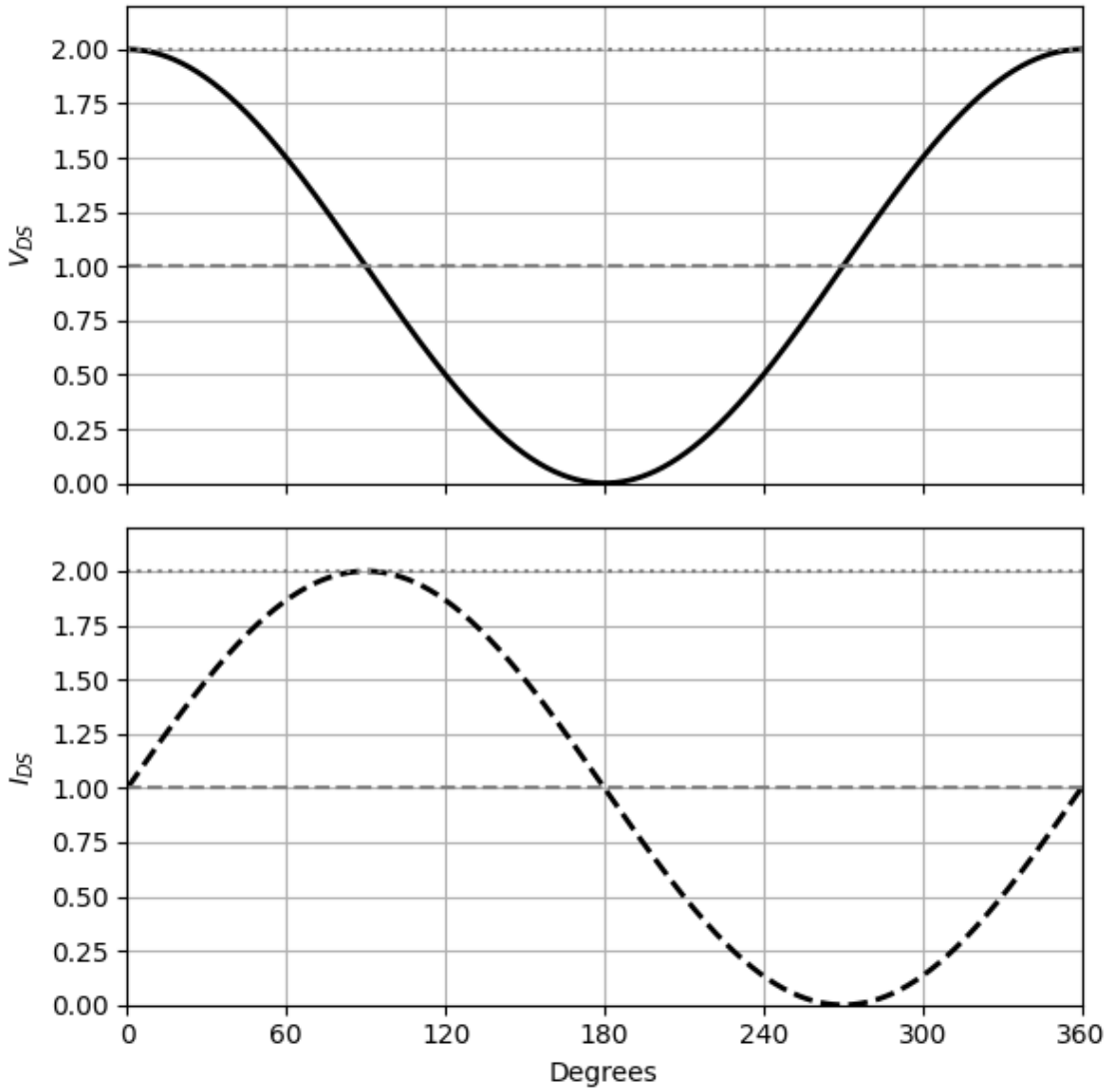

Figure 3.1 Class-A amplifier voltage and current waveforms.

cases: the conventional cascode amplifier, the interstage peaked cascode, and the fully shunt peaked cascode, which has both gate and interstage inductors. These models are illustrated in Fig. 3.3, Fig. 3.4, and Fig. 3.5, respectively. In Fig. 3.3, the standard cascode topology is shown. Fig. 3.4 introduces the interstage inductor L_p, placed between the common-source and common-gate transistors. Finally, Fig. 3.5 presents the proposed fully shunt peaked structure, in which the gate inductor L_g is added at the input of the upper transistor to further enhance high-frequency performance.

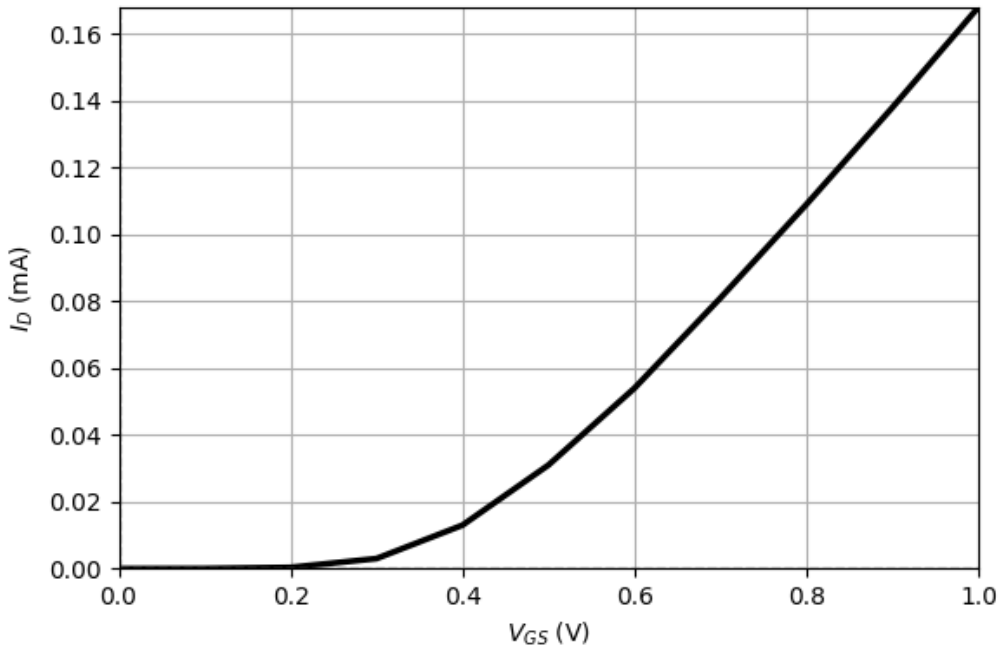

Figure 3.2 I_{ds} vs v_{gs} graph of 65-nm CMOS.

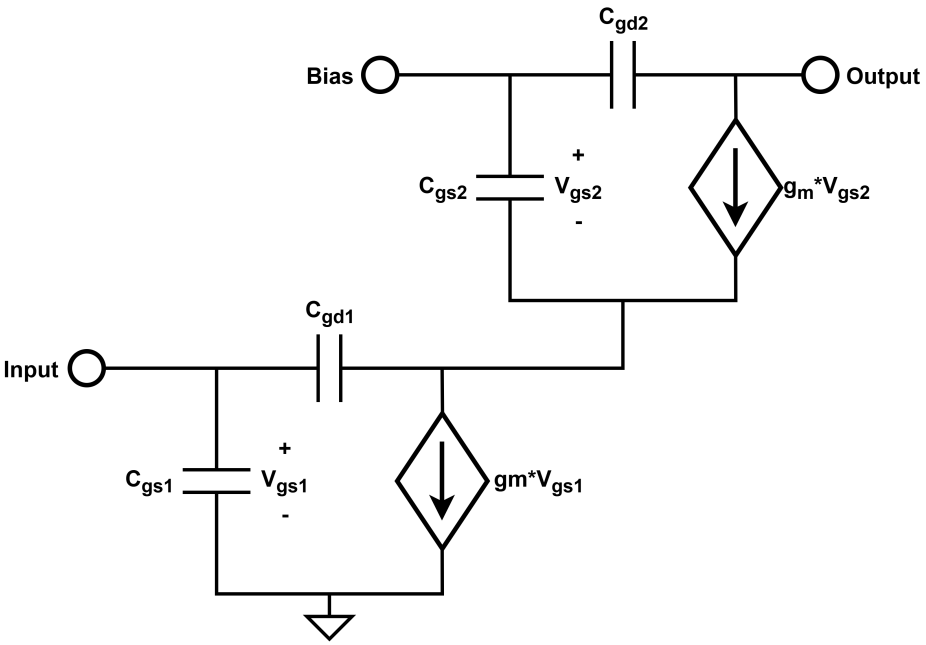

Figure 3.3 Small-signal model of cascode FET.

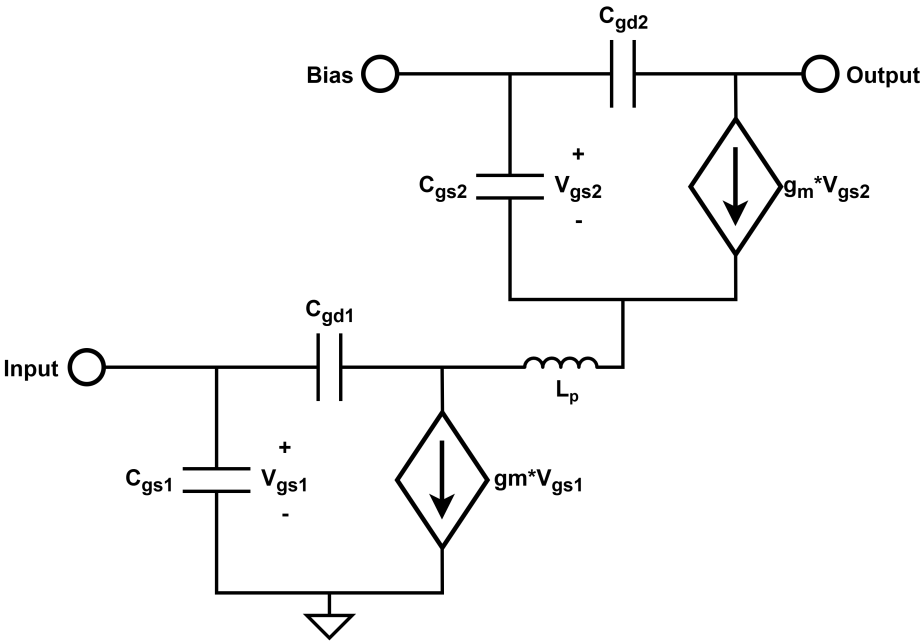

Figure 3.4 Small-signal model with interstage peaking using L_p.

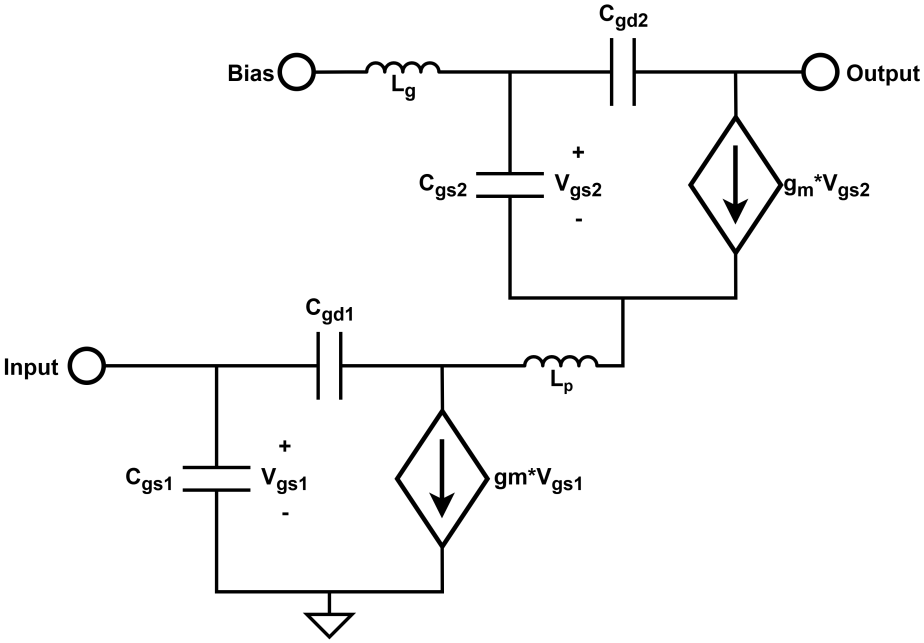

Figure 3.5 Fully shunt-peaked model with both L_p and L_g.

The corresponding analytical expressions for the transconductance $G_m(s) = \frac{I_{\text{out}}}{V_{\text{in}}}$ are derived for each configuration by applying small-signal analysis. All sources except the input are shorted, and the output is treated as a virtual AC ground. The expression for the conventional cascode is given in Eq. 3.1, where the roll-off is clearly dominated by the parasitic capacitances.

(3.1)
$$G_{m,\mathrm{reg}}(s) = \frac{g_m^2 + g_m s C_{gd1}}{g_m + sC_{gd1} + sC_{gs2}}$$

For the interstage-peaked case with L_p, the enhancement is introduced by modifying the denominator through the addition of an inductive term:

(3.2)
$$G_{m,\mathrm{int}}(s) = \frac{g_m\left(g_m + sC_{gd1}\right)}{g_m + sC_{gs2} + sC_{gd1}\left(1 + sL_p(g_m + sC_{gs2})\right)}$$

In the fully shunt-peaked case, shown in Eq. 3.3, both L_p and L_g are incorporated. The peaking effect is resulted by resonating the C_{gd2}. As seen in the equation, the inductors L_g and L_p are positioned to form resonance with parasitic capacitances such as C_{gd2}, C_{gs2}, and C_{gd1}, enhancing transconductance by compensating the capacitive roll-off.:

(3.3)
$$G_{m,\mathrm{full}}(s) = \frac{g_m\left(\dfrac{s^2 L_g C_{gs2}}{1 + s^2 L_g(C_{gd2} + C_{gs2})} - 1\right)(g_m + sC_{gd1})sL_p}{1 + \left(C_{gd1} - \frac{1}{sL_p}\right)\left[1 + \left(\dfrac{s^2 L_g C_{gs2}}{1 + s^2 L_g(C_{gd2} + C_{gs2})} - 1\right)sL_p(g_m + sC_{gs2})\right]sL_p}$$

To validate the analytical results, these expressions were evaluated using Python. Fig. 3.6 presents the computed transconductance magnitudes over frequency for all three configurations.

As expected, the regular cascode configuration shows an early decline in G_m due to the absence of peaking. The interstage-peaked version demonstrates a moderate extension of bandwidth, with slower decay in transconductance, with the exception of an increase after 100 GHz. The fully shunt-peaked version exhibits the best high-frequency performance, maintaining a higher G_m up to approximately 70 GHz. These results confirm that inter-stage peaking compensates for parasitic loss and extends bandwidth. This is achieved by establishing resonance conditions that boost the response in desired frequency bands, resulting in effective peaking behavior as seen in the plotted G_m. However, this peaking method results with reduction of stability in higher frequencies due to the upper transistor is shorted by the peaking methods which makes it behave like common source amplifier.

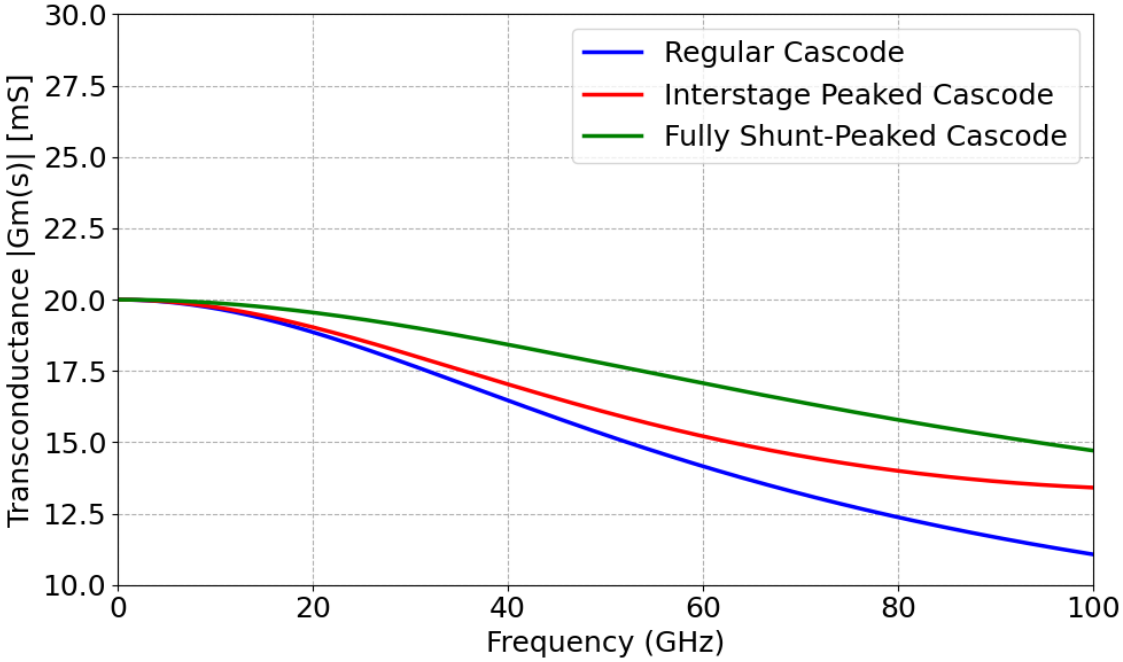

Figure 3.6 Transconductance comparison of regular, interstage, and fully peaking methods in cascode.

3.3 Proposed Design Procedures

In this section, we will discuss DAs design procedures, which can be divided into two parts: stage number optimization and passive (inductor) optimizations for area reduction.

3.3.1 Stage Number and Cascading Strategy

As previously discussed in the background, the number of stages is the most significant factor that needs to be considered in DA design. It was explained that an increased number of stages results in higher gain up to an optimal point and also increases output power. However, it comes with the trade-off of increased area and increased power consumption. Therefore, while designing DAs, the number of stages should be chosen optimally in the specifications' needs.

To determine the optimal number of stages, comparison graphs for different stage numbers needed to be analyzed. For this purpose, using Advanced Design System (ADS), DAs based on 65-nm CMOS were implemented to achieve their optimum

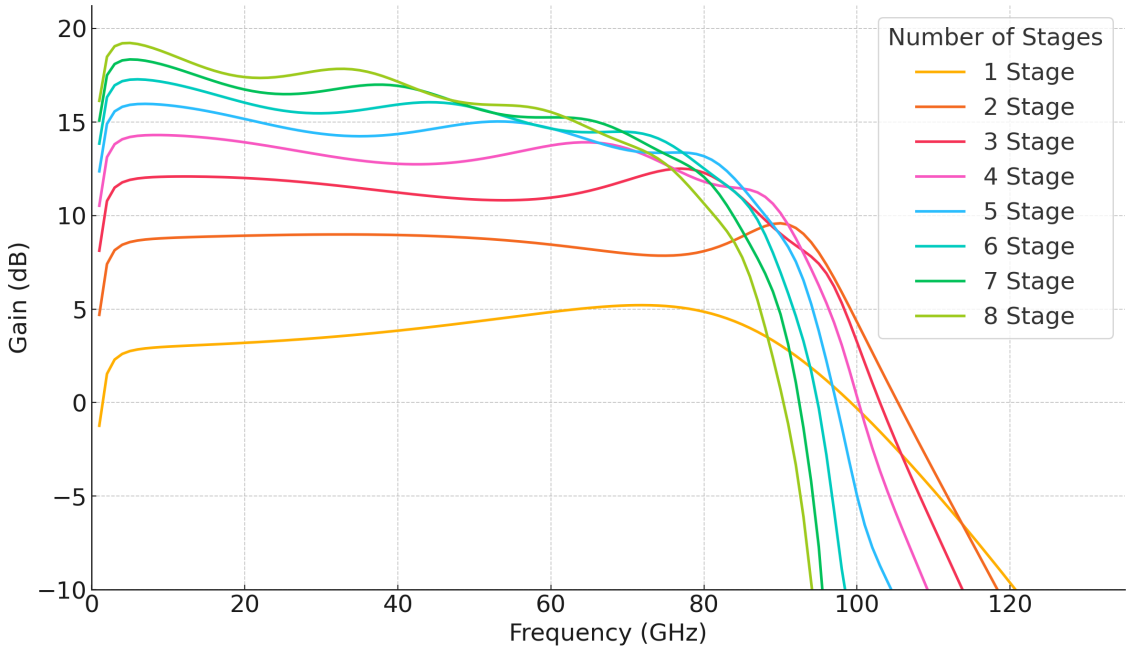

Figure 3.7 Different number of stages gain vs frequency.

gains while ensuring unconditional stability in every case. The results can be seen in Fig. 3.7.

Simulation confirms the expected gain rise with stage count. Also, proven in Eq.2.8, after a number of stages, the gain increase is no longer linearly increasing. It is expected that, if the number of stages increases gain will stagnate and even reduce. Beyond six stages, ATL parasitics reduce bandwidth. It can be seen in Table.3.1 and is supported by the background. After 6 stages, the bandwidth is no longer sufficient for the design requirements.

Table 3.1 3-dB Bandwidth vs. Number of Stages

Number of Stages	3-dB Bandwidth (GHz)
1	90.0
2	95.0
3	87.0
4	85.0
5	79.0
6	71.0
7	53.0
8	45.0

Then, the design delay was analyzed to validate the theoretical relationship between the number of stages and signal delay, as defined in Eq. 2.13. As previously discussed, increased gain should lead to increased delay as a trade-off. This is confirmed in Fig. 3.8, which is increasing with every stage. As the number of stages increases,

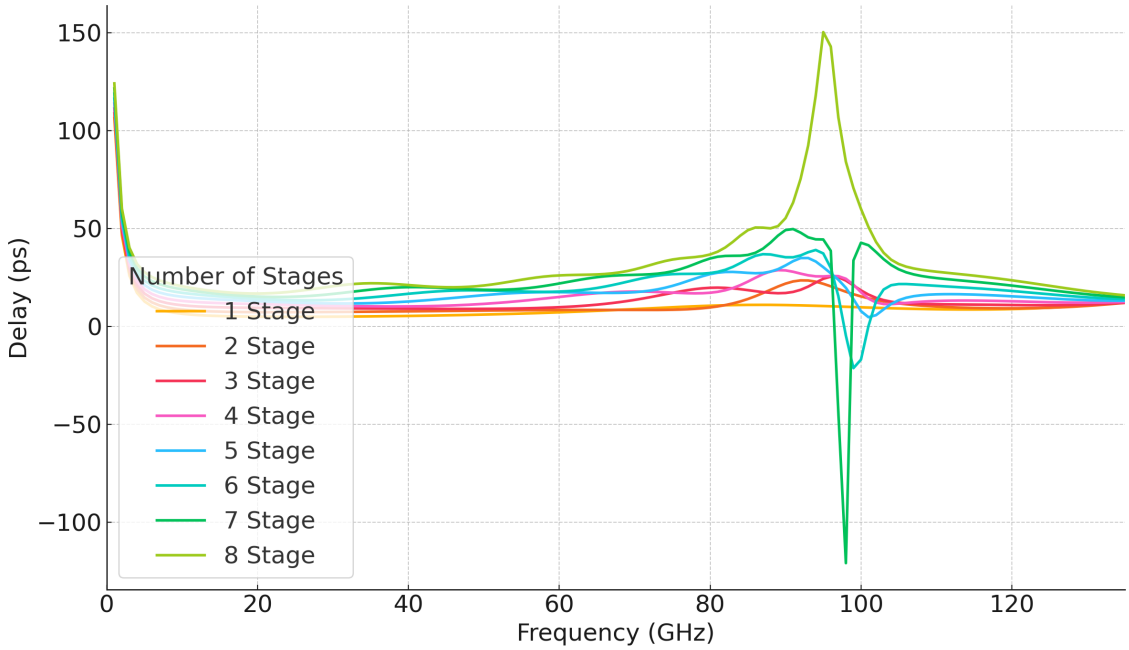

Figure 3.8 Different number of stages delay vs frequency.

the delay also increases. In the graph, the 6 and 7 stage designs show negative delay values at 99 GHz due to their band-stop filter behavior, which results from the ATLs.

Furthermore, the relationship between the number of stages and the output 1-dB compression point at 70 GHz is presented in Fig. 3.9. In theory, it is confirmed that the number of stages increases output power like a gain parameter due to each stage's contribution, but not linearly. In the figure, after 4 stages, the number is linearly increasing up to 7 stages, then starts to drop due to the loss resulting from the passives.

The results above showed that the 6 stage design best matches the target specifications of this research, providing a wide bandwidth covering 70 GHz, a high $OP_{1\text{dB}}$ of 14.3 dBm at 70 GHz, and a nearly flat gain of 15 dB across the frequency range. Therefore, this stage number is selected as the optimal point for implementing the DA.

3.3.2 Low-Quality Factor Inductor-Based Area Reduction Technique

In the background, it is discussed that inductor Q and inductance per area have an opposite relationship. Therefore, some designs have better area inductance, like a

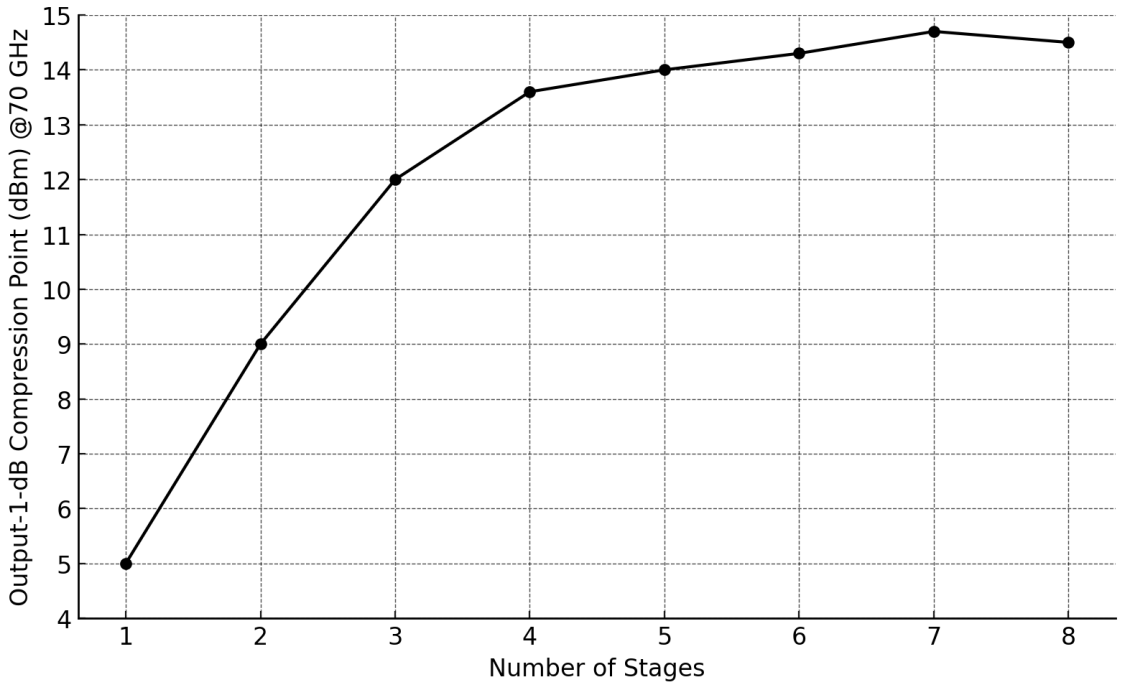

Figure 3.9 Different number of stages $OP_{1\text{dB}}$ vs frequency.

square over an octagonal inductor. One of the major disadvantageous of DAs can be reduced by this method.

This can be proved by combining bot Eq.3.3 and Eq.2.8, which, when applied with the design g_m of 56 mS, the results can be seen in Fig.3.10. In this figure, it is proven that the Q of inductors has less impact in a range of 5 to 12, and even between 8 to 12, there is less than 0.3 dB difference. Therefore, the trade of lower Q can be used to reduce the area with low loss in gain.

Figure 3.11 One turn and two turn square inductor layouts

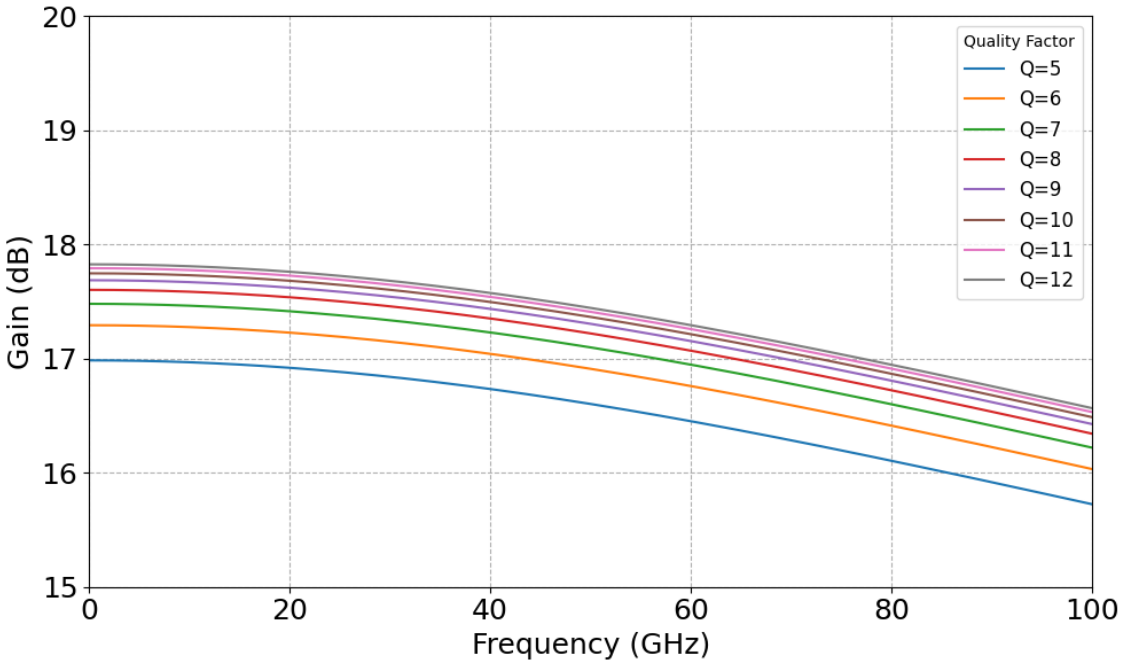

Figure 3.10 Fully Shunt-Peaked Cascode $G_m(f)$ in different Q inductors vs frequency.

Then, the proposed square inductors are designed as 1-turn and 2-turn square spiral inductors, and the layouts are presented in Fig.3.11. It is well known that the square turn number increases the inductance per area.

Table 3.2 Schematic inductor values

	Lin	**Lout**	**Lg**	**Lp**
Inductance (pH)	120	120	60	60
Q	9	9	7	7

These values are represented in the Table 3.2, the schematic inductance and Q values used in the initial circuit-level simulations. However, as the next step of design, inductance needed to be designed by Ansys HFSS to reflect realistic electromagnetic behavior.

After integration of the designed inductors in Table 3.2, it is observed that the targeted results of DA did not meet due to the parasitic effects of the real inductors did not match the perfect inductor components of ADS. As a result, several layout-level adjustments were required. These included changes in inner diameter to increase the inductance to achieve the desired performance parameters of DA while minimizing area.

The updated layout inductance values and their corresponding layout areas are presented in the following Table 3.3.

Table 3.3 Post-layout inductor values and area consumption

	Lin	**Lout**	**Lg**	**Lp**
Inductance (pH)	120	155	65	72
Q	8.4	8.9	8.5	8.4
Area (μm^2)	1681	1936	1190.25	1260.25

In conclusion, the final layout includes eight L_{in}, eight L_{out}, six L_{p}, and six L_{g} inductors. Among these, two of the L_{in} and two of the L_{out} inductors are designed with two-thirds of the original inductance value, as only half of the inductance is required in those positions. As a result, the total inductor area sums up to 39,242 (μm^2), which corresponds to 0.0392 (mm^2).

.

3.4 Simulation Results

This section presents schematic results 6-stage DPA on Fig.3.12 that uses inductors based on HFSS designs without the interconnections, focusing on key performance metrics across the 1 to 100 GHz frequency range. The parameters analyzed include input/output reflection coefficients ($S(1,1)$, $S(2,2)$), gain ($S(2,1)$), output 1-dB compression point (OP_{1dB}), saturated output power (P_{sat}), power-added efficiency (PAE) at OP_{1dB} and in max value, NF, and the stability factor (K). All simulations were conducted in ADS using TSMC 65-nm technology and the extracted S-parameters of inductors using HFSS to incorporate the effects of parasitics.

The input and output matching can be seen in Fig.3.14. The $S(1,1)$ remains below -10 dB till 67 GHz and -7 dB till 83 GHz and the $S(2,2)$ remains below -10 dB till 70 GHz and -7 dB till 85 GHz. In DAs, most of the literature uses -7 dB as a reference point for usable matching, which both $S(1,1)$ and $S(2,2)$ hold in our wanted range of above 70 GHz bandwidth. The gain $S(2,1)$, depicted in Fig. 3.13, achieves a peak gain of approximately 15.8 dB around 4 GHz and gradually rolls till 83 GHz with is its 3-dB bandwidth point. This means that the DPA has a bandwidth of 82 GHz, which is well above our aim of 70 GHz bandwidth. It has an average gain of 13.75 dB with gain bandwidth product(GBP) of 1126 GHz.

The output power and power added efficiency(PAE) are analyzed across 10 to 70 GHz, with results summarized in Fig. 3.15. The OP1dB ranges between the lowest at 70 GHz with 11.5 dBm to the highest 14.6 dBm at 30 GHz, while the P_{sat} reaches up to 18.5 dBm. This correlates with the Psat and OP1dB. PAE at OP1dB ranges from 5.2% to 8.6%, while the peak PAE achieves 20% at 10 GHz and degrades at higher frequencies.

The NF of the amplifier, shown in Fig. 3.17, starts around 4.6 dB at 1 GHz and decreases slightly across the frequency band, lowest 3.9 dB at 25 GHz and increases till the 82 GHz to 9 dB NF. This NF shows inconsistent noise performance despite the stable gain. This makes the design unusable in noise-sensitive applications like the first components of the receiver end. The group delay response in Fig. 3.16 shows a relatively flat and well-controlled behavior as design considerations with an average 30 to 35 ps delay, making it usable across the wideband operations.

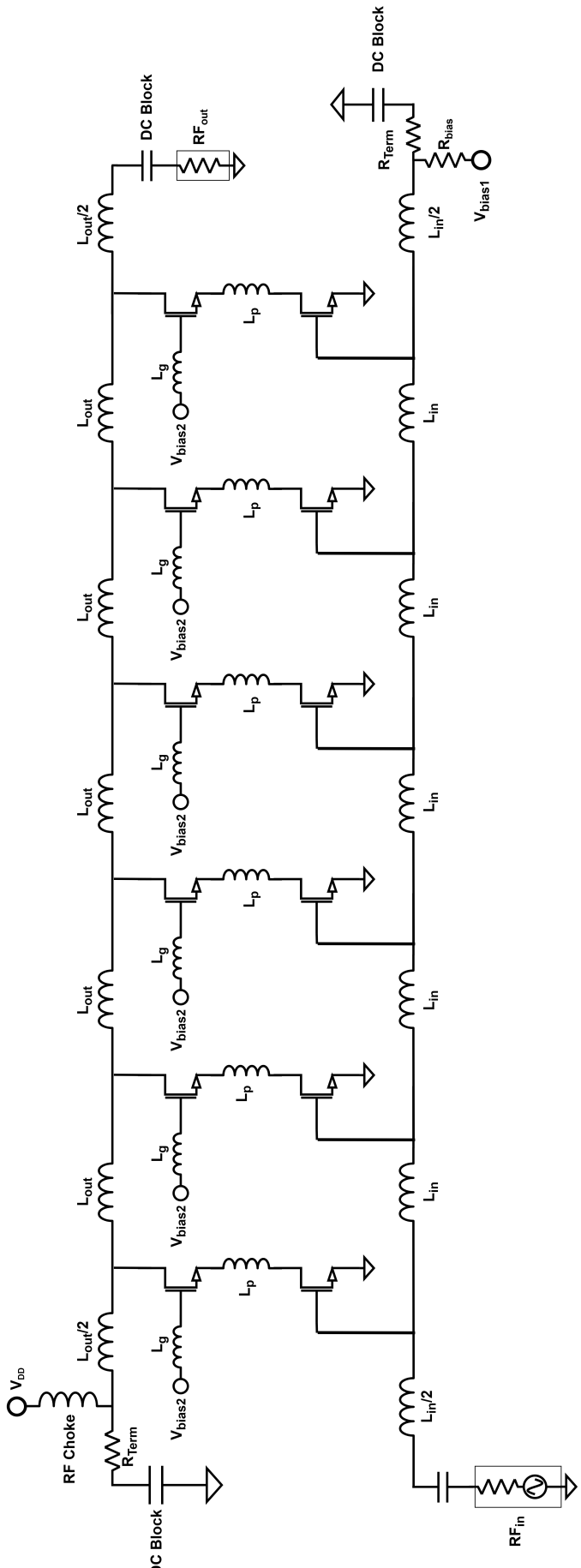

Figure 3.12 Schematic of the six-stage DPA.

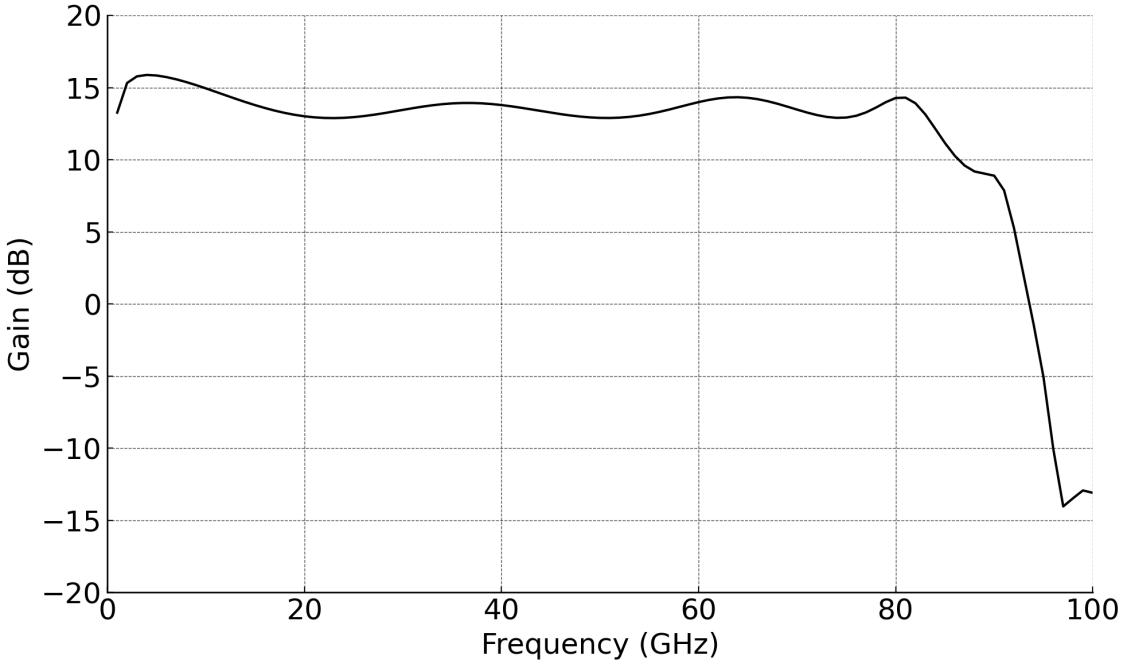

Figure 3.13 Gain of the six-stage DPA across frequency.

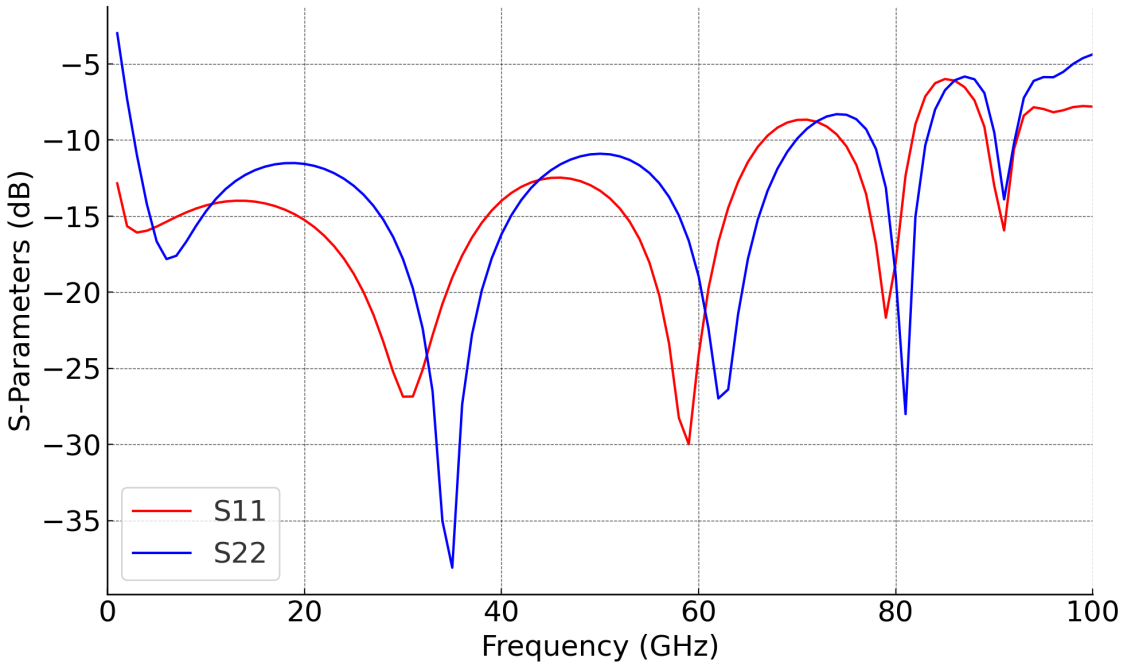

Figure 3.14 Input and output matching of the six-stage DPA across frequency.

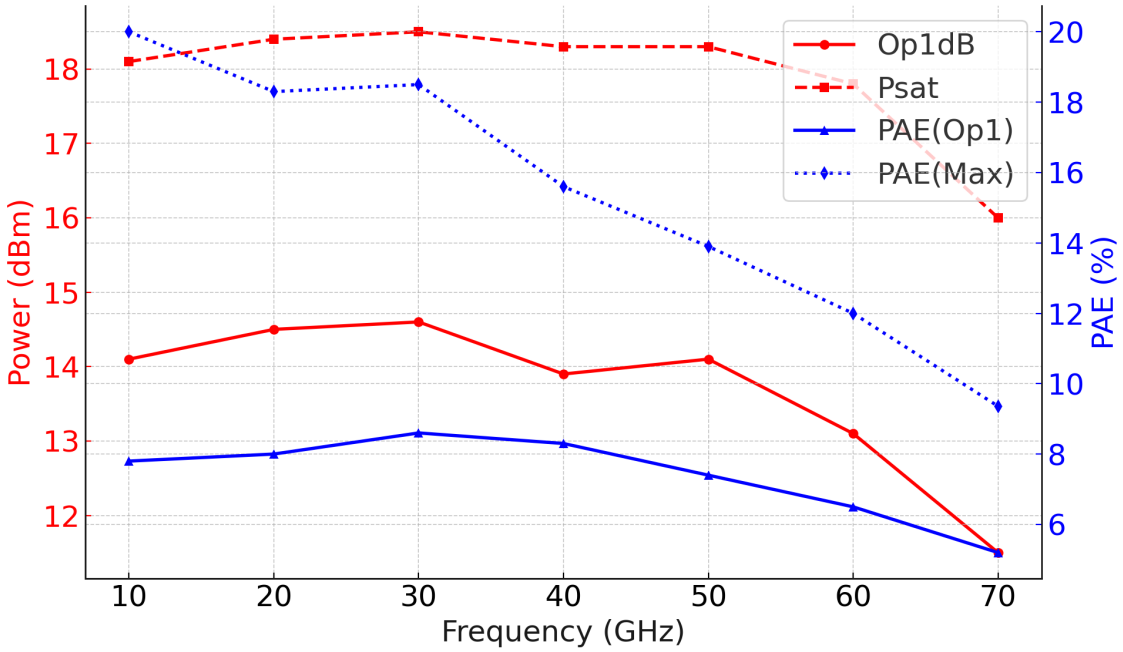

Figure 3.15 $OP_{1\text{dB}}$, P_{sat}, PAE at $OP_{1\text{dB}}$, and maximum PAE of the six-stage DPA across frequency.

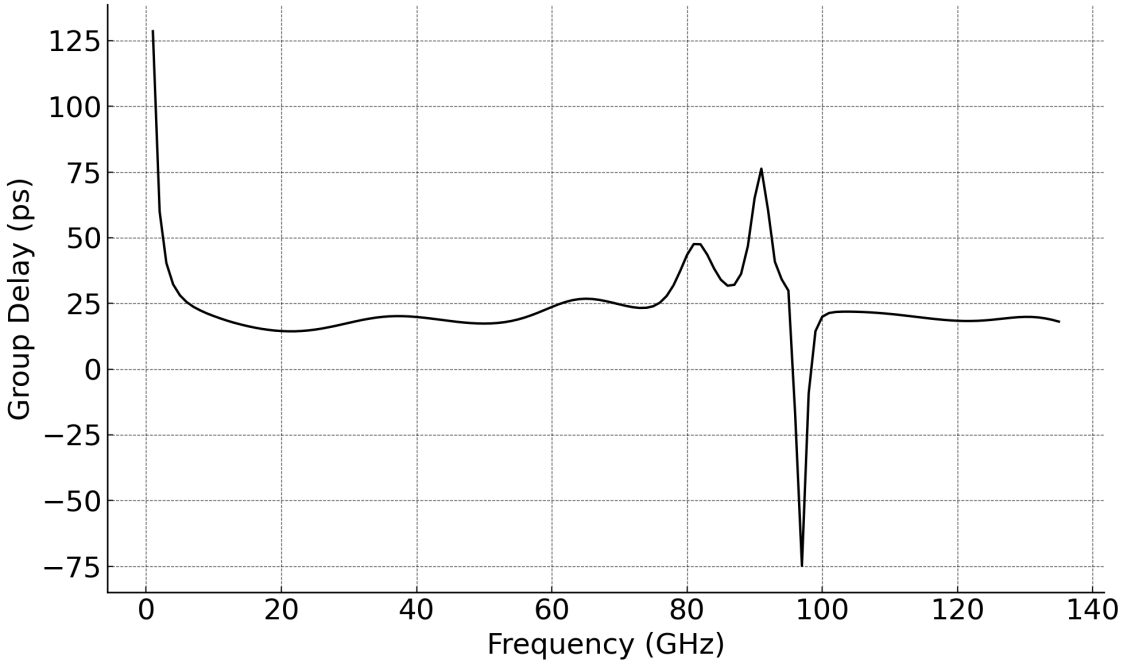

Figure 3.16 Delay of the six-stage DPA across frequency.

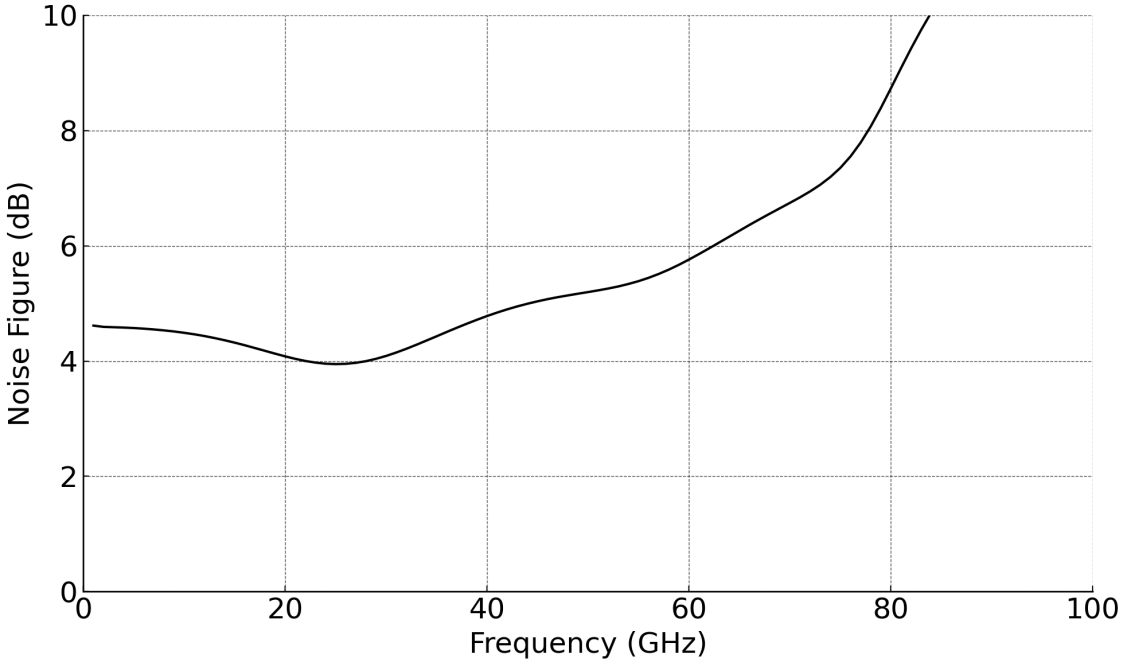

Figure 3.17 NF of the six-stage DPA across frequency.

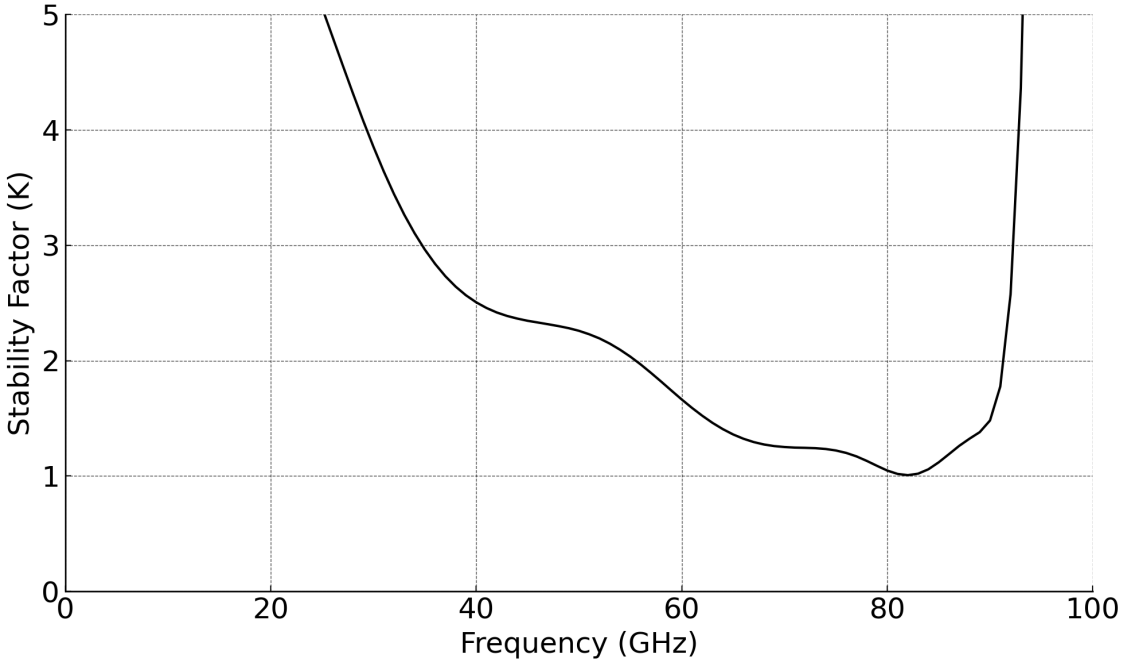

Figure 3.18 Stability factor of the six-stage DPA across frequency.

As one of the important parameters due to the inherently low stability of DA, it is essential to check the stability factor. The stability plot is shown in Fig. 3.18. The minimum value in the plot is 1.007 at 80 GHz. However, since the stability factor remains above 1 across the entire frequency range, the design is considered unconditionally stable.

Inductors typically occupy 50% of the ATL-DA area. Our set of 0.049 mm^2 inductor implies a total layout of 0.1 to 0.15 mm^2.

The area of the design can also be estimated. According to the literature, inductor-based ATL DA typically use around 50% of the chip area to inductors, while transistors occupy the remaining area and interconnects. In our design, the total inductor area is approximately 0.049 (mm^2), which suggests that the total layout area is expected to fall within the range of 0.1 (mm^2) to 0.15 (mm^2) if it is fabricated.

3.5 Comparison to Literature

A comprehensive comparison of the proposed design with prior state-of-the-art DPAs and DAs is presented in Table 3.4. The literature includes various technologies such as CMOS, RFSOI, SiGe BiCMOS, and InP. Although InP and SiGe technologies, such as those in Fang et al. (2016); Kazan & Rebeiz (2021); Nguyen et al. (2023), offer high gain and broad bandwidth, they typically require larger chip areas. For RFSOI-based works like El-Aassar & Rebeiz (2019b,2,2) demonstrate wide bandwidths up to and beyond 100 GHz, with exceptionally high peak OP1dB values around 21 dBm, while also achieving smaller area consumption compared to SiGe and InP designs. However, it is important to note that SOI-based designs benefit from higher supply voltages, which helps to achieve such high output power. In contrast, supply voltage is limited to around 3.3 V in SiGe and up to 2.4 V in bulk CMOS processes.

CMOS-based DPAs, especially those implemented in 65-nm nodes Hsu et al. (2020); Tarar et al. (2024), often face trade-offs between high gain and high output power. For example, the work in Hsu et al. (2020) achieves an impressive 30 dB gain and 2435 GHz GBP, but requires 254 mW of power dissipation and occupies an area greater than 0.6 mm^2. Also, the paper reveals that the bandwidth is not the range of 3 dB to maximum, but this time, 5 dB to maximum gain. In contrast, our proposed design achieves a flat gain of 13.75 dB across an 82 GHz bandwidth, resulting in a GBP of 1126 GHz. The OP1dB performance reaches 14.5 dBm, 13.9 dBm, and 13.1 dBm at 20, 40, and 60 GHz, respectively. These results are competitive with, or even superior to, all bulk CMOS implementations found in the literature, and in some cases surpass designs in other technologies that benefit from higher supply voltages.

The area efficiency of the suggested DPA is one of its main benefits. It provides

Table 3.4 Comparison of State-of-the-Art DPA

Ref.	**Tech.**	**BW (GHz)**	**Pdc (mW)**	**Gain (dB)**	**GBP**	**OP1dB (dBm)**	**PAE (%)**	**Area (mm^2)**	**V_{DD} (V)**
El-Aassar & Rebeiz (2019b)	45-nm RFSOI	DC–108	890 / 660	23	1525	19.5 (20)	9.1 (25), 12.5 (50), 5.9 (70)	0.31 (ext. bias-T)	5 / 6.6
El-Aassar & Rebeiz (2019a)	45-nm CMOS SOI	100	–	–	640	19.0 (20), 18.5 (40), 17.5 (60)	12 (20), 10.7 (40), 8.4 (60)	0.33 (no ext. bias-T)	5
Fang et al. (2016)	SiGe BiCMOS 90nm	14–105	–	12	362	14.9 (peak)	9.7 (peak)	1.51 (ext. bias-T)	2.7–4
Tsai et al. (2005)	45-nm RFSOI	10–82	–	13	361	13	17	0.8 (ext. bias-T)	–
El-Aassar & Rebeiz (2020a)	45-nm RFSOI	DC–120	–	16	757	21.3 (20), 20 (50)	13.8 (20), 10 (40), 10.2 (60)	0.51 (ext. bias-T)	4.8
Fang & Buckwalter (2019)	45-nm RFSOI	11–83	–	12.6	499	22.4	–	0.8 (ext. bias-T)	1.5–2.4
Hsu, Wang & Wang (2020)	65-nm CMOS	14–91	254	30	2435	7.4 (40–67)	2	0.62 (no ext. bias-T)	2.4
Tarar et al. (2024)	65-nm CMOS	3–53	345	>9.3	146	12	–	1.33 (no ext. bias-T)	2.2
Kazan & Rebeiz (2021)	90-nm SiGe HBT	120	–	27	2577	13.1 (peak)	7 (20), 3 (90)	1.24 (no ext. bias-T)	1.8–2.8
Nguyen et al. (2023)	InP HBT	7–115	–	16	–	15 (75)	6.8 (75)	1.75 (ext. bias-T)	1.15–5.8
El-Aassar & Rebeiz (2020b)	45-nm RFSOI	2.5–104	820	33	4533	22.5	10.4 (20), 7.7 (40), 11.6 (70)	0.58 (semi-ext. bias-T)	4.8, 2
Our Work	65-nm CMOS	82	216	13.75	1126	14.5 (20), 13.9 (40), 13.1 (60)	8 (20), 8.3 (49), 6.5 (60)	0.1–0.15 (ext. bias-T)	2.4

a small and completely integrable solution with an estimated total layout area of 0.10-0.15 mm^2. All things considered, the amplifier offers a great trade-off between gain, bandwidth, OP1dB, efficiency, and area, making it a solid candidates for future ultra-wideband systems.

4. DISTRIBUTED LOW NOISE AMPLIFIER

Distributed low noise amplifiers(DLNAs) are used when both high bandwidth and linear NF are needed at the same time. DA's structure naturally fits wideband systems. In this work, a DLNA is designed as the first stage of a receiver or transmitter. The focus is on achieving wideband gain and low stable NF, with a compact layout using area reduction methods. The design steps, performance targets, and key trade-offs are presented in this chapter.

4.1 Design Considerations of the DLNA

As discussed earlier, DAs are widely used in ultra-wideband systems. However, most of them are not optimized for low and flat NF across a wide frequency range, which limits their use in low-noise applications. In the literature, DLNAs have been implemented using various technologies, including bulk CMOS (Feng et al., 2017; Hsu et al., 2020; Wu et al., 2022) and some with LP configurations (Jahanian & Heydari, 2012), SOI CMOS (Fang & Buckwalter, 2019), GaN HEMT (Thome, Brückner & Quay, 2024), and SiGe BiCMOS (Baeyens, Mansha & Rücker, 2022; Heydari, 2007; Moez & Elmasry, 2008).

In this design, the DLNA is intended to serve as the first stage in the signal chain, enabling low and stable noise across the entire system. To meet this goal, the transistors are carefully biased and sized to minimize the NF while preserving gain. Staging is also optimized to balance noise, gain, and bandwidth.

Similar to the power amplifier discussed earlier, area reduction remains a key objective in this work. For this reason, shape-optimized inductors are used to minimize layout size. A lower quality factor is accepted as a trade-off to achieve a more compact footprint.

Recent designs based on bulk CMOS, SOI CMOS, GaN HEMT, and SiGe technologies typically report NF around 6 dB and average gain of approximately 15 dB. While some of these demonstrate low NF across wide bandwidths, they generally operate below 20 GHz. In contrast, the DLNA presented in this thesis targets a much wider frequency range, exceeding 70 GHz, while aiming to improve both noise and gain performance, all within a compact layout.

4.2 Theoretical Calculations

This section presents the theoretical foundations that will impact the design flow and performance metrics of the DLNA. The two main topics covered are NF modeling, which defines the minimum achievable noise performance of the system, and total transconductance (G_m) optimization using peaking techniques that were discussed previously, which extends bandwidth while maintaining gain.

4.2.1 NF Calculation

As previously discussed (Aitchison, 1985), the noise performance of DAs was first analyzed by Aitchison. He proposed an expression for the total NF in MESFET-based designs. His model assumes lossless lines, perfect matching, and does not include flicker noise or correlations between gate and channel noise. These simplifications make it less usable for CMOS based implementations.

Heydari (2007) addressed these limitations by developing a more complete model for CMOS technologies. His formulation includes all key noise sources like thermal noise, gate-induced noise with proper correlation to the channel, flicker noise, and resistive noise from terminations. In the paper, he proposed two equations are given in his work one for general applications that includes flicker noise and the other for high-frequency use. Since this design targets broadband operation beyond 1 GHz, the high-frequency expression is used and can be seen in Eq.4.1

$$F_{\text{tot}} = 1 + F_{\text{flicker}} + \frac{1}{(N g_m Z_T)^2} + \left(\frac{\sin N\beta}{N \sin\beta}\right)^2$$

$$+\frac{\gamma}{N g_m Z_T}\left(1 + \frac{2N^2+1}{3}\left|\frac{\kappa_c}{c}\right|^2\left[(\omega\tau_{GS})^2 + 2N\kappa_c(\omega\tau_{GS})\right]\right) \quad (Heydari,\ 2007) \tag{4.1}$$

In this equation, the total NF depends on the number of stages N, per-stage transconductance g_m, termination impedance Z_T, channel noise coefficient γ, gate-source delay τ_{GS}, and the correlation coefficient κ_c. The sinusoidal term in there relates the distributed structure's reverse noise propagation, while the $\omega\tau_{GS}$ term shows the impact of timing at high frequencies. Flicker noise becomes negligible above 100 MHz, so it is excluded here.

This model is more aligned with real CMOS behavior and is backed by both simulations and measurements in Heydari's work. It offers a reliable foundation for low-noise DA design across wide frequency bands.

To validate Eq.4.1, a Python simulation was run. Fig.4.1 shows how the NF changes with different stage numbers across frequency. Even though the parameters used in the simulation are not exactly taken from a 65-nm CMOS process, the results still give a clear idea that after a certain number of stages, the noise starts to increase, especially at higher frequencies. For instance, around 70 GHz, using more than five stages causes the NF to rise noticeably, which is not acceptable for low-noise design. So, the number of stages should be chosen carefully based on this kind of behavior.

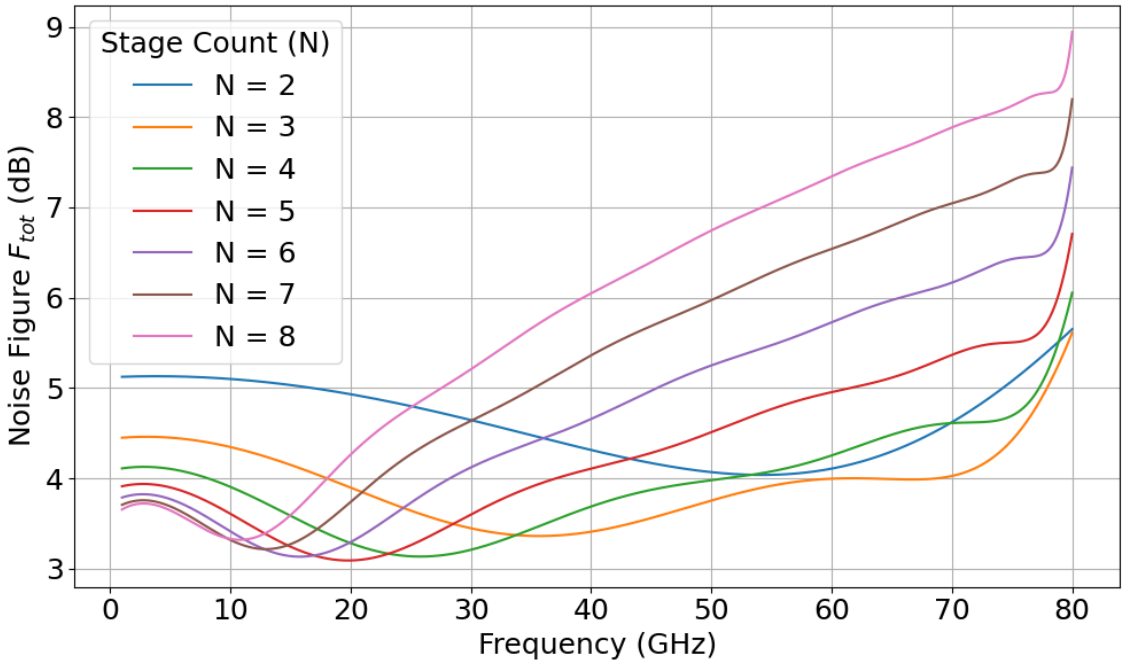

Figure 4.1 Noise figure of different numbers of stages with Eq.4.1.

4.2.2 Total Transconductance Peaking

As previously discussed, DAs main disadvantage is loss at higher frequencies due to the reduction in the transistor's effective transconductance. This reduction in g_m not only limits the achievable gain but also negatively impacts the NF.

In a DLNA, maintaining high G_m at elevated frequencies is crucial for both gain increase and NF minimization. This motivates the adoption of peaking techniques to boost G_m at high frequencies.

As discussed in the previous DPA section, the fully shunt-peaked cascode structure yields the highest overall transconductance among the examined topologies, while the regular DA exhibits the lowest. Accordingly, Fig. 4.2 compares the theoretical G_m expressions Eq. 4.2 and Eq. 4.3 in a 3-stage DA implementation. The results confirm that the enhanced G_m achieved through shunt peaking significantly reducese NF and show the inverse relationship between G_m and NF.

The gain performance of these topologies has already been analyzed in the DPA section and will not be repeated here, but the gain is also increased with peaking methods.

$$G_{m,\mathrm{reg}}(s) = \frac{g_m^2 + g_m s C_{gd1}}{g_m + s C_{gd1} + s C_{gs2}} \tag{4.2}$$

$$G_{m,\mathrm{full}}(s) = \frac{g_m \left(\frac{s^2 L_g C_{gs2}}{1 + s^2 L_g (C_{gd2} + C_{gs2})} - 1 \right) (g_m + s C_{gd1}) s L_p}{1 + \left(C_{gd1} - \frac{1}{s L_p} \right) \left[1 + \left(\frac{s^2 L_g C_{gs2}}{1 + s^2 L_g (C_{gd2} + C_{gs2})} - 1 \right) s L_p (g_m + s C_{gs2}) \right] s L_p} \tag{4.3}$$

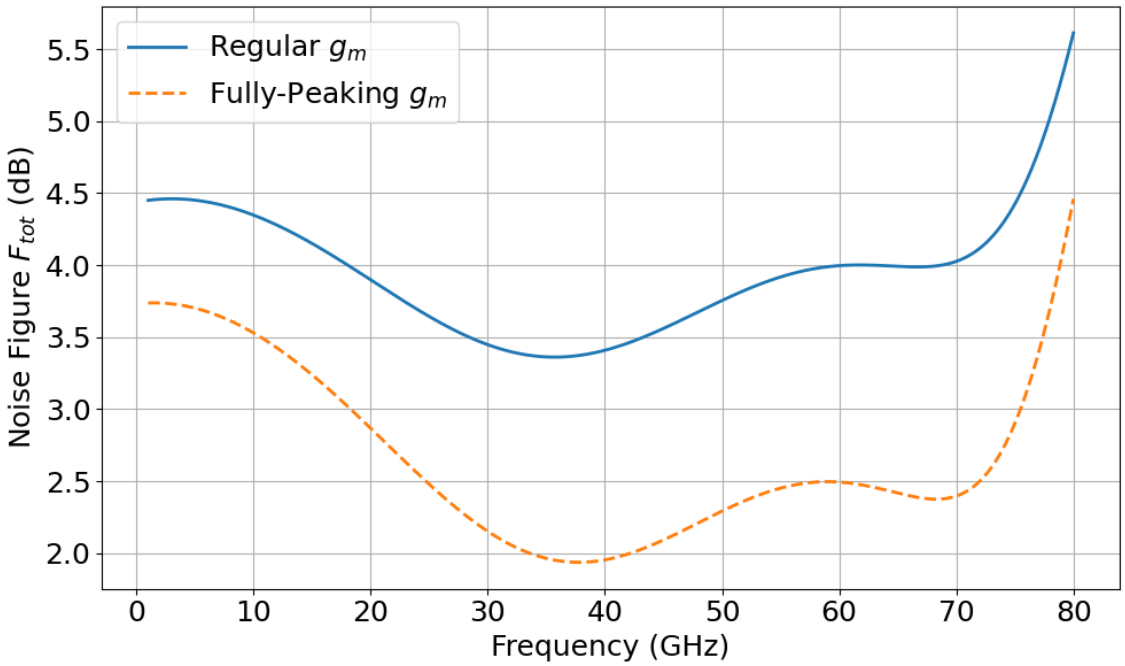

Figure 4.2 Noise figure of a 3-stage DA comparing regular and fully shunt-peaked G_m structures.

4.3 Methodology of Proposed Design or Proposed Design Procedures

This section presents the DLNA design procedures, which are optimal biasing for low noise, optimization of the number of stages in the DA, and low-quality factor inductor design to reduce the area.

4.3.1 Optimal Biasing

One of the most important things in low-noise amplifiers is to choose the optimal biasing for the transistors. They are one of the major sources of noise, and unlike other noise sources, they can be controlled by biasing.

In Fig. 4.3, the effect of cascode amplifiers can be seen on the bias of the common source stage. The top transistor gets around 1.2 V more than the bias we give to the bottom one. From the figure, we can say that after 0.6 V, the transistor starts to operate in a region where noise increases slowly and linearly. Around 0.64 V and 0.65 V, the NF is the lowest, about 0.868 dB. But still, any value between 0.6 and 0.7 V can be chosen since the change in noise is not that much.

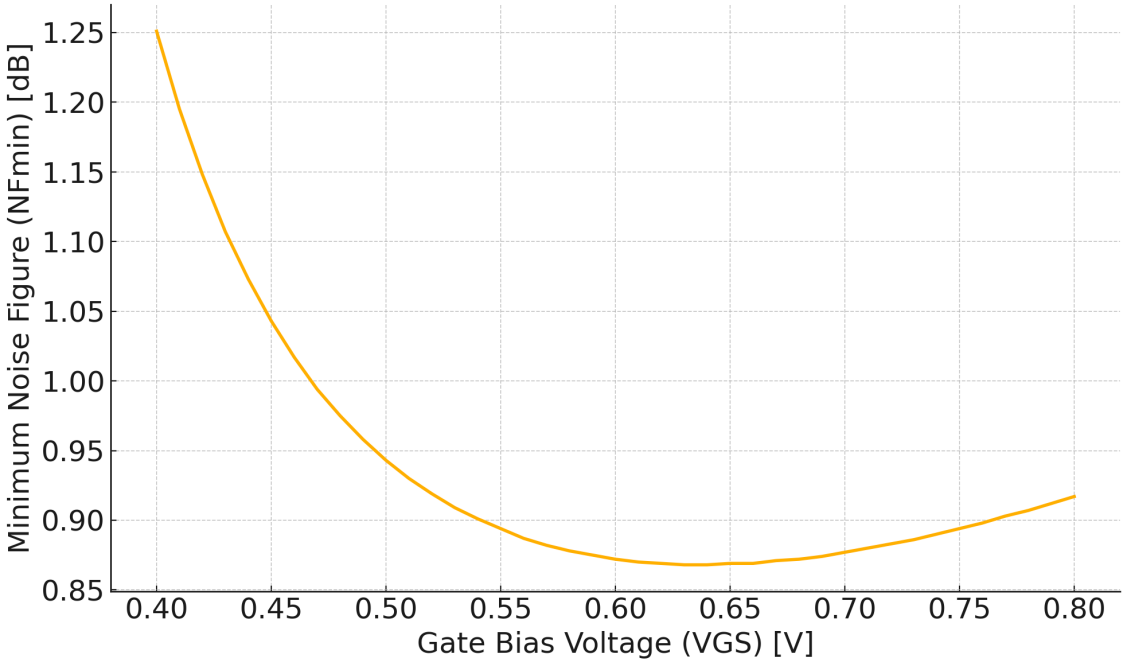

Figure 4.3 NF_{min} vsV_{GS} of a cascode.

4.3.2 Optimal Transistor Sizing

In the DLNA design, optimal transistor sizing plays an important role. Distributed amplifiers already provide a relatively good noise match by structure, but with proper sizing, it can be improved further. Since the lowest noise is achieved through noise matching, size becomes a critical factor.

In this work, the transistor sizes were selected smaller than those in the DPA design.

The main reason is that increasing transistor size tends to increase the noise figure at high frequencies, which is not acceptable for a DLNA targeting 6 dB NF at 70 GHz. On top of that, the design aims to reach 14 dB gain over 70 GHz bandwidth, so parasitic capacitance must be kept minimal. Therefore, smaller transistors were chosen to have wideband performance without sacrificing gain. This balance between gain, bandwidth, and noise affected the sizing choices in the design.

4.3.3 Stage Number Optimization

The selection of the stage number is one of the key controlling factors of DA. In this selection for DLNA, design must be considered in two areas, which are gain and NF. Different than DPA, stage comparison designs are mainly optimized for linear NF rather than high gain.

In Fig. 4.4, gain vs frequency is shown for stage numbers between 2 and 7. As expected, the gain increases with more stages, especially up to 6 stages. However, after 6 stages, the increase in gain stops, but it starts to increase bandwidth.

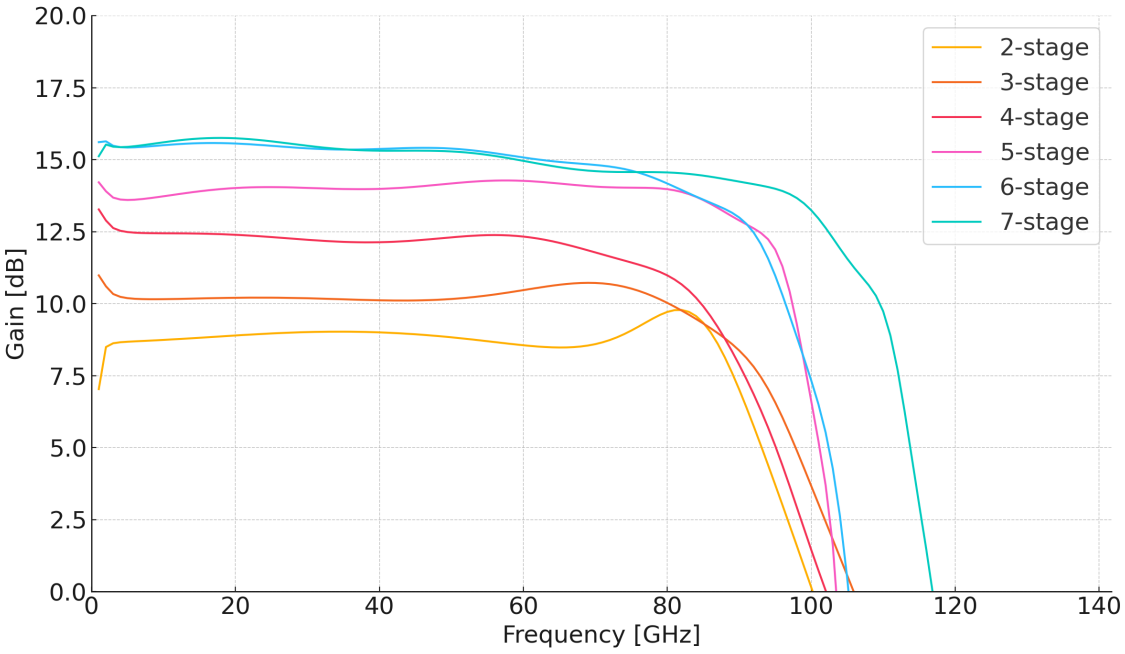

Figure 4.4 Gain vs frequency of stages between 2 to 7.

On the other hand, Fig. 4.5 shows how the NF changes with the number of stages. It decreases as we add more stages, but again, after 6 stages, the difference becomes

almost negligible. However, the 7-staged one has a slightly lower NF with 5.3 dB than the 6-stage; therefore, the 7-staged one will be used to design DLNA.

Based on these results, using 7 stages gives a good trade-off between gain and noise.

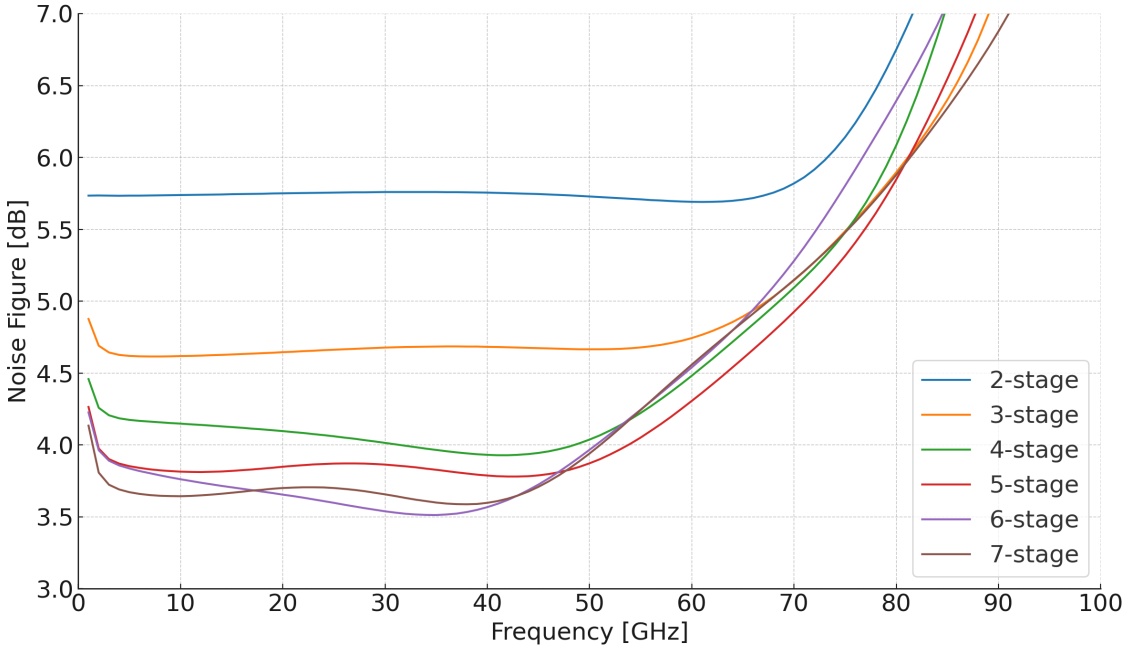

Figure 4.5 NF vs frequency of stages between 2 and 7.

4.3.4 Low-Quality Factor Inductor-Based Area Reduction Technique

In our low-quality factor inductor-based design, before going into layout, we first decided how much lower Q we could use without losing performance. This step was done at the schematic level. In the end, the values used are shown in Table 4.1. The average Q is around 8, which is lower than the one used in the previous design.

Table 4.1 Schematic inductor values of DLNA

	Lin	**Lout**	**Lg**	**Lp**
Inductance (pH)	114	142	60	60
Quality Factor (Q)	8	8	8	8

After that, inductors were designed in Ansys HFSS to extract their S-parameters and use them in ADS for post-layout simulation. As shown in Table 4.2, the layout values changed a bit due to parasitics, but the Q stayed below 9, and the area was still kept compact.

Table 4.2 Post-layout inductor values and area consumption of DLNA

	Lin	**Lout**	**Lg**	**Lp**
Inductance (pH)	116	168	61	65
Quality Factor (Q)	8.9	8.2	8.4	8.5
Area (μm^2)	1640.25	2025	1156.25	1183.35

The inductors were designed as 2-turn square spirals, as shown in Fig. 4.6. This structure was preferred because it gives enough inductance in a small area. Compared to the previous design with a higher Q, this approach significantly reduced the total layout area while maintaining circuit functionality.

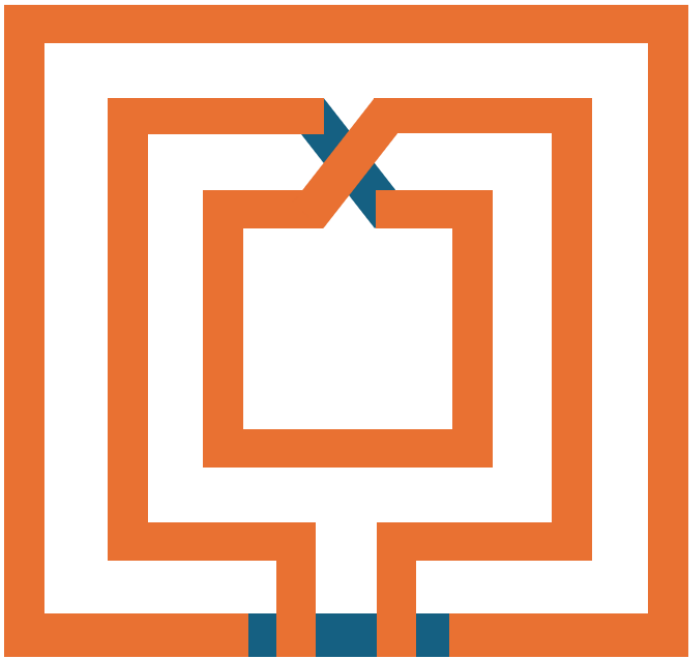

Figure 4.6 2-turn square inductor layout.

In conclusion, the final layout includes nine L_{in}, nine L_{out}, seven L_{p}, and seven L_{g} inductors. Among these, two of the L_{in} and two of the L_{out} inductors are designed with two-thirds of the original inductance value, as only half of the inductance is required in those positions. As a result, the total inductor area sums up to 49,364 (μm^2), which corresponds to 0.0493 (mm^2).

4.4 Simulation Results

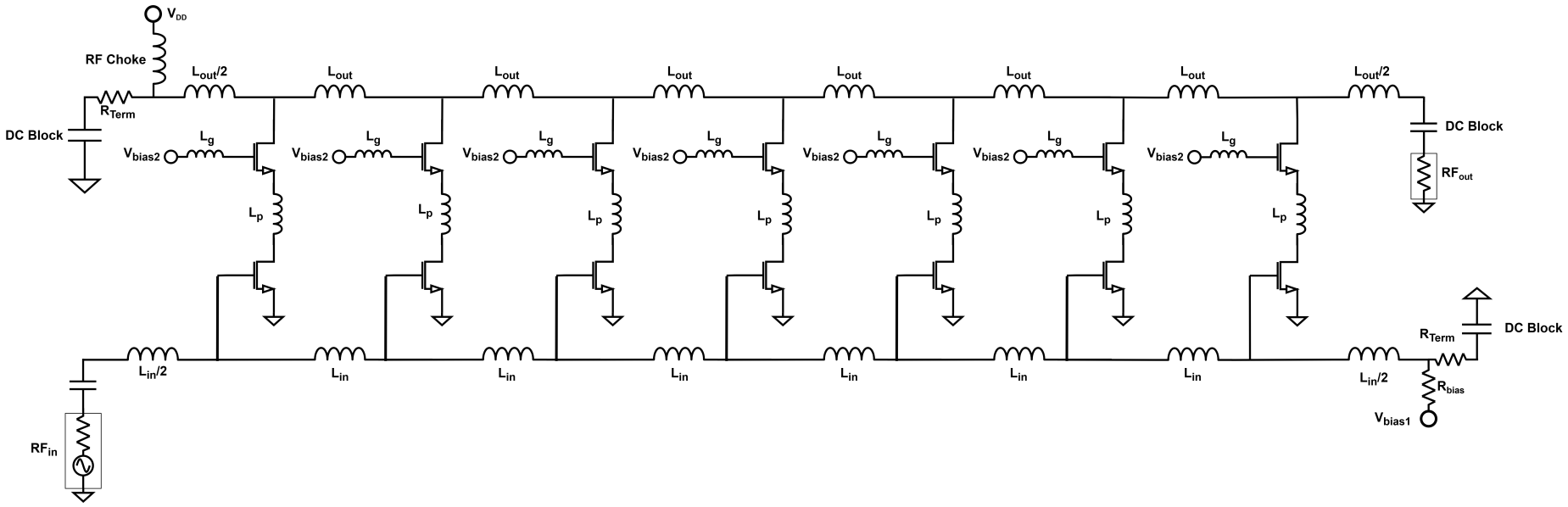

Figure 4.7 Schematic of the seven-stage DLNA.

This section presents schematic results 7-stage DLNA on Fig.4.7 that uses inductors based on HFSS designs' s-parameter extraction, focusing on key performance metrics across the 1 to 100 GHz frequency range. The parameters analyzed include ($S(1,1)$, $S(2,2)$), gain ($S(2,1)$), $OP_{1\text{dB}}$, NF, and the stability factor (K). All simulations were conducted in ADS using TSMC 65-nm technology.

The input and output matching can be seen in Fig.4.9. The $S(1,1)$ remains below -10 dB between 3 to 94 GHz, and the $S(2,2)$ remains below -10 dB between 2 to 93 GHz. The gain $S(2,1)$, depicted in Fig. 4.8, achieves a peak gain of approximately 15.4 dB around 1 GHz and gradually rolls off till 94 GHz which is its 3-dB bandwidth point. This means that the DLNA has a bandwidth of 93 GHz, which is well above our aim of 70 GHz bandwidth. It has an average gain of 13.5 dB with a gain bandwidth product(GBP) of 1271 GHz.

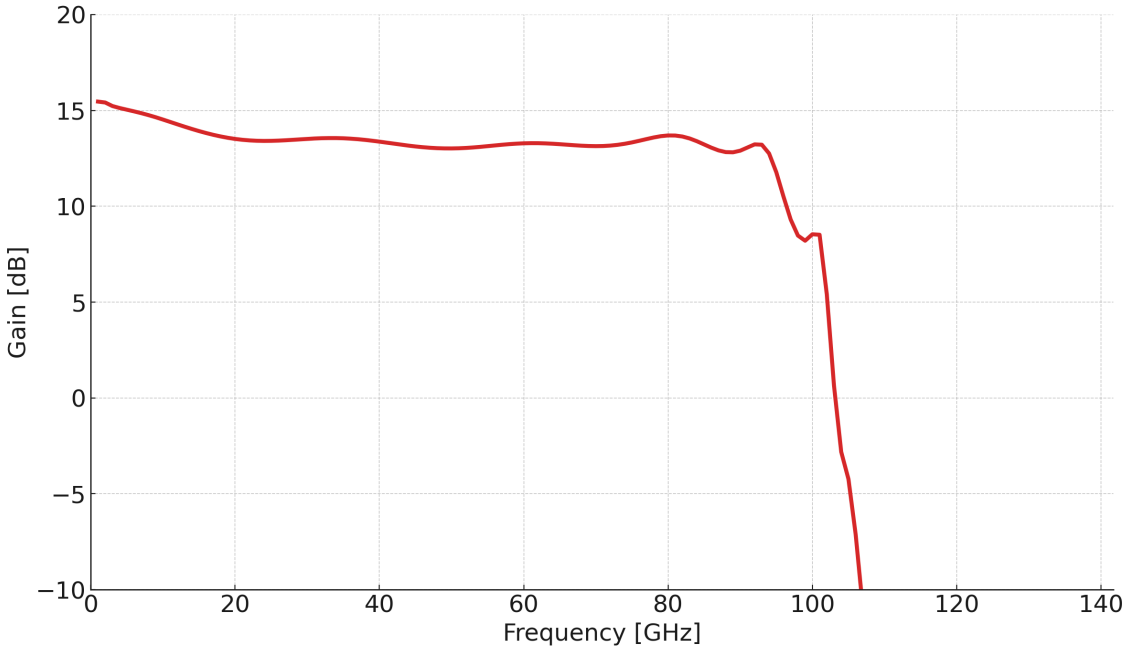

Figure 4.8 Gain of the seven-stage DLNA.

The output power is analyzed across 10 to 90 GHz, with results summarized in Fig. 4.10. The $OP_{1\text{dB}}$ ranges from the lowest at 90 GHz, with 7.3 dBm, to the highest at 10 GHz, with 13.2 dBm; higher frequencies have lower output power.

The NF of the DLNA is the most important parameter of all due to the importance of low noise in DLNAs, which is shown in Fig. 4.11, starting at 4.1 dB at 1 GHz and decreasing slightly across the frequency band, lowest 3.6 dB at 25 GHz and increases till the 90 GHz to 9 dB NF. However, the over-achieved bandwidth of this design is not showing our desired range of 70 GHz with a very low noise of 6 dB at 70 GHz. Although it is higher than the simulations due to the passive losses of the inductor

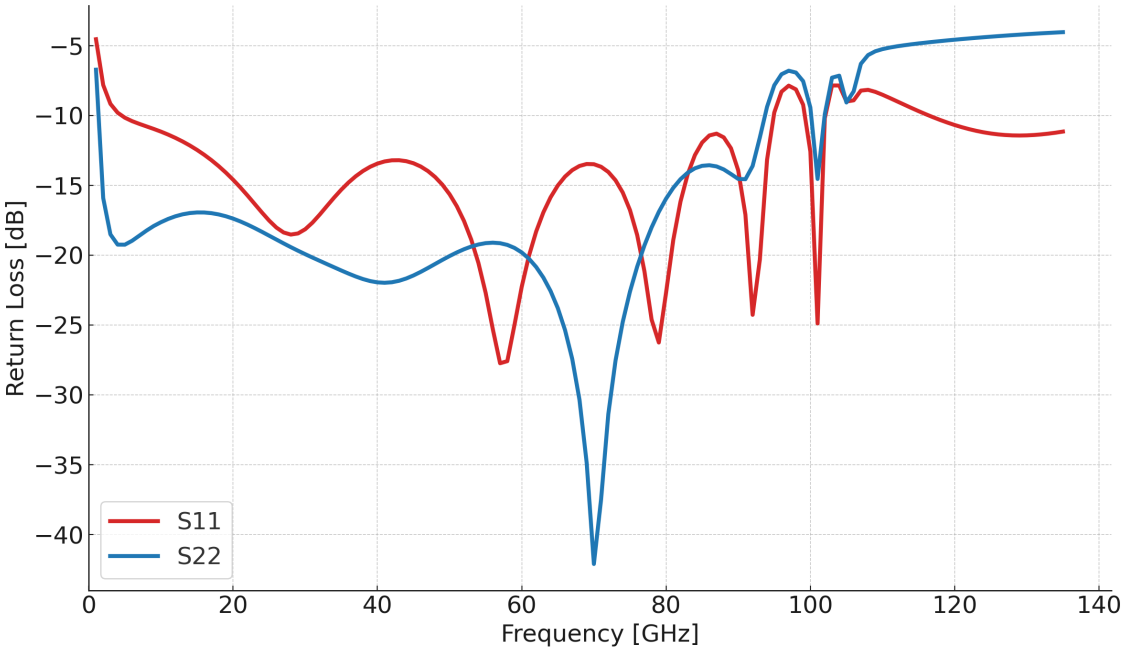

Figure 4.9 Input and output matching of the seven-stage DLNA.

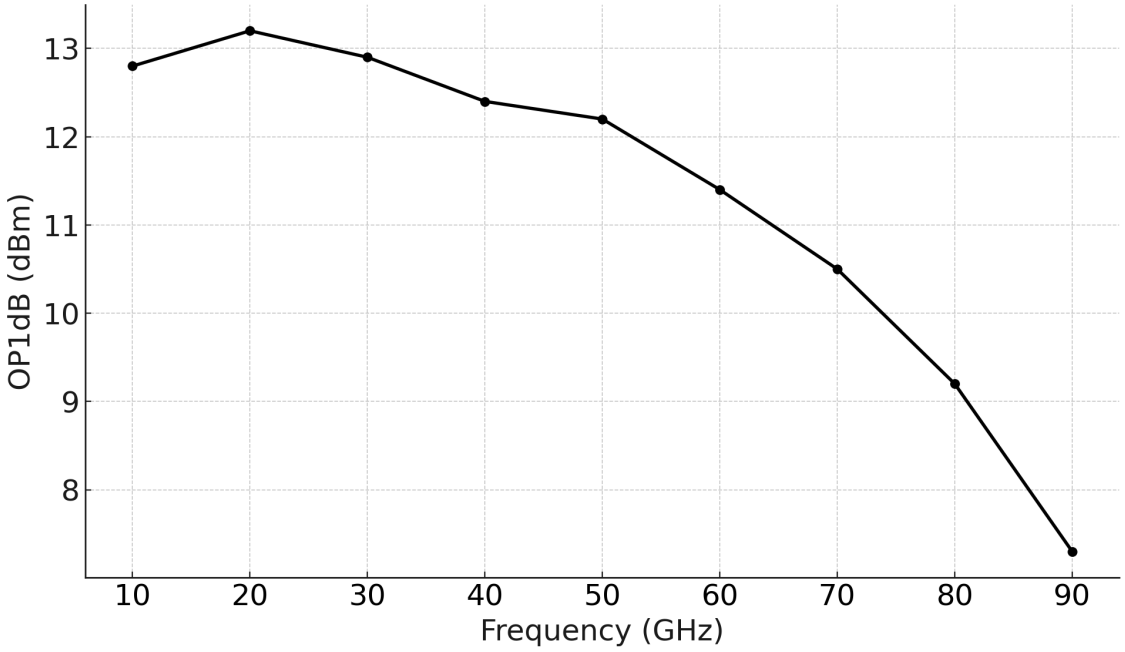

Figure 4.10 $OP_{1\mathrm{dB}}$ the seven-stage DLNA.

design is achieved a linear noise among the frequency range when looking at the literature, and a possible solution for ultrawide-band applications. Also, when the noise figure is compared to the minimum noise figure of the simulation, approximately 0.085dB difference occurs between 1-70 GHz, which proves that the design noise matching is done correctly, which is done by optimum sizing and optimum input termination resistance.

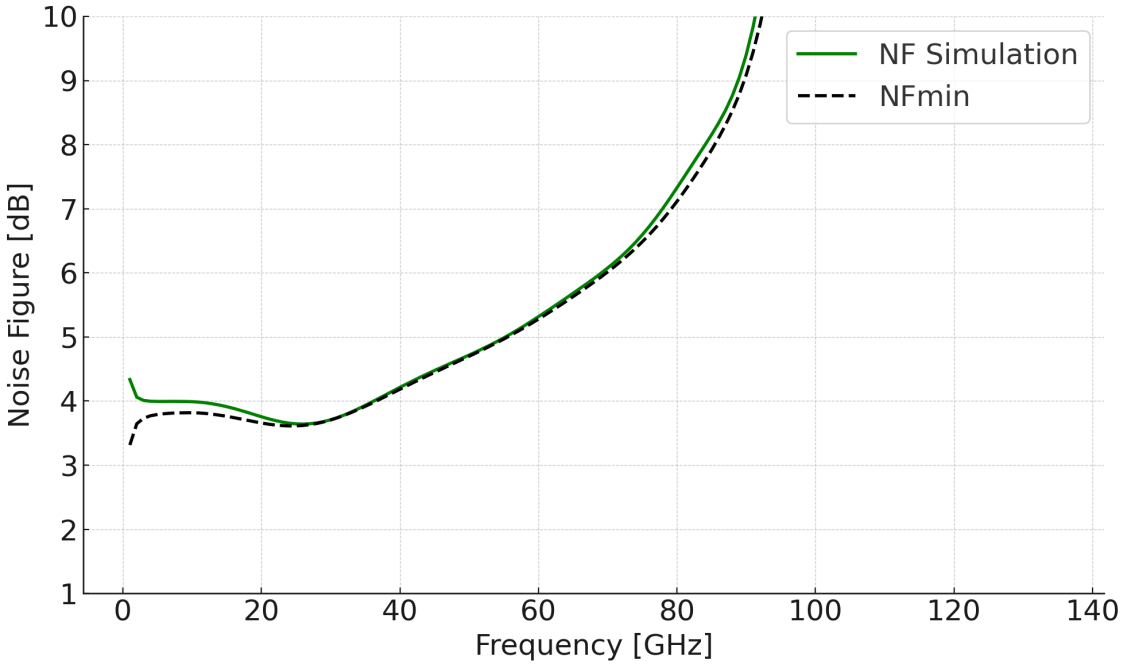

Figure 4.11 Noise figure of simulation and minimum noise figure of the seven-stage DLNA.

The group delay response in Fig. 4.12 shows a relatively flat and well-controlled behavior as design considerations with an average 20 ps delay, making it usable across the wideband operations.

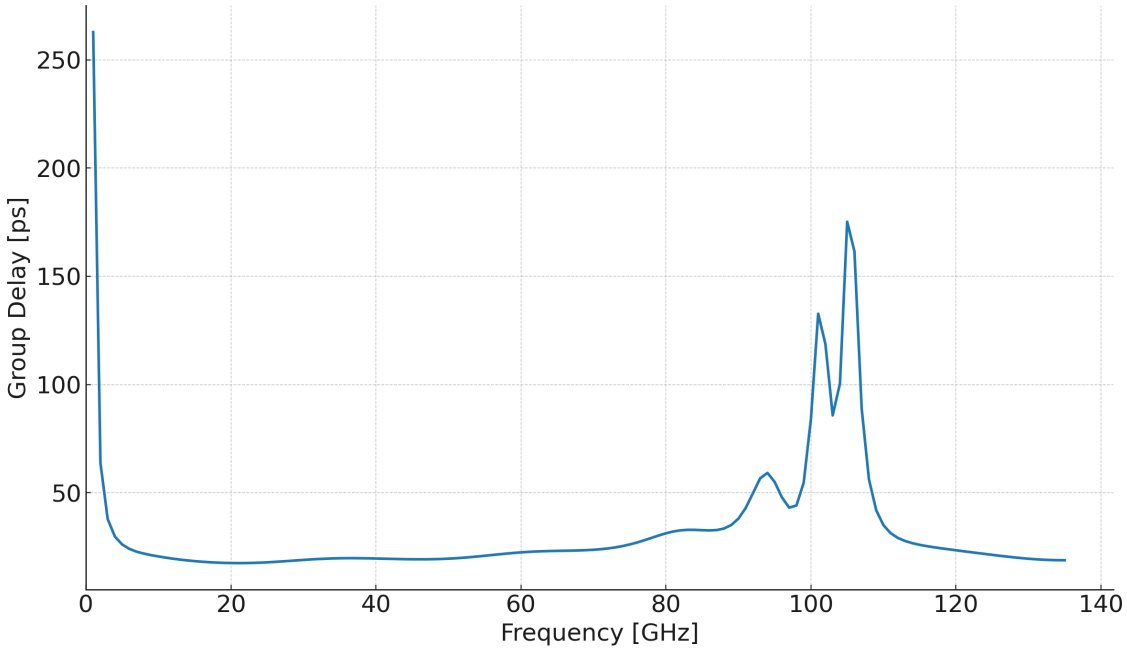

Figure 4.12 Delay of the seven-stage DLNA.

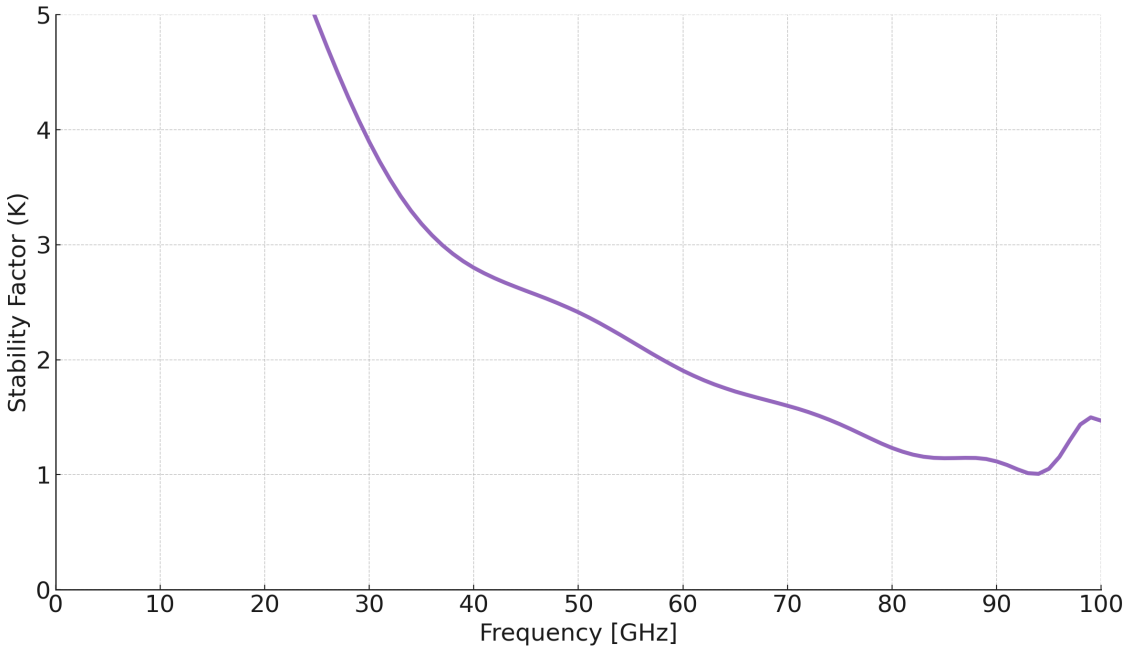

Figure 4.13 Stability factor of the seven-stage DLNA.

The stability plot is shown in Fig. 4.13. The minimum value in the plot is 1.007 at 94 GHz. However, since the stability factor remains above 1 across the entire frequency range, the design is considered unconditionally stable.

The area of the design can also be estimated. In the literature, inductor-based ATL DAs usually have around 50% of the chip area taken up by inductors, while the

rest is for transistors and interconnects. In our case, total inductor area is around 0.0494 (mm^2), so if this design is produced, the overall layout area is expected to fall somewhere between 0.0108 and 0.162 (mm^2), depending on how compact the final layout ends up.

4.5 Comparison to Literature

In Table 4.3, the proposed seven-stage DLNA is compared against various state-of-the-art DLNA designs, which are based on CMOS, RFSOI, SiGe BiCMOS, and GaN technologies. Other works may surpass in some metrics, but our design has superior or competitive performance across other key parameters. Compared to CMOS designs like Jahanian & Heydari (2012), which achieves 22 dB gain over 70 GHz, our design extends the bandwidth to 93 GHz with an average gain of 13.6 dB, resulting in a significantly higher gain-bandwidth product of 1271 GHz compared to 818 GHz. Moreover, Jahanian & Heydari (2012) occupies a larger area (0.93 mm^2) and depends on external biasing, whereas our estimated area is 0.108–0.162 mm^2, showing the area reduction.

RFSOI-based designs like Feng et al. (2017) achieve a low noise of 5.3 dB but offer a gain of 13 dB. Our DLNA maintains a lower NF of 3.6-6 dB over a wider band. Similarly, Wu et al. (2022) delivers 17.2 dB gain but suffers from poor OP_{1dB} of -1 dBm, lower GBP of 478 GHz, and external biasing, whereas our work achieves 7.3-13.1 dBm OP_{1dB} and higher GBP without such trade-offs. High-gain designs like Hsu et al. (2020) reach 30 dB and 2435 GHz GBP but at the cost of high power (254 mW) and larger NF (5.9-7.2 dB), whereas our design stays below 6 dB NF with better group delay behavior. SiGe BiCMOS designs 1 to 3 Baeyens et al. (2022), though benefiting from higher f_T, are costly and complex, while showing similar or worse NF, making our CMOS design more efficient and scalable.

GaN-based works like Thome et al. (2024) achieve 129 GHz bandwidth and high output power but compromise on gain (6.7 dB), area, and power (720 mW). In contrast, our DLNA provides a much more balanced performance profile suited for compact, low-noise wideband systems. In summary, the proposed design has a bandwidth of 1-94 GHz, a NF of 3.-6dB, reasonable OP_{1dB} up to 13.2 dBm, and a compact area, offering a strong candidate for ultra-wideband low-noise applications.

Table 4.3 Comparison of State-of-the-Art DLNA

Ref.	**Year**	**Tech.**	**Bandwidth (GHz)**	**Pdc (mW)**	**Gain (dB)**	**GBP**	OP_{1dB} **(dBm)**	**Area (mm^2)**	**V$_{DD}$ (V)**	**Group Delay (ps)**	**NF (dB)**
Jahanian & Heydari (2012)	2012	65-nm CMOS LP	70	19.5	22	818	10	0.93 (ext. bias-T)	1.3	50 range	6.9–7.9
Fang & Buckwalter (2019)	2018	45-nm RFSOI	10–82	–	13	361	13	0.8 (ext. bias-T)	–	<10	5.3
Wu et al. (2022)	2021	65-nm CMOS	2–68	120	17.2	478	−1 (20)	0.855 (ext. bias-T)	1.2	max 80	8–10
Feng et al. (2017)-1	2017	65-nm CMOS	62.5–92.5	27	18.5	–	2.5	0.24 (ext. bias-T)	1.8	–	5.5–7.9
Feng et al. (2017)-2	2017	65-nm CMOS	63.5–91	12	13.3	–	−2	0.24 (no ext. bias-T)	1.2	–	6.4–8.5
Hsu et al. (2020)	2020	65-nm CMOS	14–91	254	30	2435	7.4 (40–67)	0.62 (no ext. bias-T)	2.4	–	5.9–7.2
Baeyens et al. (2022)-1	2022	130-nm SiGe BiCMOS IHP	<170	350	19	1515	–	0.14 (core only ext. bias-T)	3.3	–	(6–3.4–4) 4.7 @100
Baeyens et al. (2022)-2	2022	130-nm SiGe BiCMOS IHP	<170	250	16	1072	–	0.14 (core only ext. bias-T)	3.3	–	5.2 @100
Baeyens et al. (2022)-3	2022	130-nm SiGe BiCMOS IHP	<170	250	13.5	804	–	0.14 (core only ext. bias-T)	3.3	–	6.4 @100
Moez & Elmasry (2008)	2008	130-nm CMOS	3–9.4	30	12	80	5	0.825 (ext. bias-T)	–	–	1.8–4.7
Thome et al. (2024)	2024	GaN HEMT	2–129	720	6.7	850*	17.9–20.2	–	–	–	3.1–5.7
Our Work	2025	65-nm CMOS	93	168	15.4 peak, 13.6 avg	1271	13.2–7.3	0.108–0.162 (ext. bias-T)	2.4	20	3.6-6

5. CONCLUSION AND FUTURE WORK

5.1 Summary of the Work

This thesis has confirmed that distributed amplifier (DA) architectures can satisfy ultra-wideband (UWB) requirements and still fit within a possibility of a compact silicon footprint. Two schematic level designs were made in TSMC 65 nm bulk CMOS: a six-stage distributed power amplifier (DPA) that spans 1−82 GHz with an average gain of 13.8 dB and an OP_{1dB} range of 11.5–14.6 dBm, and a seven-stage distributed low-noise amplifier (DLNA) covering 1−94 GHz with 13.5 dB mean gain and a noise figure below 6 dB up to 70 GHz. Inductors we simulated using 65-nm CMOS substrate layers in HFSS. The inductive footprints of the DPA and DLNA are 0.049 mm^2 and 0.049 mm^2, respectively, yielding a combined active-plus-passive area below 0.1 to 0.15 mm^2 range for both amplifiers, by far the smallest reported for CMOS DAs operating beyond 70 GHz.

Compactness was achieved without using slow-wave transmission lines or stacked inductors. Instead, the design is based on fully shunt-peaked cascode gain cells combined with carefully modeled two-turn square inductors. These low-Q inductors contribute less than 0.5 dB gain loss. A clear and structured design flow starting with stage number optimization, followed by G_m peaking synthesis, bias tuning for lowest noise figure, full EM co-simulation of inductors and integrating them helped push the gain-bandwidth product to 1.13 THz for the DPA and 1.27 THz for the DLNA, both exceeding recent CMOS designs in terms of performance and area.

5.2 Future Work

In the short term, schematic-level designs of the DLNA and DPA, including EM-based inductors, should be moved to post-layout simulations. The simulation design might undergo some changes; therefore, certain parameters should be adjusted. The resulting designs should then be produced and packaged. Afterward, real-life tests should be performed. If complications occur during these tests, investigations should be carried out to determine what might be causing the issues.

In the longer term, if a problem is identified, it should be solved, and the design should be reproduced. If it works as expected, then a full system with a bandwidth of 70 GHz should be developed, including an integrated mixer and antenna to transmit the signal.

BIBLIOGRAPHY

Aitchison, C. (1985). The intrinsic noise figure of the mesfet distributed amplifier. *IEEE Transactions on Microwave Theory and Techniques*, *33*(6), 460–466.

Aitchison, C. & Mbabele, M. (2001). Third order intermodulation improvement in distributed amplifiers. In *2001 31st European Microwave Conference*, (pp. 1–4).

Arbabian, A. & Niknejad, A. M. (2009). Design of a cmos tapered cascaded multistage distributed amplifier. *IEEE Transactions on Microwave Theory and Techniques*, *57*(4), 938–947.

Ayasli, Y., Mozzi, R., Vorhaus, J., Reynolds, L., & Pucel, R. (1982). A monolithic gaas 1-13-ghz traveling-wave amplifier. *IEEE Transactions on Microwave Theory and Techniques*, *30*(7), 976–981.

Baeyens, Y., Mansha, M. W., & Rücker, H. (2022). A single-stage low-noise sige hbt distributed amplifier with 13 dbm output power and 20 db gain in d-band and over 170 ghz bandwidth. In *2022 17th European Microwave Integrated Circuits Conference (EuMIC)*, (pp. 52–55).

Bevilacqua, A. & Niknejad, A. (2004). An ultrawideband cmos low-noise amplifier for 3.1-10.6-ghz wireless receivers. *IEEE Journal of Solid-State Circuits*, *39*(12), 2259–2268.

Celik, U. & Reynaert, P. (2021). Robust, efficient distributed power amplifier achieving 96 gbit/s with 10 dbm average output power and 3.7 *IEEE Journal of Solid-State Circuits*, *56*(2), 382–391.

Chen, H.-H. & Hsu, Y.-W. (2022). Analytic design of on-chip spiral inductor with variable line width. *Electronics*, *11*(13).

Chen, J. & Liou, J. (2004). On-chip spiral inductors for rf applications: An overview. *JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE*, *4*.

El-Aassar, O. & Rebeiz, G. M. (2019a). A compact pmos stacked-soi distributed power amplifier with over 100-ghz bandwidth and up to 22-dbm saturated output power. *IEEE Solid-State Circuits Letters*, *2*(2), 9–12.

El-Aassar, O. & Rebeiz, G. M. (2019b). A dc-to-108-ghz cmos soi distributed power amplifier and modulator driver leveraging multi-drive complementary stacked cells. *IEEE Journal of Solid-State Circuits*, *54*(12), 3437–3451.

El-Aassar, O. & Rebeiz, G. M. (2020a). A 120-ghz bandwidth cmos distributed power amplifier with multi-drive intra-stack coupling. *IEEE Microwave and Wireless Components Letters*, *30*(8), 782–785.

El-Aassar, O. & Rebeiz, G. M. (2020b). A cascaded multi-drive stacked-soi distributed power amplifier with 23.5 dbm peak output power and over 4.5-thz gbw. *IEEE Transactions on Microwave Theory and Techniques*, *68*(7), 3111–3119.

El-Chaar, M., Vincent, L., Arnould, J.-D., de Souza, A. A. L., Bourdel, S., & Podevin, F. (2022). Accurate design method for millimeter wave distributed amplifier based on four-port chain (abcd) matrix model. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *69*(11), 4510–4523.

Fang, K. & Buckwalter, J. F. (2019). Efficient linear millimeter-wave distributed transceivers in cmos soi. *IEEE Transactions on Microwave Theory and Tech-*

niques, *67*(1), 295–307.

Fang, K., Levy, C. S., & Buckwalter, J. F. (2016). Supply-scaling for efficiency enhancement in distributed power amplifiers. *IEEE Journal of Solid-State Circuits*, *51*(9), 1994–2005.

Federal Communications Commission (2002). First Report and Order: Revision of Part 15 of the Commission's Rules Regarding Ultra-Wideband Transmission Systems. `https://www.fcc.gov/document/revision-part-15-commissions-rules-regarding-ultra-wideband-7`. ET Docket No. 98-153.

Feng, G., Boon, C. C., Meng, F., Yi, X., Yang, K., Li, C., & Luong, H. C. (2017). Pole-converging intrastage bandwidth extension technique for wideband amplifiers. *IEEE Journal of Solid-State Circuits*, *52*(3), 769–780.

Ginzton, E., Hewlett, W., Jasberg, J., & Noe, J. (1948). Distributed amplification. *Proceedings of the IRE*, *36*(8), 956–969.

Heydari, P. (2007). Design and analysis of a performance-optimized cmos uwb distributed lna. *IEEE Journal of Solid-State Circuits*, *42*(9), 1892–1905.

Heydari, P. & Safiallah, M. (2023). Evolution of broadband amplifier design: From single-stage to distributed topology. *IEEE Microwave Magazine*, *24*(9), 18–29.

Hsiao, C.-Y., Su, T.-Y., & Hsu, S. S. H. (2013). Cmos distributed amplifiers using gate–drain transformer feedback technique. *IEEE Transactions on Microwave Theory and Techniques*, *61*(8), 2901–2910.

Hsu, C.-M., Wang, Y., & Wang, H. (2020). A 14-91 ghz distributed amplifier in 65-nm cmos. In *2020 IEEE Asia-Pacific Microwave Conference (APMC)*, (pp. 1009–1011).

Hu, J., Ma, K., Xie, C., Liu, B., & Feng, Q. (2024). A high-gain distributed amplifier using gain cell with current-reused and gain-enhancement techniques. In *2024 IEEE MTT-S International Wireless Symposium (IWS)*, (pp. 1–3).

Hu, Z., Zhang, Q., & Ma, K. (2022). A 1–42 ghz gan distributed amplifier with adjustable gain by voltage-controlled switch. *IEEE Microwave and Wireless Components Letters*, *32*(4), 339–342.

Ismail, A. & Abidi, A. (2004). A 3-10-ghz low-noise amplifier with wideband lc-ladder matching network. *IEEE Journal of Solid-State Circuits*, *39*(12), 2269–2277.

Jahanian, A. & Heydari, P. (2012). A cmos distributed amplifier with distributed active input balun using gbw and linearity enhancing techniques. *IEEE Transactions on Microwave Theory and Techniques*, *60*(5), 1331–1341.

Kazan, O. & Rebeiz, G. M. (2021). A 10-130 ghz distributed power amplifier achieving 2.6 thz gbw with peak 13.1 dbm output p1db for ultra-wideband applications in 90nm sige hbt technology. In *2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, (pp. 1–4).

Kim, J. (2019). A wideband triple-stacked cmos distributed power amplifier using double inductive peaking. *IEEE Microwave and Wireless Components Letters*, *29*(12), 787–790.

Lee, D., Park, J., Choi, K.-S., Liu, Y., & Wang, H. (2023). A 137-ghz ultra-wide bandwidth high-linearity cmos distributed amplifier for high-speed communication. In *ESSCIRC 2023- IEEE 49th European Solid State Circuits Conference (ESSCIRC)*, (pp. 73–76).

Lee, J. & Cressler, J. (2005). A 3-10 ghz sige resistive feedback low noise amplifier for uwb applications. In *2005 IEEE Radio Frequency integrated Circuits (RFIC) Symposium - Digest of Papers*, (pp. 545–548).

Lee, T. H. (2003). *The Design of CMOS Radio-Frequency Integrated Circuits* (2 ed.). Cambridge University Press.

Moez, K. & Elmasry, M. I. (2008). A low-noise cmos distributed amplifier for ultra-wide-band applications. *IEEE Transactions on Circuits and Systems II: Express Briefs*, *55*(2), 126–130.

Nguyen, N. L. K., Cui, C., Nguyen, D. P., Stameroff, A. N., & Pham, A.-V. (2023). A 7–115-ghz distributed amplifier with 24-dbm output power using quadruple-stacked hbt in inp. *IEEE Microwave and Wireless Technology Letters*, *33*(6), 715–718.

Percival, W. S. (1937). Improvements in and relating to thermionic valve circuits.

Razavi, B. (2002). *Design of Integrated Circuits for Optical Communications* (1 ed.). USA: McGraw-Hill, Inc.

Tarar, M. M., Qayyum, S., Ali, A., & Negra, R. (2024). Loss-compensated cascaded multistage distributed power amplifier in 65nm cmos technology. *IEEE Access*, *12*, 98917–98927.

Testa, P. V., Belfiore, G., Paulo, R., Carta, C., & Ellinger, F. (2015). 170 ghz sige-bicmos loss-compensated distributed amplifier. *IEEE Journal of Solid-State Circuits*, *50*(10), 2228–2238.

Thome, F., Brückner, P., & Quay, R. (2024). A > 120-ghz bandwidth, >20-dbm pout, <6-db noise-figure distributed amplifier mmic in a gan-on-sic hemt technology. *IEEE Transactions on Microwave Theory and Techniques*, *72*(10), 5809–5817.

Tsai, M.-D., Wang, H., Kuan, J.-F., & Chang, C.-S. (2005). A 70ghz cascaded multi-stage distributed amplifier in 90nm cmos technology. In *ISSCC. 2005 IEEE International Digest of Technical Papers. Solid-State Circuits Conference, 2005.*, (pp. 402–606 Vol. 1).

Wu, Y.-M., Kao, Y.-H., & Chu, T.-S. (2022). A 68-ghz loss compensated distributed amplifier using frequency interleaved technique in 65-nm cmos technology. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *30*(1), 29–39.

Yang, L. & Giannakis, G. (2004). Ultra-wideband communications: an idea whose time has come. *IEEE Signal Processing Magazine*, *21*(6), 26–54.

Yağmurlu, S. A. & Tokgöz, K. K. (2024). Compact slow-wave transmission line design with high effective dielectric constant. In *2024 15th National Conference on Electrical and Electronics Engineering (ELECO)*, (pp. 1–5).

Yin, W.-Y., Xie, J.-Y., Kang, K., Shi, J., Mao, J.-F., & Sun, X.-W. (2008). Vertical topologies of miniature multispiral stacked inductors. *IEEE Transactions on Microwave Theory and Techniques*, *56*(2), 475–486.