SYSTEM IMPLEMENTATION OF A 4X1 MIMO T/R MODULE AND KA-BAND LOW NOISE AMPLIFIERS FOR 5G APPLICATIONS

by
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ABSTRACT

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The demands for 5G systems are escalating rapidly, with a focus on higher data rates, lower latency, and long-distance communications. In order to fulfill these requirements, it is necessary to enhance noise suppression in receiver systems and to increase the linearity of communication links. Moreover, the power level of the signal is vital in compensating for the loss incurred through the air; hence, the gain of the system must be high enough. To meet these requirements, various approaches have been proposed, such as phased array systems, which comprise sub-blocks that manage the phase and amplitude of the system. By controlling these blocks, the direction and link distance can be regulated.

In this thesis, the first step was implementing a system comprising 4x1 Multiple in Multiple Out (MIMO) chips and down/upconverter mixers. The system-level performance of these configurations was subsequently tested. A comparative analysis was conducted between 0.13 μm SiGe BiCMOS technology and 0.13 μm SiGe BiCMOS Cu technology with respect to their noise performance characteristics, which involves the design and testing of a low noise amplifier (LNA) in 0.13 μm SiGe BiCMOS Cu technology. After these evaluations, two distinct LNAs were designed using 0.13 μm SOI CMOS technology to improve the linearity. Their performance was analyzed and compared with the previously designed LNA.

ÖZET

4X1 MIMO ALICI VERİCİ MODÜLLERİNİN SİSTEM ENTEGRASYONU VE 5G UYGULAMALARI İÇİN KA BANT DÜŞÜK GÜRÜLTÜLÜ YÜKSELTİCİLER

ŞERAFETTİN SERHAN ÖZBOZ

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Anahtar Kelimeler: MIMO T/RX, 5G SİSTEMLER, DÜŞÜK GÜRÜLTÜLÜ YÜKSELTİCİLER, 24 -30 GHz

5G sistemlerin talepleri, daha yüksek veri hızı, daha düşük gecikme süresi ve daha uzak mesafe iletişimine odaklanarak hızla artıyor. Bunları gerçekleştirmek için, alıcı sistemlerde gürültü bastırmanın arttırılması ve iletişim bağlantılarının doğrusallığını artırılması gerekmektedir. Ayrıca, güç seviyesi hava yoluyla oluşan kaybın telafi edilmesinde hayati önem taşır; dolayısıyla, kazanç yeterince yüksek olmalıdır. Bu koşulları sağlamak için çeşitli yaklaşımlar kullanılmıştır, alt bloklardan oluşan aşamalı faz dizi sistemleri bunlardan biridir. Bu sistemler alt bloklar ile sistemin genliğini ve fazını kontrol edebilirler. Bu kontrol ile sinyalin yönü ve ne kadar uzağa gideceği ayarlanabilir.

Bu tezde ilk aşama olarak 4x1 MIMO çipleri yukarı aşağı karıştırıclar ile birleştirilmiştir sonrasında sistem seviyesinde performansları test edilmiştir. Sonrasında 0.13 μm SiGe BiCMOS teknolojisi ve 0.13 μm SiGe BiCMOS Cu arasındaki farklar incelenmiştir. Bununla beraber 0.13 μm SiGe BiCMOS Cu teknolojisi kullanılarak düşük gürültülü yükseltici tasarlanıp bu çipin performansı test edilmiştir. Bu değerlendirmelerin ardından doğrusallığı geliştirmek için iki farklı düşük gürültülü yükseltici 0.13 μm SOI CMOS teknolojisinde tasarlanmıştır. Bu tasarımların performansları önceki tasarım göz önünde bulundurularak incelenmiştir.

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To my family...
Aileme...

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1. INTRODUCTION

1.1 5G Communication Systems

Mobile communication has seen rapid evolution, with the requirements needed to satisfy the demands of such communication systems escalating alongside this development. The rise in popularity of video calls and high usage by large populations have compelled enhancements in data transfer capabilities. Every generation of communication systems has witnessed a significant increase in utilized bandwidth, fulfilling the corresponding requirements of the time.

The first generation (1G) of mobile technology was introduced in 1980, featuring analog mobile phone systems (AMPS). As the number of users rapidly increased, there emerged a need to augment capacity, leading to the development and introduction of second-generation (2G) technology by the end of the 1980s. During this generation, bandwidths of 890 MHz - 960 MHz were employed, with maximum data rates of 28.8 kilo bits per second (BPS). Given the limited data rate capability of 2G, the third generation (3G) was launched in 2001. This generation made high-speed internet and video communications available, with data rates escalating to approximately 2 MBPS. A substantial increase in data rates was observed in the transition from 3G to the fourth generation (4G), with rates reaching up to 200 MBPS (Rao, 2012). The evolution of mobile communication systems is depicted in Fig. 1.1.

The fifth-generation (5G) standards in communication systems aim to attain high data rates in the scale of GHz, low latency, and extended-range communications (Andrews, Buzzi, Choi, Hanly, Lozano, Soong & Zhang, 2014). However, meeting these demands escalates the complexity of the systems, necessitating the development of various techniques to address these requirements. These techniques have evolved over time, involving innovation in aspects such as phased array systems,

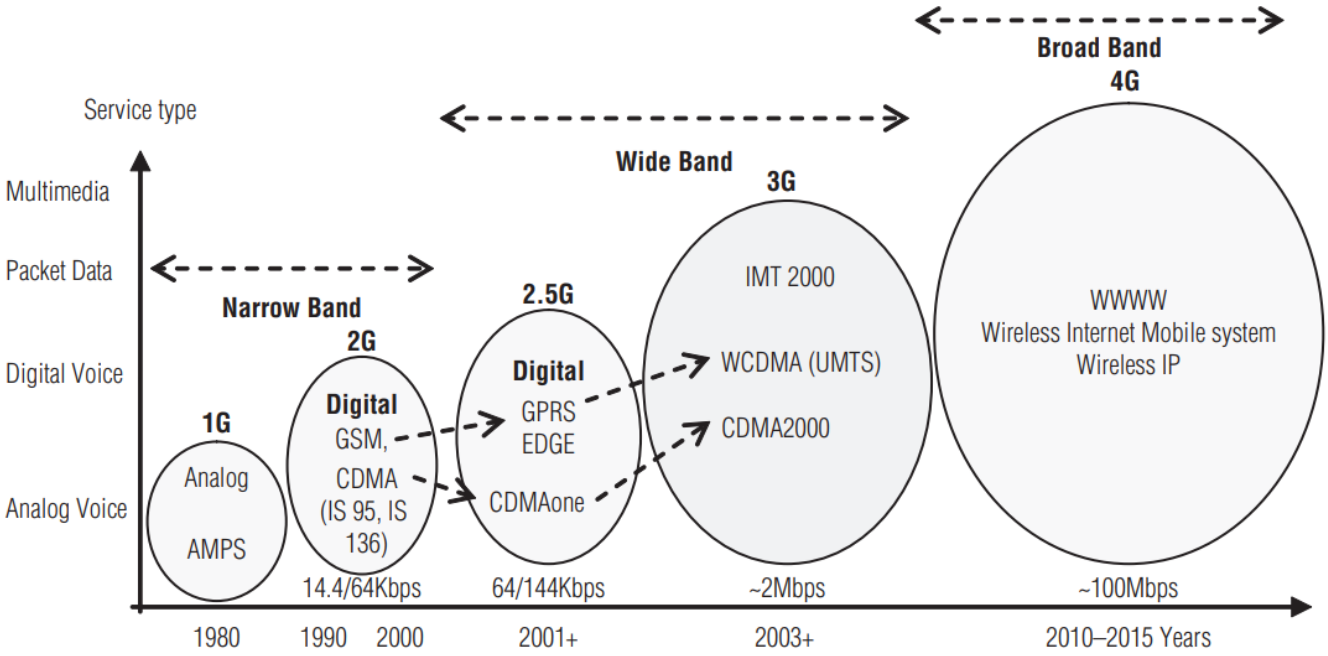


Figure 1.1 The history of the mobile communication (Rao, 2012)

beam-forming techniques, and noise suppression, all contributing towards the continual progression of mobile communication technologies.

Multiple-input multiple-output (MIMO) millimeter-wave modules are widely used due to their extensive communication range, where beam resolutions have become critical aspects. The path loss significantly degrades the signal over such long distances. As illustrated in equation (1.1), 'G' denotes the gain of the transmitter and receiver antennas, while 'P' signifies the power of the transmitter and receiver chains. The term 20log in the equation embodies the path loss in the air (Roh, Seol, Park, Lee, Lee, Kim, Cho, Cheun & Aryanfar, 2014). It's evident from the equation that as the distance increases, adjustments need to be made to the antenna gains or the power of the transmitter and receiver chains. However, distance is not the only cause of attenuation. As presented in the Fig. 1.2 at some frequencies the atmospheric loss increase significantly therefore working in these frequency bands demands more compensation (Rappaport et al., 2011). The reason these peaks are occurring is that at some frequencies the wavelength of the signal is aligned with the sizes of the some atoms in the air therefore additional attenuations are start occuring. Consequently, phased array antenna-based solutions have gained popularity owing to their beam-steering capability, which can achieve a high signal-to-noise ratio (SNR).

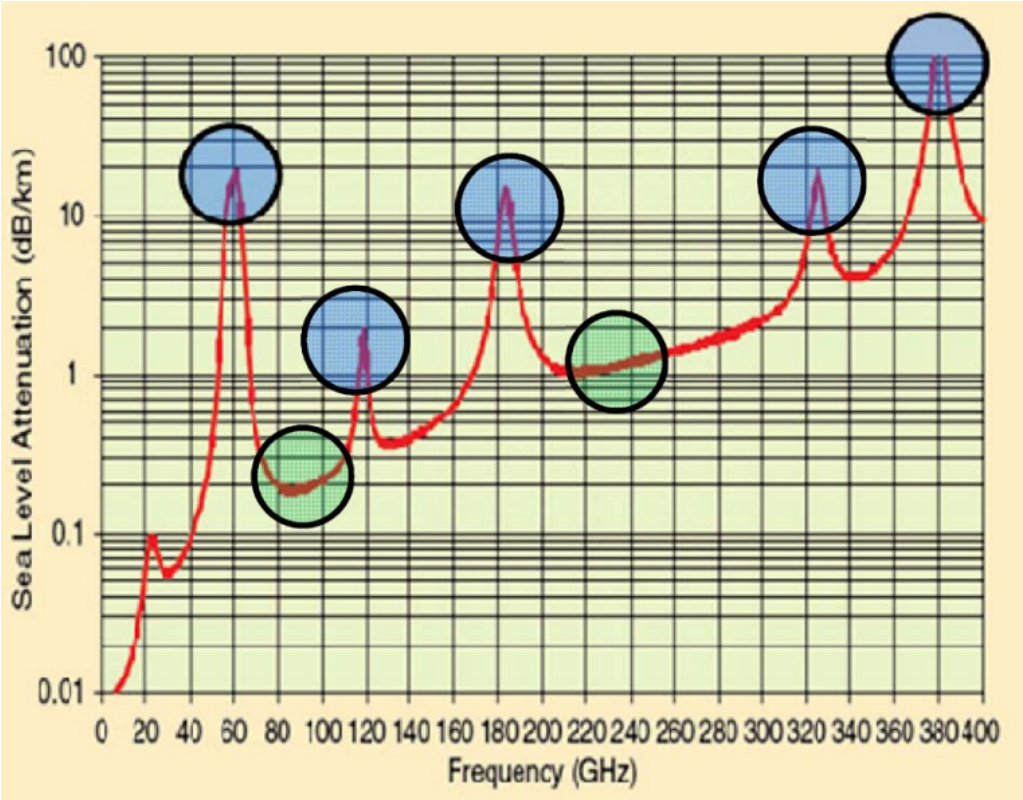


Figure 1.2 The atmospheric attenuation points respect to frequency (Rappaport et al., 2011)

$$P_r = P_t + G_t + G_r + 20log(\frac{c}{4\pi * Rf})(dBm) \tag{1.1}$$

Once the requisite signal power level needed to compensate for the path loss, as per equation (1.1), is determined, the maximum amount of data that can be transmitted through one channel can be calculated using equation (1.2). In this equation, 'B' represents the data bandwidth, 'S' denotes the received signal level, and 'N' signifies the noise level. It is clear from this equation that, for high data rate transfer, the received signal level must be as high as possible, and noise should be minimized, or in other words, the SNR should be high.

$$C = B * log_2(1 + \frac{S}{N}) \tag{1.2}$$

$$N = kTB \tag{1.3}$$

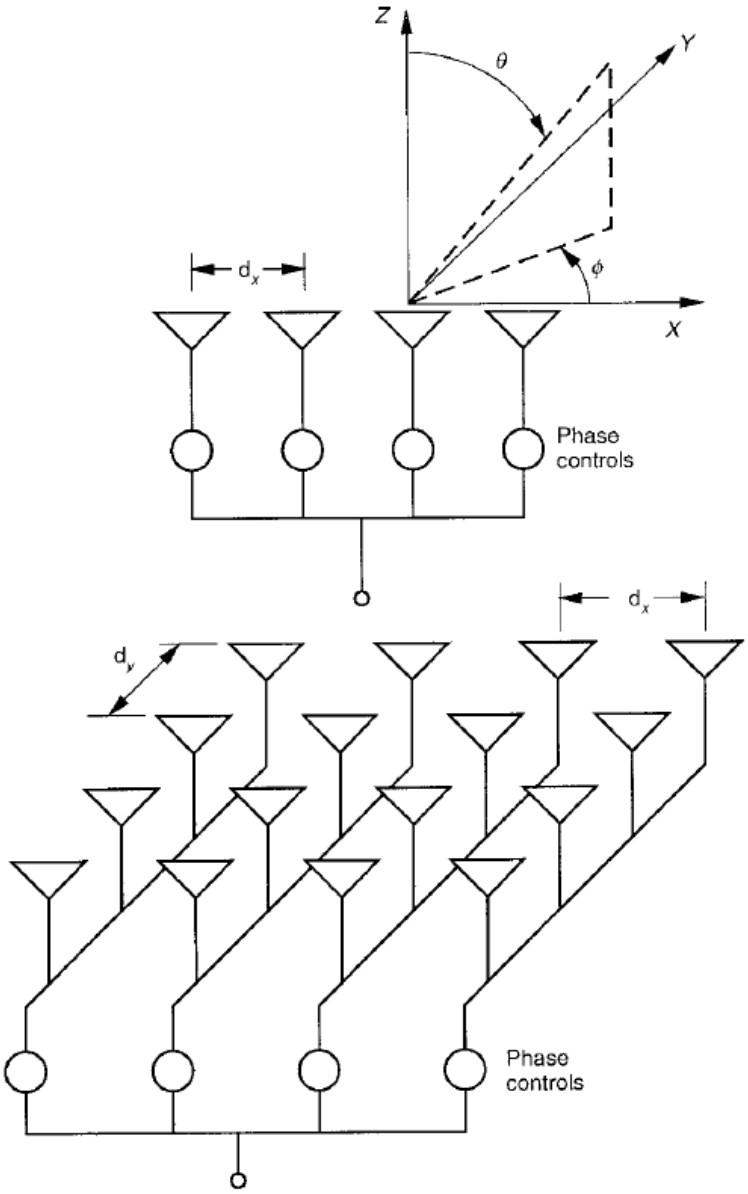


Figure 1.3 The demonstration of the phassed array systems (Mailloux, 1994)

Another important requirement for high data transfer is bandwidth. As bandwidth increases, the data rate also increases significantly. However, as indicated in equation (1.3), as bandwidth increases, so does the noise level. In equation (1.3), 'k' is the Boltzmann constant, thus its effect will always be present. The other parameter, 'T', represents temperature. As the temperature decreases, higher data rates can be achieved.

1.2 Phased Array Systems

Phased array systems are modules that incorporate multiple antennas. Along with phase shifters (PS), these systems can control the phase of each individual antenna and carry out beam scanning. Such systems also include a variable gain amplifier (VGA) or attenuator (ATT) to control the system's amplitude for pattern shaping (Mailloux, 1994). Furthermore, amplifiers are used to boost the signal. In a receiver system, a low noise amplifier (LNA) is employed as the first block, while a power amplifier (PA) is utilized at the final stage in a transmitter system. The use of antenna arrays aims to enhance the directivity of the beam, as illustrated in Fig. 1.3. since in the system, there are an array of antenna elements, causing variations in the arrival of the signal. The variable 'N' in equation (1.4) indicates the antenna element. Since each channel has its own control blocks, the beam can be adjusted with respect to the angle θ.

$$x = N * d * sin(\theta) \tag{1.4}$$

As there are multiple antennas in a phased array system, the arrival times of signals will differ among antennas, unless the arrival angle is precisely 90 degrees. Consequently, the PS manage the phase of the system and calibrate the signals such that they align across all channels and control the direction of the beam. This calibration is achieved by taking equation (1.4) into account. The distance between these antennas is set at $\lambda/2$ to ensure that all signals aggregate coherently at the frequency of interest. This scenario presents one of the trade-offs in phased array systems. Given that λ is frequency-dependent, the applications of phased arrays tend to be narrowband compared to true time-delayed systems.

1.3 Technology

Silicon (Si), being one of the most abundant elements in nature and amenable to doping, is widely used in the IC industry. Silicon Germanium (SiGe) technologies require smaller bandgaps compared to Si, due to the introduced germanium reducing

the bandgap level (Cressler & Niu, 2003). Another significant attribute of SiGe technology is its easy integration with SiGe Heterojunction Bipolar Transistors (HBT) and Si Complementary Metal Oxide Semiconductor (CMOS) technologies. This advantage facilitates the utilization of SiGe Bipolar Complementary Metal Oxide Semiconductor (BiCMOS) technologies. A major advantage of SiGe technologies over III-V semiconductors is the ability for integration with CMOS.

As previously mentioned, receiver systems need to exhibit good noise performance and linearity, and remain cost-effective to enable mass manufacturing. In terms of linearity and noise, SiGe BiCMOS technology outperforms CMOS technologies, while offering comparable performance to III-V technologies. Furthermore, SiGe shows more advantages in terms of phase noise, output conductance, and power dissipation. However, when it comes to linearity, III-V technologies showcase superior performance, as presented in Table 1.1. The 0.13 μm SiGe BiCMOS technology boasts a transit frequency (f_t) of 240 GHz and a maximum oscillation frequency (f_{max}) of 340 GHz.

This thesis makes use of three different technologies, which will be discussed in greater detail in Chapter 3. The differences between SiGe BiCMOS and SiGe BiCMOS Cu technologies. SiGe BiCMOS technology consists of five lower-level metal layers and two top metals which utilize aluminum (Al). In contrast, SiGe BiCMOS Cu technology maintains the similar five lower metals but includes an additional two copper layers. These copper layers have higher conductance, thus offering lower sheet resistance (Aljuhani & Rebeiz, 2019). Since the current-carrying capacity of copper is superior to that of aluminum, it enhances the quality factors of the inductors.

The GlobalFoundries 0.13 μm Silicon on Insulator (SOI) CMOS technology is also utilized in this work and will be expounded upon in more detail in Chapter 3. This technology has a transit f_t of 220 GHz and a f_{max} of 250 GHz (Kuo, Kuo). It comprises three lower metal layers and one top metal layer. Given that there is only one top metal layer thick enough to minimize sheet resistance suitably for inductor design, this layer is employed for that purpose. As the name suggests the body terminal of the transistor is left floated and isolated, which decreases the parasitic effects due to the body connection. As the name implies, the body terminal of the transistor is left floating and isolated, thereby reducing the parasitic effects that may otherwise arise from the body connection. Another advantageous feature of SOI CMOS technology is its facility for straightforward digital implementation, coupled with cost-effective manufacturing options.

Table 1.1 The comparison of the different technologies (Excellent: ++; Very good: +; Good: 0; Fair: - ; Poor: - -)(Cressler & Niu, 2003)

Performance Metric	SiGe HBT	Si BJT	Si CMOS	III-V Mesfet	III-V HBT	III-V HEMT
Frequency Response	+	0	0	+	++	++
1/f and phase noise	++	+	-	- -	0	- -
Broadband Noise	+	0	0	+	+	++
Linearity	+	+	+	++	+	++
Output conductance	++	+	-	-	++	-
Transconductane/area	++	++	- -	-	++	-
Power dissipation	++	+	-	-	+	0
CMOS integration	++	++	N/A	- -	- -	- -
IC cost	0	0	+	-	-	- -

1.4 Motivation

The demands for data transfer have significantly increased with the introduction of the 5G New Radio (NR) communication specifications (Lin, Li, Baldemair, Cheng, Parkvall, Larsson, Koorapaty, Frenne, Falahati, Grovlen & Werner, 2019). To fulfill the requirements for long-distance communications and high data rate transfers, it is critical to ensure high noise suppression and linearity, as indicated in Equation (1.2). Initially, the system-level receiver chain was tested to assess the SNR performance. Subsequently, this thesis examines different technologies to meet these demands and discusses the outcomes. Specifically, two distinct designs were conceived for linearity improvement, and their performances are thoroughly discussed.

1.5 Thesis Organization

The subsequent chapter focuses on the system implementation of the 4x1 MIMO Transmitter (Tx) and Receiver (Rx) integrated circuits (IC). To process the data, both Analog to Digital Converter (ADC) and Digital to Analog Converter (DAC) are necessary components of the transmitter and receiver systems. Consequently, in the receiver system, it becomes necessary to reduce the frequency levels of the received signal. To facilitate this, a passive HMC 292 ADI mixer is used to downconvert the frequency to 500 MHz. Conversely, in the transmitter system, the data to be transmitted exists at lower frequencies and must be upconverted to the target frequency. Here again, the HMC 292 ADI mixer is employed for its upconversion capability.

Chapter 3 examines three distinct LNAs. The first LNA, designed using 0.13 μm SiGe BiCMOS Cu technology, is assessed to ascertain whether its noise performance can be enhanced compared to the 0.13 μm SiGe BiCMOS technology. Consequently, the quality factors of the identical inductors in both technologies are examined. Given the critical role of the base inductor in terms of noise, it has been given primary consideration. The LNA's measurement results and simulation data are compared and analyzed. The subsequent two LNAs are designed using 0.13 μm SOI CMOS technology. The first LNA is conceived as a reference LNA, aimed at achieving optimal noise and linearity performance, along with flat gain and satisfactory matching. A linearization technique is then applied to the second LNA, after which the results from these two LNAs are compared and discussed.

The final chapter discusses the summary of the work undertaken and explains the future work to be completed.

2. MIMO SYSTEM APPLICATION

2.1 Introduction

This chapter analyzes the fundamental components incorporated in the designed modules, together with an analysis of the resultant measurements. The system under consideration is composed of distinct Rx and Tx modules, each furnished with common sub-blocks. Both modules incorporate a 4x1 Multiple-Input Multiple-Output (MIMO) chip and a Direct Current (DC) to a 24-28 GHz mixer. The MIMO chips were designed by my colleague, Abdurrahman Burak (Burak, 2021), employing 0.13-μm SiGe BiCMOS technology. In addition, an Analog Devices Inc. (ADI) HMC292 mixer chip was utilized as a mixer. The MIMO chips were specifically designed to function within the 24-28 GHz frequency band.

2.2 MIMO Chips

The block diagram depicting the architecture of the transmitter and receiver is provided in Fig. 2.1 and Fig. 2.2. Each channel in the architecture includes four primary elements: a 6-bit phase shifter, a 1-bit attenuator, and a 3-bit VGA. The arrangement is identical for both transmitter and receiver blocks.

To achieve a superior Side Lobe Level (SLL) suppression rate, both phase and amplitude bits need to be elevated. According to the reference (Mailloux, 2017), each bit increment enhances the suppression level by 6 dB, a relationship illustrated in Fig. 2.3. Furthermore, an increased number of antennas can further augment the

SLL suppression rate.

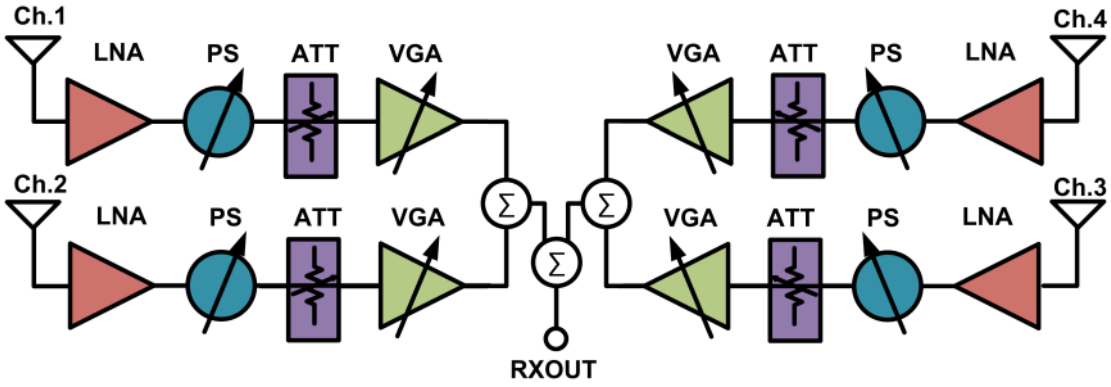


Figure 2.1 Block diagram of the Rx MIMO chip

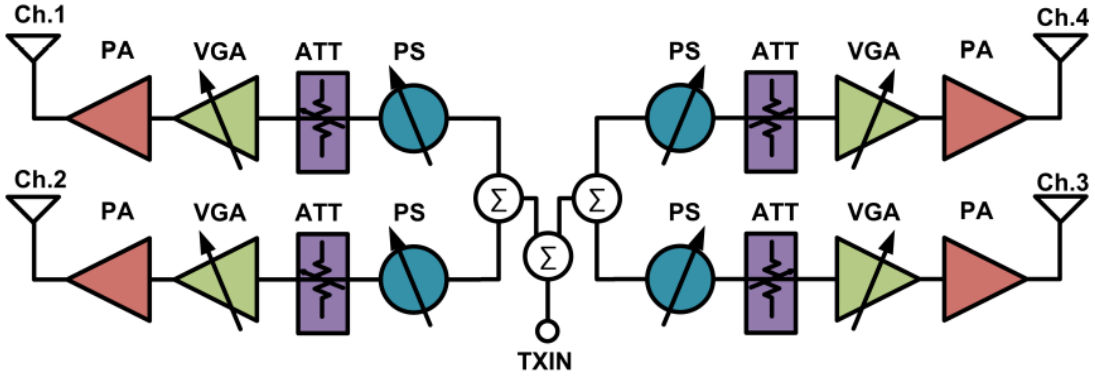


Figure 2.2 Block diagram of the Tx MIMO chip

The gain control section of the system encompasses two distinct blocks devised to expand the control range without escalating the Root Mean Square (RMS) phase error. The maximum attenuation level is 15 dB. Accordingly, the VGA and the attenuator are calibrated to attenuate a maximum of 7 dB and 8 dB, respectively.

The system employs a PA for the transmitter architecture and a LNA for the receiver architecture. Channels are combined via the Wilkinson combiner, and control voltages are regulated using the Serial Peripheral Interface (SPI) block.

The PS, attenuator, and VGA are identical for both Tx and Rx architectures. However, their placement varies within the transmitter and receiver chains, reflecting the different operational requirements of each component.

In the transmitter, the PA, being the component that delivers the highest power, is strategically positioned at the end of the channel. The VGA, due to its superior linearity performance compared to the PS, is located just before the PA. To avoid

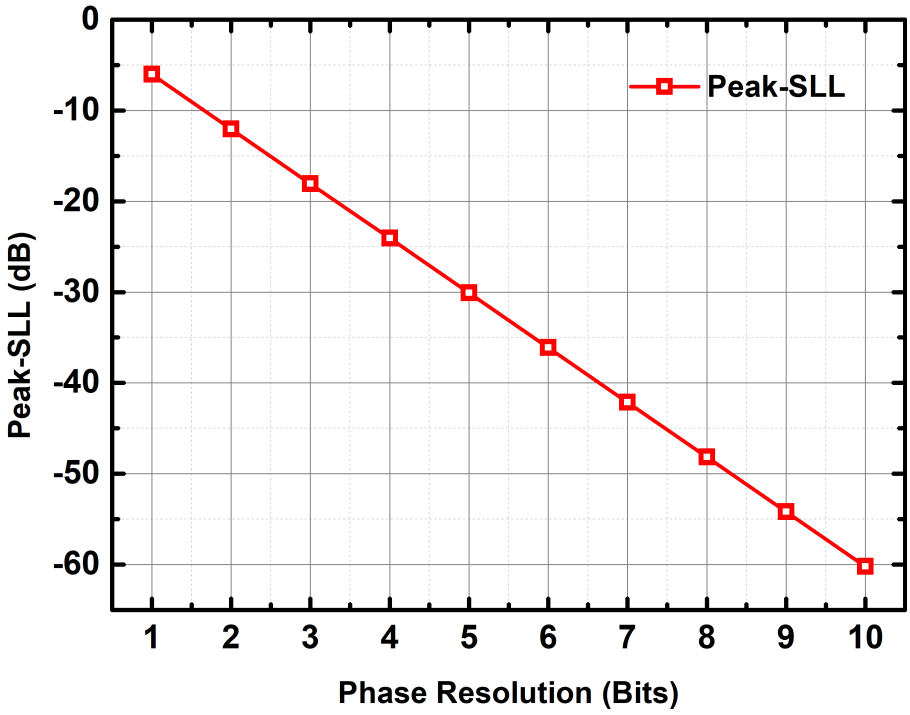


Figure 2.3 Peak SLL suppression on increasing number of bits.

degradation of amplitude and phase performance of the entire system due to return losses, the attenuator is situated before the VGA.

In the receiver chain, component placement is dictated by each sub-block's linearity and noise performance. The LNA is placed at the forefront due to its excellent noise performance. Despite the PS's comparatively poorer noise performance, it follows the LNA to optimize linearity. The LNA's role in suppressing noise in the initial stage ensures that the PS does not contribute to a gradual degradation of the system's overall noise performance. As with the transmitter module, the attenuator is positioned prior to the VGA for the same rationale.

The photographs of the chips are displayed in Fig. 2.4. Each channel for both chips occupies an area of 1.85x0.45 mm^2. The input and output return losses of both the Tx and Rx modules are depicted in Fig. 2.6 and Fig. 2.7 respectively. In the Rx channel, the input return loss is below -10 dB within the 26-35 GHz range. In contrast, for the Tx channel, the input return loss is below -10 dB within the 19-31 GHz range. Regarding the output return loss, in the Rx channel, it is less than -10 dB within the 24-40 GHz range. Meanwhile, the output return loss in the Tx channel is below -10 dB in the 22-27 GHz range across all amplitude control levels. Measurements for S22 of the Rx module and S11 of the Tx module deviate from the simulation results due to the shunt capacitive effects of the pads. However, these measurements still align with the frequency band, as illustrated in Fig. 2.8 and Fig.

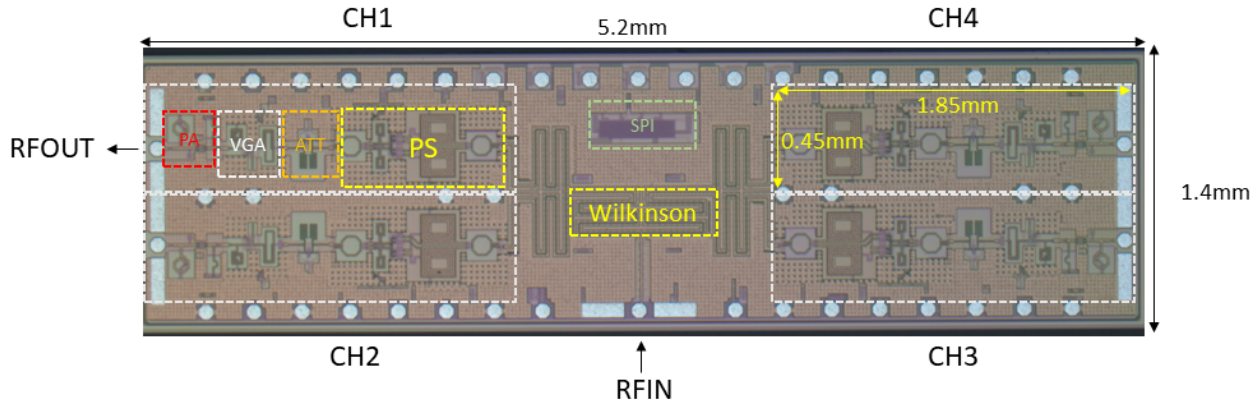


Figure 2.4 Die photograph of the Tx chip

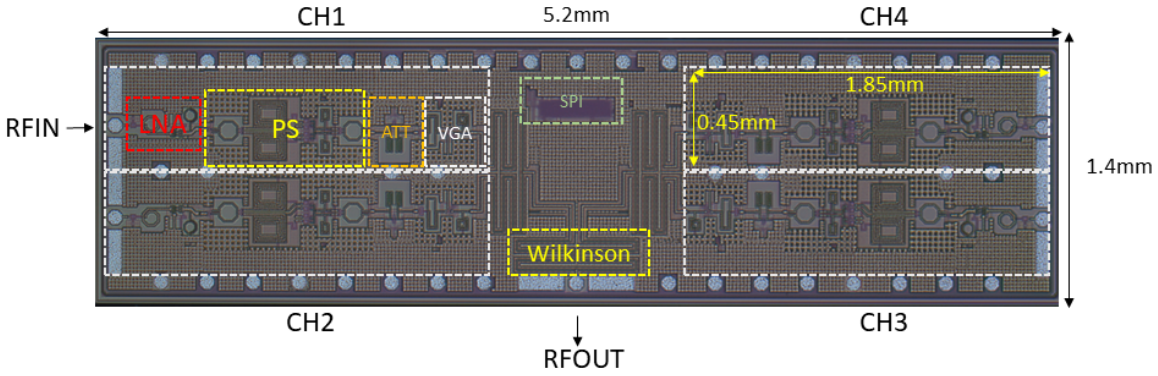


Figure 2.5 Die photograph of the Rx chip

2.9.

The single-channel peak gain for the Rx module is 15.3 dB at a 26 GHz frequency, with a 3 dB bandwidth exceeding 7.5 GHz. For the Tx module, the peak gain stands at 26.2 dB at a 26 GHz frequency, with a 3 dB bandwidth exceeding 7 GHz. The Wilkinson divider imparts an 8 dB loss, hence, this 8 dB loss is incorporated when calculating the gain of the blocks, as depicted in Fig. 2.10 and Fig. 2.11.

The measured Noise Figure (NF) performance of the Rx module stands at 4.3 dB at the 26 GHz center frequency, with the NF not exceeding 4.6 dB across the frequency band. Fig. 2.12 presents a comparison between the simulated and measured NF performances.

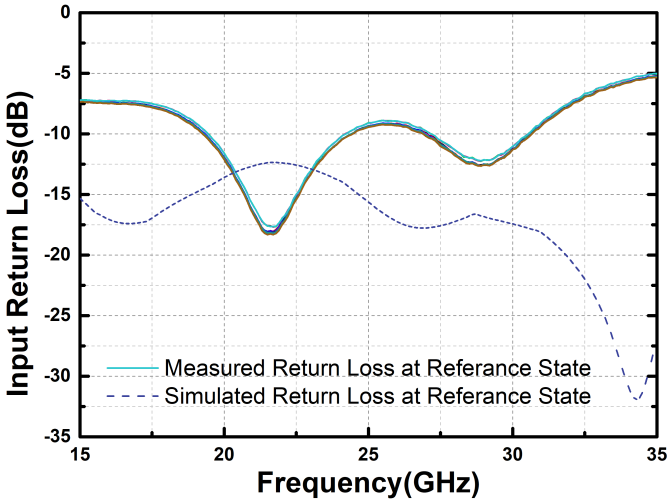


Figure 2.6 S11 of the Tx chip

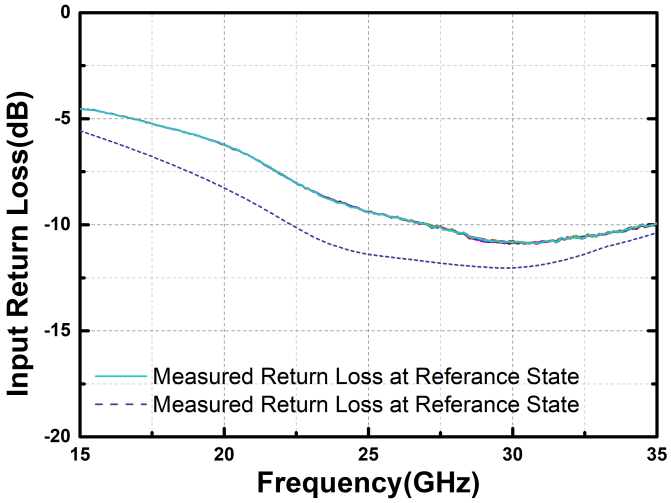


Figure 2.7 S11 of the Rx module

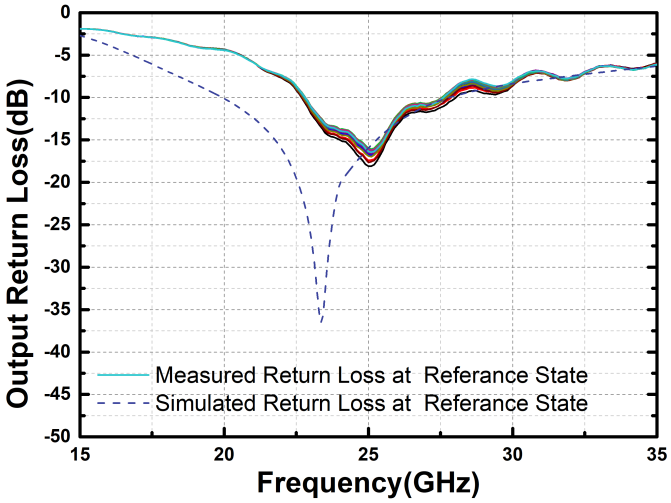


Figure 2.8 S22 of the Tx chip

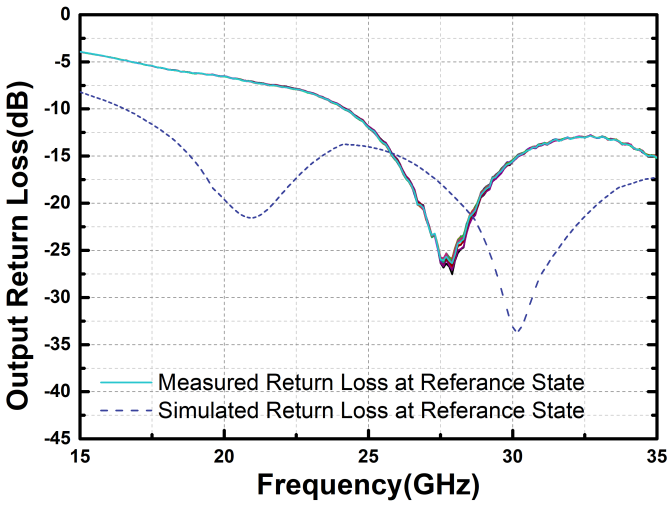


Figure 2.9 S22 of the Rx chip

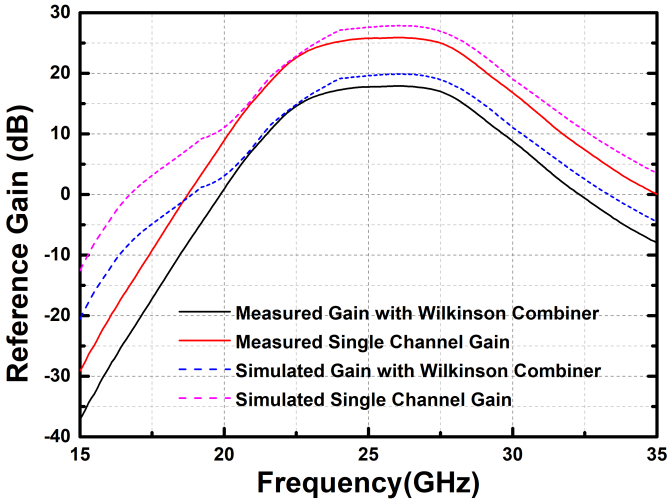


Figure 2.10 S21 of the Tx chip

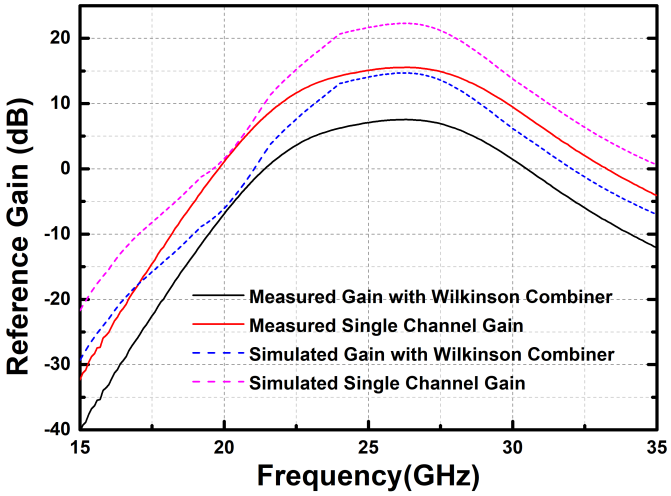


Figure 2.11 S21 of the Rx chip

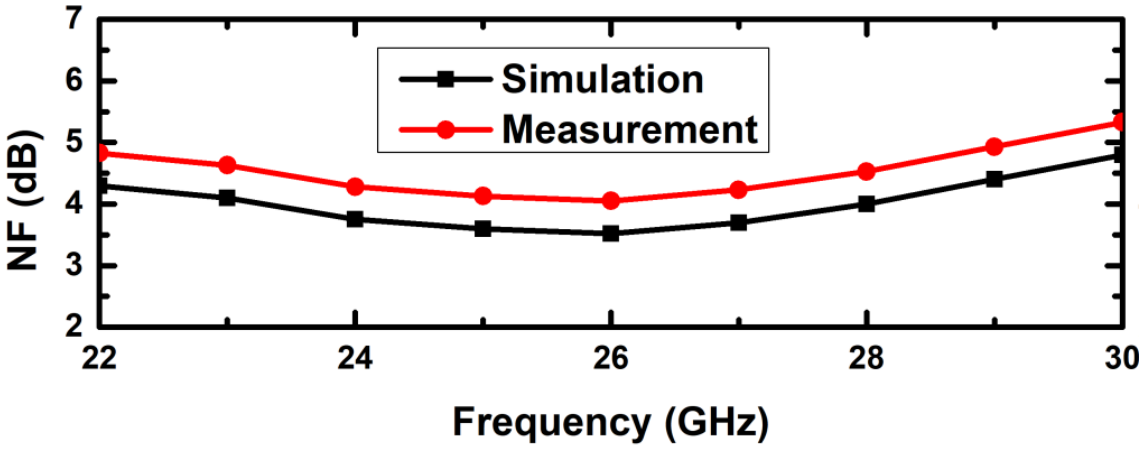


Figure 2.12 Noise figure of the Rx chip

2.3 Design of the PCB

The Rx and Tx chips are integrated with an off-chip mixer (Analog Devices Inc. HMC292) to facilitate signal downconversion/upconversion. A Rogers 6209 PCB substrate is utilized to merge these two blocks. The Rx and Tx dies are packaged using flip-chip packaging.

Both chips occupy the same sub-blocks with the exception of the LNA and PA. Therefore, their dimensions are identical. However, the LNA and PA are situated at the input and output of the blockchain respectively. The sequence of the remaining sub-blocks VGA, PA, and attenuator varies due to the optimization of either linearity or the NF.

Given the different sub-block placements for each module, unique matching circuitry has been designed for both the Tx and Rx on the board. Matching between the modules and mixer on the PCB is achieved with transmission lines and open stub transmission lines. The positioning of the open stub and its corresponding ground via placements are critical for conjugate matching. The behavior of the open stub, whether it acts more capacitive, depends on the distance of the ground vias from the transmission lines and stubs, given that the transmission lines used are coplanar.

The input of the Rx module is designed exclusively with transmission lines to optimize both the Noise Figure and matching. To augment the isolation between each port, ground vias are situated at the sides of each transmission line. Electromagnetic (EM) simulations were conducted using the Keysight ADS tool. The PCB implementations are depicted in Fig. 2.13 and Fig. 2.14.

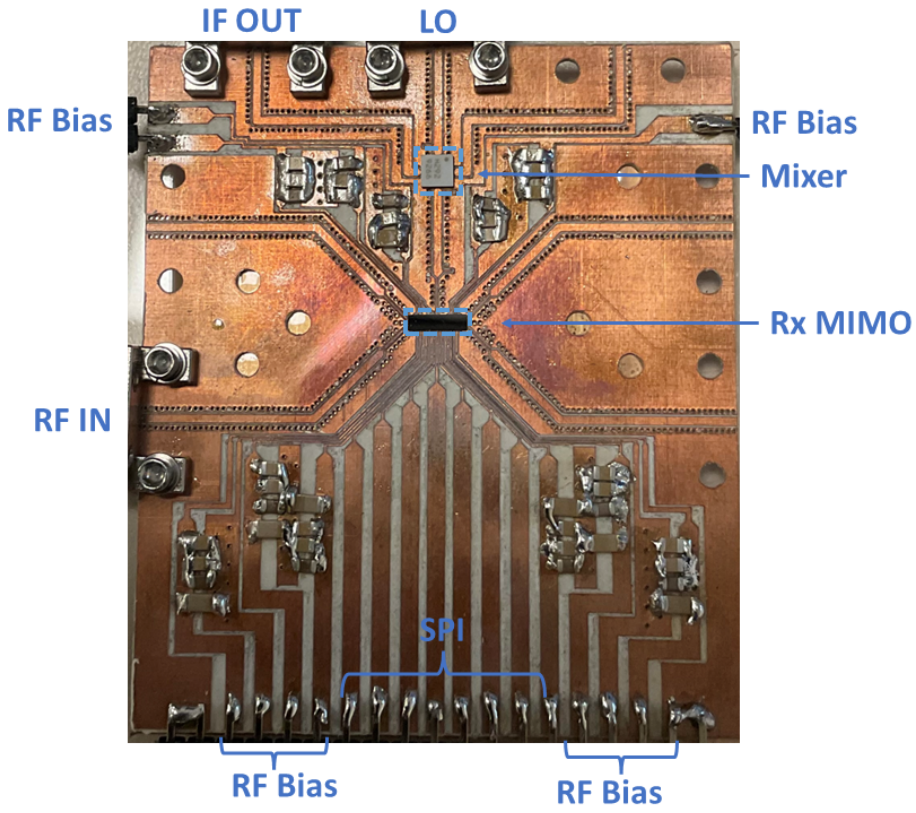


Figure 2.13 Receiver PCB design

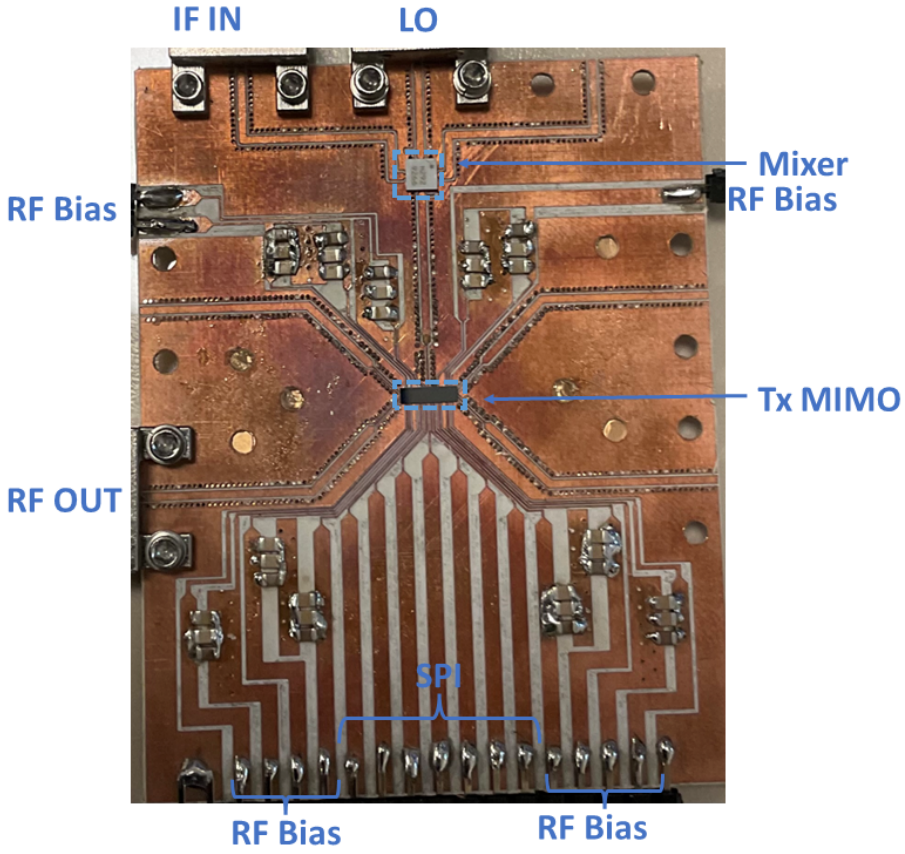


Figure 2.14 Transmitter PCB design

2.3.1 System Measurements

The S-parameters of the system were initially measured using a Keysight N5224A Programmable Network Analyzer (PNA). The Radio Frequency (RF) cables were connected to the input and output terminals of the boards, with the Local Oscillator (LO) signal generated using an E8257D PSG Analog Signal Generator. The measurement setup for both boards is depicted in Fig. 2.15 and Fig. 2.16.

The input frequency of the Rx board ranges from 24 to 28 GHz, while the output is approximately 500 MHz. Given the low output frequency, which is to be demodulated and digitized via an ADC, the output port matching is not critical. Similarly, the Tx board's input is 500 MHz; therefore, input matching is not a critical consideration, with the primary focus being on output matching.

The EM simulated and measured input return losses for the Rx board are presented in Fig. 2.17, while the simulated and measured output return losses are shown in Fig. 2.18. Given that both designs utilize coplanar transmission lines for matching, therefore multiple peak points are present in both designs. Both the Rx and Tx matching results demonstrate shifts due to the bump capacitances originating from the flip-chip packaging of the MIMO chips.

The measurement setups for the IP1dB are delineated in Fig. 2.19. The E8257D PSG Analog Signal Generator was employed to provide the LO power, maintaining a power level of 18dBm for both Tx and Rx boards. The E8267D PSG Vector Signal Generator was utilized to provide the input signal for both cases.

For the Rx board, the input signal was routed through one channel of the MIMO system, and the IF output port of the mixer was examined using the E4448A PSA Series Spectrum Analyzer. Different power levels of input signals were tested by modifying the LO frequency while maintaining the output frequency at 500MHz.

In the case of the Tx board, the input signal was applied through the IF input of the mixer at 500 MHz via the E8267D PSG Vector Signal Generator, and the output signal was captured in one channel of the MIMO system within the 24-28GHz band. To sweep the frequency levels, the LO frequency was adjusted while maintaining the frequency of the input signal at the 500MHz level.

As both designs considered only one channel, the resultant values were multiplied by four to account for the four channels of the MIMO system. However, the loss from the Wilkinson divider, approximately 7 dB, was subtracted from the total gain.

The IP1dB in terms of varying frequencies is presented in Fig. 2.20. As expected,

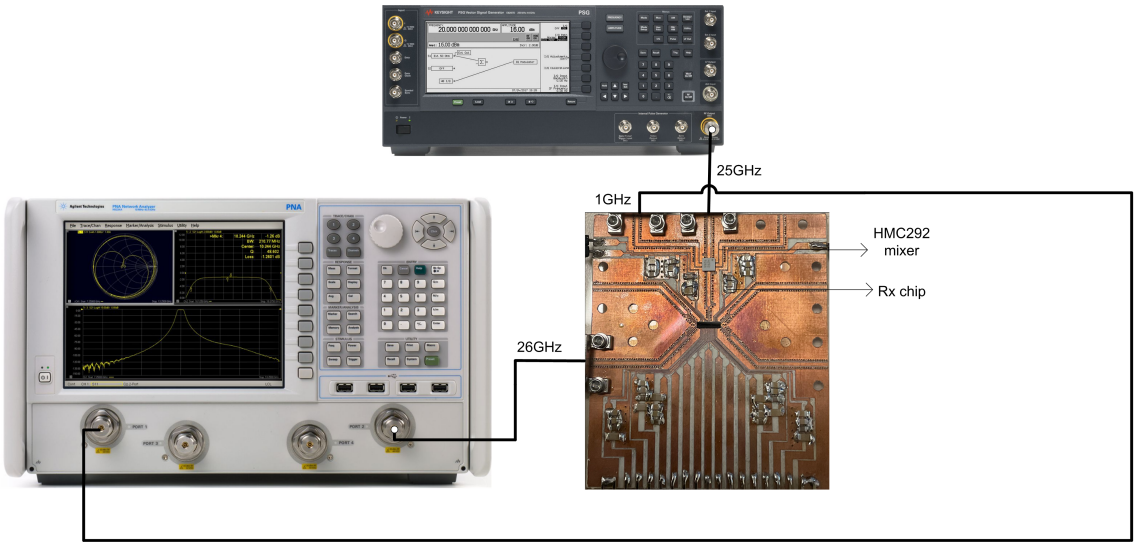


Figure 2.15 Rx board S11 measurement setup

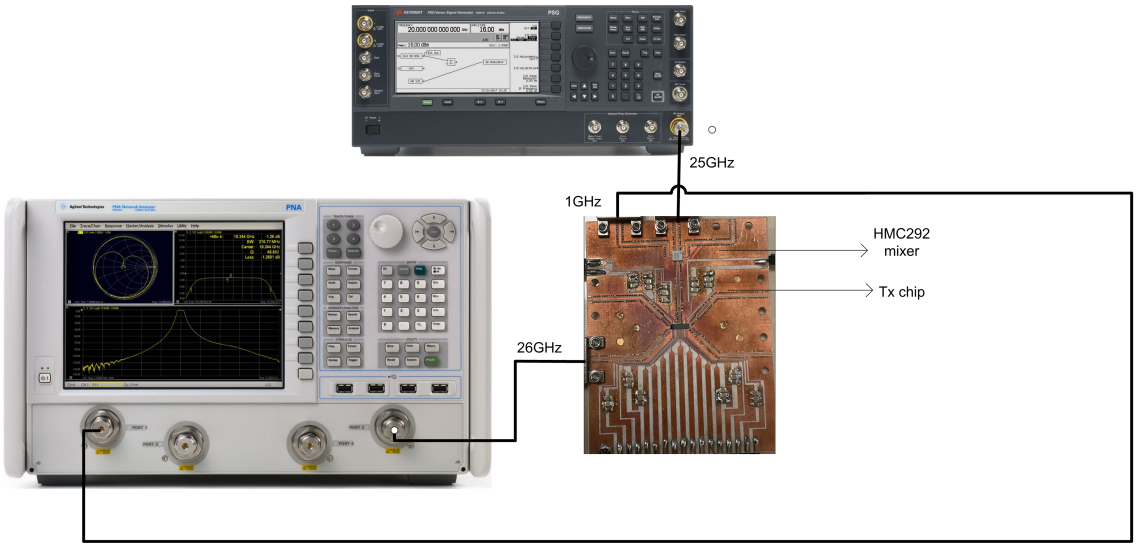


Figure 2.16 Tx board S22 measurement setup

the Rx board performance was approximately 1dB lower than that of the Tx board. The relationships between the input and output powers of the boards are depicted in Fig. 2.21. The mixer used is a passive type and exhibits an 10dB insertion loss. The board itself incurs around a 8 dB loss. The gain performances of both designs are coherent with the expected values, considering these loss factors.

The Error Vector Magnitude (EVM) measurement setup for the Rx and Tx modules is depicted in Fig. 2.22. For the Rx communication link, a modulated signal in the RF band is generated by the E8267D PSG Vector Signal Generator and applied to the PCB's input port. An external LO signal from the E8257D PSG Analog Signal Generator is used to downconvert the signal to 500 MHz by the mixer. The N9040B UXA Signal Analyzer then demodulates the Intermediate Frequency (IF)

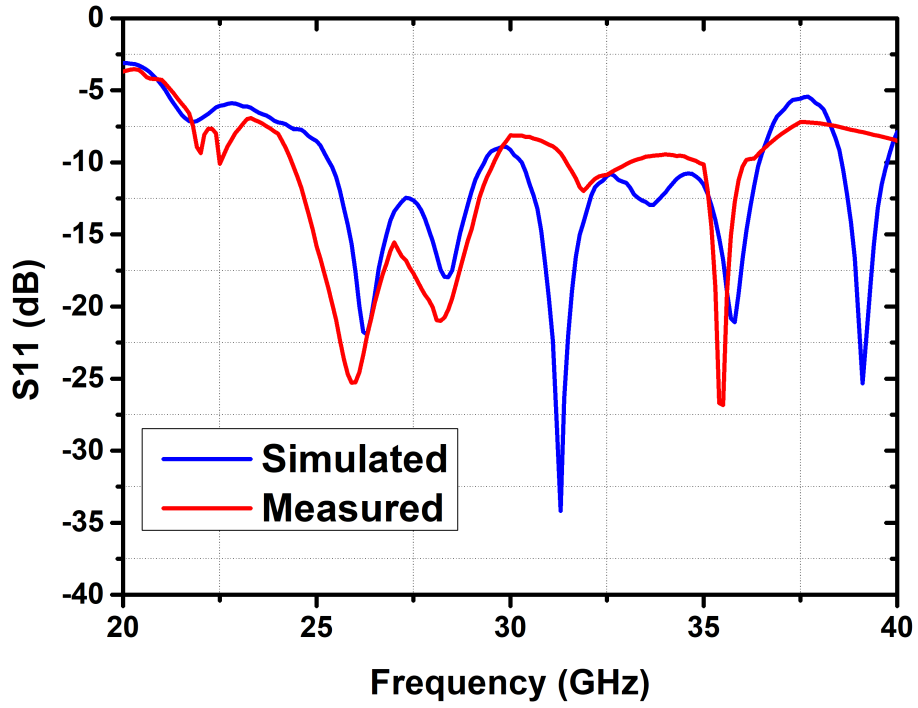


Figure 2.17 Rx board S11 measurement results

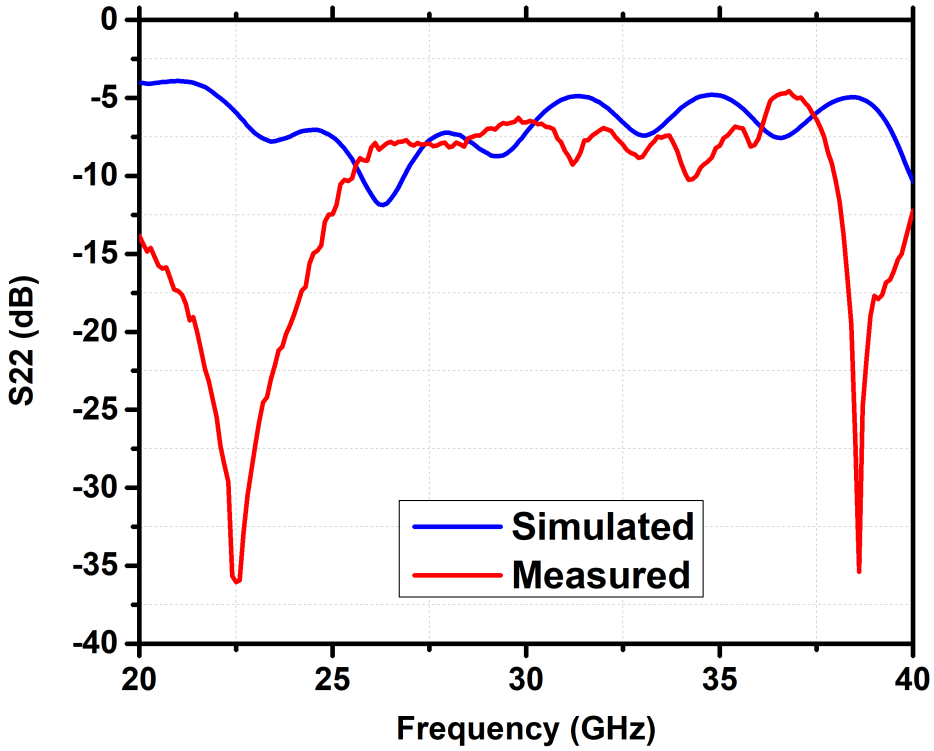
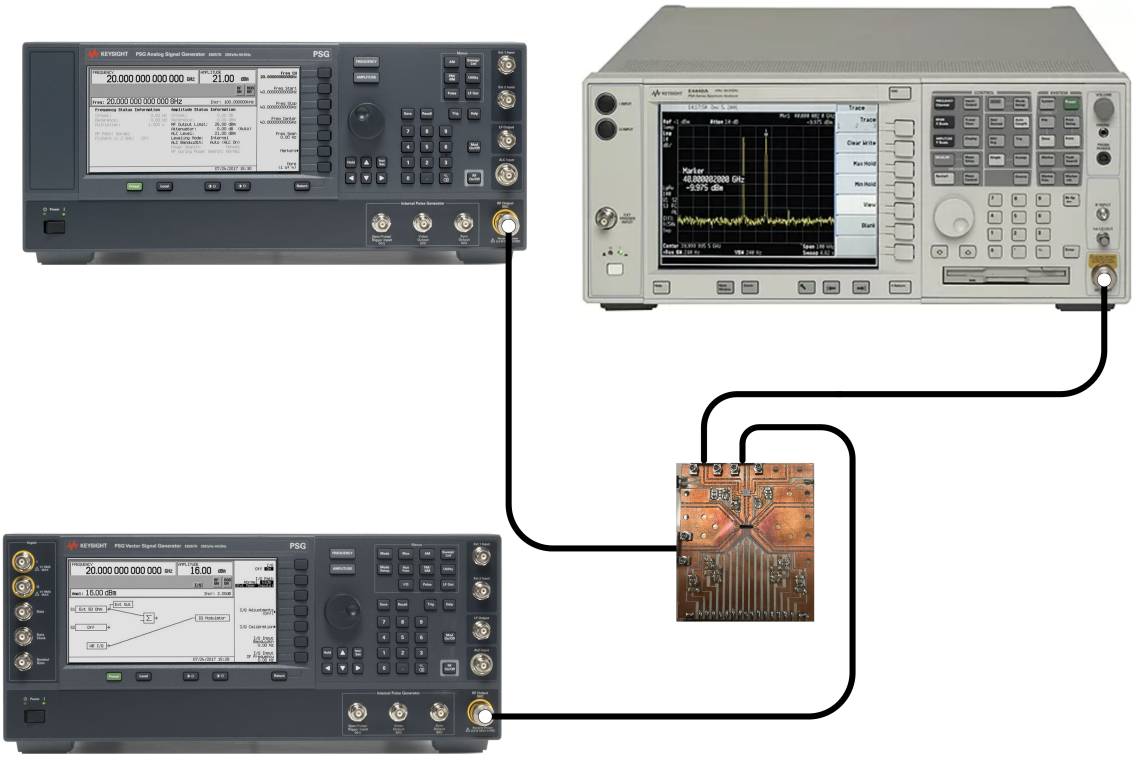
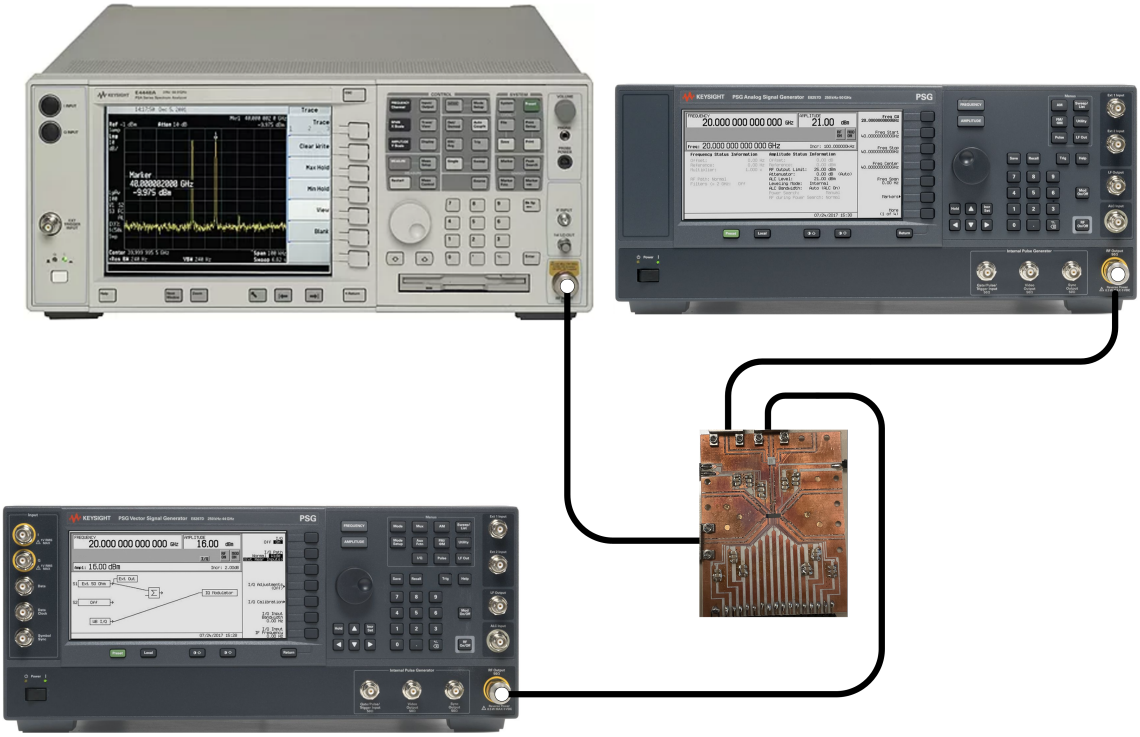


Figure 2.18 Tx board S22 measurement results



(a)



(b)

Figure 2.19 IP1dB measurement setup (a) Rx board (b) Tx board

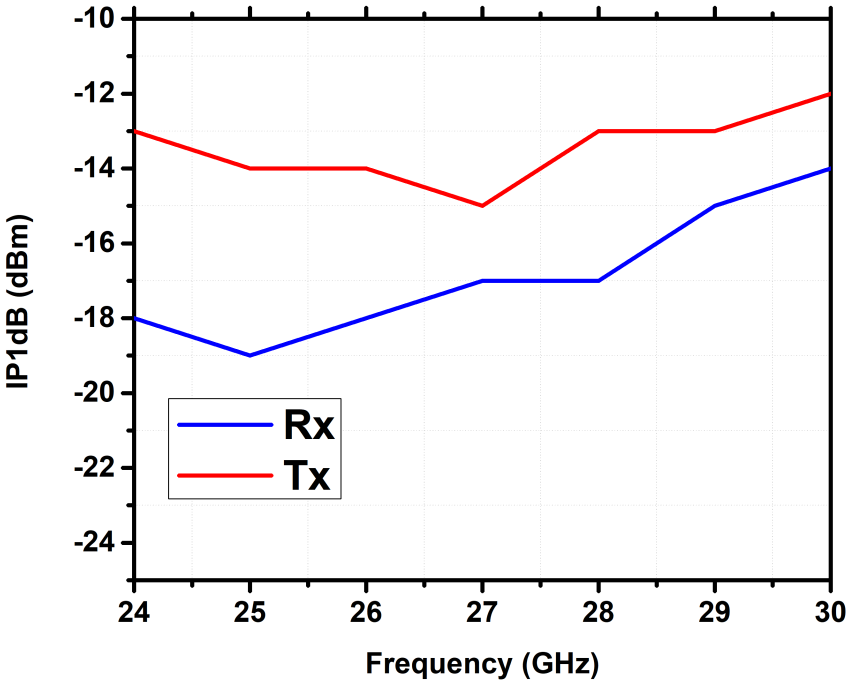


Figure 2.20 IP1dB of the both Rx and Tx board for different frequency levels

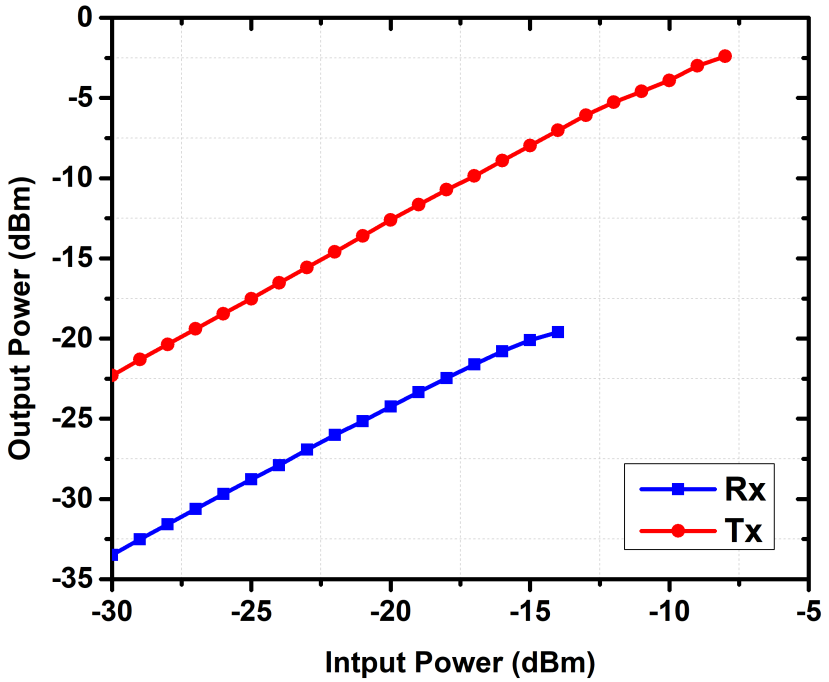
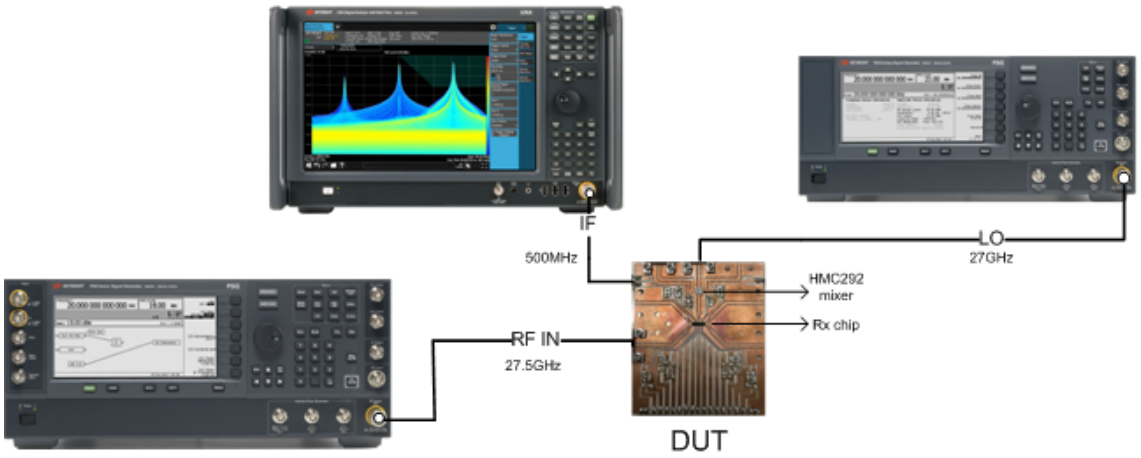
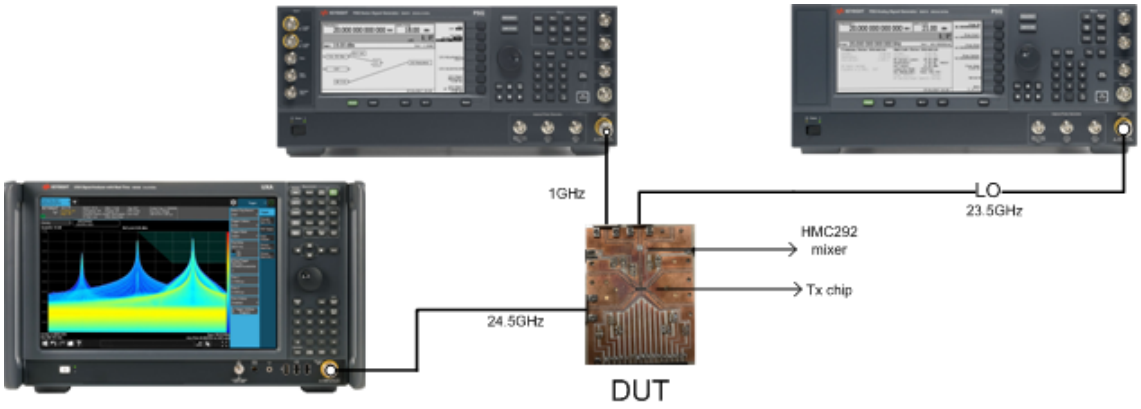


Figure 2.21 Power levels of the Rx and Tx board for different input powers



(a)



(b)

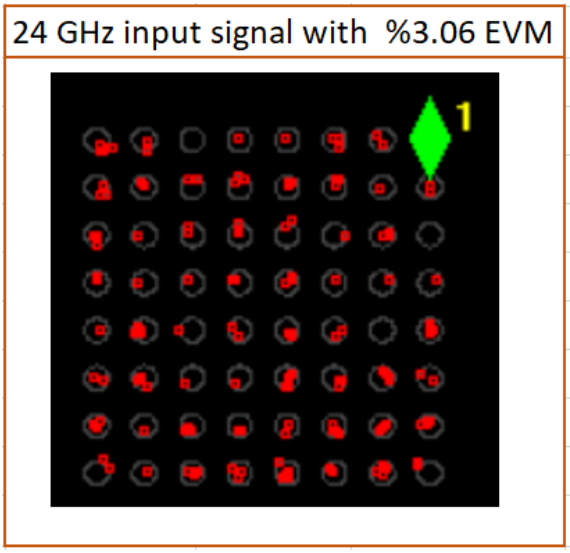
Figure 2.22 EVM measurement setup (a) Rx board (b) Tx board

band-modulated signal.

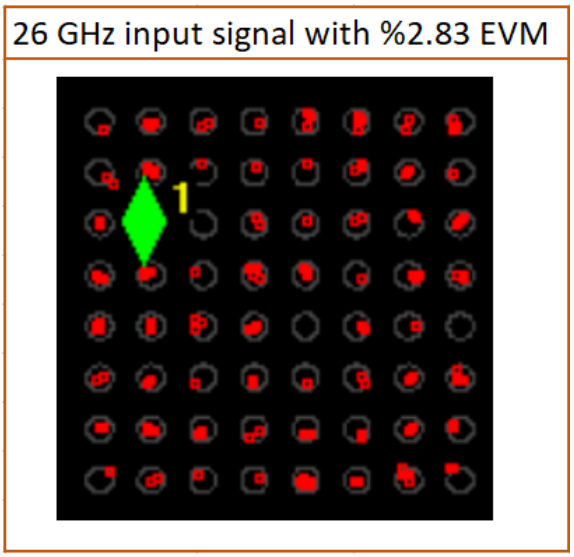
For the Tx measurements, a modulated IF signal (1 GHz) and an external LO are applied to the mixer. This process upconverts the signal to the RF band (24-28 GHz). The RF signal is subsequently demodulated using a signal analyzer identical to the one used in the Rx module. Different center frequency input signals have been applied in order to observe the behavior of the total system in the frequency band of interest.

Fig. 2.23 and Fig. 2.24 present the constellation diagrams for both the Rx and Tx modules across a range of frequencies. For the Rx module, a 50 Mbaud signal yielded a data rate of 300 Mbps across various carrier frequencies within the band. A 64-Quadrature Amplitude Modulation (QAM) scheme was employed, resulting in an EVM of 2.83% at the center frequency.

The selection of a modulation scheme is significantly influenced by the associated SNR performance, as the system's Bit Error Rate (BER) needs to remain minimally at 10^{-3} for an optimum function (Koranga & Barman, 2013). It is worth noting



(a)



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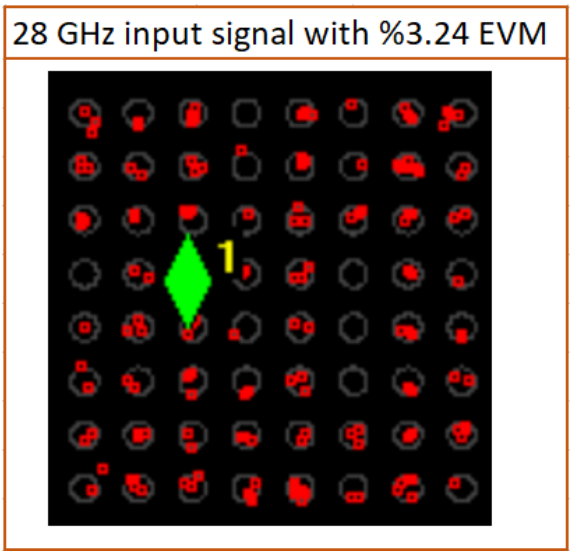
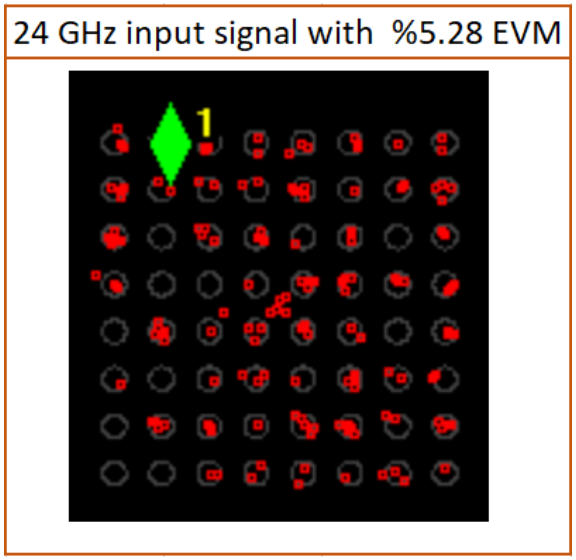
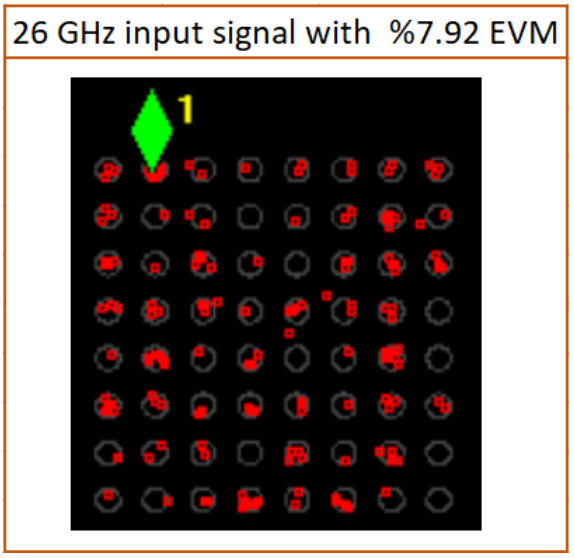


(c)

Figure 2.23 Measured EVM of Rx module using 64-QAM for different frequencies (a) 24GHz (b) 26GHz (c) 28GHz.



(a)



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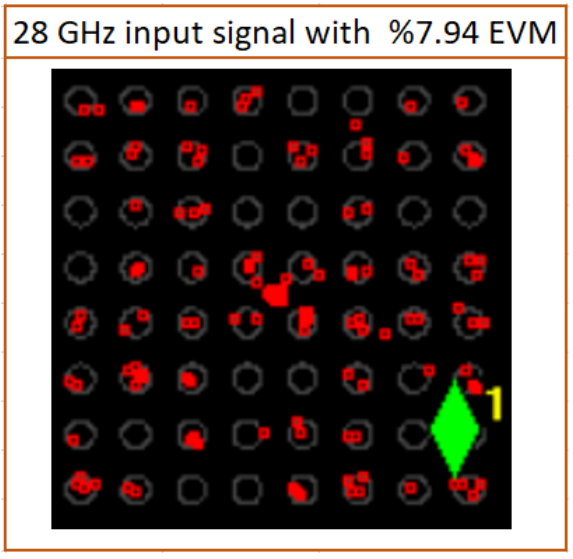


(c)

Figure 2.24 Measured EVM of Tx module using 64-QAM for different frequencies (a) 24GHz (b) 26GHz (c) 28GHz.

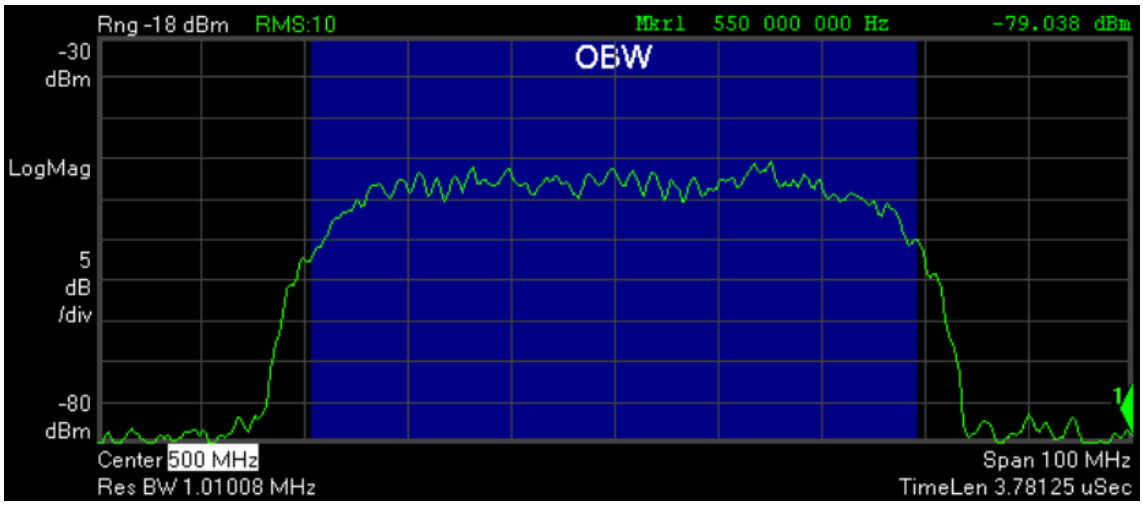


Figure 2.25 Rx SNR performance

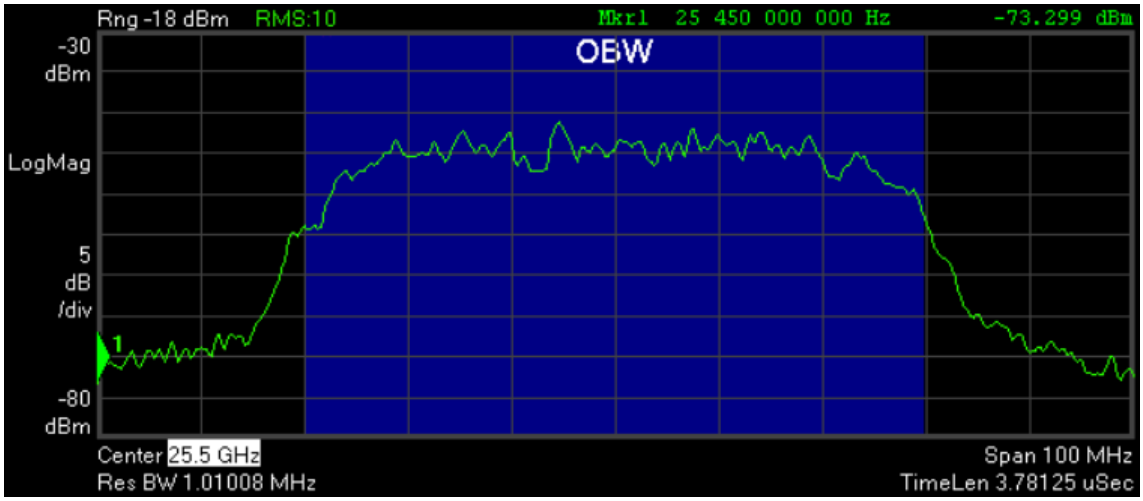


Figure 2.26 Tx SNR performance

that when the bit rate doubles, the required SNR correspondingly increases by 3dB, as illustrated in Table 2.1. As depicted in Fig. 2.25, the Rx possesses an SNR higher than 22.5dB, thereby making the 64-QAM an appropriate modulation scheme choice. The number preceding the QAM term signifies the number of bits transmitted per cycle, relating to the base 2 logarithm, as shown in equation (2.1).

$$QAM_{type} = 2^{Number of Bits} \tag{2.1}$$

The Tx module, on the other hand, achieved a data rate of 300 Mbps with the same 50 Mbaud signal across various carrier frequencies. An input power of -10 dBm was applied; since the gain of the Tx module is approximately 25.5 dB, the module operates close to the non-linear region, leading to an EVM value degradation compared

Table 2.1 Minimum Required SNR Values for Various Modulation Types

Modulation Type	Required SNR (dB)
BPSK	6.8
QPSK	9.8
16-QAM	16.5
64-QAM	22.5
256-QAM	28.5

to the Rx. Further degradation of the Tx is attributed to the high LO power on a very proximate LO frequency. This effect could be nullified by incorporating an additional mixer or upconverting a higher frequency IF signal.

The SNR, also referred as the Modulation Error Ratio (MER), of the Rx module, is 27.22 dB at the center frequency, while the SNR MER of the Tx module is 15.08 dB. Fig. 2.25 and Fig. 2.26 display the bandwidth of the corresponding signal at the center frequencies.

2.4 Conclusion

The 4x1 MIMO chips were implemented in tandem with the HMC 292 down/upconverter mixer to assess the comprehensive system performance. The input and output return losses were evaluated at RF frequencies, along with power measurements at both IF and RF frequencies. The Rx system downconverted the 24-28 GHz signal to 500 MHz, while the Tx system upconverted the 500 MHz signal to 24-28 GHz. EVM measurements were conducted with various LO frequencies, and data rates of 300 MBPS were achieved using a 64-QAM modulation technique with a 50 MHz bandwidth. The optimal performance in EVM measurements for the Rx was observed to be 2.83 % at the center frequency. On the other hand, the Tx exhibited its best performance at 5.28 % at 24 GHz.

3. LOW NOISE AMPLIFIER FOR 5G APPLICATIONS IN Ka BAND

3.1 Introduction

In this chapter, three distinct LNAs operating in the Ka-band are introduced. The discussion begins with LNA requirements and design procedures. Then a comparative analysis of the technology used for the first LNA and the LNA that is used in Rx MIMO is discussed. The first LNA is fabricated using a 130nm SiGe BiCMOS Cu technology, while the following two LNAs are designed using 130nm SOI CMOS technology. The performance characteristics and techniques employed for these two LNAs are then discussed in detail.

3.2 Low Noise Amplifier General Considerations

Low Noise Amplifiers are the initial blocks of the receiver chains. Their main purpose is to amplify the signal received from the antenna while minimizing noise contribution as much as possible. Given that the LNA is the first block in the chain, its noise directly influences the receiver chain, as demonstrated by the Friis equation in (3.1) (Pozar, 2011). The noise contributions from subsequent blocks will be divided by the gain of the previous stages. Therefore, the gain of the LNA should be sufficient to suppress the noise contribution from the subsequent stages. As noted in the previous chapter, for high data rate communication, the SNR of the total system should exceed certain thresholds to use different modulation schemes. A high-performance LNA can greatly improve this ratio by suppressing noise and pro-

viding gain. Notably, the gain provided by the LNA serves dual purposes. Besides suppressing the noise of subsequent stages, it also enables data transfer over longer distances, as outlined in the path loss equation (1.1).

$$F^T = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... \tag{3.1}$$

Linearity is another significant requirement for LNAs. Ideally, an amplifier should linearly amplify the input signals; however, due to the inherent nonlinearity of a transistor, this is not always achievable. The relationship between the input and output of a system, when a signal cosωt is applied, is outlined in equation (3.2). Every component of this equation represents the harmonics of the system.

Expanding the input-output relation using the Taylor series (as presented in Eq. (3.3)), the point at which the second term of this equation is compressed by 1dB (i.e., A is decreased by 1 in the dB scale) is defined as the 1dB compression point (IP1dB). This concept is mathematically represented in equation (3.4).

The linearity performance of a system can also be observed by applying two closely spaced tones to the system, making the input A_1cosω_1t+A_2cosω_2t. The second harmonics of these two tones will fall far beyond the fundamental frequency in the spectrum, as they will be ω_1+ω_2. In contrast, the third harmonic frequencies, derived from 2ω_1-ω_2 and 2ω_2-ω_1, will lie very close to the fundamental tones.

At low power levels, the third-order harmonics can be tolerated, as their amplitude is significantly smaller. However, at higher input power levels, the power of the third harmonics can match the fundamental signal's power, thus significantly disrupting the desired signal. The point at which the third harmonics become equal to the fundamental frequencies is referred to as the third-order intermodulation intercept point ((IIP3). From equation (3.4), it is evident that IP1dB and the IIP3 points are related, with the typical difference between them being approximately 9 dB.

That is why the LNA should be capable of linearly amplifying the input signal, even at higher power levels, and should be able to operate with interferers close to the frequency of interest. This phenomenon is particularly crucial for large bandwidth applications, as many interferers originate from adjacent channels (Razavi, 1998).

$$y(t) = \alpha_1 A cos\omega * t + \alpha_2 A^2 cos^2\omega * t + \alpha_3 A^3 cos^3\omega * t + ... \tag{3.2}$$

$$y(t) = \frac{\alpha_2 A^2}{2} + (\alpha_1 A + \frac{3 * \alpha_3 A^3}{4}) cos\omega * t + \frac{\alpha_2 A^2}{2} * cos2\omega * t + \frac{3 * \alpha_3 A^3}{4} * cos3\omega * t \tag{3.3}$$

$$A_{in,1dB} = \sqrt{0.145 * \frac{\alpha_1}{\alpha_3}} \tag{3.4}$$

The significance of input matching in LNAs cannot be overstated. In most cases, the input impedance is matched to 50 Ω to facilitate maximum power transfer. However, in LNAs, noise matching bears equal importance to power matching. Thus, during the design process, initial attention is paid to determining appropriate sizes to enable simultaneous matching of noise and power. Following this, the base/gate voltage of the input transistor is adjusted to minimize the Minimum Noise Figure (NFmin) as much as possible.

Several topologies can be employed in LNA design, each with its own set of trade-offs. For instance, the common emitter/source (CE/CS) topology can yield an impressively low noise performance, but with a moderate gain performance. The cascode LNA, which encompasses both CE/CS and common base/gate (CB/CG) topologies, can reach higher gain levels. Furthermore, since the input and output terminals of the amplifier are not directly interconnected via C_{GD} or C_{BC} junction capacitors, the amplifier's stability is enhanced. Nevertheless, the inclusion of an additional transistor increases the system's noise performance (Allstot, Li & Shekhar, 2004).

3.3 Cascode LNA in 0.13 μm SiGe BiCMOS Copper technology

3.3.1 Design and Analysis

The design process commences with the setting of sizes and bias voltages, followed by input matching, achieved using the series base inductor and the degeneration inductor. As these two components are sufficient enough for the input matching network, the transistor is biased through a 10 kΩ resistor and a bypass capacitor.

Given that the design necessitates a gain higher than 10dB, the cascode topology emerges as an appropriate choice. A two-stage network could have been a potential alternative, but it would increase noise due to the loading effect on the first stage's output and the additional noise contribution from the Friis equation (3.1).

The bias voltages of the CB stage are significantly important for determining the corresponding collector current, in other words, the system's power consumption. They are also crucial for establishing the transconductance (gm) of the CE transistor, and consequently, the system's linearity. Once noise and power matching are achieved and the desired current is determined, the output matching network is designed to attain a gain greater than 10 dB. This involves the use of a collector resistor, inductor, and output capacitor. These passive components alter the amplifier's gain while matching the output impedance of the stage to 50 Ω. The schematic of the total circuit is given in Fig. 3.1.

After settling on the main components of the design, the next phase is to devise the bias networks. Figure 3.1 presents the circuit diagram of the bias networks. The advantage of this biasing technique lies in its minimization of the current flowing to the base of the main transistors. Given that the bias node is connected to the base and the emitter of the npn transistors, the current of this net is a combination of both. As the base-emitter voltage (V_{BE}) saturates at 0.7V, the bias voltages will be minimized while ensuring that the current contribution to the main circuit remains insignificant.

As previously mentioned, noise is one of the most crucial parameters in communication links. The SNR plays a key role in enhancing data transfer and increasing the number of data bits sent per cycle. Consequently, the NF of the LNA should be as low as possible. Among the various components, the base inductor stands out as the most significant contributor to noise. The noise contribution of the base inductor increases as its quality factor diminishes. The quality factor is indicative of a component's efficiency, with a lower quality factor denoting greater loss. Certain parameters, such as geometry, parasitic capacitances, and the conductance of the material used, determine an inductor's quality factor.

The technology used in the MIMO chips was 0.13 μm SiGe BiCMOS. To investigate if the SNR of the entire system could be boosted by employing 0.13 μm SiGe BiCMOS Cu technology, this LNA was designed with the aforementioned technology. The conductance of the top aluminum metals in 0.13 μm SiGe BiCMOS is 30300000 S/m and 27800000 S/m respectively, while the conductance of both top copper metals in 0.13 μm SiGe BiCMOS Cu is 52083000 S/m Considering that these metal layers are the most conductive amongst all the other layers, they are primarily

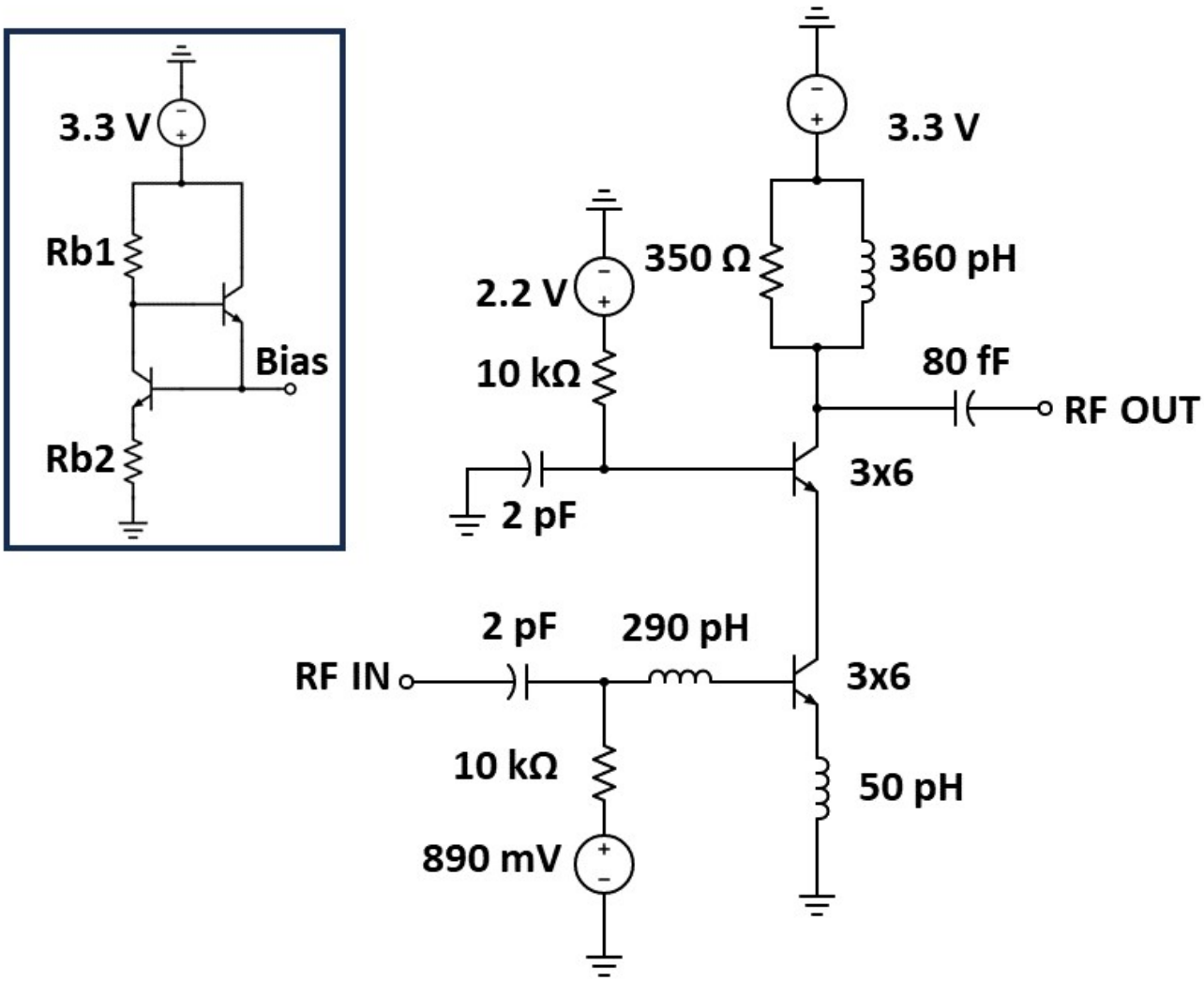
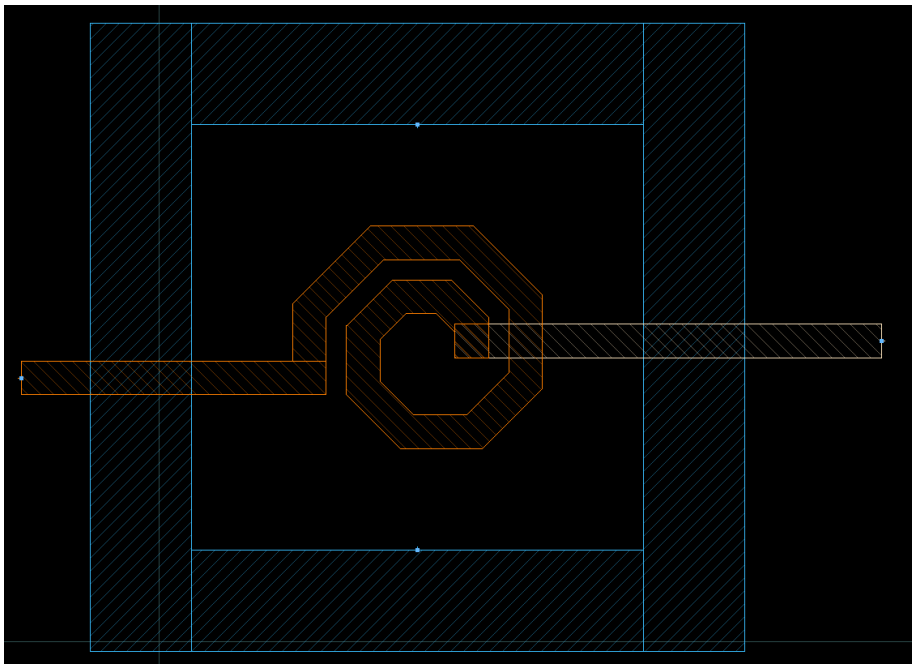
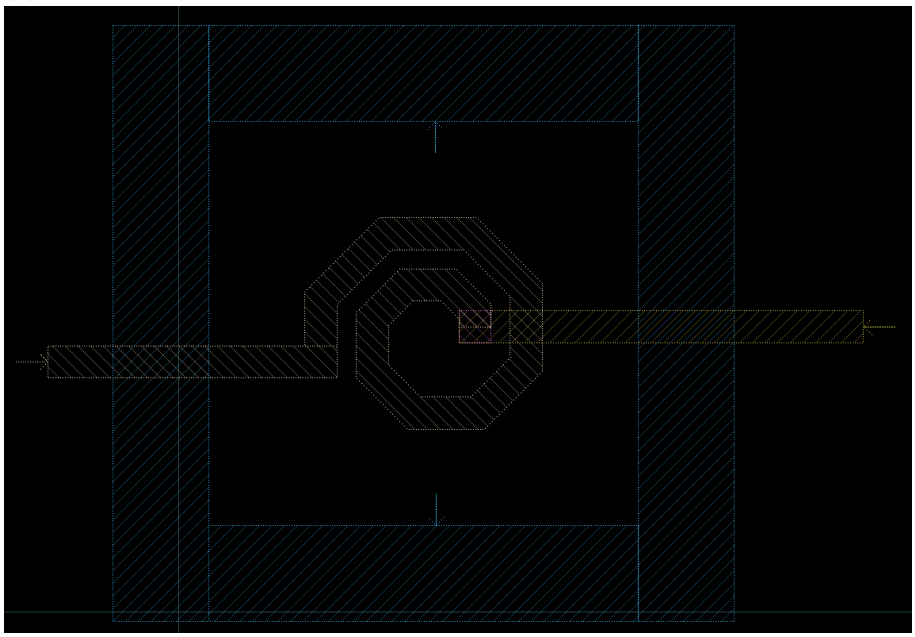


Figure 3.1 Schematic of the cascode LNA



(a)



(b)

Figure 3.2 The geometric shapes of the inductors in 2 different technologies (a) 130nm SiGe BiCMOS (b) 130nm SiGe BiCMOS Cu

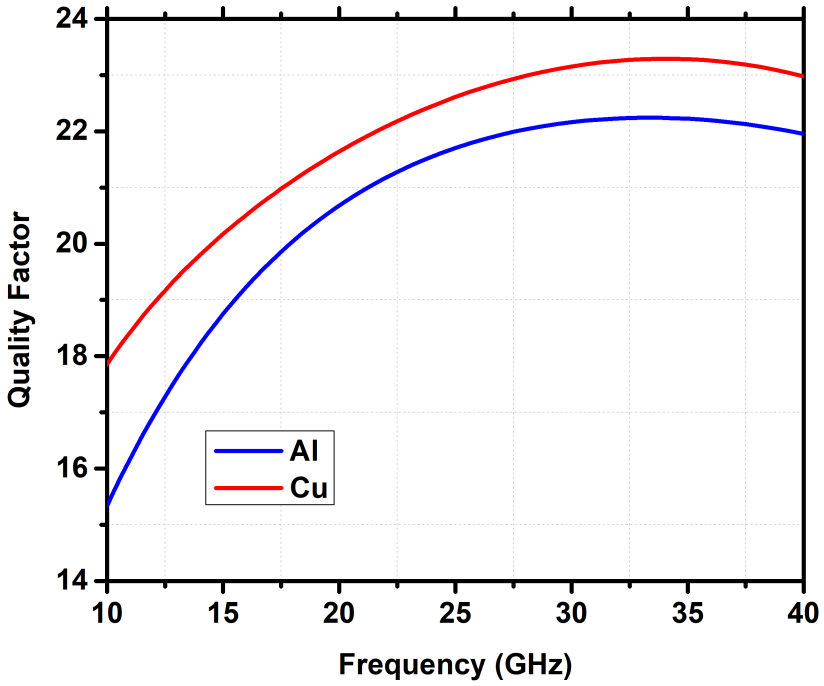


Figure 3.3 The quality factors differences between 130nm SiGe BiCMOS and 130nm SiGe BiCMOS Cu.

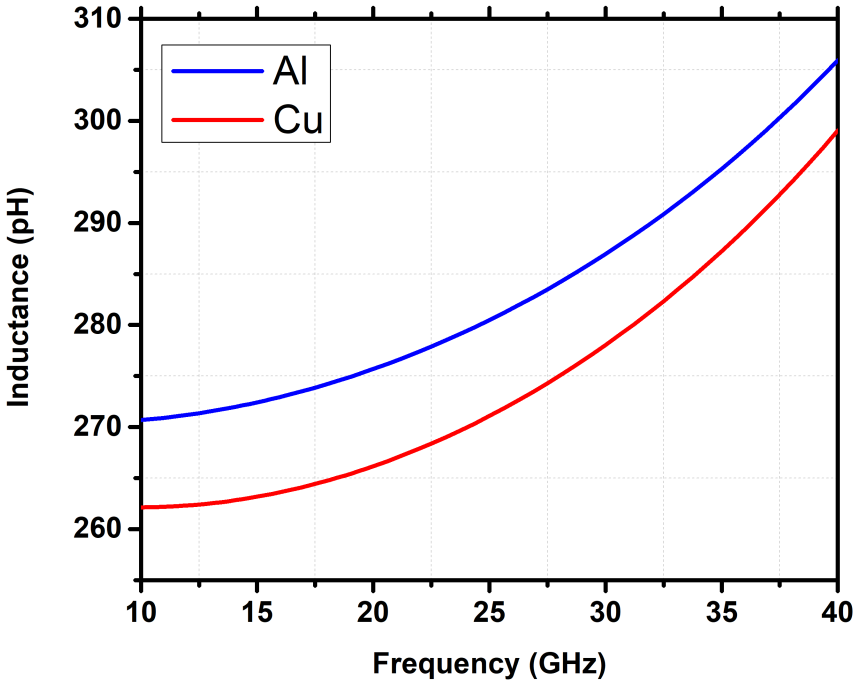


Figure 3.4 The inductance differences between 130nm SiGe BiCMOS and 130nm SiGe BiCMOS Cu.

used in inductor design. As a result, the inductor geometries were assessed using these two technologies in order to determine their corresponding quality factors and inductance values. Since the lower layers are identical for these two technologies, and they possess similar geometric structures, their corresponding capacitances will be approximately equivalent. The geometries are depicted in Figure 3.2, the quality factors in Figure 3.3, and the corresponding inductance values in Figure 3.4.

3.3.2 Measurement Results

The photograph of the designed die is illustrated in Fig. 3.5, occupying an area of 0.198 mm^2 (0.385x0.515), exclusive of the pads. The S-parameter measurement spanned from 10GHz to 40GHz, employing Cascade Microtech 40 GHz GSG probes in tandem with the Keysight N5224A PNA Network Analyzer. The network analyzer was initially calibrated within the range of 10-40 GHz, and the corresponding measurement setup is depicted in Fig. 3.6.

Both simulated and measured return loss performances are displayed in Fig. 3.7. Due to the parasitic capacitances associated with the pads, the input is shifted downwards on the Smith chart, a phenomenon also observable for the output. However, due to the more inductive positioning of S22, the parasitic capacitances only shifted its peak point. As expected, the design exhibited no signs of instability, indicative of the advantageous input-output isolation provided by the cascode topology.

The amplifier's gain performance showed enhancement in comparison to the simulation results. This is attributed to the increase in the observed supply current, which was expected to be 9.8 mA but measured at approximately 11.3 mA, thereby increasing the corresponding gm value of the CE amplifier. As indicated in Fig. 3.8, the LNA's measured peak gain is 13.62 dB at 24 GHz, compared to the simulated peak gain of 12.4 dB, signifying a 1 dB increase in total gain. Nonetheless, the 3 dB bandwidth remained constant at 18-33 GHz for both simulation and measured results.

The setup for the IP1dB measurement is depicted in Fig. 3.9. Initial steps involve applying varying levels of input power from the E8257D PSG Analog Signal Generator to the chip, facilitated by RF cables and Cascade Microtech 40 GHz GSG probes. Subsequently, the output is captured using the Keysight E4448A PSA Series Spectrum Analyzer. To ascertain IP1dB values for various frequencies, different input powers were applied across the band of interest.

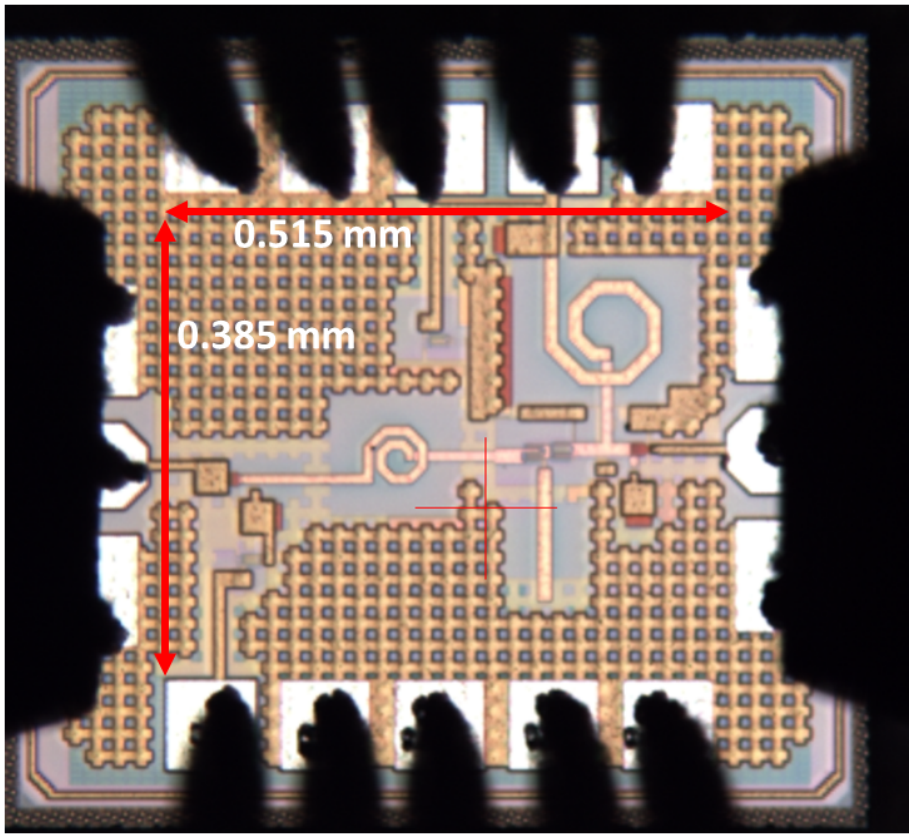


Figure 3.5 The die photograph of the cascode LNA in 130nm SiGe BiCMOS Cu.

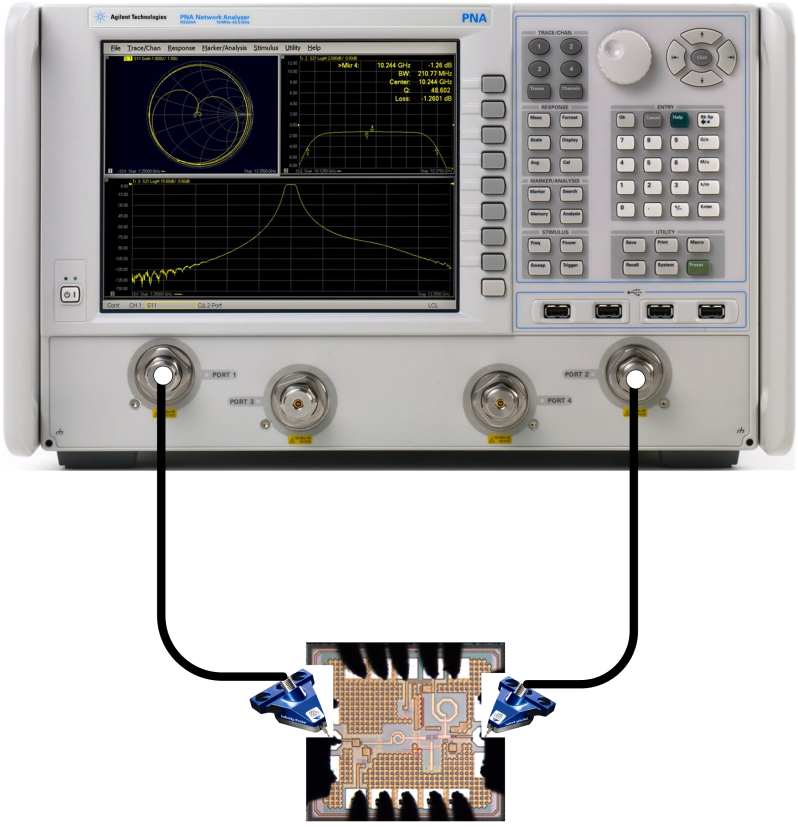


Figure 3.6 The s-parameter measurement setup of the cascode LNA in 130nm SiGe BiCMOS Cu.

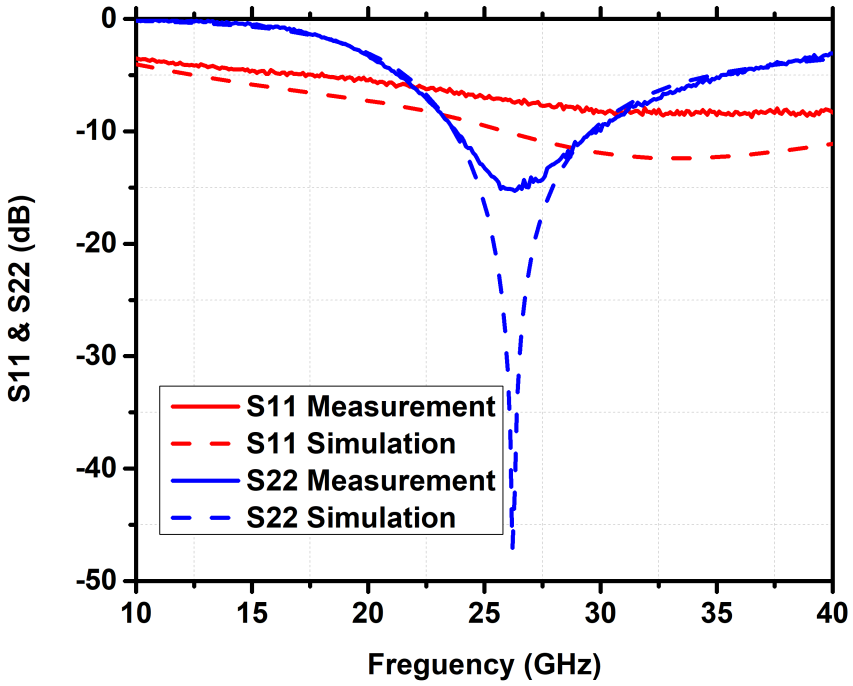


Figure 3.7 The measured and simulated return losses of the cascode LNA in 130nm SiGe BiCMOS Cu.

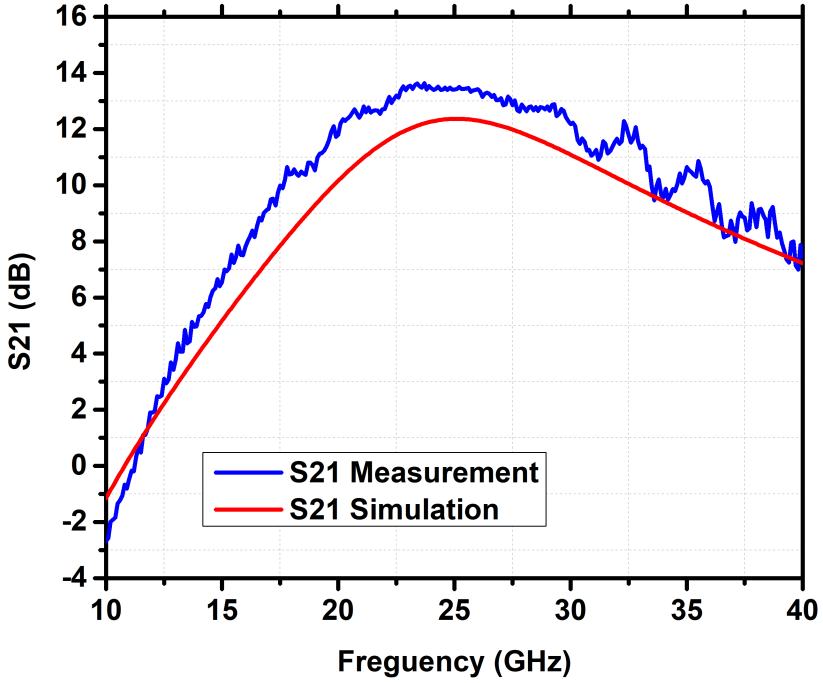


Figure 3.8 The measured and simulated gain of the cascode LNA in 130nm SiGe BiCMOS Cu.

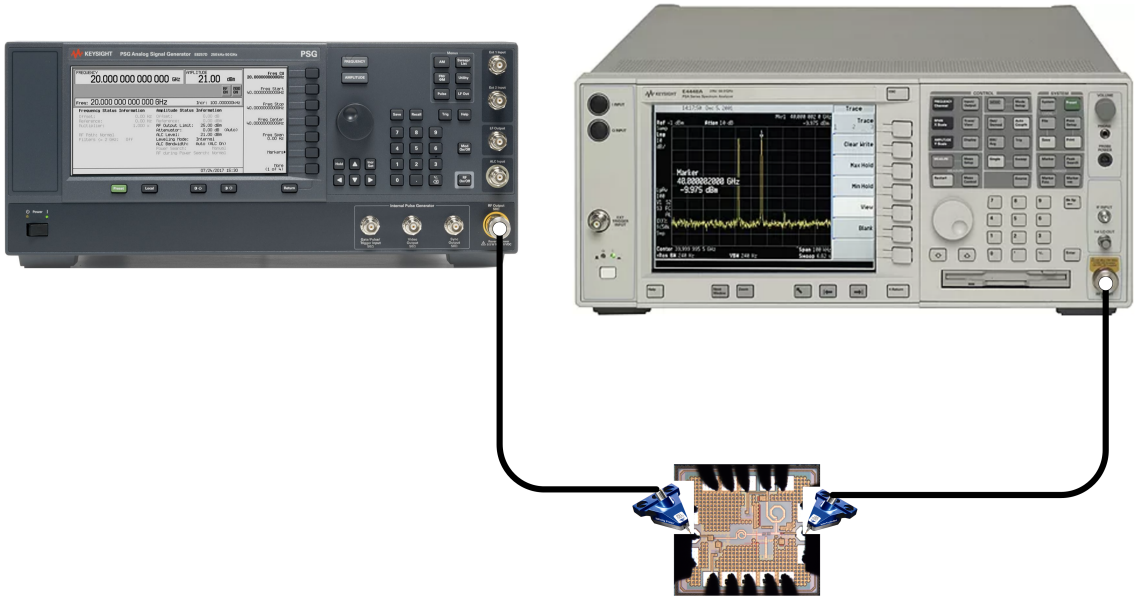


Figure 3.9 The measured and simulated IP1dB measurement setup of the cascode LNA.

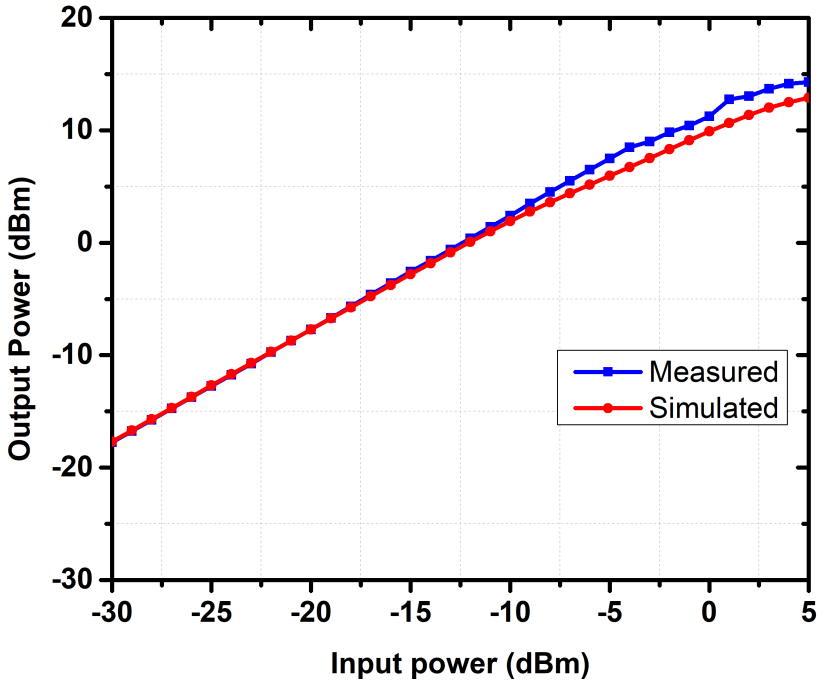


Figure 3.10 Measured and simulated output power levels of the cascode LNA in different input powers.

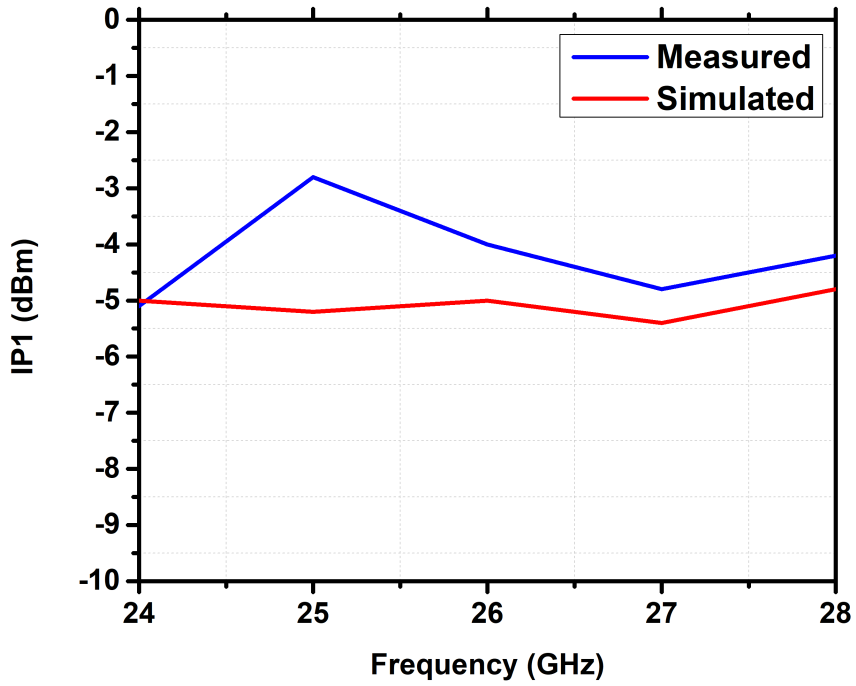


Figure 3.11 The measured and simulated IP1dB of the cascode LNA in different frequencies in the band of interest.

Fig. 3.10 illustrates the input and output powers of the LNA at the center frequency (26 GHz). The measured results align closely with the simulated results; however, an increase in the system's current shifts the IP1dB towards higher input levels. This process was reiterated for other frequencies, with the resultant data presented in Fig. 3.11.

An analysis of Fig. 3.11 reveals approximately a 2 dB discrepancy between the simulated and measured results. This considerable difference is attributed to soft compression around the -5 dBm power level, whereby a 1.5 mA variation increases the IP1dB point by approximately 2 dB.

The setup for the IIP3 measurements is presented in Fig. 3.12. Two tones were utilized for the experiment, with a spacing of 10 MHz between them. At the center frequency measurements, a 27.005 GHz signal was applied from the E8257D PSG Analog Signal Generator, while a complementary signal of 26.995 GHz was produced using the Keysight N5224A PNA Network Analyzer. These two tones were subsequently combined with the aid of a coupler before being fed into the LNA. The resultant output was captured and analyzed using the Keysight E4448A PSA Series Spectrum Analyzer. The measurement results for both the OIP3 and IIP3 performances of the LNA are presented in Fig. 3.13. Given that the peak gain of

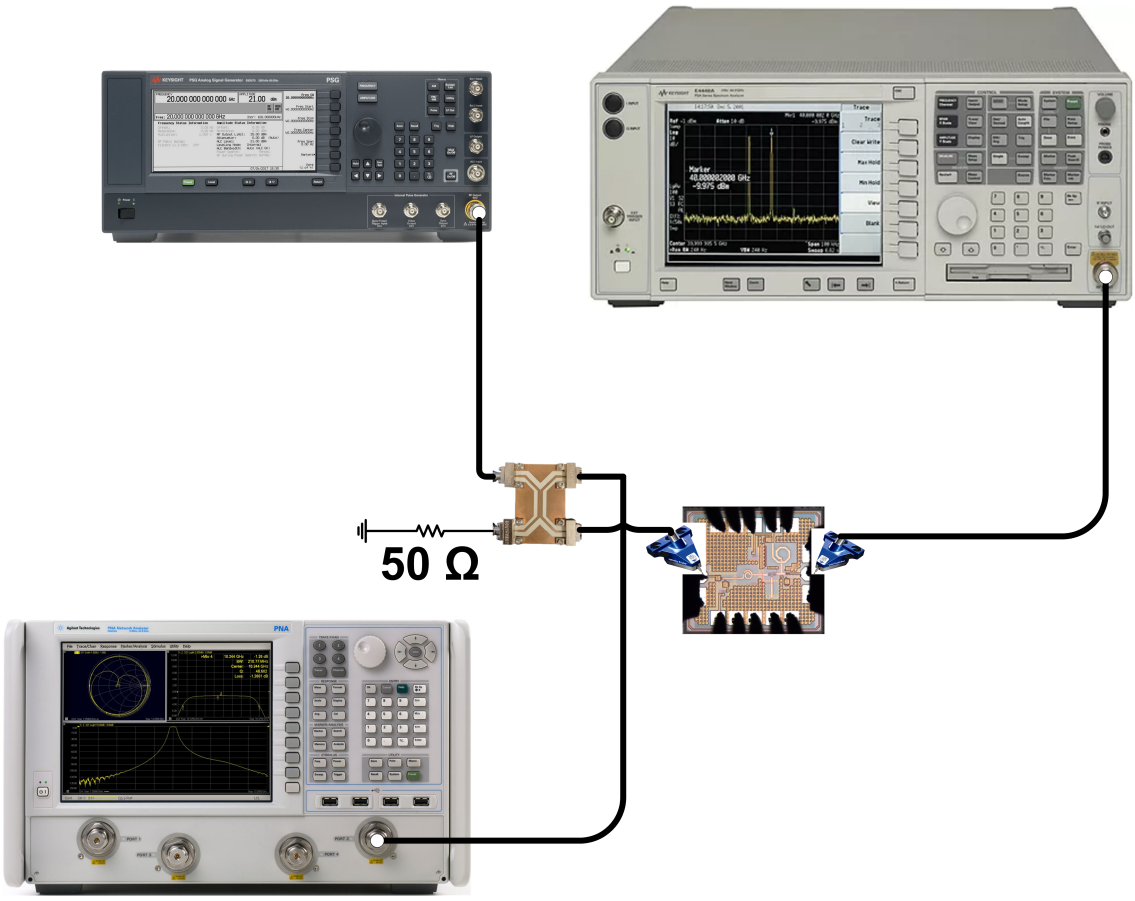


Figure 3.12 The measured and simulated IP1dB measurement setup of the cascode LNA.

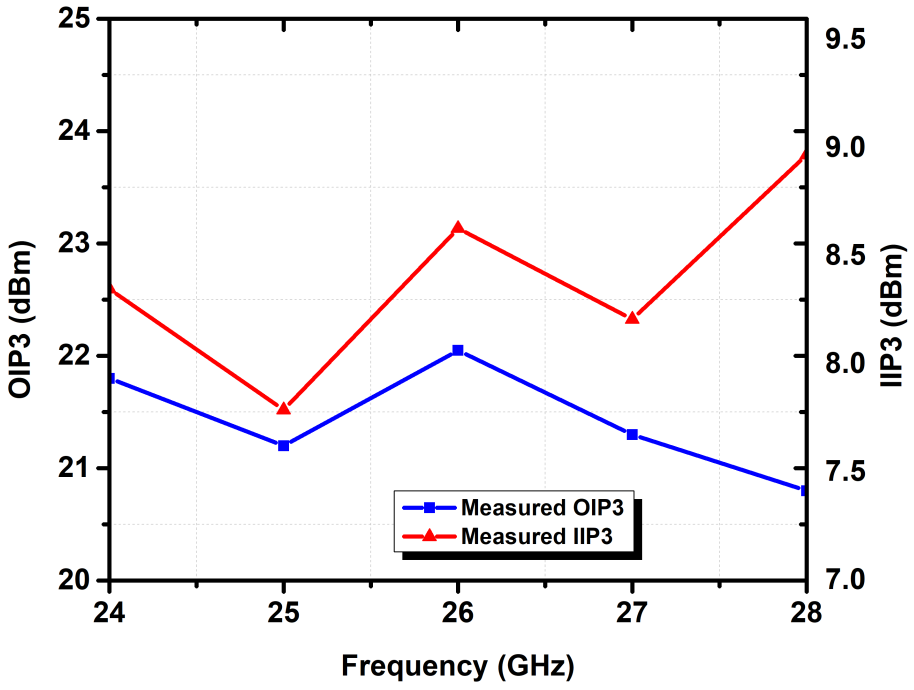


Figure 3.13 The measured OIP3 and IIP3 of the cascode LNA

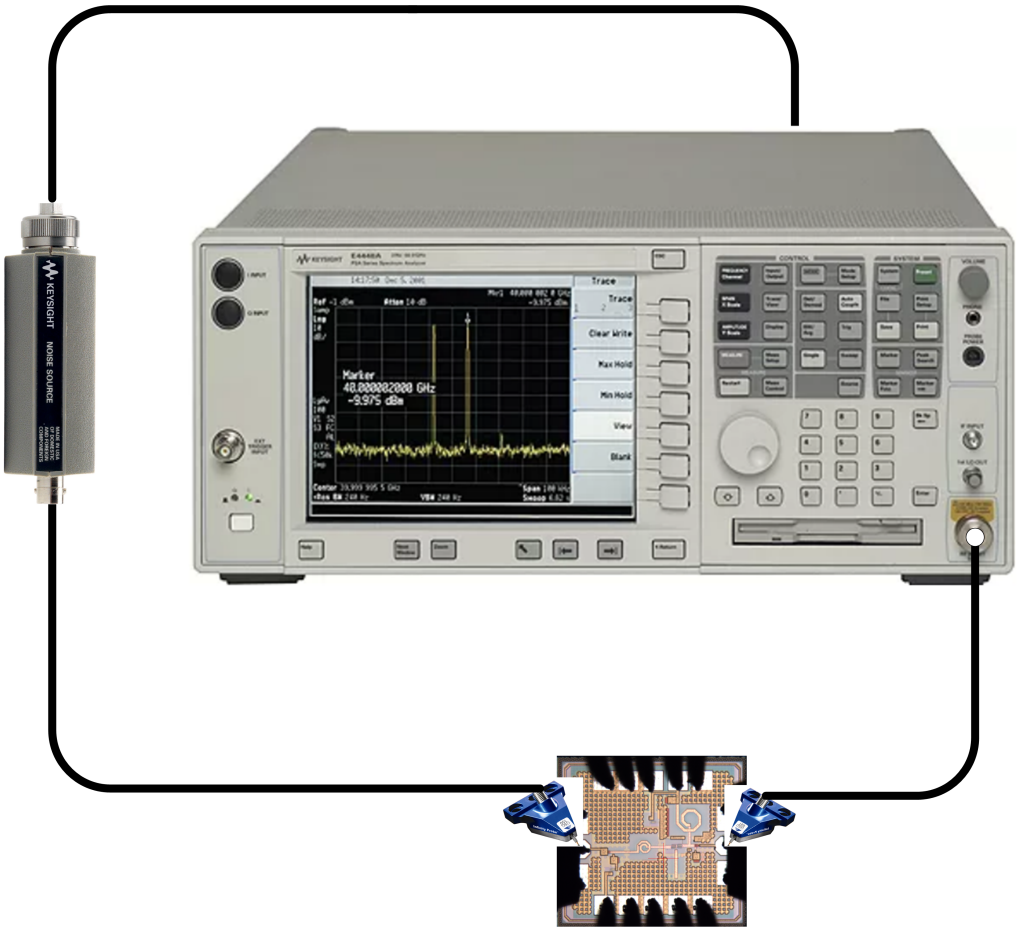


Figure 3.14 The NF measurement setup of the cascode LNA.

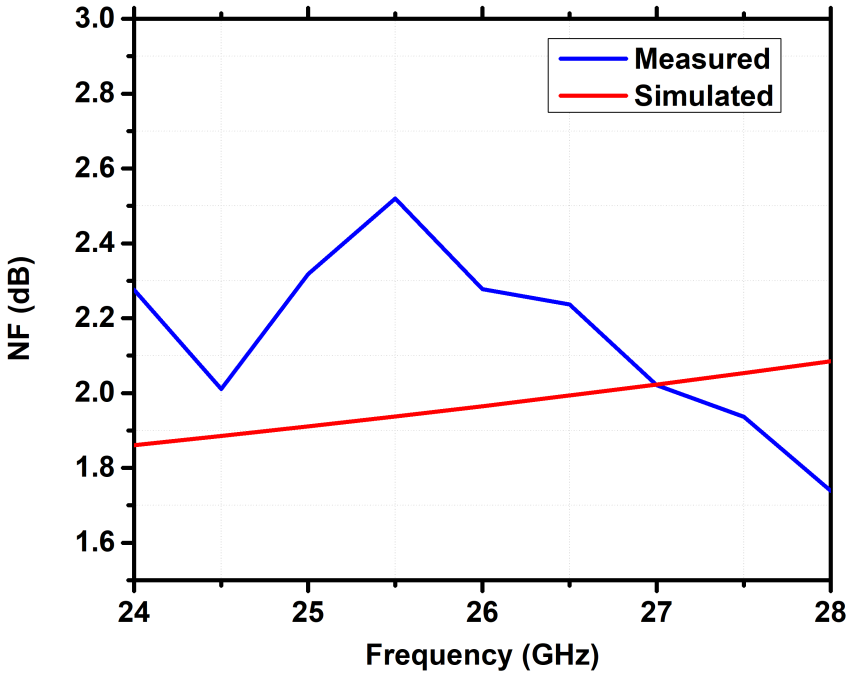


Figure 3.15 The simulated and measured results of the cascode LNA.

the LNA is 13.4dB and experiences a decline as frequency increases, the design's IIP3 is highest at 28 GHz with a measure of 8.8 dBm. Correspondingly, the peak OIP3 is observed at 26 GHz with 22 dBm.

The setup for the NF measurement of the LNA is delineated in Fig. 3.14. Initially, the noise source Keysight 346CK01 is calibrated in conjunction with the Keysight E4448A PSA Series Spectrum Analyzer. Subsequently, this calibrated NF source is connected to the input of the amplifier, and the resultant outputs are collected using the Keysight E4448A PSA Series Spectrum Analyzer. To ascertain the noise associated with the die devoid of cable losses, equation (3.1) is employed.

The simulated and measured NF performances of the LNA are presented in Fig. 3.15. The NF is observed worst at 25.5 GHz with 2.52 dB and best at 28 GHz with 1.73 dB. The NF is increased for lower frequency levels due to the input return loss shifting due to the capacitive effects of the pads.

3.3.3 Comparison

The comparison table for different LNAs in literature with the center frequency around 26 GHz (Adabi, Heydari, Bohsali & Niknejad, 2007; Burak, Altintas, Yazici & Gurbuz, 2021; Elkholy, Shakib, Dunworth, Aparin & Entesari, 2018; Gurol, 2022; Issakov & Ciocoveanu, 2019) has presented in Table 3.1. Designs are compared with different Figure Of Merits (FoM) values. The FoM_1 given in equation (3.5) is comparing IP1dB with the other fundamental parameters of the LNA. whereas the FoM_2 given in (3.6) compares IIP3 of the designs.

$$FoM_1 = \frac{G[abs] * IP1dB[mW] * BW[MHz]}{(F_{min} - 1) * P_{DC}[mW]} \tag{3.5}$$

$$FoM_2 = \frac{G[abs] * IIP3[mW] * BW[MHz]}{(F_{min} - 1) * P_{DC}[mW]} \tag{3.6}$$

The designed system significantly outperforms numerous other designs documented in the existing literature, as evidenced by the FoM performances presented in Table 3.1. However, the input return losses of the design are somewhat restricted due to the capacitive effects of the pads, thereby limiting the LNA's bandwidth. Notably,

the study by (Issakov & Ciocoveanu, 2019) exhibits superior performance in terms of FoM_1, which can be attributed to the implementation of an exceedingly low-power design coupled with a wide bandwidth. The 130nm SiGe BiCMOS Cu technology has improved the noise performance compared to conventional 130nm SiGe BiCMOS technology. However, the power consumption has increased as a trade-off to achieve higher linearity performance.

Table 3.1 The performances of the LNA in the literature

References	**(Adabi et al., 2007)**	**(Elkholy et al., 2018)**	**(Burak et al., 2021)**	**(Issakov & Ciocoveanu, 2019)**	**(Gurol, 2022)**	**This Work**
Technology	90 nm CMOS	40 nm Bulk-CMOS	0.13μm SiGe BiCMOS	45 nm SOI CMOS	0.13μm SOI CMOS	**0.13μm SiGe BiCMOS Cu**
Frequency (GHz)	30	28	26	20.5	24	**26**
Gain (dB)	27.1	20	12.8	10.5	12.9	**13.5**
Area (mm^2)	0.26	0.63	0.23	0.18	0.61	**0.198**
P_{DC} **(mW)**	31.6	16.25	5.4	6	32.67	**37.29**
IP1dB (dBm)	-21.6	-17	-10.5	-10.3	-10	**-4**
IIP3 (dBm)	-12.6	-7.5	1	-0.3	1	**8.8**
NF_{min} **(dB)**	3.3	2.9	2.08	1.4	2.7	**1.73**
FoM_1 **(MHz)**	730	336	1023	5505	623	**1967**
FoM_2 **(MHz)**	5799	2995	14461	55056	7844	**31180**

3.4 Common Source LNA in 0.13μm SOI CMOS technology

3.4.1 Design Analysis

The following section discusses the design of two LNAs using a 0.13 μm SOI CMOS technology. The primary objectives of an LNA design include achieving low NF to increase the SNR of the receiver chain and ensuring system linearity. The previous LNA has been implemented in a SiGe BiCMOS Cu technology to investigate whether it's possible to further improve the SNR of the MIMO system discussed in Chapter 2. This is of significant importance due to the critical role the SNR plays in the performance of any communication system.

The other crucial aspect of LNAs that this excerpt emphasizes is the linearity of the systems. In wideband applications, numerous interference tones can significantly degrade data transfer. Therefore, the LNAs designed using 0.13 μm SOI CMOS technology aim to achieve high linearity along with a good NF performance.

The IIP3 and IP1dB values of the amplifiers are determined through gain subtraction of the OP1dB and OIP3 values. It's critical to maintain a flat gain across the wideband frequency band. Achieving flat gain means that the IIP3 values will be relatively similar across a broad frequency range, improving the linearity and, consequently, the performance of the amplifier across its operating bandwidth.

This segment describes the specific design requirements for an LNA using a two-stage approach. The design aims to achieve a gain higher than 15dB in the frequency range of 24-30 GHz, with an emphasis on maintaining flatness in the frequency of interest. In addition to this, the design strives for an NF lower than 2dB, an IIP3 higher than -5 dBm, and an IP1dB higher than -15 dBm.

In order to achieve gain flatness across the frequency of interest, a technique known as 'gain staggering' is used. The principle of this method is depicted in Fig. 3.16. Essentially, the gain of the first stage is designed to be high at lower frequencies, while the second stage's gain is high at higher frequencies. When these two stages are cascaded, the resulting system achieves a flat gain across a broad bandwidth, which helps maintain consistent performance across the frequency range.

However, for this technique to work, the LNA needs to have at least two stages, each

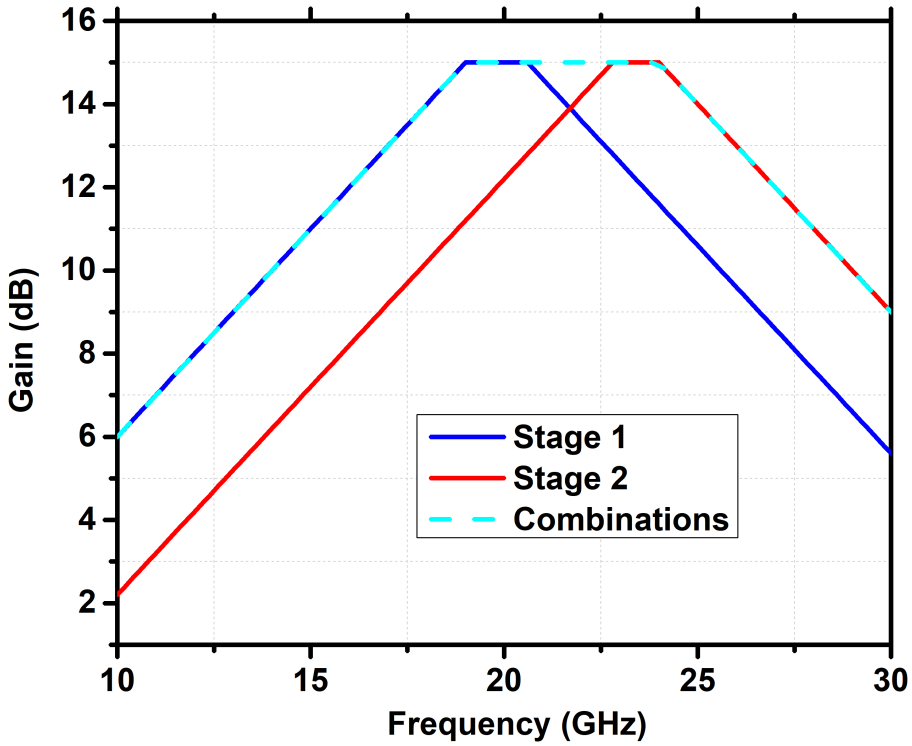


Figure 3.16 Gain staggering working principle

introducing a certain level of noise. To minimize the noise contribution, especially from the second stage which could otherwise lead to an NF higher than 2dB, both stages are designed using the CS configuration. This layout is popular for its beneficial noise characteristics, thereby ensuring the minimum possible noise contribution from both stages.

In the design of the first stage of the LNA, several aspects have to be considered. The bias voltage and the size of the transistor are determined simultaneously with noise and power matching, and by identifying the peak gain of the stage.

In the setup, a shunt inductor is used as an RF choke and a matching element. This is done in tandem with a source degeneration inductor and a gate inductor. The role of the gate inductor is significant in this context. It's designed to have a high quality factor as possible to reduce the noise contribution of the stage.

In addition, the source degeneration inductor plays a critical role in this design. The CS topology can suffer from output-to-input feedback via the drain-gate C_{DG} capacitor, which can lead to oscillations. By introducing a source degeneration inductor, negative feedback is provided to the system, thus increasing the overall stability of the amplifier. However, the inclusion of a source degeneration inductor also reduces

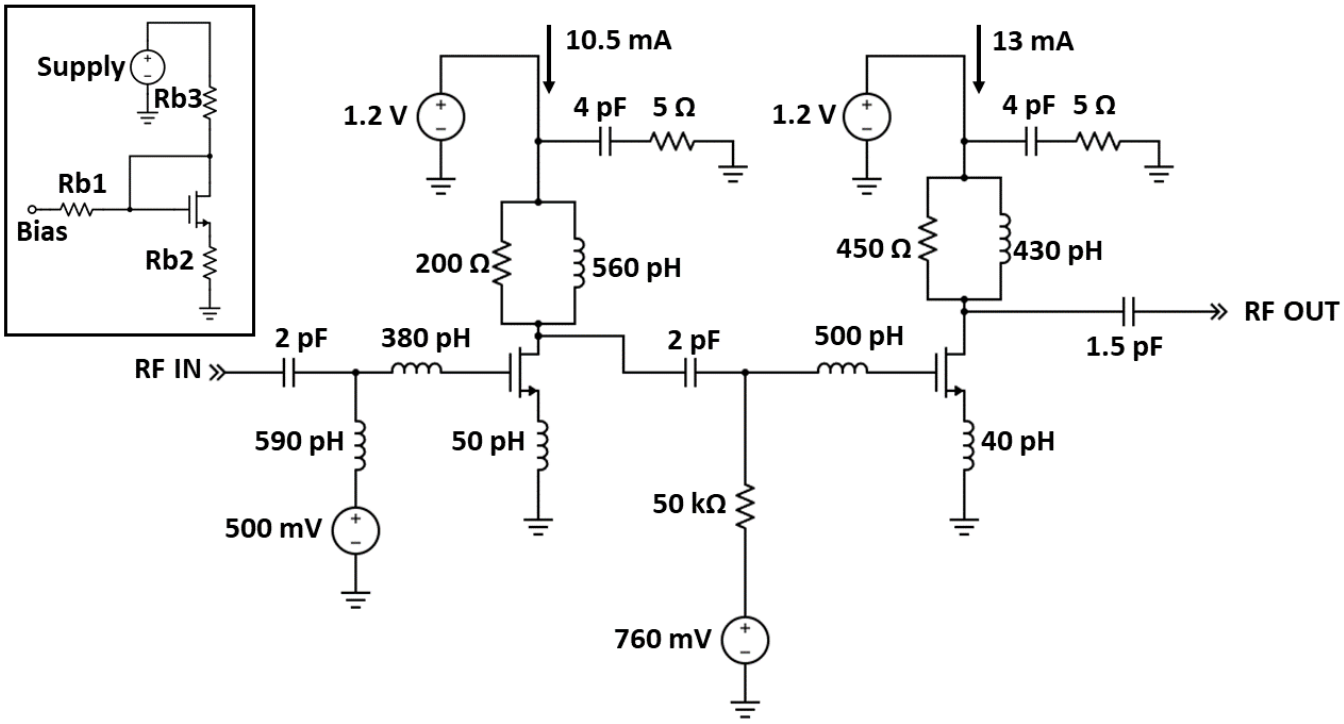


Figure 3.17 schematic of the proposed 0.13 μm SOI CMOS LNA.

the gain of the amplifier. Therefore, the value of this inductor is carefully optimized to balance both matching and gain. The first stage of the LNA is designed with a specific drain current of 10.5 mA. The transistor in this stage is designed with a width of 1 μm and comprises 54 fingers. To handle the current at the drain, a multiplier of 3 is used, resulting in 18 fingers per row.

The design of the first stage's output aims for a gain of around 8 dB. To achieve this, the drain inductor and resistor are designed to provide the required gain, and they also function as output-matching components alongside the DC block capacitor. It's important to note that the output of the first stage is not directly designed to match a 50 Ω impedance because, for maximum power transfer, conjugate matching is necessary.

Following the same principle, the input of the second stage is designed to obtain conjugate matching for the frequency of interest. This is achieved by designing the input impedance of the second stage to be the complex conjugate of the output impedance of the first stage at the desired frequency. This is done using a series gate inductor and a degeneration inductor at the source. This approach ensures optimal power transfer and gains across the LNA.

The bias voltage of the second stage is selected to maximize linearity, and the sizes of the transistor are chosen for peak voltage at 25 GHz. The selected transistor

sizes are 36 fingers with a width of 1 μm. For similar reasons as the first stage, the multiplier is selected as 2, which results in 18 fingers per row.

The passive components at the output are selected to achieve 50 Ω matching along with providing a gain of around 8 dB. The selected current for this stage is 13 mA. These design considerations help in achieving the desired specifications of gain, bandwidth, and linearity for the LNA. The used supply voltages are 1.2 V, therefore the corresponding power consumption is 28.2 mW. The schematic representation of the design is presented in Fig. 3.17. The 5 Ω resistor connected series to bypass capacitors in order to decrease the quality factors of the capacitors and increase the stability factor.

3.4.2 Applied Linearization

Various techniques for improving the IIP3 have been proposed in the literature. While they all operate on the same basic principle, their specific implementations can differ due to the unique trade-offs each method presents.

In essence, all these methods employ an auxiliary device to generate a third-order harmonic with a negative phase. This harmonic is then fed back into the main transistor. The effect of this is to suppress the third harmonic, as indicated by equation (3.7). However, the auxiliary transistor also generates its own fundamental frequencies, as shown in equation (3.8).

These fundamentals, when fed back into the main transistor, can degrade the overall gain of the system. Consequently, even if the magnitudes of the third-order harmonics of the auxiliary transistor and the main transistor are identical, the IIP3 cannot reach infinitely high values.

This is because the fundamental frequencies generated by the auxiliary transistor introduce an additional non-linearity to the system, which limits the improvement that can be achieved in the IIP3. In other words, the auxiliary transistor's contribution to the overall signal isn't just the third-order harmonic, but also the fundamental frequencies, which have the potential to degrade the overall performance.

This is a crucial consideration in system design, and achieving optimal IIP3 performance often requires careful balancing of these factors (Zhang & Sánchez-Sinencio, 2011).

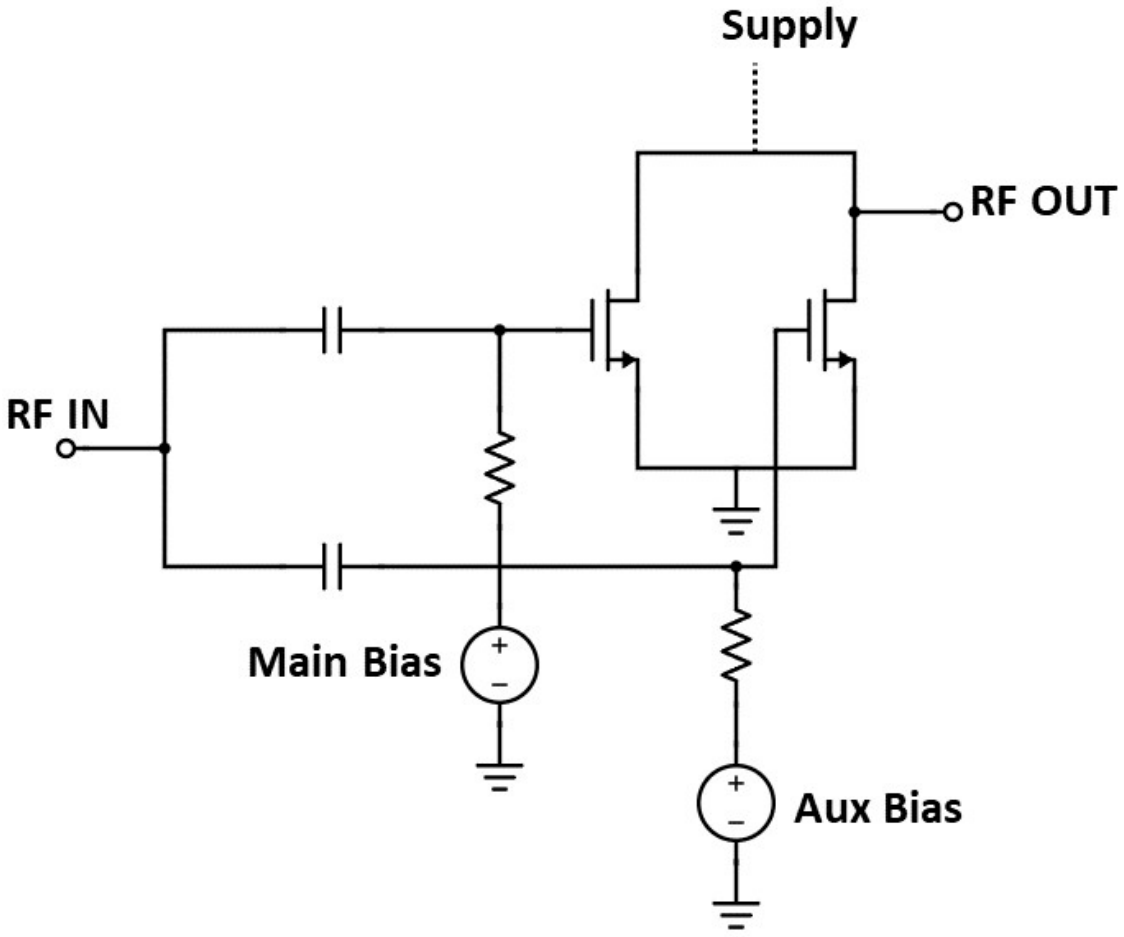


Figure 3.18 Basic demonstration of the derivative superposition

$$Y = Y_{main} - Y_{auxiliary} \tag{3.7}$$

$$Y_{auxiliary} = g_1 X + g_2 X^2 + g_3 X^3 \tag{3.8}$$

The possibility of optimally biasing the main transistor, without the use of any additional transistor, presents one method for third harmonic cancellation. However, the biasing point where optimal cancellation occurs is typically at substantially low voltage levels. Consequently, the amplification process may be significantly compromised (Aparin, Brown & Larson, 2004).

Another prevalent strategy involves the post-distortion method, which employs feedback from the amplifier's output nonlinearity to the main transistor. Numerous variations of this approach exist. For instance, (Yoon, An, Kang, Kim, Lee, Jang,

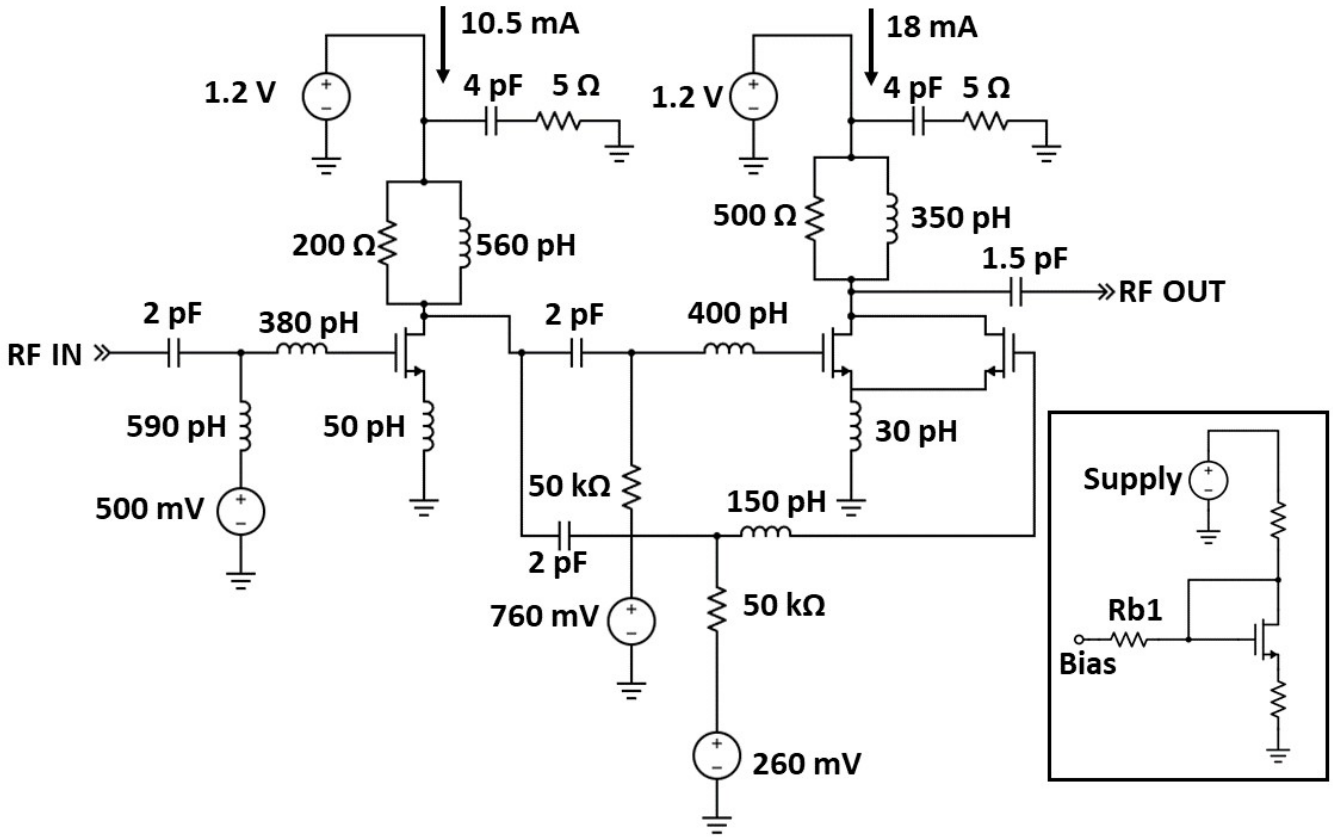


Figure 3.19 schematic of the proposed 0.13 μm SOI CMOS LNA with implemented DS.

Minn, Suh, Lee, Kim, Kim, Lee, Choi, Son & Yang, 2019) applies a diode-connected device to feed back the negative third harmonic, thus facilitating its cancellation. Another post-distortion method, (Kim, Aparin, Barnett & Persico, 2006) utilizes a cascode device at the output, feeding back to the main device. Such post-distortion methods predominantly employ feedback mechanisms.

In addition to these, the feedforward method constitutes an alternative for canceling the third-order harmonic. Rather than extracting the nonlinearity from the output and feeding it back into the system, it is plausible to extract it from the input, amplify it, and subsequently feed it to the output to achieve cancellation (Ding & Harjani, 2001).

A final strategy involves a distinctive type of feedforward technique which is called derivative superposition (DS). As illustrated in Fig. 3.18, this method connects an auxiliary transistor parallel to the main system, using a different bias voltage that optimally cancels the system's third-order harmonics (Xin & Sanchez-Sinencio, 2004)

The second die, designed using 0.13 μm SOI CMOS technology as well, employs a

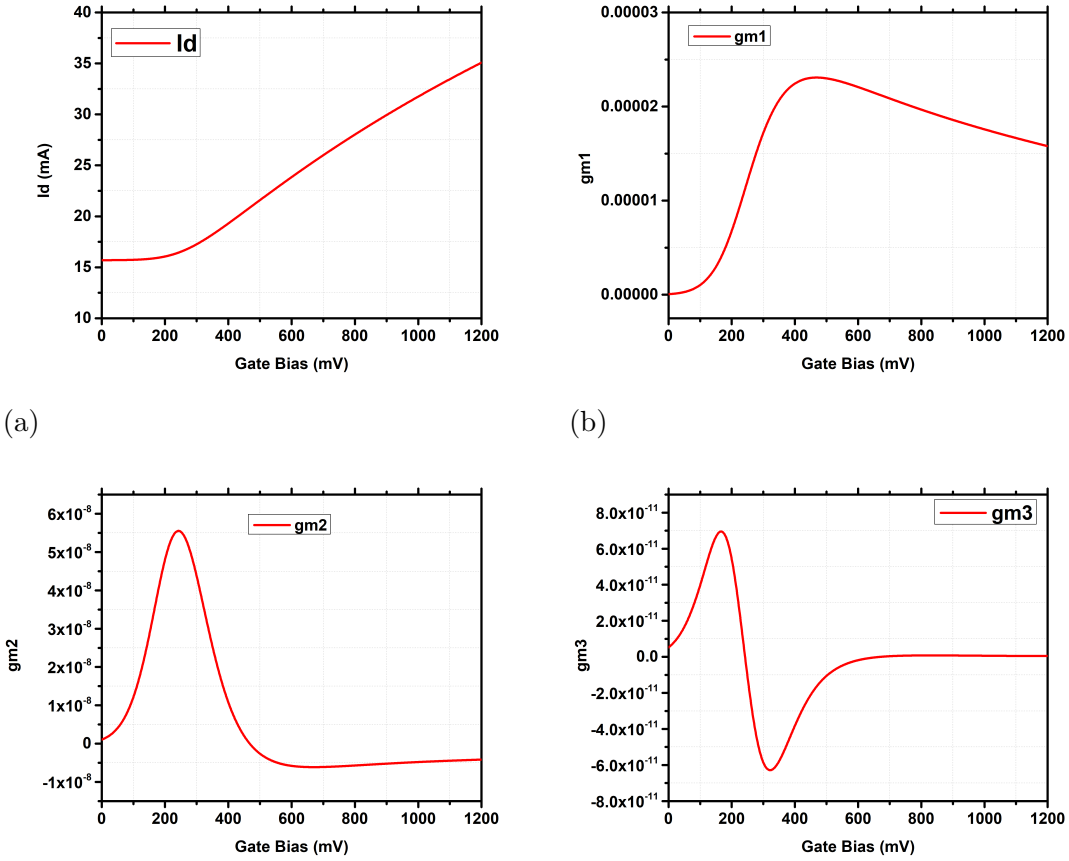


Figure 3.20 The derivative of the current to find the optimal bias point. (a) Id (b) gm1 (c) gm2 (d) gm3

DS method to enhance the linearity of the LNA. The auxiliary transistor is linked to the second stage of the amplifier. The proposed improved LNA with the DS linearization technique applied is presented in Fig. 3.19. The capacitive effect of the additional load to the first stage is shifting the conjugate matching of the first and second stages therefore additional 150 pH inductor is placed to the gate of the auxiliary device.

The bias points of the auxiliary stage are ascertained by computing the derivative of the drain current concerning the gate voltage of the auxiliary transistor, as depicted in Fig. 3.20. Since the third order cancellation is required third derivative is taken off the drain current. The bias point, where the third-order harmonic is approximately zero, is selected. However, it should be noted that this point tends to shift towards higher voltages following the layout process. Additionally, the sizes of the auxiliary transistor are meticulously swept to identify the optimal sizes that will both deliver superior linearity performance and minimal degradation of gain. The selected sizes are 5 fingers with 1 μm width and 3 multiplier.

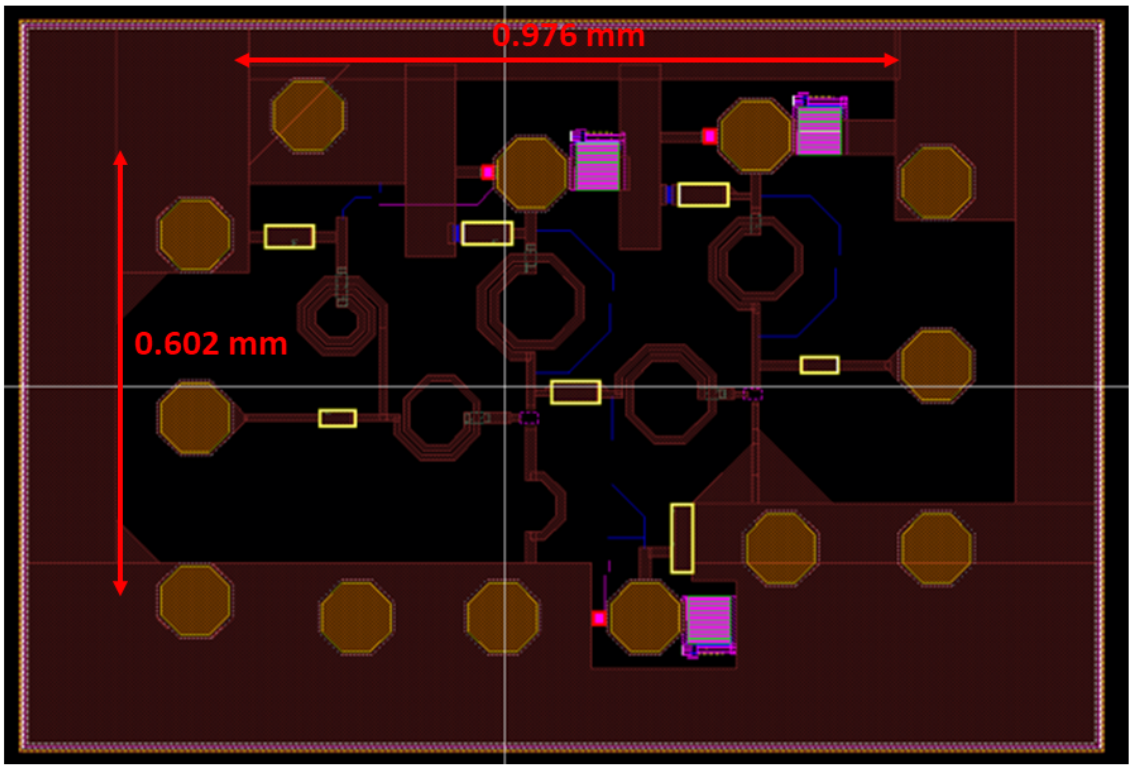


Figure 3.21 Layout of the proposed reference 0.13 μm SOI CMOS LNA.

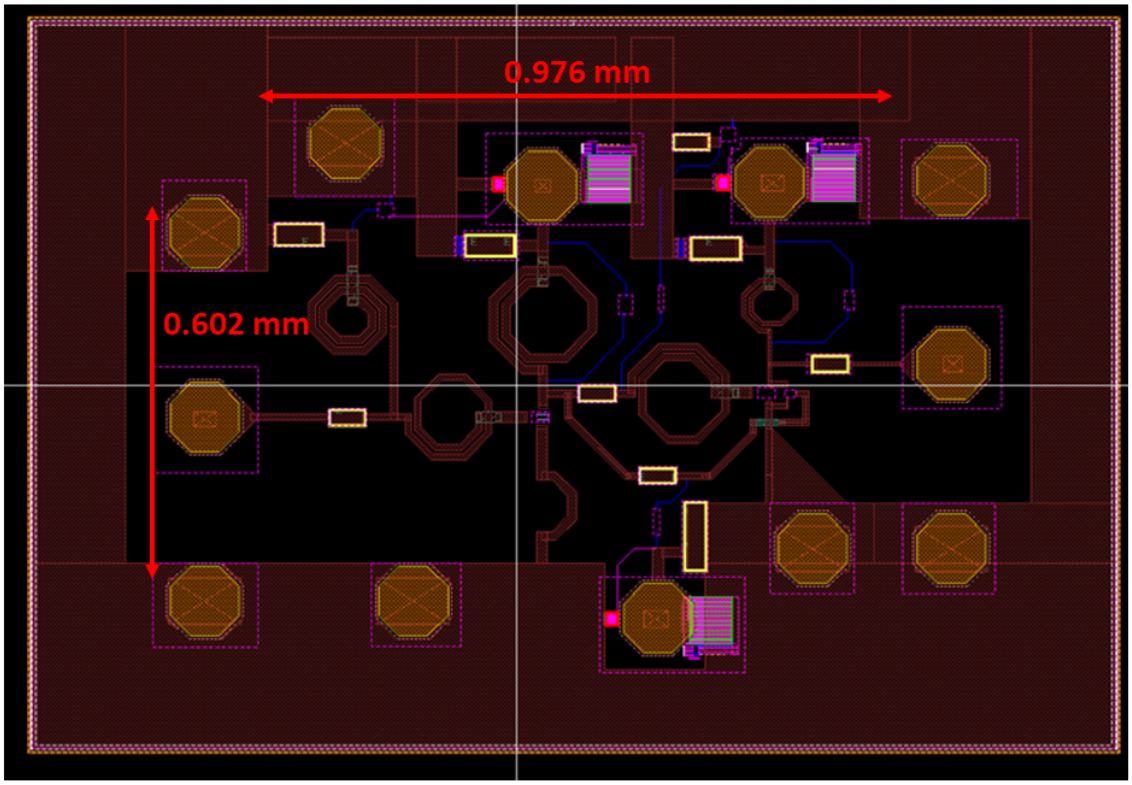


Figure 3.22 Layout of the proposed 0.13 μm SOI CMOS LNA with implemented DS.

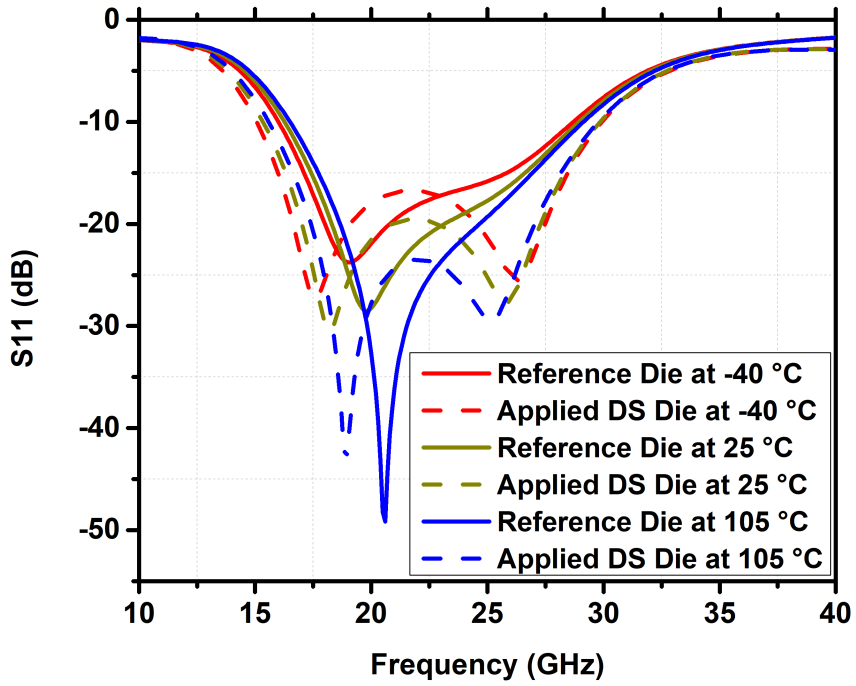


Figure 3.23 Input return loss performance of the 0.13 μm SOI CMOS LNA and the implemented DS linearization technique

3.4.3 Simulations Results of the SOI LNAs

The layouts of the designed chips are presented in Fig. 3.21 and Fig. 3.22. Each design occupies an area of 0.587 mm^2 (0.602x0.976), excluding the pads. The design intends for flip-chip packaging, thus, EM simulations are carried out, incorporating the packaging, bumps, and PCB. As illustrated in Fig. 3.21 and Fig. 3.22, Electrostatic Discharge (ESD) protection devices are positioned along the supply lines to eliminate any static effect in the measurement process. As observable from Fig. 3.22, to implement the derivative superposition, an input-to-drain connection is necessary. Consequently, this results in an additional capacitive effect on the output.

As depicted in Fig. 3.23, the input return losses of both dies fall below -10dB in the range of 15 GHz to 30 GHz for temperature values between -40 - 105 °C. The capacitive effect of the load at the first stage's output pulls the higher frequencies closer to the 50 Ω impedance, thereby leading to significant improvement in input matching in the second design.

In terms of output matching, both designs are below -10dB for the frequency of interest. As demonstrated in Fig 3.24, the die implementing the DS method is

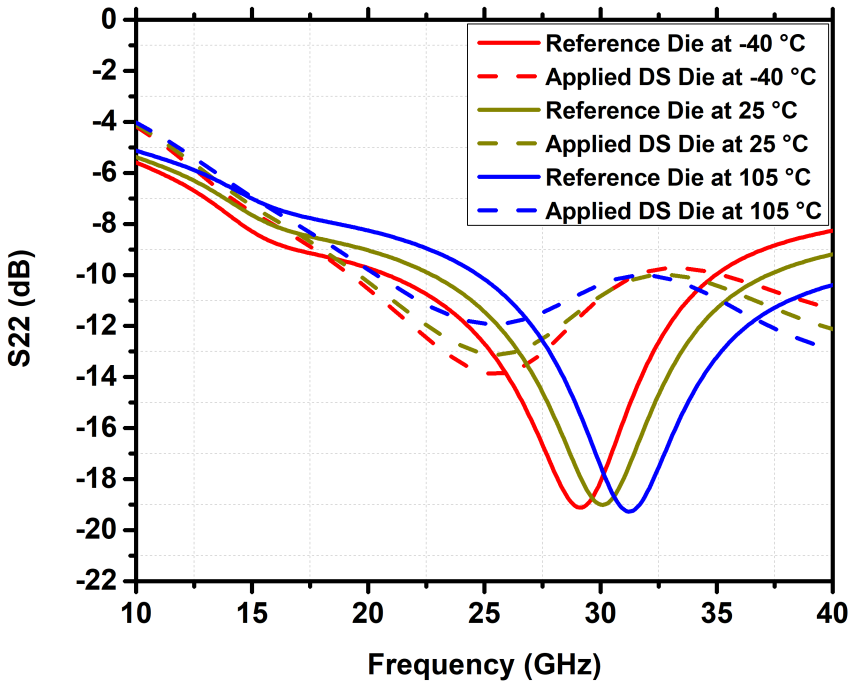


Figure 3.24 Output return loss performance of the 0.13 μm SOI CMOS LNA and the implemented DS linearization technique

shifted towards the lower frequencies. To facilitate matching, the output inductance is slightly reduced. Although the output does not fall below -10 dB for the lower frequencies, as is the case with S11, it still maintains a level below -8 dB. As the temperature increases the output matching of the reference die shifts to the higher frequencies.

A trade-off becomes apparent when examining the gain of the implemented DS die. This is reduced by around 2 dB in the frequency of interest. However, both designs still satisfy the criteria for gain flatness. The 3-dB bandwidth of both designs is 13-30 GHz. It should be noted, however, that the return losses of the design drastically decrease at the 13 GHz frequency, rendering the 13-15 GHz frequencies unsuitable for amplification. The gain graphs of both designs are depicted in Fig. 3.25.

Regarding the NF performance of the system, the loading effect on the output of the first stage elevates the NF by around 0.1 dB. However, both designs maintain an NF performance below 2 dB within the 15-30 GHz bandwidth. The maximum NF of the reference die is 1.87 dB at 30 GHz, and that of the DS-applied die is 1.96 dB at 30 GHz. The minimum NFs for the reference die and the DS-applied die occurs at 24 GHz with 1.65 dB and at 21 GHz with 1.7 dB, respectively at the nominal temperature value. The NF performances of both designs are presented in

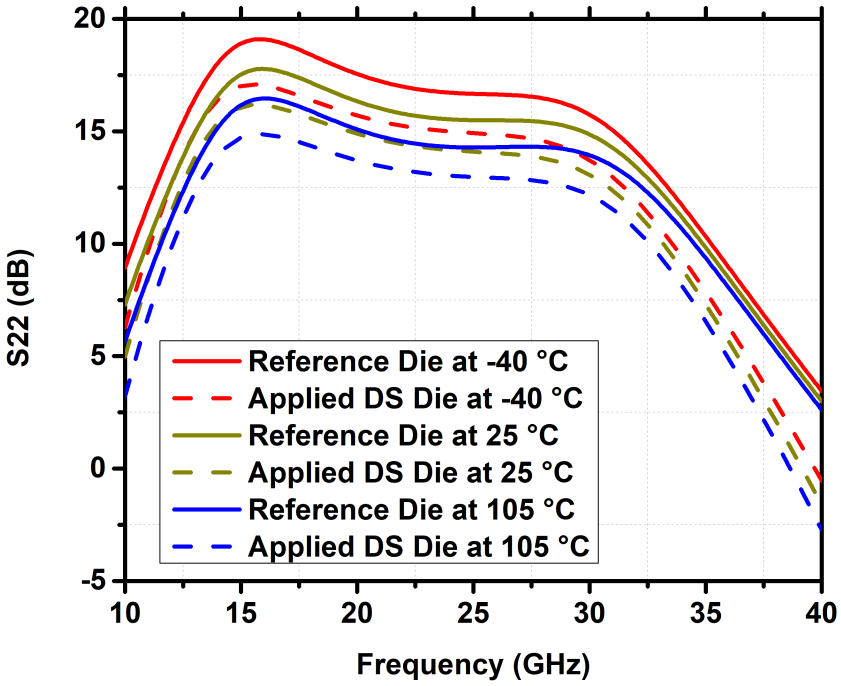


Figure 3.25 The gain performance of the 0.13 μm SOI CMOS LNA and the implemented DS linearization technique

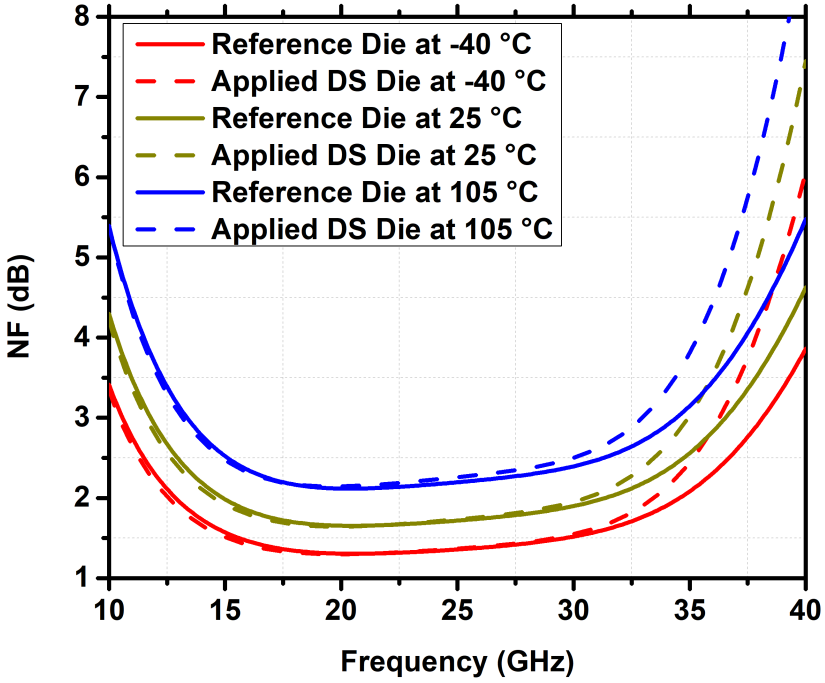


Figure 3.26 Noise figure performance of the 0.13 μm SOI CMOS LNA and the implemented DS linearization technique

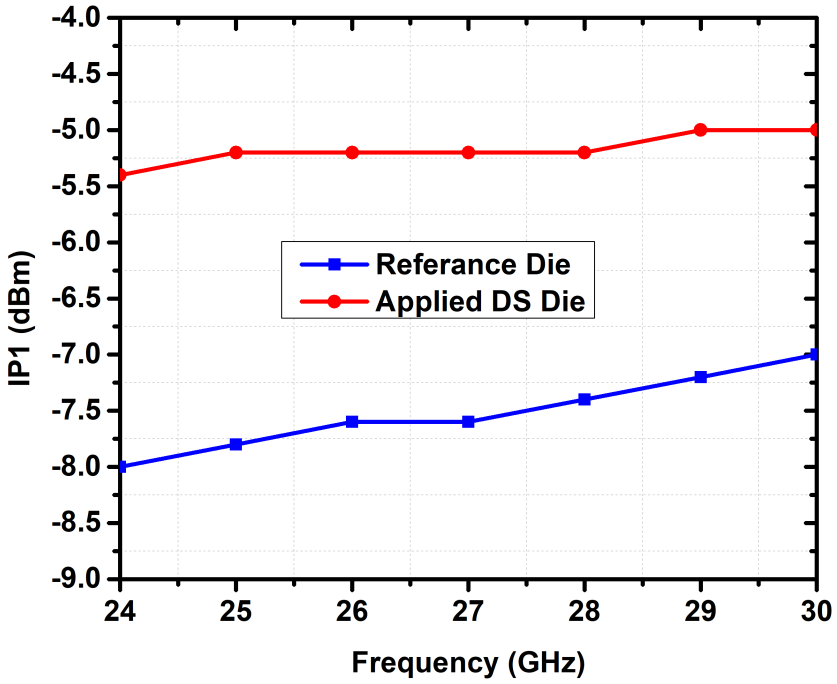


Figure 3.27 The IP1dB performance of the 0.13 μm SOI CMOS LNA and the implemented DS linearization technique with respect to frequency

Fig. 3.26. As the temperature increases, the NF of the LNA also rises, owing to the increased electron excitations.

The performance of the Input Power at 1dB Compression Point (IP1dB) at various frequencies is depicted in Fig. 3.27. The implementation of DS boosted the IP1dB by approximately 2 dB within the frequency of interest. The highest IP1dB for the reference die was observed at 30 GHz with a measure of -7.4 dBm, while the DS-applied die demonstrated an optimal IP1dB performance at -5.2 dBm. A power sweep for both the reference and the DS-applied die, conducted at the central frequency, is presented in Fig. 3.28.

The OIP3 performance of both the reference die and the DS-applied die is delineated in Fig. 3.29. The OIP3 was examined at various power levels, with the DS application enhancing the OIP3 performance of the system by approximately 2 dB at lower frequencies. However, as frequency increases, the capacitive effect arising from the DS implementation's input-to-output path compromises performance. The corresponding IIP3 performance of the dies, with an applied input power of -20 dBm, is depicted in Fig. 3.30. The most substantial improvement, an increase of 3 dB, was noted at 25.5 GHz.

Stability is a significant concern for CS topology due to the C_{GD} capacitor, as

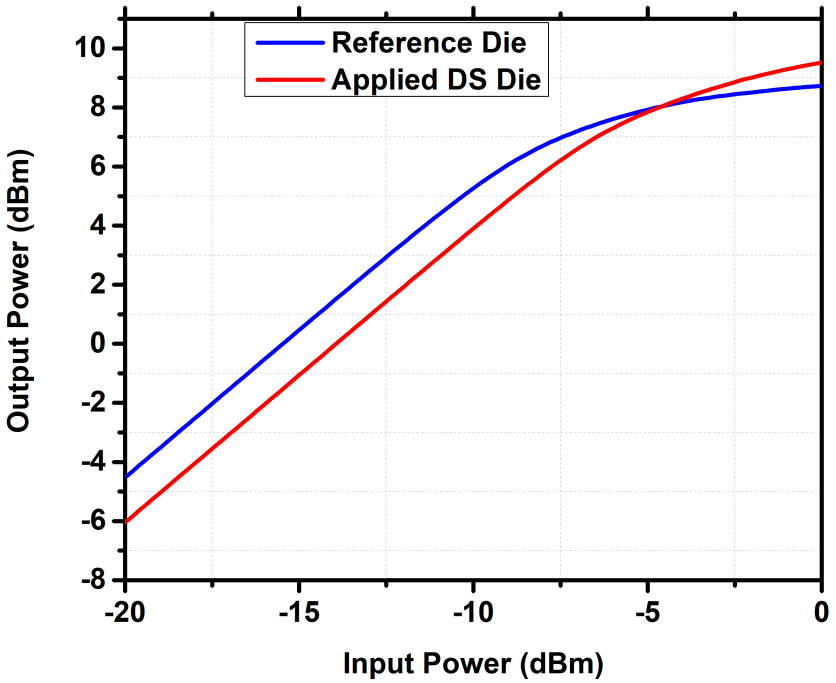


Figure 3.28 The IP1dB performance of the 0.13 μm SOI CMOS LNA and the implemented DS linearization technique with respect to different power levels

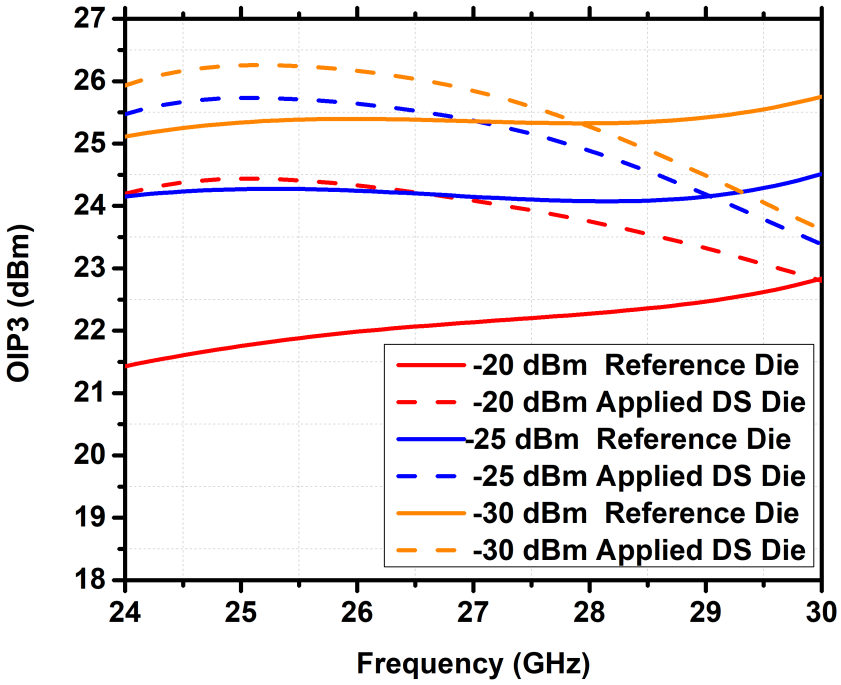


Figure 3.29 The OIP3 performance of the 0.13 μm SOI CMOS LNA and the implemented DS linearization technique with respect to frequency for different power levels

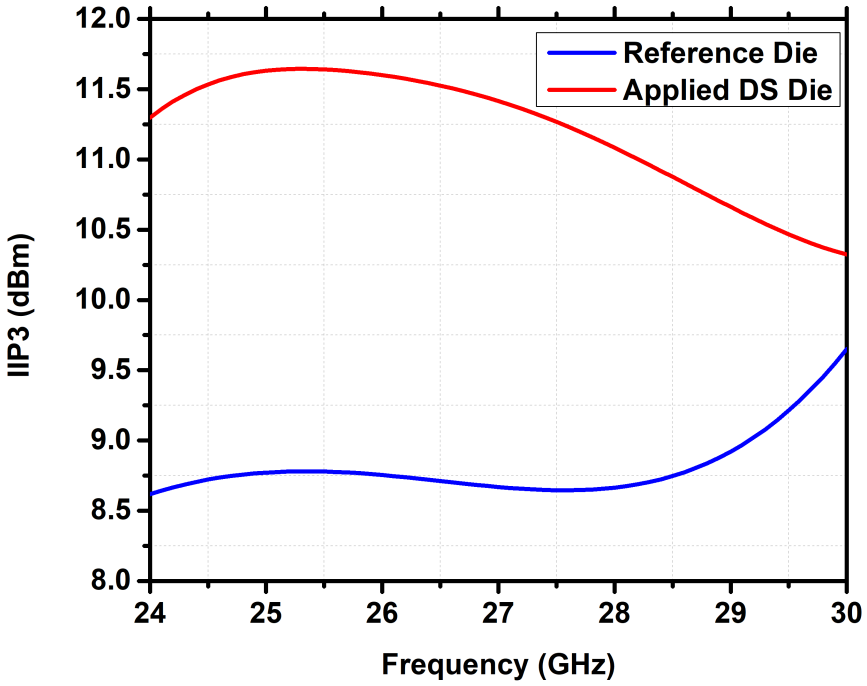


Figure 3.30 The IIP3 performance of the 0.13 μm SOI CMOS LNA and the implemented DS linearization technique at -20 dBm

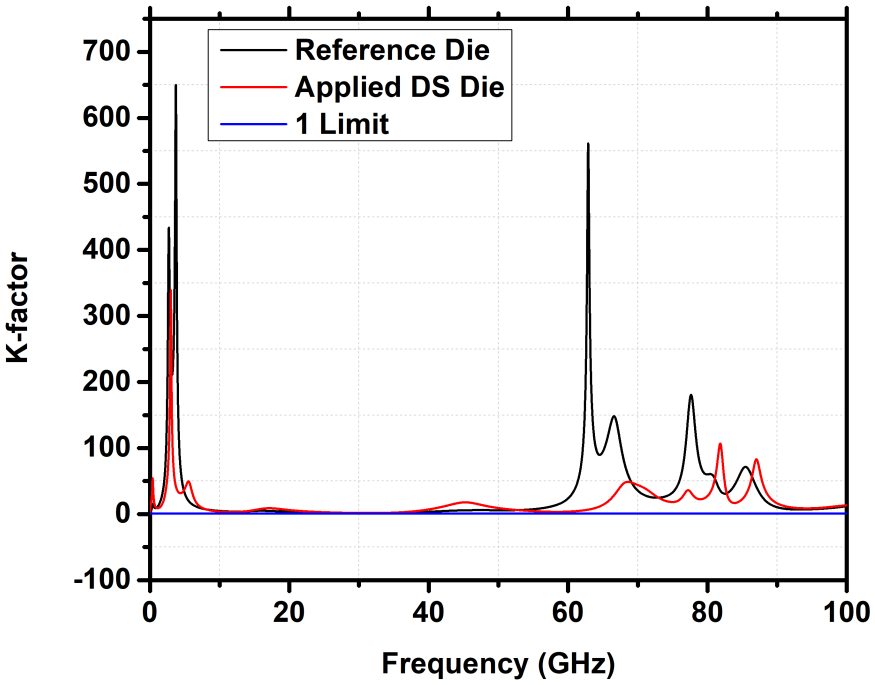


Figure 3.31 The stability performance of the 0.13 μm SOI CMOS LNA and the implemented DS linearization technique

mentioned previously. Therefore, the stability of both designs has been examined across a wide frequency range, from 10MHz to 100GHz, since it is crucial that stability is established at all frequency points. The stability of the design is examined via the K-factor, with a value above 1 indicating the achievement of unconditional stability. Fig. 3.31 portrays the K-factor for both designs. The formula for K- factor is presented in equation (3.9)

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 - |\delta|^2}{2|S_{11}S_{22}|} \tag{3.9}$$

3.4.4 Conclusion

The comparison of both LNAs with those reported in the literature is presented in Table 3.2. The FoMs are calculated using equations (3.5)-(3.6). Both LNAs analyzed in this thesis outperform those in the table, primarily due to their superior linearity performance. However, in terms of gain, the LNA reported by (Kolb, Potschka, Maiwald, Aufinger, Dietz & Weigel, 2020) exhibits the highest value when compared with the other LNAs in the table. (Morkner, Kennan, Niedzwiecki & Galla, 2011) achieved a very low NF owing to its extensive bandwidth of 1-20 GHz, as lower NFs are more readily achievable at lower frequencies.

Table 3.2 The performances of the LNA in the literature compared the SOI LNAs

References	[1]	[2]	[3]	[4]	[5]	[6]	**Cu LNA**	**Reference LNA**	**Applied DS LNA**
Technology	0.13μm SiGe BiCMOS	0.18μm SiGe BiCMOS	90nm RF CMOS	45 nm SOI CMOS	0.15μm GaAs PHEMT	0.13μm SiGe BiCMOS	**0.13μm SiGe BiCMOS Cu**	**0.13μm SOI CMOS**	**0.13μm SOI CMOS**
Freq. (GHz)	21.4-30.6	16-24	17.-21	17-24	1-20	24-28	**24-28**	**15-30**	**15-30**
Gain (dB)	24	19	12.3	19.5	20	12.8	**13.5**	**16**	**14**
Area (mm^2)	0.07	0.389	0.68	1.44	1.8	0.23	**0.198**	**0.587**	**0.587**
P_{DC} **(mW)**	25.1	22.5	11.2	32.5	175	5.4	**37.29**	**28.3**	**34.2**
IP1dB (dBm)	-13	-0.16	-11	-18.5	-9	-10.5	**-4**	**-7.6**	**-4.4**
IIP3 (dBm)	-	-4	-2.3	-8	3	1	**2.7**	**8.6**	**11.5**
NF_{min} **(dB)**	2.18	1.83	2.1	2	1.1	2.08	**1.73**	**1.64**	**1.7**
FoM_1 **(MHz)**	7077	1353	581	529	4741	1023	**1967**	**7992**	**8348**
FoM_2 **(MHz)**	-	21455	4307	5944	75153	14461	**31180**	**333171**	**324811**

[1] (Kolb et al., 2020)
[2] (Kanar & Rebeiz, 2014)
[3] (Aspemyr, Jacobsson, Bao, Sjoland, Ferndahl & Carchon, 2006)
[4] (Kanar & Rebeiz, 2013)
[5] (Morkner et al., 2011)
[6] (Burak et al., 2021)

4. CONCLUSION

4.1 Summary of Work

The rapid advancement in 5G technologies is necessitating heightened demands for high data rate transfer, extensive-range communications, and low latency. To augment this data rate, emerging techniques, such as phased array systems, are being leveraged. These systems employ beam-forming strategies to regulate the beam's focus, significantly enhancing its directivity. In order to accommodate a surge in data transfer through these methodologies, the corresponding SNR must be as high as possible, thereby increasing the volume of data transfer per cycle. Consequently, it is vital for the receiver chain to suppress noise to the greatest extent possible. Furthermore, bandwidth bears considerable importance in terms of data transfer: the wider the bandwidth, the greater the corresponding data transfer. To achieve these conditions, it is essential to maintain the NF of the system as low as possible and ensure high linearity.

In this thesis, the 4x1 Tx/Rx MIMO modules, designed in 0.13 μm SiGe BiCMOS by (Burak, 2021), were implemented as a complete system by integrating an HMC 292 mixer by ADI. Subsequently, an LNA was designed in 0.13 μm SiGe BiCMOS Cu technology and fabricated in to evaluate if the NF of the 4x1 Rx MIMO could be further improved. The performance of this LNA was examined.

Subsequent to this, in an effort to enhance the linearity of the LNA, two distinct LNAs were designed using GlabalFoundries 0.13 μm SOI CMOS technology. The first LNA was designed as the reference LNA, achieving gain flatness. In contrast, the second LNA was designed by implementing the DS technique to improve the system's linearity. The results of these two LNAs were analyzed, with corresponding trade-offs considered.

4.2 Future Work

The LNA designed using 0.13 μm SiGe BiCMOS Cu technology will be integrated with the remaining blocks to gauge improvements within the total system, while also enhancing the input return loss of this specific block.

The LNAs designed using 0.13 μm SOI CMOS technology will be prepared for tape-out and subsequently fabricated. Post-fabrication, their performance will be verified through measurements and compared with the simulation results. The gain of the dies, upon which DS has been applied, will be further improved without compromising the linearity performance.

BIBLIOGRAPHY

Adabi, E., Heydari, B., Bohsali, M., & Niknejad, A. M. (2007). 30 ghz cmos low noise amplifier. In *2007 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, (pp. 625–628).

Aljuhani, A. H. & Rebeiz, G. M. (2019). A 12.5 mw packaged k-band cmos soi lna with 1.5 db nf. In *2019 IEEE MTT-S International Microwave Symposium (IMS)*, (pp. 156–159).

Allstot, D., Li, X., & Shekhar, S. (2004). Design considerations for cmos low-noise amplifiers. (pp. 97 – 100).

Andrews, J. G., Buzzi, S., Choi, W., Hanly, S. V., Lozano, A., Soong, A. C. K., & Zhang, J. C. (2014). What will 5g be? *IEEE Journal on Selected Areas in Communications*, *32*(6), 1065–1082.

Aparin, V., Brown, G., & Larson, L. (2004). Linearization of cmos lna's via optimum gate biasing. In *2004 IEEE International Symposium on Circuits and Systems (IEEE Cat. No.04CH37512)*, volume 4, (pp. IV–748).

Aspemyr, L., Jacobsson, H., Bao, M., Sjoland, H., Ferndahl, M., & Carchon, G. (2006). A 15 ghz and a 20 ghz low noise amplifier in 90 nm rf-cmos. In *Digest of Papers. 2006 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, (pp. 4 pp.–).

Burak, A. (2021). 4x1 mimo compact half duplex rf t/r module with high resolution in 130 nm sige bicmos for 5g applications. Master's thesis, Sabanci University.

Burak, A., Altintas, K., Yazici, M., & Gurbuz, Y. (2021). Lna designs for 5g receiver applications. In *2021 IEEE Asia-Pacific Microwave Conference (APMC)*, (pp. 10–12).

Cressler, J. & Niu, G. (2003). *Silicon-germanium Heterojunction Bipolar Transistors*. Artech House.

Ding, Y. & Harjani, R. (2001). A +18 dbm iip3 lna in 0.35 /spl mu/m cmos. In *2001 IEEE International Solid-State Circuits Conference. Digest of Technical Papers. ISSCC (Cat. No.01CH37177)*, (pp. 162–163).

Elkholy, M., Shakib, S., Dunworth, J., Aparin, V., & Entesari, K. (2018). A wide-band variable gain lna with high oip3 for 5g using 40-nm bulk cmos. *IEEE Microwave and Wireless Components Letters*, *28*(1), 64–66.

Gurol, E. (2022). Highly linear low noise amplifiers using cmos soi and sige bicmos technologies for 5g (28 ghz) applications. Master's thesis, Sabanci University.

Issakov, V. & Ciocoveanu, R. (2019). Low-power k-band lna in 45 nm soi cmos. In *2019 IEEE International Conference on Microwaves, Antennas, Communications and Electronic Systems (COMCAS)*, (pp. 1–4).

Kanar, T. & Rebeiz, G. M. (2013). A 16-24 ghz cmos soi lna with 2.2 db mean noise figure. In *2013 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, (pp. 1–4).

Kanar, T. & Rebeiz, G. M. (2014). X- and k-band sige hbt lnas with 1.2- and 2.2-db mean noise figures. *IEEE Transactions on Microwave Theory and Techniques*, *62*(10), 2381–2389.

Kim, N., Aparin, V., Barnett, K., & Persico, C. (2006). A cellular-band cdma 0.25-/spl mu/m cmos lna linearized using active post-distortion. *IEEE Journal of*

Solid-State Circuits, *41*(7), 1530–1534.

Kolb, K., Potschka, J., Maiwald, T., Aufinger, K., Dietz, M., & Weigel, R. (2020). A 28 ghz broadband low noise amplifier in a 130 nm bicmos technology for 5g applications. In *2020 23rd International Microwave and Radar Conference (MIKON)*, (pp. 192–195).

Koranga, A. & Barman, K. (2013). Performance enhancement of wimax using adaptive modulation scheme. *International Journal of Scientific and Engineering Research*, *4*, 1794–1797.

Kuo, J. *low-voltage soi cmos vlsi devices and circuits*. Wiley-India.

Lin, X., Li, J., Baldemair, R., Cheng, J.-F. T., Parkvall, S., Larsson, D. C., Koorapaty, H., Frenne, M., Falahati, S., Grovlen, A., & Werner, K. (2019). 5g new radio: Unveiling the essentials of the next generation wireless access technology. *IEEE Communications Standards Magazine*, *3*(3), 30–37.

Mailloux, R. (1994). *Phased Array Antenna Handbook*. Antennas and Propagation Library. Artech House.

Mailloux, R. (2017). Phased array antenna handbook, third edition.

Morkner, H., Kennan, W., Niedzwiecki, T., & Galla, T. (2011). A novel small phemt lna that integrates active matching for 1 to 20ghz and 1.1db nf performance. In *2011 6th European Microwave Integrated Circuit Conference*, (pp. 370–373).

Pozar, D. (2011). *Microwave Engineering, 4th Edition*. Wiley.

Rao, G. (2012). *Cellular Mobile Communication*. Pearson Education India.

Rappaport, T. S., Murdock, J. N., & Gutierrez, F. (2011). State of the art in 60-ghz integrated circuits and systems for wireless communications. *Proceedings of the IEEE*, *99*(8), 1390–1436.

Razavi, B. (1998). *Rf Microelectronics*. Prentice Hall.

Roh, W., Seol, J.-Y., Park, J., Lee, B., Lee, J., Kim, Y., Cho, J., Cheun, K., & Aryanfar, F. (2014). Millimeter-wave beamforming as an enabling technology for 5g cellular communications: theoretical feasibility and prototype results. *IEEE Communications Magazine*, *52*(2), 106–113.

Xin, C. & Sanchez-Sinencio, E. (2004). A linearization technique for rf low noise amplifier. In *2004 IEEE International Symposium on Circuits and Systems (ISCAS)*, volume 4, (pp. IV–313).

Yoon, Y., An, K. H., Kang, D., Kim, K., Lee, S., Jang, J. S., Minn, D., Suh, B., Lee, J., Kim, J., Kim, M., Lee, J. H., Choi, S. T., Son, J., & Yang, S.-G. (2019). A highly linear 28ghz 16-element phased-array receiver with wide gain control for 5g nr application. In *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, (pp. 287–290).

Zhang, H. & Sánchez-Sinencio, E. (2011). Linearization techniques for cmos low noise amplifiers: A tutorial. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *58*(1), 22–36.