DESIGN OF VOLTAGE CONTROLLED OSCILLATOR AND INTEGER-N DIVIDER FOR 5G FREQUENCY SYNTHESIZER APPLICATION

by
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ABSTRACT

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Keywords: Voltage Controlled Oscillator,Integer-N Divider, Phase Locked Loop , Frequency Synthesis, 5G, SiGe

In 5G systems, transceivers require LO signals at mmWave frequencies with low phase noise to meet the SNR required for data rates of multiple gigabits per second. In addition, the PN causes detection errors, causing internal noise, and further performance degradation. The primary on-chip solution for generating an LO signal is a phase-locked loop used as a frequency synthesizer to generate a frequency range from a given reference that meets the required noise performance. The VCO is the integral block that affects the overall performance the most among the blocks that make up the phase locked loop.

This thesis focuses on designing the VCO and integer-N frequency divider circuits for Type-II fourth order integer-N PLL-based frequency synthesizer realized in IHP SG13S technology. Two different VCOs that have 3 and 4-bit capacitor banks are realized. Both designs utilize the varactor linearity control method to exploit the tuning range and the quality factor relation. The measured 3-bit VCO achieves a tuning range between 9.46 to 11.092 GHz and has a phase noise of -114.42 dBc/Hz at 1MHz offset at the center frequency with a power consumption of 28.7 mW and 2.38 mm^2 area. The simulation results of the 4-bit VCO are a 9.5 to 12.02 GHz tuning range and -116.2 dBc/Hz noise at the center frequency, with a power consumption of 30mW and 2.33 mm^2 area. Furthermore, the design of the divider is examined, and modifications to improve the area and power consumption are done, which performs the required division VCO output to 100MHz. Finally, the realized PLL has a simulated phase noise of -108.7 dBc/Hz and an area of 4.67 mm^2.

ÖZET

5G Frekans Sentezleyici Uygulaması için Voltaj Kontrollü Osilatör ve Tamsayı-N Bölücü Tasarımı

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ELEKTRONİK MÜHENDİSLİĞİ YÜKSEK LİSANS TEZİ, YAZ 2022

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5G sistemlerinde, alıcı-vericiler, saniyede çoklu gigabit veri hızları için gereken SNR'yi karşılamak için düşük faz gürültülü mmWave frekanslarında LO sinyalleri gerektirir. Ayrıca PN, algılama hatalarına neden olarak dahili parazite ve daha fazla performans düşüşüne neden olur. Bir LO sinyali üretmek için çip üzerinde birincil çözüm, belirli bir referanstan gerekli gürültü performansını karşılayan bir frekans aralığı oluşturmak için frekans sentezleyici olarak kullanılan faz kilitli bir döngüdür. VCO, faz kilitli döngüyü oluşturan bloklar arasında genel performansı en çok etkileyen integral bloktur.

Bu tez, IHP SG13S teknolojisinde gerçekleştirilen Tip-II dördüncü mertebeden tamsayı-N PLL tabanlı ferkans sentezleyici için VCO ve tamsayı-N bölücü devrelerinin tasarımına odaklanmaktadır. 3 ve 4 bitlik kapasitör banklarına sahip iki farklı VCO gerçeklenmiştir. Her iki tasarım da ayar aralığını ve kalite faktörü ilişkisini kullanmak için varaktör doğrusallık kontrol yöntemi kullanır. Ölçülen 3-bitlik VCO, 9.46-11.092 GHz ayarlanma aralığına sahiptir ve merkez frekansta -114.42 dBc/Hz faz gürültüsünü, 28.7 mW güç tüketimi ve 2.38 mm^2 alanda sağlar. 4-bitlik VCO benzetim sonuçlarında 30mW güç tüketimi ve 2.33 mm^2 alanda, 9.5-12.02 GHz ayarrlanma aralığı ve merkez frekansta -116.2 dBc/Hz gürültrü sağlamıştır. Ayrıca VCO'nun çıkışını bölerek 100MHz'e yaklaştıran bölücü devresi incelenmiş, alan ve güç tüketimini azaltacak geliştirmeler yapılmıştır. Son olarak, gerçeklenen PLL, benzetim sonuçları doğrultusunda -108.7 dBc/hz gürültüye sahiptir ve 4.67 mm^2 alan kaplamaktadır.

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Her zaman yanımda olan aileme...
To my family, who are always by my side...

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LTE Long-Term Evolution 1

MIM Metal-Insulator-Metal 33

MIMO Multiple Input Multiple Output 4

mmWave Millimeter Wavelenghts 1

MOSFET Metal-oxide Semiconductor Field Effect Transistor 12

NF Noise Figure 3

PFD Phase Frequency Detector 9

PLL Phase Locked Loop 5

PN Phase Noise 3

PVT Process Variation and Temperature 7

RF Radio Frequency 3

SA Spectrum Analyzer 64

SiGe Silicon Germanium 11

SNR Signal to Noise Ratio 3

SSCR Single Sideband to Carrier Ratio 31

TDC Time to Digital Converter 24

TRX Transceiver 3

Varactor Variable Capacitor 12

VCO Voltage Controlled Oscillator 7

YIG Yttrium Iron Garnet 5

1. INTRODUCTION

1.1 5G Communication Systems

The recent technological advancements made wireless communication systems include different variety of functionalities and have become critical structures used in various applications. Considering the wide usage of these systems, the total data traffic due to wireless communication increased by %74 from 2005 to 2020 (CISCO, 2017). Furthermore, this traffic has an increasing trend since the devices contributing to data traffic per capita are expected to increase to 3.6 by 2023 (CISCO, 2018). To satisfy the rising demand and the functionality, the data rates and the bandwidth of these systems have to be increased. However, these improvements exceed the capabilities of the 4th generation long-term evolution (4G LTE) telecommunication networks. The data rate requirement of the 5G networks aims at least 1 Gbps, which is almost ten times larger than the peak data rate of 150 Mbps of LTE, and the latency of 1ms, ten times less than 10ms of LTE (Agiwal et al., 2016; Roh et al., 2014). The new data rate requirement is at least ten times higher than the long-term evolution (LTE), a mobile service providing the fastest data rate until 5G (3rd Generation Partnership Project, 2018). The sub-6 GHz does not allow the required bandwidth for such data rates since it is already occupied with applications like WiMAX, Wifi, and Bluetooth and contains denser data traffic. The provided requirements and performance expectations are the reasons behind the selection of millimeter wave bands (mmWave) for 5G applications (Rappaport et al., 2013; Andrews et al., 2014). The frequency range for Europe is 24.25 - 27.5 GHz, named n258 or 26 GHz band (EUC, 2019). Furthermore, 40-500 MHz channel bandwidth was set to achieve higher data rates (3rd Generation Partnership Project, 2018). Fig. 1.1 (Skyworks, 2017) shows the targets and application fields of the 5G, and Fig.1.2 shows the allocated frequency spectrum for different countries. It can be noticed that the designated frequency bands are overlying, which means each system in different bands can be fitted to one other (Ahmadi, 2019).

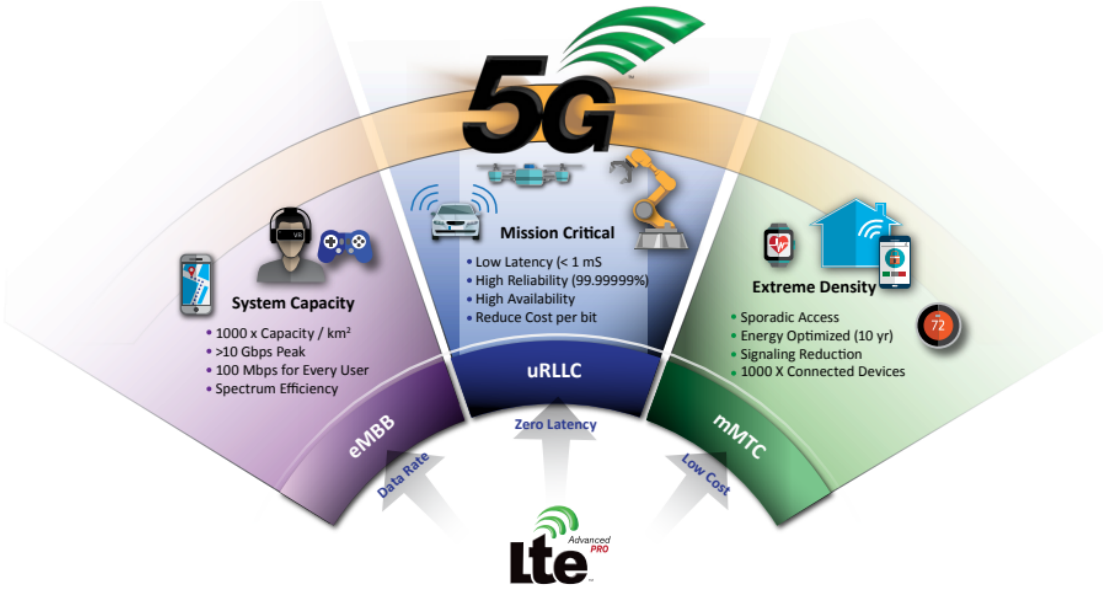


Figure 1.1 5G Targets and Applications (Skyworks, 2017)

Region	Sub-6 GHz Spectrum							mmWave Spectrum			
	New Band		Existing Band		3GPP Band	Bandwidth (MHz)	Total Bandwidth (MHz)	F_{Low} (GHz)	F_{High} (GHz)	Bandwidth (GHz)	Total Bandwidth (GHz)
	F_{Low} (MHz)	F_{High} (MHz)	F_{Low} (MHz)	F_{High} (MHz)							
Korea	3400	3700				300	300	26.50	29.50	3.00	3.00
European Union	3400	3800	2570 3400	2620 3800	38 42 + 43	50 400	450	24.25 31.80 40.50	27.35 33.40 43.50	3.10 1.60 3.00	7.70
Japan	3600 4400	4200 4900	2496 3400	2690 3600	41 42	194 800 500	1494	27.50	29.50	2.00	2.00
United States	–	–	2496 3550	2690 3700	41 48	194 150	344	27.50 37.00 38.60 64.00	28.35 38.60 40.00 71.00	0.85 1.60 1.40 7.00	10.85
China	3300 4400 4800	3600 4500 4990	2300 2555 3400	2400 2655 3600	40 41B 42	100 100 300 100 190	790	TBD			

Figure 1.2 5G Frequency Spectrum (Ahmadi, 2019)

Due to higher operating frequencies, the path loss is creating one of the most fundamental challenges in these applications. This challenge can be mitigated with an antenna that ables increased gain and adaptable directivity. Thus, the omni-directional antennas used in the previous generation are not eligible for this task (El-Halwagy, 2018). Hence, 5G systems require efficient beamforming techniques with a high level of directivity to achieve the required data rates and signal-to-noise ratio (SNR). On top of the signal directivity and SNR, the 5G system should not compromise power consumption and area. Since these systems will be employed in mobile devices too, they should be compatible with the power of a mobile device's battery for its future and feasibility, and they should have reasonable fabrication costs.

The small wavelengths of mmWave frequencies allow using numerous antenna elements in a small area to synthesize highly directional beams obtaining significant array gains (Roh et al., 2014). Regarding the raised number of its elements, the RF performance of the phased arrays is mission-critical for 5G systems. The phased array systems realized in the mmWave band for 5G will enable high data rates for a large number of users compared to the previous generation. The targeted high data rates will be achieved by creating a large bandwidth connection between the base stations and mobile devices.

1.2 Effect of Reference Signal on Performance of 5G Systems

Transmit/Receive (Transceiver - TRX) modules are the main factors that determine the properties of array structures since they contain elements of many different applications, from RF circuit elements for beam forming to baseband(BB) signal processing. Considering the TRX modules in 5G systems are realized in the mmWave band, the generation of a LO signal with desired specifications and distribution of this signal to each element in the array is crucial for 5G systems (El-Halwagy, 2018). The reason is that the phase noise (PN), power, and the frequency of the LO signal affect not only the mixer it is connected to but the whole system performance. For instance, the long routings of the LO signal throughout the system will cause signal loss, leading to increased noise figure (NF) and lowered conversion gain to the mixer to which the LO signal is connected. This problem can be overcome by adding buffers in the LO distribution network; however additional buffers will raise the overall power consumption. Moreover, the signal distortion in the LO network is another issue; any effect that lowers the purity of the LO signal will end up as limited resolution, and a lower data acquisition rate (El-Halwagy, 2018). Phase noise

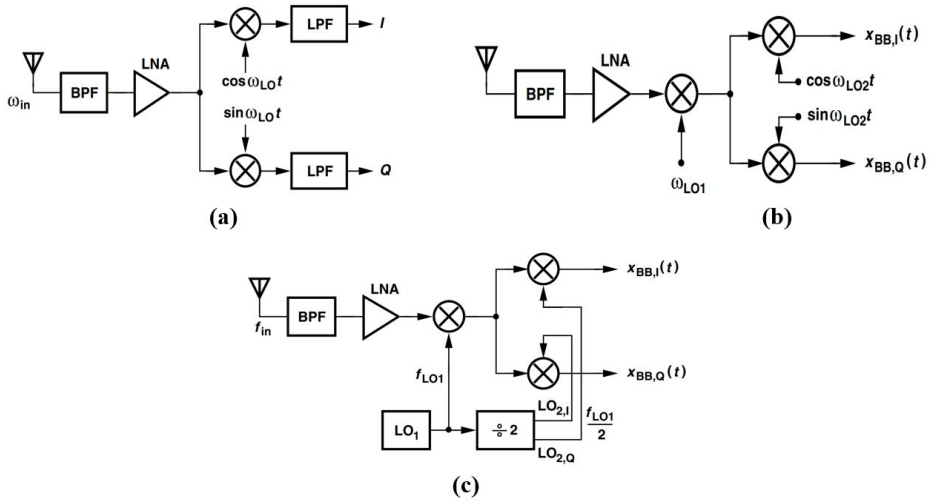


Figure 1.3 Different Frequency Conversion Techniques Used in Receivers (a) Direct (b)Heterodyne (c) Sliding-IF based

is also a significant contributor to the performance limitations; it can disturb the beam properties or degrade the system's capacity by lessening the effective channel (Hohne & Ranki, 2010). The challenges of LO signal quality and distribution make the frequency conversion techniques a vital subject in 5G MIMO applications. Mainly preferred conversion techniques to overcome LO requirements are shown in Fig.1.3 (Razavi, 2011), independent from the beamforming approach. Depending on the preferred technique, the LO signals' expectations alter accordingly.

The direct conversion technique is shown in Fig.1.3(a) downconverts the RF signal with the mixer directly in the receiver chain (upconverts to RF in the transmitter chain). This approach can achieve the required BB (or RF) signal with a single LO signal and a mixer. Also, there a no image frequencies to be suppressed due to a single conversion. Nevertheless, the mixers in this method require an LO signal with a frequency the same as the RF signal. This brings challenges to the generation and distribution of the LO signal in the system. On the other hand, by making the conversion in two steps, the heterodyne conversion, shown in Fig.1.3(b)., relaxes the LO signal generation but requires two different LO signals with different frequencies. Furthermore, both approaches require LO signals with a 90-degree phase shift (quadrature signals) to prevent self-corruption at the baseband (Razavi, 2011). In the sliding-IF architecture shown in Fig.1.3(c), the exact two-step conversion is used, but the secondary LO signal is generated using the first signal and a frequency divider; thus, a single LO is sufficient for this application. Furthermore, if the frequency synthesizer is placed near the mixer, routing in mmWave frequencies will be shorter, leading to a more manageable distribution of the LO signal. Since the second LO signal generated with the frequency divider has a lower frequency, its routing is also not creating any challenges.

1.3 Frequency Synthesis Approaches

A LO signal generation with low PN/jitter and low power consumption is the bottleneck of the state-of-the-art 5G MIMO systems. For applications operating at frequencies up to several hundred MHz, crystal oscillators are used at low frequencies for low-phase noise frequency synthesis. However, common crystal oscillators are not feasible for high data rate applications. At higher frequencies, crystal has to be very thin, which makes them very flimsy and hard to fabricate. Some counterexamples, such as Yttrium Iron Garnet (YIG) resonators with high-quality factors, can be used in mmWave applications with good PN performance (van Delden et al., 2019), but yet they require heterogeneous fabrication with silicon IC technologies.

Another challenge related to crystal oscillators utilization is that their oscillation frequency is fixed. Modern telecommunication systems, wireless, wire-line, and optical, require tunable frequency to operate at different fractions of a frequency band or even between bands. Tunability is also helpful in suppressing errors and noise in the system. Furthermore, modern communication systems operate in multiple channels, even bands; thus, the reference carrier frequency is often changed. This requires generating fast-switching, a frequency stable reference signal. In order to satisfy these requirements, a frequency synthesizer uses one or few very stable reference frequencies to generate required single or multiple ranges of frequencies as commanded by a digital control (Stazewski & Balsara, 2006). Fig.1.4 shows the diagram representation of these devices.

The synthesizers are realized with three main approaches: Direct Analog, Direct Digital, and Indirect or Phase-Locked Loop (PLL) based. Also, there are hybrid ones that combine these main approaches. Detailed analysis and comparison of these techniques are made (Stazewski & Balsara, 2006; Shu & Sanchez-Sinencio, 2005). The basic principles of these synthesizers and their block diagrams are as follows:

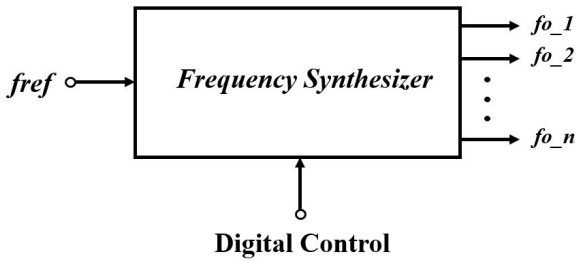


Figure 1.4 Basic Frequency Synthesizer Representation

Direct Analog Synthesis: The direct analog synthesis (DAS), also known as mix/filter/divide, utilizes steps of frequency multipliers, dividers, band-pass filters, and other signal manipulations to generate the desired frequencies by using a single reference input. The methodology is called direct since the error correction procedure is skipped, so the output quality is only related to the quality of the input signal (Stazewski & Balsara, 2006). Although the system is called analog, the division and frequency selection are made digitally (Reinhardt et al., 1986). These synthesizers employ excellent phase noise and spurious performance; however, they occupy a large area, have high power consumption, and are expensive to fabricate. Because of the remarked disadvantages, the DAS method is used predominantly in instrumentation and is unfit for portable, low-power applications like mobile communications (Stazewski & Balsara, 2006). Fig.1.5 shows an example of DAS (Reinhardt et al., 1986); the switched reference generators, shown in Fig.1.5b provide the reference signals to the mixers in the divide and mix block shown in Fig.1.5a. The reference signals are generated by multiplying the reference signal input and depending on the desired frequency, and they are selected by a digital control from the switch array. The output frequency of a DAS can be found with (1.1).

$$f_{\text{out}} = f_1 + 0.1f_2 + 0.01f3 \tag{1.1}$$

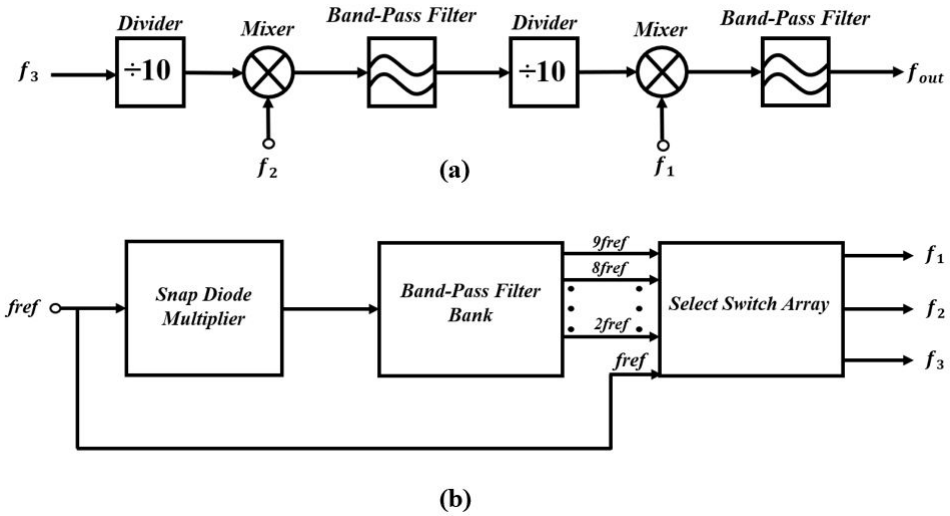


Figure 1.5 Direct Analog Synthesizer Block Diagram

Direct Digital Synthesis: Direct digital synthesis (DDS) uses a digital bit sequence known as a tuning word and develops the necessary output frequency. It uses digital logic and memory to produce the desired signal and then transforms it into analog by a digital to analog converter (DAC). Since the signal is generated entirely digitally, it allows precisely knowing and precisely controlling the signal's

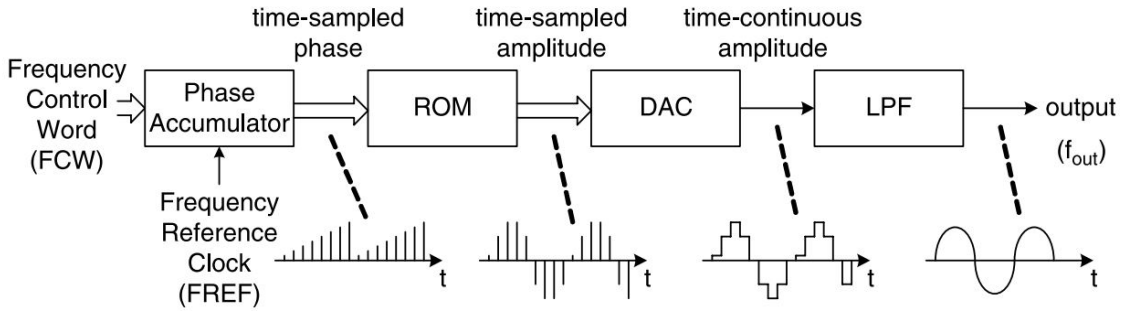


Figure 1.6 Direct Digital Synthesizer Block Diagram (Stazewski & Balsara,2006)

amplitude, phase, and frequency. DDS utilizes high-speed switching; however, the power consumption might become extreme in high-frequency output cases. Furthermore, Nyquist's theory shows that DDS can attain a maximum frequency equal to half of the reference clock (Shu & Sanchez-Sinencio, 2005). While the system is called digital, the output components DAC and the filter used to suppress spurs have profound analog design challenges. Regarding these drawbacks, including high power consumption at gigahertz frequencies, the DDS is unsuitable for mmWave applications; due to its costly implementation. DDS is mainly used only in military applications to this date (Stazewski & Balsara, 2006). Fig.1.6 shows the block diagram of the DDS system, and (1.2) gives the output frequency calculation where W represents the length of the input word. d

$$f_{\text{out}} = \frac{f_{\text{ref}}(FCW)}{2^W} \tag{1.2}$$

PLL Based Synthesis: Voltage-controlled oscillators (VCO) are the choice of LO signal generation in high-frequency applications, but using them standalone is not feasible for complex systems. The process and temperature variations (PVT) will create instability in the oscillation frequency, thus increasing the noise introduced to the system and lower SNR. Additionally, in complex systems with many components, VCO performance can suffer from performance degradations due to coupling with other signals in the system. In order to ensure VCO's output stability, its phase should be adjustable by a control mechanism to make VCO's phase precisely track with a stable reference signal. The required control mechanism can be achieved with a phase-locked loop (PLL), which is a negative feedback system that makes a system track with another (Best, 2007).

The main aim of a PLL is to generate a very accurate frequency output by using an accurate input source, typically a crystal oscillator, which is used as the

reference to obtain a low phase noise output from a high-frequency VCO. In order to generate the required signal, the high-frequency output of the VCO is degraded to the frequency of the reference signal; then, phases of the divided output and the reference signal are compared. Depending on the difference, the loop adjusts the oscillator's frequency until the phase difference is 0. In summary, the loop synchronizes the input reference with the oscillator output in phase; in other words, it "locks." The topologies used for PLL design are divided into two depending on how the loop frequency divider implements frequency division, Integer-N, and Fractional-N. The output frequency of integer-N and Fractional-N can be found with (1.3) and (1.4), respectively. A block diagram of a PLL is given in Fig. 1.7, independent of the division method.

$$f_{\text{out}} = N \cdot f_{\text{ref}} \tag{1.3}$$

$$f_{\text{out}} = (N + \frac{1}{R}) \cdot f_{\text{ref}} \tag{1.4}$$

The required LO performance for 5G communication systems stated in Section1.2, the primary on-chip solution for generating such an LO signal is PLL-based synthesis to create a range of frequencies from a given reference, satisfying the required noise performance. They can be easily adjusted to the current technologies and have lower power consumption than other synthesizer techniques, making them suitable for mobile applications (Shu & Sanchez-Sinencio, 2005). Table.1.1 gives a comparison of the frequency synthesizers that are covered.

1.4 Motivation

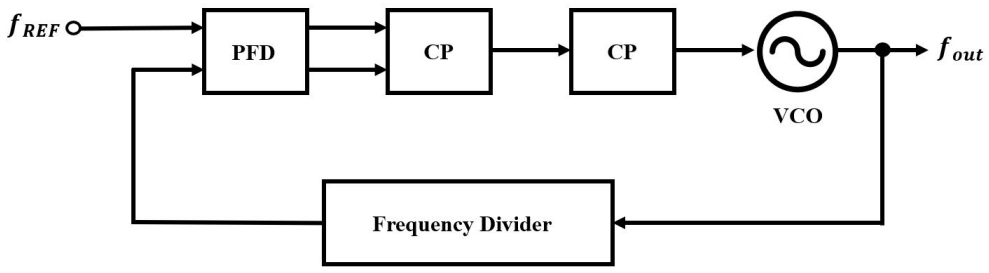


Figure 1.7 General PLL Block Diagram

Table 1.1 Comparison of The Frequency Synthesis Methods (Shu & Sanchez-Sinencio, 2005)

Architecture	Advantages	Disadvantages
Direct Analog Synthesis	Fast switching, Low noise and spur Good for microwave	Large area High power consumption
Direct Digital Synthesis	Fast switching Good resolution	High power consumption Spur
Integer-N PLL	Low power Low noise	Slow switching
Fractional-N PLL	Relatively faster switching	Fractional Spur

The greatest expectation from the new generation 5G MIMO systems is to increase the SNR by decreasing the phase noise of the LO signal. On top of the PN requirements, the frequency synthesizer has to provide a tunable frequency range with proper stability and switching speed while having low area and power consumption. These requirements make the PLL, the primary frequency synthesis solution, a vital block for communication systems. The main building blocks of the PLLs are a phase/frequency detector (PFD), a charge pump (CP), a loop filter(LF), VCO, and a frequency divider. Since the VCO has the most impact on overall PN and directly determines the tuning range among the blocks composing the PLL, VCO is the integral block that impacts the overall performance most. The main objectives of this thesis are to design a VCO and optimize the frequency divider for a synthesizer to be operated for a sliding-IF-based transceiver module in 5G systems. The frequency divider requires optimizations because the initial design consumes a lot of power and occupies a large area. In this work, a hybrid logic combining current mode logic and CMOS logic is implemented to overcome divider-related issues.

The frequency synthesizer of interest and its place in the TRX module are shown in Fig. 1.8, along with the focus of this work. The selected topology for the realization of the PLL is Integer-N since the project focuses on obtaining low phase noise with low power consumption. The integer-N's counterpart, fractional-N PLLs, may exhibit faster switching, but they require extra circuitry to suppress fractional spurs and noise. The additional circuitry requirement of the fractional-N PLL means additional power consumption and complexity.

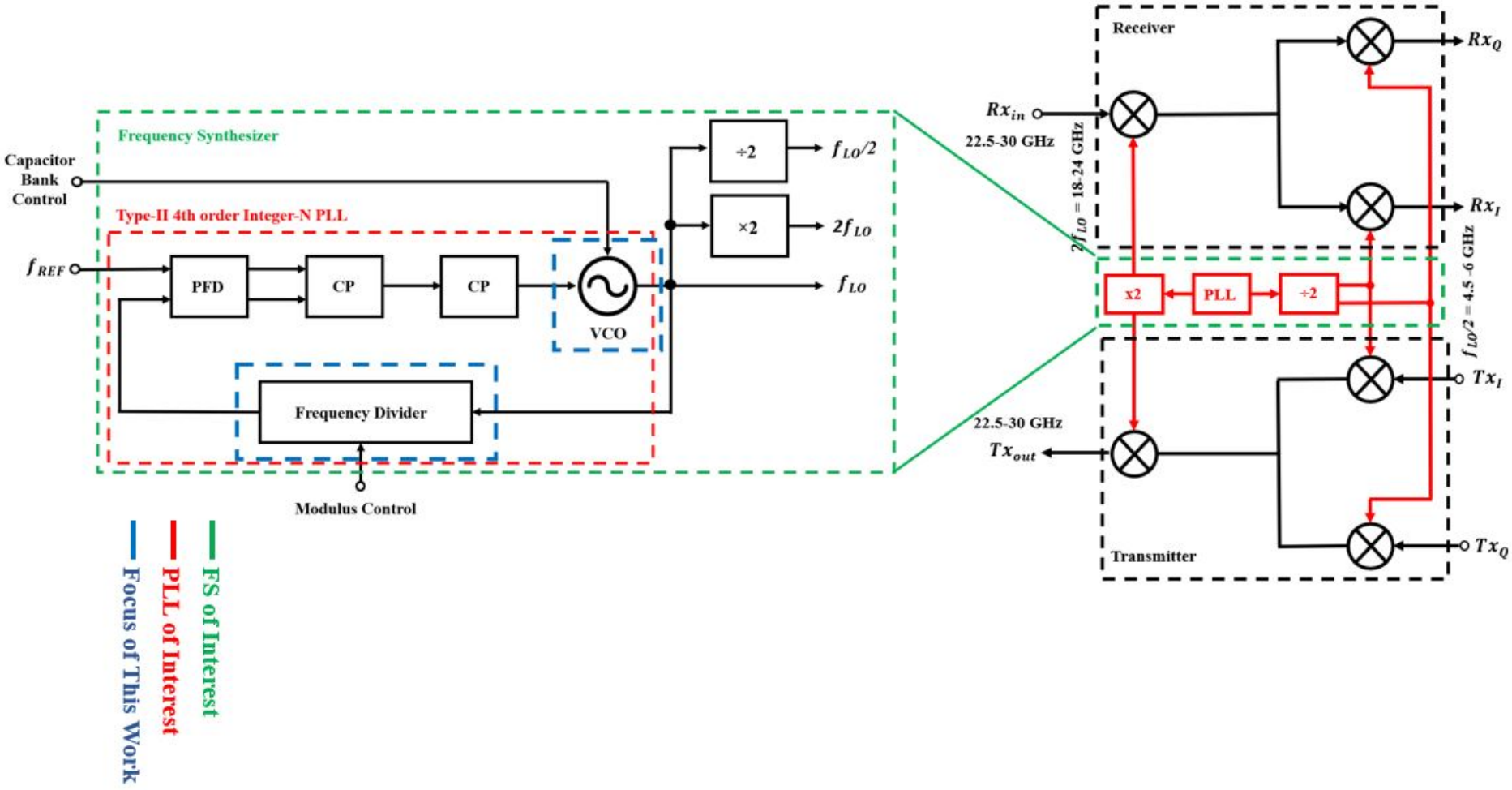


Figure 1.8 Block Diagram Representation of the FS, PLL of interest and Focus of This Work

1.5 Technology Selection

Table 1.2 Comparison of Common Technologies for RF Applications (+ +:Excellent, +: Very Good, 0: Good, - Fair, - - Poor)

Performance Metric	SiGe HBT	III-V HBT	Si CMOS
Frequency Response	+	++	0
1/f and PN	++	-	0
Broadband Noise	+	+	0
Linearity	+	+	+
Output Conductance	++	++	-
Transconductance/Area	++	++	- -
Power Dissipation	++	+	-
CMOS Integration	++	- -	N/A
Cost	0	+	-

The integrated circuit (IC) market mainly uses the three technologies, which are silicon-germanium (SiGe) heterojunction transistors(HBT), the latest generation III-V compound HBTs and conventional silicon complementary metal-oxide semiconductor (CMOS) technologies. The comparison of these technologies for radio-frequency IC (RFIC) applications are shown in Table1.2 (Cressler & Niu, 2003). The CMOS technologies are advantageous in digital applications due to their high scalability; however, considering the high-frequency applications, they perform poorly compared to the other two technologies due to their frequency response. The new generation III-V technologies, such as Gallium-Arsenide (GaAs) and Indium-Phosphite (InP), can handle high power and operate at the sub-THz range. Although III-V technology seems superior for purely RF applications, they have limited application fields because they cannot be integrated with CMOS technology, and the modern 5G blocks, including the frequency synthesizers, require a digital function to employ many functionalities on a single chip. This issue makes SiGe HBT technologies, which have comparable frequency response properties to III-V compounds, as well as high integrability with CMOS, a perfect candidate for versatile 5G blocks. Furthermore, SiGe HBT technologies provide better 1/f and phase noise performance than their alternative. As mentioned in the previous sections, good PN performance of the LO signal is essential for the SNR of the 5G TRX systems; thus, realizing the blocks like VCOs and frequency synthesizer in SiGe technology is more favorable. So because of the stated reasons, a 0.13um SiGe BiCMOS process provided by IHP is selected for the realization of the frequency synthesizer of interest in this work. The technology HBT transistors with f_t / f_{fmax} of 250/340 GHz. For the CMOS integration, two types of MOS field effect tran-

sistors (MOSFET) are provided; the standard transistors operate at Vdd=1.2 V, and if higher breakdown voltages are needed, high voltage (HV) MOSFETs that can operate with 3.3V are also provided. Lastly, the technology provides a layout-optimized MOS variable capacitor (Varactor), which decreases the design challenges of the VCO.

1.6 Organization

In Chapter 1 presents, the evolution of 5G systems and the importance of the LO signal performance on those systems are discussed. Later, the LO signal requirements and its generation techniques are examined on top of the methods used to lighten the LO signal distribution challenges throughout the system. Finally, the motivation behind this work and analysis of the technology used is given.

Chapter 2 explains the fundamentals of the oscillator design from the feedback point of view. The typical oscillator implementations in mmWave frequencies and LC oscillators are analyzed at the device level. Furthermore, the overview of analog charge pump PLL and its comparison with its digital counterpart is examined. Chapter 3 presents the detailed design steps of the Type-II fourth order Integer-N PLL and their simulation results. Furthermore, the system integration steps and an overview of behavioral modeling of the complete PLL are shown.

Chapter 4 gives the measurement methodologies, setups, and results for the designed VCO. Furthermore, a comparison of the measurement results with the literature is also presented. Finally, Chapter 5 summarizes the work done in this thesis and future work to be carried out to improve the frequency synthesizer design.

2. Fundamentals of Oscillators & Analog Charge Pump PLL

2.1 Oscillator Fundamentals

2.1.1 Oscillation Condition

An oscillator is a device that can generate the desired output signal without any input signal, but only by its internal perturbations (noise) and feedback mechanism. The necessary condition can be understood by manipulating a linear negative feedback system (Fig.2.1a) with the transfer characteristic shown in (2.1) to make it unstable.

$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1+H(s)} \tag{2.1}$$

Assuming the H(s) of the feedback shown in Fig.2.1a becomes -1, for a frequency $s = jw_0$. In this case, the open loop frequency response introduces a unity magnitude and a 180°, which means 0 phase margin as shown in Fig.2.1b (Razavi, 2020). In this case, the system's gain from input to output goes to infinity, which means any noise in the system will be amplified indefinitely and will generate a periodic signal at the output with a frequency of w_0.

This behavior of H(s) at a particular frequency means its phase shift is so drastic that it changes the system's feedback from negative to positive. If the open loop characteristics are analyzed under this condition, applying a node X signal will be influenced by 180 phase shifts by H(s) and 180 more by the negative feedback loop itself. A total phase shift of 360 degrees means that the signal returns and will add up to itself while circling the loop (Razavi, 2020). This statement brought the oscillation criteria shown in (2.2) and (2.3), which are called the "Barkhausen's" criteria. Furthermore, $H(jw_0) = -1$ is called the startup condition of the oscillator,

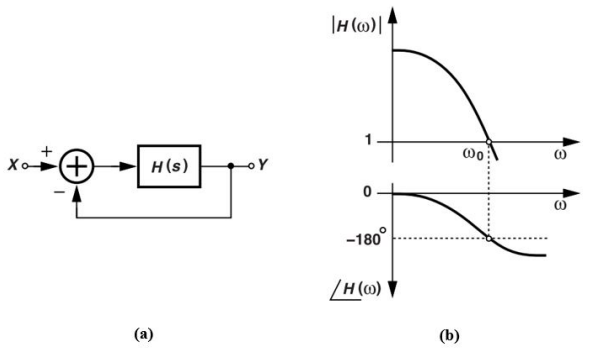


Figure 2.1 a) Negative Feedback System b) Open Loop Frequency Response (Zero Phase Margin) (Razavi,2011)

which implies the minimum requirement for making the system start to oscillate. Growth of an oscillation when the conditions are satisfied, can be seen in Fig.2.2, the input w_0 shown in Fig.2.2(a) represents the internal noise in the system. It should be noted that oscillators do not require input to start up; this perturbation can be introduced anywhere in the loop.

$$| H(jw_0) | = 1 \tag{2.2}$$

$$\angle H(jw_0) = 180^\circ \tag{2.3}$$

The growth of the signal due to the infinite loop gain is limited to a point in reality due to the active device's non-linearities. After a certain point, the active device that provides the gain will saturate due to its nonlinear transconductance behavior, and the growing oscillation amplitude will be limited in amplitude (Hegazi et al., 2001). Section 4.1.1 analyzes the impact of this non-linearity on oscillator design. The following section that explains the LC oscillators will present the oscillation condition and the transconductance dependency on the oscillation condition.

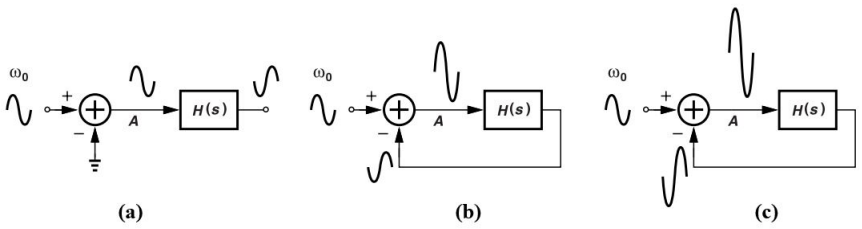


Figure 2.2 Growth of a Oscillation In the feedback due to H(jw_0) = -1 (Razavi,2020)

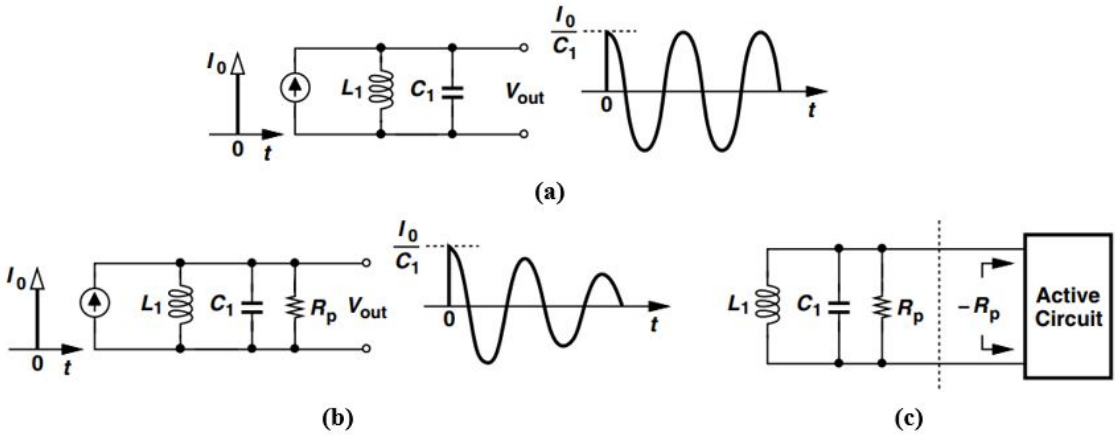


Figure 2.3 a) Response of an Ideal Tank to an Impulse b) Tank circuit with Loss c) Removing of the loss with negative resistance

2.1.1.1 "Harmonic"- LC Resonator Oscillators

Oscillators are fundamentally divided into two “Ring Oscillators” and “Harmonic Oscillators.” Although ring oscillators, which employ a chain of odd number inverters, are advantageous in terms of small area and ease of design, they cannot satisfy the phase noise requirements as harmonic oscillators in high-frequency applications. Harmonic oscillators use a frequency elective element, a resonator circuit (tank circuit), to generate an output signal at the wanted frequency. Although there are examples of series resonance LC circuits in the literature (Pepe et al., 2018), the parallel resonant circuit shown in Fig.4 is the most widely used approach. Ideally, when an impulse is applied to an LC resonator circuit with lossless components, charged C_1 capacitor will first discharge on L_1 inductor. Once the V_{out} voltage becomes 0, L_1 obtains a current equal to $L_1 \cdot \partial V_{out} / \partial t$, and charges the capacitor with an opposite polarity. As a result, a periodic signal will be generated at the resonance frequency at the output, as seen in Fig.2.3a. However, L1 and C1 denote a parasitic resistance to the resonator and cause the output to be dampened in time, as seen in Fig.2.3b. In order for the output to be continuous, a negative resistor is added to the circuit by using active circuit elements (transistors) as shown in Fig.2.3c, and so a regular sine wave is formed by eliminating the effect of parasitic resistance.

The common topologies to implement this resonator circuit with a negative resistance to compensate for the parasitic tank resistance are Colpitts, Hartley, and cross-coupled topologies. The following chapters will investigate how these topologies implement the negative resistance and ensure the oscillation condition.

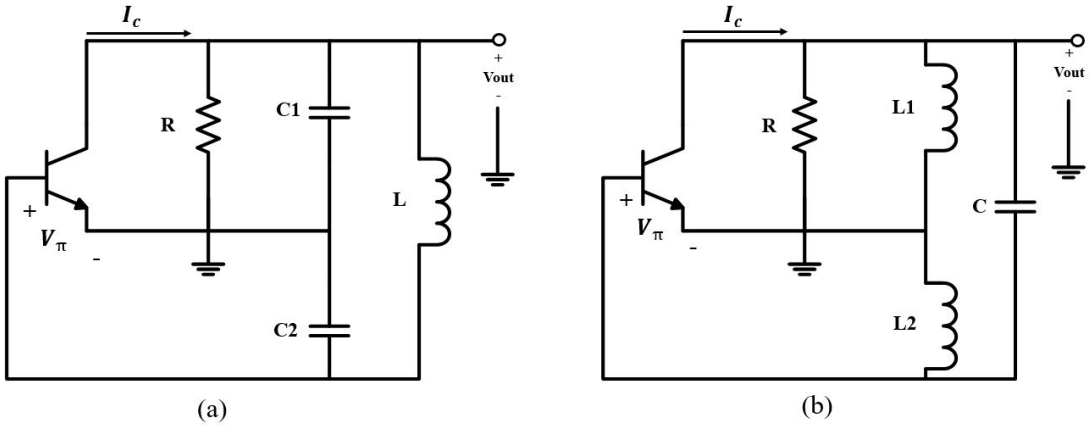


Figure 2.4 a) Colpitts b) Hartley Oscillator

2.1.1.2 Colpitts and Hartley Oscillators

The schematic of the Colpitts and Hartley oscillators is given in Fig.2.4.The feedback is achieved by using capacitive or inductive voltage dividers, and R represents the parasitic tank resistance. Both topologies use a parallel LC resonator circuit connected to the collector and base. Between these topologies, the Colpitts oscillator is favorable in integrated applications since the Hartley oscillator requires two inductors, leading to large area occupation. It can be seen that both circuits are generating a collector current in the shown direction in Fig.2.4 due to base-emitter voltage generated with voltage division. In order to understand how these circuits provide the oscillation condition, a small-signal model of the Colpitts oscillator is taken under investigation, as shown in Fig. 2.5. Parasitics capacitances and input resistance r_π are neglected for simplicity. Afterward, the node equation at the collector node is written as (2.4).

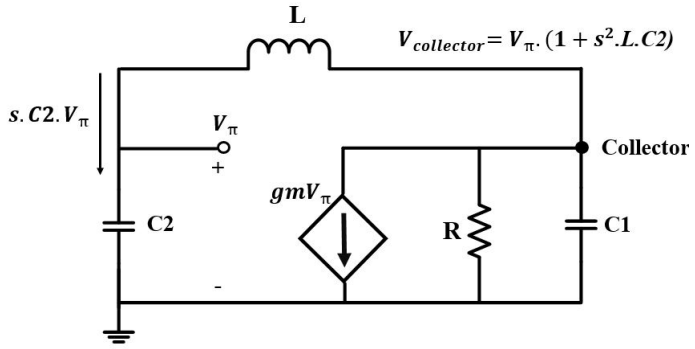


Figure 2.5 Colpitts Oscillator Small Signal Model

$$sC_2V_\pi + g_mV_\pi + (\frac{1}{R} + sC_1) \cdot (1 + s^2LC_2) \cdot V_\pi = 0 \tag{2.4}$$

By eliminating V_π, since it is a non- zero value, (2.4) rewritten as (2.5) where s = jω, putting the imaginery components and the real parts together.

$$\left(g_m + \frac{1}{R} - \frac{w^2 L C_2}{R}\right) + j[w(C_1 + C_2) - w^3 L C_1 C_2] = 0 \tag{2.5}$$

Making the imaginary part 0, at resonance frequency, gives the oscillation frequency w_0, (2.6)

$$\omega_0 = 1/\sqrt{L \cdot (\frac{C_1 C_2}{C_1 + C_2})} \tag{2.6}$$

$$g_m R = C_2/C_1 \tag{2.7}$$

Plugging in the w_0 into (2.5), the real part of the equation denotes the equality given in (2.7). This tells us that the gain of the system from the base to the collector has to be equal to the inverse of the voltage division ratio (C_1/C_2). In order to ensure oscillation to start, gmR should be larger than C_2/C_1, thus satisfying the minimum unity gain requirement and sustaining the oscillation. Considering the C_2 is generally twice as large as the C_1 gmR should be larger or equal to 2.

2.1.1.3 Cross Coupled (CC) Oscillators

The cross-coupled topology is the first choice in RF applications due to its robust operation (Razavi, 2011). It is formed by two transistors connected in the differential configuration, and each transistor has a parallel LC resonator, as shown in Fig.2.6a. The critical feedback is achieved by combining the base of one transistor with the other one's collector. Due to its differential nature, the tank circuitry can also be designed differential; Fig. 2.6b shows the tank where 2Rp represents the total parallel tank resistance. The oscillation will start when the negative resistance Z_1 is introduced to the tank circuit and will be larger than the parallel tank resistance in magnitude. The oscillation condition can be calculated by connecting a voltage source to get the negative resistance value as shown in Fig.2.6c and comparing it with Rp at the tank resonance frequency, where $V_X = V_2$- V_1. These calculations are made assuming that the cross-coupled transistors are ideally achieving complete switching, and one is forward biased while the other is off.

$$I_X = g_{m1} \cdot V_1 = -g_{m2} \cdot V_2 \tag{2.8}$$

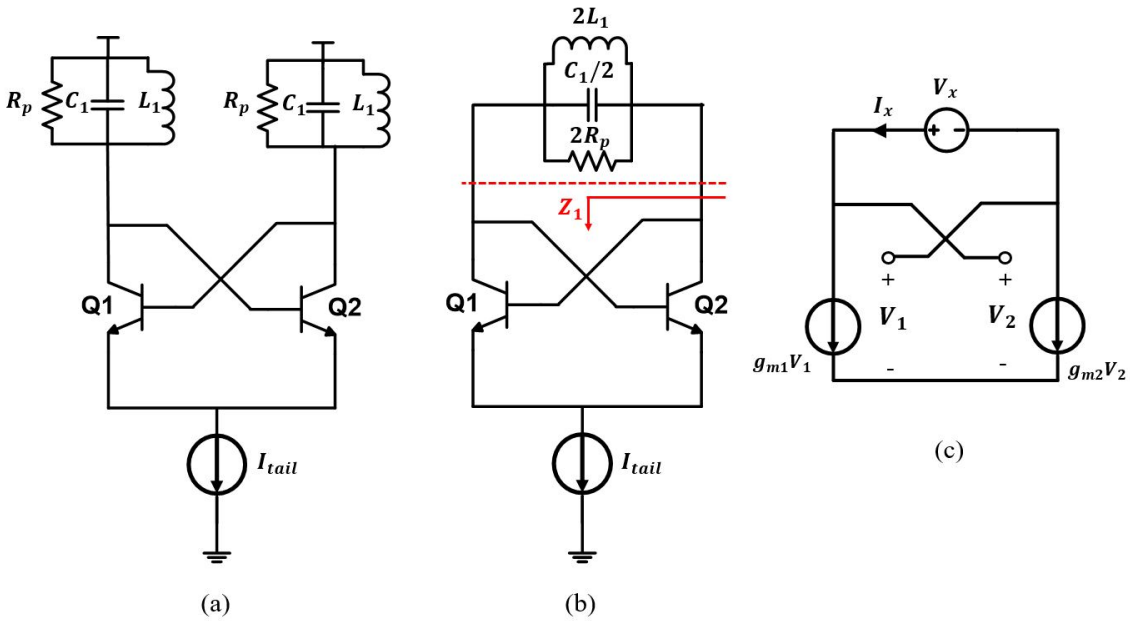


Figure 2.6 a) General CC topology b) Differential Tank Circuit c) CC pair negative impedance calculation

$$I_X = g_m1 \cdot V_1 = -g_m2 \cdot V_2 \tag{2.9}$$

Using the Relation of $V_X = V_2 - V_1$

$$\frac{V_X}{I_X} = -\left(\frac{1}{g_m1} + \frac{1}{g_m2}\right) \tag{2.10}$$

The transistors are identical devices thus $g_{m1} = g_{m2} = g_m$, and comparing the negative impedance's magnitude with the tank resistance $2R_p$, we will then get the oscillation condition. as given in (2.11)

$$\frac{2}{g_m} \leq 2R_p \;\; \rightarrow g_m R_p \geq 1 \tag{2.11}$$

The cross-coupled topology provides a better start-up condition compared to Colpitts but requires higher power consumption and is more prone to noise due to increased device parasitics. However, a comparison between CC and Colpitts's oscillators designed with HBT transistors showed that CC could have identical or even better PN performance (Fard & Andreani, 2007). Due to its advantages, cross-coupled topology was selected to implement the VCO of interest in this work.

2.1.2 Oscillator Performance Parameters

The requirements expected from an oscillator can be divided into system and interface specifications. The first group includes requirements such as the generated signal's purity, frequency tunability, and the system's linearity. The 2nd group of requirements is the oscillator's driving capability and output voltage swing. Since the oscillators are driving many blocks in the system, such as mixers in TRX modules and dividers in PLLs, they should provide sufficient swing and power to maintain the operation of those blocks. The next sections will briefly explain the system requirements and their effects on performance.

2.1.2.1 Phase Noise

Phase noise is the widening deviation of the VCO spectrum from an impulse due to random fluctuations in the VCO output frequency due to non-ideal elements, as shown in Fig.2.7.

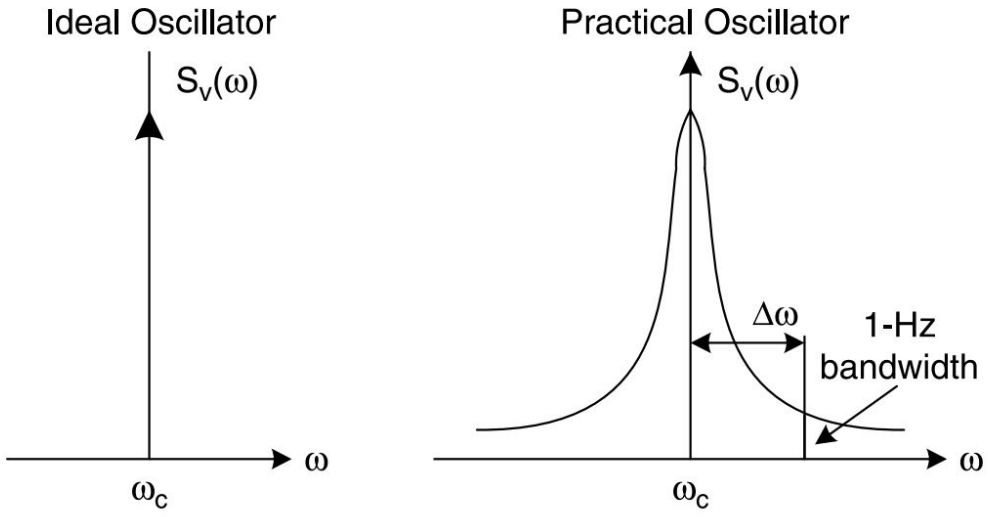


Figure 2.7 The broadening of an impulse due to Phase Noise

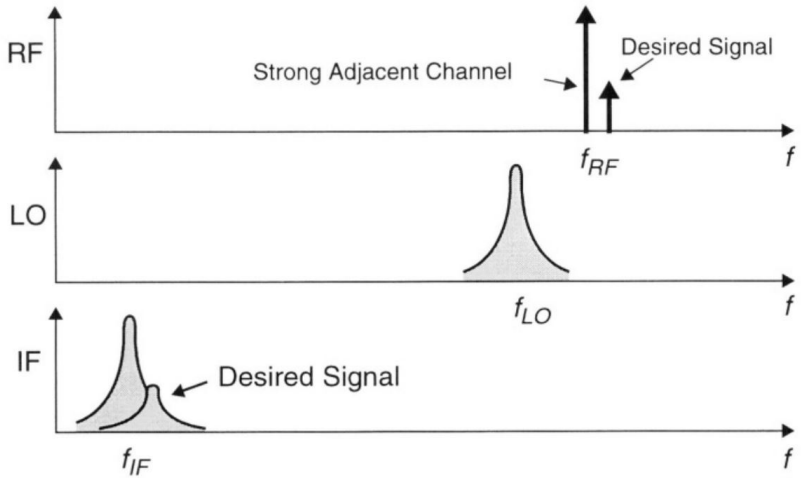


Figure 2.8 Example of PN Effect in Receivers in the presence of Strong Adjacent Channel (Hajimiri & Lee, 1999)

The effect of the phase noise on 5G communication systems is explained in Section.1.2, and to picture its impact, a receiver, for instance, Fig.1.3b., can be examined. Suppose the system tunes to a weak signal accompanied by a strong adjacent channel, as shown in Fig. 2.8. If the LO has a significant phase noise, the downconversion of the strong interferer to the IF frequency where the desired signal has the effect as shown in the IF graph in Fig. 2.8. The resulting interference considerably lessens the system's dynamic range; therefore, phase noise performance is crucial, and decreasing it will directly increase the SNR of the desired signal (Hajimiri & Lee, 1999).

2.1.2.2 Frequency Tuning and VCO Gain K_{VCO}

The frequency tuning in the RF oscillators is essential for their implementation in communications systems. The LO signal should be tunable in order to operate at different channels. The term "voltage controlled" originates from tuning the output frequency by adding a component that changes the output frequency as a function of voltage. In LC oscillators, this component is a variable capacitor (Varactor-Varicap). This component changes its capacitance value by changing the control voltage, thus changing the oscillation frequency. However, this device employs non-linearities; its capacitance does not change linearly, so they should be operated where they have the most linear behavior. Moreover, this linearity is directly correlated with the VCO's PN performance (Rogers et al., 2000). The linearity of the VCO is represented by VCO gain K_{VCO}, and the oscillation frequency can be represented by (2.12), where $V_{control}$ is the varactors control voltage.

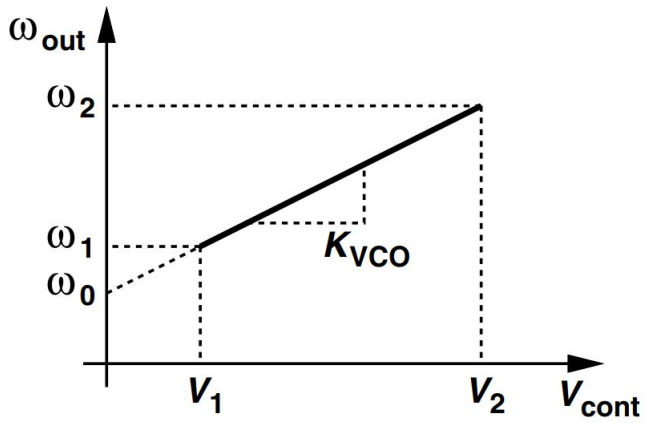


Figure 2.9 VCO Gain Characteristics

$$\omega_{\text{osc}} = \omega_0 + K_{\text{VCO}} \cdot V_{\text{control}} \tag{2.12}$$

The VCO gain stands for the sensitivity of the VCO, which highly depends on the varactor linearity. It is defined as a change of frequency per voltage, which is the varactor's control voltage. $\text{K}_{\text{VCO}} = \partial\omega_{\text{osc}}/\partial V_{\text{control}}$ and the unit is Hz/V. The graphical representation is shown in Fig. 2.9.

Although the varactor provides a certain tuning range since they have limited variability, they are not enough to satisfy the extensive frequency range by itself. In order to enhance the tuning range, a discrete tuning can be added to the tank circuit by controllably adding a capacitor to the tank with the help of switches. First of the main issues implementing these switched capacitors is that the parasitics introduced to the tank by the switches will increase the phase noise; secondly, the capacitor banks should be arranged such that the whole frequency range will be covered and there will be no blind zones in the tuning range as shown in Fig. 2.10, (Razavi, 2011). Detailed implementation of the capacitor banks is covered in Section.4.1.3.

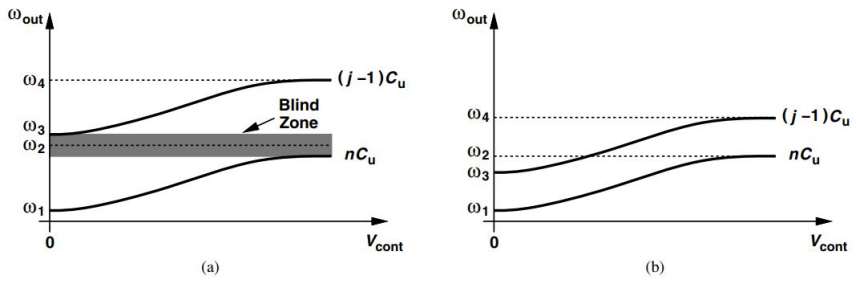


Figure 2.10 a) Frequency Tuning Curves with Blind Zone b) Proper Implementation of Discrete Tuning (Razavi,2011)

2.2 PLL Fundamentals

2.2.1 Analog Charge Pump PLL

This system is not fully analog. It is called analog since the structure is mainly based on analog elements. The two main topologies, Integer-N and Fractional-N, are only different from each other in terms of the way they implement the frequency division. The general topology of the analog CP PLL is shown in Fig. 2.11. The first building block of PFD is a digital circuit. It detects frequency when there is a significant phase difference or, in other words, the frequency difference between the divided VCO output and the reference signal. Secondly, it operates as a phase detector when the input frequencies are almost equal. In the end, PFD generates a signal that represents the phase error. In Type-I PLLs, the output of the PFD can be directly fed into VCO via the loop filter as a control voltage, but in Type-II PLLs, a charge pump is introduced. As a second integrator, CP and LF cancel out the static phase error together (Razavi, 2020); thus, unwanted sidebands are minimized. The digital output of PFD/CP (pulse signal) can not be directly fed into the VCO as control voltage; in that case, the output frequency will flip from one to another, which will cause spuriousness in the output. In order to prevent this error, the generated charge pump pulse signal is transferred to the loop filter, which is essentially a low pass filter. It will cancel out the high-frequency components and make the control signal as constant as possible. The high-frequency output of the VCO is converted to lower frequencies, close to the reference signal level, either by an Integer-N or Fractional-N divider circuit. In order to prevent fractional spurs, the fractional-N circuit requires extra circuitry called a delta-sigma modulator ($\Delta\Sigma$).

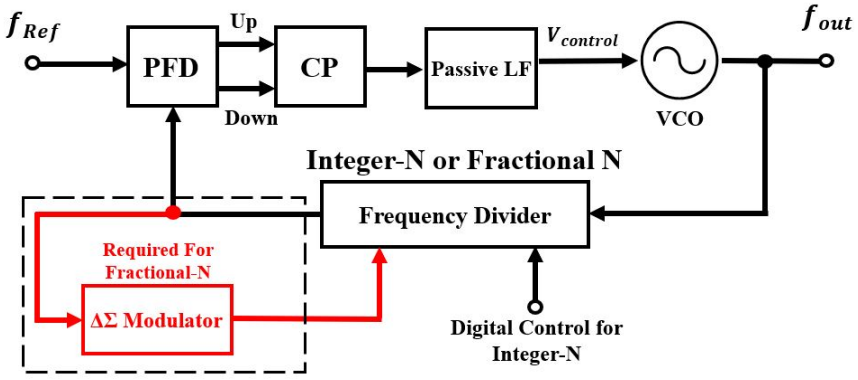


Figure 2.11 Block Diagram of Analog CP PLL

2.2.2 Digital PLL

In telecommunication bands like GSM, channel spacing is very narrow (200 kHz) compared to 5G applications, and this narrow channel spacing requires a low cut-off frequency for the loop filter. If the LF is meant to be designed as a passive block, such a filter requires capacitors in the nF range that occupy an enormous silicon area. A highly intensive digital design approach for PLL has the considerable advantages of a high level of integration and low (Stazewski & Balsara, 2006). The digital PLL (DPLL) design's first step is implementing the digital domain's loop filter.

The digital filter occupies less area than its passive counterpart. Moreover, the absence of capacitors means that their leakage current is no more an issue. The digital filter also can be adjusted, and loop stability can be maintained for a broader range (Razavi, 2020). The implementation of this filter requires a digital input, which means the current generated by PFD/CP in analog PLLs due to the phase difference between the reference signal and the divided VCO. Furthermore, the digital output of the filter should be converted back to analog for continuous tuning of the oscillator. When the requirements of digital filter implementation are considered, certain modifications shown in Fig.2.12 should be conducted. The terminology "digital" does not state that all the building blocks are digital designs. The system's VCO and PFD still work with analog outputs and inputs. However, even the non-digital signals are digitized and can be expressed with bit signals (Best, 2007).

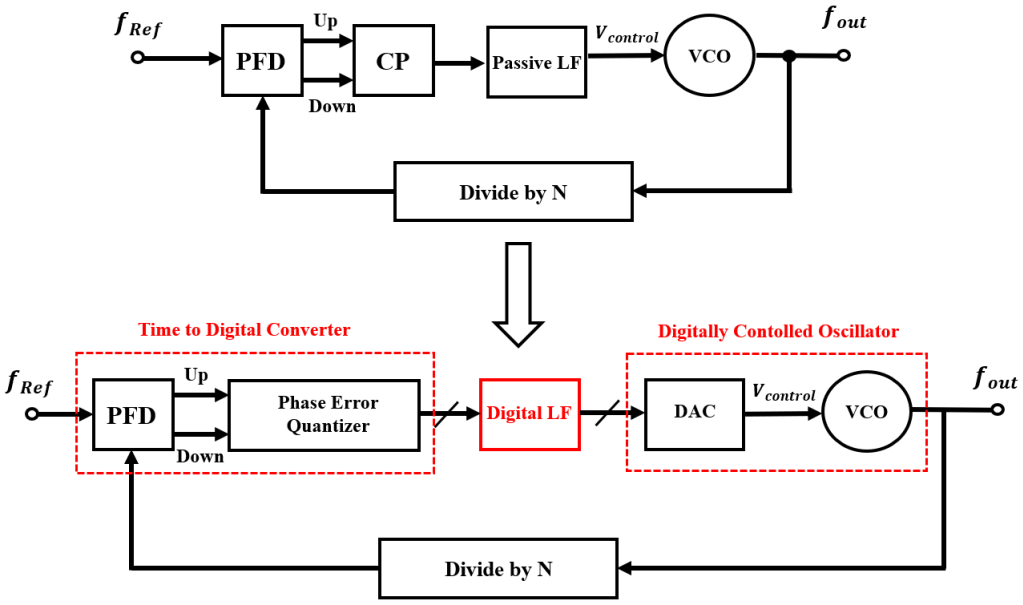


Figure 2.12 Digital PLL Building Block Comparing with the Analog PLL

Time to digital converter (TDC) combines the phase error quantizer and the PFD. The other modified block, a digitally controlled oscillator (DCO), combines a digital to analog converter and a VCO. The output of the PFD, phase error, is quantized with an analog to digital converter (ADC), and the output is fed to the loop filter. The digital output of the filter is passed through a digital to analog converter and an encoder to tune the oscillator's frequency. Finally, the loop divider design is the same as in the analog PLL. Although the system is called all-digital, TDC and DCO block still present weighty analog design challenges due to ADC, DAC, and VCO concepts (Razavi, 2020).

2.2.2.1 Comparison of Digital and Analog PLL

The main idea for both PLL architectures is the same; however, they started to differ where the analog PLL and the DPLL convert the phase error in the loop differently. Analog PLL turns the phase error into the current while DPLL converts it to the digital sequence. For instance, due to this conversion, the type of the filter is changed, which will affect the performance in terms of area and settling time.

Up to this date, analog PLLs are superior to DPLLs in terms of phase noise performance. There are some counterexamples (Yao et al., 2017), but this design uses extensive analog assistance to suppress the noise. Table.2.1 proves this statement, an analog PLL design almost twenty years ago (De Muer & Steyaert, 2002), but still, the recent state-of-the-art DPLLs (Yoo et al., 2021) are not as good as analog PLLs in terms of phase noise performance. On top of that, it is easier to optimize analog PLL since it is based on well-developed techniques and established standards. Due to their excellent phase noise performances and reliability, analog PLLs are still strictly used in 4G and 5G telecommunication applications.

Table 2.1 Comparison of Different State-of-The-Art DPLL Designs in Literature with an Analog PLL

	(De Muer & Steyaert, 2002)	(Yoo et al., 2021)	(Huang et al., 2014a)	(Huang et al., 2014b)
Phase Noise dBc/Hz	**-139 <@3MHz**	**-132 @10 MHz**	**-109.32 @10 MHz**	**-100.92 @10 MHz**
f0 (GHz)	**1.8**	**2.4**	**2.4**	**1.6**
Type	**Analog**	**Digital**	**Digital**	**Digital**

2.2.3 Linear Modelling of Type-II Analog Charge Pump PLL

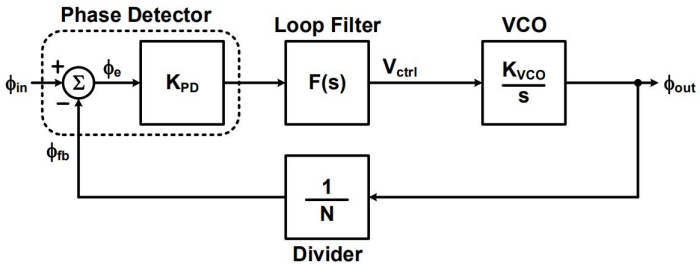


Figure 2.13 Linear Model of PLL

Linearized or small signal models shown in Fig.2.13 are valuable tools for understanding PLL dynamics, where the variable of interest is the phase. Basically, it explains how the oscillator's output phase responds to the different stimuli applied throughout the loop. It should be noted that the small signal model does not cover the whole behavior of the PLL; for that purpose, a non-linear time domain model is required. However, the linear model is helpful if the PLL is locked or near locked and gives an estimated understanding of the PLL's performance. In order to understand the whole system, each building block should be investigated individually. Transfer characteristics of each block are explained below.

Phase Frequency Detector & Charge Pump: The phase detector catches the phase difference between the input and feedback clock. This phase difference can be represented as $\Delta\Phi$ and generates an error voltage $v_e(t)$ at its output correlated to the average phase error. The PLL responds to this average error, and the change of this average $v_e(t)$ with respect to the phase error gives the PD gain K_{PD}. Ideally, the average PD gain is equal to $1/2\pi$, and its unit is rad^{-1}. The ensuing block CP, shown in Fig. 2.14 together with LF, converts the PFD output signals to units of charge that will be applied to the loop filter. Depending on the phase error, CP will either charge or discharge the filter, and the amount of the charge is proportional to PFD pulse widths. Larger phase errors will end up as larger pulse widths. The gain of the CP is the current that it generates, I_{CP}. In the linear model, the PD and CP blocks are combined, and their total gain is given in (2.13) as the new K_{PD}. Ultimately, the PFD/CP product is fed to the impedance filter (loop filter) and generates the control voltage of the VCO.

$$Total\ PFD\ \&\ CP\ Gain = \frac{I_{CP}}{2\pi}\ (\frac{Amps}{rad}) \tag{2.13}$$

Loop Filter: The filter extracts the average of the phase detector error pulses and generates the control voltage for the VCO. For stability purposes, a big capacitor at

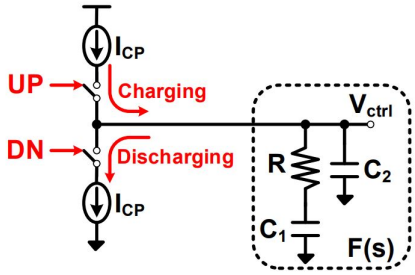


Figure 2.14 Charge Pump Operation with Loop Filter

the output can not be applied to achieve an actual average; thus, it is required to provide proportional gain to stabilize the loop in the form of a resistor in the filter, as shown in Fig.2.14. Moreover, the additional C2 capacitor is added to filter out the spurs. The transfer function, F(s), of this 2nd order filter is given in (2.14).

$$F(s) = \frac{(\frac{1}{C_2}) \cdot (s + \frac{1}{RC_1})}{s(s + \frac{C_1 + C_2}{RC_1C_2})} \tag{2.14}$$

Voltage Controlled Oscillator: VCO in the loop is being tuned by a control voltage, and it is producing an output phase accordingly. The critical element of the VCO in linear modeling is the VCO gain K_{VCO}, explained in Section 2.1.2. VCO is one of the integrators in the loop, and the mapping of its transfer function in the time domain is shown in (2.14). Due to the integration, the VCO behavior as in the Laplace Domain Model is represented as K_{VCO}/s

$$\phi_{\text{out}}(t) = \int K_{\text{VCO}} v_{\text{control}}(t) dt \tag{2.15}$$

Loop Divider: The divider is dimensionless in the linear model and its effect on the output phase and feedback phase is as follow: $\phi_{\text{feedback}}(t) = 1/\text{N}\ \phi_{\text{out}}(t)$

If the complete closed-loop transfer function is considered, which is the output phase over the input phase, the end result denotes third-order low pass transfer characteristics shown in (2.16). This function has a single zero coming from the resistor at the filter and two poles, one from the VCO and the other from the second-order filter.

$$H(s) = \frac{\phi_{\text{out}}(s)}{\phi_{\text{in}}(s)} = \frac{\frac{K_{\text{PFD}}K_{\text{VCO}}}{C_2}\left(1 + \frac{1}{RC_1}\right)}{s^3 + \left(\frac{C_1+C_2}{RC_1c_2}\right)s^2 + \left(\frac{K_{\text{PFD}}K_{\text{VCO}}}{NC_2}\right)s + \left(\frac{K_{\text{PFD}}K_{\text{VCO}}}{NRC_1C_2}\right)} \tag{2.16}$$

3. Design of TYPE-II 4th Order Integer-N PLL-Based Frequency Synthesizer

The frequency synthesizer of interest will be implemented in a sliding-IF architecture which is favored for improved image rejection and less LO distribution challenge. The proposed project aims at the European mmWave 5G bands defined between 24.25-to-27.35 GHz. For this reason, the frequency synthesizer should generate a LO signal with a frequency range from 9 to 12 GHz with a 100 MHz reference signal. The targeted phase noise performance at 1 MHz offset is -120 dBc/Hz at 1 MHZ offset. The phase noise level is critical for the SNR performance of 5G systems; thus, a challenging phase noise level was selected for the design, and there is no similar example in the literature. Furthermore, the synthesizer aims to achieve the PN performance with 150 mW power consumption and a 3 mm^2 area. The other crucial performance parameters related to PLLs stability, settling time, and noise contribution in the synthesizer related to PFD, CP, and LF are in Table.3.1. The charge pump current mismatch is crucial for the system's noise performance, so it should be minimized. Furthermore, because it is directly correlated to the frequency tuning range and has the most significant PN contribution to the system, target VCO parameters are also given in the same table. The VCO should employ a phase noise lower than -120 dBc/HZ since the other loop components will affect its noise performance. Considering the VCO and the divider are the most power-hungry blocks in a PLL, VCO's power consumption should be minimized by at least one-fourth of the power budget of 150mW. In order to be able to operate in the 26 GHz band, the output of the VCO should be multiplied with a doubler and divided by a single CML 2/3 cell, as explained in Section 3.2 to operate at the 26 GHz band.

In order to achieve the mentioned goals, a Type-II fourth order integer-N PLL-based frequency synthesizer will be designed using 0.13 μm SiGe BiCMOS technology. The reason behind the selected technology is, that the features of the developing SiGe BiCMOS technology make it possible to implement circuit architectures with various fields of applications on a single chip without sacrificing the performance in 5G systems. In this chapter, the detailed design steps and the post-layout simula-

tions of each sub-block of the Type-II fourth order integer-N PLL-based frequency synthesizer are shown in Fig. 1.8 are presented. On top of it, the system integration of the PLL and its behavioral model was also examined. The comparison of the target specifications of the synthesizer with state-of-the-art design in the literature is given in Table.3.2

Table 3.1 The Target Specifications of the PLL and VCO in the System

PLL System Specifications	**Target Values**
Phase Noise	**-120 dBc/Hz @1MHz**
Tuning Range	**9-12 GHz**
Loop Bandwidth	**1 MHz**
Phase Margin	**45**
Settling Time	**1 μs**
PFD Phase Shift	**% 1<**
Charge Pump Current	**1mA**
CP Current Mismatch	**%1 <**

VCO Specifications	**Target Values**
Phase Noise	**-120 dBc/Hz <@1MHz**
Tuning Range	**9-12**
Power Consumption	**40<**
Tuning Range	**28.57**

Table 3.2 Comparison Table of Targe Specifications and State-of-The-Art Frequency Synthesizers

	Technology	***Frequency (GHz)***	***TR (%)***	***Phase Noise (dBc/Hz @1MHz)***	***Power Consumption (mW)***	***Reference Frequency (MHz)***	***Area (mm)***	***FoM***
(Li vd., 2014)	65nm CMOS	20.6 - 48.2*	80.2	-108	148	100	2.1	195.1
(Tired vd., 2016)	180nm SiGe	24.6 - 27.8	12.2	-107	56.7	1750	1.34	179.6
(Ferriss vd., 2014)	120nm SiGe	20.5 - 24.9*	19.2	-116	115	155.52	1.23#	188.2
(Osorio vd., 2011)	40nm LP CMOS	21.4 - 25.1	15.9	-103	64	390	0.1	176.3
(Hekmat vd., 2015)	65nm CMOS	25-30	18	-107	87	N/A	1.8	181.5
Frequench Synthesizer of Interest (Target)	130nm SiGe	18-24*	28.6	-120	150	100	3	193.8

*Requires Frequency Multiplication
#External Loop Filter
FoM = -$\mathcal{L}(\Delta\omega)$ + $20log(\frac{f}{\Delta f})$ - $10log(\frac{DCPower}{1mW})$ + $10log(\frac{TR}{10})$

3.1 Design of C-C Pair LC VCO Design with Varactor Linearity Control

Two versions of VCOs are designed in this study. In order to emphasize the distinction between them, the first version is named 3-bit VCO, and the second one is named 4-bit VCO, depending on their required control for the capacitor banks. Also, they are distinctive in terms of their layout designs; 3-bit VCO is realized for flip-chip assembly, while 4-bit VCO is designed for wire-bonding. Moreover, although identical topologies are used for the core circuit and buffers, optimizations and improvements have been made for the 4-bit VCO.

The design flow of the VCOs begins with adjusting their tail current to obtain the largest output swing possible while not exceeding the power budget to optimize the PN performance. Later the tank inductor quality factor should be maximized while its value is minimized (Niknejad & Hueber, 2019). Since the inductance is minimized, the tank capacitance should be tuned to achieve desired oscillation frequency and the tuning range. The varactor that allows continuous tuning is a non-linear device; thus, it should be operated under optimum biasing conditions. This work uses a varactor linearity control mechanism to manipulate the trade-off between the TR and PN. Furthermore, in order to achieve a more extensive tuning range, capacitor banks are added to the circuit, and finally, buffers are implemented to have an interface between the subsequent stage and the VCO's core. The following sections present the detailed design steps and the differences between the versions in the respective stages. The schematic of the proposed bias decoupled CC oscillator, based on (Sadhu et al., 2018), is shown in Fig.3.1. Identical Q1 transistors connected with a positive feedback configuration to achieve a negative impedance parallel to tank circuitry, and Q2 acts as a current source. The C_d capacitor decouples the tank bias from the base bias of the Q1 transistors so that the collector and the base biasing of the transistors can be adjusted separately, and higher amplitudes; thus, better phase noise performance can be achieved without affecting the mode of operation of the transistors.

3.1.1 Tail Current Adjustment for Optimum Phase Noise

On top of the topology used for the core, biasing of the tail current source transistor, or setting the tail current, plays a critical role in phase noise performance. Theoretically, Leeson's phase noise model shown in (4.1) shows that a higher carrier power, P_{sig}, will lead to better PN performance.

$$\mathcal{L}(\Delta\omega) = \frac{2FkT}{P_{\text{sig}}}\left(1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right) \tag{3.1}$$

The tank amplitude V_{tank} can be calculated approximately as $R_{tank} \cdot I_{tail}$ assuming the complete switching of the transistors. This operation region is called the "current limited regime" since the amplitude is only specified by tank impedance and tail current; however, it will not apply when the amplitude gets close to VDD and puts the core transistors in saturation operation, which is called voltage limited regime (Hajimiri & Lee, 1999). Ideally, VCO should be biased at the edge of the

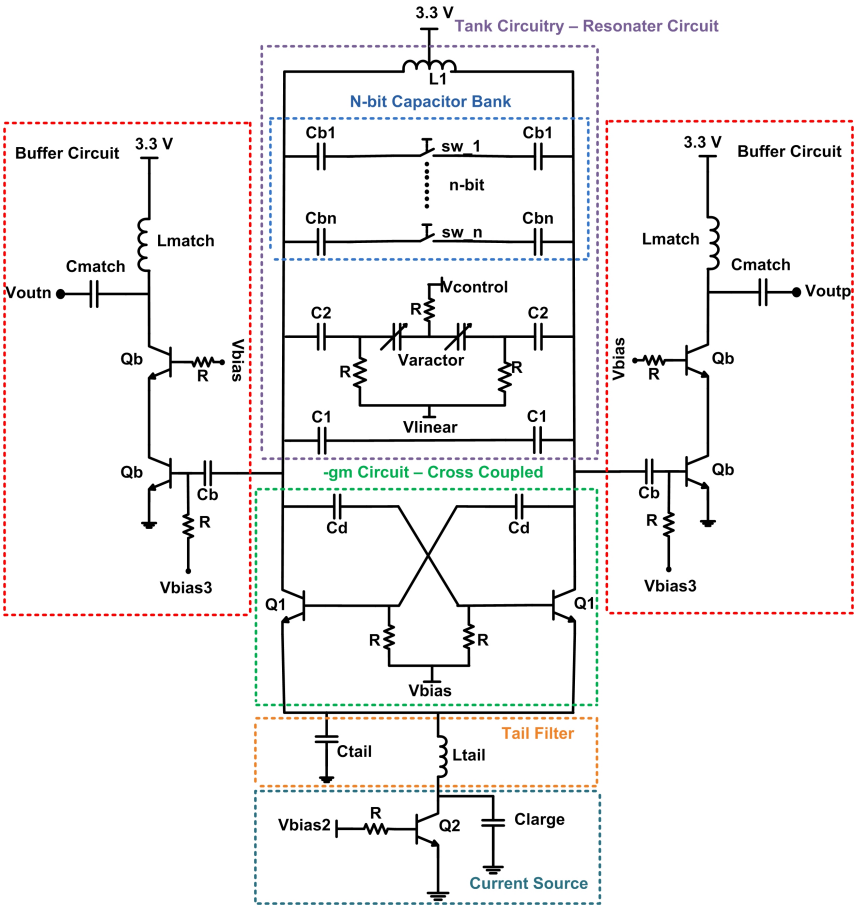


Figure 3.1 Schematic of the Designed VCO

voltage-limited region, slightly into the voltage regime, to prevent the PVT effect for optimal performance. Further increase of the tail current will derive VCO operation to voltage-limited region, where increasing tail current for lower PN will be a waste of power. Representations of these regions are shown in Fig.3.2(a). In order to find the desired biasing point for the optimum operation, tail current bias was swept versus output power. It is observed that the point for this 3-bit VCO should be 815 mV, while it is 820 mV for the 4-bit VCO, as shown in Fig.3.2(b) and Fig.3.2(c), respectively.

It is expected that the PN graph should have a decreasing behavior with the increasing current; on the contrary, it was observed in the simulation results that increased tail current causes a sharp rise in phase noise after a certain point lower than 815mV. This behavior occurs due to the low-frequency noise from the current source transistor; when the output swing gets larger, the cross-coupled Q1 transistors operate as a mixer and upconverts the tail noise near the carrier. It is experimentally verified that this noise contributes not only to amplitude modulation noise but also to phase noise, unlike the conventional circuit analysis (Samori et al., 2000). The input impedance and the switching time of the Q1 transistors depend on the tail

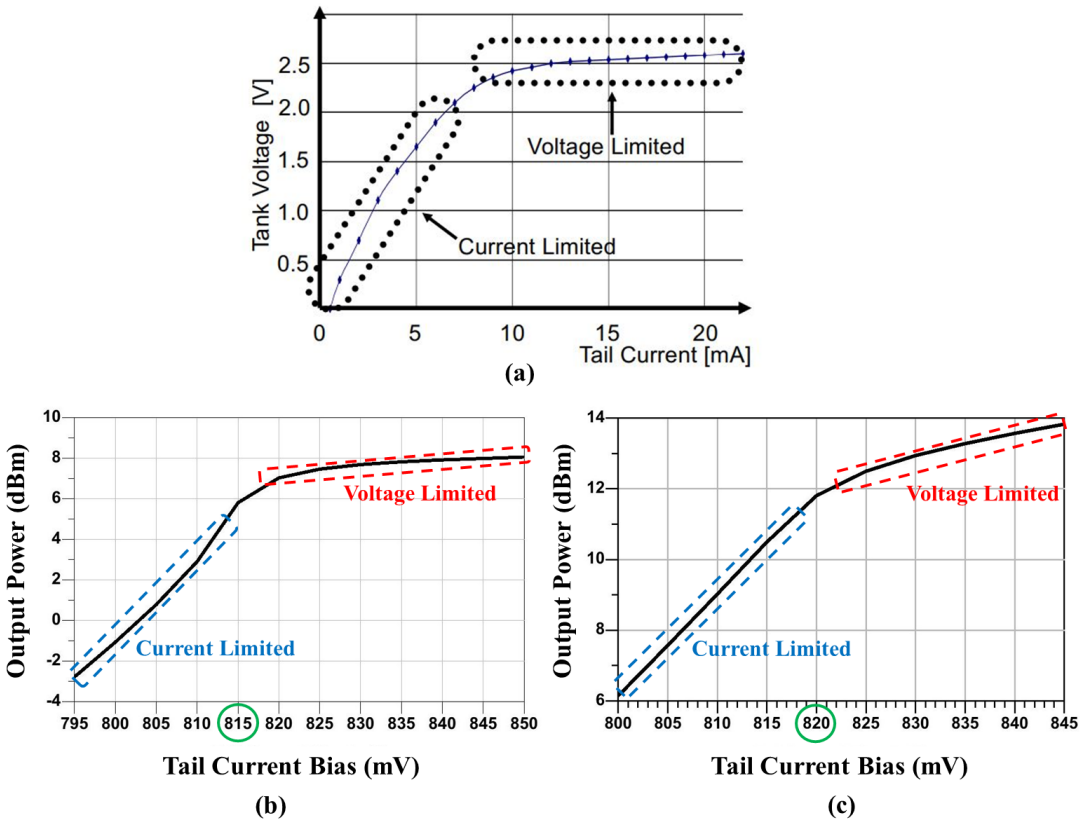


Figure 3.2 (a) Example of Current and Voltage Limited Regions
Output Power vs. Current Source Bias Voltage for (b) 3-bit VCO (c)4-bit VCO

current and add a phase delay, $\Delta\theta_{\text{loop}}$, to the feedback. This delay causes the shift in oscillation frequency from the tank resonance frequency as given in (3.2).

$$\omega_0 = \frac{1}{\sqrt{LC}}\left(1 - \frac{\Delta\theta_{\text{loop}}}{2Q}\right) \tag{3.2}$$

Fig.3.3 shows that oscillation frequency reaches its maximum and decreases with the increasing current. A sensitivity coefficient $\mathrm{K_{Itail}} = |\,\partial\omega_0/\,\partial I_{\text{tail}}\,|$, and it becomes a limiting factor to the phase noise performance. Single Sideband to Carrier Ratio (SSCR) cited as PN, shown in (4.3) where α is rad/s and modifies it to (4.4) (Samori et al., 2000). Fig. 3.4 shows the corresponding PN change with the increasing tail current.

$$SSCR(\alpha)_0 = \frac{kT \cdot \omega_0 \cdot (1+F)}{C \cdot Q \cdot \alpha^2 \cdot (A_0)^2} \tag{3.3}$$

$$SSCR(\alpha) = \frac{1}{2} \cdot {K_{\text{Itail}}}^2 \cdot \frac{S_0(\alpha)}{\alpha^2} \cdot \Delta f \tag{3.4}$$

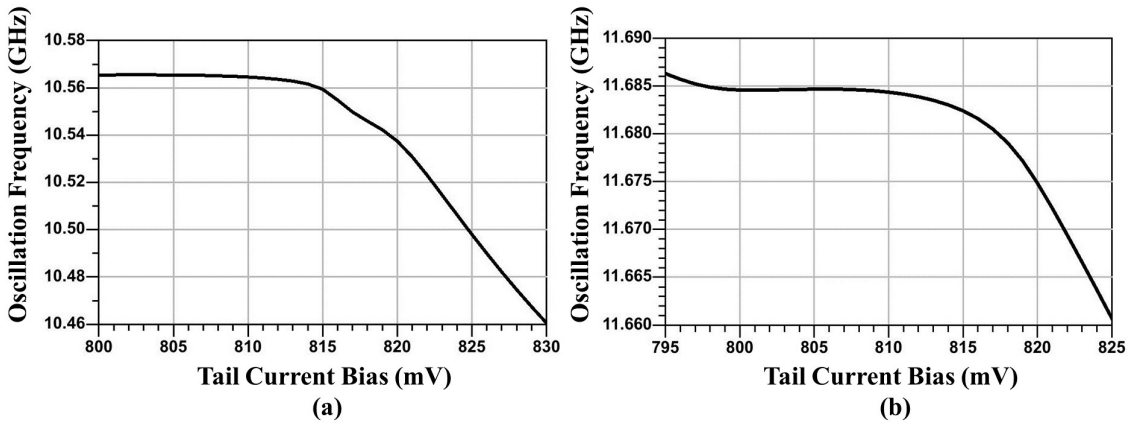


Figure 3.3 Change of Frequency with Tail Current
a) 3-bit VCO b) 4-bit VCO

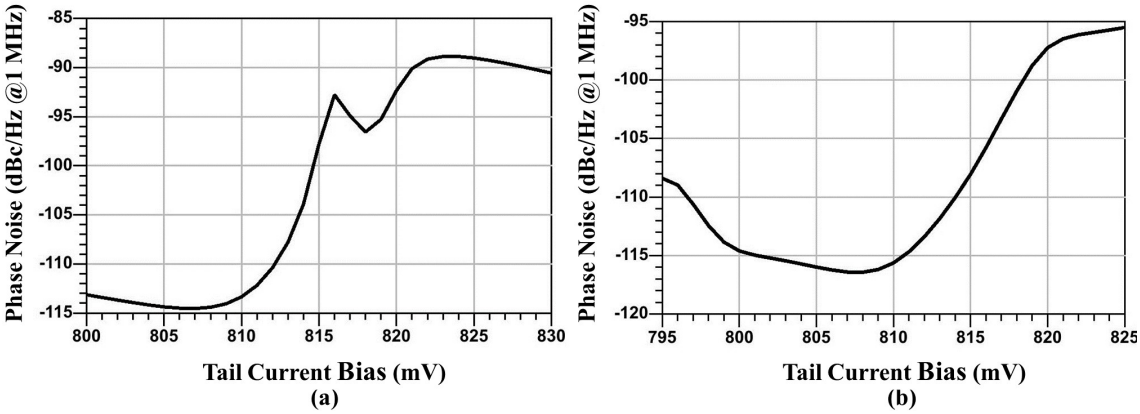


Figure 3.4 Change of PN with Tail Current
a) 3-bit VCO b) 4-bit VCO

In the light of the analysis of this behavior, the bias point of the current source transistor is selected as 805mV, where the best phase noise performance is achieved for both designs. Another outcome is that lower power consumption is achieved with the lower tail bias voltage. It should be noted that these values are for the case where all capacitor banks are closed. Depending on the capacitor bank configuration, the optimum bias point changes by a few mVs.

3.1.2 Tank Inductor Design

The LC design has the utmost importance in the VCO design. In equations (3.1) and (3.3), Q represents the overall tank quality factor which can be found in (3.5). LC oscillators can be taught as an energy transformation engine where active devices (cross-coupled transistors) alter energy from the supply to the resonator as an ac signal (Ham & Hajimiri, 2001). The larger the efficiency of this conversion, the less the phase noise; in other words, a higher quality factor directly results in lower noise. Therefore, a measure should be taken to maximize the tank quality factor. However, another critical performance parameter tuning range is affected negatively by higher quality factors; thus, the tradeoff between PN and TR should be handled carefully.

$$\frac{1}{Q_{\text{tank}}} = \frac{1}{Q_{\text{L}}} + \frac{1}{Q_{\text{C}}} \tag{3.5}$$

The bottleneck of designing an integrated resonator is that the passive devices, especially the inductors, in silicon technologies mostly have low-quality factors. The quality factor of the metal-insulator-metal (MIM) capacitors, provided by the IHP-SG13S technology, is much higher than the inductors, which typically have a quality factor of 20. The continuous frequency tuning component of the tank circuit, varactor, is an active component realized with thick gate oxide NMOS devices. The quality factor of the varactor is comparable with the inductors, but still, it has a Q of almost two times higher than the inductors in the desired operating frequency range, 9-12 GHz. Since the inductor is the limiting component, the overall tank quality can be estimated as follows; $\text{Q}_{\text{tank}} \cong \text{Q}_{\text{L}}$. The mentioned devices' quality factor comparison is shown in Fig.3.5. The inductors refer to the ones used for the 3-bit and 4-bit VCOs. Although larger inductors have higher quality factors, in theory, analyses showed that phase noise would increase with the square of the inductance value (3.6) (Ham & Hajimiri, 2001). In order to obtain the optimum performance, the inductance value should be minimized while its quality factor is maximized. Meanwhile, the capacitance at the tank should be increased to achieve the required oscillation frequency. For this sake, the C1 capacitors shown in Fig. 3.1 are added to the tank circuit.

$$\mathcal{L}(\Delta\omega) \propto \frac{L^2 \cdot I_{\text{tail}}}{{V_{\text{tank}}}^2} \tag{3.6}$$

IHP technology provides two thick metal layers optimal for routing and the inductance design. Furthermore, it provides optimized equilateral octogonal inductor designs. Using the largest routing width, 30μm, an inductor is generated using the

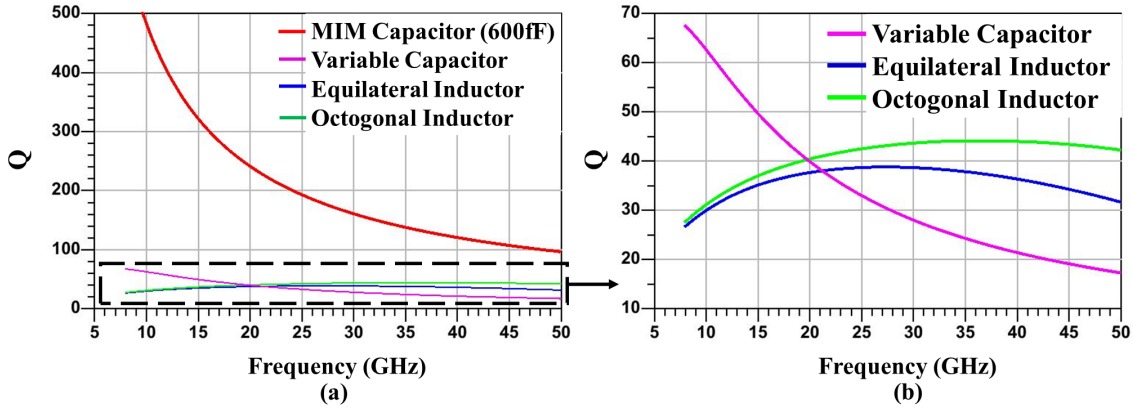


Figure 3.5 Quality Factor Comparison of Tank Components in the technology

TopMetal2 layer, shown in Fig.3.7(a); the quality factor achieved was 26 at 10.5 GHz; this design is named single layer. In order to increase the quality factor, an identical inductor in TopMetal1 is connected with multiple vias. Theoretically, the inductor's series resistance will be halved; thus, the quality factor will be improved. Fig. 3.7(b) shows the tank inductor design, named equilateral inductor, for the 3-bit VCO, stacked equilateral octagon geometry. The issue with the design is that the maximum size vias could not be placed in angled paths due to design rules provided by the IHP. Vias can only be placed with a 90-degree rotation. For the 4-bit VCO emphasizes modified octagonal inductor Fig. 3.7(c), the equilateral geometry is left, the 45-degree routings are minimized, and the via size can be maximized for the connection while the octogonal shape is kept. Also, the inner diameter of the second inductor is lowered, and its value is minimized. The lower capacitor is compensated by an extra capacitor bit added in the 4-bit VCO design. Fig.3.6a shows the quality factor comparison of the inductors mentioned and Fig.3.6b shows their inductance values.

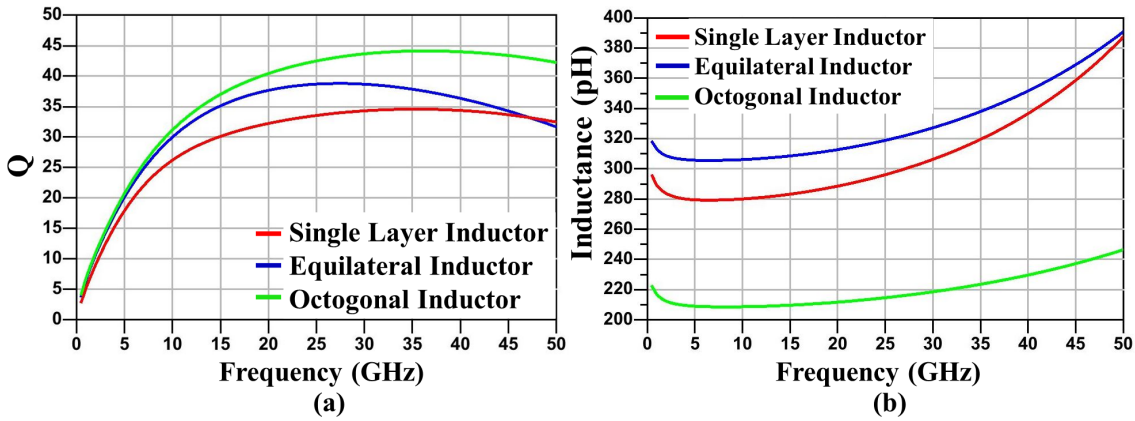


Figure 3.6 Comparison of the Inductors Under Investigation
a)Quality Factor b) Inductance

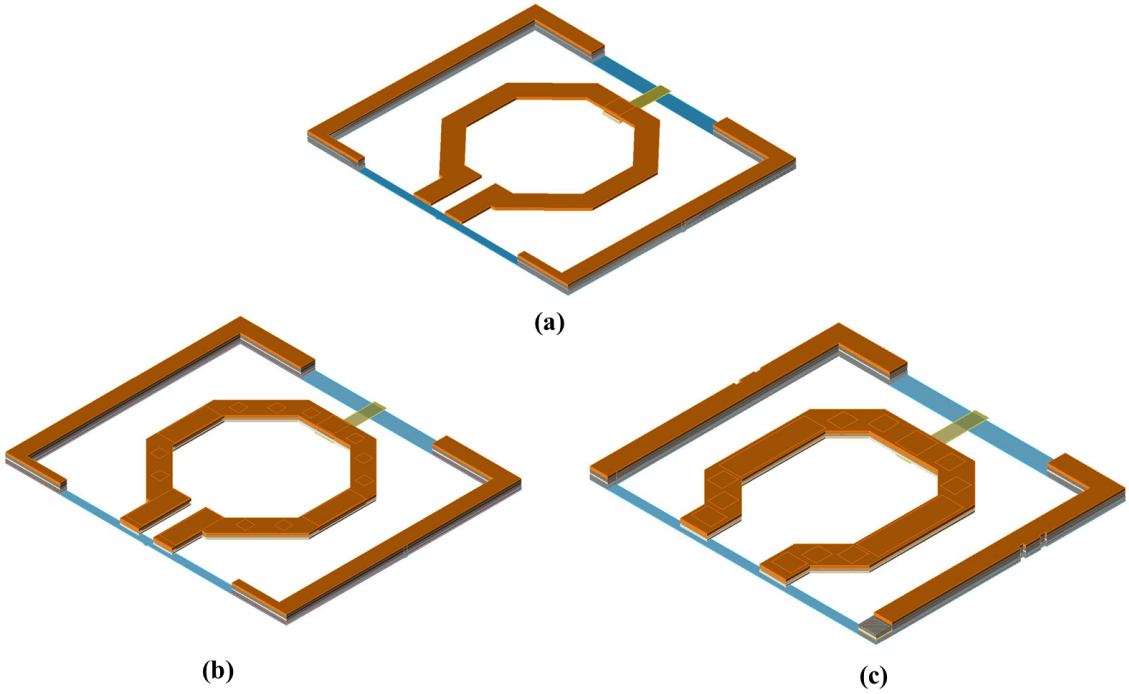


Figure 3.7 3D view of Inductor Designs
a) Single Layer b) Equilateral Inductor c) Octagonal Inductor

3.1.3 Varactor Linearity Control

The vital component of the tank circuitry, the variable capacitor (Varactor), is responsible for the continuous tuning of the oscillator. The varactor in IHPSG13S technology is realized with thick gate-oxide, and their layout is optimized to achieve maximum quality factor while achieving high C_{max}/ C_{min}. There have been further analyses and modeling of the varactor (Song & Shin, 2003; Chan et al., 2007; Bunch & Raman, 2003), but to recapitulate, they can be thought of as mos transistors whose source and drain are connected, and this connection generates a depletion region that can be controlled by voltage. The varactors in the design are operated in the accumulation and depletion mode, and their capacitance is adjustable with drain voltage shown as Vtune in Fig.3.8a; the device cross-section is given in Fig.3.8c.

Most commonly, the gate nodes of the varactor are directly connected to the Vdd of the tank circuit. In this work, by using C2 capacitors, these nodes are decoupled from the Vcc, and its biases on the gates are controlled externally. This allows to control the depletion region of the varactor and thus control its linearity. The Vlinear voltage shown in Fig.3.8b is controlling the depletion region, linearity and the C_{max}/ C_{min} of the varactor. Controlling the linearity directly allows for tuning the varactor's PN and TR trade-off and increasing capacitance change by keeping the quality factor degradation at a minimum. Fig.3.9(a) shows the quality factor

comparison with and without the linearity control method, where Vlinear is set as 1.7V. Furthermore, Fig.3.9(b) and (c) show how the capacitance change is enhanced. Method included C_{max}/ C_{min} is 1.6 while it is 1.05 without it. Furthermore, by using different Vlinear voltages, the required varactor linearity can be achieved, considering the quality factor and tuning range trade-off; Fig.3.10 shows the effect of Vlinear.

The effect of the linearity control method is experimentally shown by measurement results. The control voltage of the varactor is swept for the different Vlinear values, and the change of frequency is observed. The results are shown in Fig.3.11. The same behavior can be correlated with the results given in Fig.3.10b. The change of varactor capacitance with the control voltage also means a change of frequency in the same manner. In the design of both versions, Vlinear is chosen as 1.7V for optimal performance.

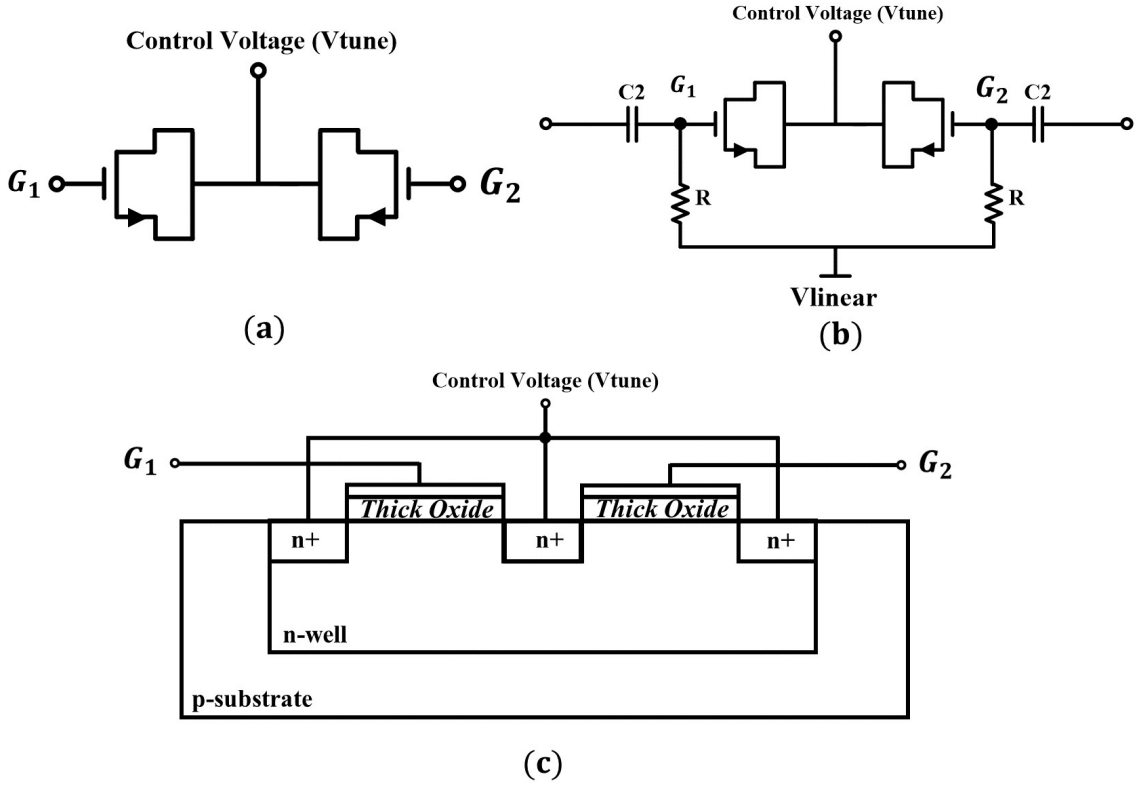


Figure 3.8 a) Basic Varactor Design b) Linearity Control Voltage Vlinear Connection c) Varactor Cross-section

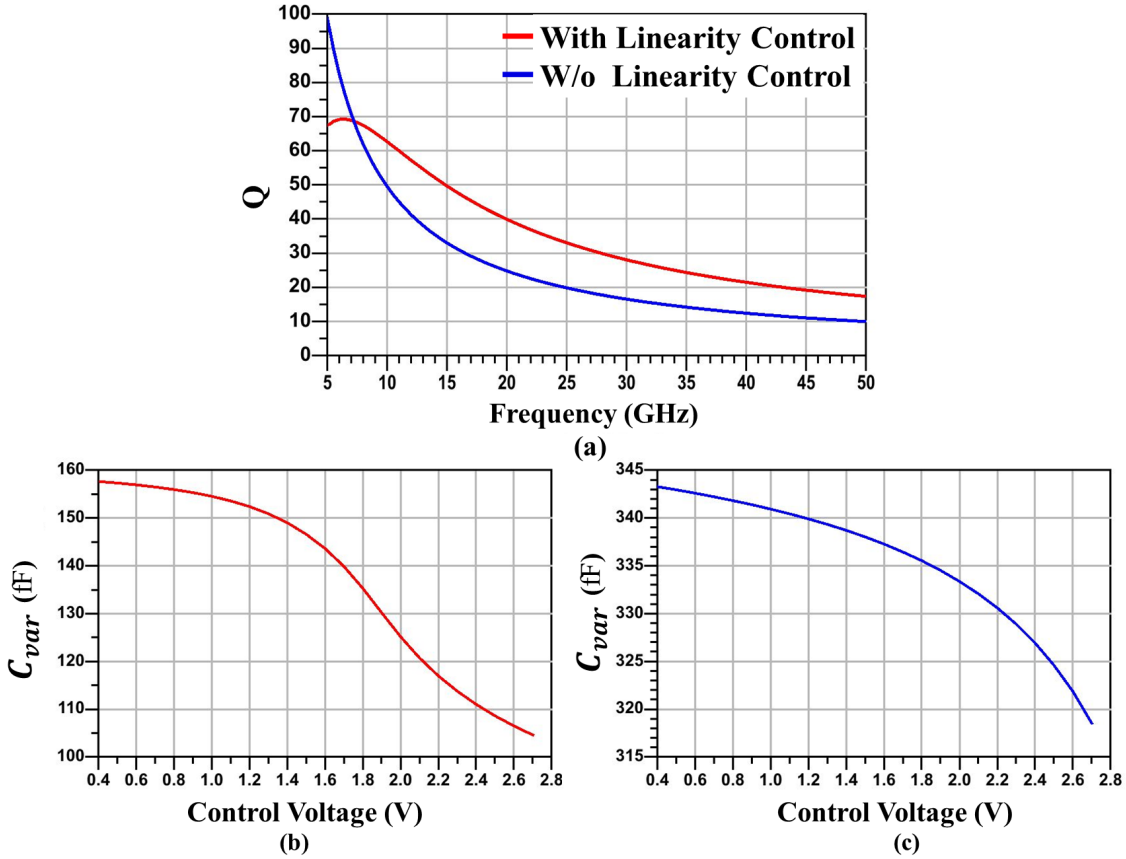


Figure 3.9 a) Effect of the Proposed method on Quality Factor Change of the C_{max}/ C_{min} b) With the Linearity Control, c) W/o the control

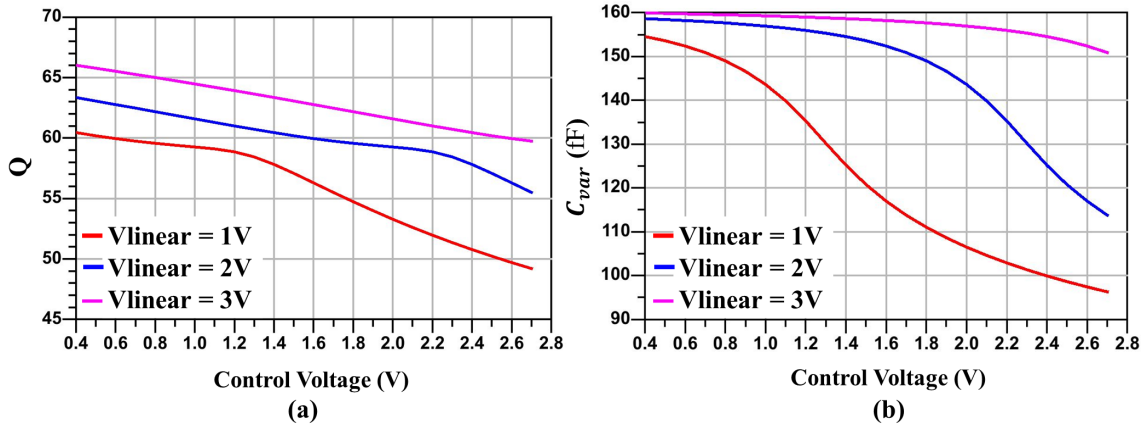


Figure 3.10 Effect of Different Vlinear Voltages on a) Quality Factor b) Change of Capacitance

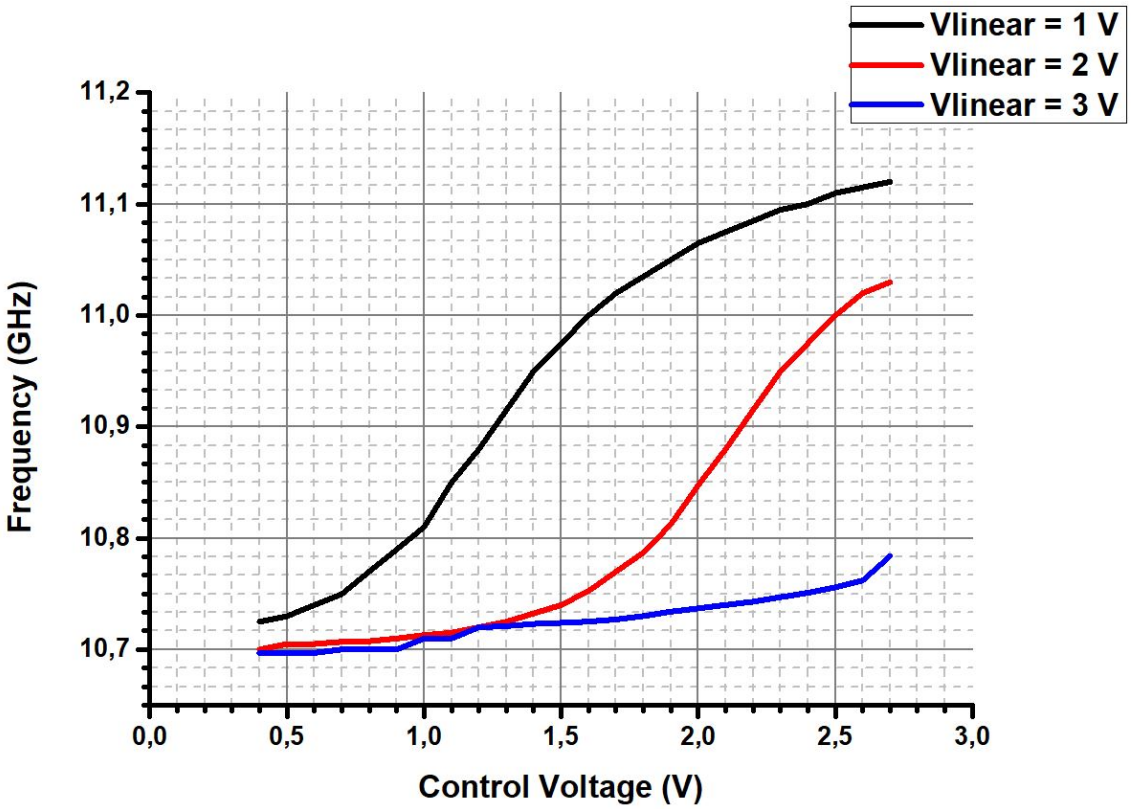


Figure 3.11 Linearity Control Measurement Results

3.1.4 Discrete Frequency Tuning

The frequency tuning of the VCO is divided into two parts: continuous tuning or fine-tuning with the varactor and discrete tuning or coarse-tuning with the capacitor bank. The change of capacitance value in the tank circuit by varactor is not enough to provide enough tuning range on its own. The capacitor bank shown in Fig.3.1 is added to the circuit for a more extensive tuning range. The capacitor bank adds more capacitance to the resonator and shifts the oscillation frequency; switches control these additional capacitors, and they are represented as bits. The control voltage of the varactor can be seen as fine-tuning, while capacitor bank bits are coarse control for oscillation frequency. The required switches can be implemented with a single MOSFET. However, this method degrades the noise performance of the VCO due to the MOS parasitics, even if they provide a more extensive tuning range. In order to reduce the parasitics introduced to the tank circuit, these switches should be added to the tank with additional circuitry, as shown in Fig. 3.12.

The approximate oscillation frequency, including the capacitor values at the bank as a voltage function, can be found with (4.7).

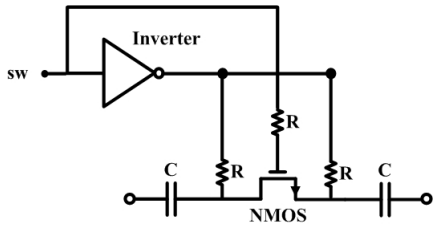


Figure 3.12 Capacitor Bank Switch with Inverter

$$f_{\text{osc}} = \frac{1}{2\pi\sqrt{\frac{L_1}{2}(C_1 + (\frac{C_2 C_{\text{var}}}{C_2 + C_{\text{var}}}) + C_{\text{par}} + C_{\text{bank,n}})}} \tag{3.7}$$

C_{par} denotes the parasitic capacitance introduced to the tank circuit by the NMOS switches. $C_{\text{bank,n}}$ represents the capacitance that is added to the tank by the capacitor bank. The minimum capacitance that can be achieved is $C_{\text{bank,0}}$ where all the switches are open, and the maximum capacitance is $C_{\text{bank,n}}$ where all the switches are closed. Each configuration's frequency can be calculated by plugging the value $n = 0, 1, 2...n$ into (3.7).

When a stand-alone NMOS switch is used to implement these banks, it will cause performance degradation in the circuit because if the signal at the tank gets close to the negative peak of the voltage swing, it will cause forward biasing of the parasitic diodes of the switch and reduce the off resistance, and tank quality (Wagner et al., 2020). Drain and source nodes of the NMOS transistor should be appropriately biased to overcome this problem. The inverters added along with the switches apply 1.2 V (3.3 for the HVMOS case) to the drain and source nodes when the switch is not used (Gate voltage is equal to 0V); thus, parasitic diodes will not be forward biased. Moreover, when the switch is closed, the on-resistance R_{on} also changes with the swing. Fig.3.13 shows the effect of the inverter added to the switches on phase noise and tuning range. Fig. 3.13(a) shows the case where all the switches are open, and Fig. 3.13(b) shows where they are all closed.

The bank's capacitor values should be picked so that there will be no blind zone between the different bit configurations of the banks, as explained in Section. x, as well as the sizes of the transistors. Large transistors will introduce more capacitance, but they will have lower R. In the first version of the VCO, the capacitor bank is realized as 3-bit with standard MOSFETS in the technology; on the other hand, the second version of VCO has a 4-bit capacitor bank realized with high-voltage, thick gate oxide MOSFETs. The incrementation of the bits will provide a more extensive tuning range, and HVMOSs allow higher swings since they have higher breakdown voltages.

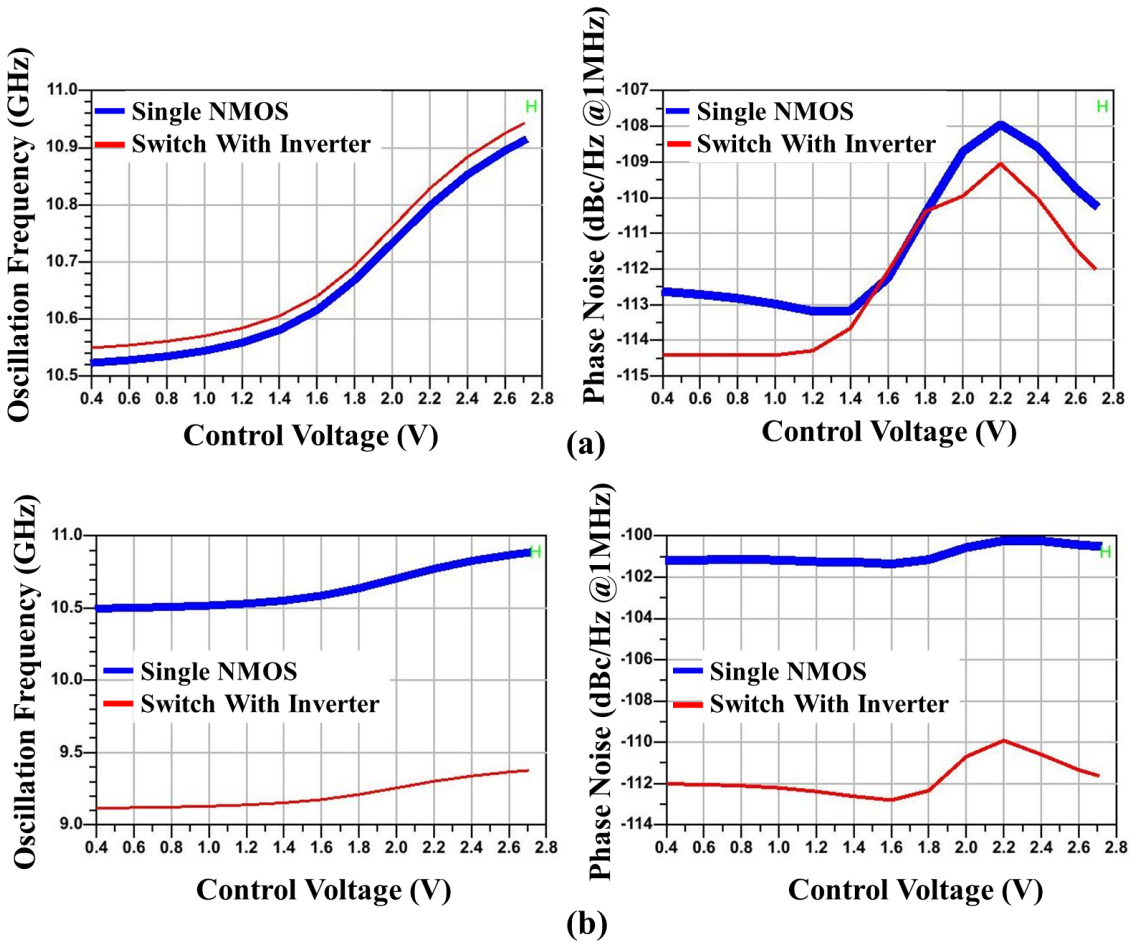


Figure 3.13 Effect of the Inverter at the Bank Switch when
All switches are a) Open b) Closed

3.1.5 Tail Noise Filter

The current source transistor also contributes to the overall phase noise performance due to its thermal noise around the second harmonic (Hegazi et al., 2001). In order to filter out the noise from the oscillator core, there should be a high impedance introduced at the emitter of the Q1 transistors. To achieve the required impedance, the tail filter shown in Fig.3.1 is implemented, and its impedance that is seen from the emitters of the Q1 transistors, Z_{tail} is shown in (4.8)

$$Z_{\text{tail}} = \frac{j.\omega.L_{\text{tail}}}{1-\omega^2.L_{\text{tail}}.C_{\text{tail}}} \tag{3.8}$$

C_{tail} and L_{tail} components are selected such that they will resonate at $2{\cdot}f_{osc}$; thus, high impedance is generated at the emitter nodes of the core. Furthermore, C_{large} provides a low impedance path to the ground for the tail filter and also filters out the noise of the current source.

3.1.6 Output Buffer and Balun Design

A buffer is necessary at the output of the VCO core. Suppose another subsequent block or an instrument for measurements is connected directly to the output of the core. In that case, it will cause a disturbance at the oscillation or even cause it to stop because it will disturb the negative resistance of the CC pair. In order to isolate the core and combine it with the other devices, a cascode buffer was designed using the Q_b transistors (see Fig.3.1). This topology is selected because of its good isolation between input and output. The buffer input was not matched to 50Ω but only connected with a DC block capacitor C_{buff} to the core, not to affect the oscillation condition and oscillation frequency. Moreover, buffers are also used to amplify the core's output to achieve better output power performance. The outputs of the buffers are matched to 50Ω by an L-type matching network C_{match} and L_{match}.

The differential output of the buffers are converter into single-ended with a balun that employs 50Ω matching and 1:1 impedance transformation. The schematic and 3D view of the designed balun are given in Fig.3.14. Converting the output to single-ended increases the output power and improves the PN since it suppresses the even harmonics. Fig.3.15 shows the harmonic suppression in the dBm level. Fig.3.16(a) shows the balun's input matching at each port, (b) shows the phase difference between the differential ports, and (c) shows the loss.

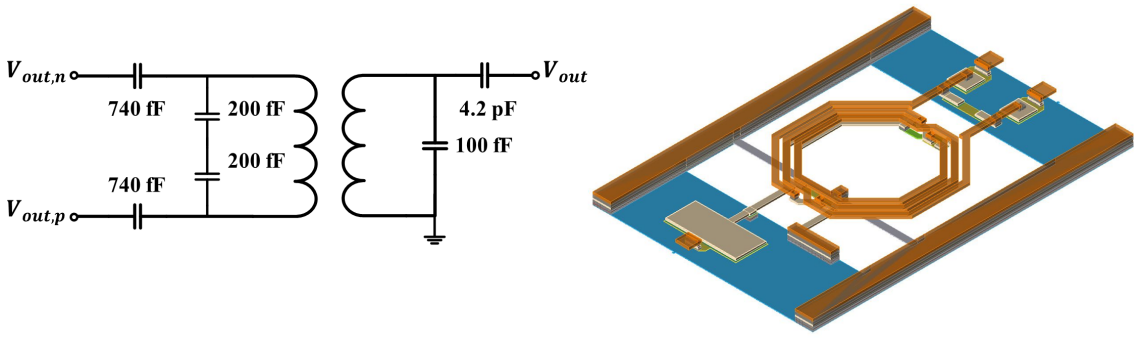


Figure 3.14 a) Schematic View b) 3D layout View of the Output Balun

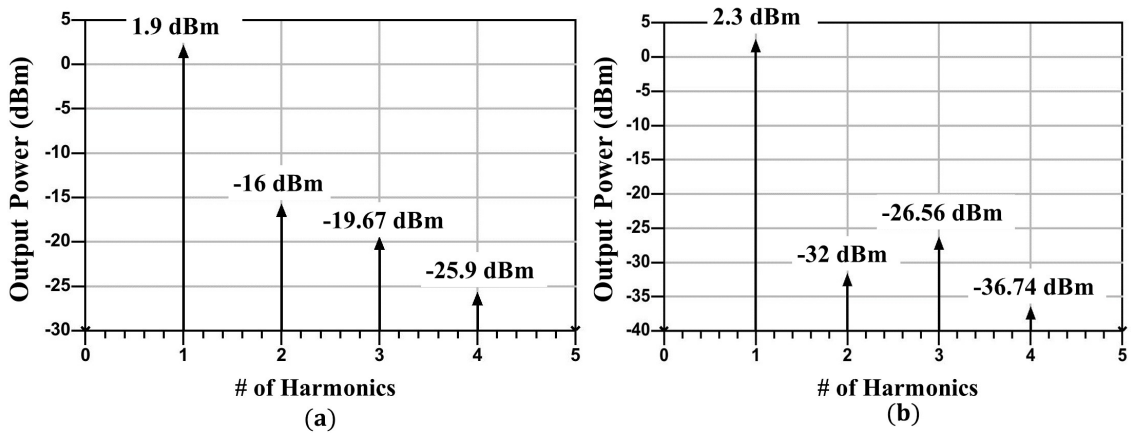


Figure 3.15 Output Spectrum a)W/o Balun b) With Balun

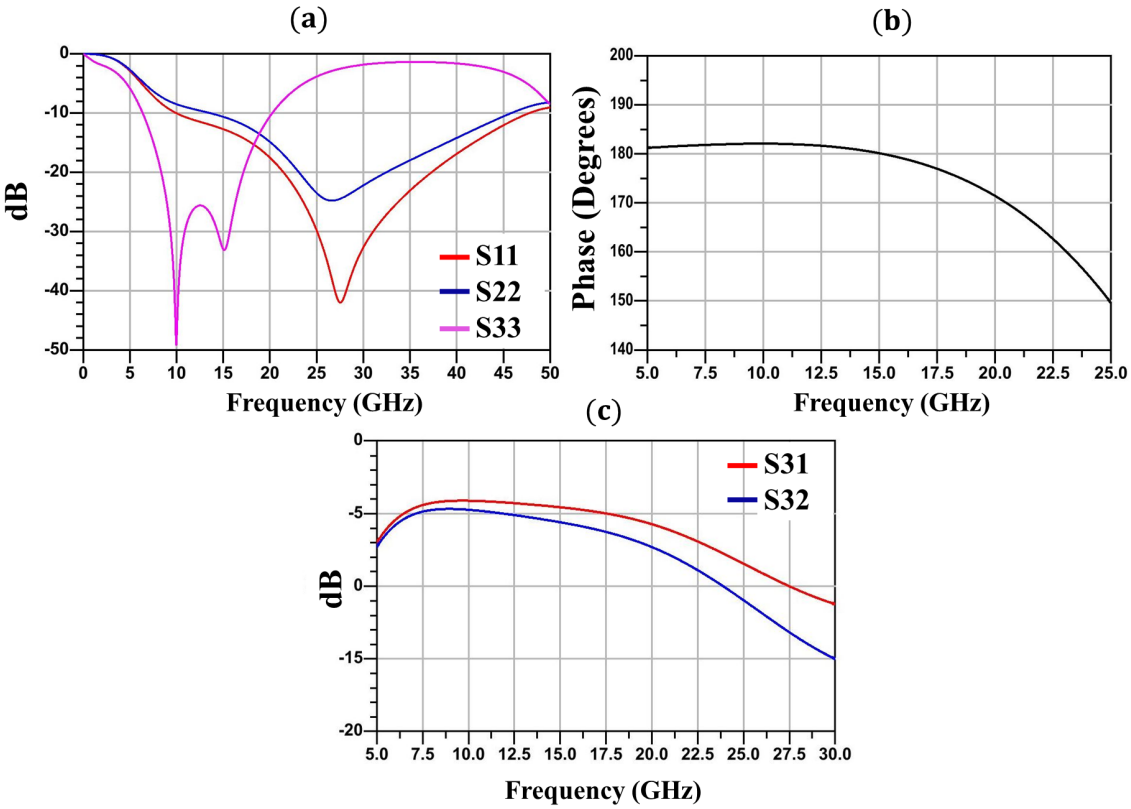


Figure 3.16 a) Input Matching b) Phase c) Loss of the Designed Output Balun

3.1.7 Design Overview and Post-Layout Simulation Results

In this work, two versions of VCOs were designed, and their respective results are shared in the following sections. The first version achieves a PN performance close to the target value given in Table.1.2, with lower power consumption than the target value. However, it could not achieve the desired frequency tuning range. These issues

are addressed in the second version using an inductor with a higher quality factor and a 4-bit capacitor bank with HV-CMOS transistors. The device parameters of both VCOs are given in Table. 3.3. Rather than those specifically analyzed above, the capacitance and inductor values may differ due to device parasitics employed or the different routings. Each value is selected to obtain maximum performance. The biasing of the core transistors, current source, and buffers are identical for both cases.

Table 3.3 Design Parameters and Biasing Voltages of The Designed VCO

Passive Device	*3-bit VCO*	*4-bitn VCO*
Cd	145 fF	80 fF
Cb	60 fF	75 fF
C1	520 fF	475 fF
C2	650 fF	420 fF
Varactor	9.74/0.8 x16	9.74 / 0.8 x16
Cb1	70 fF	70 fF
Cb2	135 fF	130 fF
Cb3	280 fF	250 fF
Cb4	N/A	400 fF
Ctail	245 fF	400 fF
Clarge	1.8 pF	3 pF
Cmatch	300 fF	300 fF
L1	315 pH	210 pH
Lmatch	1.2 nH	1.2 nH
Ltail	75 pH	60 pH

Transistor Sizes and Biasing	*3-bit VCO*	*4-bit VCO*
Q1	2 x 7	2 x 8
Q2	9 x7	9 x 8
Qb	2 x 8	2 x 8
Sw1 W/L	7.95/0.13	30 / 0.33
Sw2 W/L	45 / 0.13	70 / 0.33
Sw3 W/L	70 / 0.13	150 / 0.33
Sw4 W/L	N/A	180 / 0.33
Inverter PMOS W/L	2 / 0.13	2 / 0.33
Inverter NMOS W/L	1 / 0.13	1 / 0.33
Vbias	2.4 V	2.45 V
Vbias2	800 - 815 mV	805 - 820 mV
Vbias3	820 mV	820 mV
Vlinear	1.7 V	1.7 V
Cap Bank Switch Voltage	1.2 V	3.3 V
Vcontrol	0.4 - 2.7 V	0.4 - 2.7 V

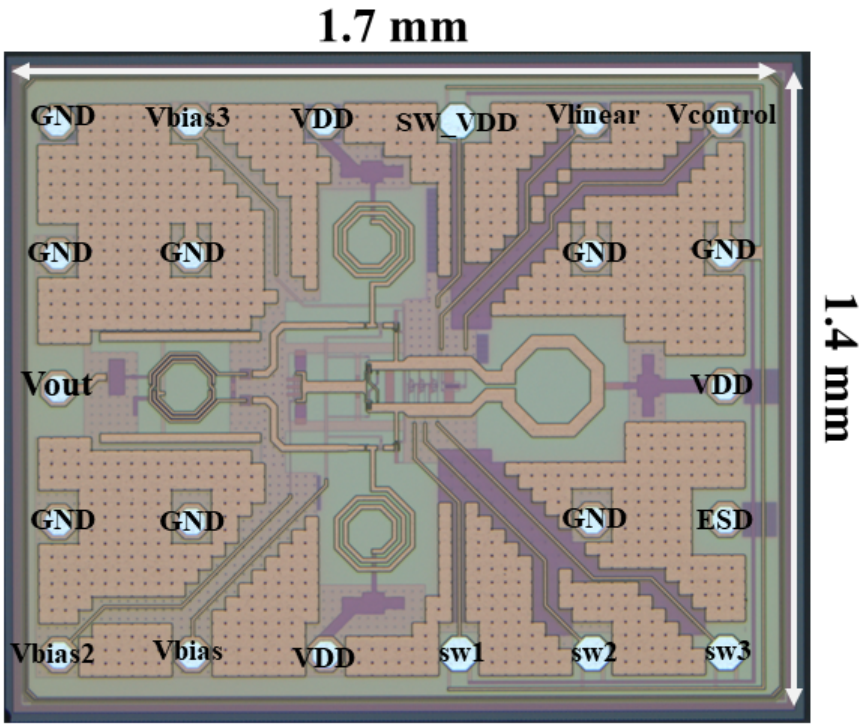


Figure 3.17 3-bit VCO Realized in IHP SG13S Technology for Flip-Chip Assembly

3.1.7.1 3-bit Bank VCO Results

The micrograph of the 3-bit VCO is given in Fig. 3.17. VCO generates signals between 9.12 - 11.02 GHz using a 3-bit capacitor bank. The PN at the center frequency is -115 dBc/Hz @1MHz offset, as shown in Fig. 3.18, and has a power consumption of 25 mW. The design is made for flip-chip assembly and occupies 2.38 mm^2, including the buffers and the output balun. Frequency tuning curves depending on the state of the bits (3 bit - 8 states) are shown in Fig. 3.19, and the PN performance over the changing control voltage for each bit is given in Fig. 3.20. The simulation results also contain the effects of flip-chip assembly and board effects.

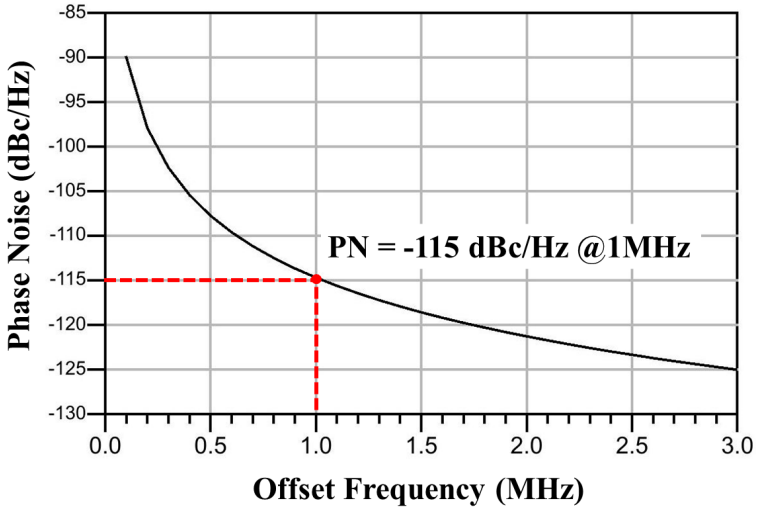


Figure 3.18 PN at Center Frequency

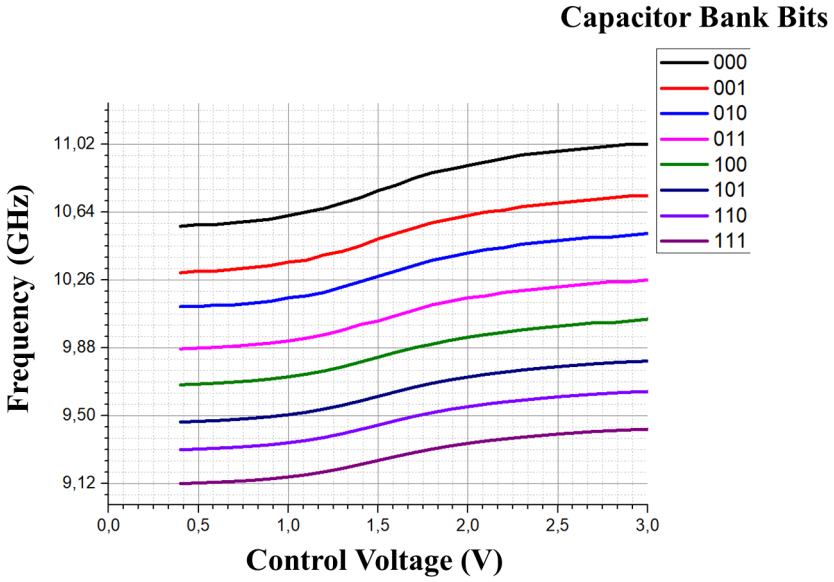


Figure 3.19 Frequency Tuning Curves

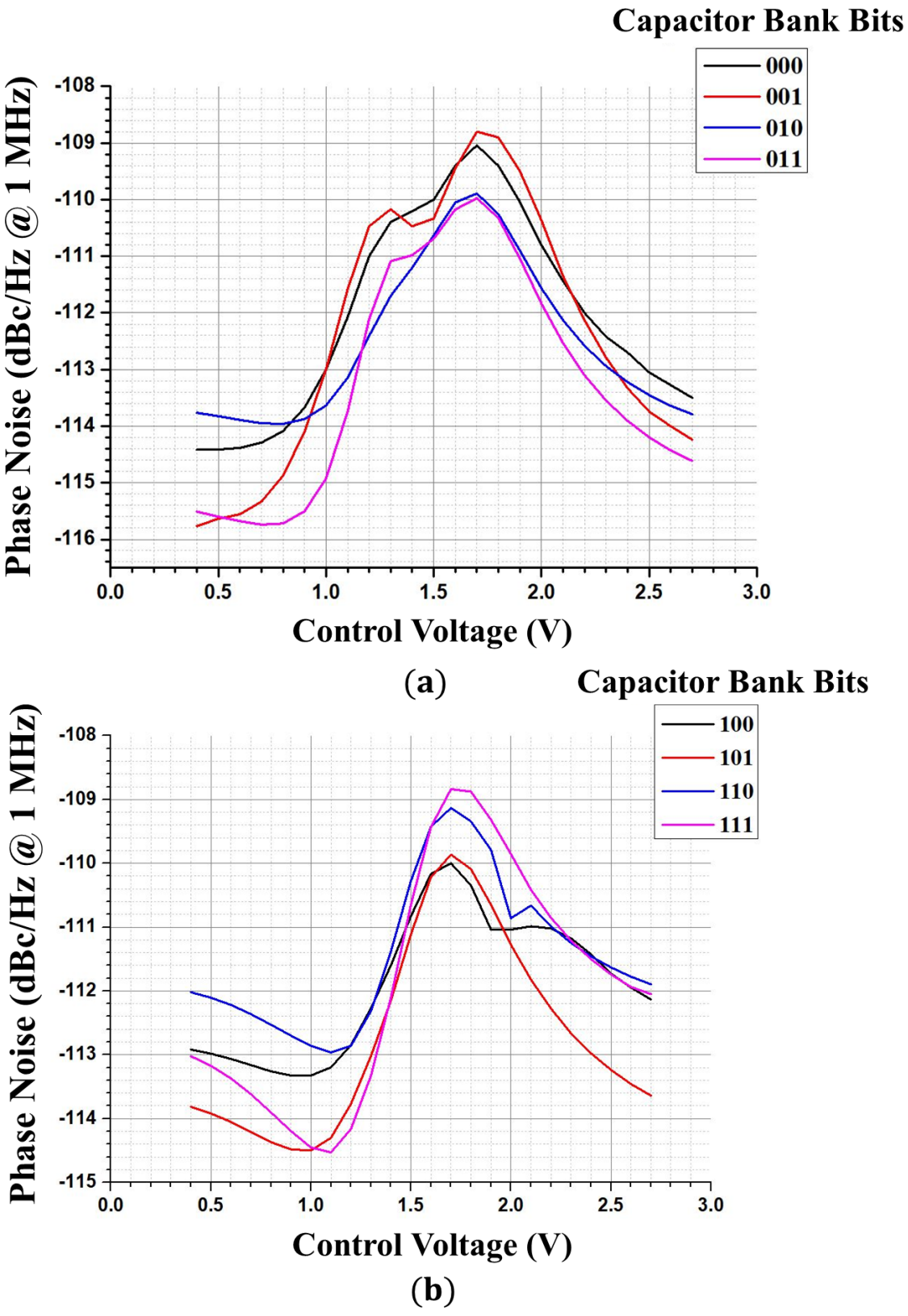


Figure 3.20 PN vs. Control Voltage a) First 4 bit states b) Last bit 4 States

3.1.7.2 4-bit Bank VCO Results

The micrograph of the 4-bit VCO is given in Fig. 3.21. This design employs a range of frequencies from 9.5 to 12.02 GHz with a 4-bit (16 states) capacitor bank. The PN at the center frequency is -116.2 dBc/Hz at 1MHz offset (Fig. 3.22), and the total power consumption is 30mW. Since the overall PLL design requires many pads, the design for the flip chip is left. The second version is designed for wire bonding. In order to take inductance coming from the wire bonds, inductors with a finite quality factor are added to the DC supplies. The pads are designed according to RF probes for the RF output measurement, and the total area is 2.33 mm^2. Frequency tuning curves of the design are given in Fig. 3.23, and the PN performance over the control voltage at different capacitor bank states is given in Fig. 3.24.

Table.3.4 shows the performance comparison of the two designs in terms of the post-layout simulation results. The octogonal inductor used in 4-bit VCO improves the phase noise performance by increasing the tank Q and its decreased inductance, as explained in (3.6). Furthermore, degraded phase noise allowed extra capacitor bank bit to be added to the tank; thus, the tuning range is improved without sacrificing the noise. In conclusion, the improvements done on top of the 3-bit VCO made the 4-bit VCO closer to the targeted values both in terms of noise and the tuning range, while both of the designs achieve power consumption below the targeted value.

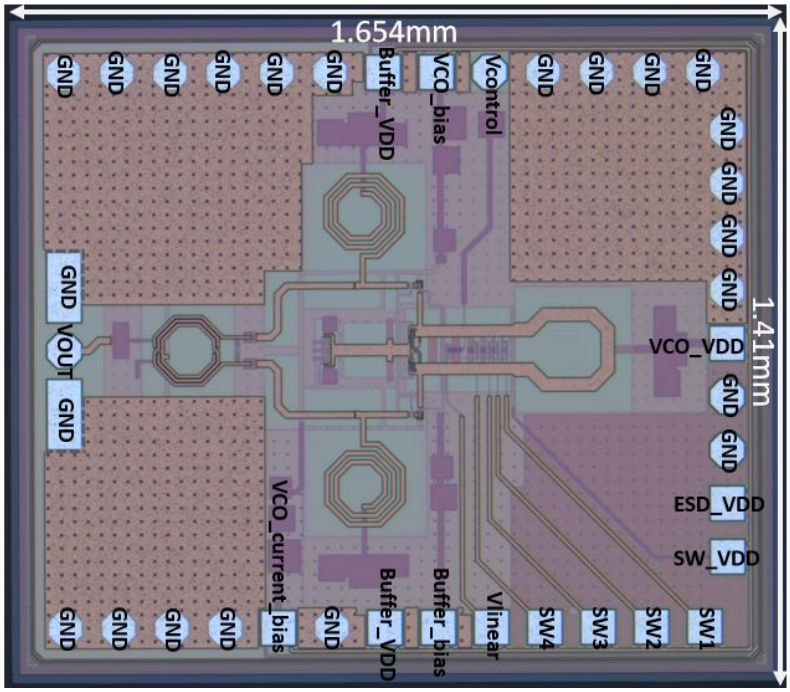


Figure 3.21 Second Version VCO Realized in IHP SG13S Technology for Wire-Bonding and Probe Measurement

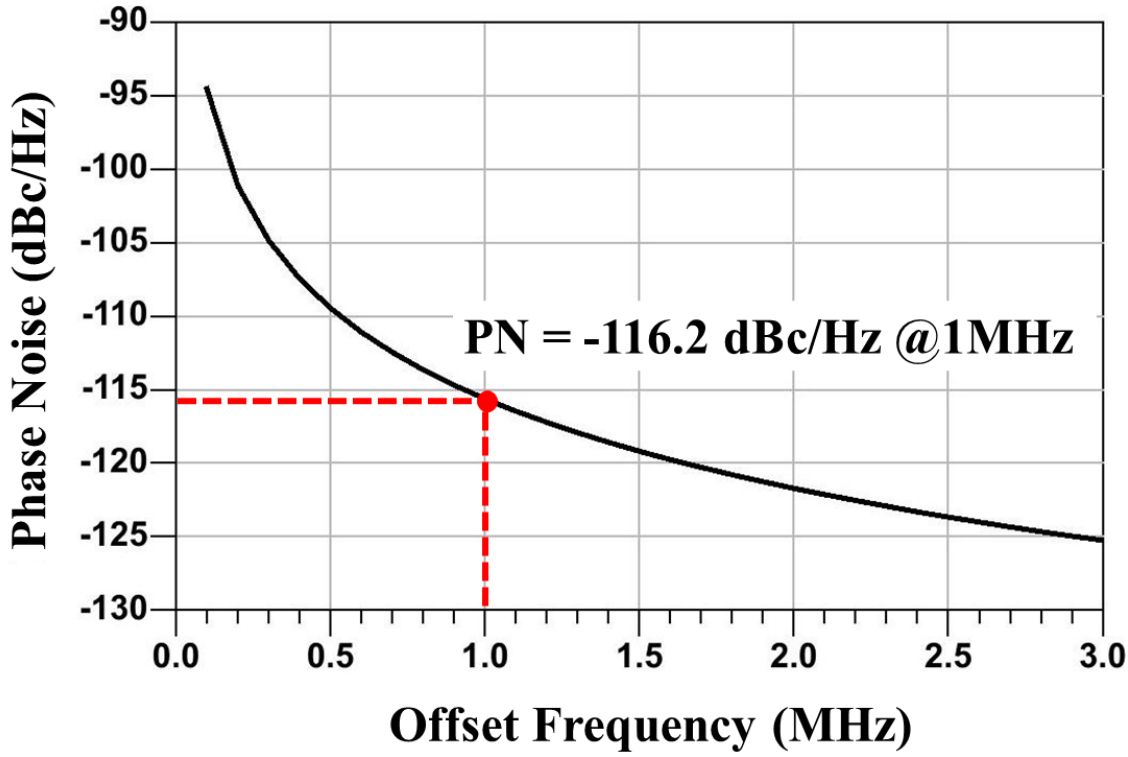


Figure 3.22 PN at Center Frequency

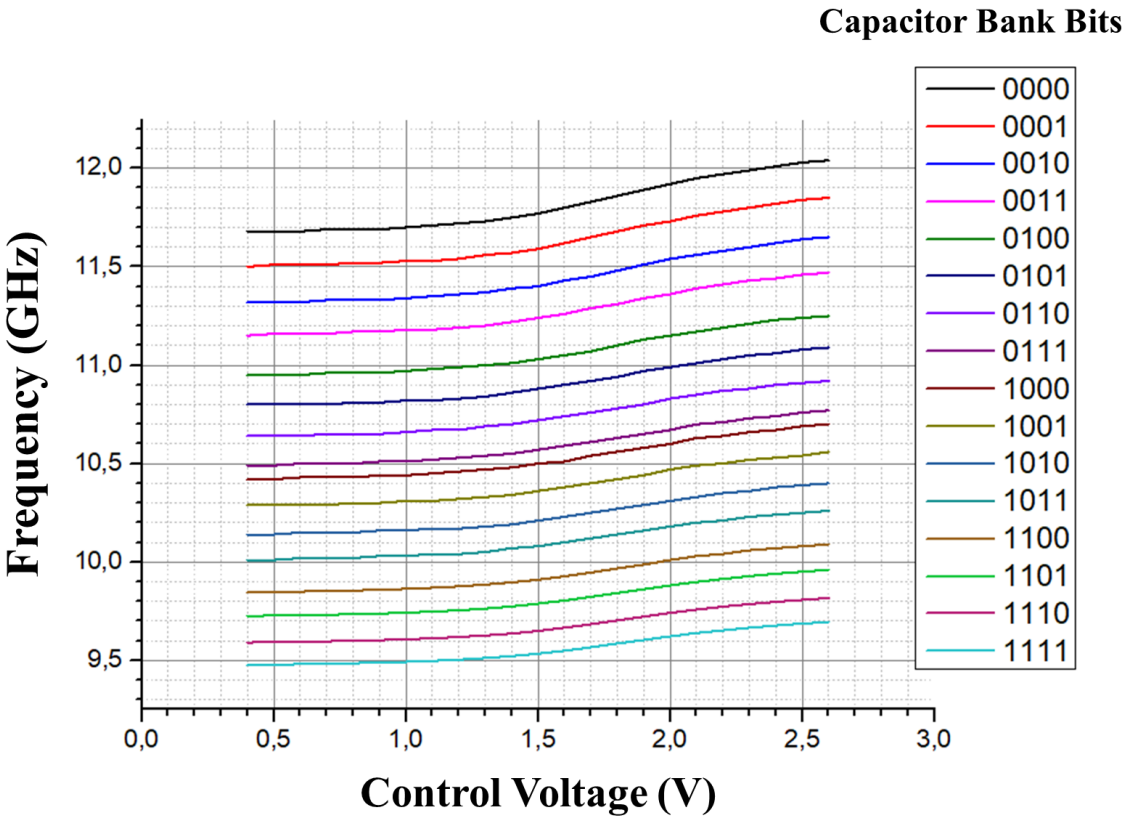


Figure 3.23 Frequency Tuning Curves

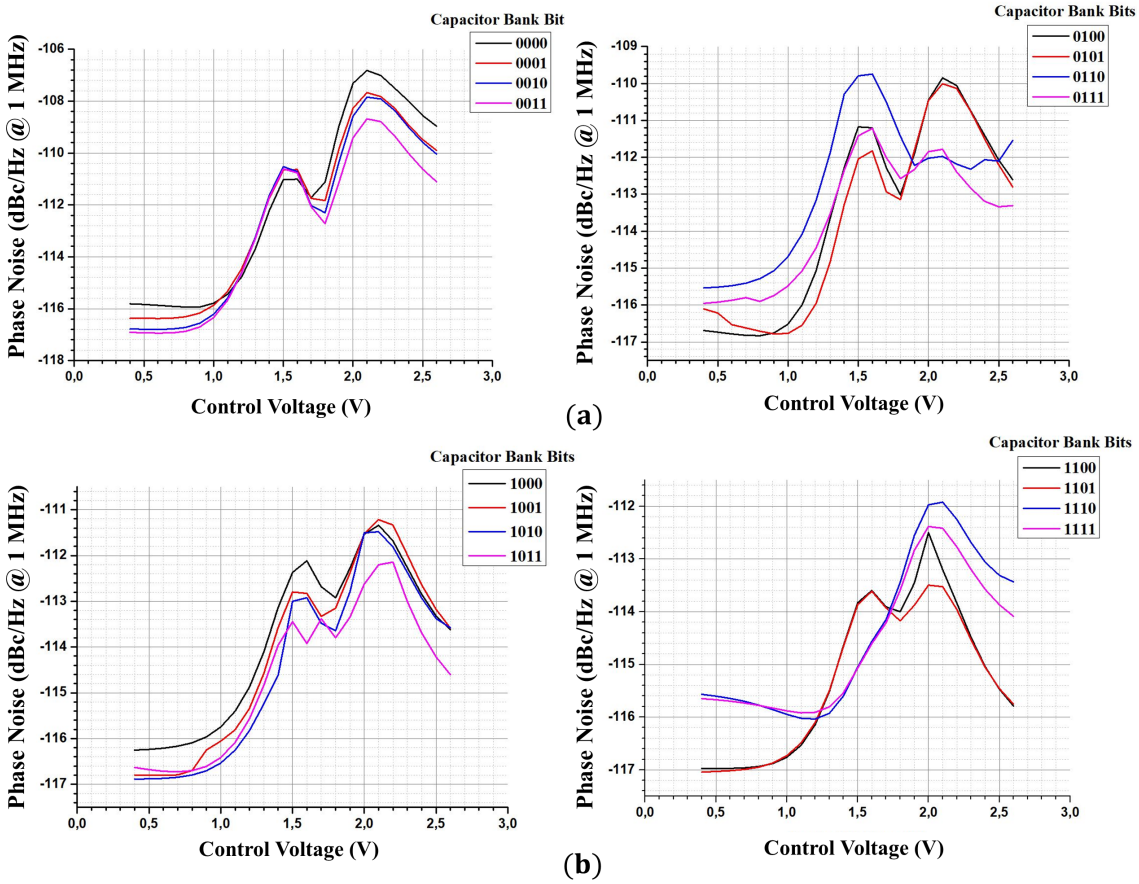


Figure 3.24 PN vs. Control Voltage a) First 8 states b) Last 8 States

Table 3.4 Performance Comparison of 3-bit and 4-bit VCO simulation Results with the Target Specs

	Target Specifications	***3-bit VCO Sim***	***4-bit VCO Sim***
Phase Noise @1 MHz	**-120 dBc/Hz <**	**-115 dBc/Hz**	**-116.2 dBc/Hz**
Frequency Range (GHz)	**9 - 12**	**9.12 - 11.02**	**9.5 - 12.02**
Center Frequency (GHz)	**10.5**	**10.07**	**10.76**
Tuning Range	**%28.57**	**%18.87**	**%23.42**
Power Consumption (mW)	**40 <**	**25**	**30**
FoM	**>184.4**	**181.1**	**182.1**
FoM_T	**>186**	**183.83**	**185.76**

FoM = $-\mathcal{L}(\Delta\omega) + 20log(\frac{f}{\Delta f}) - 10log(\frac{DCPower}{1mW})$ $FoM_T = FoM + 10log(\frac{TR}{10})$

3.2 Divide by-N, Frequency Divider

The frequency divider is one of the fundamental components of a PLL that divides the high-frequency VCO output frequency in multiple orders to bring it to the reference signal's MHz range. The division ratio also has to be programmable in order to be able to adapt to the oscillators changing frequency. There are four main approaches for realizing the divider in mmWave applications: static, dynamic, miller, and injection-locked. Dynamic dividers can function at very high frequencies but suffer from low operation range and require high input power, miller dividers are easy to design, but they introduce high noise; finally, injection locking can operate at high frequencies but, like dynamic dividers, has a limited bandwidth (Zhou et al., 2019). The static dividers are the most appropriate candidate due to their robustness for RF applications with the drawback of high power consumption. There are two approaches to realizing the divider, the analog implementation that uses current mode logic (CML) suitable for high-speed applications but has high power consumption, and the digital approach that uses a counter based on CMOS logic. Since the input of the divider will be between 9 to 12 GHz, and the CMOS transistors of the technology will not be able to operate in these frequencies; thus an analog implementation with HBT transistors is selected for the initial design, named fully CML-based divider.

3.2.1 Fully CML Based Divider Design

The MMD structure (Vaucher et al., 2000) consists of a chain of numerous divide by 2/3 cells shown in Fig.3.25. The control voltage C[n] selects the modulus of the divider. Logic "1" activates division by three, and "0" activates division by two. Considering the frequency range of the VCO, the required division rate should change between 90 to 120; thus, five of these 2/3 cells are required.

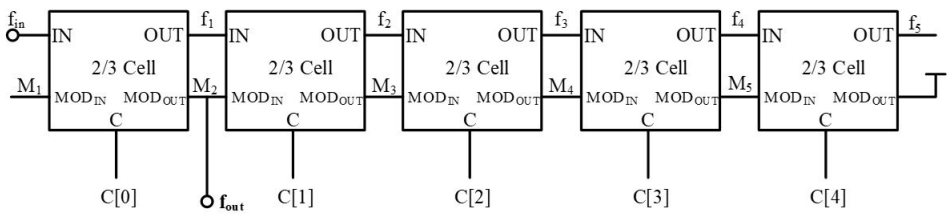


Figure 3.25 Block Diagram of the Initial Design with five 2/3 cells

Fig.3.26a shows the block diagram of a single 2/3 block. These blocks contain two parts; first, one is called the end of cycle logic, where the modin and modout signals are used, and the division modulus is decided depending on the control and the modin signals; the second one is the presecaler logic, where the division operation is done, and the output is generated (Vaucher et al., 2000). The upper two flip-flops that are shown in Fig.3.26a form the prescelar, and the other two form the end of cycle logic. Fig.3.26b and c illustrate the schematic of the A and B blocks designated in the 2/3 cell. The A block is a buffered latch that can drive the clock to the next stage of the 2/3 cell. Based on the speed and loading from the next block, the B cell is terminated with a buffer based on the design. Moreover, the resistors (RL and RE) and the tail current will differ for each stage due to different fanout and speed requirements. The micrograph of the standalone divider is shown in Fig.3.27, which has an area of 1.1 mm^2.

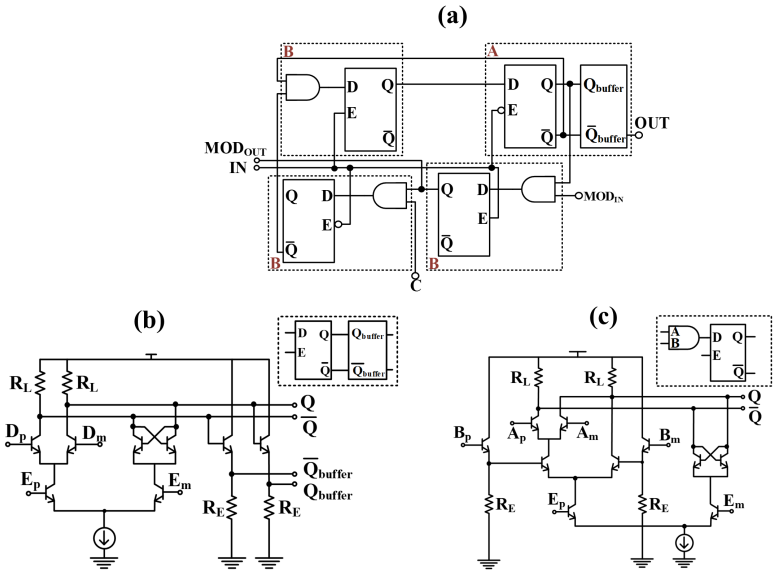


Figure 3.26 a) Block Diagram of 2/3 Cell b) D-latch with buffers c) D-lath with AND gate

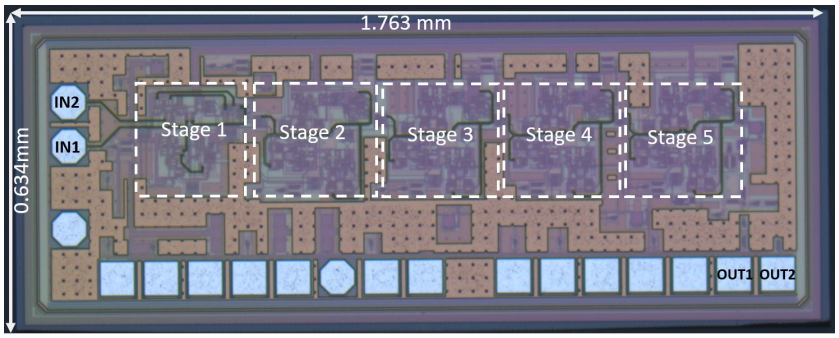


Figure 3.27 Micrograph of The Fabricated Divider

3.2.2 Fully CML Based Divider Post-Layout Simulation Results

Fig.3.28 shows the waveform when a 9.5 GHz input frequency with a 0-2.5 V swing is an input to the divider and attains 99.07 MHz as the output frequency. Fig.3.29a compares the output frequency of the divider for different input frequencies starting from 9 GHz until 12 GHz with a step size of 500 MHz. Since the integer N-PLL can not perform the division to get 100 MHz, its modulus control is selected to achieve the closest frequency to the reference Fig. 3.29b compares the absolute value of the difference between the reference frequency and the output frequency for the same range of input frequencies as in Fig.3.29a. The maximum and minimum difference between the absolute value of the difference between the reference frequency and the output frequency is 14.66 MHz and 930 kHz, respectively. The PFD can tolerate the maximum difference of 20 MHz and lock the PLL. I would like to thank Cerin Ninan Kunnatharayil for his effort in realizing this design.

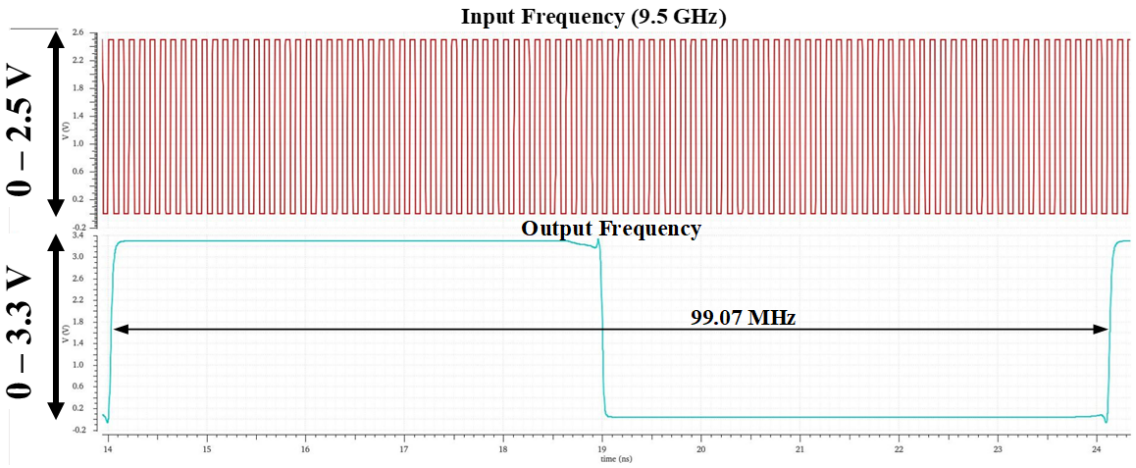


Figure 3.28 Output Waveform for 9.5 GHz Input

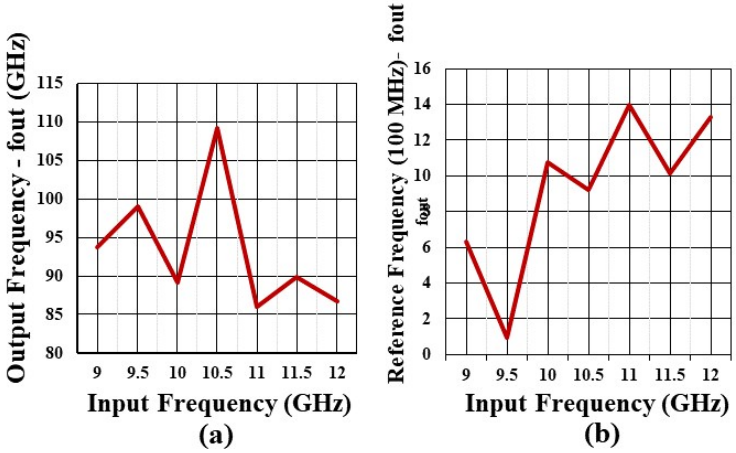


Figure 3.29 a) Output frequency Behaviour with Different Input Frequencies b) Absolute difference between reference and divider output

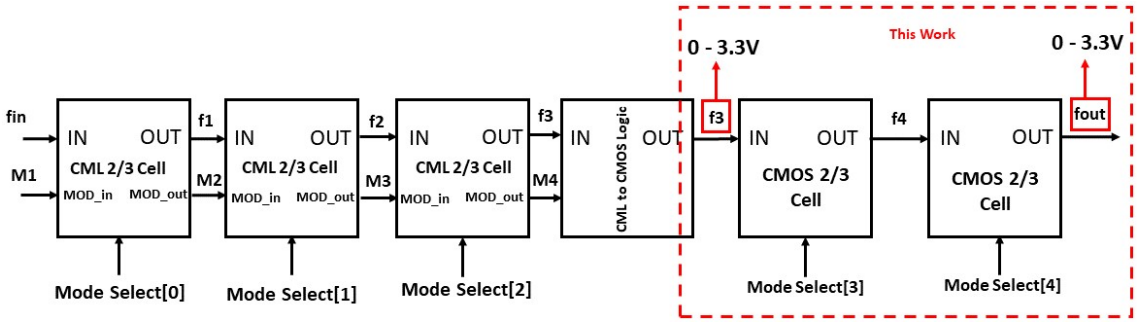


Figure 3.30 Block Diagram of the New Divider

3.2.3 Modified Divide by N circuit

Although the initial design performed without any problem, it consumes a high dynamic power, up to 1.5W, and a large area. This section tries to tackle and solves these problems up to a certain point. The idea is that CMOS divider cells can be used after the 3rd 2/3 CML cell since the output frequency after that point will be 1.5 GHz maximum, where CMOS transistors can operate. The 4th and the 5th cells are removed from the initial design, and the output of the 3rd cell is fed into the "CML to CMOS Logic" that had been designed for the divider-PFD interface, as shown in Fig.3.30. This output is divided by DFF-based small area, low power consumption 2/3 cells designed with CMOS logic.

The topology used for the CMOS divider is shown in Fig.3.31 (Razavi, 2020). Here, the input signal is connected to the clock node of the flip-flops, and "Mode Select" controls the modulus, divided by 2 or 3 selections. If the "Mode Select" is low, the Q1bar signal transits through or gate, and the circuit divides by 3. In the other case where "Mode Select" is high, Q1bar has no effect, and the circuit is downsized to a single flip flop, the AND gate passes Q2bar to the A node, and the second flip flop FF2 acts as a divide by two circuits. Q2 signal represents the output of the divider.

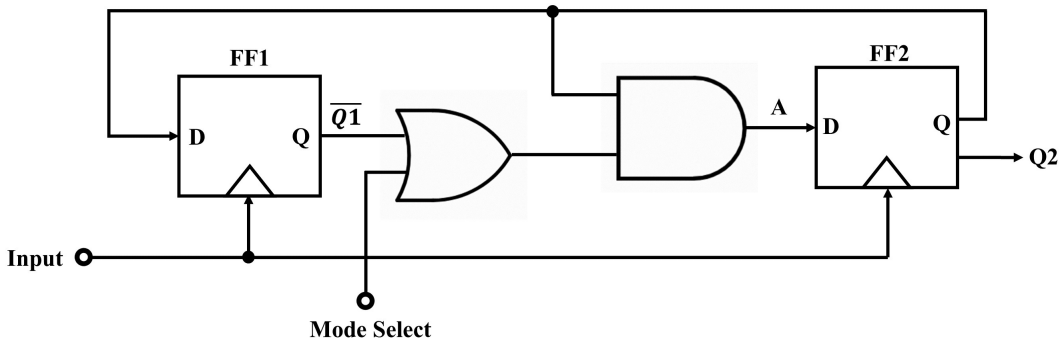


Figure 3.31 CMOS Dual Modulus Design Used for Implementation

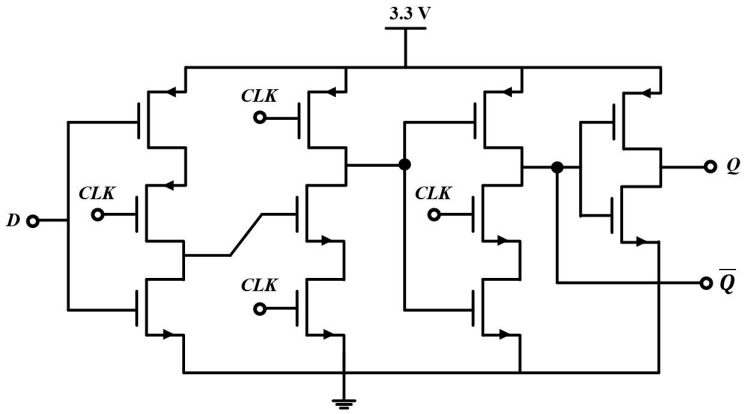


Figure 3.32 TSPC D-Flip Flop

The flip-flops are designed with True-Single Phase Clock (TSPC) topology as positive edge triggered D-flip-flops, as shown in Fig.6. This topology is selected due to its advantages for high-speed applications compared to traditional CMOS logic. Also, it offers low complexity, realized with only 11 transistors (Kang & Leblebici, 2003). The working principle of this circuit is as follows: initially, when the clock is low, the initial stage acts as a transparent latch to acquire the input signal, while the output node of the 2nd stage is precharged. During this cycle, the third stage and the inverter keeps the previous state. When the clock inverts to high, the first stage stops the transparent behavior, and 2nd stage starts evaluation; at the same time, 3rd stage becomes transparent and transmits the hold value to output. The other components of the divider AND and OR gates are designed with a straightforward CMOS logic design. The HV NMOS transistors are sized at a W/L ratio of 1 μm/0.33 μm, and PMOS transistors are sized at 3 μm/0.33 μm.

3.2.4 CMOS 2/3 Cell Post-Layout Results

The layout of the designed CMOS 2/3 cell is shown in Fig.3.33a. Three buffers are implemented to ensure the robustness of the feedback signal from the Qbar of the DFF2 to the D input of the first DFF. Later, each of these stages are connected back to back, as shown in Fig.3.33b, to achieve 2 stage divider to be implemented in the CML logic design. The total area of a single stage is 780 μ^2 while two cells combined occupy 1680 μ^2. The same single stage that has been implemented with HBTs and CML logic has an area of 0.0825 mm^2. The large area difference between these blocks is shown in Fig.3.34.

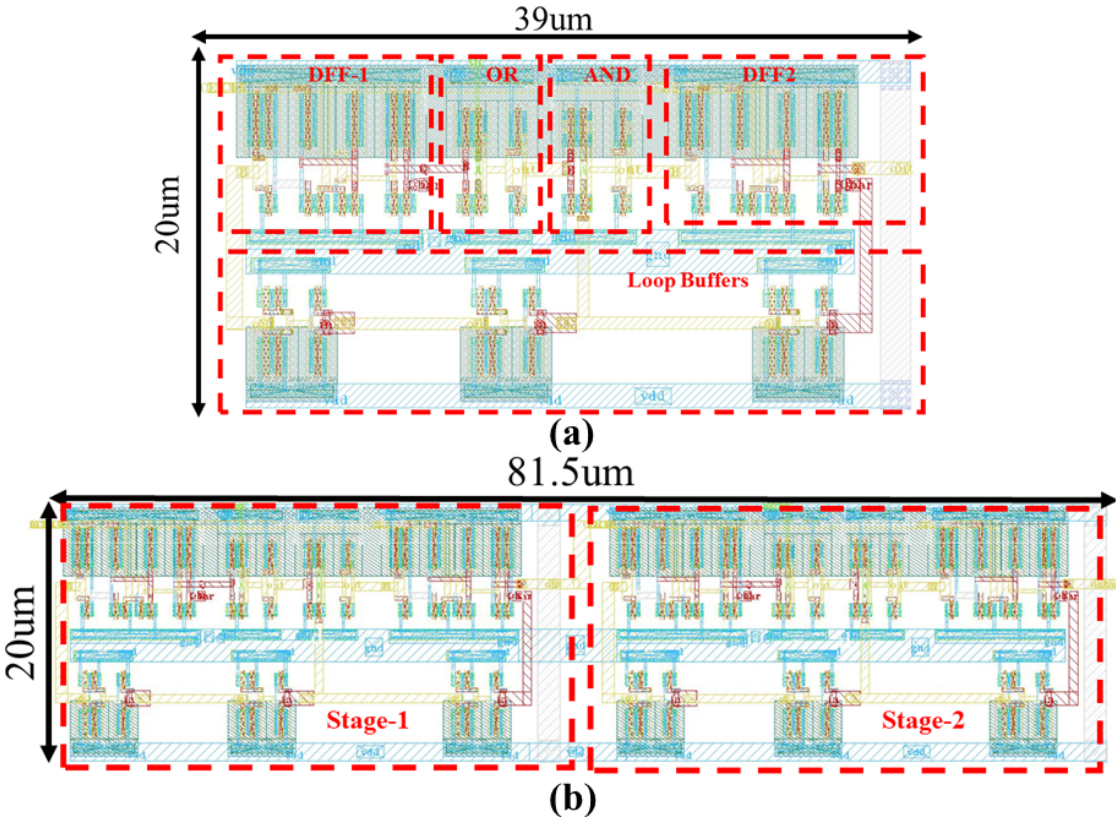


Figure 3.33 a) Single Stage b) Two Stage CMOS Divider Cell Layout

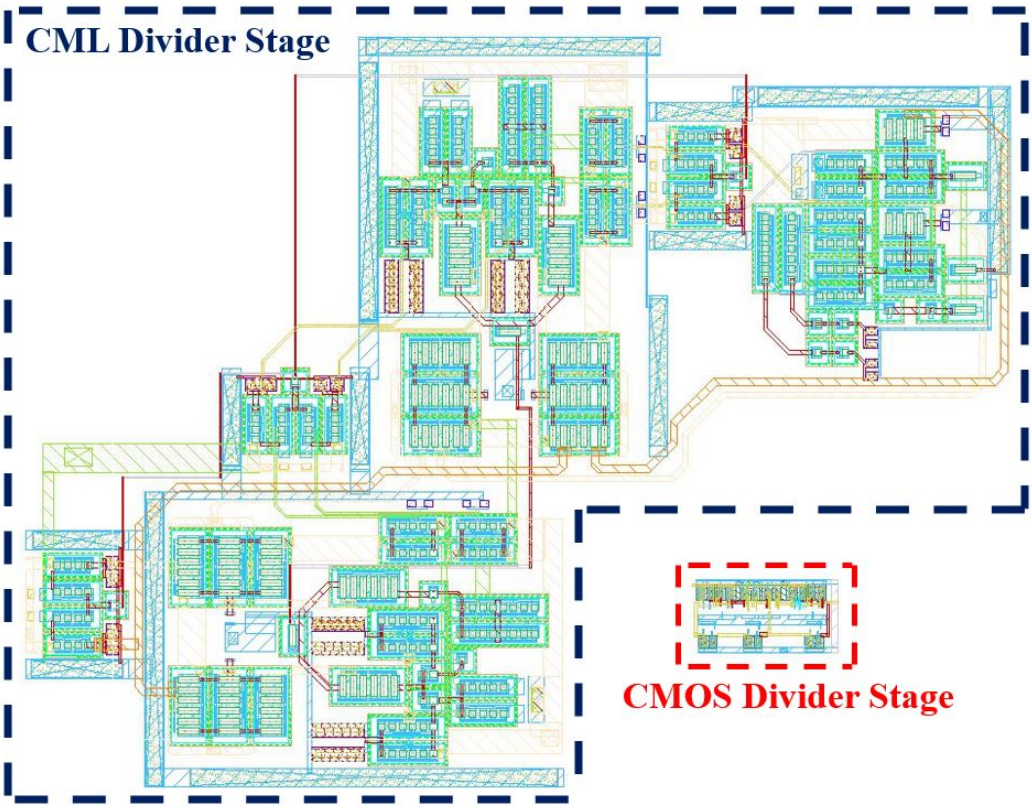


Figure 3.34 Area Comparison of Single CML and CMOS 2/3 Cells

Initially, the 2 CMOS MMD is simulated on itself with a 1.5 GHz input; this frequency is the maximum available frequency coming from the 3-stage CML logic. The standalone simulation results of the 2-stage performing divide by 4,6 and 9 are given in Fig.3.35a, b and c, respectively. Afterward, the CMOS logic divider is integrated with the CML logic and simulated with a 12 GHz input. The waveforms are given in Fig.3.36a and b show the CMOS dividers performing divide by 4 and 9 operations on the output coming from the CML to CMOS logic. It should be noted that the CML logic division is set to a 2x3x3 configuration. However, the outcome is smaller than expected; thus, as a part of future work, the bias of the CML logic should be reduced to implement the required division, which will lead to further power consumption improvements.

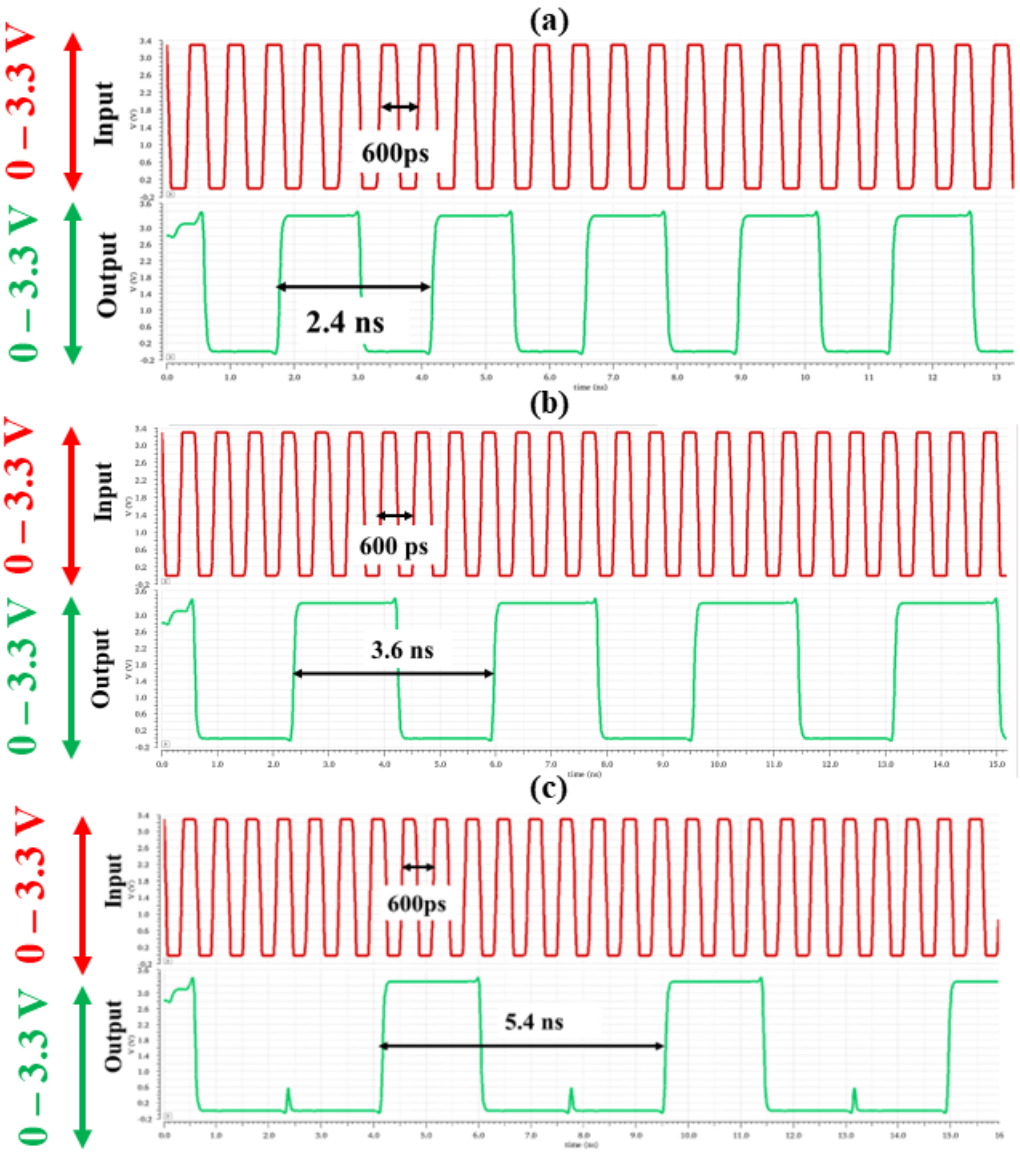


Figure 3.35 2-stage Standalone Simulation Results of the Designed Divider Divide by a) Four b) Six c) Nine

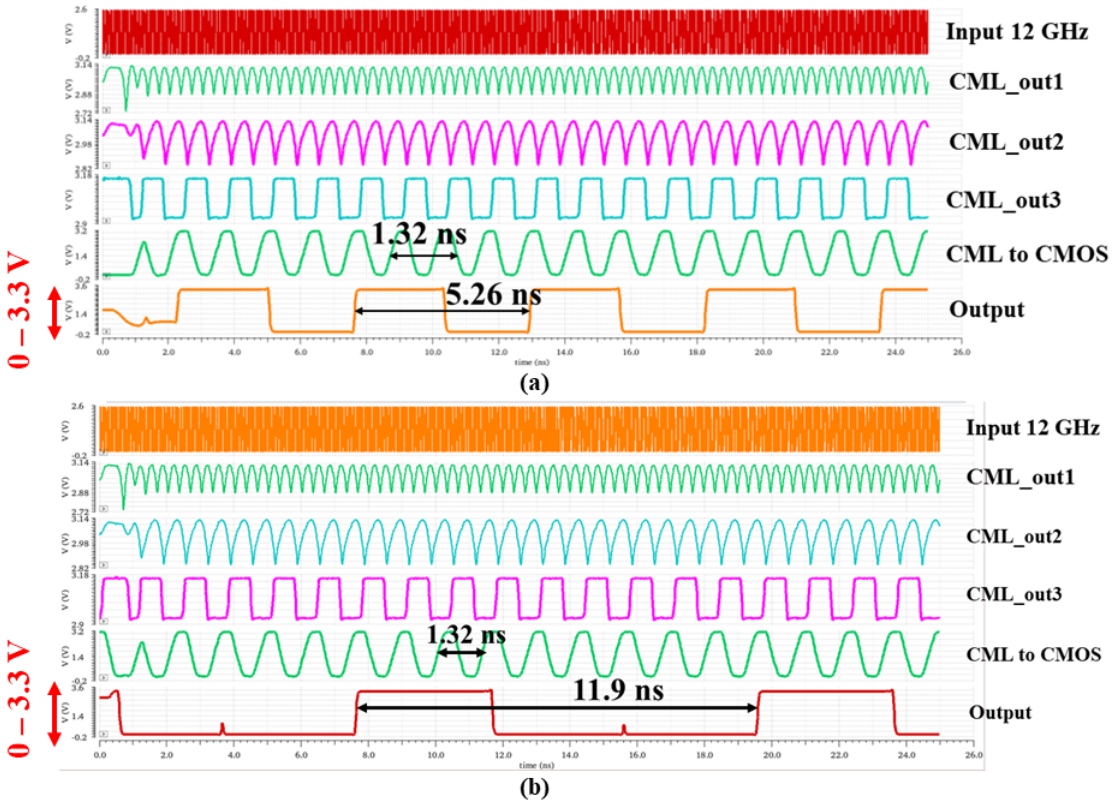


Figure 3.36 Complete Simulation Results of the Designed Divider CMOS Divider Stages Perform Divide by a) Four b) Nine

Table.3.5 gives the area and dynamic power consumption comparisons of a single CML and CMOS divider stages. The CMOS divider could perform the same required operation with a power consumption of almost fifty times less and with an area two orders of magnitude smaller.

Table 3.5 Comparison of CML and CMOS Divider Cells

	Dynamic Power Consumption (mW)	**Area μm^2**
CML Divider Cell	**380**	**300 μm x 275 μm**
CMOS Divider Cell	**7.7**	**20 μm x 39 μm**

3.3 PFD/CP & LF Designs

The following blocks presented in this section are designed by Ajten Fejzullahu. A brief overview of the designs and their combined simulation results are given. The detailed design flow can be seen in her thesis work(Fejzullahu, 2022).

3.3.1 Phase/Frequency Detector Design

PFD is a digital block that detects the phase of the frequency difference between two signals and outputs a pulse signal that signifies the difference. The inputs of the realized PFD are an ABRACON ABLNO crystal oscillator with a frequency of 100 MHz and a PN of -155 dBc/Hz @1 MHz, and the divided output of the VCO. For this work, NAND-based topology, shown in Fig.3.37 is selected rather than the NOR-base topologies due to its superior PN performance at high frequencies (Homayoun & Razavi, 2013). The topology works under three different cases: UP, DOWN, and LOCK, respectively. UP signal is generated by PFD when the phase of the reference signal leads the phase of the output of the divider while the DOWN signal is generated for the inverse case. On the other hand, whenever two signals arrive with a 0 phase difference, the system generates both UP and DOWN signals simultaneously and enters the LOCK state. Results of the simulations for the outputs of PFD, CP, and LF are shown in Fig. 3.39. The reset output of the NAND gate will remain at low logic as long as its NAND gate receives logic one inputs, and whenever the Reset signal performs a falling transition, both UP and DOWN signals will rise.

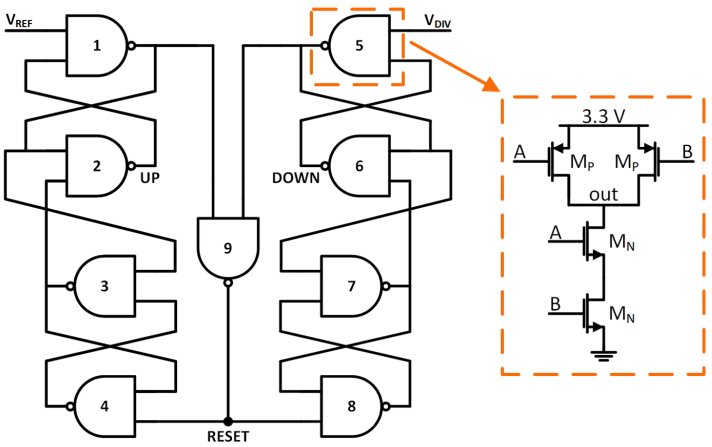


Figure 3.37 NAND-based PFD

3.3.2 Charge Pump Design

The charge pump is used to create an increasing or decreasing current based on the magnitude of the tail current in the CP when a UP and down pulse are activated, respectively. Fig.3.38 shows the schematic of the charge pump. The charge pump must create a linear change in current when a UP or DOWN pulse is applied. However, in reality, the mismatch between the current source generated by the PMOS and NMOS during charge and discharging creates a non-linearity. To avoid this current mismatch, a large capacitor is placed between the gate of M3 and the supply. Similarly, a large capacitor is placed between the base of the Q1 transistor to the ground. This large capacitance ensures a constant voltage at the base/ gate terminal of the transistor for any sudden fluctuations. Moreover, a unity gain buffer is placed, as shown in Fig.3.38, to minimize the current mismatch ensuring the voltage at the drains of M2 transistors is the same. The VCO requires to have a constant voltage between 0.3 - 2.3 V. The upper limit of the aforementioned voltage range defines the supply voltage of the charge pump. Since the maximum voltage of the control voltage is 2.3 V, therefore the supply voltage is taken as 2.6 V. The power consumed by the charge pumps is 6.71 mW. The "Vcontrol" signal at the bottom of Fig.3.39 shows the output of the CP according to the UP and DOWN signals of the PFD.

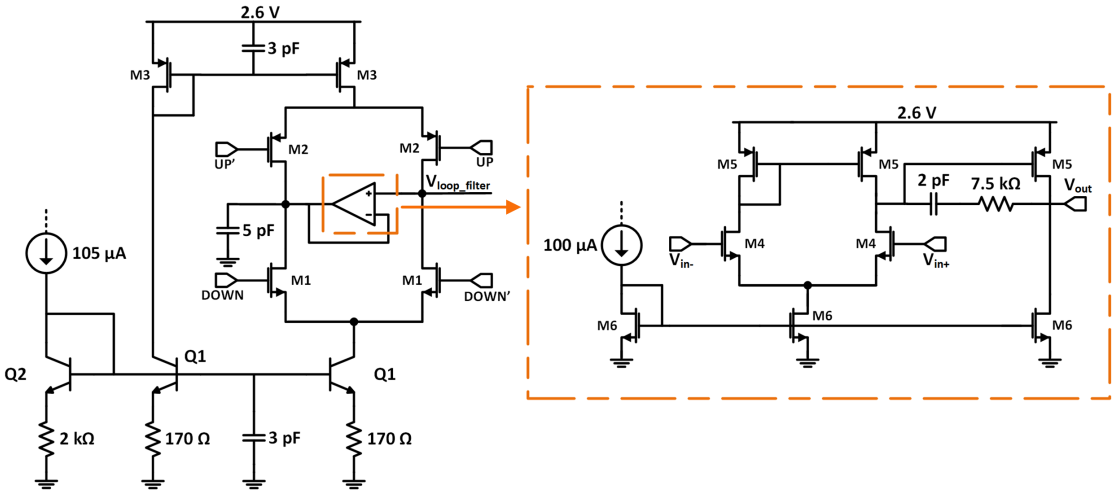


Figure 3.38 Schematic of the Designed CP

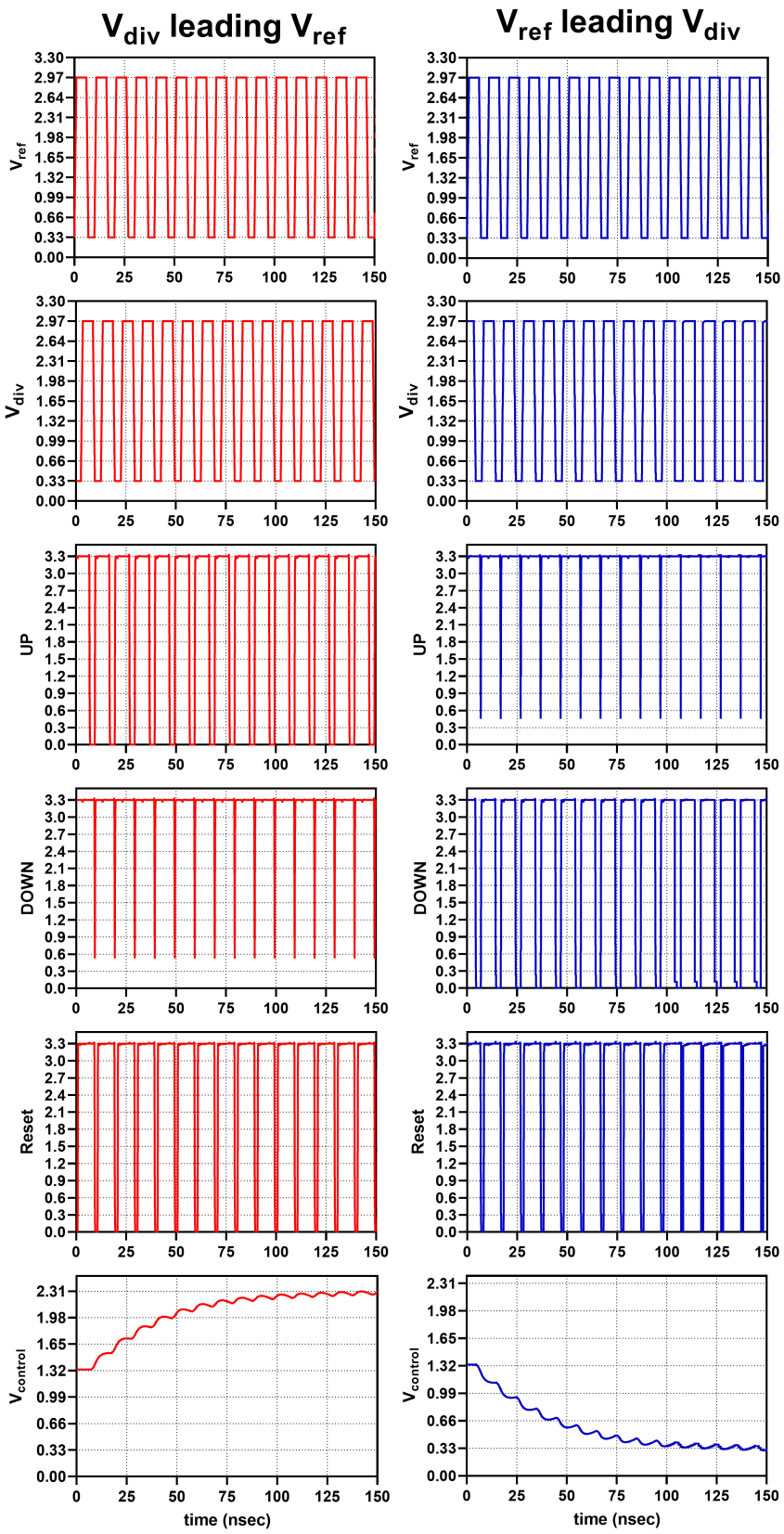


Figure 3.39 Simulation Results of PFD accompanied with CP and LF

3.3.3 Loop Filter Design

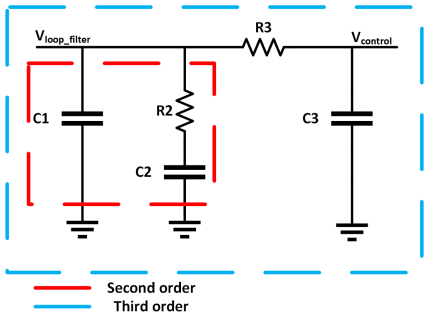


Figure 3.40 Third Order Loop Filter Design For the Synthesizer

The output of the charge pump is connected to the loop filter. The requirement of the input to the VCO is a constant DC signal. However, the charging or discharging of the capacitor at the output of the charge pump creates a high–frequency component that is removed by the loop filter as it has the characteristics of a low pass filter. The third-order filter is chosen to create a high-roll off, as shown in Fig.3.40.

3.4 System Integration and Behavioral Modelling of the PLL

The placement of each sub-block of a PLL in the whole system layout has to be handled carefully. The closed loop PLL that is designed in this work is shown in Fig.3.41. The PFD/CP/LF blocks are placed as close as possible to the VCO since any interference that occurs in the control voltage line will severely degrade the PLL performance. Furthermore, the interface between the VCO output to the divider input requires extra buffers and the addition of a DC offset. The single-ended output of the VCO is divided with a Wilkinson power divider, and one end goes to the output of the chip while the other end is connected to another balun for differential signaling. Since the input of the divider requires a differential signal with a swing from at least 0 to 2V, the divider buffers are added to the circuit to amplify the signal, and later via an inductor, their common mode changed to 1V. In order to test the interface between the VCO and the divider, using Keysight ADS, the post-layout simulations of the VCO, including the power divider and the circuitry required for the divider interface, were added to the Cadence environment using s2p files. Fig.3.42 shows the signals at the input of the divider and the divided output; it is observed that the divider can generate the 3.3 Vpp signal that is required by the PFD by the VCO's buffered output.

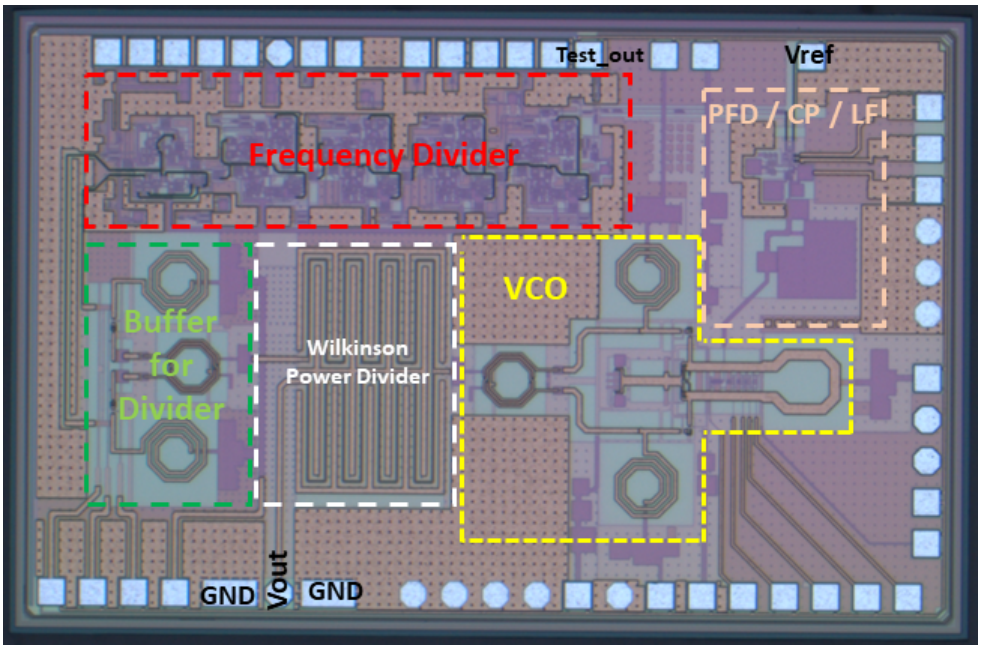


Figure 3.41 Realized Closed Loop PLL Chip

Figure 3.42 Divider Input Coming from the VCO and The Square Divided Output to PFD

3.4.1 System Behavioral Simulations

The system was simulated in MATLAB using Simulink (Fejzullahu, 2022). Initially, the loop filter parameters were extracted by providing specifications of the loop filter, charge pump, and VCO. The open loop and closed response were attained based on the filter parameters. Fig.3.43a shows the open loop bode plot, and Fig.3.43b shows the step response of the closed-loop PLL when the frequency was locked at 10.7 GHz.

To achieve more realistic PN results, the phase noise of the PLL was also attained from the ADS environment to achieve more realistic PN results. Phase noise of -108.7 dBc/Hz, @1 MHz offset, was acquired for a 3.86 pA/Hz of output current noise from

the PFD, CP, and LF, as shown in Fig.3.44. It should be noted that in this model, the noise is only valid for the offset frequencies at 1 MHz and above. In this model generated in ADS, the lower offset frequency noises of the VCO cause calculation errors; nominally, the noise of the VCO is much higher than the total PLL below 500 kHz. On further analysis, it was observed that there was a two dBc/Hz improvement in the phase noise when the output current noise was reduced to 1 pA. Moreover, it was observed that even the CP current affects the phase noise. It was observed on increasing the current of the CP from 1 mA to 3.86 mA, the simulated phase noise improved from -104.768 dBc/Hz to -110.341 dBc/Hz. Table.3.6 compares the achieved and target values of the designed PLL. Moreover, using a reference crystal oscillator will lower phase noise will allow increasing the loop bandwidth leading to lower phase noise by suppressing the VCO PN. The targeted and achieved TR is directly related to the VCO and can be achieved by adjusting the capacitor bank values.

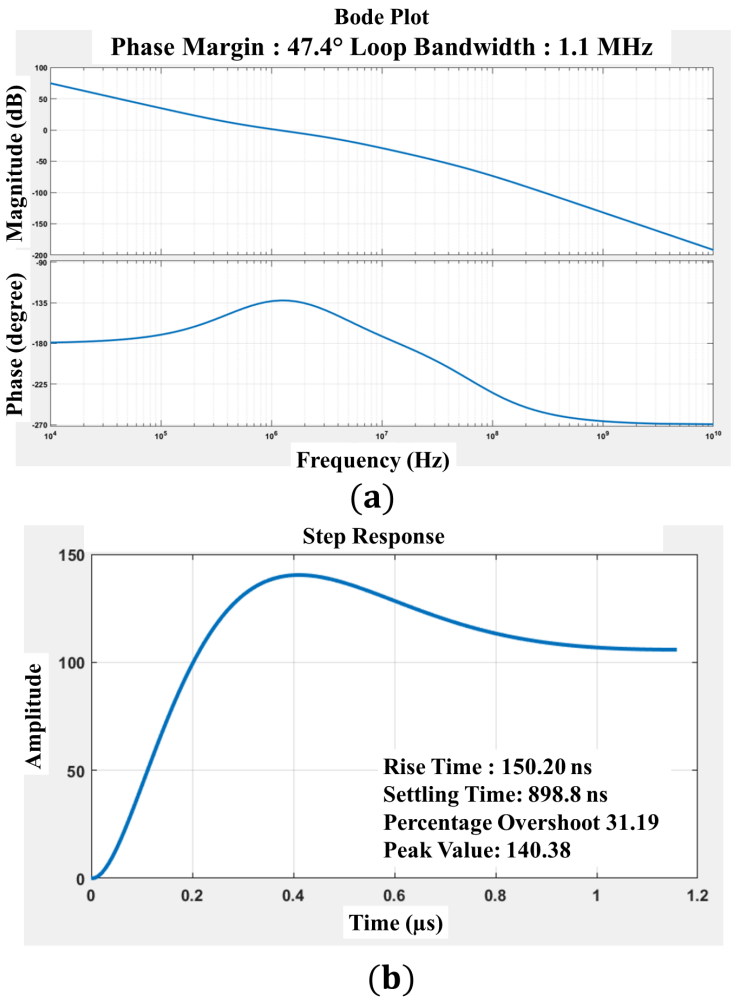


Figure 3.43 Simulation of a) Bode plot of Open-Loop System b) Step Response of the Closed Loop

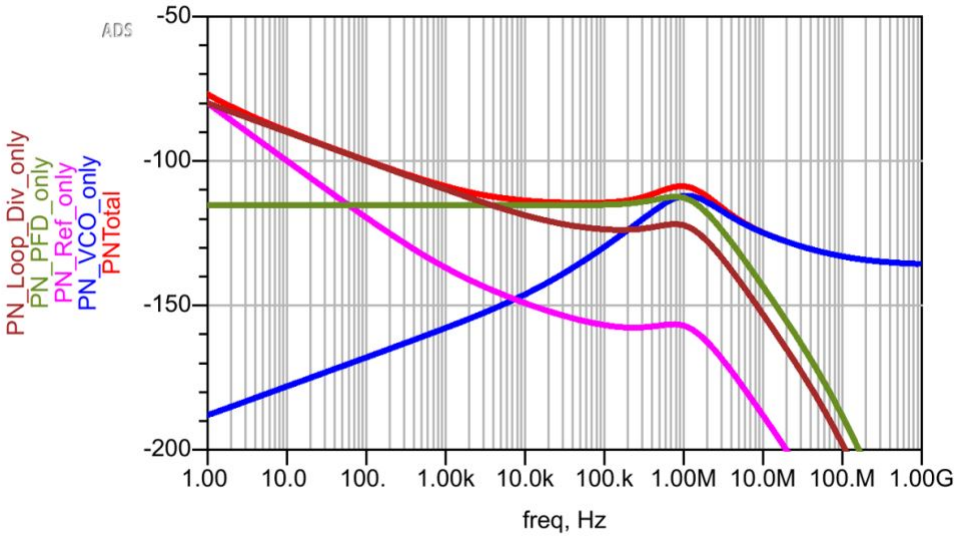


Figure 3.44 Phase Noise Simulation in ADS

Table 3.6 Comparison of the Targeted Values and Achieved Simulated Values

	Target	**Simulated**
Phase Noise (dBc/Hz @1MHz)	**-120**	**-108.7**
Frequency Range (GHz)	**9-12**	**9.5-12.06**
Loop Bandwidth	**1 MHz**	**1.1**
Settling Time	**1u**	**898.8n**
PFD Phase Shift	**%1<**	**%0.19**
Charge Pump Current	**1 mA**	**1 mA**
Charge Pump Current Mismatch	**%1<**	**%0.75**

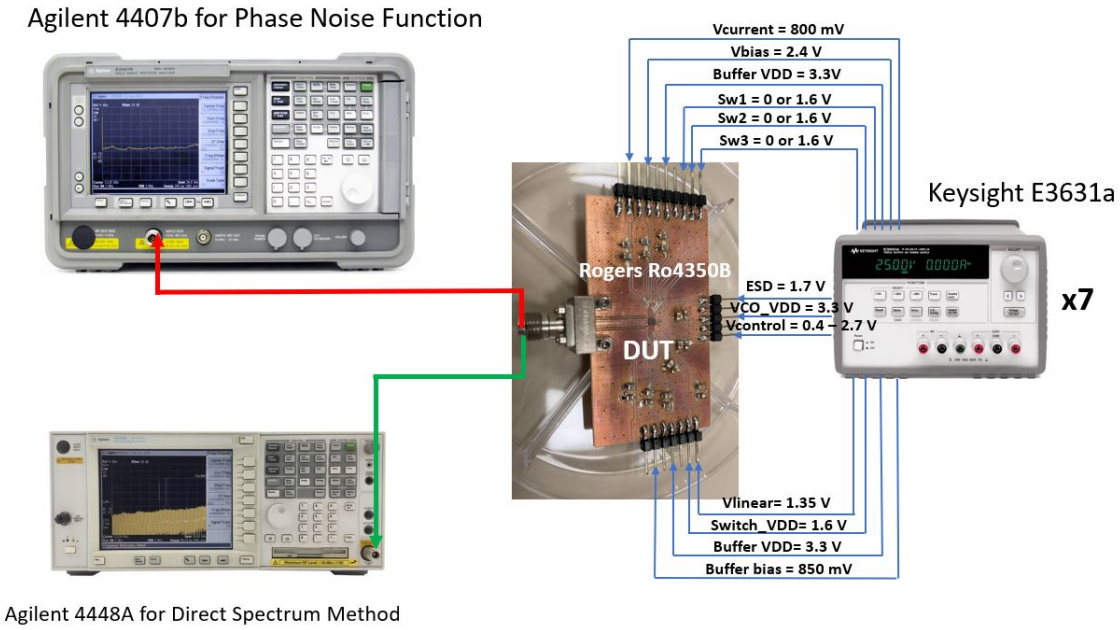
4. Measurement Methodologies & Results of the PLL

In this chapter, the measurement methodologies and setups are presented, as well as the completed results. Among the designed VCOs, only the 3-bit version is measured thoroughly, and the test setup for the second version is prepared by the time this thesis is written. This chapter presents the results of the 3-bit version and the test setup of the 4-bit version. On top of it the possible measurement methodologies for frequency divider and open/closed loop PLLs. The PFD/CP/LF block measurements done by Ajten Fejzullahu in her thesis work (Fejzullahu, 2022).

4.1 VCO Measurements

The two main parameters of the VCO to be measured are the oscillation frequency, tuning range, and phase noise. The measurements related to the frequency can be directly measured by using a spectrum analyzer, sweeping the control voltage of the VCO, and changing the capacitor bank bit configuration. However, the phase noise measurements require care to achieve correct results. Two different measurement methodologies for the phase noise have followed; the first one was measured with the most fundamental method, "Direct Spectrum," using an Agilent 4448A spectrum analyzer (SA), and the second method uses Agilent 4407b SA, which provides a phase noise specified functionality. The required bias voltages that the circuit requires are given from Keysight E3631a via jumper cables and headers that are soldered on the measurement printed circuit board. In addition to the measurement methods, the connection of the output of the VCOs to the SAs also creates a difference. The 3-bit VCO is designed for flip-chip assembly; thus, it requires a board design to achieve proper RF trace on the board. On the other hand, 4-bit VCO requires wire bond connections to a chip carrier and RF probes for the measurements. Only the 3-bit VCO could have been measured fully among the two versions. The following sections explain the steps that are followed for the measurement of the 3-bit VCO and the methodology to follow for the measurement of the 4-bit VCO.

4.1.1 3-bit VCO Flip-Chip Measurements



a

Figure 4.1 VCO Measurement Setup with Agilent 4407b and Agilent 4448A Spectrum Analyzers

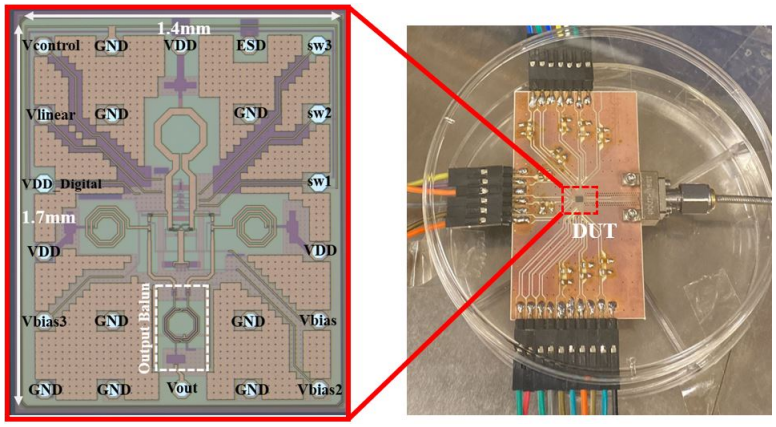


Figure 4.2 Flip-chip assembled Device Under Test

This version of the VCO is attached directly to the Rogers Ro4350b substrate using the flip chip method, as shown in Fig. 4.2. The initial choice of phase noise measurement was the direct spectrum method. During these measurements, the whole spectrum range was not scanned; only the capacitor bank operation and the output power were observed while keeping the control voltage at the minimum, which is 0.4 V. Further measurements for the two other samples are conducted with the "Phase Noise Functionality" of the Agilent 4407b, which are different from each

other since one of them has a malfunction at one of its capacitor banks. The next sections explain the measurement procedure starting from the board design.

4.1.1.1 Flip-Chip Test Board Design

The test board is designed using the Keysight Advanced Design System (ADS). The substrate parameters are added to the ADS, and a 50Ω matched line is designed for the VCOs output. The line is connected to an end-launch connector for the measurements. The designed board is shown in Fig.4.3, and its matching is shown in Fig.4.4. The bias voltages are given to the circuit by headers, and various decoupled SMD capacitors are added to bias lines.

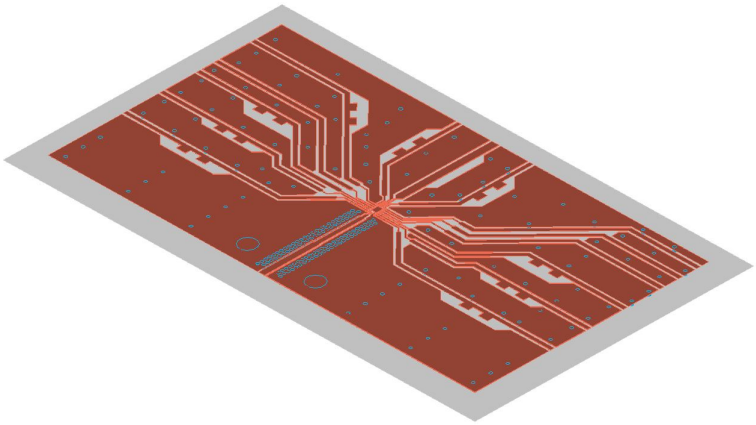


Figure 4.3 Test Board on Rogers 4350b

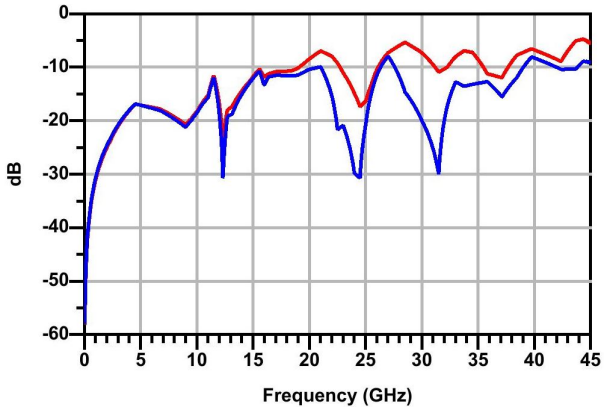


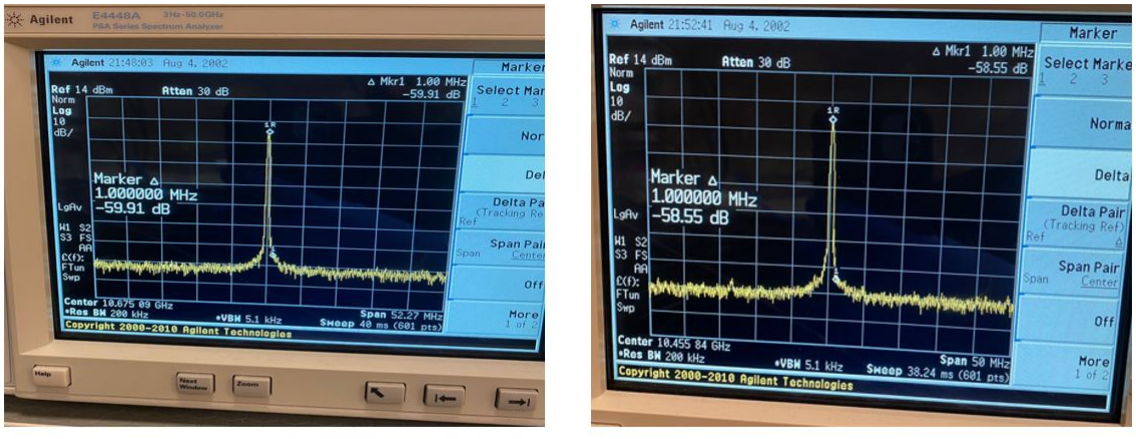
Figure 4.4 Matching of the RF-line on the Test Board

4.1.1.2 Direct Spectrum Method

The direct spectrum method requires applying the phase noise calculation theory manually. However, it is not feasible for the spectrum analyzer to calculate the power with 1 Hz resolution; even if it can somehow measure to results will not be correct. Also, small resolution bandwidths take longer for the analyzer to monitor the signal. Realistically, the RBW of an analyzer is set to 10 kHz or above for measurement. In this case, signals that are included in higher and lower offsets will add up as noise. For this reason, the theoretical PN calculation should be modified to (4.9). The calculated noise is normalized to the noise with the 1 Hz bandwidth.

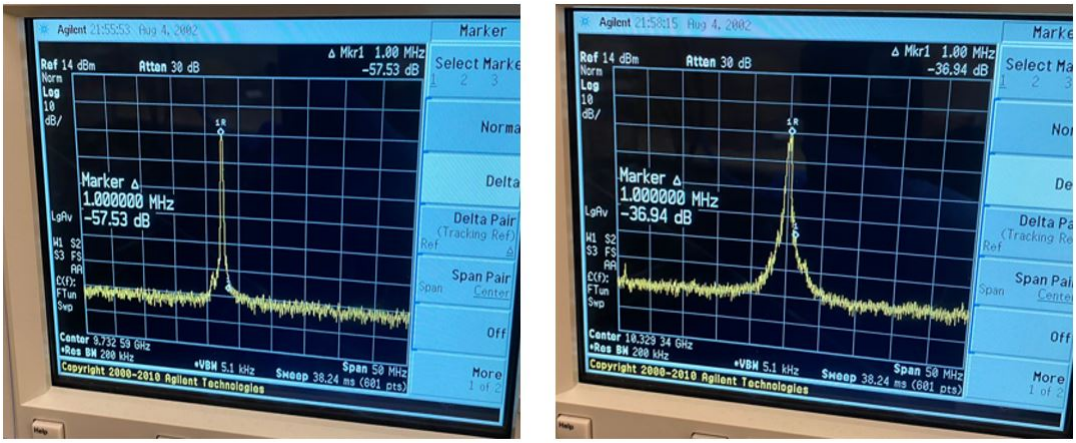
$$\mathcal{L}(\Delta f) = P_n(dBm/Hz) - P_{\text{carrier}} - 10 \cdot log(RBW) \tag{4.1}$$

With this measurement method, signal generators with known phase noises were measured first. These are the TI LMX2594EVM, the PLL evaluation board from Texas Instruments, and the two high-frequency signal generators in our lab. Based on the measurements of these sources, in addition to (4.9), an additional -5, -6 dBc should be subtracted from the calculated noise for an accurate phase noise measurement. During the measurements, it was observed that the 2nd bit in the capacitor banks did not work correctly and added extra phase noise to the circuit. In Fig.4.5 and Fig.4.6, phase noise measurements for different capacitor banks are shown. Fig.4.6(b) also shows the broadening in the spectrum when the 2nd bit is used.



(a) (b)

Figure 4.5 a) Bit Config : 000 PN = -116 dBc/Hz
b) Bit Config : 001 PN = -115.55 dBc/Hz



(a) **(b)**

Figure 4.6 a) Bit Config : 101 PN = -114.53 dBc/Hz
b) Bit Config : 010 PN = -95 dBc/Hz

Although measurements can be taken with the direct spectrum method, this method has been abandoned because it takes a lot of time and has a high margin of error. Instead, the measurement was taken with the Agilent 4407b spectrum analyzer, which has the "Phase Noise Measurement" function.

4.1.1.3 Measurement with Phase Noise Function

The PN measurement function inside the Agilent 4407b Spectrum analyzer provides phase noise measurement by optimizing the calculation techniques mentioned above and more. The only thing to be considered in this method is that if the analyzer cannot detect the carrier power correctly, it cannot measure the noise correctly. For this reason, the power of the carrier signal should be measured first from the spectrum analysis, and then this function should be used. Fig.4.1 shows the measurement setup used in this method. The output of the VCO is connected to the analyzer with an RF cable as in the previous method. DC voltages are required for the circuit provided by Keysight E3631a power supplies using jumper cables.

Again, in this setup, measurements were taken by connecting the above sources to understand the measurement method's accuracy. The same values as the measured phase noise shared by the companies can be observed in the datasheets of the signal generators without the need for extra calculations and calibrations.

VCO with the Defective Capacitor Bank bit:

In this measured sample, similar to the previous one, the first bit of the capacitor bank is malfunctioning. While it changes the oscillation frequency more than it

should, it causes a severe increase in phase noise. Fig.4.7a shows the spur forming and spectrum broadening with the activation of the first switch. The oscillation range is from 9.52 to 11.093 GHz, and the power consumption is 32.3 mW. However, there are blind zones between the tuning curves. The phase noise obtained with all the bank switches open (000 configurations) is -119 dBc/Hz, as shown in Fig. 4.7b. The PN at the center frequency is directly measured at 1 MHz offset, 100 different measurements are conducted, and their average is given in Fig. 4.8a. The analyzer occasionally cannot capture the carrier frequency in the log plot because the noise from power supplies causes changes in the oscillation frequency. Fig.4.8b shows the incorrectly measured carrier power in the log plot. The frequency tuning curves and the spectrum analysis at the center frequency are shown in Fig.4.9a and Fig.4.9b, respectively.

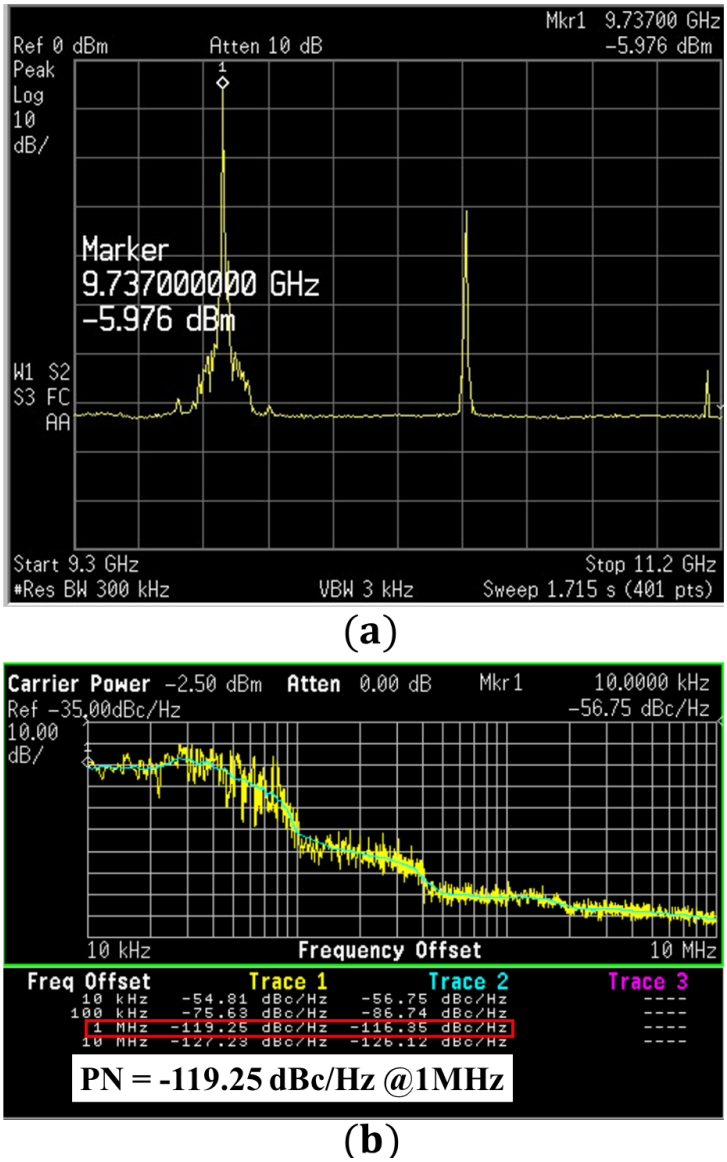
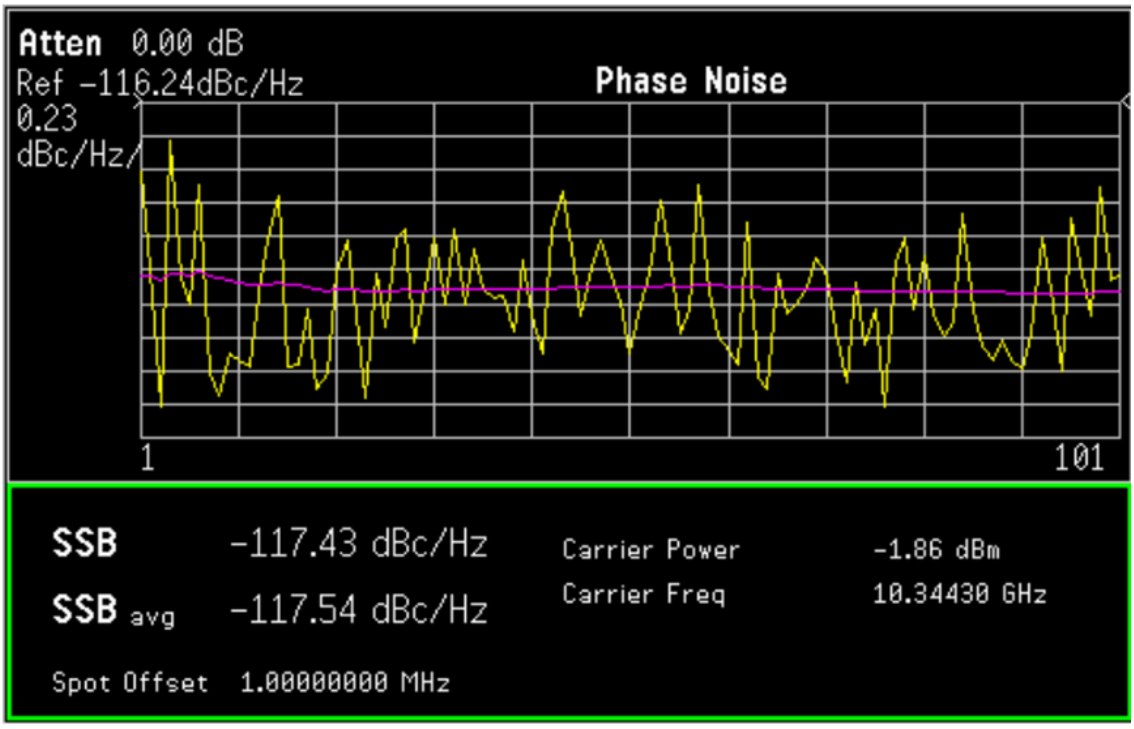
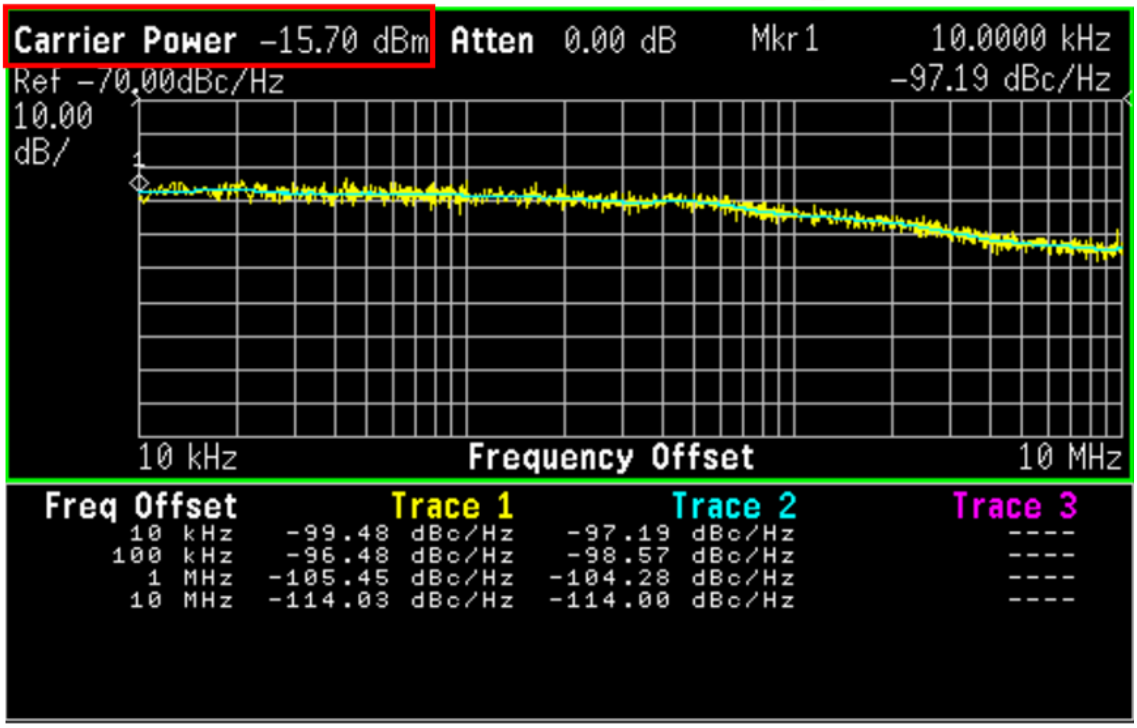


Figure 4.7 a) Spur Generation When 1st Switch Activated
b) PN Measurement with 000 Bit Configuration



(a)

Incorrect Carrier Power at Center Freq (10.34 GHz)



(b)

Figure 4.8 a) Average Phase Noise at 1MHz Offset
b) Wrong PN Measurement due to False Carrier Power Detection

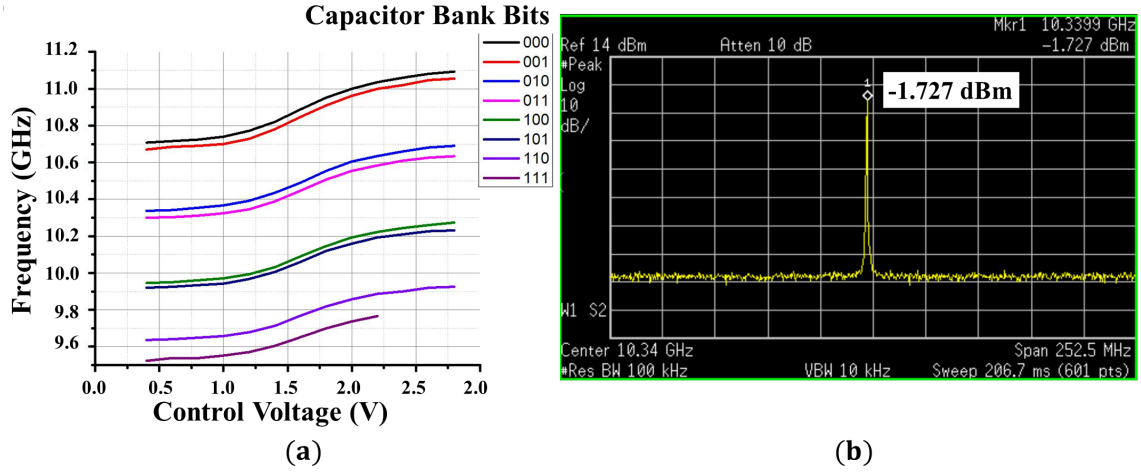


Figure 4.9 a) Frequency Tuning Curves
b) Spectrum Analysis at Center Frequency

Fully Functional VCO Measurements

In this sample, the capacitor banks operate without problems, and the measurement results are close to the post-layout simulations. The minimum PN measured is -116 dBc/Hz, and the PN at the center frequency is -114.42 dBc/Hz, as shown in Fig. 4.10. The achieved oscillation frequency range is 9.4612 to 11.092 GHz, and the power consumption is 28.7 mW. The center frequency spectrum view and the frequency tuning curves are given in Fig4.11.

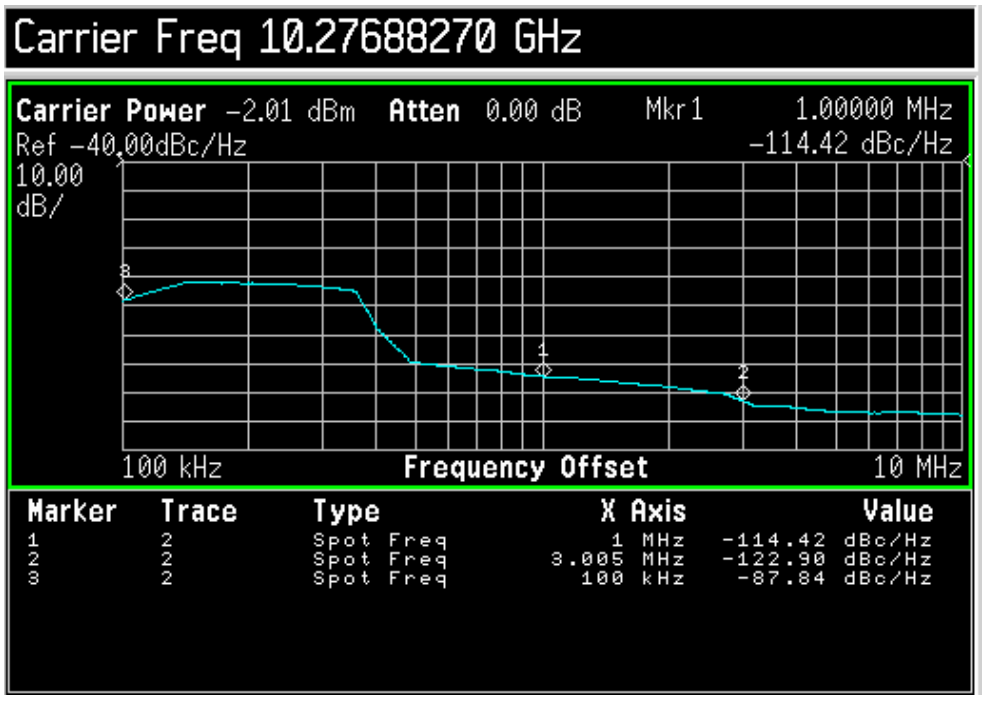


Figure 4.10 PN at Center Frequency

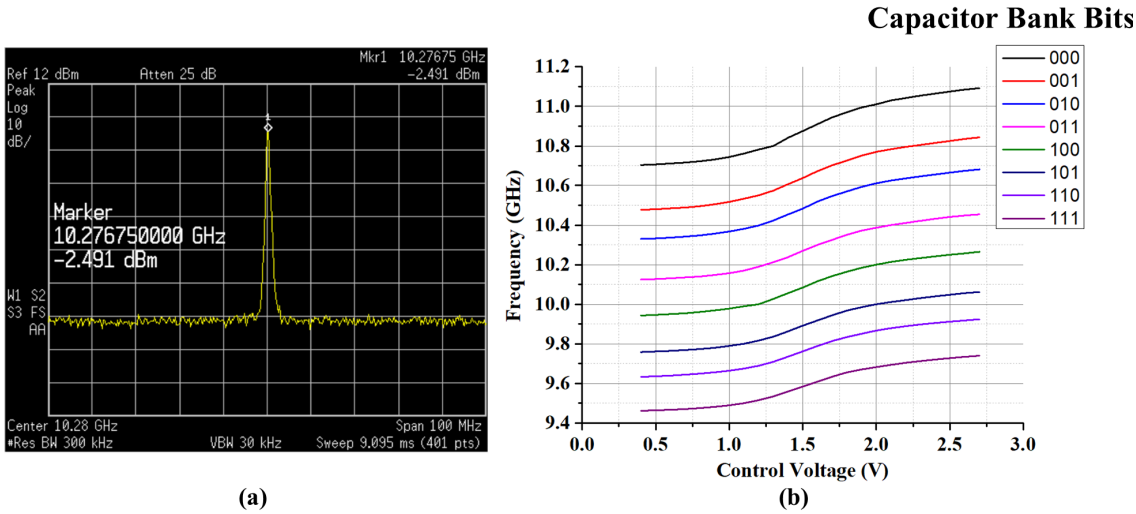


Figure 4.11 a) Spectrum View at Center Freq b) Measured Frequency Tuning Curves

The Table 4.1 compares the measured VCOs with the target specifications. Each DC bias of the design is provided externally; thus, they could be adjusted to achieve the best performance. An initial comparison can be made between the measurement results of the same chip. The 1st measurement with the defective capacitor bank employs a phase noise performance better than the post-layout simulations. The possible reason for this result is that the faulty switch is also not introducing the parasitics to the tank while its gate voltage is low; thus, higher tank quality leads to better PN. However, once the switch is activated, it causes a PN beyond the acceptable limit; also, to achieve the best phase noise performance, its current source bias is increased, leading to higher power consumption. Finally, due to the faulty switch, blind zones exist in the frequency tuning curves; thus, this sample is not considered a correct measurement. On the other hand, the second measured sample has not suffered from the defective capacitor bank, and the full frequency range could have been covered without any anomaly. Hence the second measurement is taken into consideration as the final result.

Table 4.1 Comparison of the Measurement Results with Target Specifications and Post-Layout Simulations

	Target Values	**Post-Layout Results**	**1st Measurement**	**2nd Measurement**
Phase Noise (dBc/Hz @1MHz)	-120 <	-115	-117.54	-114.42
Frequency Range (GHz)	9-12	9.12 - 11.02	9.52 - 11.093*	9.461-11.092
Center Freq (GHz)	10.5	10.07	10.3	10.276
Tuning Range (%)	28.57	18.87	15.27	15.88
Power Consumption (mW)	35-40 <	25	32.3	28.7

*Contains blind zone in the Tuning Curves

Compared to the post-layout simulation results, the PN is almost the same; however, the frequency range is shifted, with a more observable difference at the lower end. The capacitance coming from the flip-chip process and the process variations are two leading candidates for this shift. Also, the current source bias is slightly increased to achieve the sweet spot for the PN at the center frequency, leading to higher power consumption. Finally, due to the frequency shift, the center frequencies of the simulations and the measurements are changed; thus, if the optimized PN performance of the simulations results in the center frequency of the measurements, it is likely to obtain better performance than the obtained results.

The comparison of the performance metrics of the measured 3-bit VCO design with its counterparts in the literature is given in Table. 4.2. The measured VCO has one magnitude of order better power consumption and offers double the TR, where (Hyvert et al., 2016) has a better PN of -120 dBc/Hz. On the other hand, it outperforms the (Sadhu et al., 2018) by PN performance sense with a similar power consumption performance; however, the tuning range of the other design is slightly more extensive than the measured VCO in this work. The proposed work surpasses the other works in the literature by all means; thus, they are not explicitly analyzed.

Table 4.2 Comparison of the Measured VCO with Similar Counterparts in the Literature

	Phase Noise (dBc/Hz)	**Center Frequency (GHz)**	**Tuning Range (%)**	**Power Consumption (mW)**	**Technology**	**FoM**	**FoM$_T$**
(Hyvert et al., 2016)	**-120 @1 MHz**	**14.12**	**%8.9**	**233**	**0.25 μm SiGe:C BiCMOS**	**178.95**	**177.9**
(Jamal et al., 2018)	**-99 @1MHz**	**27.32**	**%30.2**	**45**	**130nm SiGe BiCMOS**	**172**	**182**
(Pohl et al., 2012)	**-108 @1MHz**	**21.75**	**%17.4**	**60**	**0.35 μm SiGe:C BiCMOS**	**176**	**181**
(Hyvert et al., 2015)	**-97 @100 kHz**	**14.24**	**%9.1**	**123**	**0.25 μm SiGe:C BiCMOS**	**179.3**	**178.5**
(Sadhu et al., 2018)	**-110.6 @1 MHz**	**17.5**	**%17.1**	**27.5**	**130nm SiGe BiCMOS**	**181.07**	**185.75**
Measured VCO	**-114.42 @1 MHz**	**10.276**	**%15.88**	**28.7**	**130nm SiGe BiCMOS**	**180.1**	**182.1**

FoM = -$\mathcal{L}(\Delta\omega)$ + $20log(\frac{f}{\Delta f})$ - $10log(\frac{DCPower}{1mW})$ FoM$_T$ = FoM + $10log(\frac{TR}{10})$

4.1.2 Wirebonded 4-bit VCO Measurement Setup Considerations

Unlike the flip-chip assembly, the 4-bit VCO, designed for the wire bond, does not require any design effort on the PCB. In order to measure the design, two dies are epoxied on a 44-pin chip carrier, and the DC pads are connected to the carrier with gold wire bonds. The wire bond diagram and the bonded chips are shown in Fig.4.12. The package is soldered on an FR4 substrate for providing the DC voltages via headers. However, due to its high inductance, the RF output connection can not be made with a wire bond. Thus, an RF probe should be used for the measurements. Fig.4.13 shows the measurement setup, the 50Ω matched RF probes, which have the pin configuration of ground-signal-ground, will be lowered to the output pad of the VCO and then will be connected to the SA with an RF cable. Later the PN will be measured with Agilent 4407b's phase noise personality.

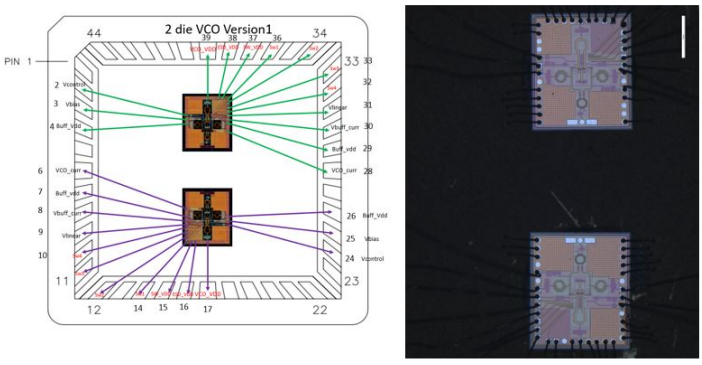


Figure 4.12 The bonding diagram for the VCO and its realization on a 44pin Chip Carrier

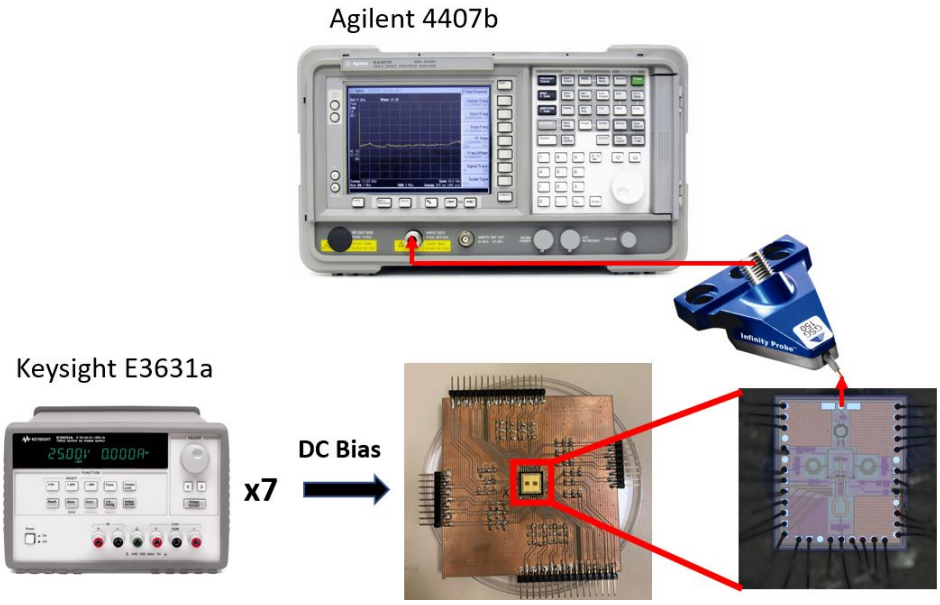


Figure 4.13 The Measurement Setup For the 4-bit VCO

4.2 Frequency Divider Measurement Setup Considerations

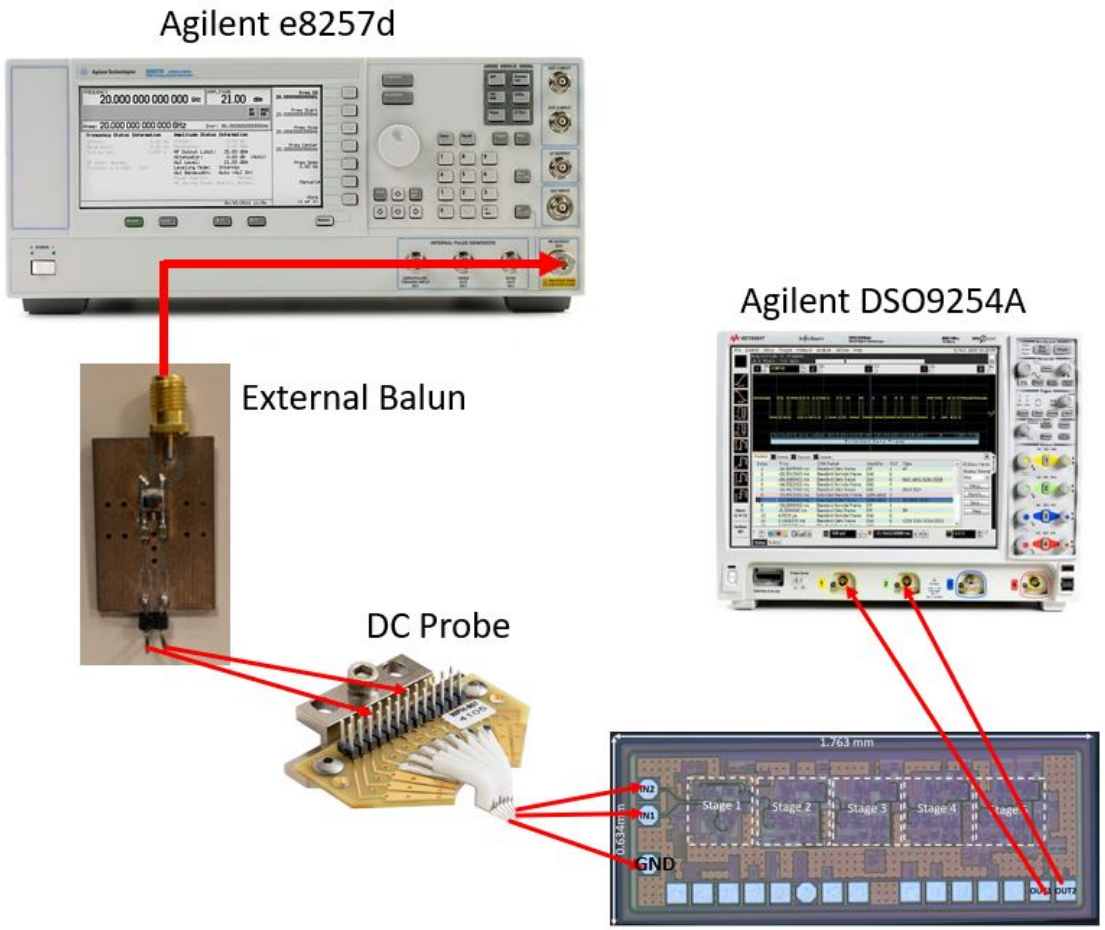


Figure 4.14 Divider Measurement Setup

The divider is also designed for the wire-bond assembly and will be epoxied to a chip carrier. The drawback of this design is that the differential RF inputs are unsuitable for the probes. Thus, a DC probe can be used to give differential inputs to the pads of the die since the signal loss is not a concern for initial measurement. An Agilent e8257d PSG Analog signal generator will provide the 9-12 GHz input, and by using an external balun, the signal will be converted to differential to be provided to the divider. Finally, the wire-bonded low-frequency output of the divider can be measured from headers on the test board using an Agilent DSO9254A 2.4GHz Digital Oscilloscope. Fig. 4.14 shows the candidate measurement setup.

4.3 Open & Closed Loop PLL Measurement Setup Considerations

4.3.1 Open Loop Measurement Setup

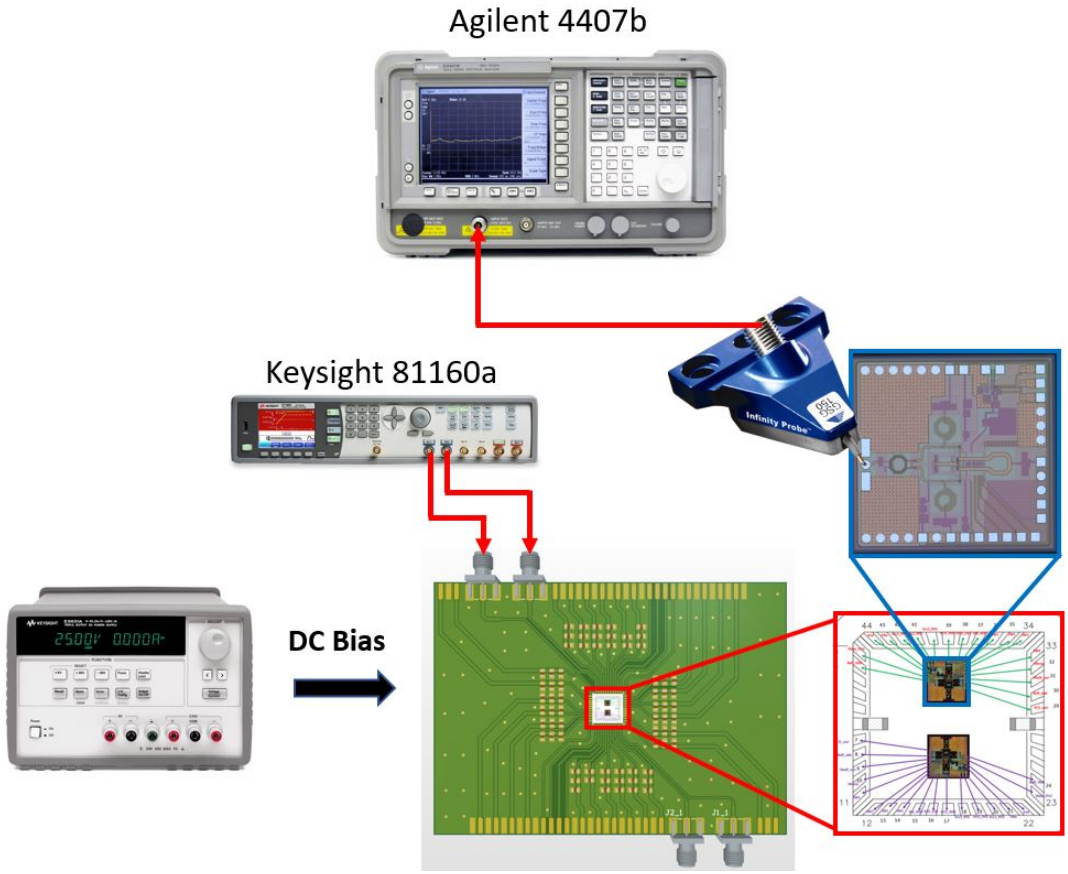


Figure 4.15 Open Loop Measurement Setup

The measurement of the open loop system containing the VCO and PFD/CP/LF components is essential to understand how well they work together and the control voltage's effect on VCO will change the phase noise. The measurement setup for the open loop is given in Fig. 4.15. Due to a few pads added to VCOs on the die, two devices can be connected to a 44-pin chip carrier. Decoupling capacitors are added to the chip carrier ground to prevent ground bounce for the PFD block. Except for the RF output of the VCO, all the pad connections can be made with wire bonding. A Keysight 81160a arbitrary signal generator will be used to provide two input signals to the PFD representing the feedback signal and the reference signal. VCO's frequency change can be observed via Agilent 4407b SA by controlling these signals' phases. This change can be compared with the simulation results, and it can be understood if the PFD/CP/LF blocks provide the correct control voltage with a leading or lagging feedback signal.

4.3.2 Closed Loop Measurement Setup

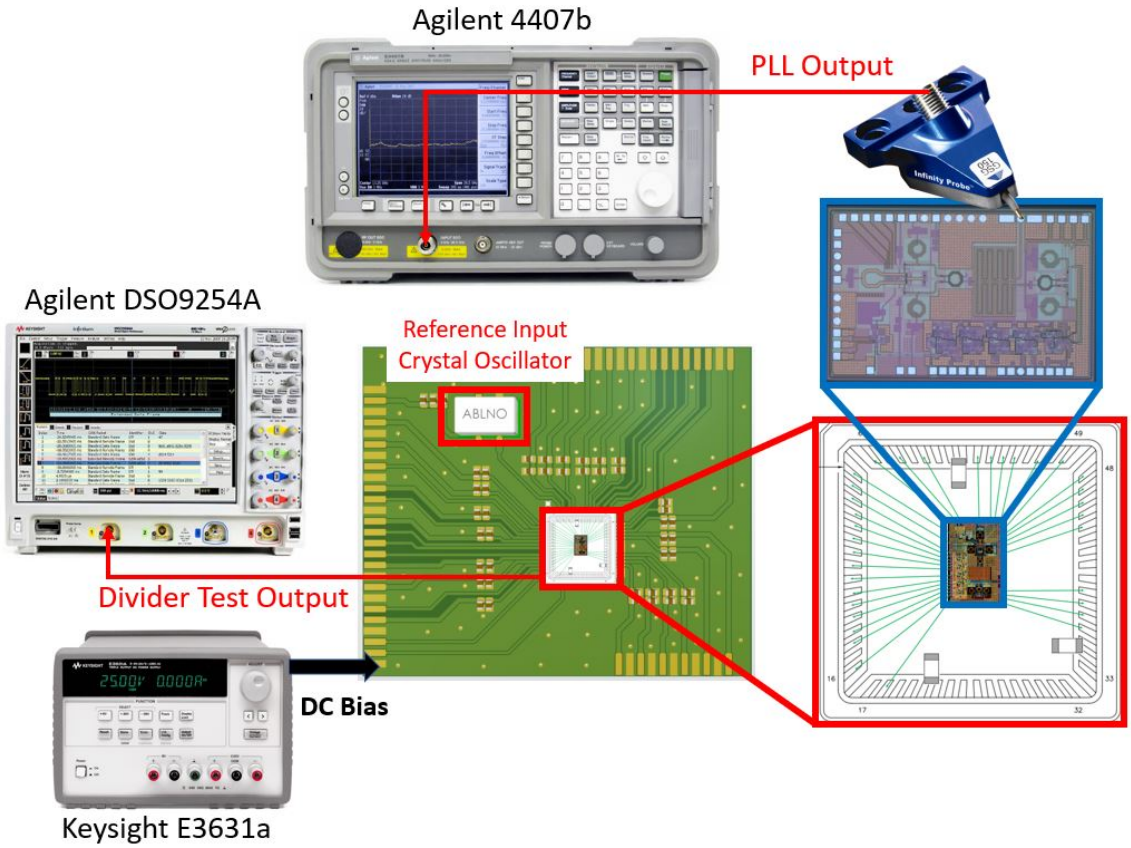


Figure 4.16 Closed Loop Measurement Setup

The closed loop assembly requires a 64-pin chip carrier due to its high pad number; decoupling capacitors are added to the carrier to prevent ground bouncing. The candidate setup for the closed loop measurements is given in Fig. 4.16. The ABRACON ABLNO crystal oscillator will provide the reference signal to the system; other than that, the only input to the setup is the DC biases. The output of the PLL can be monitored with Agilent 4407b, and phase noise can be measured with its phase noise functionality as done with the VCO measurements. Furthermore, the divider's test output can be checked with Agilent DSO9254A digital oscilloscope to understand the system's lock condition. A trigger level can be set, and with the system's start-up, the time it takes for the divider's output to get stable frequency will give the system's settling time.

5. CONCLUSION AND FUTURE WORK

5.1 Summary of the Work

The improvements in wireless systems enabled the communication systems to expand their market to various applications, which was reflected as the raised data transmit and receive traffic. Extending the bandwidth of the wireless communication frequency spectrum is a solution that meets the new data transfer requirements. However, the frequency spectrum of the recent generation systems, which is lower than 6 GHz, is crowded with several applications such as WiMAX and WiFi. Hence, millimeter wave (mmWave) bands are seen as a significant candidate due to promising a wide bandwidth and increased capacity for the 5th generation (5G) of wireless communication systems. The realization of 5G communication networks in mmWave bands reflects a 20 Gbps of data rate. In order to achieve the target data rates, the system SNR should be maximized. The performance of the LO signal and its distribution along the transceiver in the 5G systems is the critical element for the high SNR. In order to achieve a clean LO signal, a Type-II fourth order Integer-N frequency synthesizer with -120 dBc/Hz PN at 1 MHz is examined.

The PN of the VCO is the limiting factor of a frequency synthesizer. In this work, two different VCOs that use three and four-bit capacitor banks are realized. The cross-coupled topology is selected in the realization of the circuits. In order to minimize the phase noise while achieving the required tuning range, an effort is made to optimize the tank circuit components. Firstly, a stacked inductor design is tested and improved to achieve maximum Q with minimum inductance; furthermore, a varactor linearity control mechanism is examined. This control method aimed to increase the Cmax/Cmin ratio while minimizing the loss of quality factor. Adjusting the linearity voltage allows an optimum point for the maximum tuning range with a minimum PN increase. This method is also experimentally verified. The simulation results of the 4-bit VCO exhibit a 9.5-12.02 GHz tuning range while achieving -116.2 dBc/Hz @1MHz phase noise with 30mW power consumption. Also, the 3-bit VCO

is measured, and a tuning range between 9.451-11.092 GHz tuning range is achieved, with a -114.42 dBc/Hz PN with 28.7 mW power consumption. On top of the VCO designs, the full CML base divider topology is optimized to achieve better area and dynamic power consumption by implementing lower frequency stages with CMOS logic. CMOS logic dividers consume 7.7 mW, while a CML divider consumes 380 mW.

5.2 Future Work

The 3-bit VCO measurements are completed, and the first thing to be done is to complete the 4-bit VCO measurement, and comparison should be made if the standard CMOS or the HVCMOS operates close to the simulation results; this comparison will decide which device will be used in the next design. Furthermore, the capacitor bank bits should be modified to achieve a full tuning range of 9-12 GHz with a margin. On top of it, the measurement of the remaining blocks, divider, open and closed loop PLLs, should be completed before making further modifications. For the upcoming tapeouts, designing a closed loop PLL with an external loop filter should be considered because, in this manner, the optimum loop bandwidth for the minimum phase noise can be found by changing the SMD capacitors and resistors.

Another effort should be made to improve the measurability of both the sub-blocks and the whole system. Firstly, the output balun used for the VCO can be placed at the input of the divider for its standalone measurements. Moreover, a lock detector can be implemented to increase the observability of the lock condition of the PLL.

Lastly, once the PLL design is complete, it can be combined with the frequency doubler and the divider for the complete frequency synthesizer operation for the 5G sliding-IF Architecture.

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