HIGH ISOLATION DOUBLE-BALANCED DOWN-CONVERTER MIXER COMBINED WITH ACTIVE BALUN AND FREQUENCY SYNTHESIZER IN SIGE BICMOS FOR 5G APPLICATIONS

by
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Aileme...
To my family...

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High Isolation Double-Balanced Down-Converter Mixer combined with Active Balun and Frequency Synthesizer in SiGe BiCMOS for 5G Applications

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Keywords: mm-wave integrated circuit, SiGe BiCMOS, K-Ka band, down-converter, Gilbert Cell mixer, frequency synthesizer, PLL, VCO, PFD, CP, LF.

Abstract

In this thesis, the design of high isolation down-converter mixers for 5G applications is scrutinized. Sliding IF transceiver architecture appropriate frequency synthesizer is researched and designed. The frequency synthesizer consists of integer-N fourth order Type-II PLL, a frequency double, and a frequency divider by two. To effectively combine the digital/analog circuits with the RF blocks, the IHP's 130 nm SiGe BiCMOS technology is employed.

The proposed mixer achieves high isolation even though the input RF signal is applied as single-ended. The RF leakages are prevented by employing a resonator at the emitter of the transconductance stage, such that the isolation values are equivalent to the ones of the double-balanced mixer. For 26 GHz, the conversion gain (CG) is -7.72 dB. The corresponding 1dB input compression point (IP_{1dB}) is 5.7 dBm. The RF-IF, LO-RF, and LO-IF isolations are above 35 dB, 45 dB, and 35 dB, respectively. The power consumption is 56 mW with a 3.3 V voltage supply, and the active area without the pads is 1 mm^2.

The PLL block consists of a voltage-controlled oscillator (VCO), a phase frequency detector (PFD), a charge pump (CP), a loop filter (LF), and integer-N divider. The VCO has a phase noise of -114 dBc/Hz, tuning range of 15.88 %, power consumption of 28.7 mW, and an area of 2.3 mm^2. The simulated phase noise of the closed loop PLL is -108.7 dBc/Hz.

5G Uygulamaları için SiGe BiCMOS'ta Aktif Balun ile birleştirilmiş Yüksek İzolasyonlu Double-Balanced Frekans Düşürücü Karıştırıcısı ve Frekans Sentezleyici

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Özet

Bu tezde, 5G uygulamaları için yüksek izolasyonlu frekans düşürücü karıştırıcısı tasarımı incelenmiştir. Sliding IF alıcı-verici mimarisine uygun frekans sentezleyici araştırılmış ve tasarlanmıştır. Frekans sentezleyici, tamsayı-N dördüncü dereceden Tip-II faz kilitlemeli döngü'den, bir frekans çiftleyici'den ve bölü iki frekans bölücüden oluşur. Dijital/analog devreleri RF bloklarıyla etkin bir şekilde birleştirmek için IHP'nin 130 nm SiGe BiCMOS teknolojisi kullanılır.

Önerilen karıştırıcı, giriş RF sinyali single-ended olarak uygulanmasına rağmen yüksek izolasyon sağlamaktadır. Transkondüktans kademesinin emitöründe rezonatör kullanılarak RF sızıntıları engellenir, izolasyon değerleri double-balanced karıştırıcısına denk gelir. 26 GHz için dönüştürme kazancı (CG) -7,72 dB'dir. Karşılık gelen 1dB giriş sıkıştırma noktası (IP_{1dB}) 5,7 dBm'dir. RF-IF, LO-RF ve LO-IF izolasyonları sırasıyla 35 dB, 45 dB ve 35 dB'nin üzerindedir. Güç tüketimi 3,3 V voltaj kaynağı ile 56 mW'dir ve pedler olmadan aktif alan 1 mm^2'dir.

PLL bloğu, gerilim denetimli bir osilatör (VCO), faz frekans dedektörü (PFD), yük pompası (CP), döngü filtresi (LF) ve tamsayı-N bölücüden oluşur. VCO, -114 dBc/Hz faz gürültüsüne, %15,88 ayarlama aralığına, 28,7 mW güç tüketimine ve 2,3 mm^2 alana sahiptir. PLL'nin simüle edilmiş kapalı döngü faz gürültüsü -108.7 dBc/Hz'dir.

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List of Abbreviations

AVG	Average
BJT	Bipolar Junction Transistor
CG	Conversion Gain
CL	Conversion Loss
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common-Mode Rejection Ratio
CP	Charge Pump
CPW	Co-Planar Waveguide
DSB	Double-Sidebands
FoM	Figure of Merit
HBT	Heterojunction Bipolar Transistor
IC	Integrated Circuit
IF	Intermediate Frequency
$\mathbf{IIP_3}$	Input Third Order Intercept Point
IL	Insertion Loss
IM	Image Frequency
$\mathbf{IM_3}$	Third Order Intermodulation Products
$\mathbf{IP_{1dB}}$	Input 1-dB Compression Point
IRR	Image Rejection Ratio
LDO	Low Dropout Regulator
LF	Loop Filter
LNA	Low Noise Amplifie
LO	Local Oscillator
MIM	Metal-Insulator-Metal
NF	Noise Figure
PCB	Printed Circuit Board
PD	Phase Detector
PFD	Phase-Frequency Detector
PLL	Phase-Locked Loop
PM	Phase Margin
PN	Phase Noise
PS	Phase Shifter
PSG	Programmable Signal Generator
Q	Quality Factor
RF	Radio Frequency
SA	Spectrum Analyzer
SD	Standard Deviation
SDM	Sigma-Delta Modulator
SiGe	Silicon-Germanium
SSB	Single-Sideband
TL	Transmission Line
TR	Tuning Range
VCO	Voltage Controlled Oscillator
VNA	Vector Network Analyzer

1 Introduction

1.1 Phase Locked Loops and Frequency Synthesizers

Phase locked loop (PLL) is a closed loop negative feedback system used to adjust the output frequency and phase of the oscillator to the input frequency and phase of the reference signal. The mathematical representation of feedback control systems was introduced by J.C.Maxwell in [9]. In the 1930s, the synchronous homodyne receiver was one of the early investigations on phase lock [10]. The homodyne receiver/direct conversion receiver converts the high-frequency input signal directly to the baseband, such that the local oscillating (LO) signal frequency is equal to the one of the RF signal, as shown in Fig. 1.1 (c). In this case, the circuit becomes a phase detector between the two input frequencies. The heterodyne and superheterodyne receiver architectures are depicted to show the complexity differences between these architectures, Fig. 1.1 (a) - (b). In the televisions, the synchronization of the horizontal and vertical scans was enabled through phase lock receivers [11].

In the 20th century, economical and technological motivations pushed the performance metrics of the telecommunication standards. A cellular phone contains the digital & baseband back-end circuitry, enabling the processing of the data, and the RF & IF analog front-end circuit, the wireless communication [12]. The transmitted and received signals are up-converted and down-converted through a mixer. This mixer requires a local oscillating signal to enable frequency conversion. The local oscillating signal is generated through an oscillator and controlled through the

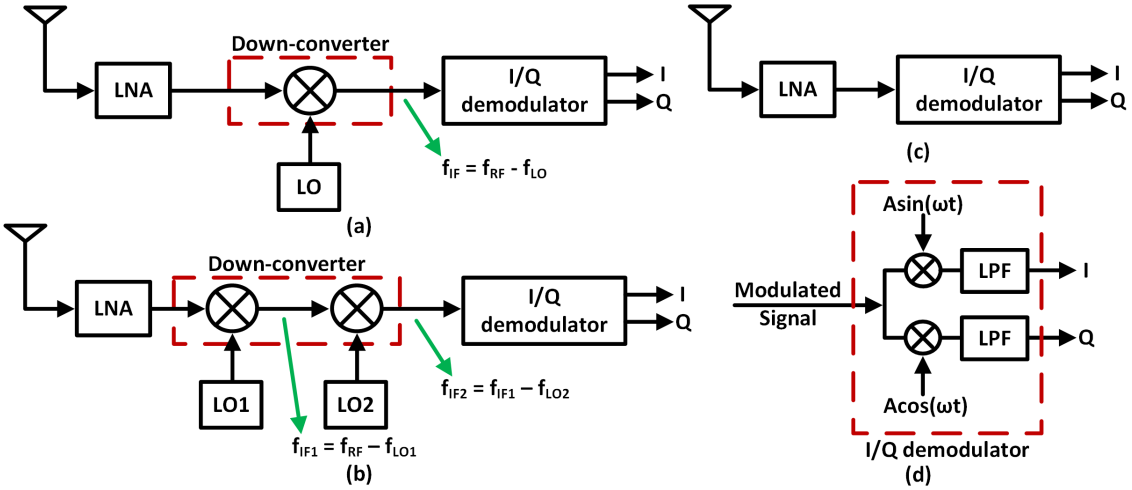


Figure 1.1: Block diagram of (a) heterodyne, (b) superheterodyne, and (c) homodyne receiver architecture; and (d) I/Q demodulator employed in receivers.

PLL, frequency synthesizer. For cellular application, power consumption must be minimum for maximum recharging battery life, low phase noise to avoid adjacent channel interference and to increase the number of simultaneously on channels, and fast frequency switch to avoid interferences to other channels [13].

High-frequency systems have attracted the interest of the scientific world due to the low bandwidth available at low frequencies. In the mm-wave, the losses increase, while large bandwidths are available for higher data rates and users. The next generation of mobile networks (5G) is proposed that can be in the mm-waves and E-band (71-76 GHz, 81-86 GHz, 92-95 GHz) frequency ranges [14]. A 5G prototype for the 24-30 GHz frequency range was proposed for Winter Olympics in Korea [15].

1.2 Motivation

The receiver architecture determines the complexity of the down-converter from the mm-waves to the baseband. The LO signal distribution technique can be challenging. The distribution of the LO signal from a conventional frequency synthesizer to different receivers can cause amplitude and phase imbalances [16]. Furthermore, the distribution of the LO signal at the board level is area-consuming, and the high PCB losses at high LO frequencies reduce performance values. The solution is provided at a 60 GHz transceiver which integrated a PLL [17]. In this way, only the input reference signal must routed in the PCB level, and the number of transceiver blocks can be easily modified.

The sliding IF transceiver architecture is suggested to minimize the high frequency and accurate quadrature LO signal specifications [18]. Furthermore, for conventional superheterodyne architectures, multiple oscillators are employed, which results in high leakages between the oscillators [1]. Other works have also proposed the sliding IF architecture for 5G applications [19–21].

The proposed frequency synthesizer is suitable for sliding IF transceiver architectures, as shown in Fig. 1.2. The divide by two architecture does not require additional circuitry for the I/Q signal generation. This architecture reduces the complexity, area, and power consumption of the circuitry.

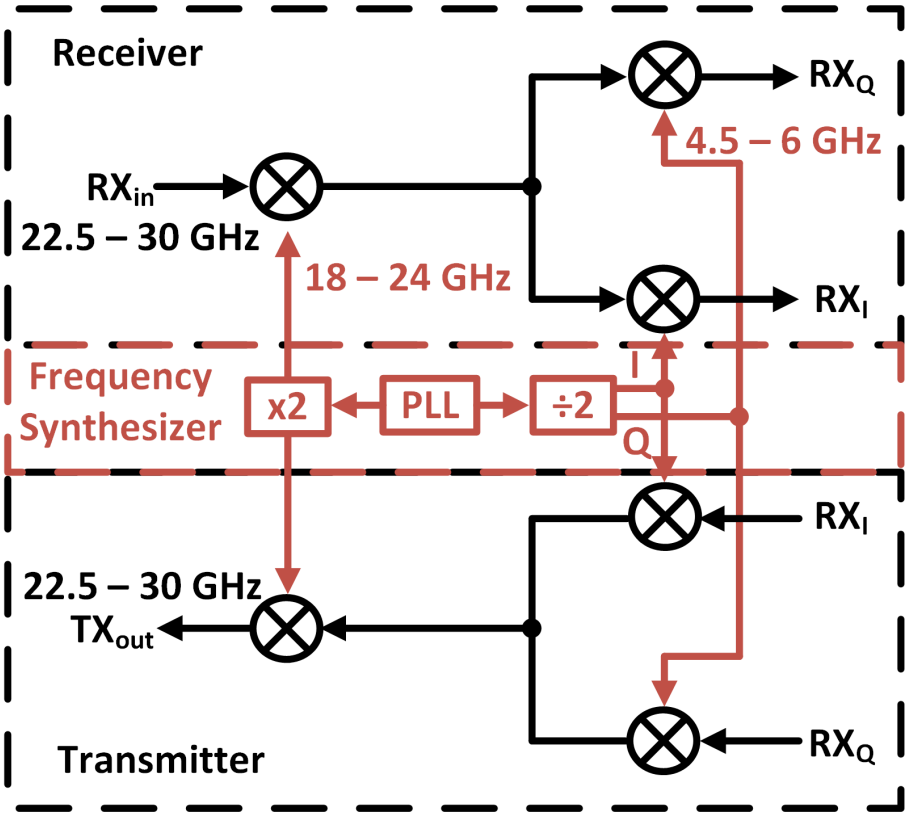


Figure 1.2: Block diagram of frequency synthesizer with sliding-IF transceiver.

1.3 Technology Selection

The technology selection is considered the frequency synthesizer system and its 5G application. The frequency synthesizer consists of RF, analog, and digital blocks. So, the technology employed must be able to operate in high frequencies, for the RF blocks; mixer, VCO, doubler, divide by 2. Moreover, high linearity, adequate gain, low noise, and low cost is required. Exceptional CMOS (Complementary metal-oxide semiconductor) integration is essential for the digital and analog blocks. Several technologies are going to be scrutinized to select the most suitable one.

The III-V semiconductor technologies are superior in terms of frequency response, noise, power consumption, and linearity compared to the other technologies. The advantages of the CMOS technology are its low cost, high yields, and low power consumption [22]. The SiGe heterojunction bipolar transistor (HBT) offers a similar frequency response as one of the III-V technologies. SiGe HBT technology is suitable for applications where high-frequency response, low noise figure, excellent CMOS integration, and low fabrication cost are necessary. The summary of the performance comparison of different device technologies is presented in Table 1.1.

Considering the above mentioned performance necessities and the available technologies. The proposed designs are fabricated in IHP's 130 nm SG13S2 SiGe BiCMOS technology. This technology offers HBTs with f_t/f_{max} of 250/340 GHz and BV_{CEO} of 1.8 V. Moreover, this technology offers CMOS devices with breakdown voltage of 2.7 V and -3.1 V for the NMOS and PMOS devices, whose maximum applicable base and drain voltages are 1.2 V. The high voltage counterparts of these devices exist as HVNMOS and HVPMOS with breakdown voltages of 6.1 V and -5.6 V, respectively. The maximum base and drain voltage values are 3.3 V.

Table 1.1: Relative Performance Comparison of Various Device Technologies for RFICs [6].

Performance Metric	SiGe HBT	Si BJT	Si CMOS	III-V MESFET	III-V HBT	III-V HEMT
Frequency response	+	0	0	+	++	++
1/f and phase noise	++	+	-	–	0	–
Broadband noise	+	0	0	+	+	++
Linearity	+	+	+	++	+	++
Output conductance	++	+	-	-	++	-
Transconductance/area	++	++	–	-	++	-
Power dissipation	++	+	-	-	+	0
CMOS integration	++	++	N/A	–	–	–
IC cost	0	0	+	-	-	–

Excelent: ++; Very good: +; Good: 0; Fair: -; Poor:–

1.4 Organization

In the first chapter, the frequency synthesizers for 5G applications are scrutinized. Their importance and operation are underlined. The technology selection is justified according to the proposed designs. The motivation of this thesis is emphasized for the 5G application. Finally, the thesis structure is reported.

In the second chapter, the design of the double-balanced down-converter mixer combined with active balun is going to be scrutinized. The mixer fundamentals, architectures; and the down-converter mixer in a system are described. The proposed mixer is described. The isolation and conversion gain parameters are derived considering the parasitic capacitances. The design procedure is justified by simulation results. The measurement results are compared with the chip and chip with board simulations. The comparison of the measured mixer with other mixers from the literature are presented. The multi-technology RFPro simulation setup is discussed and its simulation results are presented. Finally, an area vise improved chip is presented with its simulation results, while the performance metrics are not degraded.

In the third chapter, the design of a fourth order Type-II analog PLL for frequency synthesizer is going to be scrutinized. The PLL architectures, parameters, and fundamentals are described. The linear approximation analysis of the PLL block to derive open and closed loop transfer functions is completed. The effect of each noise source on the total phase noise is predicted through the noise transfer functions. The design procedure of each sub-block and system is justified by simulation results. Finally, the measurement results and comparison of the measured blocks with their corresponding blocks in the literature are presented.

In the fourth chapter, the summary of this thesis and the future steps to be completed are described.

2 Down-Converter Mixer

In this chapter, the design of the double-balanced down-converter mixer combined with active balun is going to be scrutinized. The mixer fundamentals and the down-converter mixer in a system are described. The design procedure is justified by simulation results. The measurement results are compared with the chip and chip with board simulations. Finally the comparison of the measured mixer with other mixers from literature are presented.

2.1 Mixer Fundamentals

The block diagram view of the down-converter mixer is shown in Fig. 2.1(a). It is a three-port device that down-converts the input frequency to a lower frequency range. The two inputs are the RF and LO ports, the RF is fed with the input signal, while the LO is fed with the local oscillator which enables the down-conversion from RF to IF frequency, as shown in Fig. 2.1(b). The IF is the output port. For the up-converter mixer, the input port is the IF and the output port is the RF, due to the frequency ranges. RF represents the radio-frequency range, while IF is the intermediate-frequency one. In theory, a mixer can be designed through any nonlinear device, a diode or a transistor. The "mixing" of the RF and LO signals generates the output signal which are the harmonics and the the difference or sum of multiples of the RF and LO signals. For the downconverter case the difference between the RF and LO frequencies is taken through a low pass filter (LPF), as shown in (2.1.1) - (2.1.3) [1].

$$V_{IF}(t) = LPF\big[A_{RF}\cos(\omega_{RF}t)A_{LO}\cos(\omega_{LO}t)\big] \tag{2.1.1}$$

$$V_{IF}(t) = LPF\left[\frac{A_{RF}A_{LO}}{2}\big[\cos((\omega_{RF}-\omega_{LO})t)+\cos((\omega_{RF}+\omega_{LO})t)\big]\right] \tag{2.1.2}$$

$$V_{IF}(t) = \frac{A_{RF}A_{LO}}{2}\cos((\omega_{RF}-\omega_{LO})t) \tag{2.1.3}$$

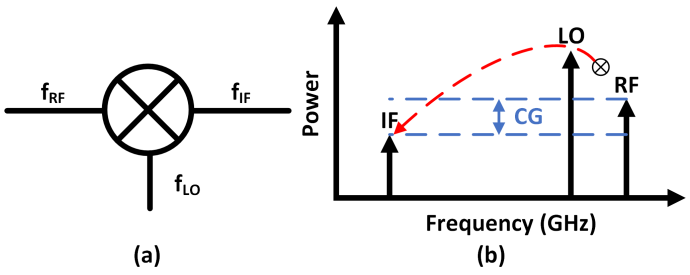


Figure 2.1: (a) Block diagram of down-conversion mixer, (b) graphical representation of down-conversion operation.

2.1.1 Mixer Parameters

The conversion gain (CG) represents the difference between the RF power and IF power in dB scale, as shown in Fig 2.1(b) and in (2.1.4). The CG is observed when the IF power is higher than the RF one. The conversion loss (CL) is observed when the RF power is higher than the IF one, this value can be represented with negative valued CG. The voltage CG is found through the division of the RMS output voltage to the RMS input voltage. When identical source and load impedances are employed the voltage CG is equal to the power CG in dB scale.

$$CG(dB) = P_{IF}(dBm) - P_{RF}(dBm) \tag{2.1.4}$$

The linearity of a mixer is described through the input 1 dB compression point (IP_{1dB}) and the input third-order intercept point (IIP_3). The IP_{1dB} is input power in which the measured output power has deviated by 1 dB from the ideal linearly increasing output power, with a slope of 1, as shown in Fig. 2.2. At close input power values of IP_{1dB}, the behavior of the mixer is unreliable. Moreover, inter-modulation distortion levels are increased and the CG is decreased. As the RF signal deviates from the small-signal condition, the input compression point occurs [3]. Higher RF input levels than the IP_{1dB} will result in amplitude modulation and phase modulation [2]. In this case, data errors will occur in quadrature amplitude modulation (QAM) architectures. The effects of the inter-modulation distortions

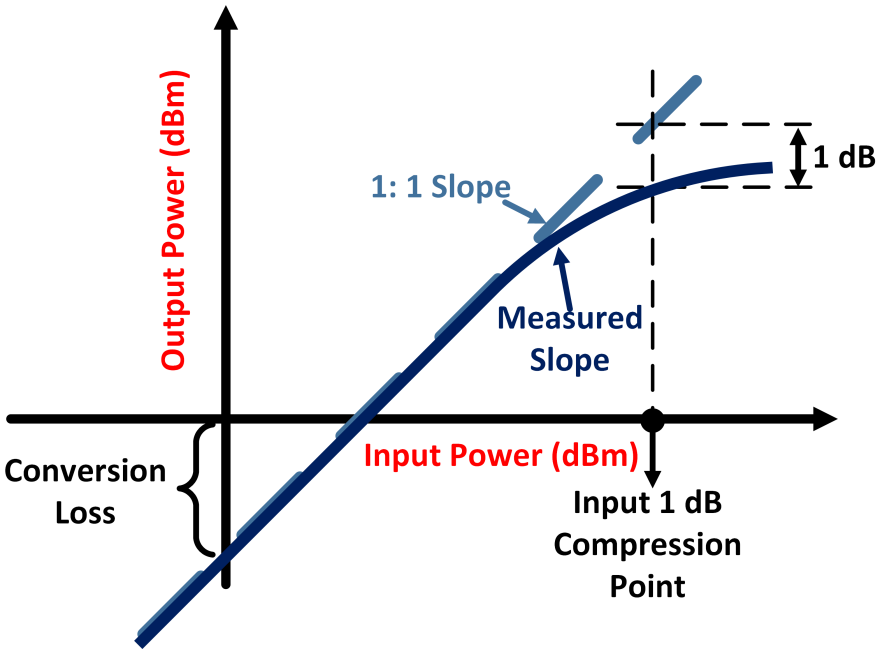


Figure 2.2: Graphical representation of IP_{1dB} [1].

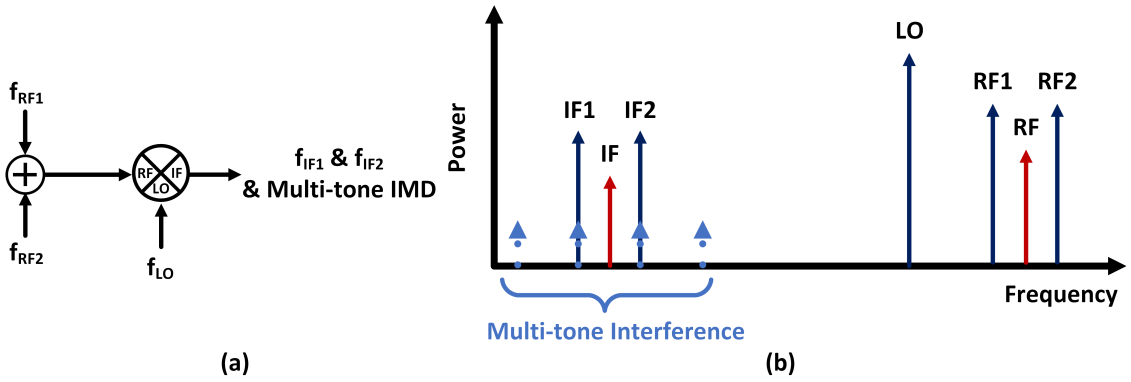


Figure 2.3: (a) Block diagram and (b) graphical representation of multi-tone IMD measurement.

on the system are shown in Fig. 2.3. Two close RF frequencies are applied to the mixer, RF1, and RF2. The inter-modulation of these two signals will distort the output power. Especially the third-order intermodulation products are close to and can interfere with the desired output signal. The third-order interference frequencies can be found in (2.1.5) and (2.1.6). Considering f_{RF1}, f_{RF2}, and f_{LO} as 27 GHz, 27.1 GHz, and 21 GHz respectively. The f_{IF1} and f_{IF2} will be present at 5.9 GHz and 6.2 GHz. These two frequencies are sufficiently close to f_{IF}, such that they can not be filtered out and the signal-to-noise ratio (SNR) will deprive.

$$f_{IF1} = 2f_{RF1} - f_{RF2} - f_{LO} \tag{2.1.5}$$

$$f_{IF2} = 2f_{RF2} - f_{RF1} - f_{LO} \tag{2.1.6}$$

The effect of the third-order intermodulation products is crucial since for each increase in the input the output is increased by three. This fast increase can deteriorate the performance when large interference signals are present, as shown in Fig. 2.4. The IIP_3 can be found at the intersection point of the extrapolated ideal line with the interference, which has a slope of 3. The IIP_3 is higher than the IP_{1dB} value by 9.6 dB, for a circuit in which only the third-order intermodulations are present.

The isolation describes the leakages from one port to another one. It is measured as the input power is provided to a port and the output power is measured at another one. The second input signal is not provided to be able to measure the leakages. Isolation is defined as the power difference between the input and output power. The LO-RF, LO-IF, and RF-IF isolation definitions are provided in Fig. 2.5 The RF-LO, IF-LO, and IF-RF isolation values are not measured since the mixer is a reciprocal device and they are approximately equal to the above-mentioned isola-

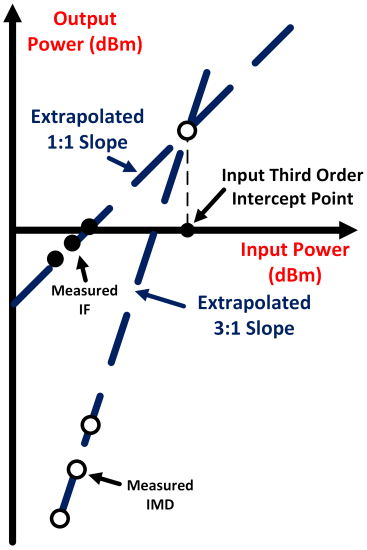


Figure 2.4: Graphical representation of IIP_3 [2].

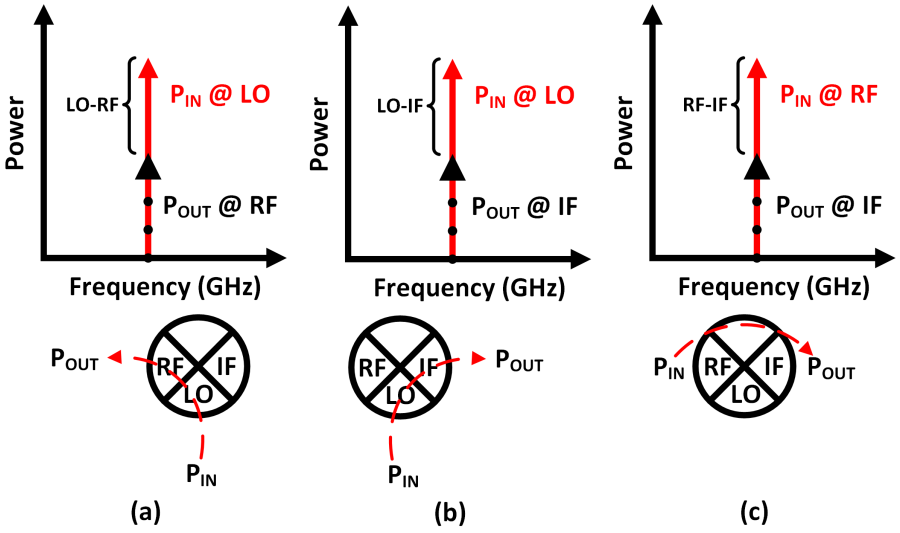


Figure 2.5: Definitions of mixer isolation for (a) LO-RF, (b) LO-IF, (c) RF-IF [3].

tions respectively. A lower LO-RF isolation value can cause interference distortion and deprive linearity. High LO-IF leakages can rise to fluctuate CG, in the case of close LO and IF frequencies. The LO leakages are dominant due its higher power levels compared to the RF and IF ones [3].

The noise factor is defined as the noise contributions from each device divided by the random input noise source. The noise figure (NF) is the noise factor in the dB scale and determines the lower level of the SNR, the minimum detectable signal. The NF of a conventional mixer is around 10-15 dB [1]. For the mixer architectures, single-sideband and double-sideband noise figures can be defined for the cases in which the RF and LO frequencies have a significant difference and IM frequency is

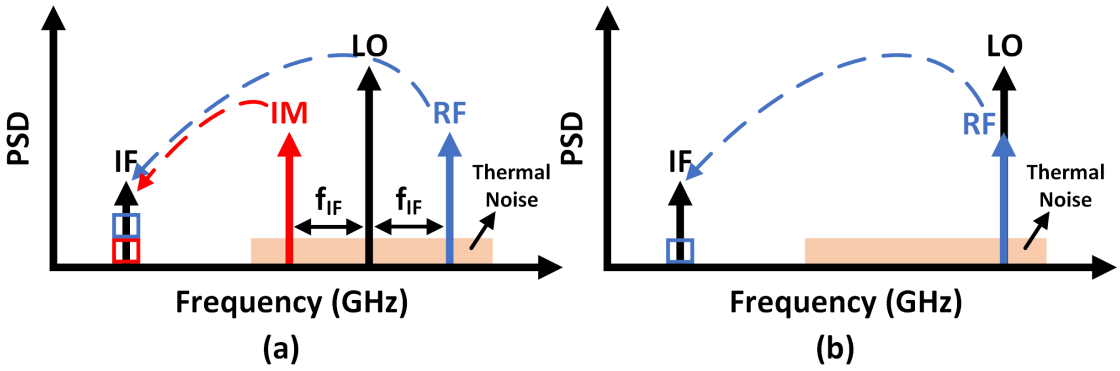


Figure 2.6: Graphical representation of (a) single-sideband (b) double-sideband noise figure.

observed; and the RF and LO frequencies are very close such that the IF is close to the baseband (0 Hz), as shown in Fig. 2.6. For SSB NF both the RF input and image signals (IM) contribute as the thermal noise such that it is twice as large as the DSB NF in which only the RF input signal contributes as the thermal noise. Ideally, the SSB NF is 3 dB higher than the DSB NF (0 dB), considering that the mixer circuit has no noise contributions [1]. SSB NF is used for the heterodyne receivers, and DSB NF is used for the homodyne/direct receivers.

2.1.2 Mixer in Receiver

Research in millimeter-wave frequency bands has been motivated in wireless communication. Due to the enlarged demand for higher transmit and receive data flow, increasing the bandwidth sets up higher data rates. The increased path loss in mm-wave frequencies was challenging for wireless communication systems. This problem was resolved through several sophisticated techniques such as beamforming. This technique utilizes directive antenna arrays. The main beamform combines the narrow beams produced by each antenna [23]. Low noise amplifier (LNA), phase shifter (PS), and down-conversion mixer are the sub-blocks of the conventional receiver architecture, as shown in Fig. 2.7. The mixer must operate appropriately with the high input power accumulated by each antenna, such that high linearity is required. The trade-off between linearity and noise figure (NF) in the mixer creates a requirement for enhancing the LNA gain to rectify the noise contributions of the mixer to the receiver. The CG must be kept large enough to suppress the noise contributions of the following stages. However, CG and linearity are inversely proportional; increasing CG to suppress noise will deprive the linearity. The receiver architecture must consider the trade-off between CG, linearity, and noise. This design is focused on 5G applications with an RF frequency range of 24.25-27.25

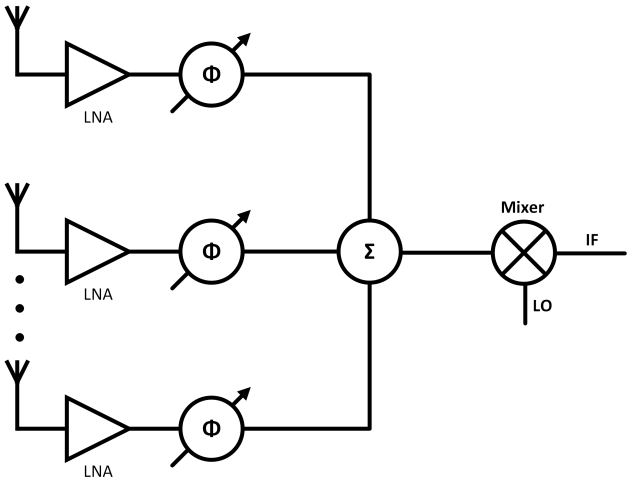


Figure 2.7: RF phase shifting phased receiver array configuration.

GHz, corresponding to the European 5G mm-waves band [24]. Subsequently, low power consumption, adequate CG, and high linearity are expected.

2.1.3 Mixer Architectures

Mixers can be categorized into unbalanced, single-balanced, and double-balanced ones as shown in Fig. 2.8 - 2.9 respectively. Their port configuration variation mainly exhibits a difference in their isolation performance. RF, LO, and IF ports are fed as differential signals for the double-balanced case, as illustrated in Fig. 2.9. Therefore it enables higher isolation between all ports thanks to the cancellation of the signals compared to the other two topologies. The unbalanced topology, where all signals are fed as single-ended, exhibits the highest leakages. Higher isolation implies that the leakages from one port to another are more suppressed. However, due to the more complex design, the NF will worsen. Linearity exhibits a trade-off between CG and voltage headroom. The transconductance stage of the multi-tanh topology contains 3 differential pairs to increase linearity, as shown in Fig. 2.10. To improve linearity, the noise is deprived compared to the previously mentioned topologies [4]. Another well known single-ended input topology is the micromixer which employs a class-AB at the transconductance stage to improve linearity, as shown in Fig. 2.11. However, determining factor of linearity is the IF stage, allowable IF swing is limited, and the RF to IF leakages are similar to the one of the single-balanced mixer [5]. The performance comparison of the mixer topologies is provided in the Table 2.1. In the case of no amplification and no quiescent power consumption (passive mixer), the compression occurs for a more extensive input power than amplified IF signal and quiescent power consumed (active mixer). On the other hand, conversion gain must be sufficiently large to suppress IF filter losses [2].

Down-conversion mixers employing transformer or active baluns have been demonstrated in the literature. Work in [25] presents that RF and LO signals are fed through active baluns. Other configurations proposed are a micromixer [5], a single-balanced mixer [26], an unbalanced mixer [27], and a double-balanced mixer, whose differential signals are fed through Marchand and transformer baluns [28], [29], and [30]. Configurable bond wire resonators were implemented as RF balun in the [31]. These different topology implementations lead to the idea to combine the active balun and transconductance stage into one stage and function as an entity, as shown in Fig. 2.12. This work focuses on a double-balanced Gilbert cell downconverter-mixer fabricated in IHP's 130 nm SiGe BiCMOS technology for 5G applications. The RF signal is provided as a single-ended signal by AC grounding one of the RF differential ports. The transconductance stage also operates as an active balun. Moreover, the power supply is fed through the IF balun, which minimizes the voltage drop and enhances linearity. The chip is packaged to the PCB through the flip-chip technique [32].

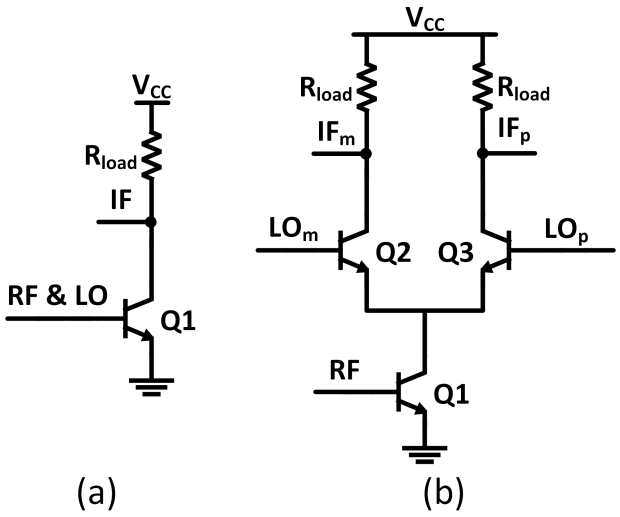


Figure 2.8: Schematic view of (a) unbalanced and (b) single balanced mixer topology.

Table 2.1: Performance comparison of different mixer topologies.

Parameter	Unbalanced	Balanced			Micromixer	Proposed
		Single	Double	Multi-tanh		
Isolation	None	RF or LO	RF and LO		RF or LO	RF and LO
Broadband	No	Yes				
Lo level	Lowest	Lower	Higher	Highest	Higher	
Linearity	Worst	Worse	Better	Best		Better
Noise	Best	Better	Worse	Worst	Worse	
Spurs	Worst	Worse	Better	Best	Worse	
LO suppress	No	Yes				
Cost	Lowest	Lower	Higher	Highest	Lower	Higher
Complexity	Lowest	Lower	Higher	Highest	Lower	Higher

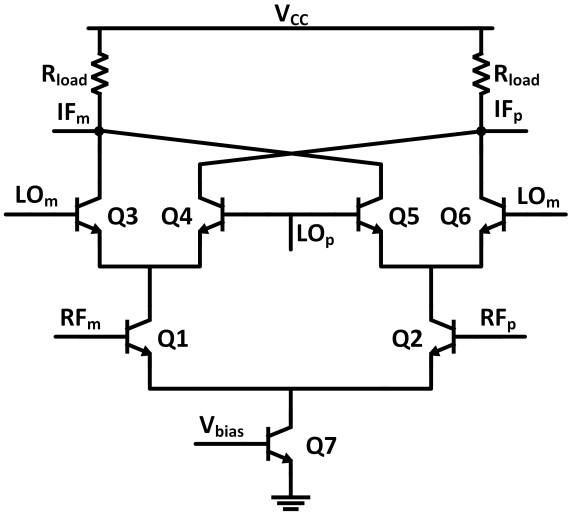


Figure 2.9: Schematic view of double balanced mixer topology.

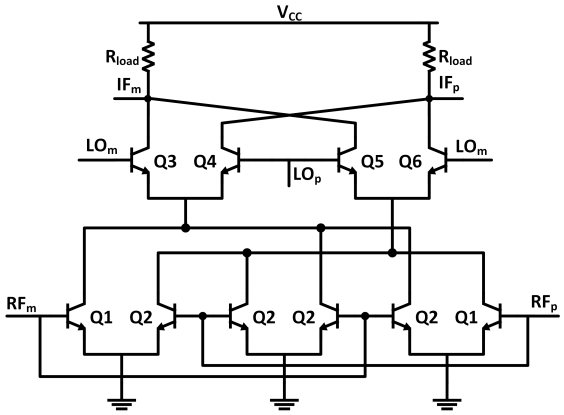
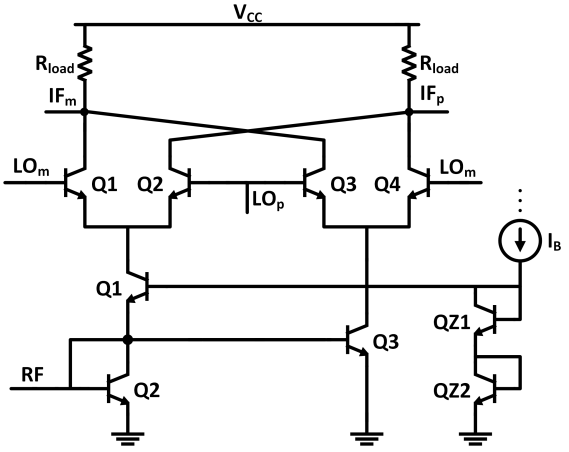


Figure 2.10: Schematic view of multi-tanh mixer topology. [4]



(a)

Figure 2.11: Schematic view of micromixer topology. [5]

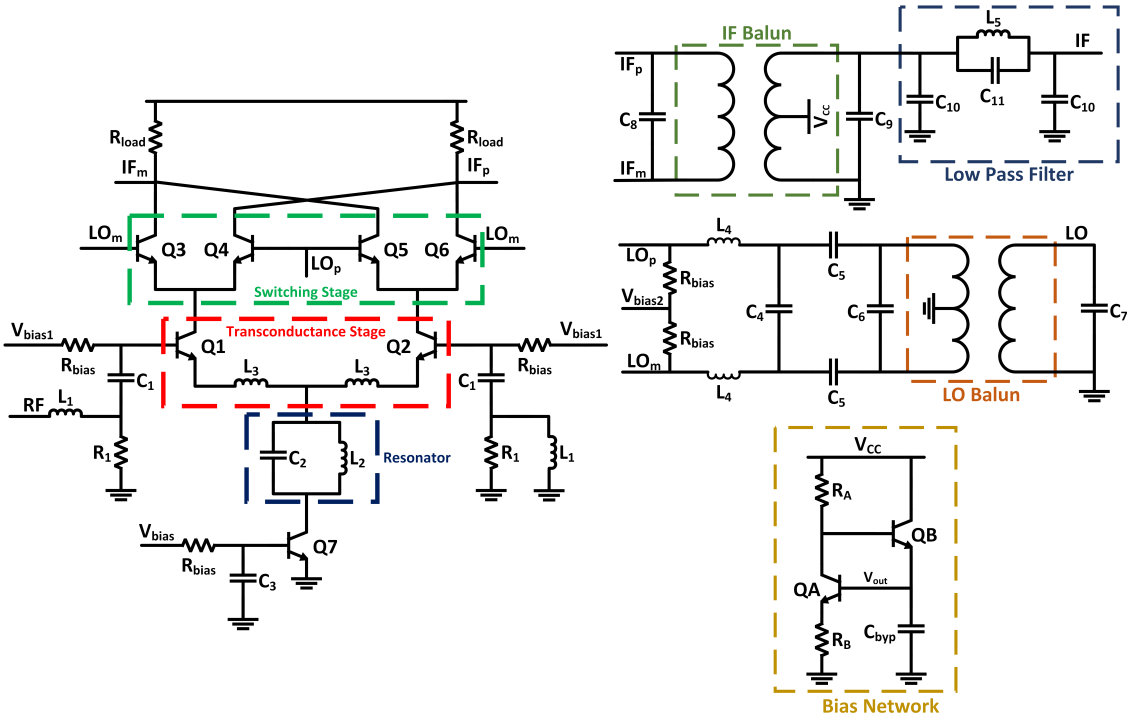


Figure 2.12: Schematic view of the proposed down-conversion mixer.

Table 2.2: Values of components employed in proposed mixer.

Q1-Q2	2x8	$\mathbf{R_1}$	100 Ω	$\mathbf{L_4}$	80 pH	$\mathbf{C_8}$	450 fF
Q3-Q4	6x8	$\mathbf{L_1}$	150 pH	$\mathbf{C_4}$	180 fF	$\mathbf{C_9}$	400 fF
Q7	8x8	$\mathbf{C_1}$	2 pF	$\mathbf{C_5}$	1 pF	$\mathbf{L_5}$	1.5 nH
$\mathbf{L_2}$	400 pH	$\mathbf{C_3}$	1 pF	$\mathbf{C_6}$	155 fF	$\mathbf{C_{10}}$	50 fF
$\mathbf{C_2}$	100 fF	$\mathbf{R_{bias}}$	2 kΩ	$\mathbf{C_7}$	90 fF	$\mathbf{C_{11}}$	100 fF
						$\mathbf{R_{load}}$	200 Ω

Table 2.3: Values of components employed in bias networks.

$\mathbf{V_{out}}$	$\mathbf{V_{bias}}$	$\mathbf{V_{bias1}}$	$\mathbf{V_{bias2}}$
	0.92 V	**1.15 V**	**2.3 V**
QA	1x2	1x2	1x2
QB	1x2	1x2	1x2
$\mathbf{R_A}$	17 kΩ	7.5 kΩ	3 kΩ
$\mathbf{R_B}$	1.5 kΩ	2 kΩ	12 kΩ
$\mathbf{C_{bypass}}$	1 pF	1 pF	1 pF

2.2 Circuit Description and Implementation

The proposed Gilbert cell mixer is depicted in Fig. 2.12. The RF input signal is introduced as a single-ended signal by AC grounding Q2, indicating that the RF leakages will be higher than a fully differential circuit. The differential RF input requires a single-ended to differential transformation; an active or a transformer balun could be employed. The former would increase the power consumption and NF and aggravate linearity. The latter would increase the chip area, deprive NF and attenuate the input signal. The trade-off between the balun topologies motivates to examine different ways of implementation. The active balun is implemented through a differential pair of transistors, as done in the transconductance stage. Combining these two stages will lower the power consumption compared to using a separate active balun. Moreover, this configuration will minimize chip area compared to the case of transformer balun implementation. The proposed Gilbert cell mixer will be more distinguishable for the up-conversion mixer design. Due to the IF transformer balun's low-frequency range, the double-balanced up-conversion mixer will occupy a considerable part of the chip area.

The straightforward design leads to RF isolation lower than 20 dB. Linearity can be deprived due to the large signal fluctuations of the RF-LO feed-through [2]. The behavior of interconnection between transconductance and switching stage was scrutinized due to leakages. Low isolation was caused by the current leakage of Q7, which ideally must provide constant DC current and RF open to the circuit. An LC resonator is added to the intermediate node, which acts as a band-stop filter for the RF signal. This circuit implementation is employed for a vector modulator phase shifter to enhance RF isolation [33]. The signal flows from the emitter of Q1 to the one of Q2 but does not leak through the Q7 transistor. The input matching circuit is also employed in the AC grounded port to preserve symmetry in the transconductance stage. The L_1 and R_1 are used for matching purposes, while the C_1 is a DC blocking capacitor.

2.2.1 Modified Circuit Analysis

Isolation Derivations

The small-signal model of the proposed Gilbert cell mixer, as shown in Fig. 2.13, demonstrates the operation of the transconductance stage as an amplifier and an active balun. The small-signal model and analysis are important for our design and objectives since the isolation values are mainly determined through the leakages

of the capacitances, whose effects are scrutinized in this analysis. The V_x, V_y, V_z, and (V_{out+}-V_{out-}) have been derived from the small-signal model. The matching circuits have been disregarded for simplicity, and the resonator at V_x since does not affect the node analysis for the RF frequency range. The RF and LO leakages to the output are being scrutinized in (2.2.1).

$$V_{out+} - V_{out-} = -\frac{1}{j\omega(C_{\mu 3} + C_{\mu 5}) + \frac{1}{R_L}}\big[V_{LO+}(gm_3 - j\omega C_{\mu 3}) + V_{LO-}(gm_5 - j\omega C_{\mu 5}) - V_y gm_3 - V_z gm_5\big] + \frac{1}{j\omega(C_{\mu 4} + C_{\mu 6}) + \frac{1}{R_L}}\big[V_{LO+}(gm_6 - j\omega C_{\mu 6}) + V_{LO-}(gm_4 - j\omega C_{\mu 4}) - V_y gm_4 - V_z gm_6\big] \quad (2.2.1)$$

In (2.2.1), the following considerations are taken $gm_3 = gm_6$, $gm_4 = gm_5$, $C_{\mu 3} = C_{\mu 6}$, and $C_{\mu 4} = C_{\mu 5}$ due to symmetry such that (2.2.2) has resulted. The differential LO signals will cancel each other since $C_{\mu 3} = C_{\mu 4}$. Complete symmetry of the switching quad is not considered straightway to show that the RF leakages will be diminished for the symmetric transconductance stage, even though the input signal is fed as single-ended, and differential output as long as the resonator is an RF open for the frequency band. Since V_y, V_z contains the RF leakages and would have canceled directly due to the symmetric switching stage.

$$V_{out+} - V_{out-} = -\frac{1}{j\omega(C_{\mu 3} + C_{\mu 4}) + \frac{1}{R_L}}\big[-2j\omega C_{\mu 3} V_{LO+} - 2j\omega C_{\mu 4} V_{LO-} - V_y(gm_4 - gm_3) - V_z(gm_3 - gm_4)\big] \quad (2.2.2)$$

Equation (2.2.3) is derived by substituting V_x, V_y, and V_z to (2.2.2). Moreover, the following equalities are considered, $gm_1 = gm_2$, $Y_1 = Y_2$, and $C_{\mu 1} = C_{\mu 2}$ due to the symmetry of the Q1 and Q2 transistors, in V_x, V_y, and V_z. It is observed that the V_x is simplified to V_{RF} / 2 due to the resonator, RF open, and symmetry of transconductance stage. The admittance seen by each transistor is given in (2.2.4)

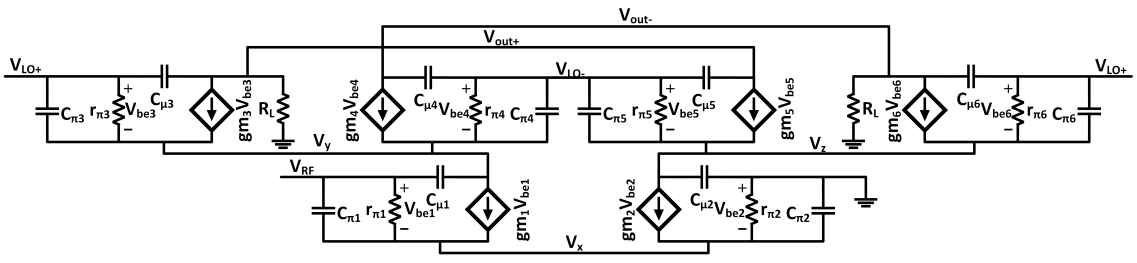


Figure 2.13: The small-signal model of the mixer.

for coherent equation derivations.

$$V_{out+} - V_{out-} = \left[\frac{gm_4 - gm_3}{C_{\mu 3} + C_{\mu 4} + \frac{1}{R_L}} \frac{1}{Y_3 + Y_4 + C_{\mu 1}}\right] \big[2Y_3 V_{LO+} + 2Y_4 V_{LO-} - V_{RF} C_{\mu 1}\big] \quad (2.2.3)$$

$$Y_{1,\ldots,6} = gm_{1,\ldots,6} + j\omega C_{\pi 1,\ldots,6} + \frac{1}{r_{\pi 1,\ldots,6}} \quad (2.2.4)$$

In (2.2.5), the differential LO signals are canceled due to common admittance. The RF leakages with common multiplier gm_1 are canceled due to the symmetry of the transconductance stage. The leakages of RF signal multiplied with $C_{\mu 1}$ are observed due to single-ended feeding of RF signal, which will be diminished due to the differential switching stage, $gm_3 = gm_4$. Regardless the RF signal is applied single-ended, the admittance and transconductance of the Q1 and Q2 are not observed at the output. So the RF leakages are decreased for this symmetric circuit implemented. Furthermore, the RF leakages must be limited with the resonator such that the assumptions made for the derivations will be maintained. The performance of the resonator will be discussed in the circuit implementation section. The RF leakage is quantified to present the designed circuit that can provide similar performance with the conventional double-balanced mixer. As in the conventional circuit, the highest possible level of symmetry is the key to achieve good isolation performance in the proposed circuit.

$$V_{out+} - V_{out-} = \frac{gm_4 - gm_3}{C_{\mu 3} + C_{\mu 4} + \frac{1}{R_L}} \frac{1}{Y_3 + Y_4 + C_{\mu 1}} V_{RF} C_{\mu 1} \quad (2.2.5)$$

The leakages from LO to RF are derived from the small-signal model in Fig. 2.13. The capacitance between the base and collector of Q1 and Q2 is added to the model to indicate the LO leakages through that capacitance to the input. The V_{RF}, V_x and V_z were derived from the node analysis at V_y, V_x, and V_z.

$$V_{RF} = \big[V_{LO+} Y_3 + V_{LO-} Y_4 - V_y(Y_3 + Y_4) + V_x gm_1\big] \frac{1}{gm_1 - C_{\mu 1}} \quad (2.2.6)$$

Equation (2.2.7) results from substituting V_x and V_z into (2.2.6). V_z is assumed to be equal to the V_y, verified during schematic simulations.

$$V_{RF} = \left[V_{LO+}\left[Y_3 - Y_6\frac{Y_3+Y_4}{Y_5+Y_6+C_{\mu 2}}\right] + V_{LO-}\left[Y_4 - Y_5\frac{Y_3+Y_4}{Y_5+Y_6+C_{\mu 2}}\right] + V_{RF}\left[\frac{gm_1Y_1}{Y_1+Y_2} - \frac{gm_2Y_1}{Y_1+Y_2}\frac{Y_3+Y_4}{Y_5+Y_6+C_{\mu 2}}\right]\right]\frac{1}{gm_1 - C_{\mu 1}} \quad (2.2.7)$$

Fully symmetrically, transconductance and switching quad are considered in (2.2.7) to derive (2.2.8). In (2.2.8), the Y_3 value will dominate $C_{\mu 1}$ due to the transconductance of the switching stage. LO leakages will be diminished due to the symmetry of the LO signal and the devices at the switching quad. The symmetry of the layout and fabrication tolerances determines the isolation profoundly. The RF signal on the right end side of (2.2.8) will be nullified since the Y_3 value dominates $C_{\mu 1}$ such that $V_{RF}(gm_1\text{-}gm_1)$ only remains.

$$V_{RF} = \left[\left(V_{LO+} + V_{LO-}\right)\left[Y_3 - Y_3\frac{2Y_3}{2Y_3+C_{\mu 1}}\right] + V_{RF}\left[\frac{gm_1Y_1}{2Y_1} - \frac{gm_1Y_1}{2Y_1}\frac{2Y_3}{2Y_3+C_{\mu 1}}\right]\right]\frac{1}{gm_1 - C_{\mu 1}} \quad (2.2.8)$$

It can be concluded that as long as the resonator acts as an RF open for the frequency range and the transconductance stage is designed for highest possible symmetry. The V_x node will be equal to V_{RF} / 2, as in the double balanced mixer. This implies that the transconductance stage will properly convert the single ended RF input to a differential one. So, the isolation values will be comparable to the ones of the double balanced mixer instead of the single-balanced one.

CG Derivation

The CG has been derived by assuming the switching stage as an ideal square wave multiplied by the current generated at the transconductance stage. The IF frequency is obtained due to the multiplication of two cosine waves, as shown in (2.2.9). As done previously, V_z is assumed to be equal to the V_y in (2.2.9) to obtain (2.2.10).

$$V_{out+} - V_{out-} = \frac{2}{\pi}\left[\cos((\omega_{RF} - \omega_{LO})t)V_{RF}R_L\left(gm_1 - j\omega C_{\mu 1}\right)\right] + \frac{4}{\pi}\cos(\omega_{LO}t)R_LC_{\mu 1}(V_y - V_z) \quad (2.2.9)$$

$$\frac{V_{out+} - V_{out-}}{V_{RF}} = \frac{2}{\pi}(gm_1 - j\omega C_{\mu 1})R_L \quad (2.2.10)$$

The conversion gain/loss in (2.2.10) ideally is equal to the one of the conventional double-balanced Gilbert cell mixer, even though the RF is single-ended fed due to the symmetry of transconductance and input matching stage. The leakages from the base to the collector diminishes the gain slightly.

2.2.2 Linearity Optimizations

Another critical parameter is linearity; the input 1 dB compression point is used to indicate the linear region operation of the mixer. The IP_{1dB} determines the upper limit of the dynamic range, and it is limited due to the odd-order nonlinearity and voltage headroom.

Emitter degeneration is employed to enhance linearity by lowering odd-order nonlinearity. The comparison between the characteristics of the common emitter and the common emitter with emitter degeneration is presented in Table 2.4 [34], and the schematic views are in Fig. 2.14. It can be observed that the R_{in} of the CE with R_e has been increased and the A_v decreased by the same factor $(1+g_mR_e)$ compared to the conventional CE. The input signal range that the CE with the R_e will not cause nonlinear distortion has been increased. The emitter degeneration introduces an impedance that lowers the third-order intermodulation product for the mixer circuit. Thus, IP_{1dB} is improved due to an improvement in odd-order nonlinearity. Moreover, the impedance presented by the emitter degeneration modifies the input impedance such that the CG drops. Inductive degeneration is preferred due to lower

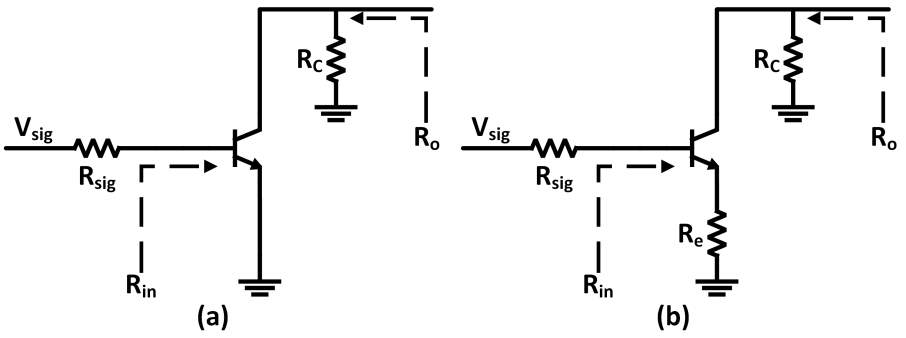


Figure 2.14: Schematic view of (a) the common emitter and (b) common emitter with R_e.

Table 2.4: Characteristics of CE BJT Amplifiers

	$\mathbf{R_{in}}$	$\mathbf{A_{vo}}$	$\mathbf{R_o}$	$\mathbf{A_v}$	$\mathbf{G_v}$
CE	$(\beta+1)r_e$	$-g_mR_c$	R_c	$-g_m(R_c \parallel R_L)$	$-\beta\frac{R_c\|R_L}{R_{sig}+(\beta+1)r_e}$
CE with $\mathbf{R_e}$	$(\beta+1)(r_e+R_e)$	$-\frac{g_mR_c}{1+g_mR_e}$	R_c	$\frac{-g_m(R_c\|R_L)}{1+g_mR_e}$	$-\beta\frac{R_c\|R_L}{R_{sig}+(\beta+1)(r_e+R_e)}$

noise contribution than resistive degeneration, and it is current efficient compared to resistive and capacitive degeneration [2]. For the A_v of the inductively degenerated circuit the R_e will be replaced with $j\omega L_3$ for the proposed mixer design.

For further improvements in linearity, voltage headroom is enhanced by feeding the DC supply voltage through the IF balun instead of the load resistors. The voltage drop at the output will depend on the ohmic losses of the balun, which are much smaller than the losses of the resistive load. An active or inductive load was not employed since it would increase the power consumption and deprive linearity of the mixer, or increase the area of the die respectively. The resistive load is employed since it occupies a very small amount of area, no additional power consumption is involved, and minimum sacrifice of linearity occurs. After the IF balun, the low pass filter is implemented to diminish the effects of the mixing spurs and the RF and LO leakage signals. The design and performance of IF balun and low pass filter will be disgusted in the following section.

2.2.3 Circuit Implementation

The first step is to determine the DC operating points for the core of the proposed circuit in Fig. 2.12. The transistors employed on transconductance and switching stage are the npn13p which have a unit emitter area of 0.0576 μm^2. In the transconductance stage, even though single-ended feeding is employed to maintain the symmetry of the circuit, the AC grounded Q2 is DC biased, and the matching circuit is used as one of the Q1. The transconductance stage mainly influences the linearity of the circuit. If the CG is kept very large, the linearity would be limited. It is biased such that it operates in class A. The base-emitter bias voltage is 0.92 V, collector-emitter voltage is 1.25 V, and device size is 2x8 to obtain the desired current across Q1, Q2 while the linearity is not limited. The transistor size of the transconductance stage is determined considering the trade-off between linearity and noise. Decreasing the transistor size would improve NF, while minimum sacrifice of linearity is observed, as shown in Fig. 2.15. The Q1-Q2 devices are the determining element for the NF as the LO signal can fully switch the Q3-Q6 devices [35]. Moreover, the base-emitter voltage is slightly higher than the one for minimum NF. The input matching consists of L_1 = 150 pH and R_1 = 100 Ω and DC blocking capacitor C_1 = 2 pF.

For the tail current transistor, Q7, the bias voltage, 920 mV is determined for optimal current while the NF is kept small. The collector-emitter voltage is set to 228 mV, such that it provides RF open and DC current to the transconductance

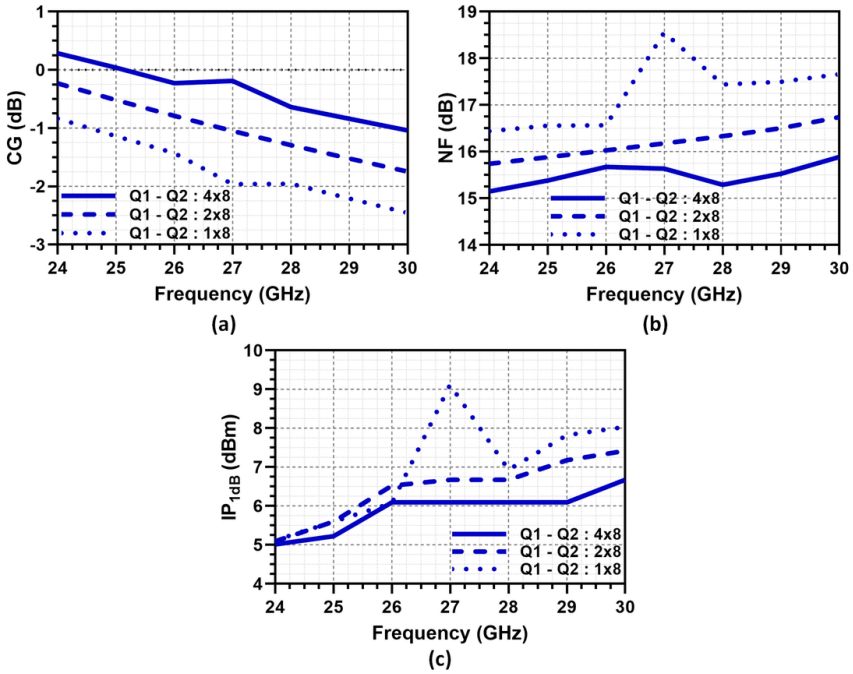


Figure 2.15: Simulated (a) CG, (b) NF and (c) IP_{1dB} for different transconductance stage transistor sizes.

stage. The optimal transistor size is 8x8, which determines the tail current that provides the determined conversion gain. The resonance frequency was 25 GHz, with L_2 = 400 pH and C_2 = 100 fF, as depicted in Fig. 2.16, S21 is higher than -10 dB for 23 - 27.5 GHz and -5 dB for 20 - 30 GHz. The insertion loss is lower than 2.5 dB for the 20 - 30 GHz range. The resonator occupies an area of 0.0173 mm^2, which is 1.7 times smaller than the area occupied by the LO balun, which would have a comparable size to the RF balun. A lower side of the RF frequency is resonating to balance the trade-off between linearity improvement and isolation reduction. As shown in Fig. 2.17 (a), the resonance frequencies of 20 GHz, 25 GHz, 30 GHz and 35 GHz exhibit bandwidths of 3.5 GHz, 4.5 GHz, 6 GHz, and 8.5 GHz, respectively. The insertion loss is below 2.5 dB for bandwidths respectively, as shown in Fig. 2.17 (b). These behaviors were obtained by modifying the resonator's capacitance value (150 fF, 100 fF, 70 fF, and 50 fF) and retaining the inductance of 400 pH. The resonance at 25 GHz is chosen, the capacitance value of C_2 is 100 fF for the optimal OP_{1dB} and LO-IF leakages; and minimum RF-IF leakages, as shown in Fig. 2.18 (a), Fig. 2.18 (b), and Fig. 2.19 (a). The LO-RF leakages exhibit discrepancies for 24 - 25 GHz range, as shown in Fig. 2.19 (b). Even though higher resonance frequencies exhibit larger bandwidths. The reactive current will be zero at the resonance frequency, open circuit for RF signal, suppressing signal loss through Q7. Furthermore, the RF isolations are improved even though RF input feeding is implemented as single-ended.

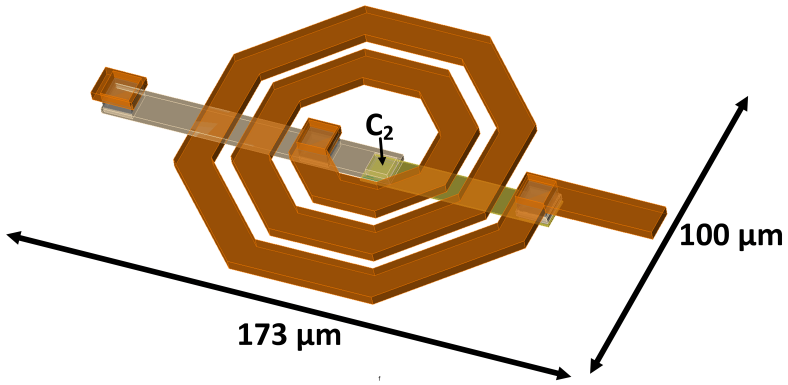


Figure 2.16: 3-D view of the resonator used for the modified Gilbert-cell mixer.

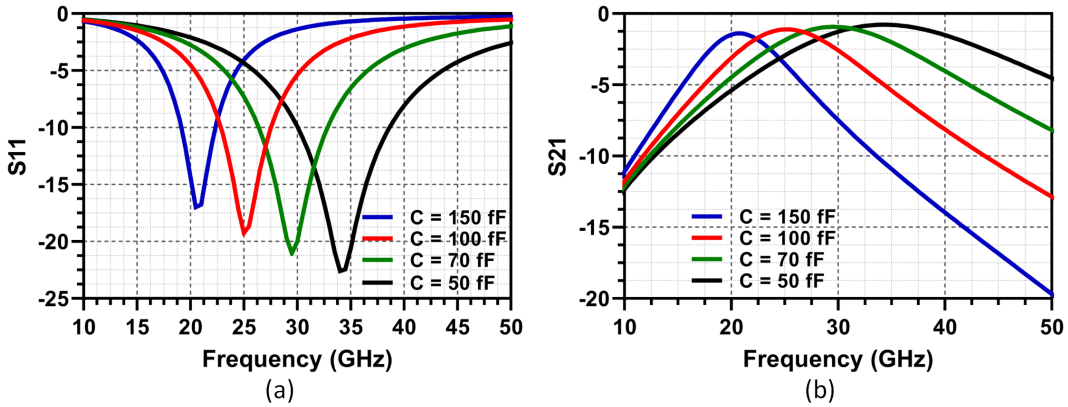


Figure 2.17: Simulated scattering parameters of the resonator; (a) S11, and (b) S21.

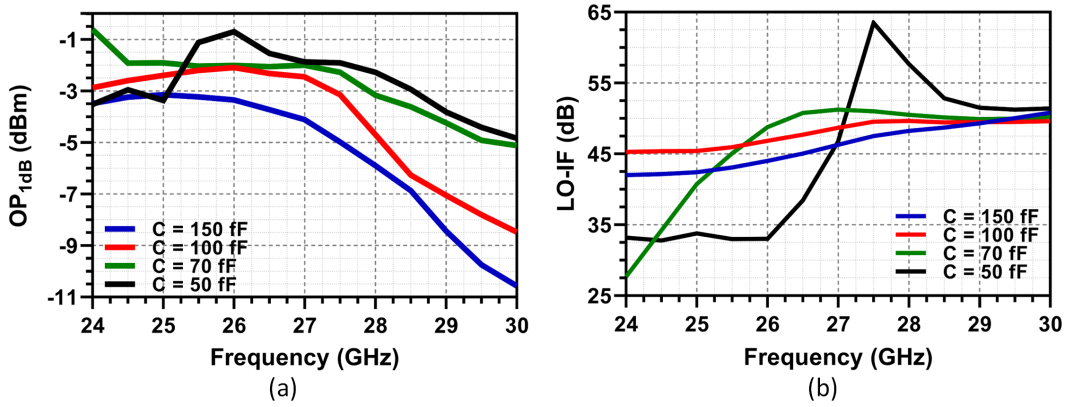


Figure 2.18: Simulated (a) OP_{1dB}, and (b) LO-IF for various resonator capacitance values.

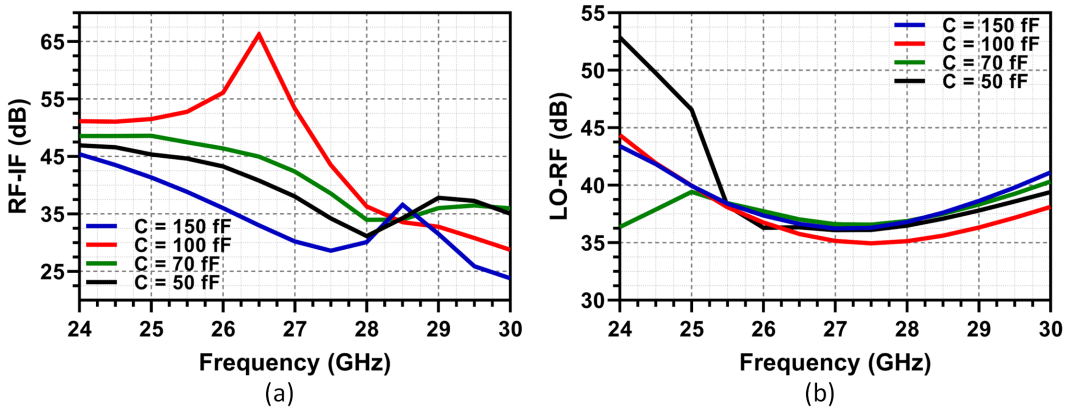


Figure 2.19: Simulated (a) RF-IF, and (b) LO-RF for various resonator capacitance values.

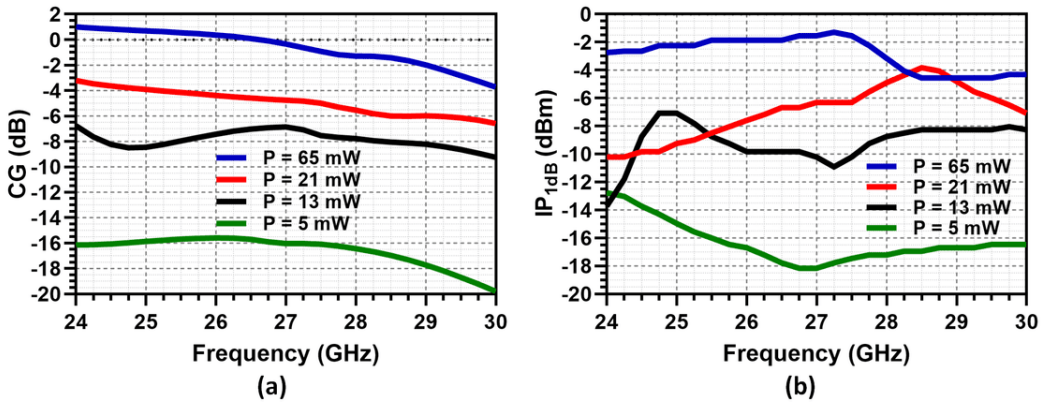


Figure 2.20: Simulated (a) CG and (b) IP_{1dB} of the EM simulated chip for different power consumptions.

The current drawn from the voltage supply is 19.6 mA and the power consumption is 65 mW. The current is determined for sufficient conversion gain, while the linearity is not limited. The power consumed is relatively high, however the CG and IP_{1dB} improve drastically. The transconductance stage is responsible for the trade-off between CG and IP_{1dB}. The higher current tail, provided through Q7, will improve linearity. To quantitatively present this expectation. The transistor size of Q7 is modified to 8, 4, and 1 which result to power consumption of 21 mW, 13 mW, and 5 mW, respectively. As the power consumed drops the CG and IP_{1dB} values are decreased, as shown in Fig. 2.20. The high power consumption was necessary for the design to obtain high CG and IP_{1dB} values.

The switching quad (Q3-Q6) size is determined as 6x8, such as large for NF enhancement, and the base bias voltage as 2.3 V to improve IP_{1dB} [2]. The rule of thumb for the size of the switching quad is to be in the same or half transconductance

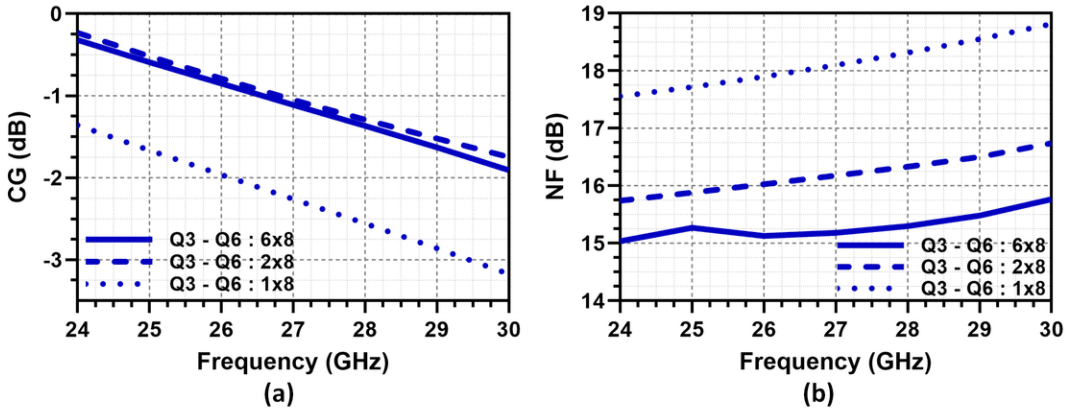


Figure 2.21: Simulated (a) CG and (b) NF for different switching quad transistor sizes.

stage transistor size. [35] However, for this design this was not applicable. Simulations in the schematic level were conducted for the same size (2x8) and half size (1x8) of the transcoductance stage transistors for the switching quad. The matching circuits were updated accordingly for each case. It is observed that the CG is not affected for the 2x8 sizing, while it is decreased for for the 1x8, as shown in Fig. 2.21(a). The NF is increasing for the decreasing switching quad transistor size, as shown in Fig. 2.21(b). The voltage supply is applied through the IF balun alternatively to the load resistors to limit the effects of the voltage headroom to linearity. The collector-emitter voltage is 1.8 V to allow a large signal swing at the output. The transformer balun is preferred due to its high linearity and no power consumption. It is based on the coupling between two overlaying metal layers (TopMetal2 and TopMetal1). The supply voltage is applied through the center tap for IF balun instead of grounding it in LO balun, as illustrated in Fig. 2.25. A shunt capacitor was implemented for matching purposes. The load resistor value is 200 Ω for CG and IF matching purposes. At the output port a shunt capacitor, which enhances isolations, is not employed due to area consuming matching circuitry. Placing a shunt capacitor would result in decrease in the gain as the frequency increases. A third-order elliptical low pass filter is added to the output to filter out the spurs, LO, and RF signals. The IF matching is completed both via balun and low pass filter. The low pass filter consists of L_5 = 1.5 nH and C_{10} = 100 fF. The LO differential signal fed to the base of the switching quad is matched to 50 Ω, through L4 = 80 pH and C_4 = 180 fF, while C_5 = 1 pF is a DC blocking capacitor. The component values employed in this design are summarized in Table 2.2.

The bias voltages applied to the bases of the current tail, transconductance, and switching devices are designed as on-chip bias networks for each value separately. The transistors employed on biasing networks are the npn13v2 which have a

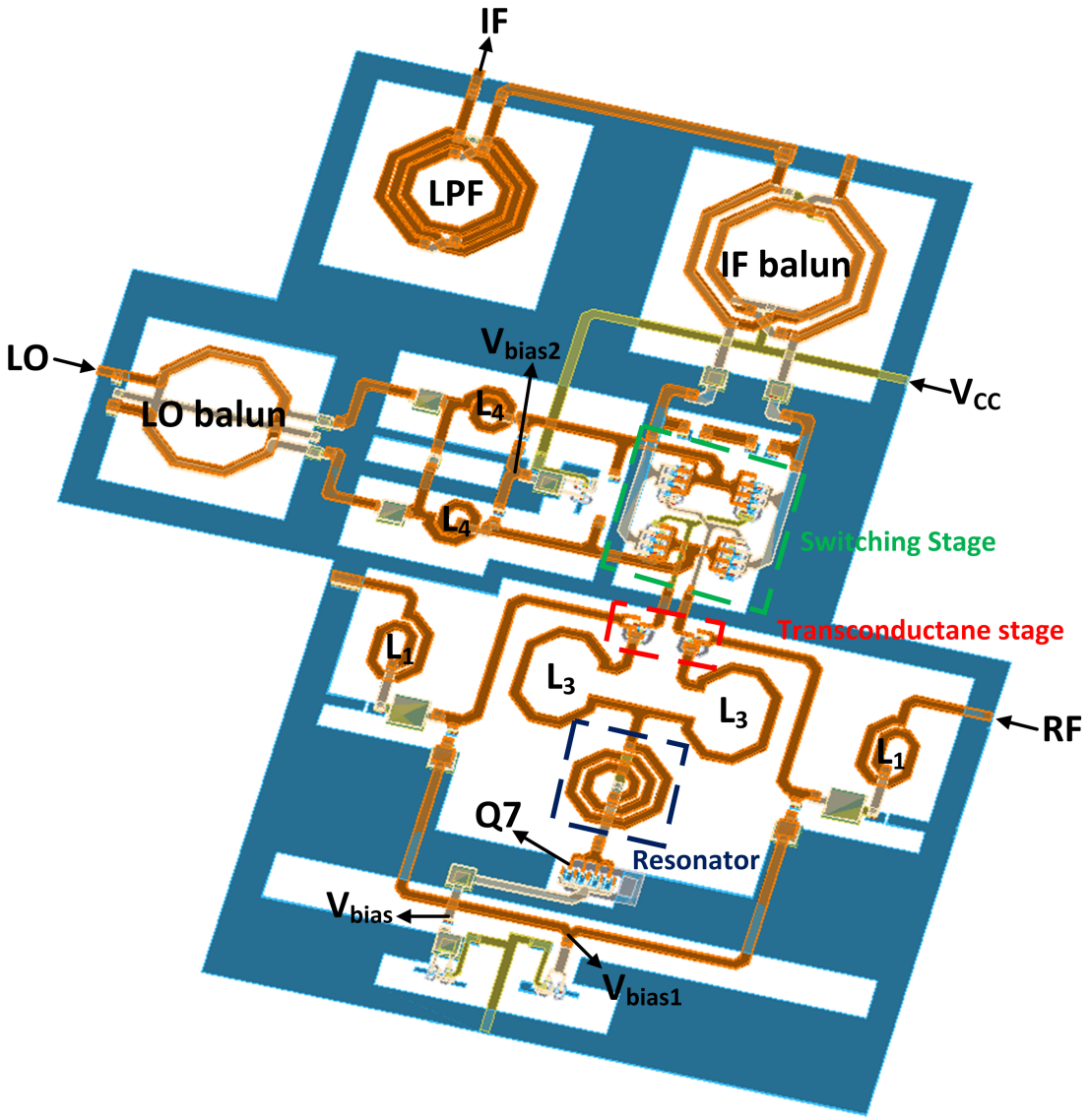


Figure 2.22: 3-D view of the proposed Gilbert-cell mixer.

unit emitter area of 0.12 μm^2. The component values employed for the bias networks are summarized in Table 2.3. To minimize the externally applied voltage sources, the only voltage supply provided is 3.3 V. The bias network of the transconductance stage is placed below Q7 in layout level to prevent asymmetry and deprive performance with the area expense. The bias voltages applied to the base are fed through a resistor, R_{bias} = 2 kΩ to avoid RF leakage to the biasing networks. All the inductors are designed using TopMetal2 due to low resistivity and distance from the ground to minimize parasitic effects. The complete simulated 3-D view of the proposed mixer is shown in Fig. 2.22

Balun Design

The conversion of the differential signal to single-ended for the LO and IF ports are conducted through transformer baluns. The passive transformer balun topology has been preferred since it enhances the linearity of the system and does not consume DC power. Compared to the active ones which can be utilized in smaller areas. The overlay geometry is employed since its performance is similar to the interleaved geometry. The area occupied will be slightly smaller since overlay geometry depends on the vertical coupling of the metal layers. Important parameters that define the performance of a transformer balun are amplitude and phase imbalance in comparison to the ideal amplitude and phase. The ideal amplitude value at the differential ports is -3 dB due to the power split of the single-ended port. The ideal phase difference at the differential ports is 180°. The common-mode rejection ratio (CMRR) combines the phase and amplitude balance performance into one value. The CMRR definition is given in (2.2.11). High CMRR values are necessary for high phase and amplitude balance [36].

$$CMRR(dB) = 20\log \mid \frac{S_{21} - S_{31}}{S_{21} + S_{31}} \mid \tag{2.2.11}$$

The LO transformer balun employs 1:1 turns, as shown in Fig. 2.23. The inductance, quality factor (Q), and resistance of primary and secondary inductors of LO balun are presented in Table 2.5. For LO and IF baluns the primary inductor is designed in the TopMetal2 layer and the secondary one in the TopMetal1 layer. These metal layers are preferred since they are at the highest level in the stack, and the parasitic capacitance to the ground is smaller compared to other metal layers. Moreover, their line resistance is the smallest, decreasing losses, and their current handling capacity is the highest compared to the other ones. The width of the inductors employed are 10 μm. The simulated phase difference and S21, and S31 amplitudes are shown in Fig. 2.24 (a). The phase imbalance ranges from 1.45° to 2.86°, and the average phase imbalance is 2.4°. The insertion loss is 1 - 2.2 dB, the maximum amplitude imbalance is 0.1 dB and the average RMS amplitude imbalance is 0.005 dB. The CMRR is above 32 dB for the whole frequency range, indicating a good balance, as shown in Fig.2.24 (b).

The IF transformer balun employs 2:2 turns, as shown in Fig. 2.25. The inductance, quality factor, and resistance of primary and secondary inductors of IF balun are presented in Table 2.5. The width of inductors and spacing between the turns are both 10 μm. The simulated phase difference and S21, and S31 amplitudes are shown in Fig. 2.26 (a). The phase imbalance is 3.7° and the insertion loss is 1.6 dB at 6 GHz. The average phase imbalance is 3.6°, the average RMS amplitude imbal-

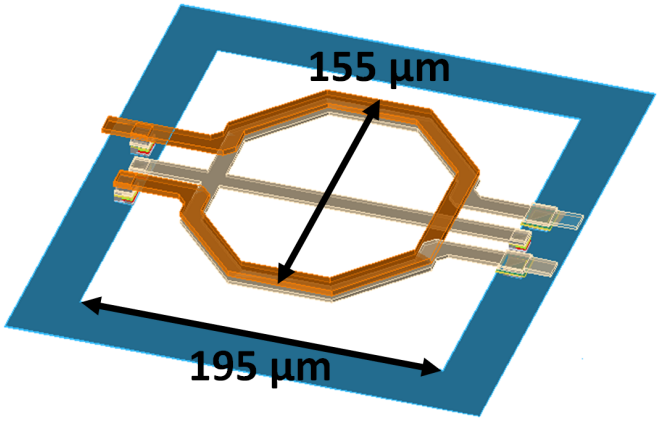


Figure 2.23: 3-D view of the LO balun used for the modified Gilbert-cell mixer.

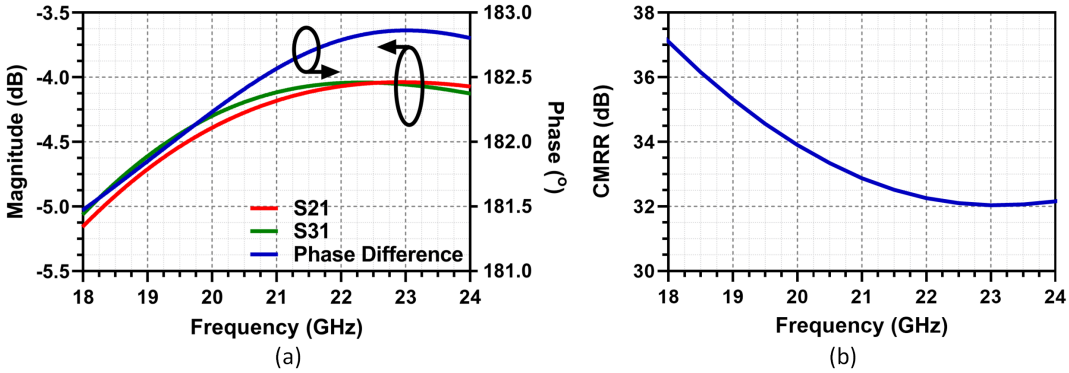


Figure 2.24: (a) Insertion loss and phase characteristics, and (b) CMRR of LO balun.

Table 2.5: Inductance, quality factor, and resistance of primary and secondary inductors employed for LO and IF baluns.

	LO balun		IF balun	
	18 GHz	**24 GHz**	**5 GHz**	**7 GHz**
$\mathbf{L_p}$ **(pH)**	298	309	915	931
$\mathbf{L_s}$ **(pH)**	313	330	951	972
$\mathbf{Q_p}$	18.55	19.6	12.7	15.2
$\mathbf{Q_s}$	16.1	17.4	8.2	10
$\mathbf{R_p}$ **(Ω)**	1.8	2.3	2.2	2.7
$\mathbf{R_s}$ **(Ω)**	2.2	2.8	3.6	4.2

ance is 0.02 dB and the maximum amplitude imbalance is 0.17 dB for the IF band is shown in Fig. 2.26 (a). The CMRR is above 25 dB for the whole frequency range, as shown in Fig.2.26 (b). It is observed that the phase and amplitude imbalance increases as the frequency increases, so the CMRR is decreasing respectively.

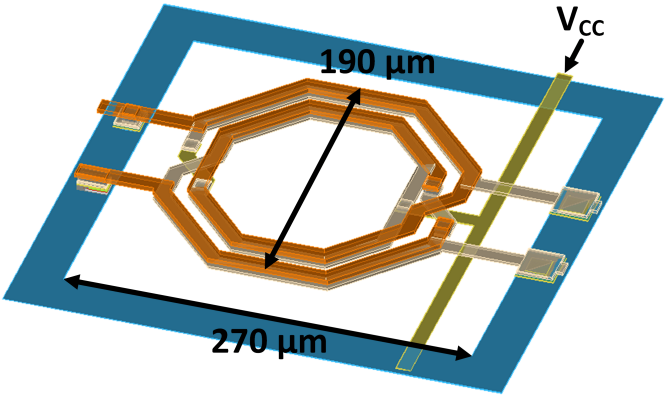


Figure 2.25: 3-D view of the IF balun used for the modified Gilbert-cell mixer.

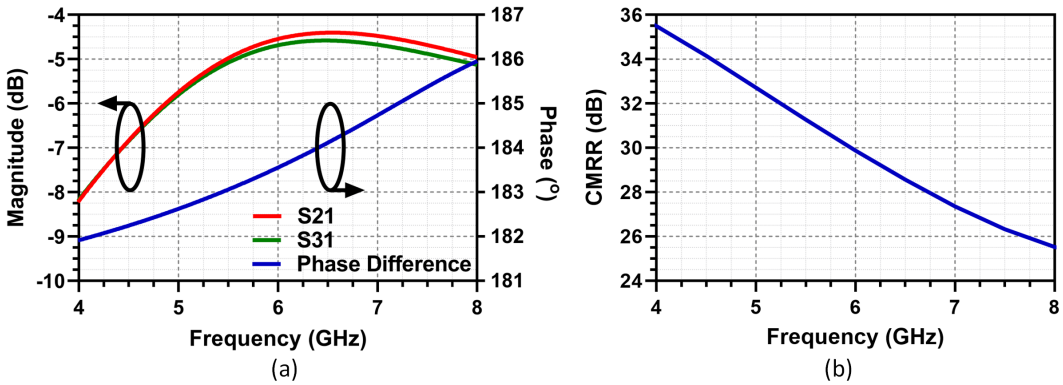


Figure 2.26: (a) Insertion loss and phase characteristics, and (b) CMRR of IF balun.

For both balun and low pass filter layout designs, the effect of eddy currents imposed by the dummy floating metals is observed when Metal1, ground, creates a closed loop around the design. The floating metals are not added to the inside and close distance of the balun layout to minimize additional losses.

Active Balun

The transconductance stage of the proposed down-conversıon mixer operates in the same way as the one of the conventional Gilbert Cell mixer and converts the single-ended input signal to a differential one. The appropriate operation is justified through the phase error and amplitude difference simulations of the full EM simulated chip with spacing between the transconductance and switching stage. The phase error is 2° - 8° and amplitude difference below 2 dB for 24 - 27.5 GHz, bandwidth of the the resonator. The imbalance contributed from the Q7, the current source, are suppresed by the resonator at the mm-wave frequencies.

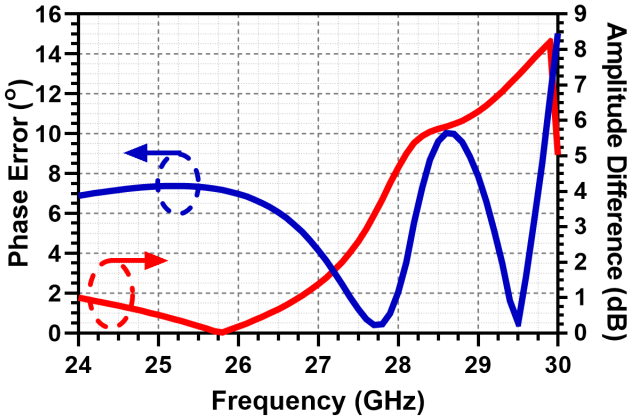


Figure 2.27: Phase error and amplitude difference of the active balun.

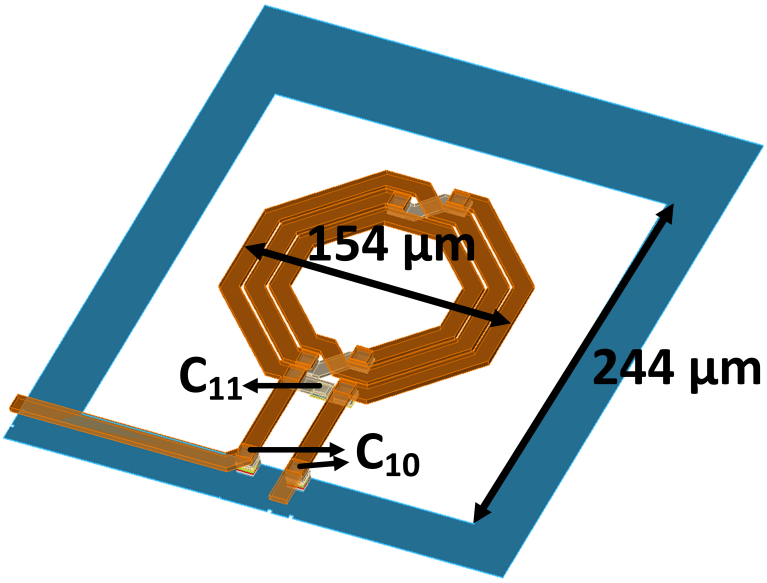


Figure 2.28: 3-D view of the low pass filter used for the modified Gilbert-cell mixer.

Low Pass Filter Design

The low pass filter shown in Fig. 2.28 is employed after the IF balun for matching purposes and to suppress RF and LO leakages at the output. The matching mismatches cause gain and linearity deprivation while the suppression of the higher frequencies improve. During the simulation the trade-off between these performance metrics were observed. Three different cases were scrutinized such as high CG performance (Matching improved), high suppression of RF frequencies (LPF improved), and the in-between these trade-off (Matching-LPF midpoint). It can be concluded as tha CG is increased through a improved matching circuit, the isolation values will reduce, as shown in Fig. 2.29 - 2.30. Considering this trade-off a design high isolation values, while the CG is minimally effect can be achieved.

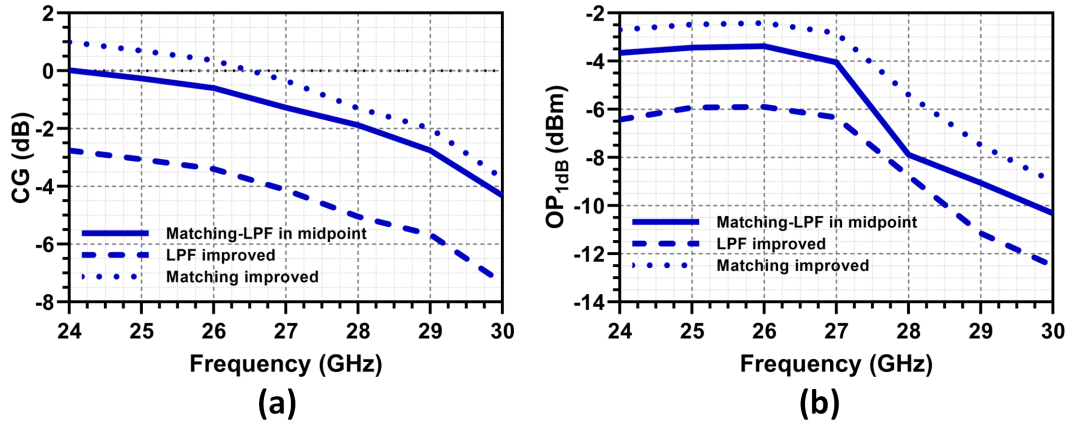


Figure 2.29: Simulated (a) CG and (b) OP_{1dB} for different IF matching and LPF configurations.

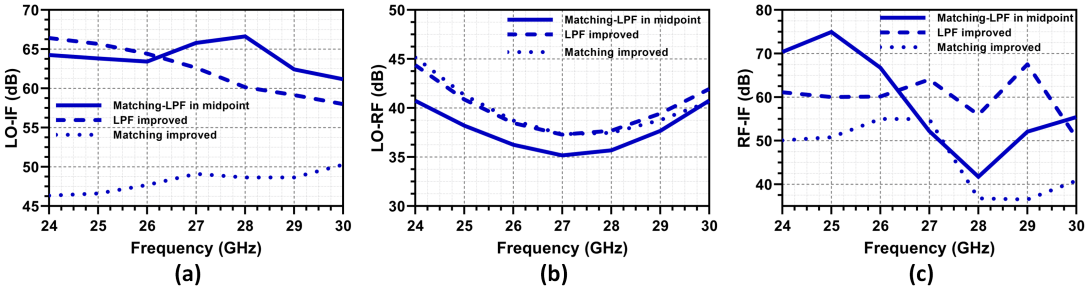


Figure 2.30: Simulated (a) LO-IF, (b) LO-RF, and (b) RF-IF isolations for different IF matching and LPF configurations.

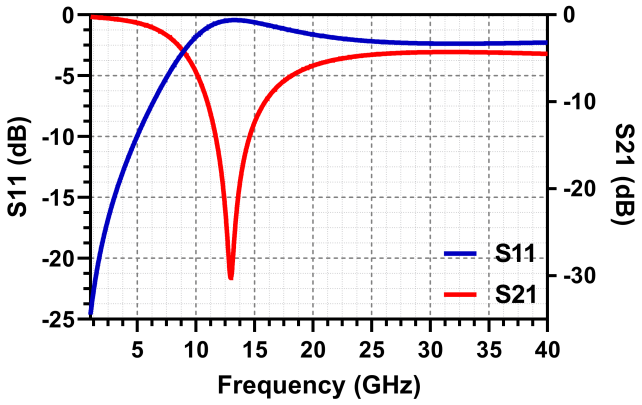


Figure 2.31: Scattering parameters of low pass filter.

The matching mismatches were minimized while the isolations were not deprived significantly. The component values are given in Table 2.2. In Fig. 2.31, the return loss and and forward transmission coefficients are presented. It is observed that the S21 parameter does not fully suppress the RF frequencies, so RF-IF isolation has decreased.

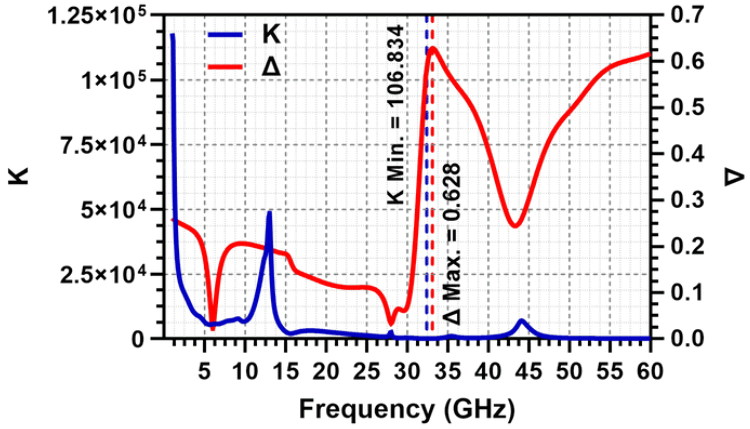


Figure 2.32: EM simulated chip K and Δ .

Stability

The stability of the mixer can be simulated when the LO port is grounded, such that the mixer becomes a two-port device [37]. The Rollet stability factor (K) and Δ are given in (2.2.12) - (2.2.13) [38]. The simulated K is larger than 1 and Δ is smaller than 1, since these two criteria are true unconditional stability is valid. The minimum K value is 106.834 at 32.4 GHz and maximum Δ value is 0.628 at 33.1 GHz, as shown in Fig. 2.32.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{2.2.12}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{2.2.13}$$

Resonator Effects Analysis

Finally, the consideration mentioned above is inspected to improve port-to-port isolation while the other specifications are not declined. The resonator is being removed from the chip layout, and the collector of Q7 is directly connected to the emitter degeneration inductors (L_3), as shown in Fig. 2.33. The EM simulation results of this version of the chip is provided below. The RF-IF isolation of the EM simulated chip without the resonator drops drastically compared to the EM simulated chip with the resonator. The LO-RF and LO-IF isolations are not affected drastically, as shown in Fig. 2.34 (a). The OP_{1dB} has been depleted, which is caused due to leakages and impedance matching mismatch caused due to the L_2 removal which affects matching substantially, as shown in Fig. 2.34 (b).

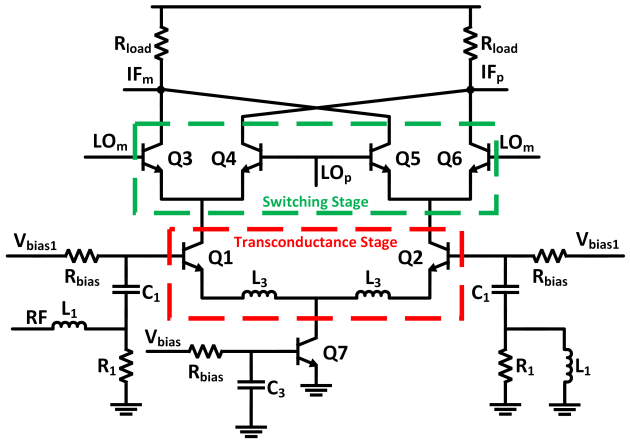


Figure 2.33: Schematic view of the chip without the resonator.

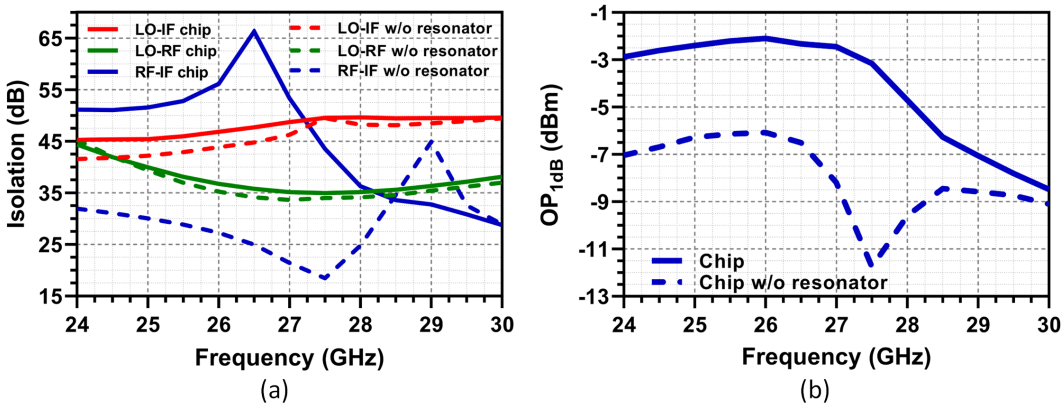


Figure 2.34: Simulated (a) isolations, and (b) OP_{1dB} of the chip with and without resonator.

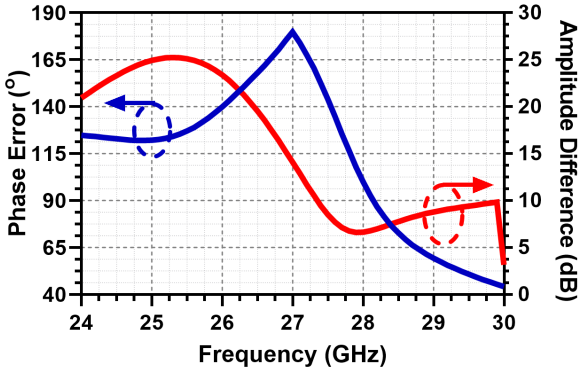


Figure 2.35: Full chip EM simulation of the phase error and amplitude difference of the active balun without resonator.

Furthermore, the phase error and amplitude difference of the chip without resonator are presented in Fig. 2.35. The phase error and amplitude difference are high which justifies the isolation decline. This shows that the V_x is not equal to half of V_{RF} and that the single ended input is not properly converted to a differential one.

Following, to prove that the RF-IF isolation will worsen even if the RF matching is improved, such that the OP_{1dB} will increase. The case in which the resonator capacitance is only removed from the EM simulated chip.

The capacitor C_2 has only been removed from the chip layout to reduce impedance mismatches since the L_2 inductor affects the RF matching, as shown in Fig. 2.36. The EM simulated chip with and without the C_2 show a similar trend and values of OP_{1dB}, as shown in Fig. 2.37 (a). RF-IF and LO-IF isolations have dropped, as shown in Fig. 2.37 (b), even though the input matching is improved. The phase error and amplitude difference have decreased compared to the without resonator case, as shown in Fig. 2.38. However, these values are higher compared to the simulations with resonator, as shown in Fig. 2.27. These simulations prove that the resonator is a necessary block for enhancing the port-to-port isolations, while the linearity is not affected significantly.

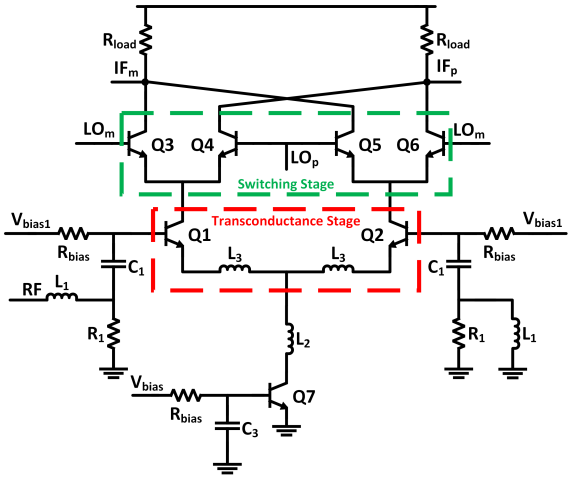


Figure 2.36: Schematic view of the chip without resonator capacitance.

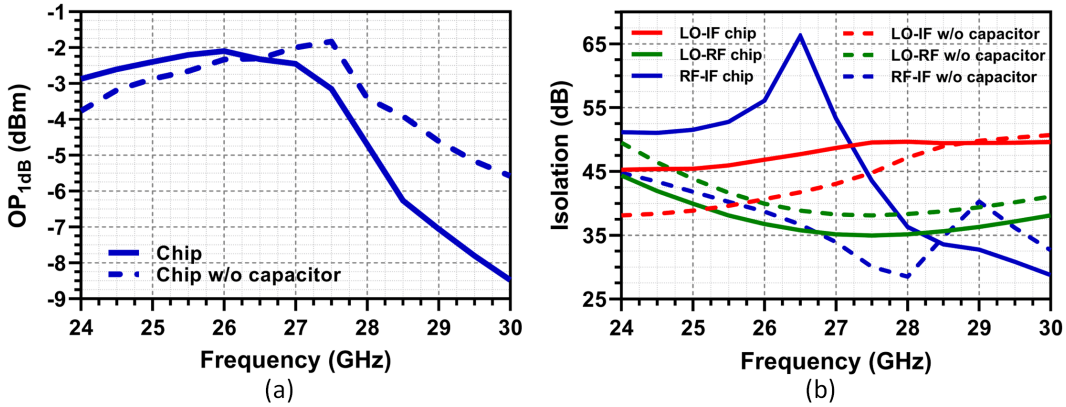


Figure 2.37: Simulated (a) OP_{1dB}, and (b) isolations of the chip with and without resonator capacitance.

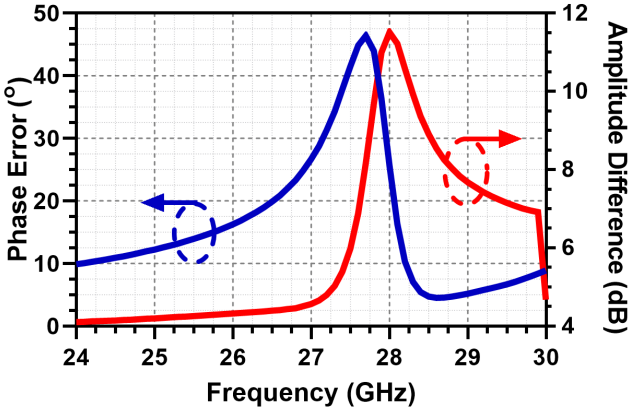


Figure 2.38: Full chip EM simulation of the phase error and amplitude difference of the active balun without resonator.

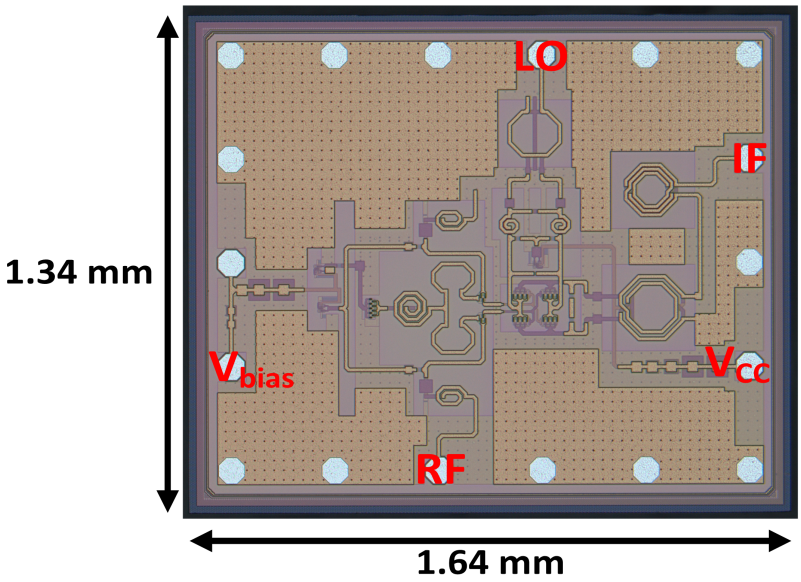


Figure 2.39: The die photograph of the mixer.

2.3 Measurement Results

The proposed design is fabricated in IHP's 130 nm SG13S2 SiGe BiCMOS technology. This technology offers HBTs with f_t/f_{max} of 250/340 GHz and BV_{CEO} of 1.8 V. The chip die is depicted in Fig. 2.39, the distance from the center of one pad to the center of the other pad is of 300 μm due to the flip chip package technique employed. The ground plane is spread through the stacked metals from pads to the middle of the chip. The full chip including pads is simulated in Momentum RF EM simulator, while the board is simulated in FEM EM simulator. The total area is 1 mm^2 for the core, inductor, and balun area and 2.2 mm^2 with the pads. The measurements of CG, IP_{1dB}, port-to-port isolations, and port return losses are

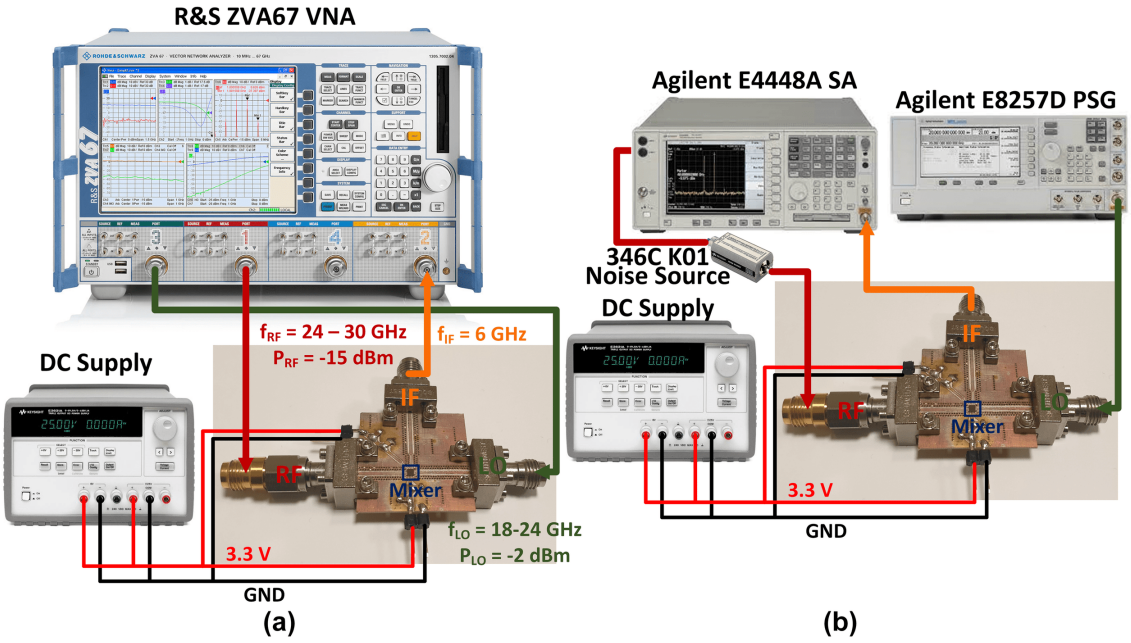


Figure 2.40: Measurement setup of the (a) VNA based and (b) NF for the mixer.

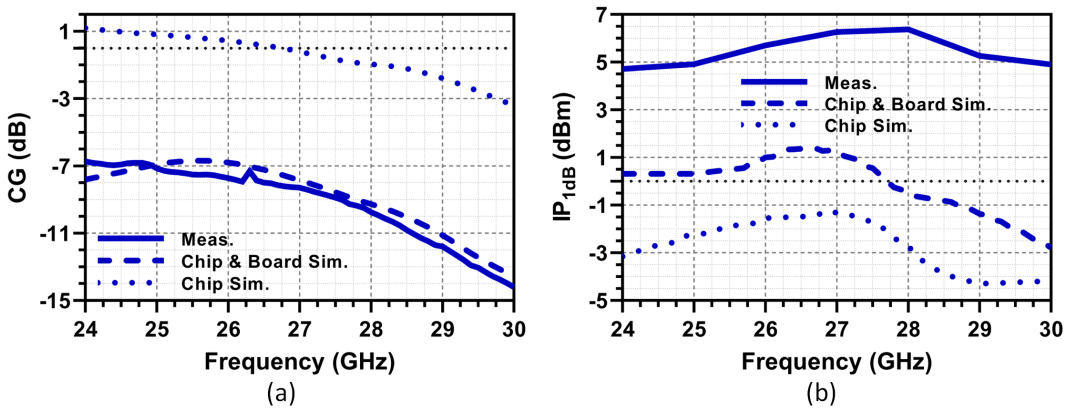


Figure 2.41: The measured, simulated chip & board, and simulated chip (a) CG, and (b) IP_{1dB} of the mixer.

conducted using Rohde & Schwarz ZVA67 VNA, as shown in Fig. 2.40(a) [39]. The SSB NF measurement at IF port is performed through Agilent E4448A SA along with Keysight 346CK01 as noise source at RF port and Agilent E8257D PSG as LO signal generator, as shown in Fig. 2.40(b) [40].

The conversion gain and IP_{1dB} versus frequency is shown in Fig. 2.41 (a); the IF frequency is 6 GHz, and the LO frequency is 18 - 24 GHz. The peak gain is 1.27 dB at 24 GHz and drops gradually from 1.27 dB to -3.4 dB for the EM simulated chip. The measured CG starts from -6.73 dB and drops to -14.19. The reduction in CG is caused due to PCB losses, which are justified through the simulation of chip

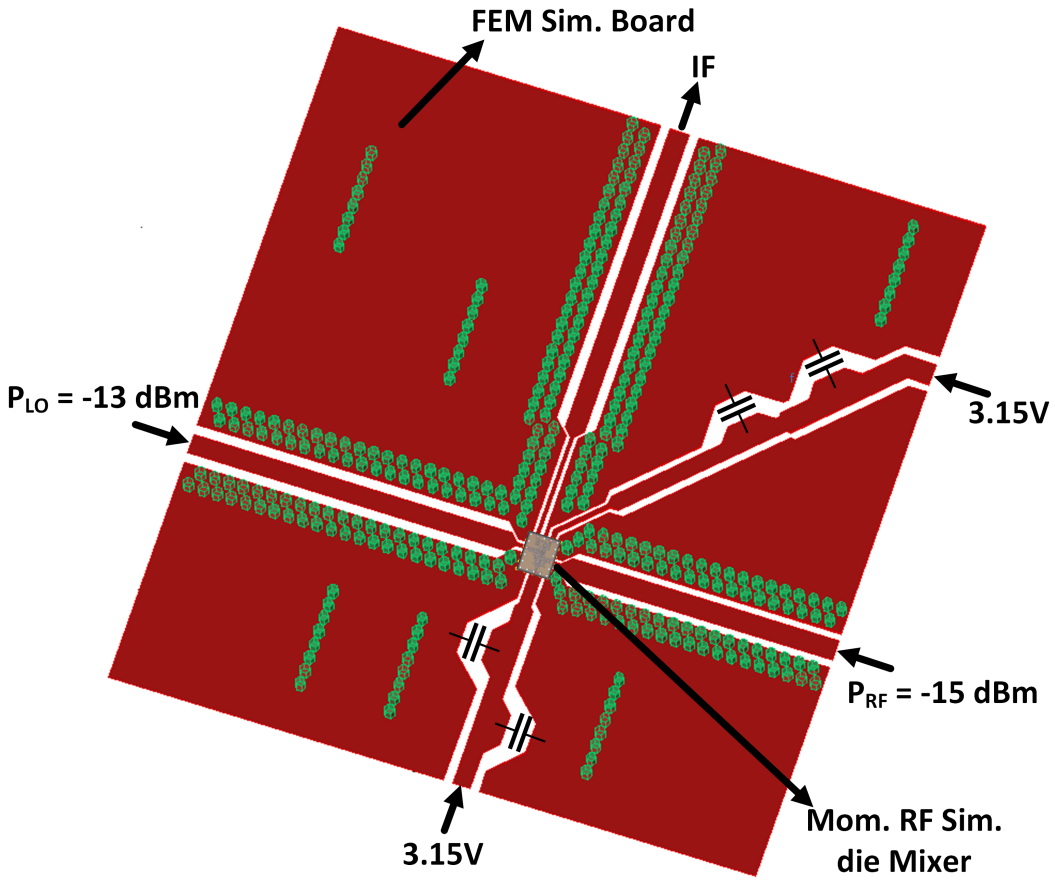


Figure 2.42: Simulation setup of the board and proposed mixer layout.

and board with a -13 dBm LO signal applied, and the bias and supply voltage are reduced to 3.15 V to match the current drawn during measurement, 17 mA. The simulation setup of the FEM simulated board and Momentum RF simulated mixer layout to match the measurement results is shown in Fig. 2.42. The measured IP_{1dB} varies from 4.71 - 6.38 dBm, and it is higher than the simulated cases, as shown in Fig. 2.41 (b). The losses on the RF board path could not be added to the simulation setup since RF power ideally does not affect the operation.

The output 1dB compression point has a flat response for 24-28 GHz and variation of 0.2 dB, and exhibits close values to the EM simulated chip. The flat response of the OP_{1dB} corresponds with the minimal phase error and amplitude difference of the active balun, as shown in Fig. 2.27. The OP_{1dB} is a determining factor for the linearity; this design is lower by 12.1 dB, 1.6 dB and 1 dB [31], [41], [28] respectively. All three works employ IF buffers that enhance CG, and apply higher LO powers and lower IF frequencies than our work. The lower OP_{1dB} is due to the input stage, which functions as an active balun and transconductance stage. This stage is forced to convert the single-end signal to a differential one and amplify it linearly. However, it has a higher value than single-balanced, double-balanced, and

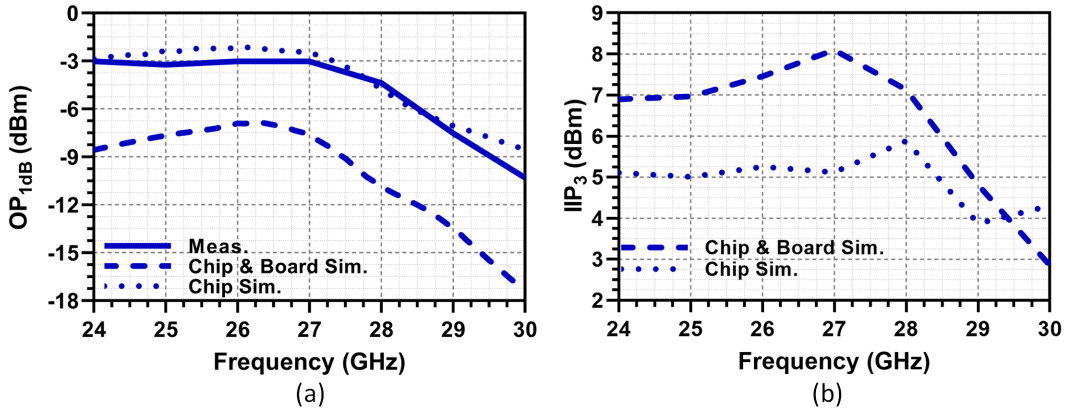


Figure 2.43: The measured, simulated chip & board, and simulated chip (a) OP_{1dB}, and (b) IIP_3 of the mixer.

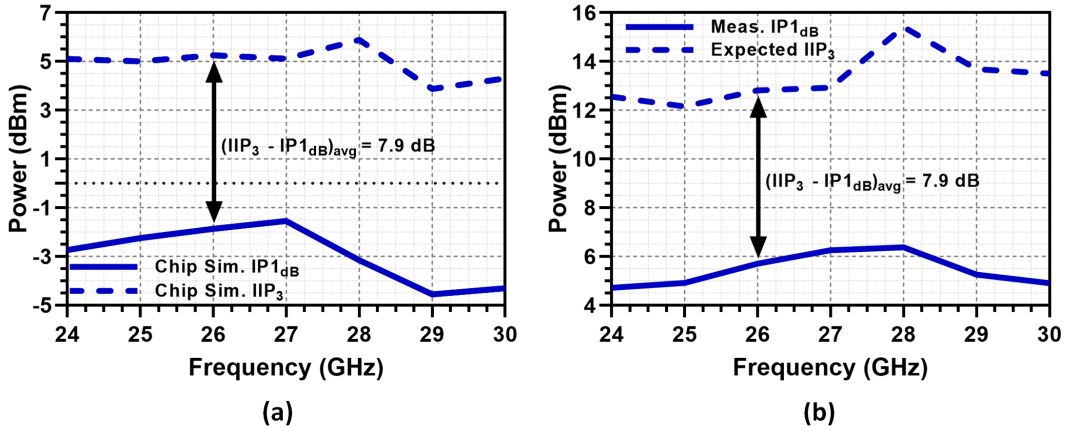


Figure 2.44: Difference between (a) the simulated chip IP_{1dB} with IIP_3 and (b) measured chip IP_{1dB} with expected IIP_3 of the mixer.

passive circuits. The LC resonator circuit limits the RF leakages to the current tail transistor. However, these can not be suppressed totally. So, the instantaneous peak signal is limited, and so is the linearity. The $\text{OP}_{1\text{dB}}$ is -3.02 dBm, 0.8 dB lower than the simulated value, at 26 GHz input frequency, with IF of 6 GHz, as shown in Fig. 2.43 (a).

The IIP_3 of the mixer was able to be simulated in chip and chip with board setup, as shown in Fig. 2.43 (b). The IIP_3 is in average 7.9 dB above the $\text{IP}_{1\text{dB}}$ for both simulations. This can provide a rough idea about the measured IIP_3 values through the measured $\text{IP}_{1\text{dB}}$. It would be expected that the measured IIP_3 will be 7.9 dB higher than the measured $\text{IP}_{1\text{dB}}$, as shown in the Figure 2.44.

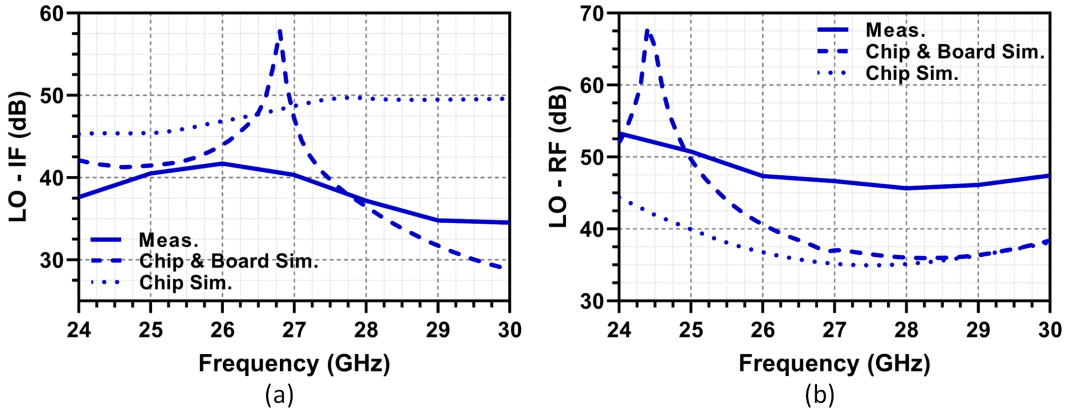


Figure 2.45: The measured, simulated chip & board, and simulated chip (a) LO-IF, and (b) LO-RF isolation of the mixer.

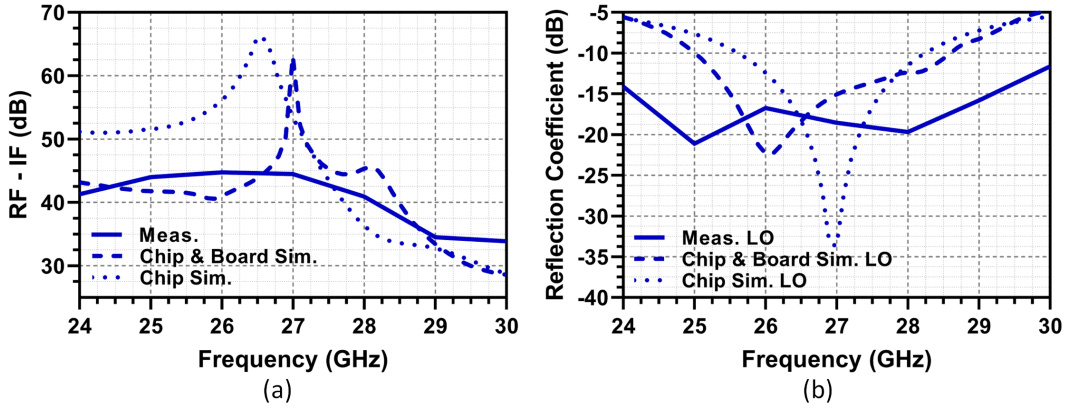


Figure 2.46: The measured, simulated chip & board, and simulated chip (a) RF-IF isolation, and (b) LO reflection coefficient of the mixer.

The measured LO-IF, LO-RF, and RF-IF isolation are higher than 35 dB for the entire frequency range, as shown in Fig. 2.45-2.46 (a) respectively. Even though the input is fed as a single-ended signal, the isolation values are comparable with the fully balanced designs. The high LO-RF isolation values and the decreased CG compared to the simulations justify the increase in the measured IP_{1dB}. The return loss at the LO and IF ports are below 10 dB for the band, as shown in Fig. 2.46 (b) and Fig. 2.47 (a). However, the RF port has a return loss of less than 10 dB for frequencies lower than 27.5 GHz, as shown in Fig. 2.47 (b). The RF and LO port return losses are depicted in their corresponding frequency range; and the IF is fixed at 6 GHz and shown for each f_{RF} - f_{LO} case, as shown in Fig. 2.46 (b) - 2.47.

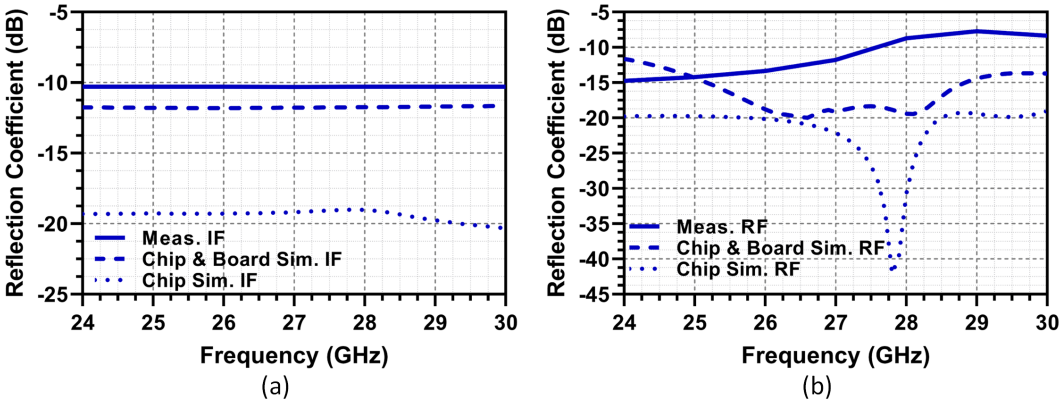


Figure 2.47: The measured, simulated chip & board, and simulated chip (a) IF, and (b) RF reflection coefficient of the mixer.

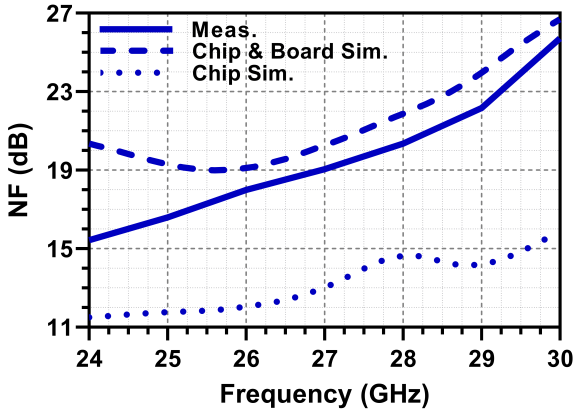


Figure 2.48: The measured, simulated chip & board, and simulated chip NF of the mixer.

The SSB NF is below 15 dB for the entire frequency band for the EM simulated chip, 2.48. The NF has drastically increased due to the PCB board effects. The IF is fixed to 6 GHz; the RF power is -15 dBm and the LO power is -2 dBm for the measurements.

Three different Figure of Merit (FoM) values are scrutinized, which are given in (2.3.1), (2.3.2), and (2.3.3). $\mathrm{FoM_1}$ considers $\mathrm{OP_{1dB}}$ and $\mathrm{P_{LO}}$ to signify the mixer's linearity. The only difference between $\mathrm{FoM_2}$ and $\mathrm{FoM_3}$ is that the latter does not consider NF. These two FoMs are more general than the $\mathrm{FoM_1}$ since almost all specifications are considered.

$$FoM_1 = \frac{OP_{1dB}[mW]}{P_{LO}[mW]} \tag{2.3.1}$$

$$FoM_2 = 10\log\left(\frac{10^{\frac{CG[dB]}{20}} \times 10^{\frac{IP_{1dB}[dBm]}{10}}}{10^{\frac{F[dB]}{10}} \times P_{DC}[W]}\right) - P_{LO}[dBm] \tag{2.3.2}$$

$$FoM_3 = 10\log\left(\frac{10^{\frac{CG[dB]}{20}} \times 10^{\frac{IP_{1dB}[dBm]}{10}}}{P_{DC}[W]}\right) - P_{LO}[dBm] \tag{2.3.3}$$

The design, implementation, and characterization results of a down-converter mixer for the 5G applications are presented. In the demonstrated mixer topology, we proposed a modified transconductance stage that amplifies the input signal and converts the single-ended signal to a differential one. Compared to conventional ones, such modification provides significant area gain since a transformer or separate active balun is not employed. However, for symmetry purposes, the bias network of the transconductance stage is placed in the middle left part, increasing area consumption. The modifications utilized for linearity improvement are emitter degeneration and balun loaded design. Table 2.6 introduces the FOMs and performance parameters to compare the proposed mixer with the previously designed ones in mm-wave frequencies. The proposed mixer illustrates comparable IP_{1dB} and isolation compared to other studies in the table, even though the input stage performs single-ended to differential conversion and amplification. The increase in LO power to -2 dBm for measurement has halved the FoM1 of our work compared to the simulation. The measured FoM_2 has a negative value due to the increased NF values due to the board losses. The FoM_1 has an average value of 0.59 and a standard variation of 0.25, these values for FoM_2 are -4.34 and 4.54, and FoM_3 are 15.28 and 1.46 respectively for the RF frequency range of interest. The power consumption is higher to improve linearity and decrease noise

All three FoMs of our work are lower than those in [31] since it employs IF buffers to enhance the CG considerably, an external IF balun to minimize the losses in the circuit, and the IF frequency range is lower than our work. FoM_2 and FoM_3 of the [28] are better due to the low power technology that enables power consumption of 6 mW while the linearity is preserved. FoM_3 of the [29] likewise has better performance due to low power consumption, 10 mW. The common characteristics of these three works, [28], [29], [31], are that an IF buffer is employed to enhance CG, the CMOS technology node used is lower (low power consumption), and a lower IF frequency range. The IF is measured differentially in [28], [29], and an external balun is used in [31]. This modified mixer topology shows that it performs in the same way as the double balanced mixer. Contrary to the single-balanced and micromixer topologies which also implement a single-ended input, the isolation is not deprived.

Table 2.6: Comparison of the presented Mixer with similar works in the literature.

Reference		[42] @ 14 GHz TMTT'06	[26] TMTT'10	[27] MTTS'10	[28] TCASII'14	[41] RFIC'16	[31] @ 25GHz VLSI'17		[29] RFIT'18	[43] APMC'18	[30] '20	[44] APMC'20	This work		
													Chip Sim.	C. B. Sim.**	Meas.
Architecture		Active	Active	Passive	Active	Passive	Active		Active	Passive	Active	Active		Active	
IF buffer		Yes	No	No	Yes	Yes	Yes		Yes	No	No	Yes		No	
LO buffer		No	Doubler	No	No	Yes	No		No	No	No	No		No	
RF	**Balun**	MM[1]	No	No	M[4]	No	2 BR[5]	3 BR	M	M	T	No		No	
	Meas.	SE[2]	SE	SE	SE	SE	SE		SE	SE	SE	SE		SE	
LO	**Balun**	M	No	No	M	No	T[6]		M	M	T	No		T	
	Meas.	SE	D[3]	SE	SE	SE	SE		SE	SE	SE	D		SE	
IF	**Balun**	No	No	No	No	No	E[6]		No	M	T	No		T	
	Meas.	SE	D	SE	D	SE	SE		D	SE	SE	D		SE	
CG (dB)		12.8	3	-8	0	8.9	17.2	15.5	-3.2	-9.5	-12.9	12	0.48	-6.8	-7.72
IP_{1dB} (dBm)		-20	-8.4	-1.5*	-1	-9.3	-7.1	-9.6	0	12	6.4	-14.8	-1.7	0.85	5.7
IIP_3 (dBm)		-8	0.5-2.6	8.1	9.5	-2.3	2.5	0	21 (5)	21.6 *	16*	-5.2*	5	7.5	12.9**
OP_{1dB} (dBm)		-8.2	-6.4	-10.5	-2	-1.4	9.1	4.9	-4.2	1.5	-7.5	-3.8	-2.22	-6.95	-3.02
NF (dB)		20	11.5	13	16	10.4	15	12.5	-	-	23.3	12	12.04	19.1	18
Isolation (dB)		22	15	15	46	-	25.6	25.7	-	15	30	-	30	28	35
f_{RF} (GHz)		1.1-18.1	20-32	22-39	20-50	20-30	22.5-28.5	21.5-32.5	23-30	25.5-28.5	24-28	25-31		24-30	
f_{IF} (GHz)		0.1	0-12	0.1	0.1	0-0.25	0-1.5		-	3	3	0.1		6	
P_{LO} (dBm)		6	5	3	0	4	3		1	15	6	0	-5	-13	-2
V_{CC} (V)		5	1.8	1.5	1.2	0.9	1.2		1.2	-	3.3	1.2		3.3	
P_{DC} (mW)		60	18	0	6	41	7.1		10	0	29.7	25	64	54	56
Area (mm^2)		1	0.19	0.33	-	1.7	0.88		0.6	2	0.26	0.1		1	
FoM_1		0.03	0.07	0.04	0.63	0.29	4.1	1.54	0.3	0.04	0.04	0.41	1.87	4.02	0.79
FoM_2		-27.38	-5.95	-	5.21	-5.38	4.98	4.13	-	-	-14.07	-4.77	3.43	4.02	-1.63
FoM_3		-7.38	5.54	-	21.21	5.02	19.98	16.63	17.4	-	9.22	7.22	15.47	23.12	16.35
Tech. (nm)		350 SiGe BiCMOS	180 BiCMOS	350 SiGe	90 CMOS LP	45 SOI CMOS	65 CMOS		90 CMOS	130 GaAs mHEMT MMIC	130 SiGe BiCMOS	22 FD-SOI		130 SiGe BiCMOS	

[1]MM : Micromixer, [2]SE : single-ended, [3]D : differential, [4]M : marchand, [5]BR : Bondwire Resonator, [6]T : transformer [7]E : external

*Estimated $IP_{1dB} = IIP_3 - 9.6$, **Expected.

2.4 Multi-technology simulations for flip chip packaging

The unpredictable PCB losses during simulations and mismatches between measurements and simulations lead to the investigation of the RFPro multi-technology simulation setup for flip chip packaging. The step-by-step tutorial for the simulation setup is provided in B. Appendix. The simulation results of the RFPro simulator are provided below and compared with the previously presented results (measurement, chip & board simulation, and chip simulation) and the setup definition is provided in Table 2.7.

The RFPro simulated CG shows very close values until 28 GHz with the measured CG, as shown in Fig. 2.49 (a). The RFPro simulated IP_{1dB} and OP_{1dB} shows a similar trend to the chip & board simulated separately, due to the losses on the RF path of the PCB, as shown in Fig. 2.49 (b) and Fig. 2.50 (a). The RFPro simulated NF shows a closer value to the measured NF compared to the chip & board simulated separately NF, as shown in Fig. 2.50 (b).

Table 2.7: Measurement and Simulation setup variable values.

	Meas.	Chip & Board Sim.	Chip Sim.	RFPro Chip & Board Sim.
P_{RF} (dBm)	-15	-15	-15	-15
P_{LO} (dBm)	-2	-13	-5	-10
V_{CC} (V)	3.3	3.15	3.3	3.125
I (mA)	17	17	20	17
Comments		Momentum RF Sim. Chip FEM Sim. Board Seperately	Momentum RF Sim. Chip	RFPro Sim. FEM Chip & Board connected through Solderball

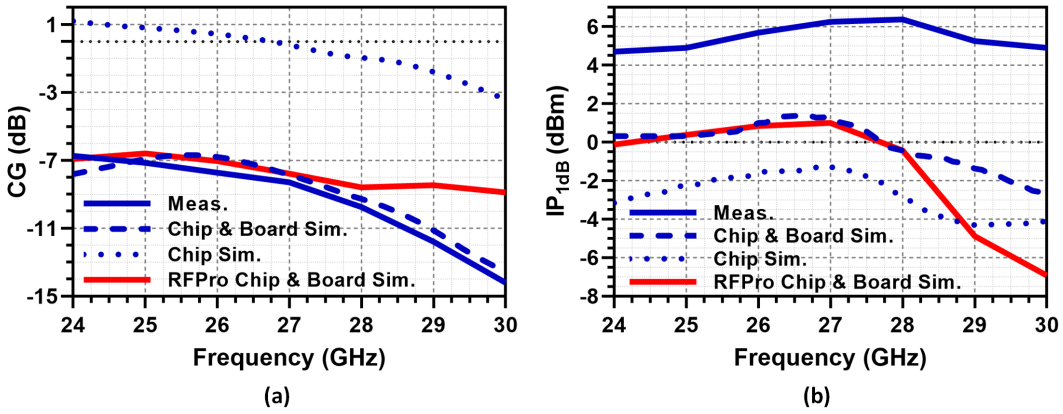


Figure 2.49: The measured, simulated chip & board, simulated chip, and RFPro simulated chip & board (a) CG, and (b) IP_{1dB} of the mixer.

The RFPro simulated isolation values exhibit lower values than the other simulation setups, as shown in Fig. 2.51 and Fig. 2.52. This provides a pessimistic approach to the isolation values for the expected measurements. The RFPro simulated reflection coefficients have closer values to the measured reflection coefficients, as shown in Fig. 2.52 (b) and Fig. 2.53.

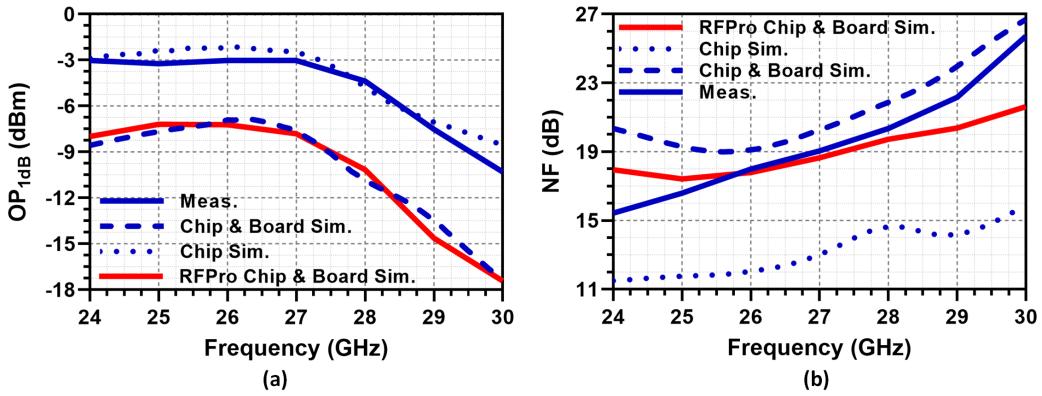


Figure 2.50: The measured, simulated chip & board, simulated chip, and RFPro simulated chip & board (a) OP_{1dB}, and (b) NF of the mixer.

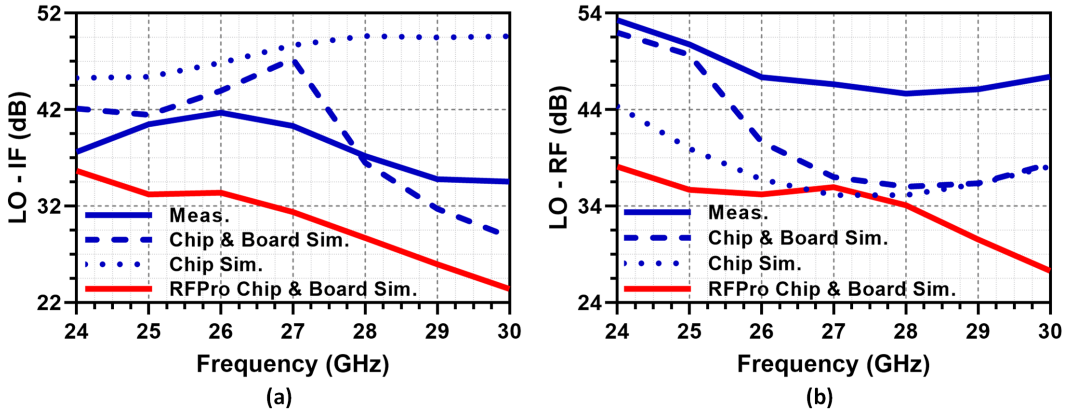


Figure 2.51: The measured, simulated chip & board, simulated chip, and RFPro simulated chip & board (a) LO - IF, and (b) LO - RF isolation of the mixer.

The RFPro simulation setup requires a lower LO power compared to the chip and board simulated separately, as shown in Table 2.7. This shows that the losses due to the solder balls are considered more accurate. However, the similarity between the RFPro simulated and the chip and board simulated separately IP_{1dB}, shows that the losses on the PCB paths cannot be predicted.

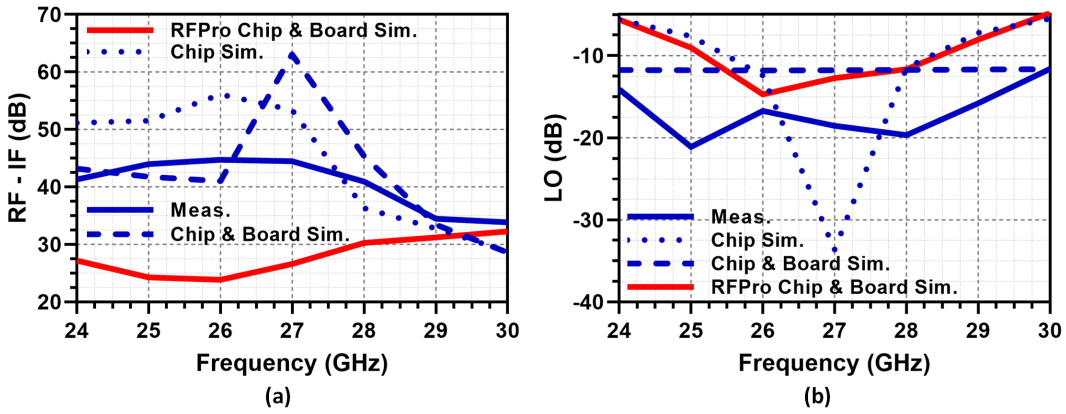


Figure 2.52: The measured, simulated chip & board, simulated chip, and RFPro simulated chip & board (a) RF - IF isolation, and (b) LO reflection coefficient of the mixer.

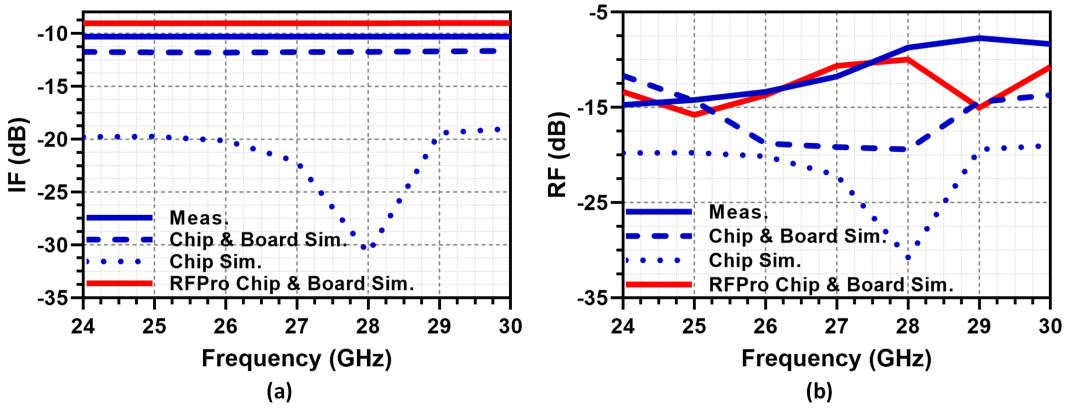


Figure 2.53: The measured, simulated chip & board, simulated chip, and RFPro simulated chip & board (a) IF, and (b) RF reflection coefficient of the mixer.

2.5 Optimizations on Performance Parameters

Optimizations to decrease area consumption and improve performance as much as possible are completed. The aim is to decrease the interconnection lengths, to minimize their effects and performance deprivation. The active components are not modified, and the transistor sizing remains the same. The floor-plan and layout geometry of the passive components are modified. The 3D layout view of the fabricated chip is shown in Fig. 2.54 (a), and the optimized one is shown in Fig. 2.54 (b). The area optimization was the first aim, so the layout geometry of the inductors is optimized, while the performance is not affected. The inductors modified are the resonator's one, L_2, and the emitter degeneration's one, L_3, (red square). The input matching is flipped in the x-axis for direct connection to the RF pad (blue square).

The floor plan of the biasing networks is modified to decrease the area consumed (violet and black squares). The geometry of the LO transformer balun is modified from the symmetric octagonal to an elliptical one. Finally, the capacitances in the IF transformer balun and low pass filter have been modified according to the matching and isolation trade-off, mentioned previously. The area is decreased from 2 mm^2 to 1.1 mm^2. The optimized chip layout is almost half of the initial one. The comparison between the fabricated chip and optimized chip simulation is provided below.

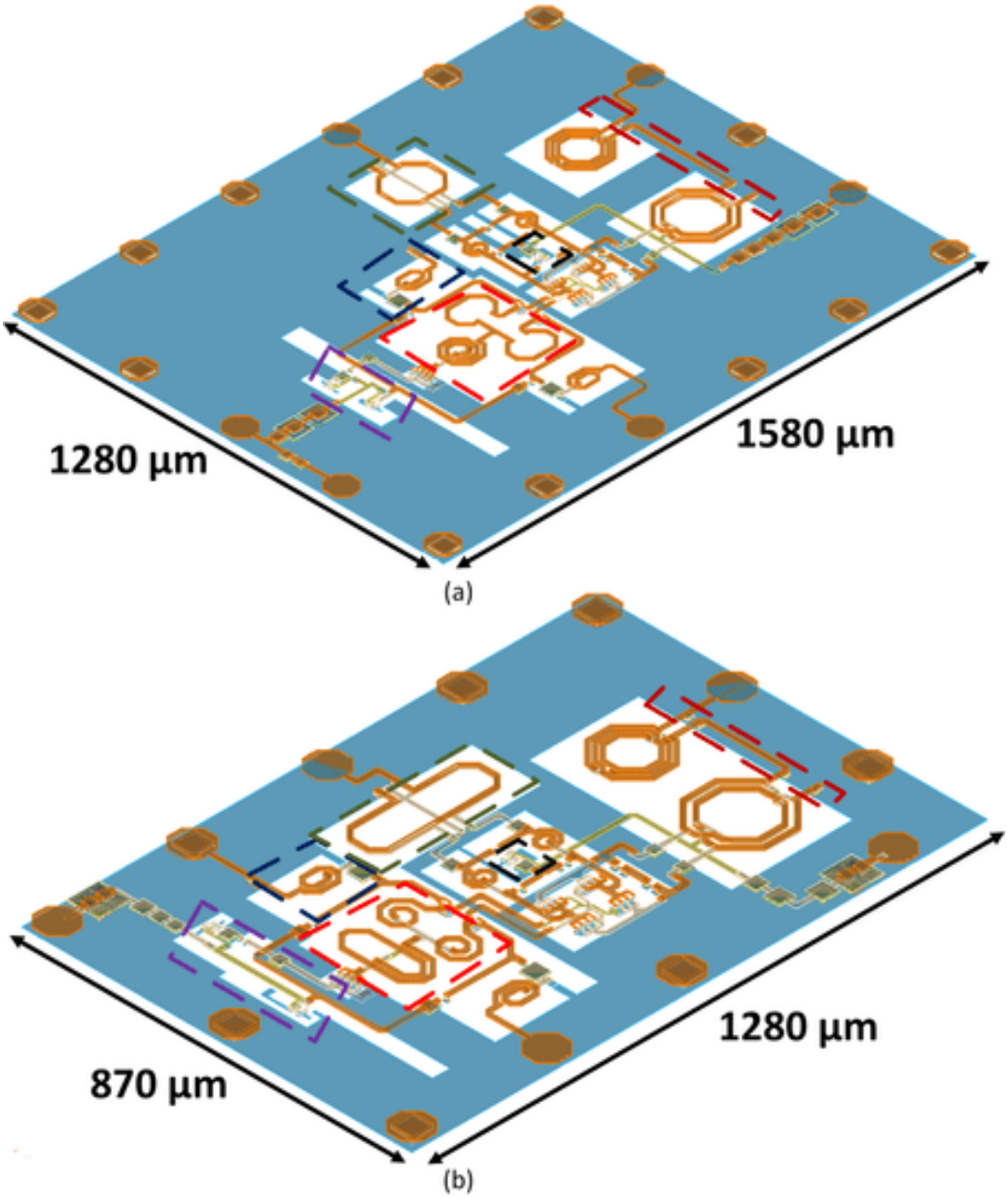


Figure 2.54: 3-D view of (a) the fabricated chip, and (b) the optimized chip.

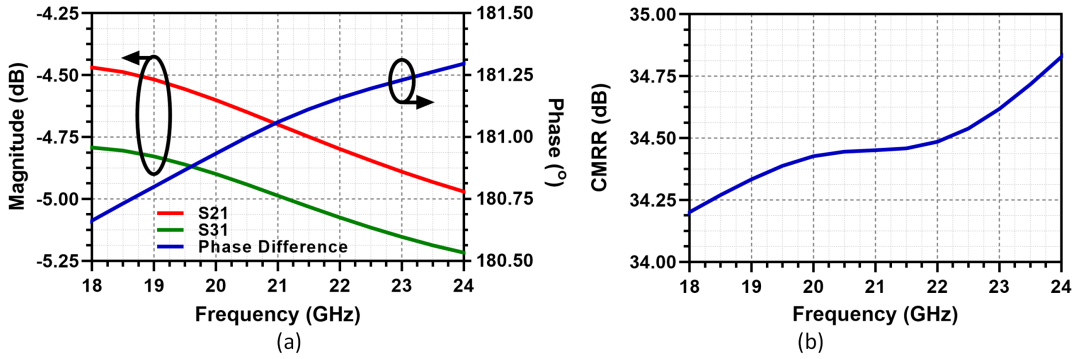


Figure 2.55: (a) Insertion loss and phase characteristics, and (b) CMRR of LO balun.

The simulated phase difference, S21, and S31 amplitudes are shown in Fig. 2.55 (a). The phase imbalance ranges from 0.66° to 1.3°, and the average phase imbalance is 1.02°. The insertion loss is 1.5 - 2.2 dB, the maximum amplitude imbalance is 0.32 dB and the average RMS amplitude imbalance is 0.082 dB. The CMRR is above 34 dB for the whole frequency range, indicating a good balance, as shown in Fig.2.55 (b). The optimized LO transformer balun has a better phase imbalance value and worse amplitude imbalance compared to the LO balun of the fabricated chip, Fig. 2.23. Moreover, the CMRR value has a higher minimum value compared to the LO balun of the fabricated chip, due to the better phase imbalance.

The simulated phase difference and S21, and S31 amplitudes are shown in Fig. 2.56 (a). The phase imbalance is 1.1° and the insertion loss is 2 dB at 6 GHz. The average phase imbalance is 1.3°, the average RMS amplitude imbalance is 1.2 dB and the maximum amplitude imbalance is 0.75 dB for the IF band as shown in Fig. 2.56 (a). The CMRR is above 22 dB for the whole frequency range, as shown in Fig.2.56 (b). The optimized IF transformer balun has a better phase imbalance value and worse amplitude imbalance compared to the IF balun of the fabricated chip, Fig. 2.25. The CMRR value of the optimized IF balun has decreased compared to the IF balun of the fabricated chip. Since the output matching has been optimized for considering the trade-off between the CG and isolation. The IF balun affects low pass filter response.

The transconductance stage has not been modified, however, due to modifications in the matching circuits and layout geometries. The simulation results of the active balun performance are presented in Fig. 2.57 (a). The phase error is 5.7° - 7.9° and the amplitude difference is below 1.45 dB for 24 - 27.5 GHz, the bandwidth of the resonator. The phase error of the optimized chip is higher for above 29.5 GHz compared to the fabricated chip. The amplitude difference of the optimized chip is

lower than 3 dB for the RF frequency range, while the amplitude difference of the fabricated chip is lower than 9 dB. Due to the shortened interconnection lines the amplitude imbalance have been decreased significantly.

The optimized LPF simulation results are presented in Fig. 2.57 (b). The RF frequencies are suppressed at -15 dB with the optimized LPF compared to 5 dB compression of the fabricated LPF. The reflection coefficient of the optimized LPF is at -25 dB, while the one of the fabricated LPF is at -10 dB.

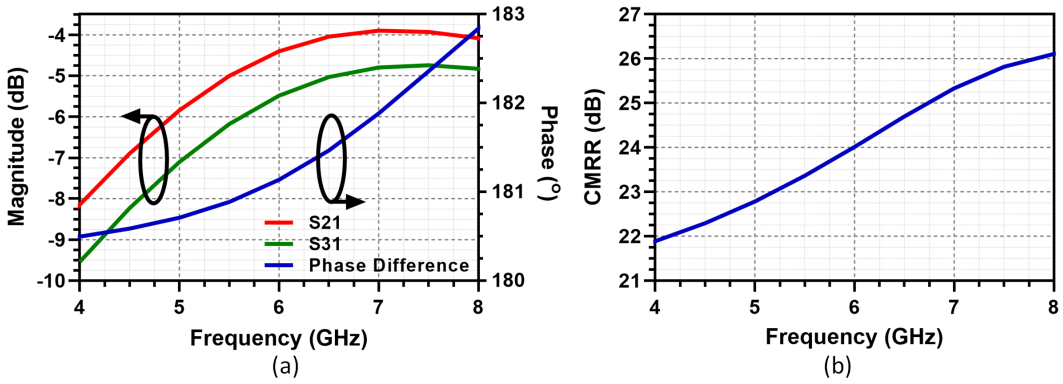


Figure 2.56: (a) Insertion loss and phase characteristics, and (b) CMRR of IF balun.

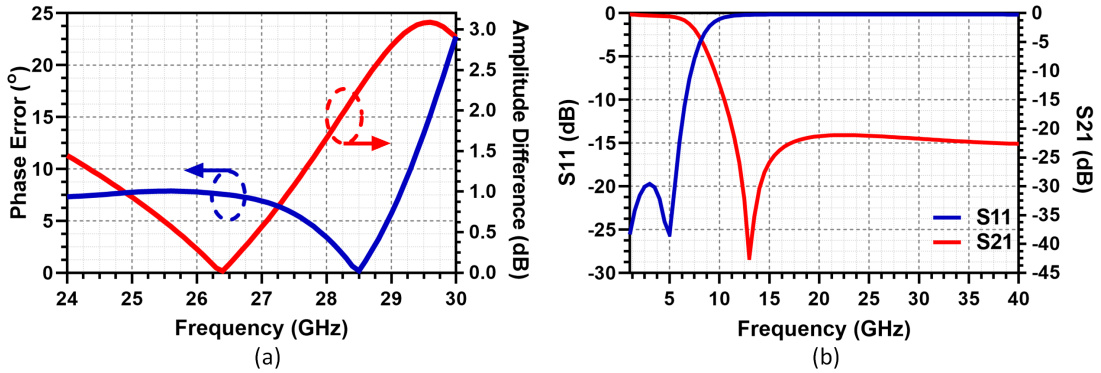


Figure 2.57: (a) Phase error and amplitude difference of the optimized chip (b) scattering parameters of optimized low pass filter.

The CG of the optimized chip has a higher value above 29 GHz compared to one of the fabricated chip. The CG of the optimized chip ranges from -1 dB to 1 dB, as shown in Fig. 2.58 (a). The IP_{1dB} depicts discontinuities due to the simulation step size of 0.2 GHz, as shown in Fig. 2.58 (b). This step size was selected for a shorter simulation period compared to the previous simulation results presented. The IP_{1dB} of the optimized chip depicts a close trend to the one of the fabricated chip. The OP_{1dB} of the optimized chip has higher values than the one of the fabricated chip above 28 GHz, as shown in Fig. 2.59 (a). The OP_{1dB} of the optimized chip ranges from -4 dB to -2 dB. The NF of the fabricated chip has lower values in the range of 26.5 - 28.5 GHz than the NF of the optimized chip, as shown in Fig. 2.59 (b). The NF of the optimized chip ranges from 11 dB to 15 dB.

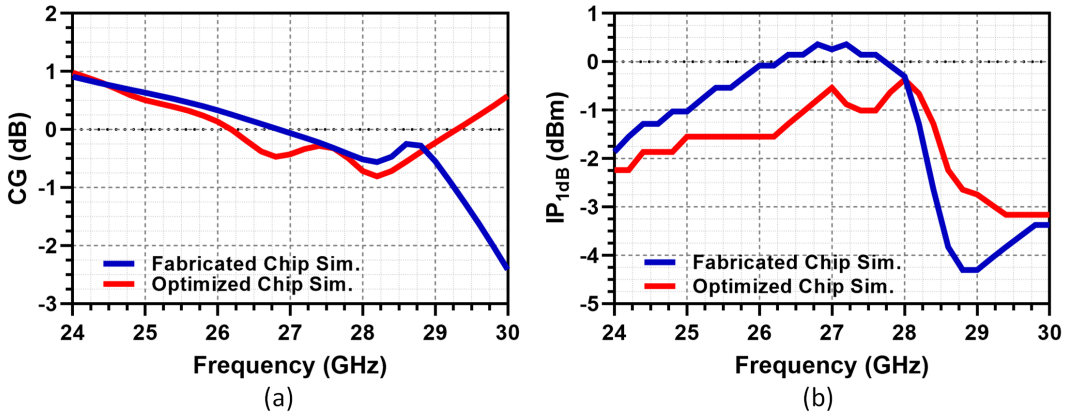


Figure 2.58: Simulation results of the (a) CG, and (b) IP_{1dB} of the fabricated and optimized chip.

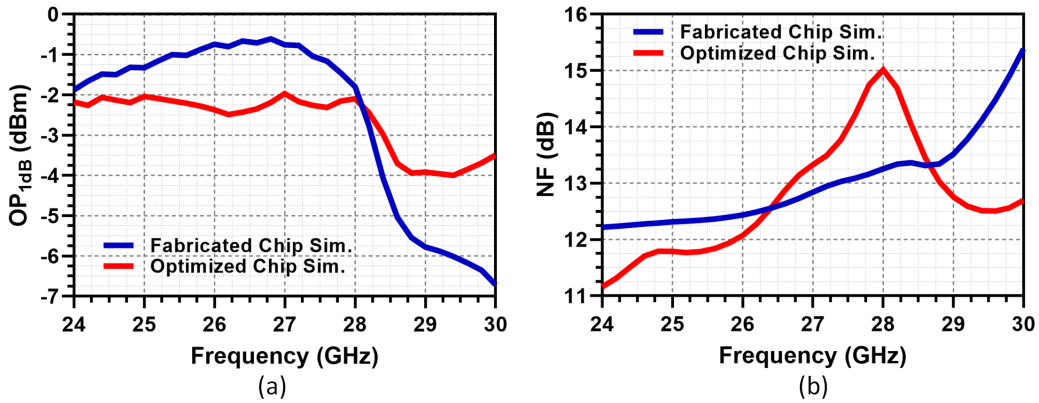


Figure 2.59: Simulation results of the (a) OP_{1dB}, and (b) NF of the fabricated and optimized chip.

The simulation results of the isolations are presented in Fig. 2.60 - 2.61 (a). The only drawback of the optimized chip is the lower LO - RF isolation values compared to the LO - RF of the fabricated chip, as shown in Fig. 2.60 (b). The reflection coefficients are presented in Fig. 2.61 (b) - 2.62. The matching circuits of the optimized chip have been modified to obtain the above-mentioned performance improvements.

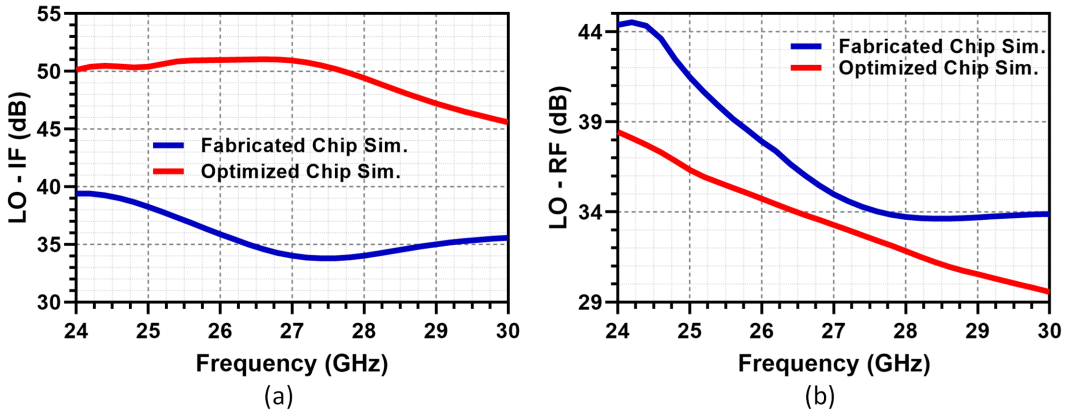


Figure 2.60: Simulation results of the (a) LO - IF, and (b) LO - RF isolation of the fabricated and optimized chip.

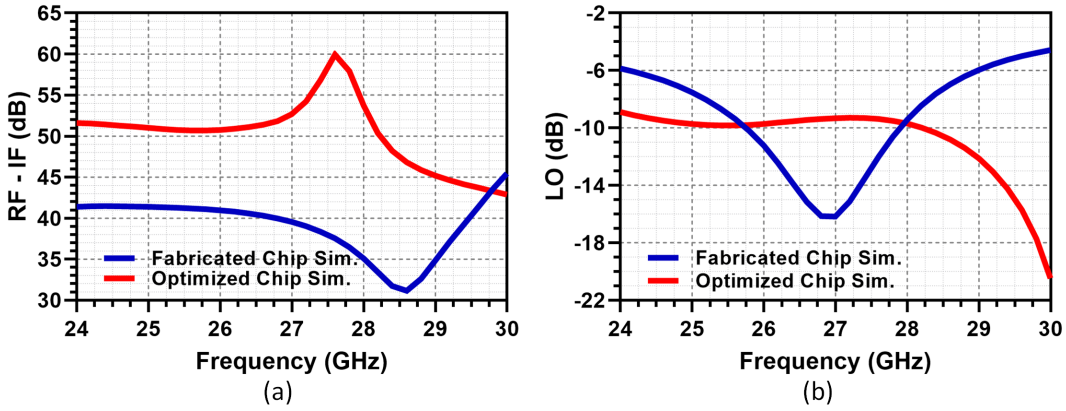


Figure 2.61: Simulation results of the (a) RF - IF isolation, and (b) LO reflection coefficient of the fabricated and optimized chip.

The performance comparison according to the FoM values has been presented in Table 2.8. The average of the performance metrics is according to the frequency range. These average values of the optimized and fabricated chip are comparable. The standard deviation of the optimized chip has a lower value for each performance parameter. Demonstrating that the performance of the optimized chip is more linear to the one of the fabricated chip. The isolation values of the optimized chip are higher

than the fabricated one. The component values modified for the optimized chip are provided in Table 2.9 with their respective values employed in the fabricated chip.

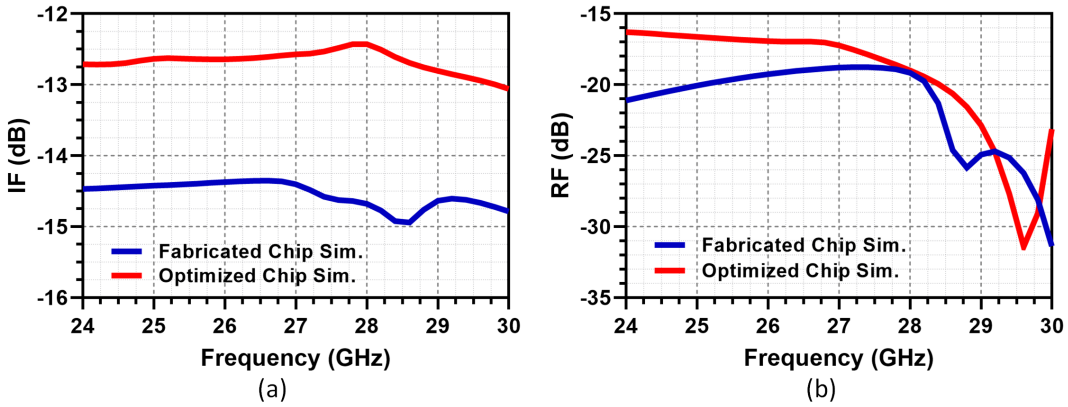


Figure 2.62: Simulation results of the (a) IF, and (b) RF reflection coefficient of the fabricated and optimized chip.

Table 2.8: Comparison of the simulation results of the fabricated Mixer chip with the optimized one.

	CG (dB)		IP_{1dB} (dBm)		OP_{1dB} (dBm)		NF (dB)		Isolation (dB)	
	AVG	SD	AVG	SD	AVG	SD	AVG	SD	MIN	MAX
Fabricated Chip Sim.	-0.15	0.8	-1.4	1.6	-2.5	2.1	13	0.8	31	45
Optimized Chip Sim.	0	0.5	-1.7	0.83	-2.65	0.7	12.7	1	30	60

	Area (mm^2)		FoM_1		FoM_2		FoM_3		P_{LO} (dB)	P_{DC} (mW)
	Core	With pads	AVG	SD	AVG	SD	AVG	SD		
Fabricated Chip Sim.	1.15	2	1.96	0.74	2.3	2.52	15.32	1.84	-5	66
Optimized Chip Sim.	0.68	1.1	1.74	0.26	2.35	1.11	15.09	0.74		

Table 2.9: Values of the components modified for the optimized chip and their respective values used for the fabricated chip.

	C_4 (fF)	C_6 (fF)	C_7 (fF)	C_9 (fF)	C_{10} (fF)
Fabricated Chip Sim.	180	155	90	400	50
Optimized Chip Sim.	200	112.5	150	200	400

3 Frequency Synthesizer

In this chapter, the design of a Type-II analog phase-locked loop (PLL) for a frequency synthesizer is going to be scrutinized. The PLL architectures, parameters, and fundamentals are described. The design procedure of each sub-block and system is justified by simulation results. Finally, the measurement results and comparison of the measured blocks with their corresponding blocks in the literature are presented.

3.1 Phase Locked Loop Fundamentals

The application field mainly determines the PLL architecture to be designed. The fields of application are digital, analog, or control systems. The PLL block is employed for jitter reduction on synchronous systems, skew suppression of the distributed clock on a PCB, and clock recovery on wireline communications of digital systems. In analog systems, the PLL is utilized as a frequency synthesizer for cellular phones, a frequency demodulator for FM radios, and a tracking filter for satellite communications. Moreover, PLLs are used in control systems to adjust the motor speed. The topologies of the sub-blocks are determined according to the application field.

The application field of the PLL discussed in this thesis is frequency synthesis for 5G cellular phones. Phase locked loop is a closed loop feedback system used to adjust the output frequency and phase of the oscillator to the input frequency of the reference signal. This controllable PLL output signal will be the LO input signal of a mixer. Before discussing the sub-blocks and their contribution to the system, the quantities that define the frequency synthesizers and system level operation is going to be scrutinized.

3.1.1 PLL Parameters

Phase noise and jitter are two related quantities. Their difference lies in which domain they are defined. Phase noise is in the frequency domain, while jitter is in the time domain. Phase noise characterization of noise is used for analog systems, while jitter is used for digital systems. Jitter is described as the variation in the time delay between the generated and ideal signal. Jitter can be categorized as timing, periodic, cycle-to-cycle, and random [45].

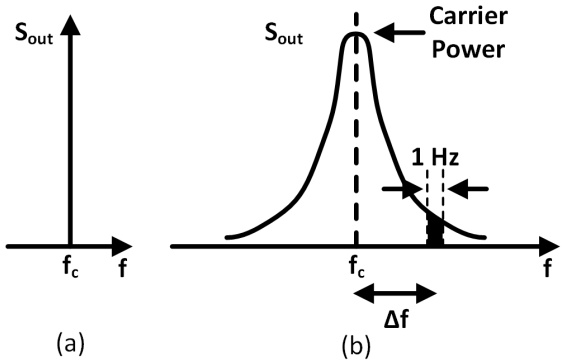


Figure 3.1: Output spectrum of (a) ideal, (b) noisy oscillator.

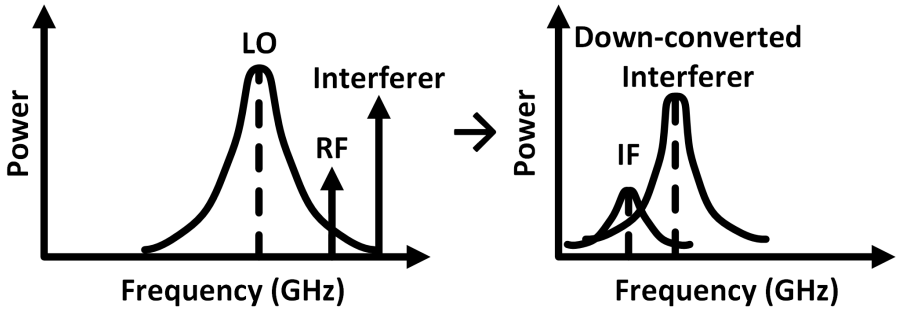


Figure 3.2: Effects of LO phase noise to the IF output when interference signal is present.

Ideally, the output spectrum of a noiseless oscillator is only the carrier power, as shown in 3.1 (a). However, due to random fluctuations in the frequency, the spectrum in Fig. 3.1 (b) is observed. The noise performance of an oscillator and PLL is characterized by phase noise. It is the power measured with 1 Hz bandwidth at an offset of Δf from the carrier frequency. This measured power is normalized using the peak carrier power [1]. The unit describing the phase noise is dBc/Hz, dB relative to the carrier. The effects of a PLL with high phase noise to a mixer when an interference signal is present, are shown in Fig. 3.2. It is observed that the IF signal is distorted due to the interference signal. The phase noise requirements are determined according to the expected SNR and interference power levels. Generally, a phase noise as low as possible is required for frequency synthesizers.

The spurs are observed in the phase noise output spectrum due to reference feed through. When the reference signal is periodically phase modulated so, spurs are the undesirable spikes at different frequency offsets, as shown in Fig. 3.3 [1]. The effects of spurs when they down-convert the interference signal can lie very close to the IF frequency band. This undesirable signal cannot be filtered out, as shown in Fig. 3.3.

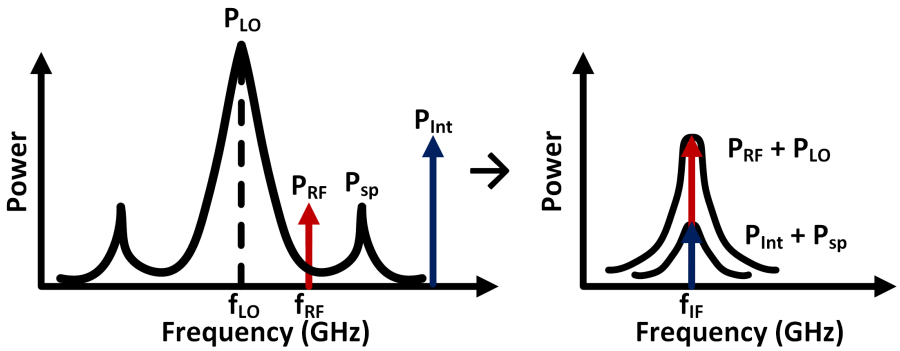


Figure 3.3: Effects of spurs with interference signals to the IF output.

Settling/lock time is the maximum time, defined by each communication standard, in which the PLL must switch to a new frequency channel. If the switching time takes a very long time for a cellular phone. The signal of this phone will interfer to the other users.

During the settling time, there can be different ranges. The lock-in range is when the output frequency synchronizes with the reference frequency immediately. The pull-in or acquisition range is when the output frequency synchronizes with the reference frequency in the end after some skip cycles occur. Cycle skipping is when the feedback loop does the opposite control needed, due to the frequency limitation of the sub-blocks. Even though the erroneous control is generated eventually, the feedback system eliminates the frequency and phase error. The hold-in or synchronization range is when the output frequency is synchronized with the reference frequency, however, the lock may not be maintained [7].

Low power and area consumption is required for longer battery life, and lower fabrication costs respectively. However, lower phase noise is obtained through higher power consumption. This trade-off must be carefully handled.

3.1.2 PLL Architectures

The PLL architectures employed as frequency synthesizers can be categorized according to the division technique. The division can be done in through the integer and fractional approach, as shown in Fig. 3.4 and Fig. 3.5 respectively.

So far, it is discussed how the output frequency and phase are synchronized with the input reference ones. The oscillator output frequency is in the mm-wave range (GHz range), such that it can be used as an LO signal for 5G applications. The fixed reference input signal is on the lower side of the radio frequency range

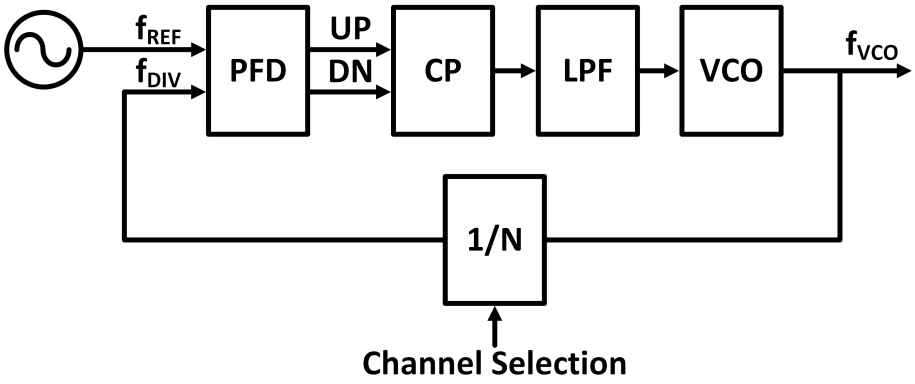


Figure 3.4: Integer-N PLL architecture.

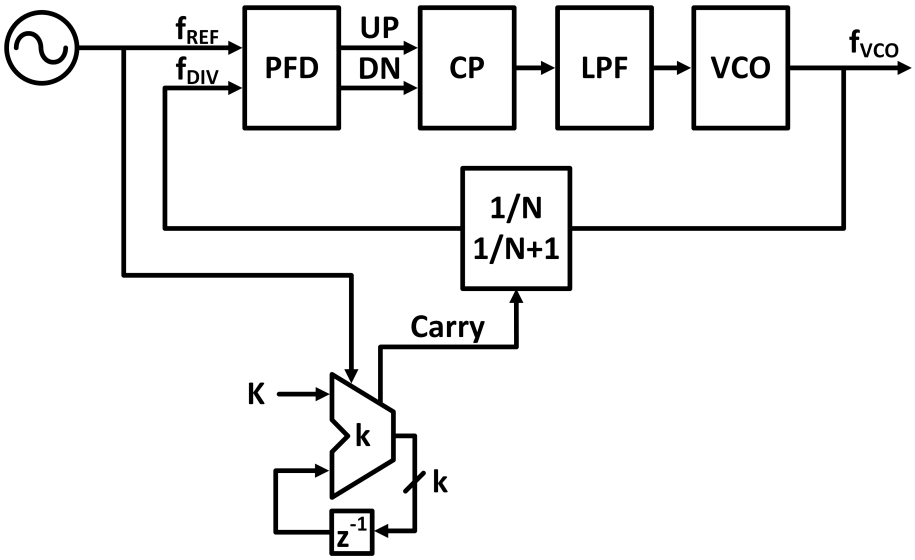


Figure 3.5: Fractional-N PLL architecture with digital accumulator.

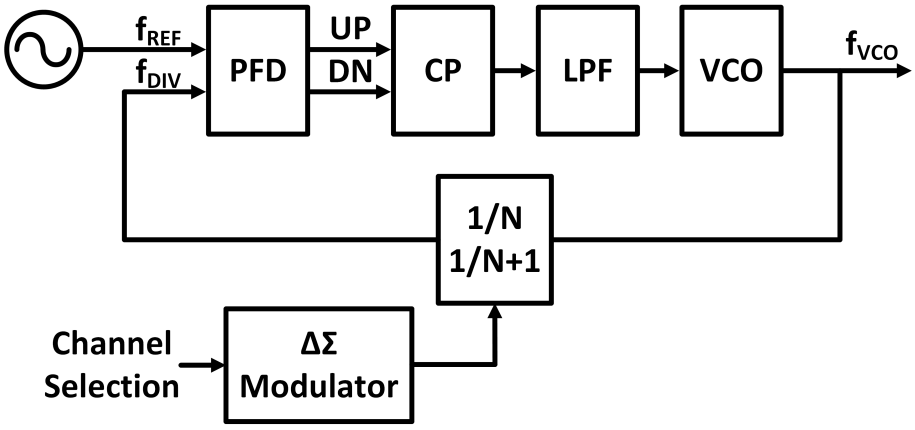


Figure 3.6: Fractional-N PLL architecture with $\Delta\Sigma$ modulator.

(MHz range), since low noise, stable, and high Q crystal oscillators are available in low frequencies. The phase frequency detector (PFD) compared the reference signal with the output of the divider. The output of the PFD is pulse sequences with a

pulse width proportional to the frequency/phase difference between the reference and divider signals. The charge pump (CP) with the loop filter (LF) generates the control voltage supplied to the voltage-controlled oscillator (VCO). The CP either adds charge to the LF or takes charge from LF according to the UP and DN signals of the PFD. The LF has a low pass filter characteristic, diminishing any high-frequency phase noises and any ramps in the control voltage. The high-frequency output of the VCO is divided by the integer N to obtain a close low-frequency signal to the reference frequency signal, as shown in Fig. 3.4. The division rate N ranges according to the f_{VCO} channel range. The relation between the output and reference frequency is given in (3.1.1), this demonstrates that the output frequency of the oscillator can be only integer multiples of the reference frequency. When low reference frequency is defined, since it determines the channel spacing, the N division ratio must be enlarged. This minimizes the allowable loop bandwidth, so the settling time will increase. Moreover, this magnifies the phase noise of the reference and other sub-blocks [46].

$$f_{VCO} = N \cdot f_{REF} \tag{3.1.1}$$

The higher reference frequency is enabled through the fractional PLL architecture, while the channel spacing is not enlarged. The fractional division ratio is obtained through two division ratios, N and N+1, whose duty cycles are not equal. In this way, the weighted average of these two division ratios is generated [47]. The fractional division ratio of 100.1 can be generated by dividing the output frequency by 100, and by 101 every tenth cycle. The control of the divider can be done directly with external control input, which would increase the phase noise. Moreover, the averaging of the fractional divider ratio can be obtained through a digital accumulator, as shown in Fig. 3.5. The input of the k-bit digital accumulator is the digital word K. So, a carry bit is generated every $K/2^k$ period of the input frequency. The division ratio of N+1 will be active for K cycles, while the N for 2^k-K cycles [12]. The average division ratio is given in (3.1.2).

$$N_{frac} = \frac{(2^k - K) \cdot N + K \cdot (N+1)}{2^k} = N + \frac{K}{2^k} \tag{3.1.2}$$

Lower channel spacing is obtained, while higher reference frequency is chosen. However, due to the periodic modulus alterations, spurs at the output will be observed. To avoid large spurs, a $\Delta\Sigma$ modulator is implemented, as shown in Fig. 3.6. This is achieved since the process of determining which division ratio will be employed is randomized. So, the spurs caused due to the reference frequency and the noises at small offsets are eliminated [48]. The output of the $\Delta\Sigma$ modulator con-

sists of the DC control value of the divider and quantization noise. The spurs can be eliminated at DC and harmonics of the reference frequency if higher order $\Delta\Sigma$ modulator is employed. However, this will increase the complexity of the system, and require technology with good performance in the digital and mm-wave domain. Moreover, the high-frequency quantization noises can be suppressed by the LF [12].

3.1.3 PLL Dynamics and Noise Sources

The performance metrics and operation of the PLL can be easily comprehended through frequency domain analysis. To simplify the derivations, the PLL will be considered as a linear, time-invariant system (LTI) in its lock state. The open loop and closed loop transfer functions will be demonstrated. The number of poles in the open loop transfer function determines the order of the PLL [49]. The number of poles that are at the origin, otherwise the number of integrators in the open loop transfer function determines the type of the PLL.

Type-I PLL Linear Analysis

The mathematical block diagram of Type-I PLL is depicted in Fig. 3.7. It is observed that for the comparison of the input and output signals, a phase detector (PD) is sufficient. Since the PLL is assumed to be locked, so a small phase difference will only occur, such that a linear approximation of each block can be conducted. The output of the PD is the DC voltage proportional to the phase error, $\mathrm{K_{PD}}\cdot\phi_{\mathrm{e}}$. The LPF is modeled as a transfer function, F(s) since according to its order the F(s) will change. The divider is omitted for simplicity since it does not affect the loop dynamics. The VCO is modeled as an integrator with a gain of $\mathrm{K_{VCO}}$. The output frequency of VCO is its free-running frequency, ω_{free}, and the excessive phase, $\mathrm{K_{VCO}}\cdot\mathrm{V_{control}}$, as shown in (3.1.3). In (3.1.4), it is shown that the phase is the integral of the frequency. Moreover, the free running frequency will not be considered in this analysis since it is a fixed value. The relation between the phase and frequency and be transformed to the S-domain from the time domain, (3.1.5). These equations proved the reason for the VCO being represented as an integrator in the mathematical block diagram.

$$\omega_{out} = \omega_{free} + K_{VCO} \cdot V_{control} \tag{3.1.3}$$

$$\phi_{out}(t) = \int \omega_{out} dt = \omega_n t + K_{VCO} \cdot \int V_{control}(t) dt \tag{3.1.4}$$

$$\frac{\Phi_{out}(s)}{V_{control}(s)} = \frac{K_{VCO}}{s} \tag{3.1.5}$$

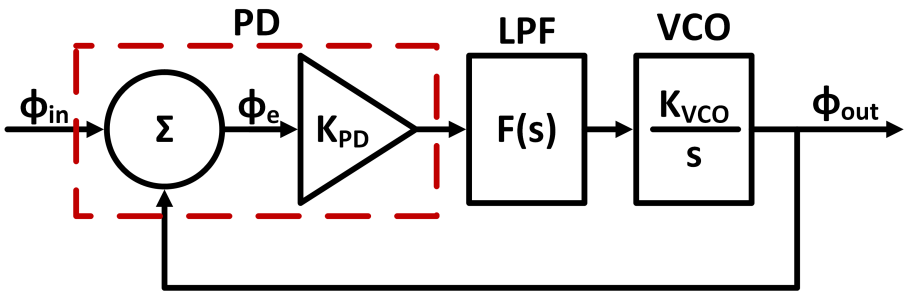


Figure 3.7: Mathematical block diagram of Type-I PLL.

The open loop, closed loop, and error transfer function are given in (3.1.6) - (3.1.8), respectively. In (3.1.6), there is only one integrator, suggesting that the PLL scrutinized is a Type-I. The loop dynamics for Type-I first and second order PLL are given in Table 3.1. The second-order transfer functions can be written in terms of ζ, the damping ratio, and ω_n, the undamped natural frequency [50]. The bandwidth of PLL is presented as ω_c.

$$G(s) = \frac{\Phi_{out}(s)}{\Phi_e(s)} = \frac{K_{PD} \cdot K_{VCO} \cdot F(s)}{s} \tag{3.1.6}$$

$$H(s) = \frac{\Phi_{out}(s)}{\Phi_{in}(s)} = \frac{G(s)}{1 + G(s)} = \frac{K_{PD} \cdot K_{VCO} \cdot F(s)}{s + K_{PD} \cdot K_{VCO} \cdot F(s)} \tag{3.1.7}$$

$$E(s) = \frac{\Phi_e(s)}{\Phi_{in}(s)} = \frac{1}{1 + G(s)} = \frac{s}{s + K_{PD} \cdot K_{VCO} \cdot F(s)} \tag{3.1.8}$$

Table 3.1: Loop Dynamics for Type-I; 1st and 2nd order PLL. [7] [8]

F(s)	K_{LPF}	$\frac{K_{LPF}}{1+\frac{1}{\omega_{LPF}}}$
G(s)	$\frac{K_1^*}{s}$	$\frac{K_1}{s\left(1+\frac{1}{\omega_{LPF}}\right)}$
H(s)	$\frac{K_1}{s+K_1}$	$\frac{K_1}{K_1+s+\frac{s^2}{\omega_{LPF}}}$
E(s)	$\frac{s}{s+K_1}$	$\frac{s(s+2\zeta\omega_n)}{s^2+2\zeta\omega_n s+\omega_n^2}$
$\boldsymbol{\omega_c}$ **(Hz)**	K_1	$2\zeta\omega_n$
$\boldsymbol{\zeta}$	-	$\frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_1}}$
$\boldsymbol{\omega_n}$	-	$\sqrt{\omega_{LPF} \cdot K_1}$
Stability	Unconditionally	Unconditionally
Order	1^{st}	2^{nd}

$^*K_1 = K_{PD} \cdot K_{LPF} \cdot K_{VCO}$,

The first-order Type-I PLL has a low pass response for the closed loop transfer function. Any signal with a higher frequency than ω_c will be suppressed. The stability is examined through the open loop transfer function. The maximum phase of the open loop transfer function is -90° since G(s) consists of only one integrator. The phase margin (PM), is defined as the phase change necessary to make a closed loop system unstable. The PM formula is defined in 3.1.9. For this case, the minimum PM is 90°, so the system is unconditionally stable. Enlarging the K_1 will minimize the steady state phase error for a channel shift. However, this will increase the loop bandwidth, and settling time. So, the phase error cannot be minimized, while the loop bandwidth is not enlarged. Moreover, the phase error is accumulated continuously, locking will be lost in this case.

$$PM = \phi_{0dB} - (-180^o) \tag{3.1.9}$$

The second-order Type-I PLL has ω_{LPF} as a variable to define the ω_n, ζ. However, in this case, also the necessary degree of freedom is not obtained. The phase of the open loop transfer function approaches -180°, but never reaches it. So, the PM value is important to avoid peaking in the transfer function.

Second-order Type-II PLL Linear Analysis

The charge pump PLL, demonstrated in Fig. 3.8, is a second-order Type-II PLL. The advantages of Type-II are the zero static phase error ideally, and the acquisition range is only determined by the tuning range of VCO [51]. The second integration to the loop is added through the CP which will make even a single capacitor act like an integrator. This is possible since the CP either charges, discharges, or no charge is leaked according to the following cases respectively. The output leads the input signal, the input signal leads the output signal, and the phase error

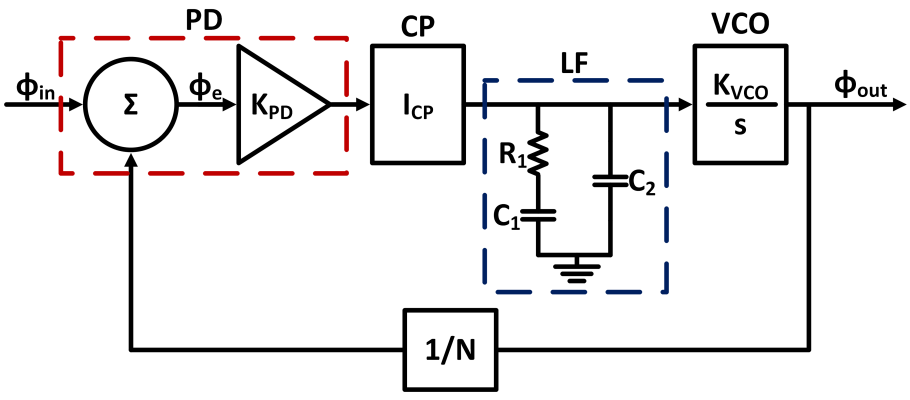


Figure 3.8: Mathematical block diagram of Type-II PLL.

between input and output signals is zero. However, the loop stability will deprive in this configuration, [52]. This is resolved by a series capacitor and resistor in LF, R_2, and C_2, which establishes a zero. So, the CP is modeled as a voltage to current converted with a current gain of I_{CP} value. The transfer function of the LF is given in (3.1.10), which can be written in the zeros and poles format, (3.1.11). Equation (3.1.12) - (3.1.13) provide the zero and pole definitions, respectively. The ω_p definition is approximated since C_2/C_1 is considered much smaller than 1 for simplicity.

$$Z(s) = \frac{1 + sR_1C_1}{sC_1\left(1 + \frac{C_2}{C_1} + sR_1C_2\right)} \tag{3.1.10}$$

$$Z(s) = \frac{1 + s/\omega_z}{sC_1\left(1 + s/\omega_p\right)} \tag{3.1.11}$$

$$\omega_z = \frac{1}{R_1C_1} \tag{3.1.12}$$

$$\omega_p \approx \frac{1}{R_1C_2} \tag{3.1.13}$$

The mathematical block diagram of VCO is the one discussed for the Type-I PLL. For completeness, the division ratio is added as an integer one for simplicity. The open, and closed loop transfer functions are given in (3.1.14) and in (3.1.15), respectively. The closed loop equation is simplified to a second-order one, considering that the ω_p is larger than the ω_n, which is $\sqrt{K}$ [53]. The analysis as a third-order loop system is given in [54]. The loop bandwidth is given in (3.1.16). For lower phase noise and faster settling, a wide loop bandwidth is suggested. While for better stability and lower spurs a narrow loop bandwidth is preferred. Table 3.2 represents the trade-offs between performance parameters for loop bandwidth and damping ratio. More detailed derivations of damping ratio, stability, and settling time can be found in [53].

$$G(s) = \frac{K_{PD} \cdot I_{CP} \cdot K_{VCO} \cdot (1 + s/\omega_z)}{s^2 \cdot N \cdot C_1 \cdot (1 + s/\omega_p)} = \frac{K \cdot (1 + s/\omega_z)}{s^2 \cdot (1 + s/\omega_p)} \tag{3.1.14}$$

$$H(s) = \frac{1 + s/\omega_z}{1 + s/\omega_z + s^2/K + s^3/(\omega_p \cdot K)} \approx \frac{1 + s/\omega_z}{1 + s/\omega_z + s^2/K} \tag{3.1.15}$$

$$\omega_c \approx \frac{\omega_n^2}{\omega_z} \tag{3.1.16}$$

Table 3.2: Design trade-offs of PLL block.

	Loop bandwidth	**Damping**
Faster settling	wide	under
Better stability	narrow	over
Lower phase noise	wide	N/A
Better spur rejection	narrow	N/A
Low jitter peaking	N/A	over
Low overshoot	N/A	over
Smaller capacitor size	wide	N/A

Noise Transfer Functions

The transfer functions of each noise source will be scrutinized, and their effect on the total phase noise be shown. The noise sources are added to the block diagram of the PLL, as shown in Fig. 3.9. The dominant noise sources are the VCO and input reference crystal oscillator, represented as the power spectral densities, S_{VCO}, and S_{in} respectively. The noise sources of the PFD and CP are taken into account as one, S_I. The LF is modeled as F(s) for clarity and S_{LF} as a noise source. The divider is omitted for simplicity. Each noise source is considered independent and projected to the output through its noise transfer function (NTF). The output noise power spectral density due to the input noise source is given in (3.1.17). Similar equations can be written for the other noise sources. The total output noise will be the summation of each noise source transferred to the output, given in (3.1.18) [55].

$$S_{\phi_{out}}^{in} = S_{\phi_{in}} \mid NTF_{in}(s) \mid^2 \tag{3.1.17}$$

$$S_{\phi_{out}}^{Total} = S_{\phi_{out}}^{in} + S_{\phi_{out}}^{I} + S_{\phi_{out}}^{LF} + S_{\phi_{out}}^{VCO} \tag{3.1.18}$$

The open loop transfer function of the PLL is given in (3.1.19), for compact equations. The derivation steps conducted for the noise transfer functions are covered in C. Appendix. The noise transfer function of the input, PD & CP, LF, and VCO is provided in (3.1.20) - (3.1.23). The LF will be considered as a block with

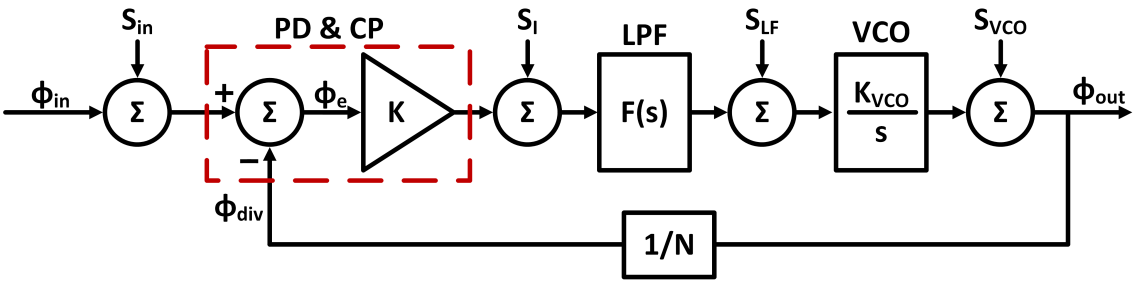


Figure 3.9: Mathematical block diagram of PLL with noise sources.

constant gain, K_{LPF}, and as an integrator, K_{LPF}/s. Such, that the bode plot of the NTF(s) can be predicted. It is observed that the input and PD & CP noise transfer functions have a low pass response for both LF cases. The LF responds as a low pass filter for the constant gain LF, and as a bandpass filter for the integrator LF. Finally, the noise transfer function of the VCO is a high pass filter. In Table 3.3 the response of each NTF(s) is summarized [56]. So, one considering the noise transfer functions can predict the optimum loop bandwidth to suppress dominant noise sources. High loop bandwidth must be utilized, when the noise from the VCO is higher than the input reference noise source [57]. However, for a stable system, the loop bandwidth must be at least ten times smaller than the input reference frequency. Low loop bandwidth would be preferred for the opposite case.

$$G(s) = \frac{K \cdot F(s) \cdot K_{VCO}}{s \cdot N} \tag{3.1.19}$$

$$NTF_{in}(s) = \frac{\phi_{out}(s)}{in(s)} = \frac{N \cdot G(s)}{1 + G(s)} \tag{3.1.20}$$

$$NTF_{I}(s) = \frac{\phi_{out}(s)}{I(s)} = \frac{\frac{N}{K} \cdot G(s)}{1 + G(s)} \tag{3.1.21}$$

$$NTF_{LF}(s) = \frac{\phi_{out}(s)}{LF(s)} = \frac{\frac{K_{VCO}}{s}}{1 + G(s)} \tag{3.1.22}$$

$$NTF_{VCO}(s) = \frac{\phi_{out}(s)}{VCO(s)} = \frac{1}{1 + G(s)} \tag{3.1.23}$$

Table 3.3: Response characteristic summary of each NTF(s).

	F(s)	
	$\mathbf{K_{LPF}}$	$\mathbf{K_{LPF}/s}$
$\mathbf{NTF_{in}(s)}$	LPF	LPF
$\mathbf{NTF_{I}(s)}$	LPF	LPF
$\mathbf{NTF_{LF}(s)}$	LPF	BPF
$\mathbf{NTF_{VCO}(s)}$	HPF	HPF

3.2 Circuit Description and Implementation

3.2.1 Phase Frequency Detector

The phase-frequency detector (PFD) is a digital sub-block that detects the phase or frequency difference between the two input clock signals. This phase difference is translated to the output as a series of pulses proportional to it. The reference signal at 100 MHz is fed to the circuit through the crystal oscillator, "ABRACON ABLO – 100 MHz", with phase noise of -155 dBc/Hz @ 1 MHz offset. The divider signal is the output of the divider block, which converts the high output frequency of the oscillator to a value close to the reference one. As shown in Fig. 3.10, the NAND-based PFD topology is preferred due to lower phase noise in higher frequencies than the NOR-based ones [58]. The first case is that a UP signal is generated when the reference signal leads the divider one; the second is that a DOWN signal is generated when the reference signal lags the divider one, as shown in Fig. 3.11. The last one is that the two input signals do not have a phase difference such that the UP and DOWN pulses are equal and narrow. The reset pulse will remain low as long as the inputs of its NAND gate are high. Both UP and DOWN signals will go high as the reset signal falling edge is fed to the following stages. The jitter in the UP and DOWN signals and the input frequency determine the phase noise.

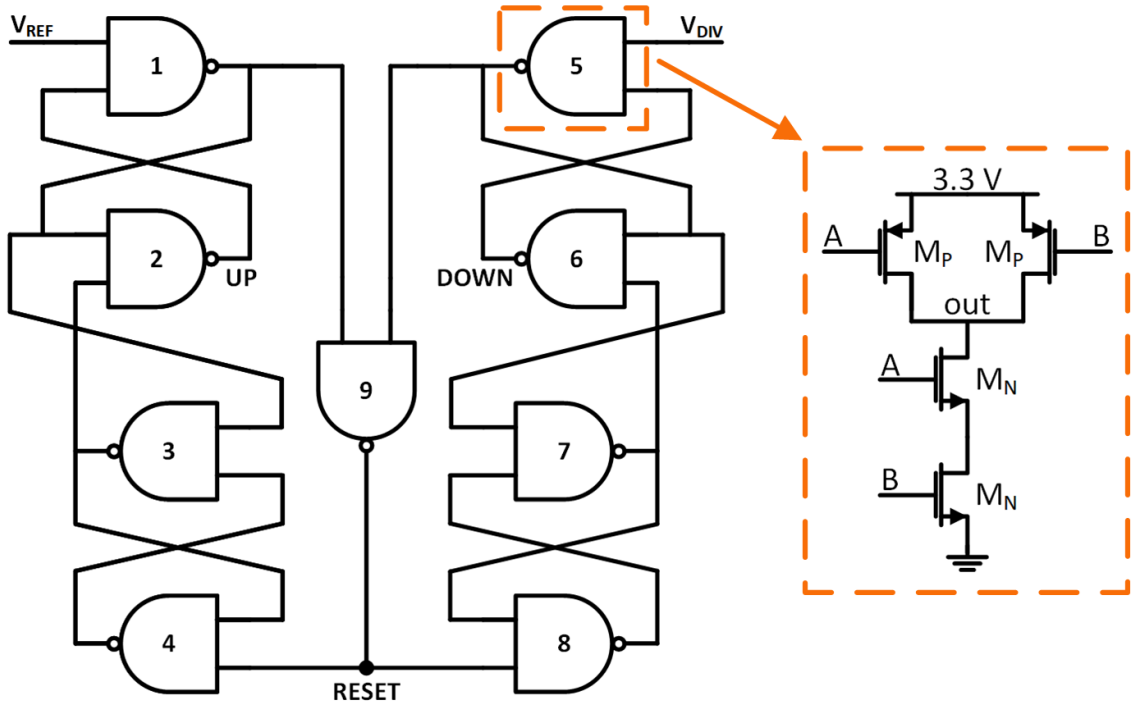


Figure 3.10: Schematic view of NAND based PFD topology.

Table 3.4: NAND based PFD component values.

Nmos		**Pmos**	
$\mathbf{W_{1,5}/L_{1,5}}$	3/0.33	$\mathbf{W_{1,5}/L_{1,5}}$	8/0.33
$\mathbf{W_{2,6}/L_{2,6}}$	5.5/0.33	$\mathbf{W_{2,6}/L_{2,6}}$	8.5/0.33
$\mathbf{W_{3,7}/L_{3,7}}$	6/0.33	$\mathbf{W_{3,7}/L_{3,7}}$	0.5/0.33
$\mathbf{W_{4,8}/L_{4,8}}$	2/0.33	$\mathbf{W_{4,8}/L_{4,8}}$	8/0.33
$\mathbf{W_{9}/L_{9}}$	2/0.33	$\mathbf{W_{9}/L_{9}}$	6/0.33

Each NAND logic gate is optimized for proper operation and phase noise. The larger the transistor width, the phase noise decreases. However, the effect of some blocks is minimal to phase noise; it is redundant to increase the device size of these. The minimum channel length is employed in the design procedure since increasing channel length translates to time constant increase, rise of path delay, and the phase noise [58]. The component values of the designed NAND based PFD are presented in Table.

The "dead zone" is the phase difference region in which the feedback mechanism of the PFD is not responding, behaves as an open-loop system. This problem is observable for a small phase difference case in which the reset signal is not wide enough to provide the time needed to activate the NAND gates. This issue results in undesirable phase variations in the PLL system, increasing the total phase noise. This small phase difference region, which results in the dead zone, decreases as the technology device size decreases. A solution to this issue is adding a delay to the reset path, such that the NAND gates will have the required time to be activated. Even number of inverters in this path will not affect the following parts of the system, the charge pump, and the loop filter, considering that the UP and DOWN are equal for the leading/lagging equivalent phase differences. A constant antibacklash delay of 1 nsec must be introduced for proper operation [59]. The transfer function of the PFD is simulated to verify that the dead zone is not present, Fig. 3.12. For this design, the device size of the NAND gate in the reset path provides the necessary constant delay to the circuit. The pulse width close to zero phase difference is approximately 3.98 nsec. The power consumption of the PFD block is 49 nW (14.84 nA * 3.3 V). The maximum average voltage value is 1.3 V since the Up and Down signals after the 2 inverters with of V_{cc1} of 2.6 V was employed, for proper operation of CP block.

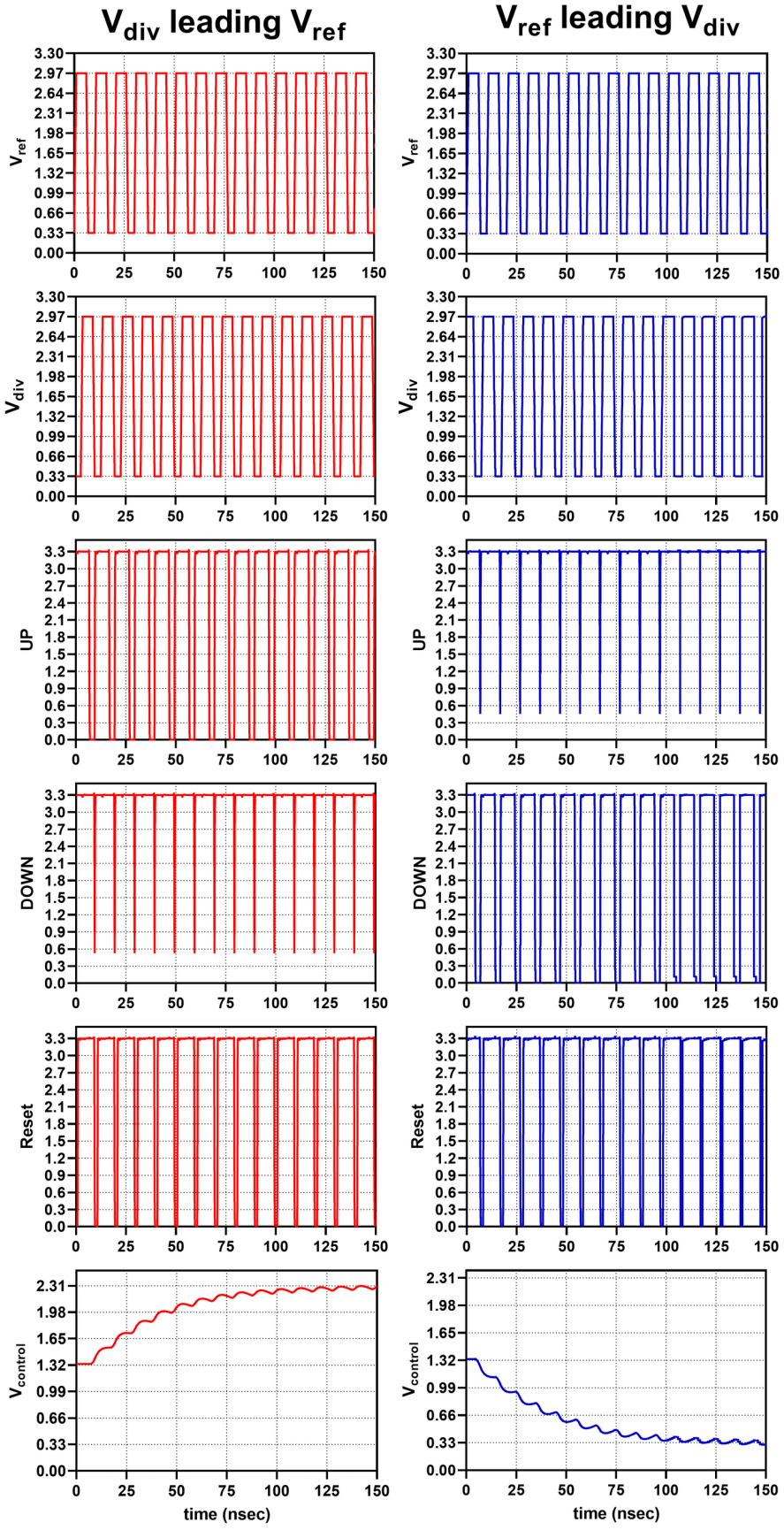


Figure 3.11: Behavioural signals of the PFD, CP, and LF.

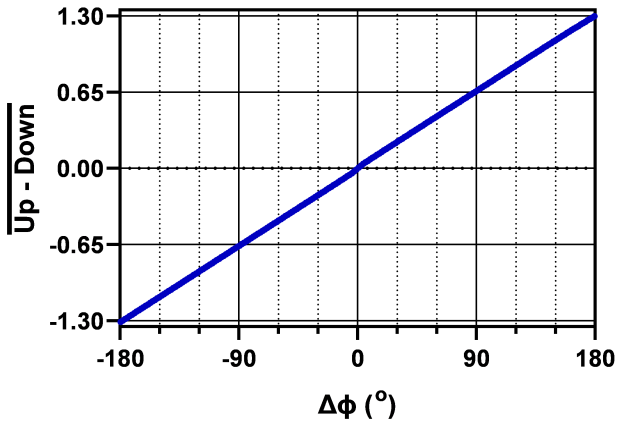


Figure 3.12: Behavioural transfer function of the PFD.

3.2.2 Charge Pump

The charge pump is an analog sub-block of the PLL system. This block translates the UP or DOWN voltage pulses to the incrementing or decrementing output current pulses whose magnitude is determined by the tail current of CP. In the conventional drain-switched CP, the UP signal controls the PMOS transistor, which charges the loop filter capacitor; and the DOWN signal controls the NMOS transistor, which discharges the loop filter capacitor. However, minimizing the current mismatch is a challenging task. For this purpose, the differential charge pump topology, as shown in Fig. 3.13, is employed. A NMOS differential pair is stacked with a PMOS one; the operational behaviour is the same as the previously mentioned topology. The differential inputs to the stacked transistors are generated through additional circuitry between the PFD and CP blocks. The UP signal is fed to an inverter and transmission gate to have the UP and UP' signals generated; the same circuitry is applied for the DOWN signal. Furthermore, a unity gain buffer is placed between the stacked pairs to minimize current mismatch. The current biased circuit uses the HBT transistors to reduce the effects of flicker noise [60].

The current mismatch will lead to asymmetric up and down currents for opposite phase differences of input signals and jitter. However, the current mismatch can be tolerated for diminutive values. The decoupling capacitors in the biasing nodes of the M3 and Q1 transistors obstruct instantaneous changes in the voltage values. Providing steady bias voltages to these transistors will reduce variances in currents and so current mismatch. The current mismatch, observed for values close to zero phase difference of the input signals in the PFD block, is 0.75%.

The system is locked for the zero phase difference of the input signals, such that no net up and down currents are generated to retain the control voltage constant.

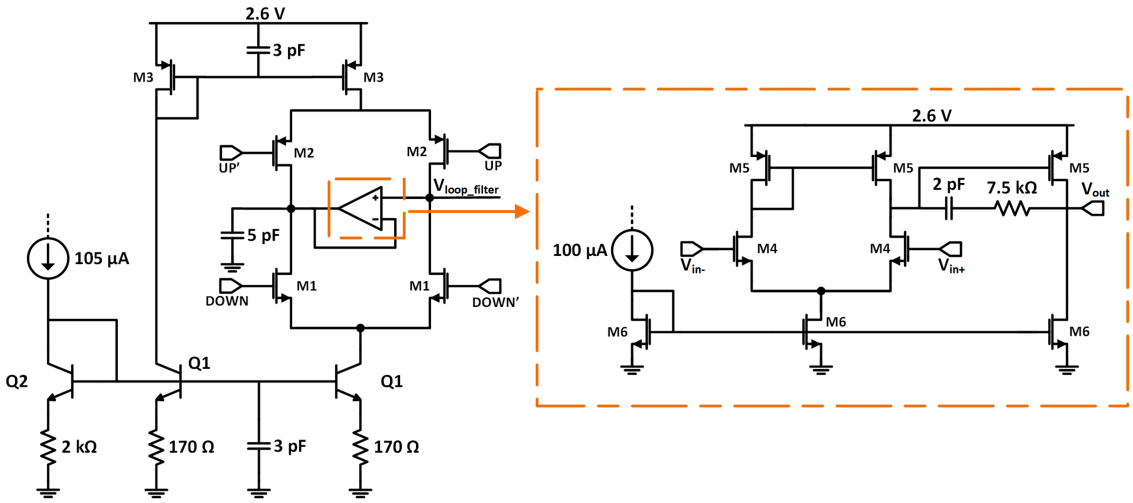


Figure 3.13: Schematic view of differential charge pump and unity gain buffer topology.

Table 3.5: Differential charge pump and unity gain buffer component values.

Charge Pump			
Q1	3x0.48µm	**Unity Gain Buffer**	
Q2	1x0.48µm	$\mathbf{W_4/L_4}$	20/0.8
$\mathbf{W_1/L_1}$	17/0.4	$\mathbf{W_5/L_5}$	26/0.8
$\mathbf{W_2/L_2}$	35/0.4	$\mathbf{W_6/L_6}$	15/2
$\mathbf{W_3/L_3}$	70/0.4		

However, if the system is locked when current mismatches occur, some charge will be applied to the capacitor of the loop filter, resulting in phase offset. The phase offset, phase difference of input signals at which the control voltage is constant, is 19.12 psec, 0.1912% shifted, which will not deprive performance metrics if kept small in value. The CP tail current is set to 1 mA considering the bandwidth and stability metrics of the open-loop system. The supply voltage is chosen as 2.6 V, such that the control voltage range will be 0.3 – 2.3 V since the varactor employed in the oscillator is in linear region. The total power consumption of the CP and unity gain buffer is 6.71 mW [(6. 035 n + 2.583 m) * 2.6]

As shown in Fig. 3.13, the unity gain buffer aims to reduce the equalize the input and output voltages of the amplifier, such that the current mismatch percentage is reduced. The circuit is designed such that the slew rate is high enough for the output to follow up the input signal. The buffer must be stable such that it will not affect the CP circuit; the phase margin is simulated to be 66°. The series capacitor and resistor are placed between the input of second stage and the output, to capacitor will increase stability, however it will decrease slew rate. This trade-off will be considered to find the optimal values for this capacitor and resistor. The

output voltage swing must be sufficient to be able to equalize the node voltages of the stacked transistors. The conventional design steps were followed for this block.

3.2.3 Loop Filter

The loop filter is responsible for converting the repetitive up and down current pulses, high-frequency components, generated by the CP to a steady voltage that will control the frequency of the oscillator. The loop filter aims to smoothen down abrupt ripples of the control voltage such that large voltage swings are avoided as an input for the oscillator. Furthermore, the loop filter has a strong influence on the loop dynamics of the PLL system. This filter has a low pass filter characteristic transfer function; its cut-off frequency corresponds to the loop bandwidth of the system [8]. The loop bandwidth significantly impacts phase noise, switching speed, and spurs of PLL.

The number of poles determines the order of the loop filter. The typical second-order loop filter consists of a shunt capacitor and shunt of a series capacitor and resistor. The shunt capacitor gets rid of the ripples in the control voltage. However, this capacitor will deprive the stability of the system [61]. The series capacitor and resistor provide the zero to stabilize the system. The third-order pole is preferred for this design to suppress the high-frequency offset spurs.

The transfer function of the loop filter is defined as the output control voltage divided by the charge pump current, (3.2.1) - (3.2.5) [8]. The following equations are provided to calculate the zero and poles. Due to the complexity of equations for the calculation of loop bandwidth and stability, Mathworks SIMULINK is used to define the numeric values of the loop filter.

$$Z(s) = \frac{1 + s \cdot T2}{s \cdot A0 + s^2 \cdot A1 + s^3 \cdot A2} \tag{3.2.1}$$

$$T2 = R2 \cdot C2 \tag{3.2.2}$$

$$A0 = C1 + C2 + C3 \tag{3.2.3}$$

$$A1 = C2 \cdot R2 \cdot (C1 + C3) + C3 \cdot R3 \cdot (C1 + C2) \tag{3.2.4}$$

$$A2 = C1 \cdot C2 \cdot C3 \cdot R2 \cdot R3 \tag{3.2.5}$$

The resistor, R2, is placed above the capacitor, C2, even though ideally, the order of the RC does not affect the transfer function or transient response. The configuration of the capacitor being on top of the resistor has not been preferred

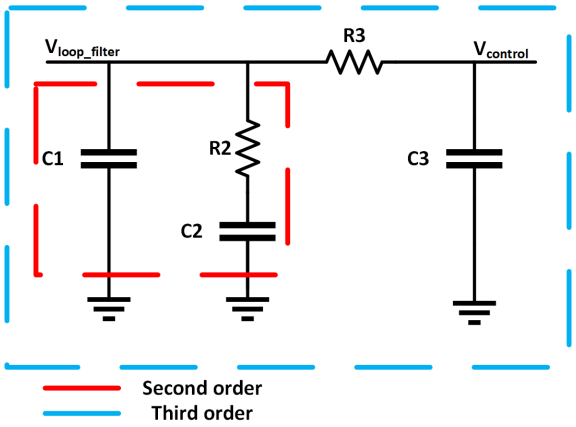


Figure 3.14: Schematic view of second and third order loop filter topology.

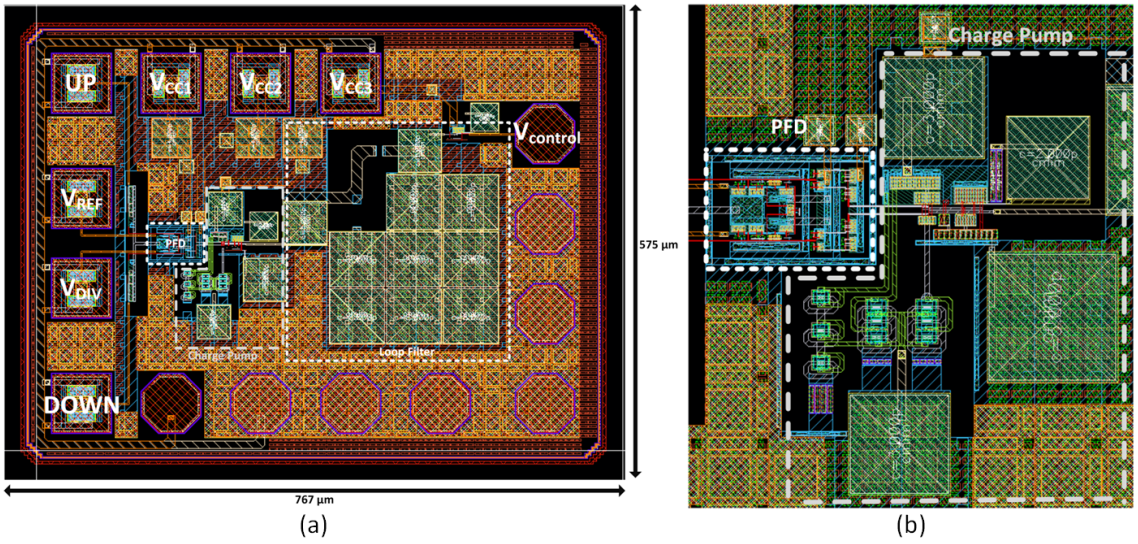


Figure 3.15: (a) Layout view of PFD, CP, and LF; (b) the close-up layout view of PFD and CP.

since the bottom plate of the capacitor will create an additional high-frequency pole. The order employed, shown in Fig. 3.14, has the disadvantage that the control voltage amplitude will affect the increased variation of switch resistance. Still, it is tolerable compared to the other configuration. The component values of the C1, C2, C3, R2, R3 are 5 pF, 64 pF, 5 pF, 5 kΩ, and 1 kΩ, respectively.

The layout view of the PFD, CP, and LF is shown in Fig. 3.15 (a) The V_{REF} and V_{DIV} are the input pads, V_{CC1} is the digital supply of 3.3 V, V_{CC2} is the digital supply of 2.6 V, and V_{CC3} is the analog supply of 2.6 V. The UP and DOWN signals are output pads to investigate the proper operation of PFD block. The $V_{control}$ pad is the output signal of the LF. After the LF a similar amplifier to the one used in CP was employed to drive the load. In Fig. 3.15 (b), a close-up view of PFD and CP blocks is depicted.

3.2.4 Wire bond effects to the transient response of the PFD & CP & LF

The effects of packaging on the PFD & CP & LF circuitry are scrutinized in simulations to ensure deviations do not occur. Different cases were analyzed as shown in Fig. 3.16. The inductance added to the ground due to the wire bond packaging created excessive bouncing to the ground voltage and disturbed the circuitry's operation. A shunt capacitor is placed on the ground wire bond to eliminate any issues during measurement, as shown in Fig. 3.16 (b). Two different configurations were analyzed to ensure operations in estimated, 1 nH, and excessive, 5 nH wire bond inductance added, Fig. 3.16 (b) and Fig. 3.16 (c). To analyse the effects of the restrained bouncings in voltage supplies, shunt capacitors were added to the respective wire bonds, as shown in Fig. 3.16 (d) and Fig. 3.16 (e).

The average and standard deviation in the voltage supplies are provided in Table 3.6 - 3.8, for different phase differences between the input signals. Each case defined in the tables corresponds to the alphabetic ordering done in Fig. 3.16. A magnitude of order decrease in deviation is observed when the shunt capacitors are added to the voltage supplies. Since the deviations without shunt capacitors are at an acceptable level, there is no need for complicating the board fabrication. Moreover, the average standard deviation is calculated for phase differences of input signals from -10 nsec to 10 nsec in Table 3.8.

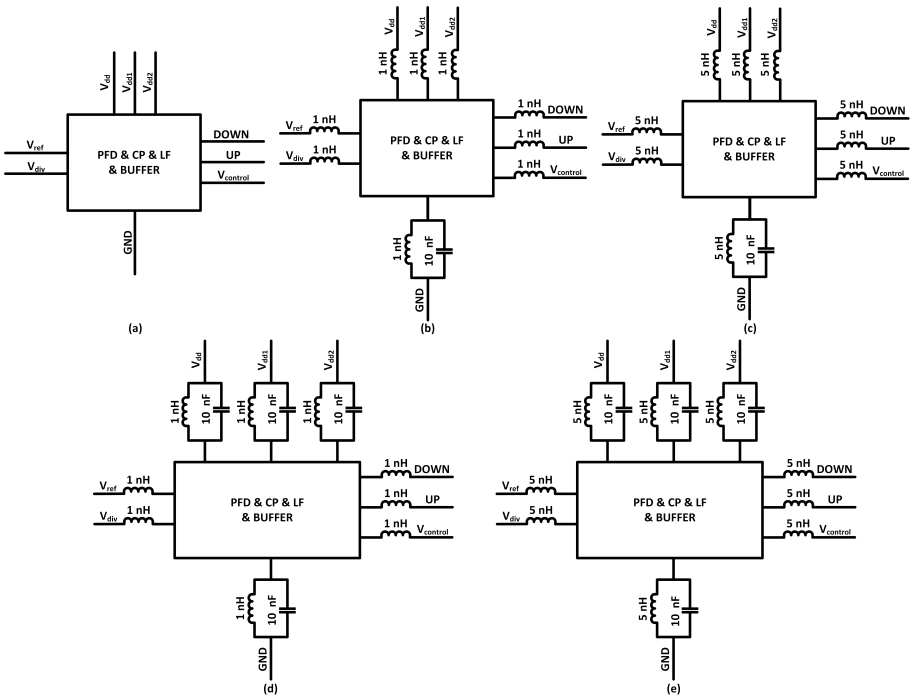


Figure 3.16: Different wire bond configurations simulated.

Table 3.6: Standard deviation in the voltage supplies for reference leading feedback signal for 2.5 nsec.

		Vdd	**Vdd_1**	**Vdd_2**	**GND**
	AVG (V)	3.3	2.6	2.6	-1.272p
Case (b)	**SD (V)**	61.23m	7.618m	3.906m	7.955p
Case (c)		174.6m	35.7m	9.213m	7.573p
Case (d)		5.764u	923.8n	1.957u	1.852p
Case (e)		5.44u	910n	1.023u	4.988p

Table 3.7: Standard deviation in the voltage supplies for reference lagging feedback signal for 2.5 nsec.

		Vdd	**Vdd_1**	**Vdd_2**	**GND**
	AVG (V)	3.3	2.6	2.6	-1.272p
Case (b)	**SD (V)**	60.75m	9.002m	3.1m	3.606p
Case (c)		237.8m	44.2m	8.262m	5.076p
Case (d)		7.63u	736.9n	2.525u	3.819p
Case (e)		7.08u	691.9n	2.808u	2.599p

Table 3.8: Standard deviation in the voltage supplies for delay sweep from -10 nsec to 10 nsec with 100 steps.

		Vdd	**Vdd_1**	**Vdd_2**	**GND**
	AVG (V)	3.3	2.6	2.6	-1.272p
Case (b)	**SD (V)**	61.22m	8.245m	4.293m	5.049p
Case (c)		204.9m	38.78m	10.13m	5.658p
Case (d)		6.573u	808.6n	1.924u	4.195p
Case (e)		6.193u	791.8n	1.758u	4.16p

In Fig. 3.17 the transient simulation results are depicted for the circuitry without wire bonds and wire bonds, cases depicted in Fig. 3.16 (a) and Fig. 3.16 (b) respectively. The bounces in the voltage supplies are observable during the rising and falling edges of the UP and DOWN signals. The bounces in the UP, DOWN, and $V_{control}$ signals are minimal and do not affect the operation of the circuitry.

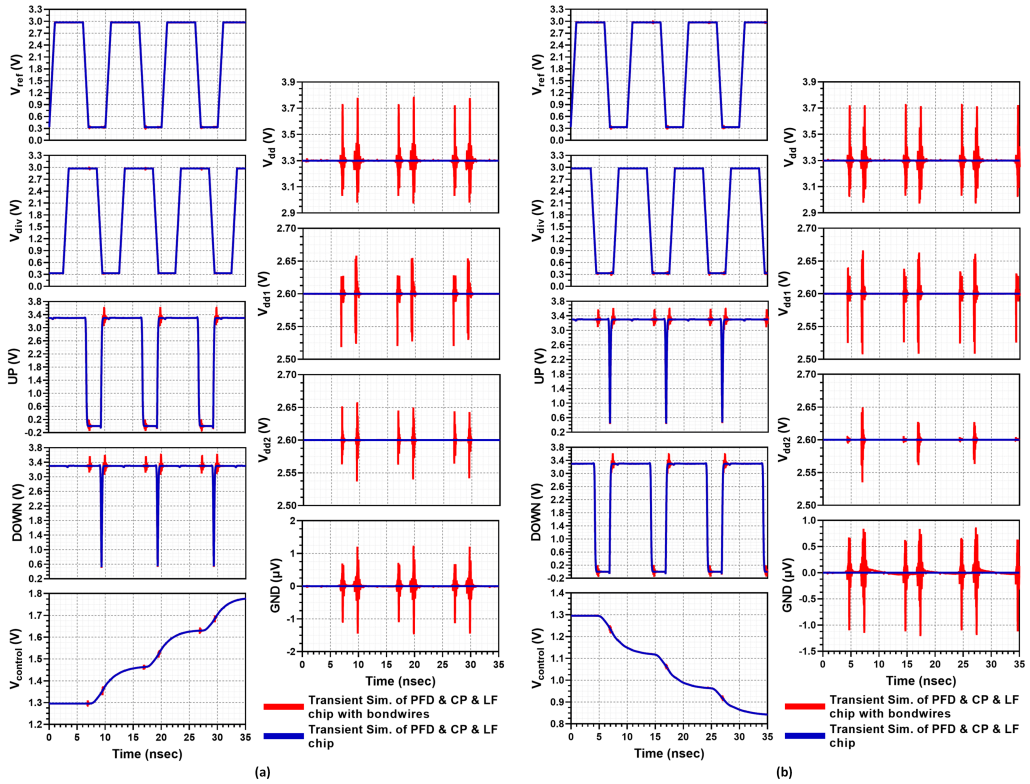


Figure 3.17: Transient Simulation of the PFD & CP & LF (a) for reference leading feedback signal for 2.5 nsec and (b) for reference lagging feedback signal for 2.5 nsec.

3.2.5 Wire bond effects to noise of the PFD & CP & LF

The effects of the wire bonds to the output noise of the PFD & CP & LF is scrutined as done for the transient operation previously. It is observed that the output noise decreases from 4.4275 pA/Hz to 4.4271 pA/Hz when the wire bonds are added to the simulation, as shown in Table 3.9. The output noise was simulated for different phase differences, however in the pA/Hz unit drastic changes in the plots was not observed, as shown in Fig. 3.18 (a). To be able to observe the difference between the output noise without and with wire bond, the output noise is plotted in dBV/Hz unit. Parametric sweep of the phase difference between the two input signals was conducted, to determine the highest, average and lowest output noise values in dBV/Hz, as shown in Fig. 3.18 (b). The lowest and average output noise cases show very close values for without and with wire bonds. The decrease in output noise is observed in the highest output noise case when wire bonds are added. Moreover, adding shunt capacitors to the supply voltages does not affect the output noise, so a board fabrication complexity increase is not needed, as shown in Table 3.9.

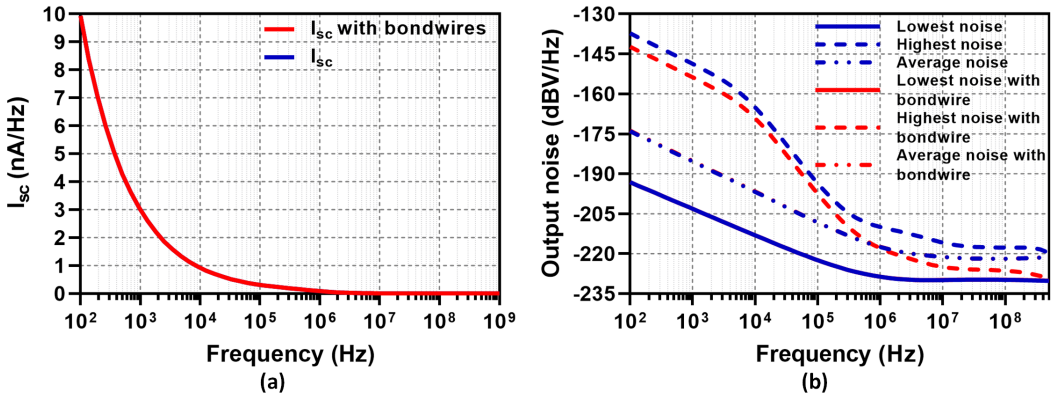


Figure 3.18: Output noise in nA/Hz and dBV/Hz units.

Table 3.9: Output noise values at 100 MHz for different wire bond configurations.

	Highest (dBV/Hz)	Average (dBV/Hz)	Lowest (dBV/Hz)	Short circuit current (pA/Hz)
Case (a)	-217.7	-221.89	-229.81	4.4275
Case (b)	-221.88	-228.16	-229.84	4.4271
Case (c)	-218.91	-221.84	-229.85	4.4253
Case (d)	-218.02	-221.9	-229.85	4.4271
Case (e)	-217.76	-221.91	-229.84	4.4252

3.2.6 Voltage Controlled Oscillator

The LO signal is generated through the oscillator, without any input signal. Any LC tank will oscillate, however due to the resistance of the inductor, it will fade away. To maintain the oscillation, the LC tank needs negative feedback. The proposed VCO schematic is shown in Fig. 3.19. The negative resistance is provided through the cross couple circuit with negative transconductance. The fine frequency tuning is done by the CMOS varactor, which was designed with gate-oxide provided by the technology. The coarse frequency tuning is done through a capacitor with discrete control implemented. The control voltages of the varactor and switches of the capacitor bank are applied externally. A balun is employed to convert the differential VCO output to a single-ended. In this way, higher output power, and higher even harmonic suppression, which decreases PN values is achieved.

The thermal noise at second harmonics of the current source transistors are depriving phase noise values [62]. A high impedance is placed at the emitter of the Q1 transistors to minimize noises, which is enabled through the C_{tail} and L_{tail} resonating at $2f_{osc}$. The noise from the current source is eliminated and ground to the L_{tail} is provided through the C_{large}.

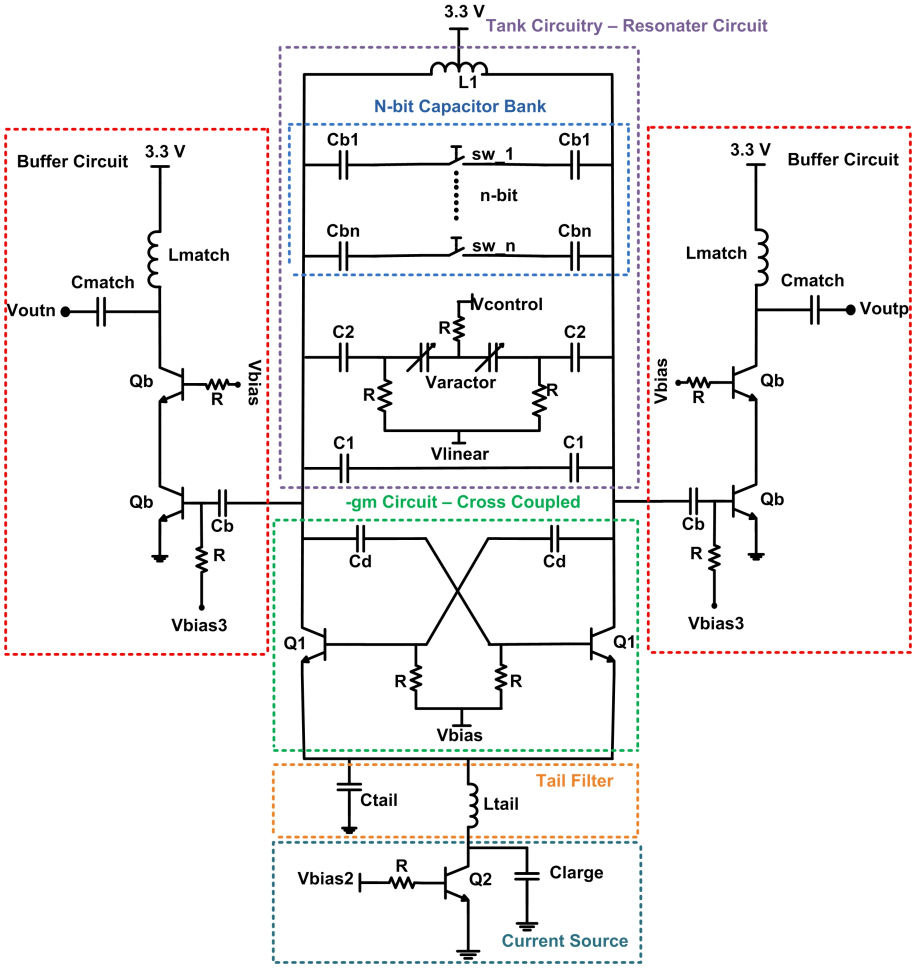


Figure 3.19: Schematic view of the proposed VCO.

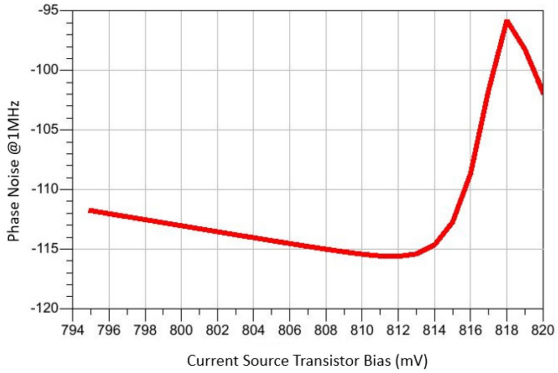


Figure 3.20: PN vs. Current Source Bias

The trade-off between phase noise and power consumption determined the current source value. In Fig. 3.20 the phase noise versus the bias voltage of the current source transistor is depicted. It is biased for maximum phase noise and power consumption of 25 mW. I would like to thank Kaan Veziroğlu for his contributions to this block.

3.2.7 Divider

The high frequency (GHz range) VCO output is divided by the reference frequency crystal oscillator input (MHz range) with minimum spacing through the divider block. This block can be implemented as a digital counter. However, the maximum input frequency is limited by the maximum operating frequency of the CMOS devices, which is 3-4 GHz. Another technique is in the analog domain, which can be implemented through a master-slave (MS) latch divider and injection-locking divider (ILD). The ILD topology was not considered due to its high power consumption. The multi-modulus frequency divider (MMDs) is established upon MS latch dividers.

The MMD topology is shown in Fig. 3.21, which contains n 2/3 divide cells [63]. The C[n] activates the respective cell; with a high voltage value divide by 3 operation is done, and with a low voltage value divide by 2 operation is done. The VCO output frequency range is from 9 GHz to 12 GHz, so the divider must consist of 5 2/3 divide cells. The block diagram of a 2/3 cell is shown in Fig. 3.22 (a). The sub-blocks A and B are depicted in Fig. 3.22 (b) and 3.22 (c) respectively. The sub-block A is buffered to be able to drive the clock of the following stage. The sub-block B is buffered according to the speed and loading of the next block. The fan-out and speed requirements of each stage determine the values of the R_L, R_E, and tail current. The layout of the divider is shown in Fig. 3.23. The area occupied by the divider is 1.084 mm2.

The simulation result of the 9.5 GHz input to the divider results to 99.07 MHz output is shown in Fig. 3.24. The absolute difference between the output frequency of the divider with the input reference frequency is shown in Fig. 3.25. The minimum and maximum values are 930 kHz and14.66 MHz, respectively. The PFD can tolerate frequency differences until 20 MHz with locking condition guaranteed. I would like to thank Cerin Ninan Kunnatharayil for his contributions to this block.

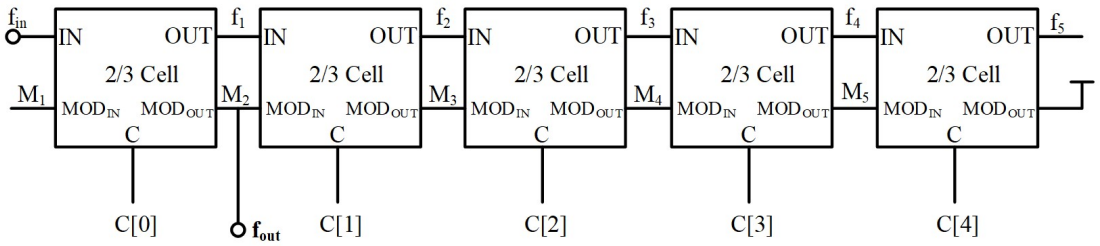


Figure 3.21: A chain of 5 divide by 2/3 cells.

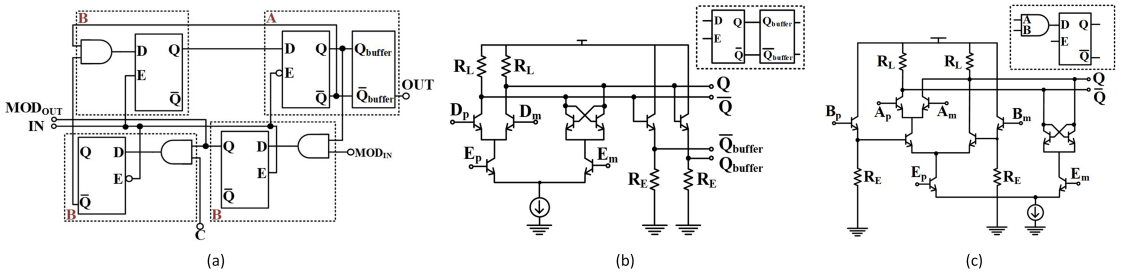


Figure 3.22: (a) Block diagram of a 2/3 divider cell; (b) Schematic of latch designated as A (c) Schematic of latch and AND gate designated as B.

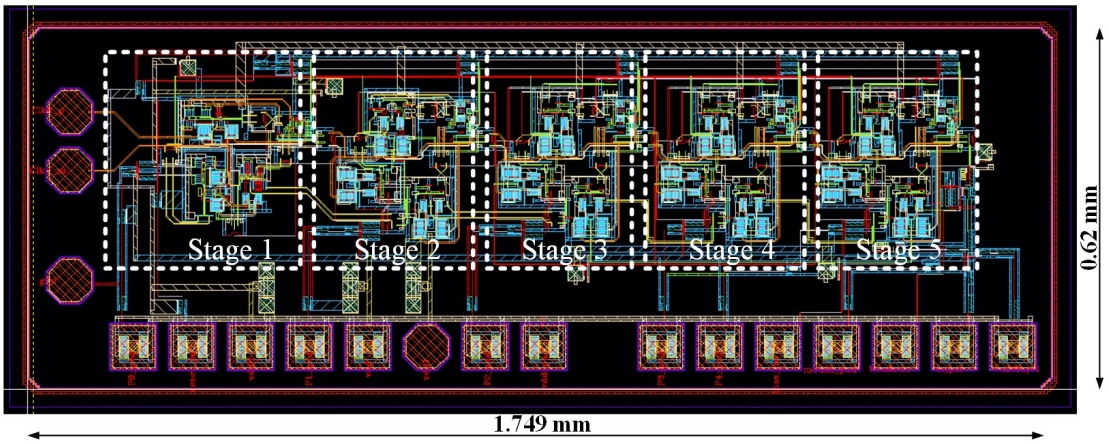


Figure 3.23: Layout view of the divider.

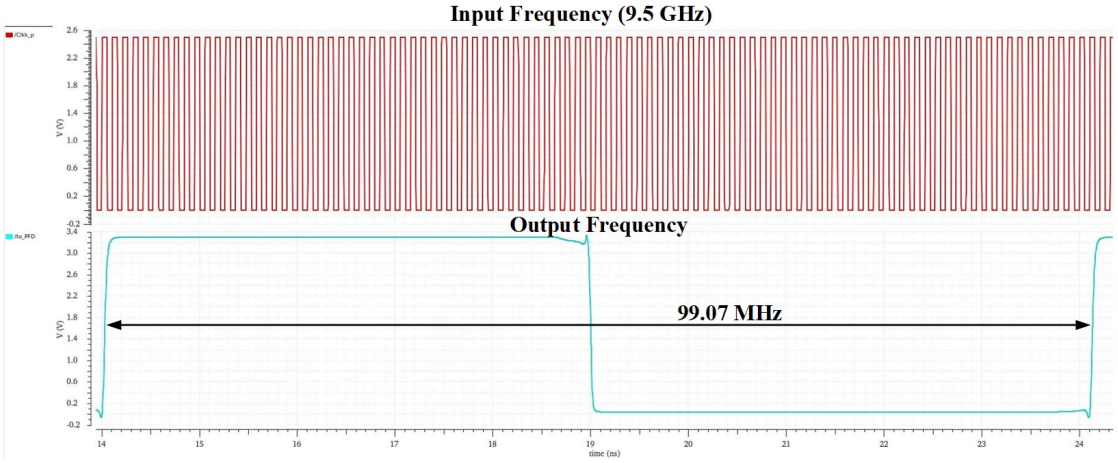


Figure 3.24: Simulation waveform when 9.5 GHz is the input frequency to the divider.

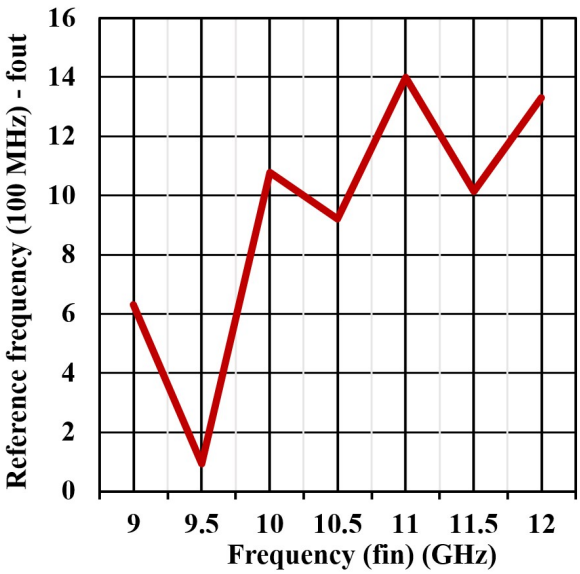


Figure 3.25: Compares the absolute value of the difference between the reference frequency (i.e. 100 MHz) and the output frequency.

3.2.8 Frequency Synthesizer

For the system level simulations Mathworks Simulink was used. Employing already existing PLL blocks, initially according to the predefined the loop bandwidth, phase margin, charge pump current, oscillator voltage sensitivity and phase noise; the loop filter parameters were calculated. The component values of the loop filter were updated for area optimization and transient response optimization. The open and closed loop response of the PLL system has been reported as shown in Fig. 3.26 - 3.27, for locking frequency of 10.7 GHz. The simulations were repeated for the corner frequencies of 9.1 GHz and 11.9 GHz, shown in Table 3.10. The Fig. 3.28 depicts idealistic results for the phase noise, even though impurities such as rise/fall time and propagation delay of PFD, current imbalance and leakage current of charge pump were implemented to the simulation model. The phase noise simulations were scrutinized in ADS environment, in which including the output noise current of the PFD, CP and LF, 3.86 pA/Hz, which was simulated in Cadence was included to the simulation model, as well as the phase noise levels of VCO for different frequency offsets were added. The phase noise simulation result is depicted in Fig. 3.29, the phase noise is -108.7 dBc/Hz @ 1MHz offset.

As stated above the loop bandwidth, phase margin, and settling time has been simulated using MATLAB/Simulink. The phase noise analysis has been conducted in ADS environment. For a better comprehension of the effects of these parameters to the phase noise different cases were scrutinized.

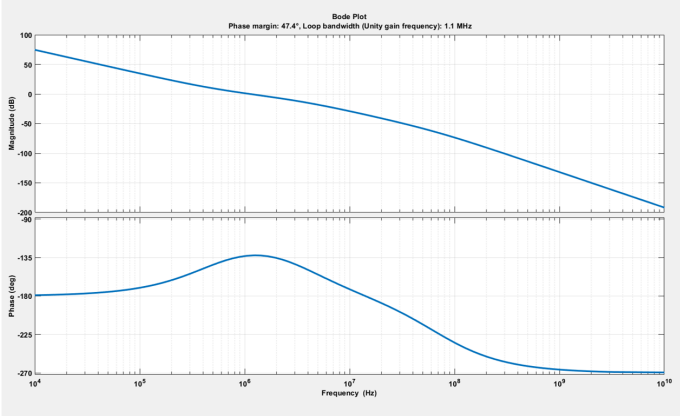


Figure 3.26: Simulated bode plot of PLL open-loop transfer function.

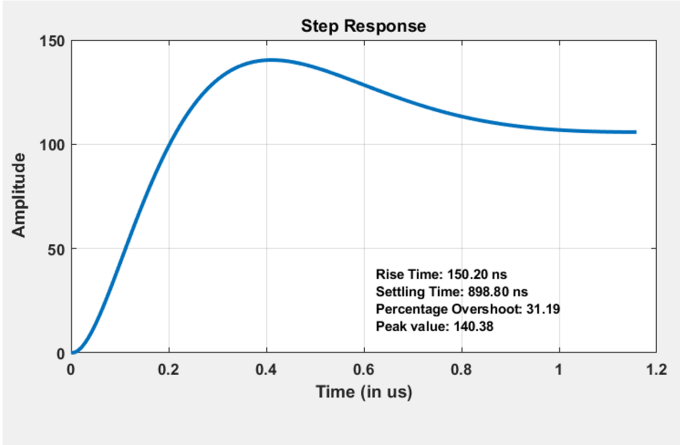


Figure 3.27: Simulated step response of close-loop PLL.

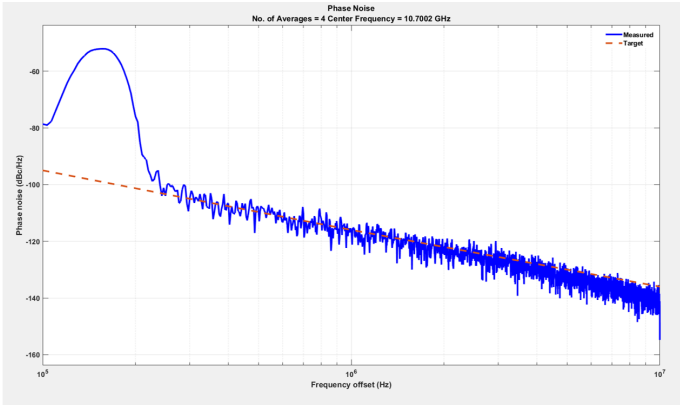


Figure 3.28: MATLAB simulated phase noise of PLL.

Table 3.10: Loop Bandwidth, phase margin and settling time simulation results.

Locking Freq. (GHz)	**Loop Bandwidth (MHz)**	**Phase Margin (°)**	**Settling Time (nsec)**
9.1	1.3	47.6	826.09
10.7	1.1	47.4	898.8
11.9	1	47	951.45
Mean	1.13	47.3	892.11

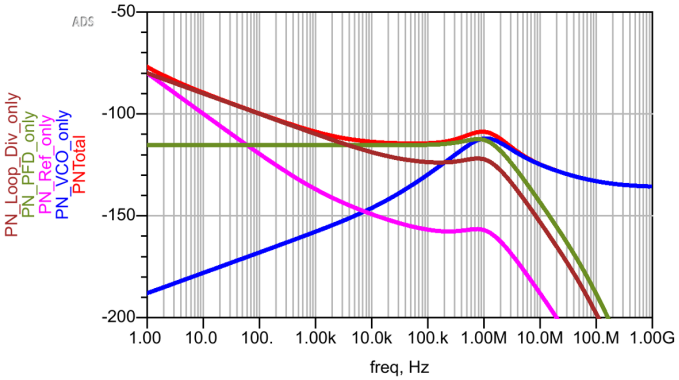


Figure 3.29: ADS simulated phase noise of PLL.

Initially the effect of the current noise of the PFD, CP, and LF blocks to the system was scrutinized. The simulated current noise is 3.86 pA, and the phase noise at 1 MHz is -108.709 dBc/Hz. If the current noise was dropped to 1 pA, while keeping all the other parameters constant was possible, the phase noise will be -110.753 dBc/Hz, a 2 dBc/Hz approximately improvement. For the current noise of 0.1 pA, the phase noise is -110.943 dBc/Hz. Subsequently keeping in mind that the challenge of reducing the current noise of the PFD, CP, and LF by a factor of 4 for a 2 dBc/Hz improvement in phase noise. Moreover, it is not known if this reduction in current noise can be observed in a new design due to technology limitations.

Another parameter that has an effect to the system behavior is the CP current. Increasing the CP current from 1 mA to 2 mA, the phase noise drops from -104.768 dBc/Hz to -106.89 dBc/Hz for an ideal loop filter designed by the MATLAB/Simulink (not optimized for transient behavior). Similarly for a CP current of 3.86 mA, the simulated phase noise is -110.341 dBc/Hz. The loop bandwidth is 1 MHz, the phase margin is 46.3°, the current noise of PFD, CP, and LF is considered as 5 pA.

A PLL system with a wide loop bandwidth exhibits a lower phase noise, faster settling time and smaller capacitor size for LF, however, the stability and spur rejection of the system will be degraded. Increasing the loop bandwidth from 1 MHz to 4 MHz, enhances the phase noise by 7 dBc/Hz approximately, for current noise of PFD, CP, and LF of 3.86 pA, CP current of 1 mA, phase margin of 46.3°, and for an ideal loop filter designed by the MATLAB/Simulink (not optimized for transient behavior). Considering the stability issues that can be observed, the loop filter can be designed with wider loop bandwidth and higher phase margin. The case of 59.7° phase margin is studied, the phase noise ± 1 dBc/Hz. However, the capacitor size is increased by 1.5 factor approximately for an ideal loop filter designed by the MATLAB/Simulink (not optimized for transient behavior).

Table 3.11: Possible optimization cases of the behavioral model of the PLL.

Current noise (pA)	**I_{CP} (mA)**	**Loop Bandwidth (MHz)**	**Phase Margin (°)**	**Settling time (nsec)**	**Phase noise (dBc/Hz @ 1 MHz)**	**Loop Filter transient behavior**	**C2 (pF)**
3.86	1	1.1	47	898.8	-108.709	optimized	64
1	1	1.1	47	898.8	-110.753	optimized	64
0.1	1	1.1	47	898.8	-110.943	optimized	64
3.86	1	1	46.3	1060	-104.768	unoptimized	115
3.86	2	1	46.3	1060	-106.89	unoptimized	230
3.86	5	1	46.3	1060	-110.341	unoptimized	575
3.86	1	4	46.3	266.04	-112.241	unoptimized	7.19
3.86	2	4	46.3	266.17	-116.365	unoptimized	14.4
3.86	5	4	46.3	266.63	-119.845	unoptimized	35.9
3.86	2	4	59.7	388.11	-115.338	unoptimized	21.8
3.86	5	4	59.7	387.66	-118.689	unoptimized	54.4

Table 3.12: Comparison of the presented frequency synthesizers with similar works in the literature.

	Frequency (GHz)	**Phase Noise (dBc/Hz @ 1 MHz)**	**TR (%)**	**P_{DC} (mW)**	**f_{REF} (MHz)**	**Area (mm^2)**	**Technology (nm)**	**FoM**
[64]	20.6-48.2*	-108	80.2	148	100	2.1	65 CMOS	195.1
[65]	24.6-27.8	-107	12.2	56.7	1750	1.34	180 SiGe	179.1
[66]	20.5-24.9*	-116	19.2	115	155.52	1.23**	120 SiGe	188.2
[67]	21.4-25.1	-103	15.9	64	390	0.1	40 LP CMOS	176.3
[68]	25-30	-107	18	87	-	1.8	65 CMOS	181.5
This work	18-24*	-108.709	15.88	150	100	4.67	130 SiGe	177.4

*Frequency multiplication necessary; **External loop filter; $FoM = -L(\Delta\omega) + 20log(\frac{f}{\Delta f}) - 10log(\frac{P_{DC}}{1mW}) + 20log(\frac{TR}{10})$

In Table 3.11 the above-mentioned cases are shown, since the LF area is dominated by the one of the C2 capacitor, this LF component is underlined only. It can be concluded that increasing the loop bandwidth the phase noise drops, while keeping the same PFD and CP design. The advantage is that area and settling time will decrease, the disadvantage is that stability and spur rejection can be an issue. Increasing the CP current, enhances the phase noise, but the capacitor area is increased drastically. The same enhancement in phase noise is observed for increasing the loop bandwidth, while capacitor area decreases. To ensure that stability will not be an issue, loop filter was designed for phase margin of 59.7°. The phase noise has a ± 1 dBc/Hz change compared to the 46.3° phase margin, and the capacitor area has been increased 1.5 times approximately.

3.3 Measurement Results

3.3.1 PFD & CP & LF

The fabricated die of the PFD & CP & LF is shown in Fig. 3.30 (a). Considering the wire bond effects the shunt capacitor is added to the ground of the package, as shown in Fig. 3.30 (b).

The measurement setup is depicted in Fig. 3.31. The square pulses of V_{REF} and V_{DIV} are generated through the "Agilent Technologies 81160A Pulse Function Arbitrary Generator". The DC $V_{control}$ voltage is observed through the "Agilent Technologies DSO-X 3012A Digital Storage Oscilloscope". The digital UP and DOWN signals are read through the "Agilent Technologies DSO9254A Digital Storage Oscilloscope".

The rising and falling of the $V_{control}$ signal was not able to be captured during the measurements since it takes 100 nsec to reach maximum or minimum voltage in simulations. The reference leading feedback the $V_{control}$ reaches 2.4 V, and the reference lagging the feedback the $V_{control}$ reaches 70 mV as shown in Fig. 3.32. Another problem encountered is that the "81160A Pulse Function Arbitrary Generator" was not able to generate perfect square waveforms at 100 MHz, resulting to hard to capture UP and DOWN signals.

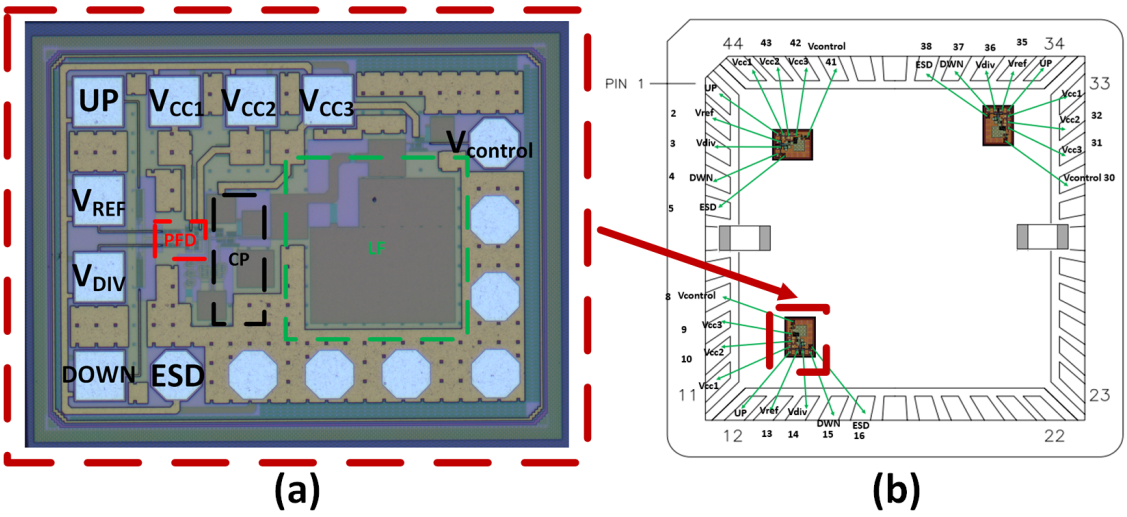


Figure 3.30: (a) Picture of the PFD & CP & LF die and (b) wire bond configuration in the package.

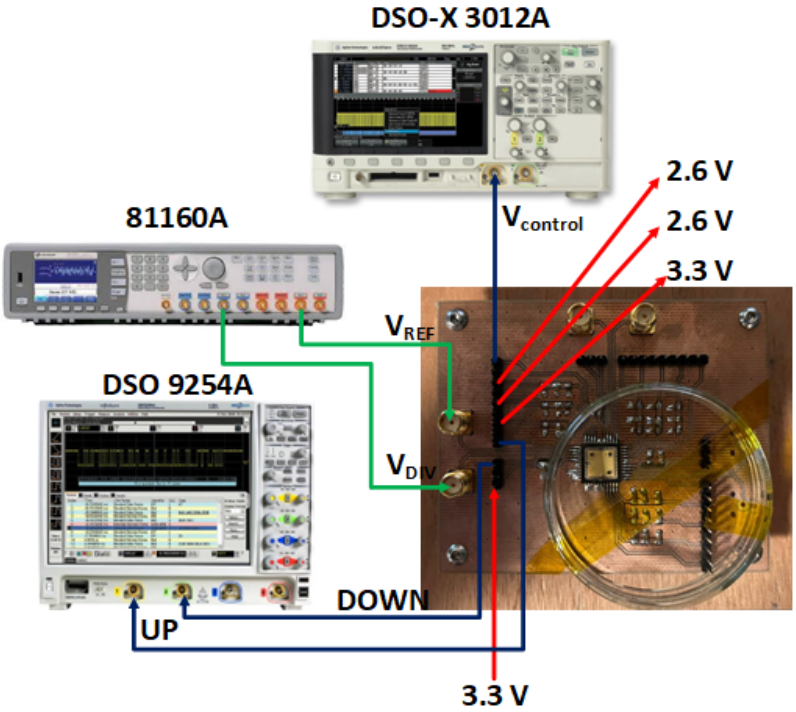


Figure 3.31: Measurement setup of the PFD & CP & LF.

Figure 3.32: Measurement of $V_{control}$ (a) for reference leading feedback signal for 1.25 nsec and (b) for reference lagging feedback signal for 1.25 nsec.

3.3.2 Voltage Controlled Oscillator

The total die area is 2.3 mm^2, as shown in Fig. 3.33. Flip-chip packaging the technique has been employed, while the PCB substrate employed is Rogers Ro4350B. The measurement of the phase noise employed the "Phase Noise Personality" of the Agilent 4407b Spectrum analyzer. At the center frequency (10.276 GHz), the measured phase noise was -114.42 dBc/Hz @ 1 MHz offset, as shown in Fig. 3.34. The power consumption of the VCO and the buffers is 28.7 mW. The tuning range is 15.88 %, 9.46 GHz - 11.092 GHz. In Table 3.13, the measured VCO is compared

with similar works in the literature. The work in [69] has a lower phase noise, however, our proposed work has a larger TR and lower power consumption. The work in [70] has a higher phase noise than our proposed VCO. However, work in [70] has a larger TR and lower power consumption.

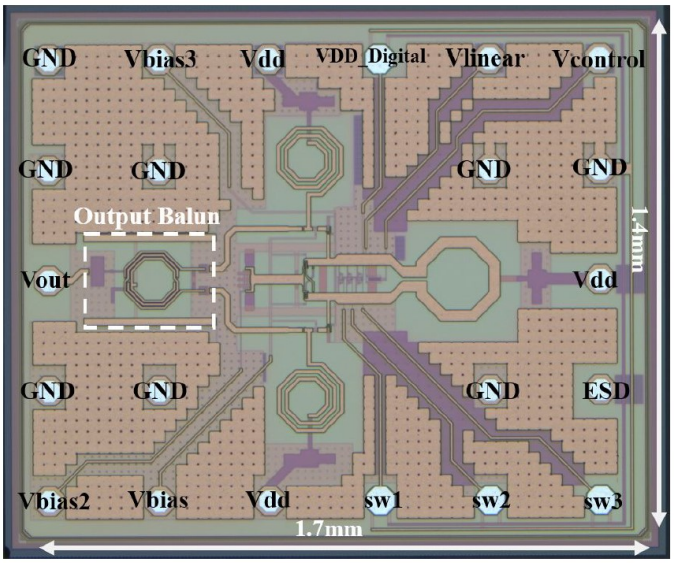


Figure 3.33: Picture of the VCO die.

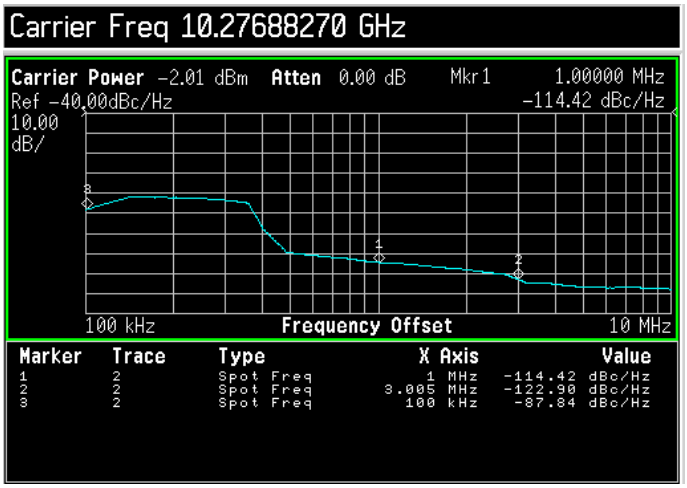


Figure 3.34: Phase Noise Measurement at Center Frequency @1MHz offset.

Table 3.13: Comparison of the presented VCO with similar works in the literature.

	Frequency (GHz)	Phase Noise (dBc/Hz @ 1 MHz)	TR (%)	PDC (mW)	Technology (nm)	FoM	FoMt
[69]	14.12	-120	8.9	233	250 SiGe	-178.95	-177.9
[71]	27.32	-99	30.2	45	130 SiGe	-172	-182
[72]	21.75	-108	17.4	60	350 SiGe	-176	-181
[73]	14.24	-97	9.1	123	250 SiGe	-179.3	-181.07
[70]	17.5	-110.6	17.1	27.5	130 SiGe	-181.07	-185.75
This work	10.276	-114.42	15.88	28.7	130 SiGe	-180.1	-182.1

$FoM = -L(\Delta\omega) + 20log(\frac{f}{\Delta f}) - 10log(\frac{P_{DC}}{1mW})$, $FoMt = FoM + 10log\left(\frac{TR}{10}\right)$

4 Conclusion & Future Work

4.1 Summary of Work

The high demand for higher quality data transfer and user handling capability has pushed the industry to the mm-wave frequency range for the 5G applications. The performance requirements for conversion and local oscillator frequency generator are very high demanding and must be handled carefully.

The down-converter mixer is required to have high isolation to avoid couplings between the LO frequencies, high linearity to be able to handle high input powers, adequate conversion gain, low power consumption, and low area occupation. The proposed mixer achieves high isolation even though the input RF signal is applied as single-ended. The transconductance stage operates as the conventional transconductance stage of the double-balanced mixer and as an active balun. The RF leakages are prevented by employing a resonator at the emitter of the transconductance stage, such that the isolation values are equivalent to the ones of the double-balanced mixer. For 26 GHz, the conversion gain (CG) is -7.72 dB. The corresponding 1dB input compression point (IP_{1dB}) is 5.7 dBm. The RF-IF, LO-RF, and LO-IF isolations are above 35 dB, 45 dB, and 35 dB, respectively. The power consumption is 56 mW with a 3.3 V voltage supply, and the active area without the pads is 1 mm^2. The architecture of the frequency synthesizer has been chosen to be applicable for sliding IF transceivers. So, each transceiver will have its frequency synthesizer, which consists of a PLL, frequency doubler, and divider by two. The PLL block consists of a VCO, PFD, CP, LF, and integer-N divider. The VCO has a phase noise of -114 dBc/Hz, tuning range of 15.88 %, power consumption of 28.7 mW, and an area of 2.3 mm^2. The simulated phase noise of the closed loop PLL is -108.7 dBc/Hz.

4.2 Future Work

The high isolation and highly linear mixer had been measured. Furthermore, its optimized version area vise will be sent for fabrication. The measurements of the divider, open loop, and closed loop PLL system will be completed. Their die photographs are shown in Fig. 4.1 - 4.3. The design of the doubler and its performance verification will be completed. The frequency synthesizer can be assembled at the chip level. Initially, the frequency synthesizer will be tested stand-alone, and the latter can be incorporated with the down-converter and up-converter mixers at the board level for inspection of the receiver and transmitter blocks.

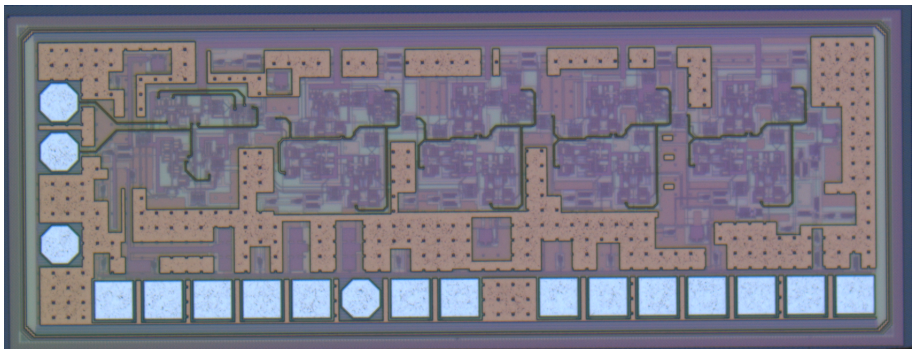


Figure 4.1: The die photograph of the divider.

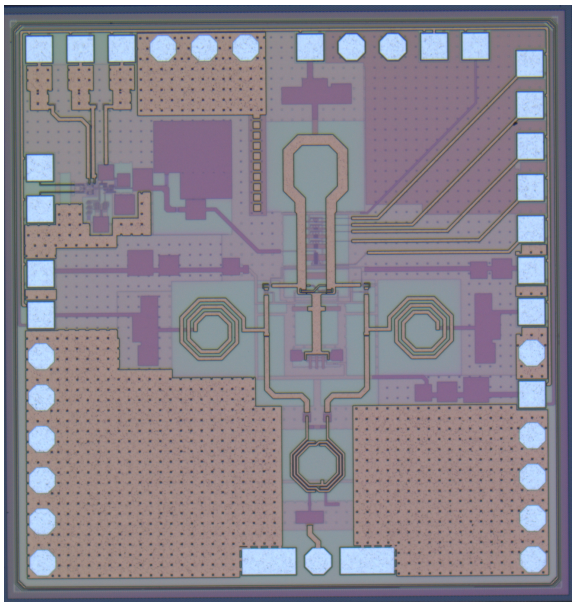


Figure 4.2: The die photograph of the open loop PLL.

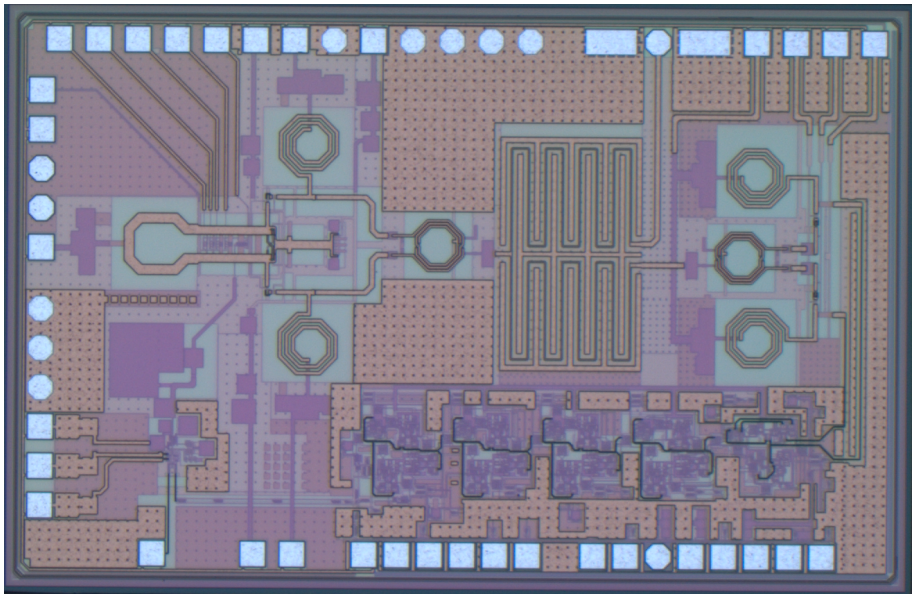


Figure 4.3: The die photograph of the closed loop PLL.

APPENDIX

A. Appendix

Isolations

RF-IF & LO-IF

The step-by-step derivation of RF and LO leakages to the output is provided below. The node voltages of V_x, V_y, V_z, V_{out+}, V_{out-} as provided in (4.2.3), (4.2.5), (4.2.7), (4.2.9), (4.2.11) respectively.

$$(V_{RF} - V_x)\left[gm_1 + j\omega C_{\pi 1} + \frac{1}{r_{\pi 1}}\right] - V_x\left[gm_2 + j\omega C_{\pi 2} + \frac{1}{r_{\pi 2}}\right] = 0 \tag{4.2.1}$$

$$V_{RF}Y_1 = V_x(Y_1 + Y_2)V_x = V_{RF}\frac{Y_1}{Y_1 + Y_2} \tag{4.2.2}$$

$$V_x = V_{RF}\frac{Y_1}{Y_1 + Y_2} \tag{4.2.3}$$

$$(V_{LO+} - V_y)\left[gm_3 + j\omega C_{\pi 3} + \frac{1}{r_{\pi 3}}\right] - (V_{LO-} - V_y)\left[gm_4 + j\omega C_{\pi 4} + \frac{1}{r_{\pi 4}}\right] = (V_{RF} - V_x)gm_1 + (V_y - V_{RF})j\omega C_{\mu 1} \tag{4.2.4}$$

$$V_y = \left[V_{LO+}Y_3 + V_{LO-}Y_4 - V_{RF}(gm_1 - j\omega C_{\mu 1}) + V_{RF}\frac{Y_1}{Y_1 + Y_2}gm_1\right]\frac{1}{Y_3 + Y_4 + j\omega C_{\mu 1}} \tag{4.2.5}$$

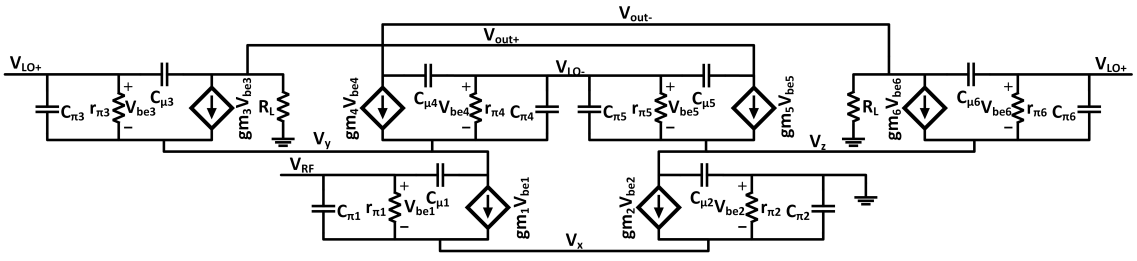


Figure 4.4: The small-signal model of the mixer.

$$(V_{LO-}-V_z)\left[gm_5+j\omega C_{\pi5}+\frac{1}{r_{\pi5}}\right]-(V_{LO+}-V_z)\left[gm_6+j\omega C_{\pi6}+\frac{1}{r_{\pi6}}\right]= (-V_x)gm_2+V_z j\omega C_{\mu2} \quad (4.2.6)$$

$$V_z=\left[V_{LO-}Y_5+V_{LO+}Y_6+V_{RF}\frac{Y_1}{Y_1+Y_2}gm_2\right]\frac{1}{Y_5+Y_6+j\omega C_{\mu2}} \quad (4.2.7)$$

$$gm_3(V_{LO+}-V_y)+gm_5(V_{LO-}-V_z)+\frac{V_{out+}}{R_L}=(V_{LO+}-V_{out+})j\omega C_{\mu3} + (V_{LO-}-V_{out+})j\omega C_{\mu5} \quad (4.2.8)$$

$$V_{out+}=-\Big[gm_3(V_{LO+}-V_y)+gm_5(V_{LO-}-V_z) - V_{LO+}j\omega C_{\mu3}-V_{LO-}j\omega C_{\mu5}\Big]\frac{1}{j\omega(C_{\mu3}+C_{\mu5})+\frac{1}{R_L}} \quad (4.2.9)$$

$$gm_4(V_{LO-}-V_y)+gm_6(V_{LO+}-V_z)+\frac{V_{out-}}{R_L}=(V_{LO-}-V_{out-})j\omega C_{\mu4} + (V_{LO+}-V_{out-})j\omega C_{\mu6} \quad (4.2.10)$$

$$V_{out-}=-\Big[gm_4(V_{LO-}-V_y)+gm_6(V_{LO+}-V_z) - V_{LO-}j\omega C_{\mu4}-V_{LO+}j\omega C_{\mu6}\Big]\frac{1}{j\omega(C_{\mu4}+C_{\mu6})+\frac{1}{R_L}} \quad (4.2.11)$$

$$V_{out+}-V_{out-}=\Big[V_{LO+}(gm_3-gm_3-2j\omega C_{\mu3})+V_{LO-}(gm_4-gm_4-2j\omega C_{\mu4}) - V_y(gm_4-gm_3)-V_z(gm_3-gm_4)\Big]\frac{1}{j\omega(C_{\mu3}+C_{\mu5})+\frac{1}{R_L}} \quad (4.2.12)$$

The denominators of V_{out+} and V_{out-} have been considered equal ($C_{\mu3}+C_{\mu5}=C_{\mu4}+C_{\mu6}$) due to the symmetry of the switching quad. As mentioned previously complete symmetry is not considered to show that the transconductance stage can cancel the RF leakages at the output even though the RF is fed as single-ended. The LO signals will cancel due to their differential nature and symmetry of the switching stage. The dominant effect on RF leakages which is the g_m multiplier will cancel out due to the symmetry of the transconductance stage. The minor effect of $C_{\mu1}$ will not be observed due to the symmetry of the switching stage as shown in (4.2.13)

and (4.2.14)

$$V_{out+} - V_{out-} = \left[2V_{LO+}Y_3 + 2V_{LO-}Y_4 - V_{RF}\left[gm_1 - j\omega C_{\mu 1} - 2gm_1\frac{Y_1}{Y_1+Y_2}\right]\right] \left[\frac{gm_4 - gm_3}{j\omega(C_{\mu 3}+C_{\mu 5}) + \frac{1}{R_L}}\right]\frac{1}{Y_3+Y_4+j\omega C_{\mu 1}} \quad (4.2.13)$$

$$V_{out+} - V_{out-} = V_{RF}j\omega C_{\mu 1}\left[\frac{gm_4 - gm_3}{j\omega(C_{\mu 3}+C_{\mu 5}) + \frac{1}{R_L}}\right]\frac{1}{Y_3+Y_4+j\omega C_{\mu 1}} = 0 \quad (4.2.14)$$

LO-RF

Equation (4.2.15) for V_{RF} has been derived from the V_y node analysis, as shown in Fig. 4.4. The V_x and V_y have been inserted into the (4.2.16) from the above-mentioned ones, (4.2.3) and (4.2.7) respectively. V_y and V_z is considered equal and verified through simulation. Equation (4.2.18) shows that the LO leakages will cancel since Y_3 will dominate $j\omega C_{\mu 1}$.

$$V_{RF} = \left[V_{LO+}Y_3 + V_{LO-}Y_4 - (Y_3+Y_4)V_y + gm_1V_x\right]\frac{1}{gm_1 - j\omega C_{\mu 1}} \quad (4.2.15)$$

$$V_{RF} = \left[V_{LO+}Y_3 + V_{LO-}Y_4 - (Y_3+Y_4)\left[V_{LO-}Y_5 + V_{LO+}Y_6 + gm_2V_{RF}\frac{Y_1}{Y_1+Y_2}\right] \frac{1}{Y_5+Y_6+j\omega C_{\mu 2}} + gm_1V_{RF}\frac{Y_1}{Y_1+Y_2}\right]\frac{1}{gm_1 - j\omega C_{\mu 1}} \quad (4.2.16)$$

$$V_{RF} = \left[V_{LO+}\left[Y_3 - Y_6\frac{Y_3+Y_4}{Y_5+Y_6+j\omega C_{\mu 2}}\right] + V_{LO-}\left[Y_4 - Y_5\frac{Y_3+Y_4}{Y_5+Y_6+j\omega C_{\mu 2}}\right] + V_{RF}\left[gm_1\frac{Y_1}{Y_1+Y_2} - gm_2\frac{Y_1}{Y_1+Y_2}\frac{1}{Y_5+Y_6+j\omega C_{\mu 2}}\right]\right]\frac{1}{gm_1 - j\omega C_{\mu 1}} \quad (4.2.17)$$

$$V_{RF} = \left[(V_{LO+} + V_{LO-})\left[Y_3 - Y_3\frac{2Y_3}{2Y_3+j\omega C_{\mu 1}}\right] + \frac{V_{RF}gm_1}{2}\left[1 - \frac{2Y_3}{2Y_3+j\omega C_{\mu 1}}\right]\right]\frac{1}{gm_1 - j\omega C_{\mu 1}} = 0 \quad (4.2.18)$$

CG

$$V_y = \left[V_{LO+}Y_3 + V_{LO-}Y_3 - V_{rf}(gm_1 - j\omega C\mu_1) + \frac{V_{rf}}{2}gm_1\right]\frac{1}{2Y_3 + j\omega C\mu_1} \quad (4.2.19)$$

$$V_y = \left[-\frac{V_{rf}}{2}gm_1 + V_{rf}j\omega C\mu_1\right]\frac{1}{2Y_3 + j\omega C\mu_1} \tag{4.2.20}$$

$$V_z = \left[V_{LO+}Y_3 + V_{LO-}Y_3 + \frac{V_{rf}}{2}gm_1\right]\frac{1}{2Y_3 + j\omega C\mu_1} \tag{4.2.21}$$

$$V_z = \left[\frac{V_{rf}}{2}gm_1\right]\frac{1}{2Y_3 + j\omega C\mu_1} \tag{4.2.22}$$

$$-2V_xY_1 = 0 \tag{4.2.23}$$

$$V_x = 0 \tag{4.2.24}$$

Impedance seen at V_y and V_z is equal due to symmetry.

$$-2V_yY_3 + i_y = -V_xgm_1 + V_yj\omega C\mu_1 \tag{4.2.25}$$

$$Z_z = Z_y = \frac{V_y}{i_y} = \frac{1}{2Y_3 + j\omega C\mu_1} \tag{4.2.26}$$

$$I_y = \frac{V_y}{Z_y} = \left[-\frac{V_{rf}}{2}gm_1 + V_{rf}j\omega C\mu_1\right]\frac{1}{2Y_3 + j\omega C\mu_1}(2Y_3 + j\omega C\mu_1) \tag{4.2.27}$$

$$I_y = \left[-\frac{V_{rf}}{2}gm_1 + V_{rf}j\omega C\mu_1\right] \tag{4.2.28}$$

$$I_z = \left[\frac{V_{rf}}{2}gm_1\right]\frac{1}{2Y_3 + j\omega C\mu_1}(2Y_3 + j\omega C\mu_1) \tag{4.2.29}$$

$$I_z = \frac{V_{rf}}{2}gm_1 \tag{4.2.30}$$

$$V_{rf} = V_{RF}\cos(\omega_{RF}) \tag{4.2.31}$$

$$V_{lo} = \frac{4}{\pi}V_{LO}\left[\cos(\omega_{LO}) + \frac{1}{3}\cos(3\omega_{LO}) + \frac{1}{5}\cos(5\omega_{LO}) + ...\right] \approx \frac{4}{\pi}V_{LO}cos(\omega_{LO}) \tag{4.2.32}$$

$$V_{out+} = \frac{4}{\pi}V_{LO}\cos(\omega_{LO})V_{RF}\cos(\omega_{RF})\left[-\frac{1}{2}gm_1 + j\omega C\mu_1\right]\frac{1}{2Y_3 + j\omega C\mu_1} \tag{4.2.33}$$

$$V_{out+} = \frac{4}{\pi}V_{LO}\cos(\omega_{LO})V_{RF}\cos(\omega_{RF})\left[-\frac{1}{2}gm_1 + j\omega C\mu_1\right]\frac{1}{2Y_3 + j\omega C\mu_1} \tag{4.2.34}$$

B. Appendix

The setup for the flip chip technology simulation is provided step by step. The connection between the board and chip is done through solder balls. RFPro electromagnetic (EM) simulation enviroment makes this multi-technology simulation possible.

1. Create two separate workspaces for the IC chip (mixer_full_chip_1_wrk) and the board (mixer_board_1_wrk) separately.
2. Add the board workspace to the IC chip workspace. (Manage Libraries)
   (a) "Add Library definition" will make workspace read only, add the IC chip library through "Add Library" with shared mode (red arrow). Add the technology definition of the IC chip workspace through "Add Library definition" (blue arrow), as shown in Fig. 4.5.

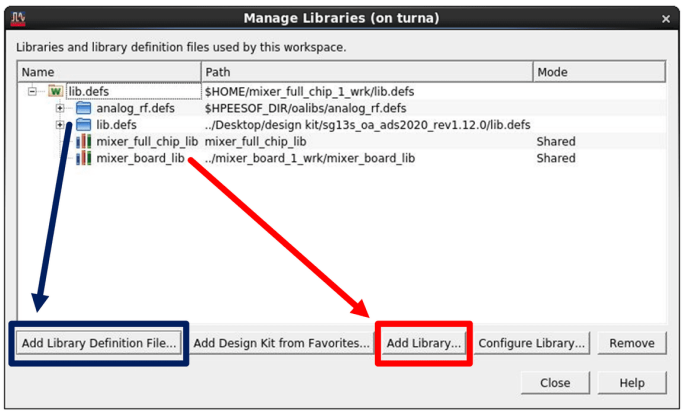


Figure 4.5: Board library addition to the chip workspace.

3. Create new layout for assembly. Choose the correct technology.
   (a) Adds package from the library added.
   (b) Look at the stack up, automatically uses the package board substrate.
      i. Create a local copy of the substrate since it is not editable. Call "tech" the substrate to make it master substrate.
      ii. Add a conductor layer to the level where chip will be added in the chip substrate. The chip_top can be left as perfect conductor or copper. Create a bounding area layer, click anywhere in blank space of substrate editor, Bound(13).
      iii. In the board substrate, bound layer is also defined. The outline of the board is defined through bound.

(c) Go to the IC chip layout, File → Customize pcell → smart mount pcell, as shown in Fig. 4.6.

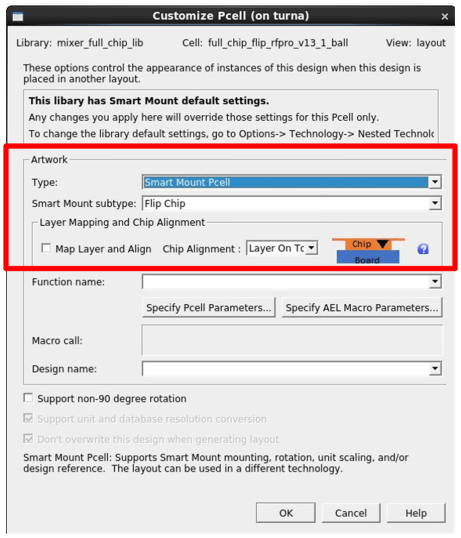


Figure 4.6: Definition of chip layout as pcell.

(d) Go to "Library View" to define the nested technology for board and chip, as shown in Fig. 4.7 - 4.8 respectively. Define smart mount type as flip chip for board workspace and custom for the chip workspace. In smart mount subtype, you can choose which mount type you will employ. In the board nested technology definition the chi_top layer is mapped to the PCB_top.

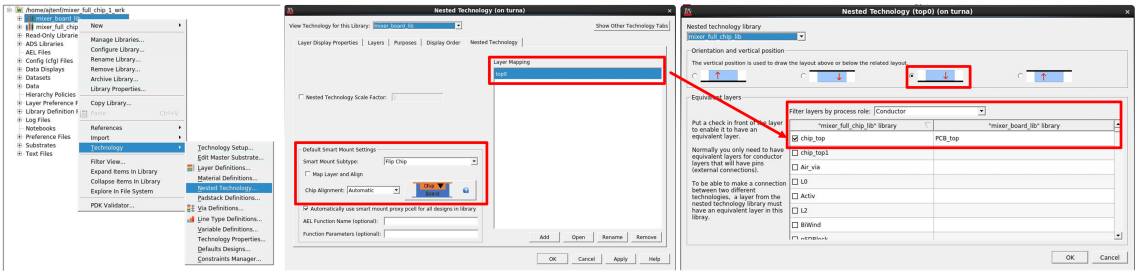


Figure 4.7: Nested technology definition of board.

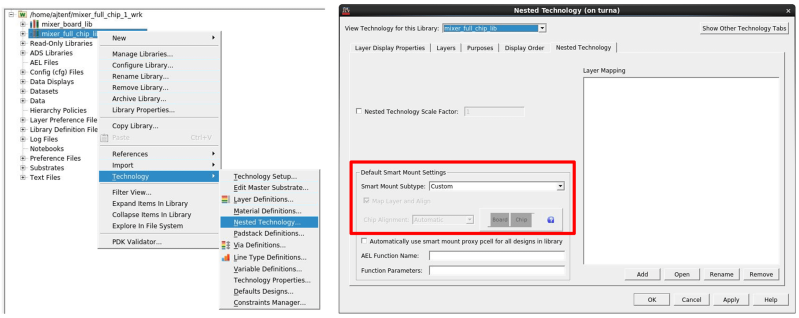


Figure 4.8: Nested technology definition of chip.

4. The full IC chip layout is drawn and simulated in conventional RFPro in its own workspace. The board layout is available from the board workspace.

5. To the board layout place the IC chip through the Insert → Component → Component Library, as shown in Fig. 4.9.

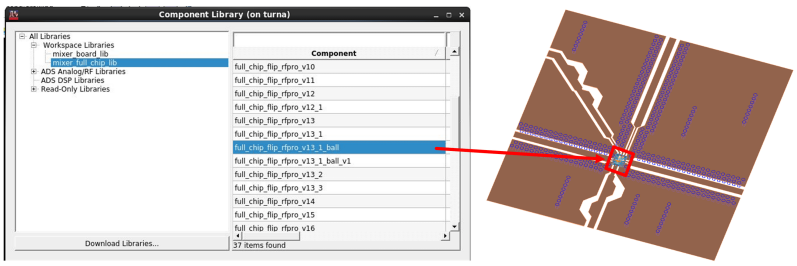


Figure 4.9: Chip placement as component to the board layout .

(a) Select and right click to the chip component and select the mount layer as the PCB_top, as shown in Fig. 4.10.

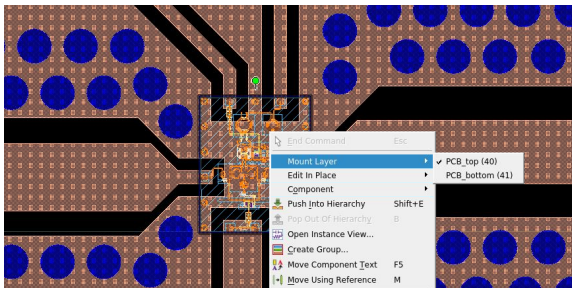


Figure 4.10: Mount layer definition of the chip to the board

6. To open the RFPro: Tools → RFPro → New...

(a) In RFPro: Create → Solder ball → Edit Solder ball → Define solder ball dimensions → Specify orientation → Advanced Mode → After clicking the arrow in red square specify the position of the solder ball, as shown in Fig. 4.11.

(b) Define Solder ball material as typical_solder or copper or gold.

(c) Define the IC chip as SubDesign. The capacitors and conductor vias as layout, while the transistors and resistors are left as circuit, as shown in Fig. 4.13.

(d) Finally, the simulation setup is defined. First the pins of the board are added as ports and the transistors and resistors are added as component models, as done for the conventional RFPro simulation. Afterwards, "Options" is doubled clicked to define the Simulator as FEM and the Solver

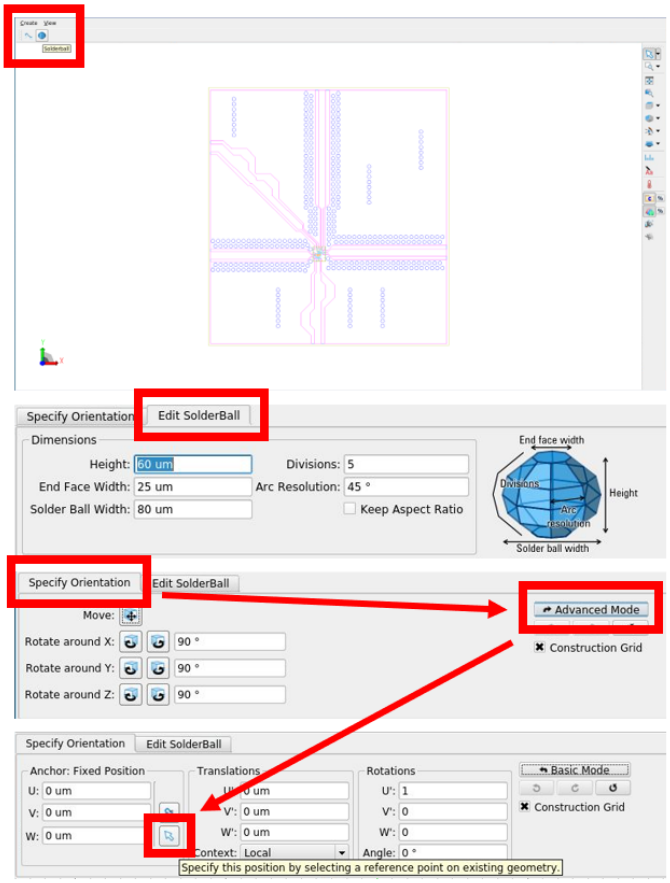


Figure 4.11: Solder ball definition and orientation steps.

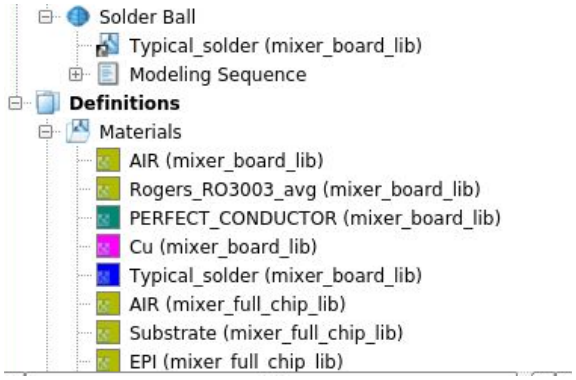


Figure 4.12: Solder ball material definition.

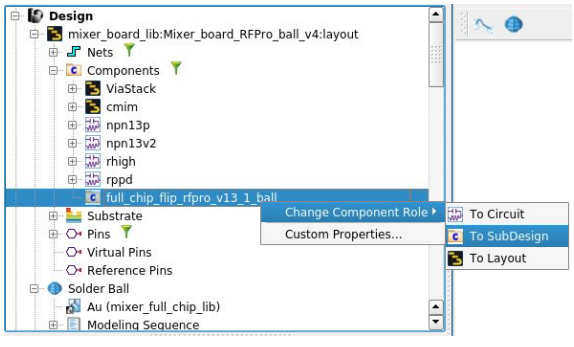


Figure 4.13: IC chip definition as subdesign.

as Direct. In the “Frequency Plans”, the frequency range of simulation is settled. The simulation starts as “Run” is clicked, as shown in Fig. 4.14.

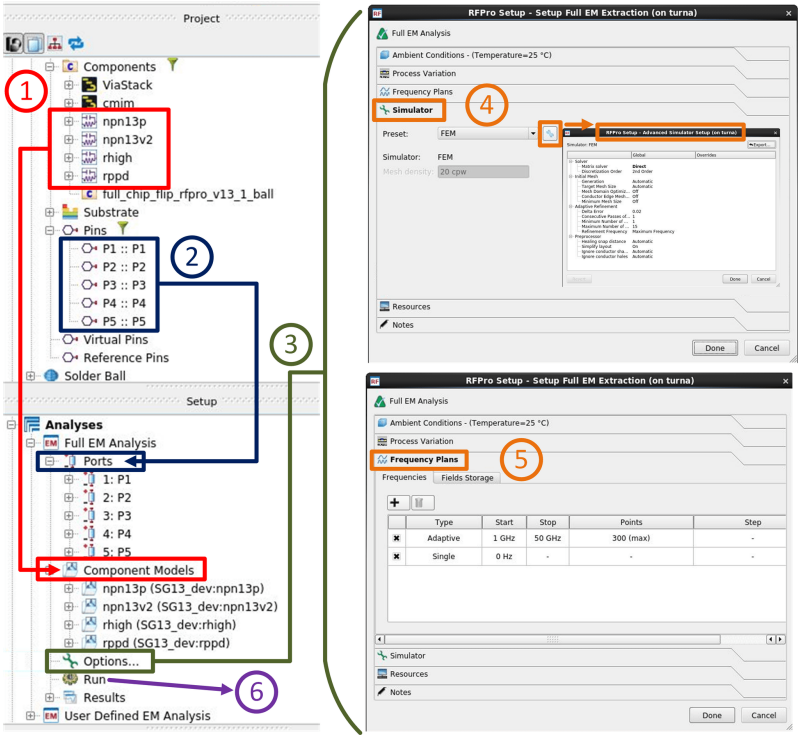


Figure 4.14: RFPro FEM simulation setup.

(e) As the simulations are completed the symbol is completed through the Results → Generate Sub Circuit. . . , as shown in Fig. 4.15.

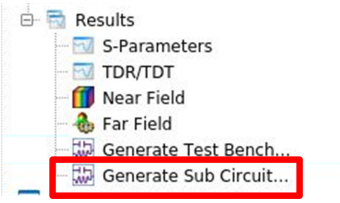


Figure 4.15: Symbol generation of the RFPro simulated board & chip.

(f) In the schematic view the symbol is defined as “schematic_Full_EM_Analysis”, as shown in Fig. 4.16.

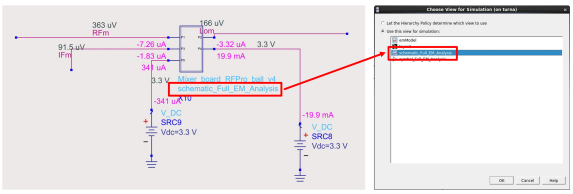


Figure 4.16: RFPro simulated chip & board schematic symbol definition.

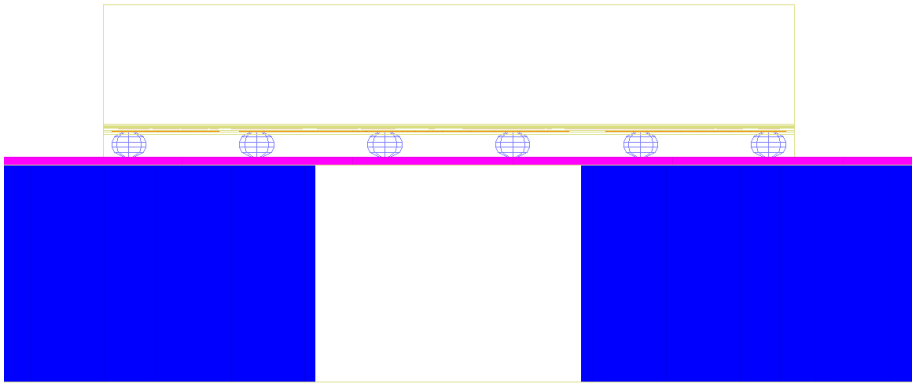


Figure 4.17: Side view of the board connected to chip through solder balls.

7. Significant Points of the Simulation Setup:

   (a) Errors during the RFPro simulations will not be showing, however the DC currents will not be flowing. The reason is that the metal layer in which the emitter of the transistor will be connected are not shorted, as shown in Fig. 4.18 (a). In the stand-alone IC chip simulation in RFPro this did not cause a problem. For correct simulation setup the metal layer in which the emitter is connected must be shorted as shown in Fig. 4.18 (b), and the transistor to be added as shown in Fig. 4.18 (c).

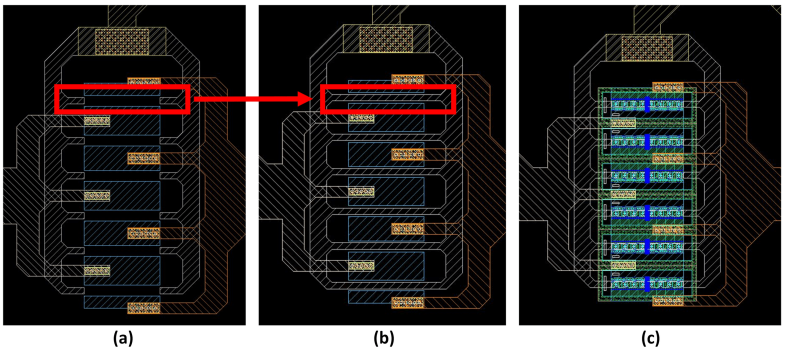


Figure 4.18: The layout view of (a) emitter metal layer with two connections, (b) shorted emitter metal layer , (c) shorted emitter metal layer with transistors.

   (b) Both the IC chip and board substrate definitions must be defined as master, since these are the ones which will be used by the RFPro simulator. In the chip substrate after the Passive layer Air of 54 um is added since it corresponds to the 60 um height of the ball, when the SiO2 and Passive layer above the TopMetal2 is considered. The solder and chip_top layers are added only for demonstration purposes and are not used during the

simulations, as shown in Fig. 4.19. The board substrate is defined in the conventional manner. with the ground plane being defined as perfect conductor, as shown in Fig. 4.20. The ground layer could have been defined at the lower side of board as a copper conductor layer (PCB_bottom), however, this did not result to any difference.

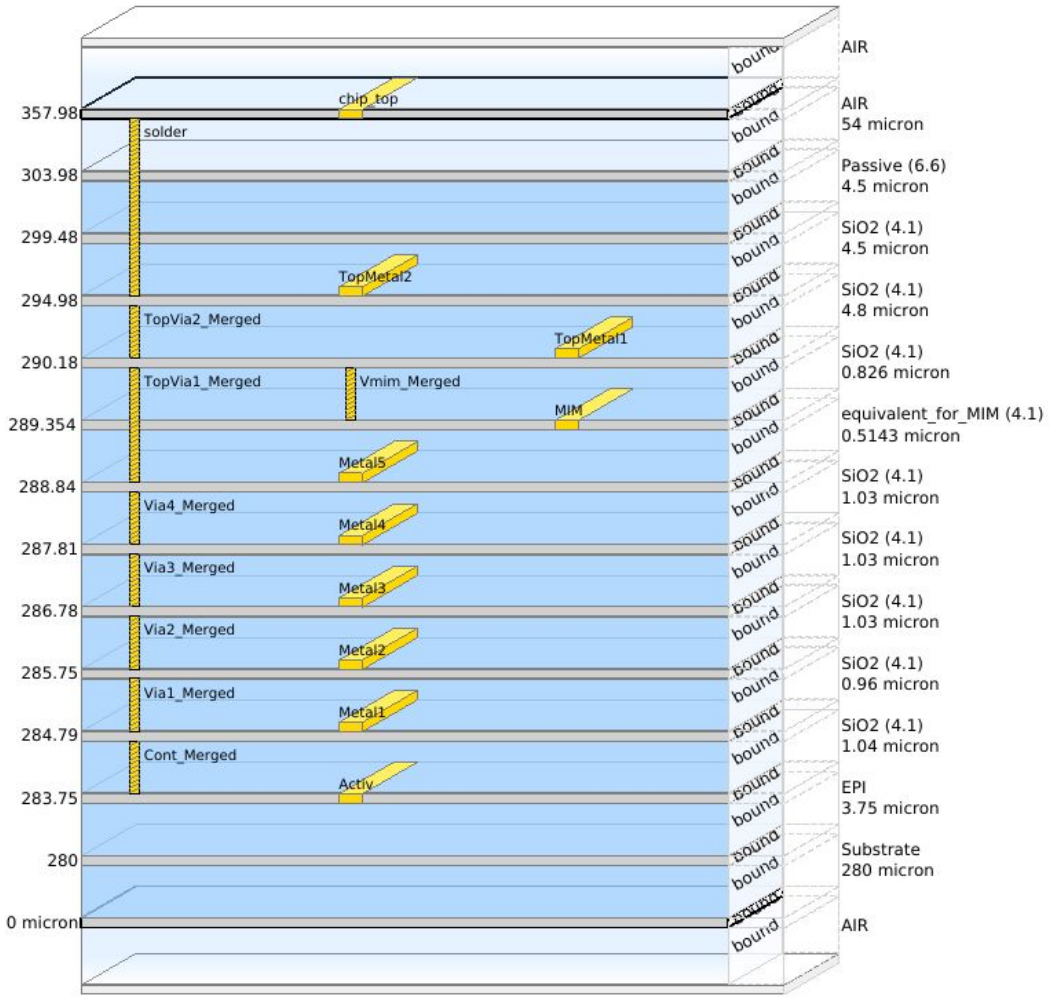


Figure 4.19: The cross section view of the IC chip substrate.

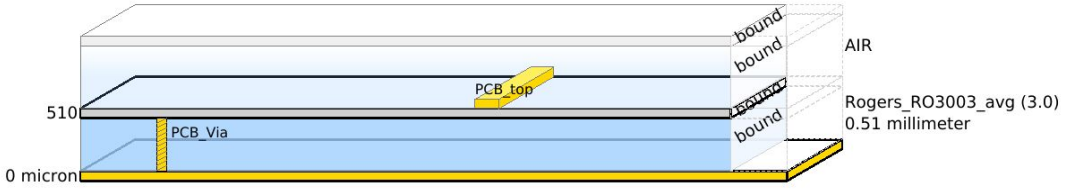


Figure 4.20: The cross section view of the board substrate.

Tutorial upon the above discussed simulation setup is available online at [74]. The tutorial upon the multi-technology setup and simulation in RFPro employing wire-bond packaging is available at [75].

C. Appendix

In this section, the noise transfer function of the input and PD & CP noise sources is going to be derived. Similar logic is applied to the other NTF(s) equations.

Eq. (4.2.35) the closed loop transfer function considering only the input noise source. The equation is arranged according to the output and input, (4.2.36). Finally, the $\mathrm{NTF_{in}}$(s) is given in (4.2.37), and in terms of open loop transfer function.

In similar manner the closed loop equation for the PF & CP noise source is written, Eq. (4.2.38). Since each noise source is added to the output node of the respective block, I(s) is added to the output of PD & CP. The equations is arranged according to I(s) and ϕ_{out} in Eq. (4.2.39). The $\mathrm{NTF_I}$(s) in terms of open loop transfer function is given in Eq. (4.2.40).

$\mathbf{NTF_{in}}$(s)

$$\phi_{out} = \left(\phi_{in} - \frac{\phi_{out}}{N}\right) \frac{K \cdot F(s) \cdot K_{VCO}}{s} \tag{4.2.35}$$

$$\phi_{out}\left(1 + \frac{K \cdot F(s) \cdot K_{VCO}}{s \cdot N}\right) = \phi_{in}\frac{K \cdot F(s) \cdot K_{VCO}}{s} \tag{4.2.36}$$

$$NTF_{in}(s) = \frac{\phi_{out}}{\phi_{in}} = \frac{\frac{K \cdot F(s) \cdot K_{VCO}}{s}}{1 + \frac{K \cdot F(s) \cdot K_{VCO}}{s \cdot N}} = \frac{N \cdot G(s)}{1 + G(s)} \tag{4.2.37}$$

$\mathbf{NTF_I}$(s)

$$\phi_{out} = \left(-\frac{\phi_{out}}{N} \cdot K + I(s)\right) \frac{F(s) \cdot K_{VCO}}{s} \tag{4.2.38}$$

$$\frac{I(s) \cdot F(s) \cdot K_{VCO}}{s} = \phi_{out}\left(1 + \frac{K \cdot F(s) \cdot K_{VCO}}{s \cdot N}\right) \tag{4.2.39}$$

$$NTF_I(s) = \frac{\phi_{out}}{I(s)} = \frac{\frac{F(s) \cdot K_{VCO}}{s}}{1 + \frac{K \cdot F(s) \cdot K_{VCO}}{s \cdot N}} = \frac{\frac{N}{K} \cdot G(s)}{1 + G(s)} \tag{4.2.40}$$

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