LOW NOISE AMPLIFIERS AND VOLTAGE VARIABLE ATTENUATORS FOR SUB-6 GHZ 5G RECEIVER SYSTEMS

by
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ABSTRACT

LOW NOISE AMPLIFIERS AND VOLTAGE VARIABLE ATTENUATORS FOR SUB-6 GHZ 5G RECEIVER SYSTEMS

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Keywords: 5G, sub-6 GHz, receiver, LNA, attenuator

To achieve the demanding performance specifications of the new generation of communication systems (5G), such as increased high data rate, communication distance, and low latency, better receiver systems, and new design methodologies are needed. Moreover, as the number of users increases and the area of usage of RF transmitter/receiver devices broadens tremendously in recent years, the cost of RF systems gained more importance; thus, the die area became another design concern. Additionally, decreasing the power consumption also gained importance as the number of IoT and health monitoring devices increases where battery life is critical. One of the requirements of 5G is a higher data rate, and in order to meet this requirement, the noise performance of the RF receiver system should be improved. Furthermore, to increase the maximum range of the communication, receiver systems with higher gain should be aimed. Finally, multi-stage sub-blocks such as digital-step attenuators should be replaced with novel and very small attenuator topologies to decrease the die area and reduce the fabrication cost of receiver systems.

This thesis focuses on designing and implementing sub-blocks of radio frequency (RF) integrated receiver (Rx) systems such as LNAs and attenuators for the Sub-6 GHz 5G communication. The presented SiGe BiCMOS LNA is designed and fabricated with IHP 130 nm SiGe BiCMOS technology, and it achieves a 27.7 dB gain and 1.15 dB noise figure, which is one of the best performance among the SiGe BiCMOS LNAs in its frequency band. In addition, two LNAs are designed and fabricated in GlobalFoundries 130 nm SOI CMOS technology, and these LNAs have a gain of 30.5 dB and 0.85 dB NF. Finally, two VVAs are designed with GlobalFoundries 130 nm SOI CMOS technology. The first VVA is fabricated and measured so that it achieves 6-bit attenuation performance over DC - 27 GHz frequency range, while the second VVA reaches ultra-high precision of 0.12 mdB attenuation per step inside the DC - 10 GHz frequency range.

ÖZET

6 GHZ ALTI 5G ALICI SISTEMLERI İÇIN DÜŞÜK GÜRÜLTÜLÜ YÜKSELTICILER VE VOLTAJ DEĞIŞKENLI ZAYIFLATICILAR

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Anahtar Kelimeler: 5G, 6 GHz altı, alıcı, LNA, zayıflatıcı

Yeni nesil iletişim sistemlerinin (5G) artan yüksek veri aktarım hızı ve maksimum iletişim mesafesinin yanı sıra düşük gecikme gibi zorlu performans özelliklerine ulaşmak için daha iyi alıcı sistemleri ve yeni tasarım metodolojilerine ihtiyaç vardır. Ayrıca son yıllarda kullanıcı sayısının artması ve RF verici/alıcı cihazlarının kullanım alanlarının büyük ölçüde genişlemesiyle birlikte RF sistemlerinin maliyeti daha da önem kazanmış olup ve çip alanı önemli bir tasarım konusu haline gelmiştir. Ayrıca IoT ve sağlık takip cihazları gibi pil ömrünün kritik olduğu cihazların sayısı arttıkça güç tüketiminin azaltılması da önem kazanmıştır. 5G'nin gereksinimlerinden biri de daha yüksek veri hızıdır ve bu gereksinimi karşılamak için RF alıcı sisteminin gürültü performansının iyileştirilmesi ve iletişimin maksimum menzilinin artırılması için daha yüksek kazançlı alıcı sistemleri hedeflenmelidir. Son olarak, çip alanını azaltmak ve alıcı sistemlerin üretim maliyetini azaltmak için, dijital adımlı zayıflatıcılar gibi çok aşamalı alt bloklar, yeni ve çok küçük zayıflatıcı topolojileri ile değiştirilmelidir.

Bu tez, LNA'lar ve zayıflatıcılar gibi 6 GHz altı 5G iletişimi sistemleri için radyo frekansı (RF) entegre alıcı (Rx) modüllerinin alt bloklarının tasarımı ve uygulanmasına odaklanmaktadır. Sunulan SiGe BiCMOS LNA, IHP 130 nm SiGe BiCMOS teknolojisi ile tasarlanmış ve üretilmiş olup kendi frekans bandında SiGe BiCMOS LNA'lar arasında en iyi performanslardan biri olan 27.7 dB kazanç ve 1.15 dB gürültü rakamına ulaşmaktadır. Buna ek olarak, GlobalFoundries 130 nm SOI CMOS teknolojisiyle iki LNA tasarlanmış ve üretilmiştir ve bu LNA'lar 30.5 dB ve 0.85 dB NF'ye sahiptir. Son olarak, GlobalFoundries 130 nm SOI CMOS teknolojisi ile iki VVA tasarlanmıştır. İlk VVA, üretilmiş olup DC - 27 GHz frekans aralığında 6 bitlik zayıflatma performansına ulaştığı kaydedilmiştir, ikinci VVA ise DC - 10 GHz frekans aralığında bit başına 0.12 mdB'lik ultra yüksek hassasiyete ulaştığı simüle edilerek gözlemlenmiştir.

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To my family...
Aileme...

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LIST OF ABBREVIATONS

NF_{min} Minimum Noise Figure 11

3GPP 3rd Generation Partnership Project 2

ADC Analog-to-Digital Converter 6

BC Body-Contacted 29

BiCMOS Bipolar Complementary Metal Oxide Semiconductor 6

CDMA Code Division Multiple Access 1

CG Common-Gate 26

CMOS Complementary Metal Oxide Semiconductor 6

CS Common-Source 25

DAC Digital-to-Analog Converter 6

dB Decibel 14

DC Direct Current 11

DSP Digital Signal Processing 6

FB Floating-Body 29

FDMA Frequency Division Multiple Access 1

FET Field-Effect-Transistors 6

FoM Figure-of-Merit 22

GaAs Gallium-Arsenide 6

GaN Gallium-Nitride 6

Gbps Gigabit-per-second 1

GHz Giga-Hertz 6

GSG Ground-Signal-Ground 18

HBT Heterojunction Bipolar Transistor 6

IC Integrated Circuit 6

IIP3 Input Third-Order Intercept Point 15

IL Insertion loss 8

IM3 3^{rd} Order Inter-Modulation Product 28

IoT Internet of Things 3

IP Internet Protocol 1

IP1dB Input 1 dB Compression Point 22

ITUR International Telecommunication Union: Radiocommunication Sector . . . 1

LNA Low Noise Amplifier 3

LTE Long Term Evolution 3

Mbps Megabit-per-second 1

MIM Metal-Insulator-Metal 7

MIMO Massive Input Massive Output 10

MMS Multimedia Message Service 1

NF Noise Figure 3

OFDMA Orthogonal Frequency Division Multiple Access 1

OIP3 Output Third-Order Intercept Point 15

Op-Amp Operational Amplifier 71

OP1dB Output 1 dB Compression Point 18

PS Phase Shifter 3

RF Radio-Frequency 3

RMS Root Mean Square 53

Rx Receiver System 3

SiGe Silicon-Germanium 6

SMS Short Message Service 1

SOI Silicon-on-Insulator 6

VGA Variable Gain Amplifier 3

VVA Voltage Variable Attenuator 8

1. INTRODUCTION

1.1 5G Communication Systems

The communication systems' standardization started with the first generation's development (1G) in 1983. In the 1G standard, transmitting and receiving voices in the analog domain are aimed, and digital modulation techniques are not employed; instead, analog modulation techniques and Frequency Division Multiple Access (FDMA) are employed (Blecher, 1980). The second generation of the communication systems (2G) was realized in 1991 and dissimilar to 1G, 2G systems operated in the digital domain and utilized Code Division Multiple Access (CDMA) and FDMA. With the employment of 2G, the data rates are increased by order of magnitude, and new services such as Short Message Service (SMS) and Multimedia Message Service (MMS) are introduced (Rahnema, 1993). The demand for higher data rates and bandwidth continued to increase, and after another ten years, the third generation of communication systems was introduced in 2002. New highly-demanding features such as mobile internet and video call became available with the increased data transfer speed of the 3G systems.

International Telecommunication Union: Radiocommunication Sector (ITUR) has aimed for higher data rates for mobile and immobile devices, where the aimed data rate is 100 Mbps for mobile and 1 Gbps for immobile devices. Orthogonal FDMA (OFDMA) and Internet Protocol (IP) switching methods have been utilized in 4G communication systems to obtain such high data rates. (Han & Lee, 2005). The mobile communication system generations are summarized in Fig. 1.1 (Rao, 2012).

Even though the data rates and bandwidths have increased tremendously with 4G communication systems, their inabilities have occurred as the communication link trend has shifted from human-to-human communication to device-to-device commu-

Technology	Various generations				
	1G	2G	2.5G	3G	4G
Design began	1970	1980	1985	1990	2000
Implementation	1984	1991	1999	2002	2012–2015
Service	Analogue voice	Digital voice	High-capacity packets, MMS	High-capacity broadband data	Higher capacity, completely IP, Multimedia
Multiple access	FDMA	TDMA, CDMA	TDMA, CDMA	CDMA	OFDMA
Standards	AMPS, TACS, NMT	CDMA, GSM, PDC	GPRS, EDGE	WCDMA, CDMA2000	Single standard
Bandwidth	1.9 kbps	14.4 kbps	384 kbps	2 Mbps	200 Mbps
Core network	PSTN	PSTN	PSTN, Packet network	Packet network	Internet

Figure 1.1 History of 1G, 2G, 3G, and 4G communication system standards.

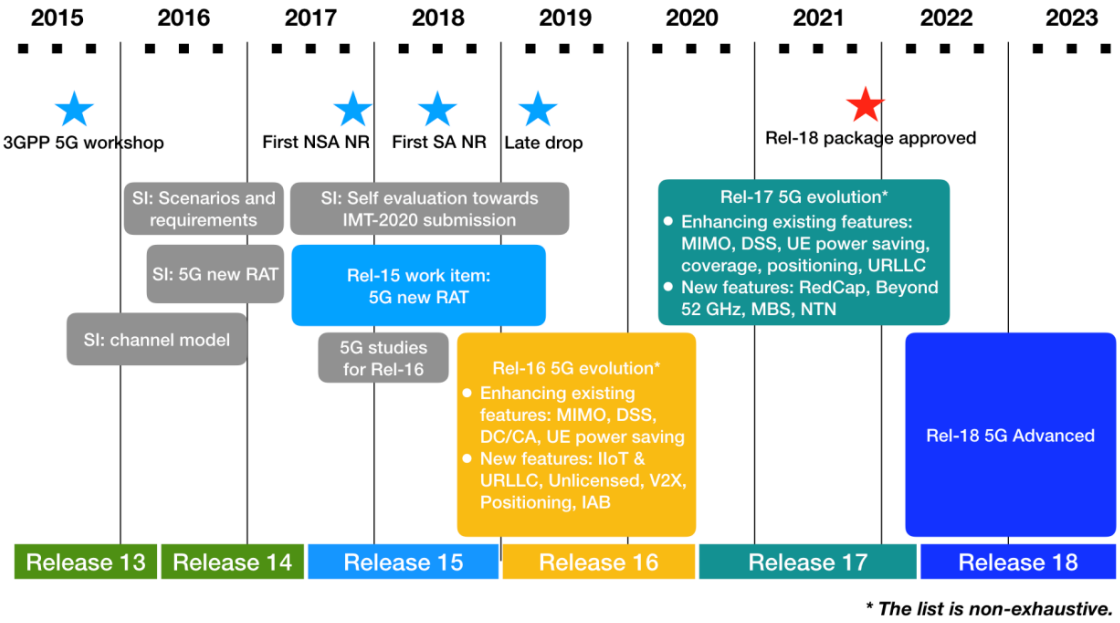

Figure 1.2 Roadmap of the 5G communication systems.

nication. Due to excessive data usage of devices, a new generation of communication systems is needed. The first release of the fifth generation of mobile communications (5G) was released in June 2018 by the 3rd Generation Partnership Project (3GPP) (Lin, Li, Baldemair, Cheng, Parkvall, Larsson, Koorapaty, Frenne, Falahati, Grovlen & Werner, 2019). Since the first release of the 5G, 3GPP has aimed to increase availability, broaden the area of usage, and improve performance. (Ghosh, Maeder, Baker & Chandramouli, 2019). The roadmap for the 5G systems is shown in Fig. 1.2 (Lin, 2022).

5G communication systems introduce a vast advancement in the connectivity ca-

Figure 1.3 Areas of usage for 5G communication systems.

pabilities that were mainly available for mobile devices such as smartphones and tablets during the Long Term Evolution (LTE) period. Increased data rates, speed, and availability will be able to push the limits for mobile devices. Moreover, with the increased availability, new possibilities will be introduced to daily lives, such as smart homes, the Internet of Things (IoT), and wearable health tracking devices, as shown in Fig. 1.3 (Xiang, Zheng & Shen, 2016). ITUR has specified some requirements for the 5G technology by studying the necessities of these application areas. According to ITUR's expectations, the number of devices connected to the internet will increase significantly with the introduction of IoT to daily lives, and data rates need to be increased with the 5G communication. Because of this, the peak downlink data rate of up to 25 Gb/s, an uplink data rate of up to 10 Gb/s are set as a goal and the specifications of the 5G communication is summarized in Fig. 1.4 (Romano, 2019).

1.2 RF Receiver Systems

Typical radio-frequency (RF) receiver systems (Rx) consist of sub-blocks such as Low Noise Amplifiers (LNA), Phase Shifters (PS), Attenuators, and Variable Gain Amplifiers (VGA), as shown in Fig. 1.5 (Burak, 2021). In the receiver systems, the noise figure (NF) is a critical parameter where the received signal's power level is very insignificant and even a small amount of additional noise power may be able to

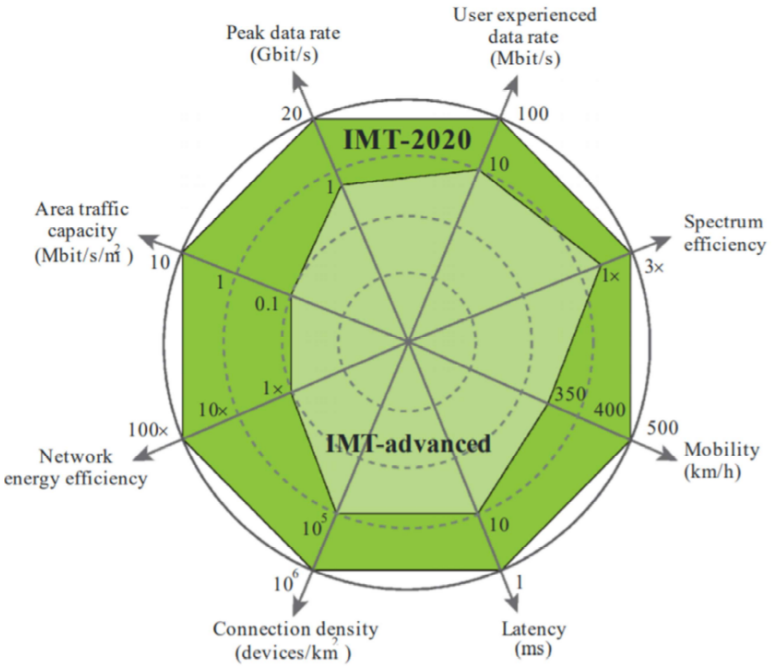

Figure 1.4 Specified requirements of 5G communication systems.

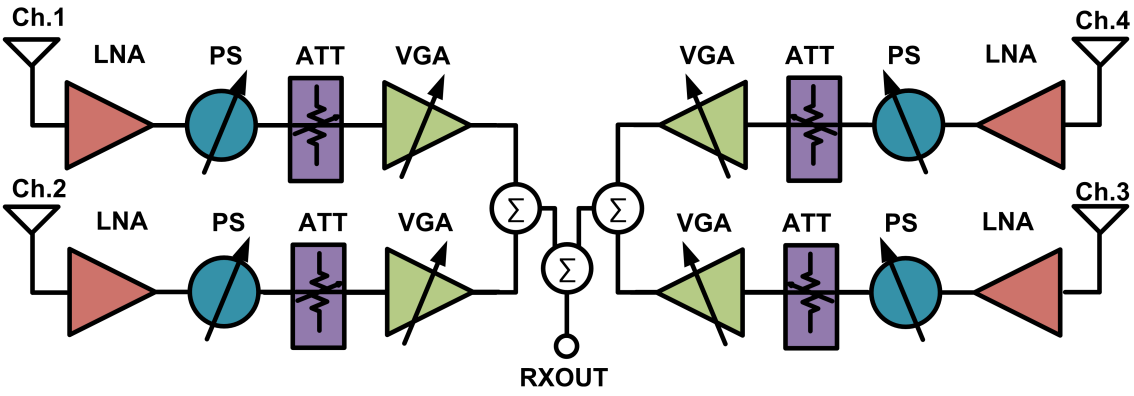

Figure 1.5 A 4-channel receiver system's block diagram.

make the signal undetectable since the NF is defined as in Eqn. 1.1 (Pozar, 2011), which is not the case for transmitter systems.

$$F = 1 + \frac{N_{added}}{N_i}. \tag{1.1}$$

In the receiver architectures, the order of the sub-blocks has significant importance since it directly affects the NF performance of the system. The noise contribution of each sub-block and the receiver system's overall NF can be calculated using Eqn. 1.2. According to Eqn. 1.2 the first sub-block in the receiver chain has to have

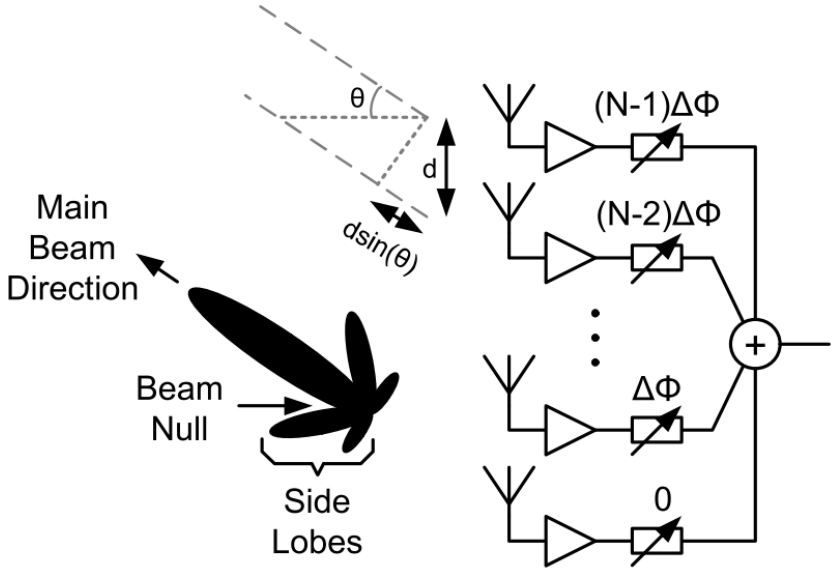

Figure 1.6 Beamforming technique with multiple antenna elements.

very low noise and very high gain to suppress the noise contribution of proceeding blocks. Hence, for many receiver systems, a high gain LNA is positioned as the first sub-block of the chain to have a better noise performance and amplify the signal level.

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3}. \tag{1.2}$$

In addition to LNA, the phase shifter is another commonly used sub-block in the receiver systems where the beamforming technique is realized. In general, this technique is actuated to increase the transmitted/received signal's power by utilizing several antennas and increasing the directivity of the whole antenna array by forming a beam by applying a phase (or time) difference between the antenna elements, as shown in Fig. 1.6 (Kalyoncu, 2019). However, beamforming is not widely used at low-frequency bands; instead, it is commonly used at mm-wave frequencies where the free path loss is more critical and challenging.

Finally, attenuators and variable gain amplifiers are amplitude control blocks used to decrease or increase the power level to obtain the signal at the desired power level. These amplitude control blocks become crucial sub-blocks when the dynamic range of the receiver system is considered; attenuators help to widen the dynamic range towards the high input power region, while VGAs are helpful to widen the dynamic range towards the low input power region.

1.3 Technology Selection

In the literature, there are three main integrated-circuits (IC) technologies that are used for RF applications, and these technologies can be listed as Silicon-Germanium (SiGe) Bipolar Complementary Metal-Oxide-Semiconductor (BiCMOS) Heterojunction Bipolar Transistor (HBT), Silicon Complementary Metal-Oxide-Semiconductor (CMOS) and III-V compound semiconductors. In general, III-V technologies such as Gallium-Arsenide (GaAs) achieve very high f_T and f_{max} values, making this technology a valuable candidate for RF circuits. Moreover, other III-V technologies like Gallium-Nitride (GaN) enable very high power handling capabilities. On the other hand, III-V technologies' fabrication costs are significantly higher than the other technologies and have low technology maturity, leading to low wafer yield, making these technologies unfavorable for mass production. In addition to cost, III-V technologies do not have CMOS integration, making digital circuits unavailable. Since the many RF transmitter and receiver chips also include circuits such as analog-to-digital converters (ADC), digital-to-analog converters (DAC), and digital signal processing (DSP) circuits, lacking CMOS integration leads to important problems for III-V technologies. Silicon CMOS technologies excel with their low cost, high integration, maturity, and yield. Moreover, Field-Effect-Transistors (FET) in this technology can perform very similar to ideal switches, which makes it attractive for RF control blocks such as switches, attenuators, and phase shifters. However, CMOS technology suffers from low f_T and f_{max} performance, making it a weak candidate for RF amplifier applications. With the development of Silicon-on-Insulator (SOI) technology, achieved f_T and f_{max} values for the CMOS technology increased significantly due to the lack of parasitic body capacitances and resistances. Noise performances of CMOS technologies are also improved with the SOI technology and can offer very low NF values. Finally, SiGe BiCMOS technology has been able to combine both CMOS integration and very high f_T and f_{max} values which makes this technology a very valuable candidate for RF applications. Even though the power handling capability of SiGe BiCMOS is not as high as GaN technologies, it excels with its high maturity and yield while having a lower cost than III-V technologies. Summary of technologies which are commonly used in IC applications are listed in Table 1.1 (Cressler & Niu, 2002).

In this thesis work, IHP Microelectronics 0.13 μm SG13S and GlobalFoundries' 0.13 μm 8SW technology processes were used. IHP's 0.13 μm technology is reported to achieve f_T and f_{max} of 250 and 340 GHz and breakdown voltage (BV) of 1.7V with its HBTs. On the other hand, GlobalFoundries 0.13 μm technology achieves

Table 1.1 Relative Performance Comparisons of Various Device Technologies for RFICs.

Performance Metric	**SiGe HBT**	**Si BJT**	**Si CMOS**	**III-V MESFET**	**III-V HBT**	**III-V HEMT**
Frequency response	+	0	0	+	++	++
1/f and phase noise	++	+	-	- -	0	- -
Broadband Noise	+	0	0	+	+	++
Linearity	+	+	+	++	+	++
Output conductance	++	+	-	-	++	-
Tranconductance/area	++	++	- -	-	++	-
Power dissipation	++	+	-	-	+	0
CMOS integration	++	++	N/A	- -	- -	- -
IC cost	0	0	+	-	-	- -

(Excellent: ++; Very good: +; Good: 0; Fair: - ; Poor: - -)

f_T and f_{max} of 220 and 250 GHz and BV of 1.2V with the technology's floating-body transistors. The IHP process consists of 5 thin metals (M1 - M5) and 2 thick top metals (TM1 - TM2), while the GlobalFoundries' process consists of 3 thin metals (M1 - MT) and single thick top metal (MA). These thick top metals can be used to realize high-quality factor inductors, while high-quality transformers and baluns may be feasible for the IHP technology only since GlobalFoundries' process lacks a secondary thick top metal. Both technologies included a high-density metal-insulator-metal (MIM) capacitor, which is crucial for RF applications. Finally, both processes offer different resistor types, such as n-well, p-well, silicided and unsilicided polysilicon.

1.4 Motivation

With the next generation of communication system technologies, data transfer rates and bandwidths become more challenging specifications than ever. These challenges have attracted the effort of academia and industry, and both parties have paid attention to new transmitter and receiver systems with better performance and lower costs. On the receiver part of the RF applications, the research aim has always been towards increased communication distance and increased data rate; because of that, low noise amplifiers have been the center of attention for the receiver systems. The advancement of low noise amplifiers started with the III-V technology process, characterized by its high cost and low yield. Even though these technologies offered

excellent performance, LNAs' future was open for further advancement. Therefore, low-cost silicon-based technologies such as SiGe BiCMOS and SOI CMOS have gained attention in academia and industry, leading to significant technological advancement in recent years. With the silicon's unparalleled cost efficiency and yield performance, these technologies became one of the best candidates for RF receiver systems.

The main objective of this thesis is to design two different high linearity low-noise amplifiers with SiGe BiCMOS and SOI CMOS technologies to investigate what advantages and disadvantages in the terms of gain, noise and linearity these technologies offer for Sub-6 GHz 5G RF applications. Moreover, with the superior RF switch performance of SOI CMOS technology, a new approach to attenuators will be demonstrated, which is called Voltage Variable Attenuator (VVA). Apart from conventional attenuator topologies, the designed VVA excels with its very low insertion loss (IL) and minimal core area, which is critical to further decreasing the receiver systems' cost. Finally, a novel VVA topology will be proposed, which aims for attenuation control with ultra-high precision and ease the control of VVAs.

1.5 Organization

This thesis' organization can be summarized as follows: in Chapter 2, firstly, changing demands and trends of receiver systems are discussed, and the newly defined requirements of the state-of-the-art LNAs are explained. Furthermore, the choice of IC technology for each LNA work and the advantages, disadvantages, and feasibility of the chosen technology is discussed. Apart from the technology discussion, analysis, and measurement results of different LNAs designed in IHP Microelectronics 0.13 μm SG13S and GlobalFoundries' 0.13 μm 8SW technology processes are presented. This part briefly explains appropriate design choices and techniques for each technology and packaging method. Finally, the designed LNAs are compared with other state-of-the-art LNAs, and the work's strong and weak points are discussed and summarized.

Chapter 3 contains fundamental knowledge of conventional attenuator topologies, discusses the strong and weak points of these topologies, and then moves towards a more novel topology. A wide-band VVA design is presented in the latter section, where necessary theoretical analyses are shown and have been proved with simu-

lation results. Following to theoretical part, measurement results of the designed VVA are presented and compared with other state-of-the-art attenuator works in the literature. Furthermore, a novel ultra-high precision VVA topology is presented with the analyses used during the design procedure, and the simulation results are shown in a later part.

Chapter 4 summarizes the work in this thesis and opens up a discussion of the limitations and possible solutions to these limitations. A list of future work finalizes the thesis.

2. HIGH LINEARITY LOW NOISE AMPLIFIERS FOR SUB-6 GHZ 5G RECEIVER SYSTEMS

2.1 Introduction

This chapter will cover design procedures, simulation, and measurement results of Sub-6 GHz high linearity LNAs. In section 2.2, shifting trends and the up-to-date requirements of state-of-the-art LNAs will be discussed. In section 2.3, an LNA designed and fabricated in 130 nm SiGe BiCMOS technology will be thoroughly discussed. Finally, in section 2.4, two 130 nm SOI CMOS LNAs' design steps, analyses, and results will be presented in detail.

2.2 Low Noise Amplifier Requirements

Sub-6 GHz applications have pushed for higher data rate requirements with each new generation. The demand for increased data rates has not only increased expectations on the noise performance of LNA but also created a demand for increased communication distances which have attracted attention to massive multiple-input-multiple-output (MIMO) systems (Huang, Nisbet, Lam, Doherty, Quaglietta & Vaillancourt, 2011). MIMO systems have introduced a new challenge for modern receiver chains, an increased linearity requirement since a stronger interferer resistance is required with each new channel in the sub-6 GHz region.

In receiver systems, a low NF is one of the most determinative specifications for a high data rate and maximizing the range of communication. Since the LNA mainly

dominates the noise figure of a receiver system, many modern receiver systems require an LNA with very low NF and high gain. Moreover, high gain increases the maximum communication distance, which is valuable for MIMO systems. Also, LNAs with high linearity are crucial if the signal detection range is significantly large and interferers are present.

Three topologies are widely available for the selection of LNA topology: common-emitter/source, common-base/gate, and cascode. Common-base/gate topology achieves noise matching with a lower power consumption than the other topologies (Zhuo, Li, Shekhar, Embabi, de Gyvez, Allstot & Sanchez-Sinencio, 2005). On the other hand, these topologies lack a low NF and high power gain performance. Common-emitter/source topologies introduce the lowest NF among these topologies. However, cascode topology offers the highest gain, which is valuable when the overall NF of the receiver chain is considered.

This chapter will discuss three different high linearity LNAs utilizing two different technologies. The first one of these LNAs mainly covers the 5 - 6 GHz frequency range, while the other two LNAs focus on a wider bandwidth of 2 - 5 GHz. 130nm SiGe BiCMOS technology has been chosen for the design and the fabrication of the high-frequency LNA since the SiGe BiCMOS technology offers higher f_T values than the other silicon-based technologies. This decision is mainly due to two advantages of SiGe BiCMOS technology. First, having higher f_T transistors improves the noise figure performance of the devices in higher frequencies. Secondly, the high gain of an LNA is a vital parameter to allow the LNA to dominate the NF of the receiver chain, which is another reason for selecting SiGe BiCMOS technology with a higher trans-conductance at the same DC current and higher f_T than the SOI CMOS (Li, Wang, Jain, Ding, Boenke, Wang, Wolf & Joseph, 2015). On the other hand, for the lower frequency LNAs, SOI CMOS technology is more feasible since it achieves lower minimum available noise figure values (NF_{min}) than SiGe BiCMOS technology. This situation can be explained by the technology's isolated substrate technology, which reduces the noise inserted from inductors and other devices through the silicon substrate. Additionally, available power gain values tend to be higher in lower frequencies; hence high power gain performances are achievable with SOI CMOS technology without using high f_T transistors. Therefore, for the design and the fabrication of the 2 - 5 GHz LNAs, 130nm SOI CMOS technology has been chosen.

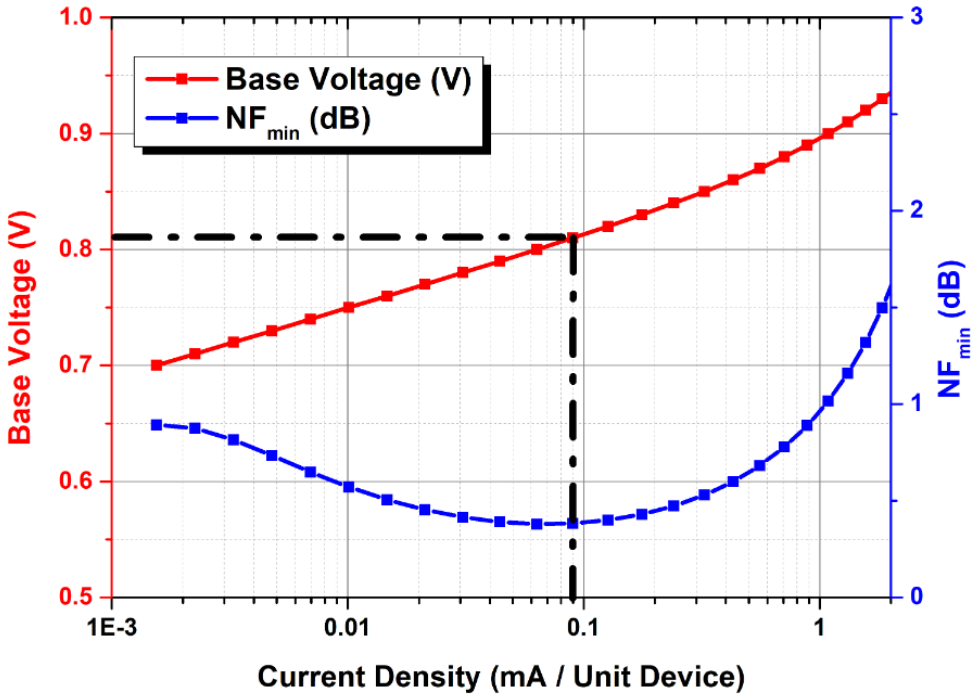

Figure 2.1 The relationship between the NF_{min}, bias voltage and the current density.

2.3 A 6 GHz Low Noise Amplifier in 130nm SiGe BiCMOS

2.3.1 Input Matching

Since noise performance is the most important performance criteria for the LNAs, optimizing the noise performance is the most critical and the first step of an LNA design. Therefore, firstly, the bias voltage of the device at the amplifier's input is chosen according to the lowest possible NF_{min}. The current density should be selected accordingly to achieve the lowest NF_{min}. The relationship between the NF_{min}, bias voltage and the current density is shown in Fig. 2.1.

Since the lowest possible NF_{min} achievable when the bias voltage is 810 mV, the total device area should be selected such that noise and power matching should be satisfied at the same time. Conventionally, this can be achieved by selecting the device size such that the optimum noise reflection coefficient Γ_{opt} is placed on the R=1 cycle on the Smith Chart. Afterward, with the help of a degeneration inductor,

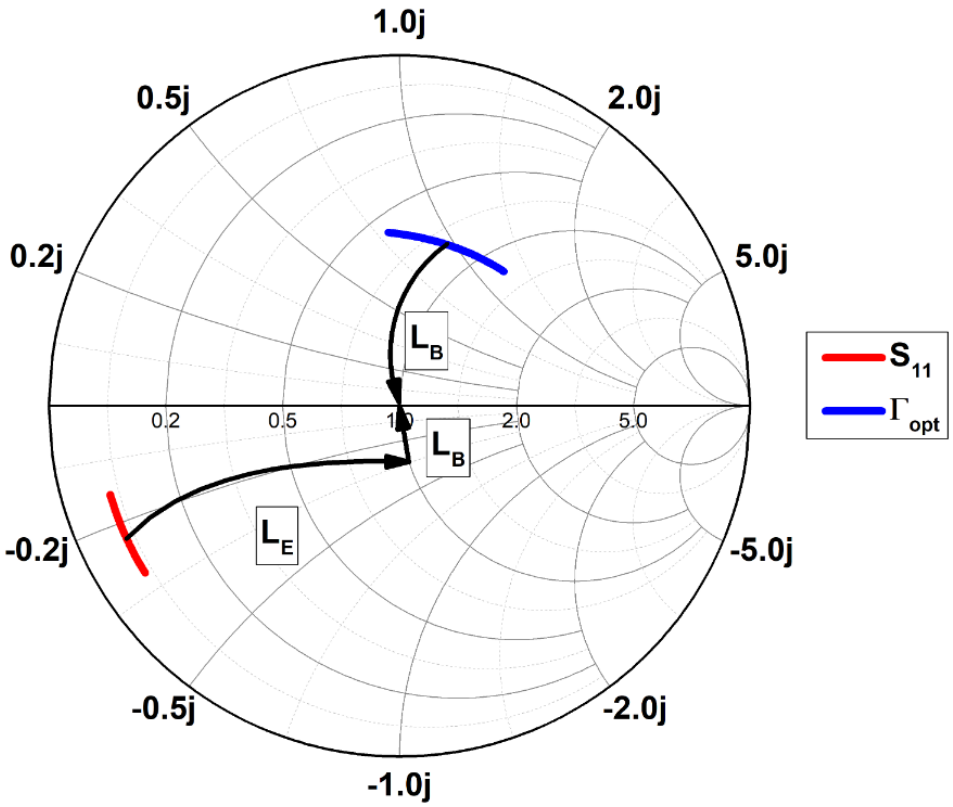

Figure 2.2 Conventional power and noise matching method for LNAs.

S_{11} is placed on the R=1 cycle, and finally, with a series base inductor, S_{11} is pushed to the center of the Smith Chart as shown in Fig. 2.2.

In this work, instead of using the conventional simultaneous power and noise matching method, the number of transistors of the common-emitter device of the first cascode stage is selected to enable input matching without using an inductor in the input matching network. For inductively degenerated cascode amplifiers, the input impedance is given in Eqn. (2.1). L_e represents the inductance at the emitter of the transistor.

$$Z_{in}(\omega) = \frac{r_\pi}{1+(\omega C_\pi r_\pi)^2}(1+\omega^2 g_m C_\pi r_\pi L_e + j(\omega g_m L_e - \omega C_\pi r_\pi)) + j\omega L_e. \tag{2.1}$$

Eqn. (2.1) shows that by carefully selecting L_e and the number of transistors of the common-emitter device at the first stage of the amplifier, the input of the amplifier can be matched to 50-Ω. The main reason for this approach is to eliminate the inductors in the input matching network because of their lossy and noisy behavior that arises from their parasitic resistances. Since simultaneous power and

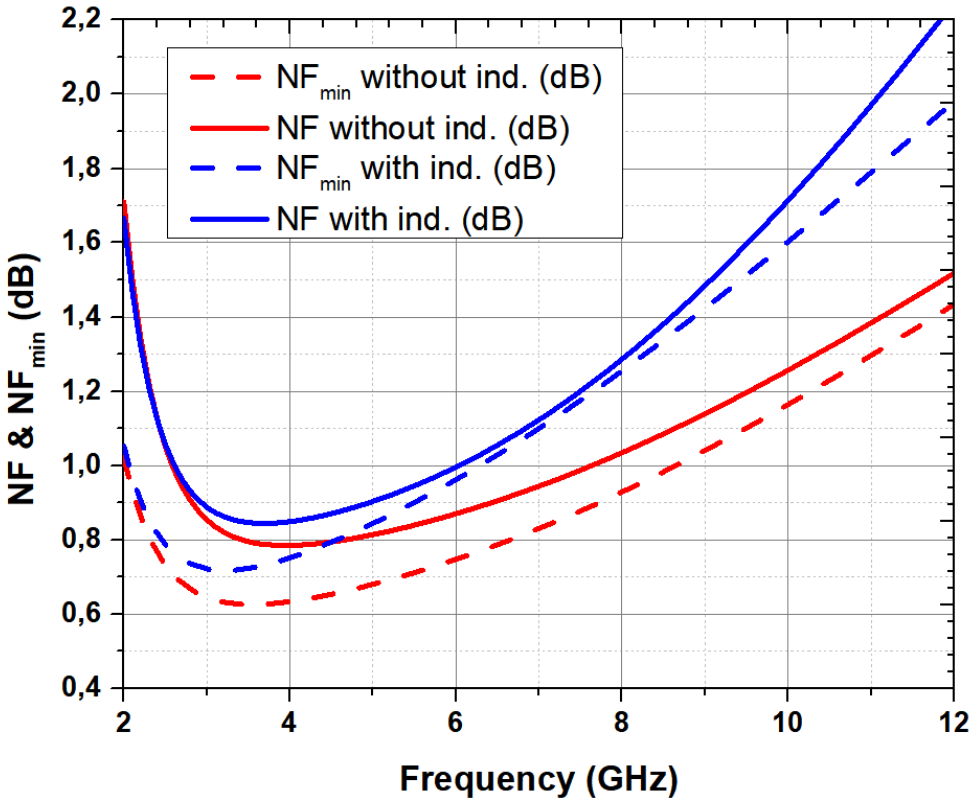

Figure 2.3 NF & NF_{min} for different input matching methods.

noise matching is not achieved in this approach, the difference between the NF and the NF_{min} is significantly higher with respect to the conventional technique. However, this method improves NF and obtains a lower NF than the conventional noise matching method. The NF difference between these two approaches is around 0.1 dB at GHz, and this gap widens as operating frequency increases. The comparison between the conventional and the modified method can be seen in Fig. 2.3. Both matching methods use inductors with the same Q-factors on the schematic level simulation.

2.3.2 Cascode Amplifier

The schematic of the LNA is shown in Fig. 2.4. Both stages of the LNA are designed in cascode topology, and cascode amplifier topology introduces high isolation between its output and input, which enables input matching with negligible effects from the output. For the second cascode stage, a higher inductively degeneration is used to increase its linearity since the overall amplifier's linearity is mainly dominated by the second stage.

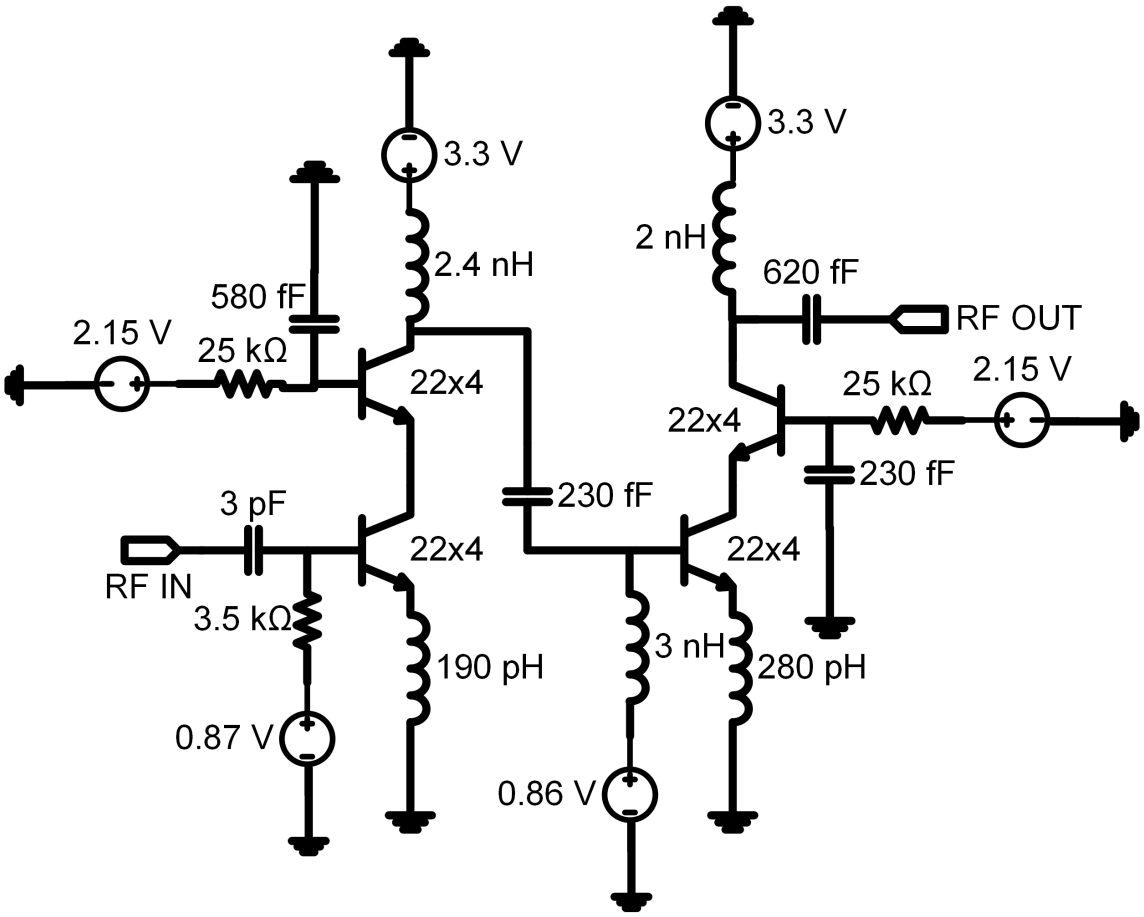

Figure 2.4 Schematic of the designed LNA.

At the base node of both common-base transistors, relatively low shunt capacitors are used, and base bias is applied over a highly resistive resistor. This method is applied to see significant impedance from the base node of these transistors instead of creating RF shorts at those nodes. The main aim of the method is to create a voltage swing at the base of these transistors to increase linearity (Rostomyan, Torii, Alluri & Asbeck, 2019). The effect of the selected capacitance on the IIP3 performance of the amplifier can be seen in Fig. 2.5. Decreasing the capacitance at the base node increases IIP3 monotonously, but as the capacitance decrease, S_{21} also decreases, making the base node's capacitance selection a trade-off between S_{21} and IIP3. Therefore, for an optimum and balanced design, a maximum S_{21} and IIP3 product (OIP3) should be considered during capacitance selection. For the second stage, OIP3 is maximized when the mentioned capacitance is selected as 230 fF.

Inter-stage and output matching is done using conventional methods using shunt inductors and series capacitors, which are also used for DC feeding and blocking purposes.

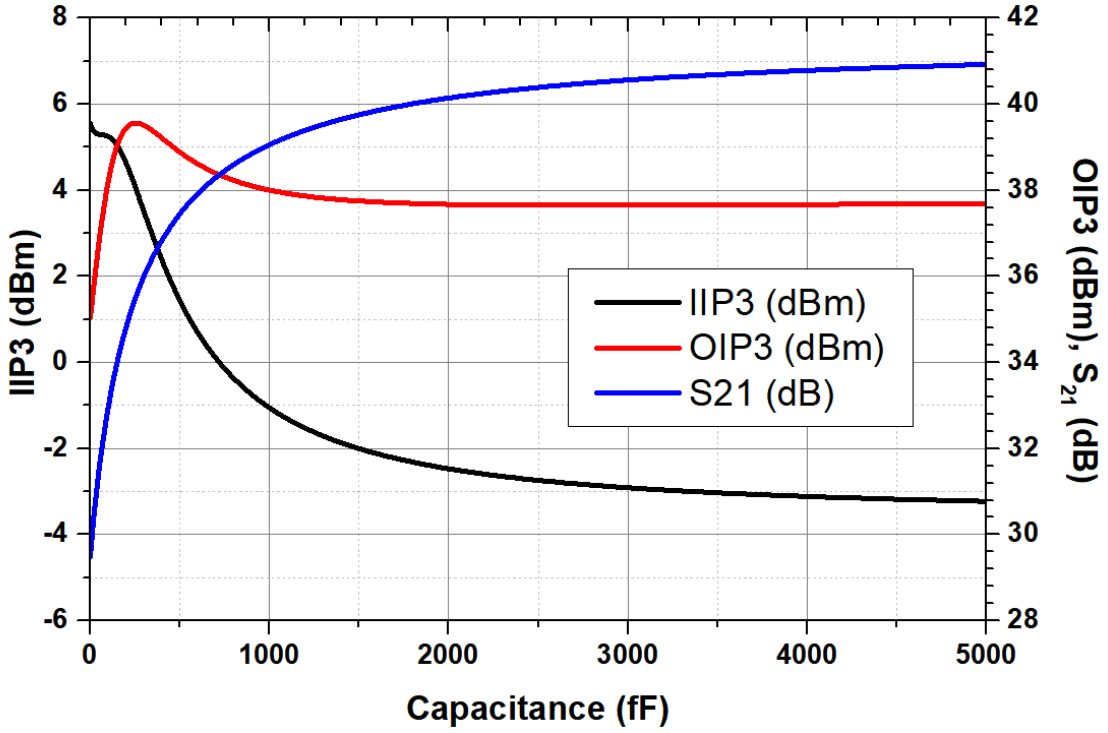

Figure 2.5 IIP3 vs. Capacitance characteristic.

2.3.3 Layout Optimization

HBTs in the IHP 130 nm SiGe BiCMOS technology have a restriction for a maximum number of transistors of eight in a single active region. If more than eight transistors were used in a single device, there should be spacing between these groups of transistors seen in Fig. 2.6. Since restriction of the number of the transistors would lead to a bigger active area and longer metal lines, NF would have increased due to increased parasitic capacitance and resistance. The mentioned restriction is avoided by redrawing active areas to create transistor groups larger than eight transistors to prevent this NF increase. In this work, all devices have 88 transistors, and 22 transistors are used per active region row for each device for an optimal layout. Core layout optimization can be seen in Fig. 2.6. Since the base signal is applied from the left side, transistors on the right side see more resistance with respect to closer transistors in the pre-optimization case. In the post-optimization case, these transistors see less parasitic resistance and capacitance due to decreased distance, which decreases the NF. Change in the NF is shown in Fig. 2.7. At 6 GHz, simulated NF is decreased by 0.05 dB. Although the NF difference may not be significant, there is no cost for the core layout optimization, and the optimization also decreases the core area, and it is applicable to other works with the same technology.

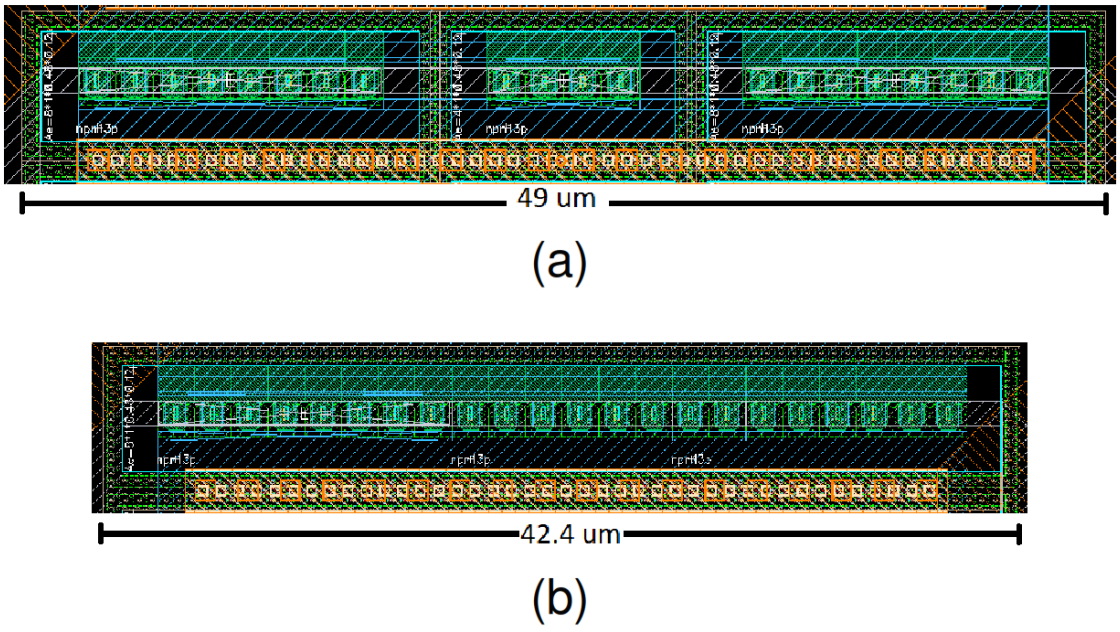

Figure 2.6 (a) Pre-layout optimization, (b) Post-layout optimization without an LVS and DRC violation.

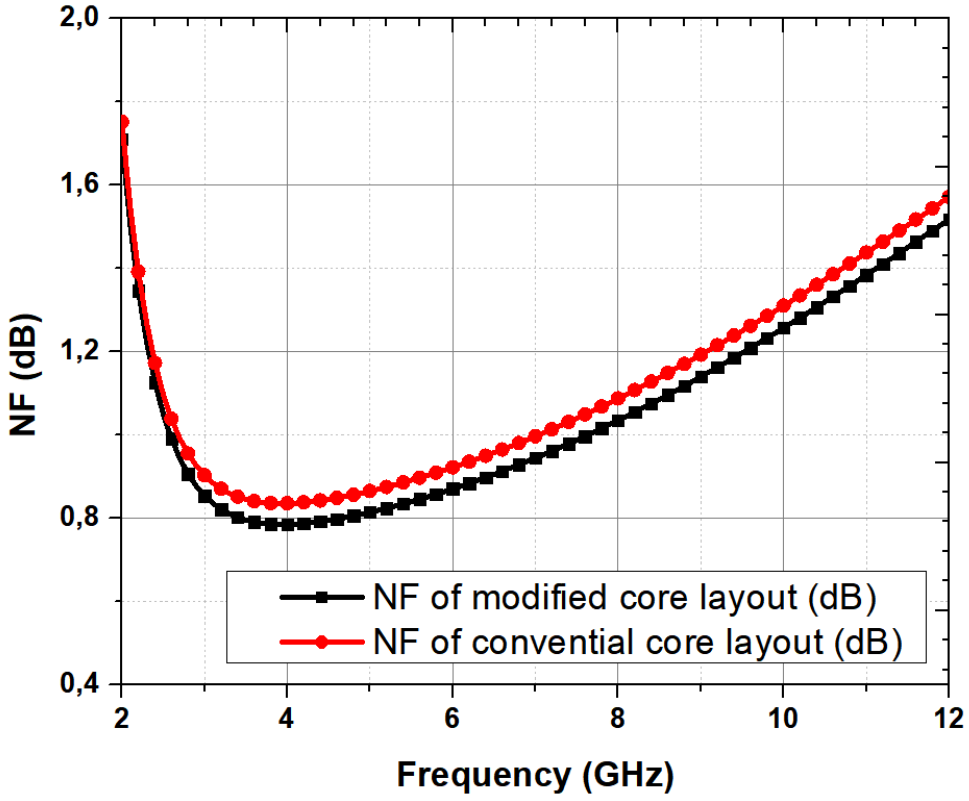

Figure 2.7 NF of conventional and modified transistor of the used technology.

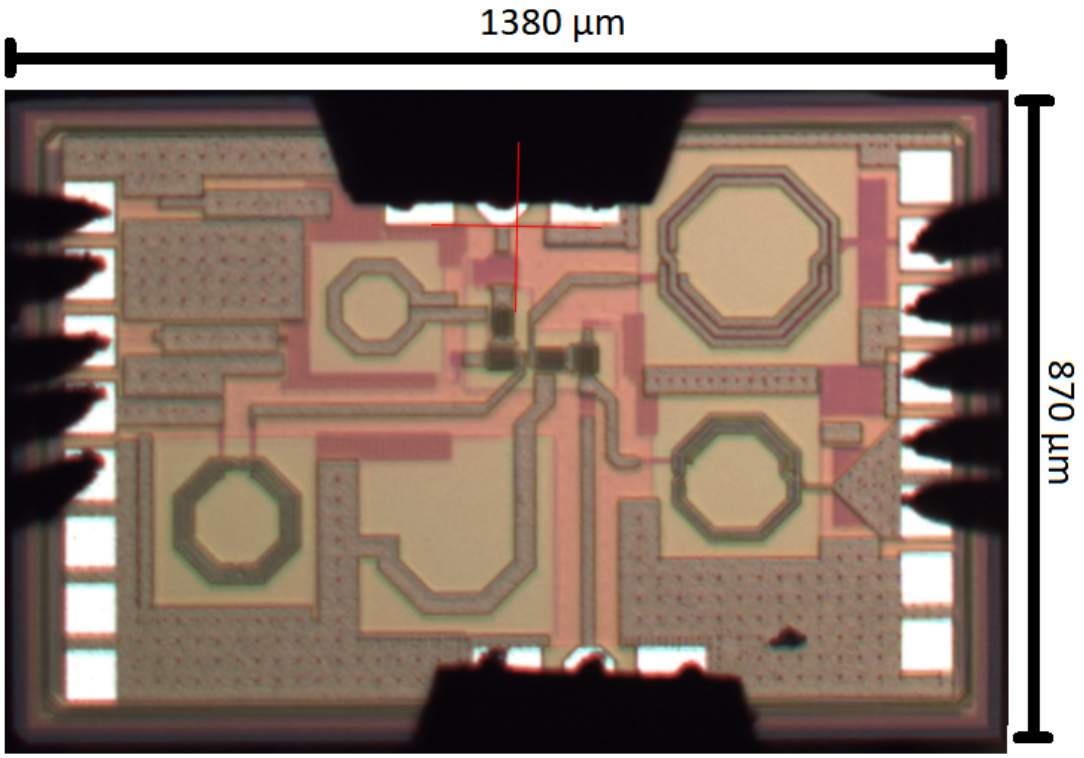

Figure 2.8 Chip photo of the two-stage cascode LNA. Total die area is 1.2 mm^2 with pads. The area without pads is 0.75 mm^2.

2.3.4 Measurement Results

This work is sent for tape-out and fabricated in IHP 130 nm SiGe BiCMOS technology. The chip photograph of the reported LNA is shown in Fig. 2.8. The chip area without pads is 0.75 mm^2. The S-parameters are measured from 3 GHz to 10 GHz with Cascade Microtech 40 GHz GSG probes by using Keysight N5224A PNA. The measurement setup for the S-parameters are shown in Fig 2.9. Noise figure measurement is conducted for the 4-10 GHz region by using Keysight E4448A PSA and 346A noise source. Noise figure measurement setup is shown in Fig 2.10. OIP3 and OP1dB performances of the LNA are measured from 4 GHz to 7 GHz by using Keysight E8257D PSG and E4448A PSA. Measurement setup for linearity is shown in Fig. 2.11.

S_{11} and S_{22} measurement results are shown in Fig. 2.12, and input and output matchings are better than -10 dB between 5.8-9.8 GHz. The measurement result of the output matching was similar to its simulation result. On the other hand, a frequency shift has been observed at the input side. Input matching's lower frequency limit had been shifted from 5 GHz to 5.8 GHz, which is addressed to the input pad's parasitic capacitance. The measured small-signal gain (S_{21}) has reached 34 dB at 4

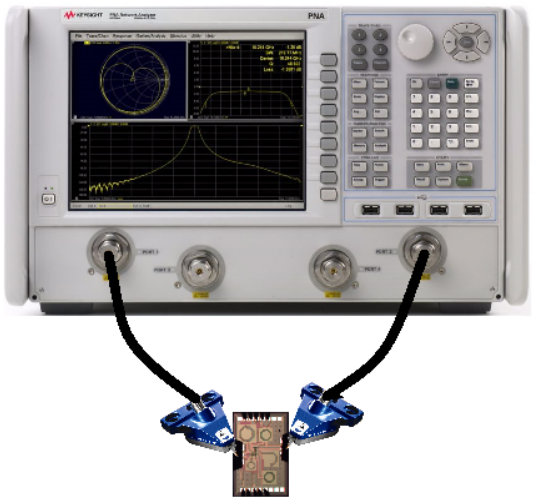

Figure 2.9 S-parameter measurement setup of the LNA.

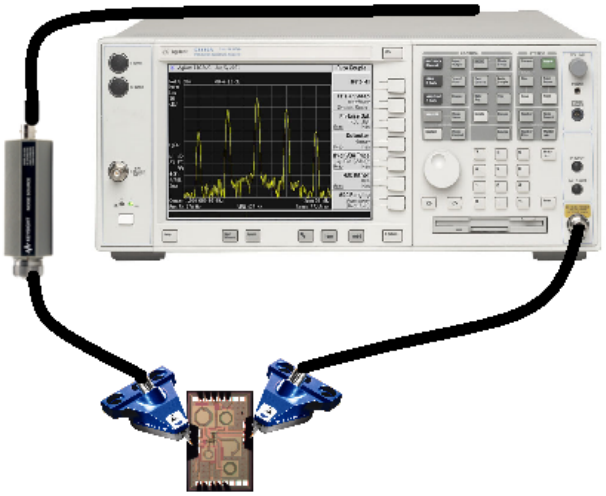

Figure 2.10 Noise figure measurement setup of the LNA.

GHz and was recorded as 27.7 dB at 6 GHz, as shown in Fig. 2.13.

The noise figure reached its lowest value, 1.05 dB at 4 GHz, and measured as 1.15 dB at 6 GHz. NF is smaller than 2 dB for the matched frequency region. However, an NF increase has been observed at the low-frequency region due to the input matching shift between 4-6 GHz. The NF measurement result can be seen in Fig. 2.14.

OIP3 measurement is done by applying two tones centered around the center frequency and the frequency spacing between the tones was selected as 10 MHz. OIP3 was measured as 31.9 dBm at 6 GHz and reached its highest value of 33 dBm at 5 GHz. Thus, the measurement result ensures a highly linear operation. Finally, the OP1dB was measured as 14.5 dBm at 6 GHz, which is a very high OP1dB value for LNAs, and it is characterized with the SiGe BiCMOS cascode amplifiers. Linearity

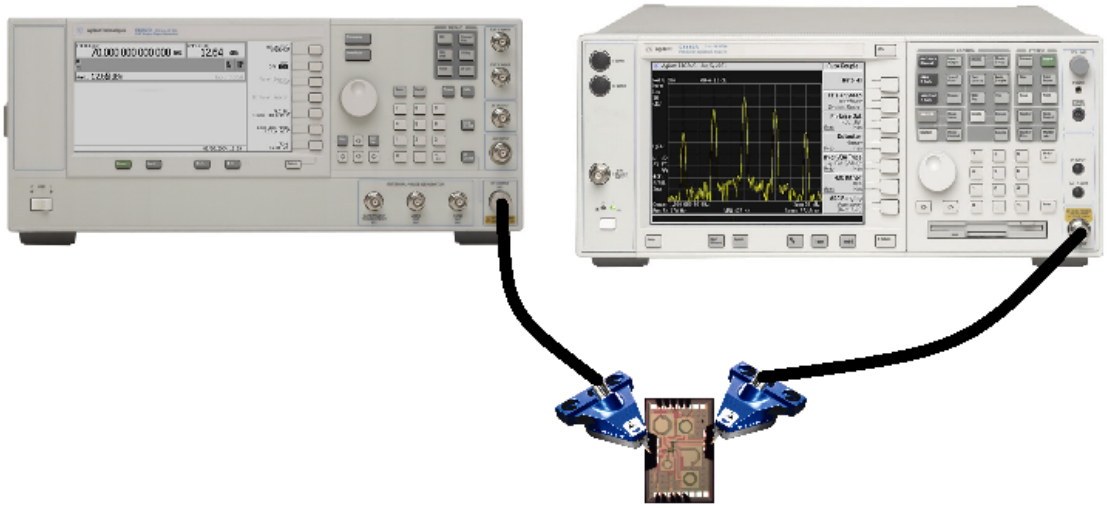

Figure 2.11 OIP3 and OP1dB measurement setup of the LNA.

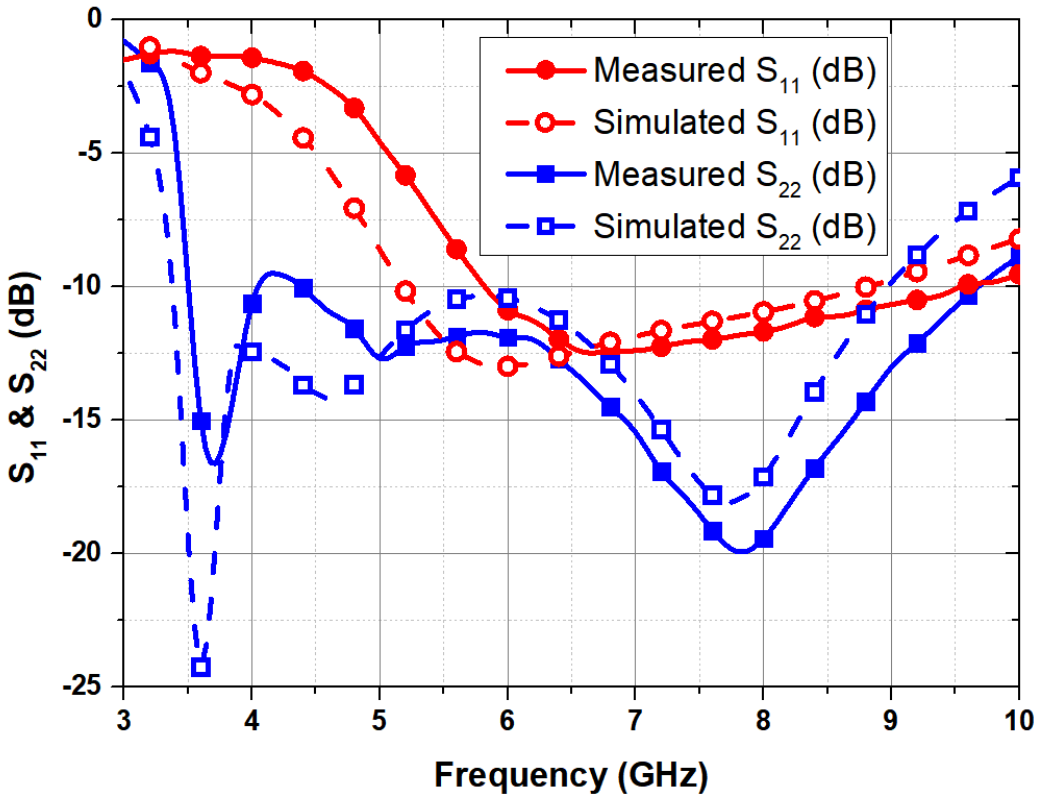

Figure 2.12 Measured and simulated S_{11} & S_{22} of the LNA.

measurement results are shown in Fig. 2.15.

Moreover, the reported LNA performed stable operation and no oscillation was observed when the LNA's output is analyzed with the spectrum analyzer.

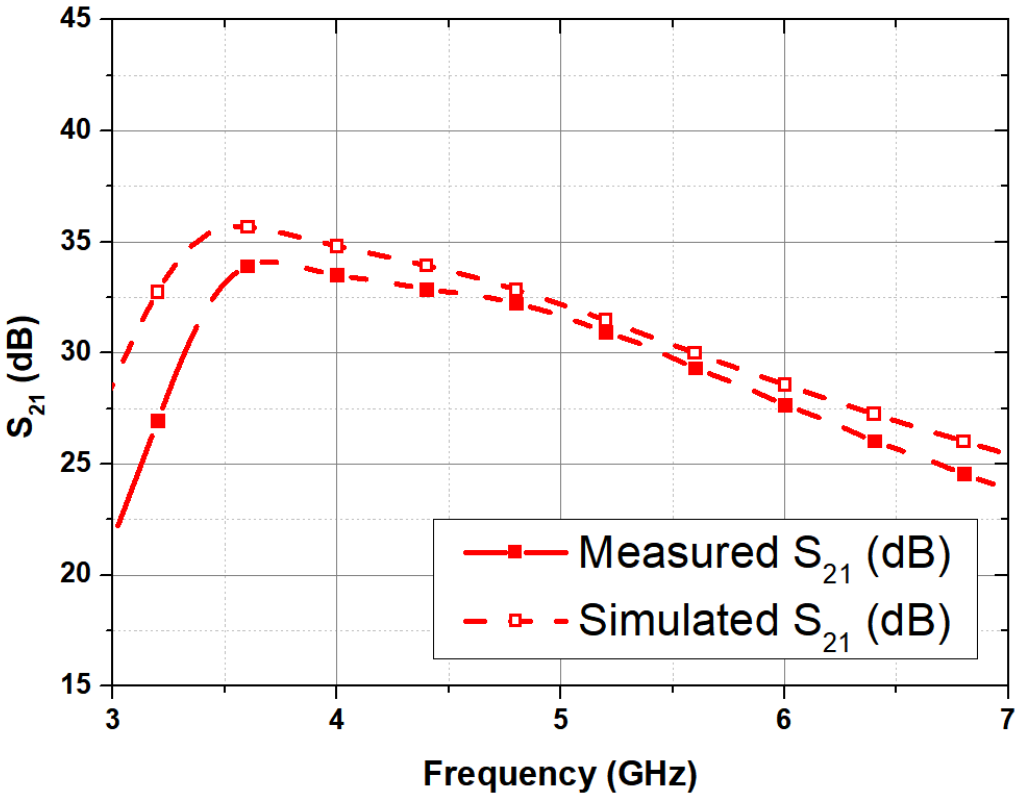

Figure 2.13 Measured and simulated S_{21} of the LNA.

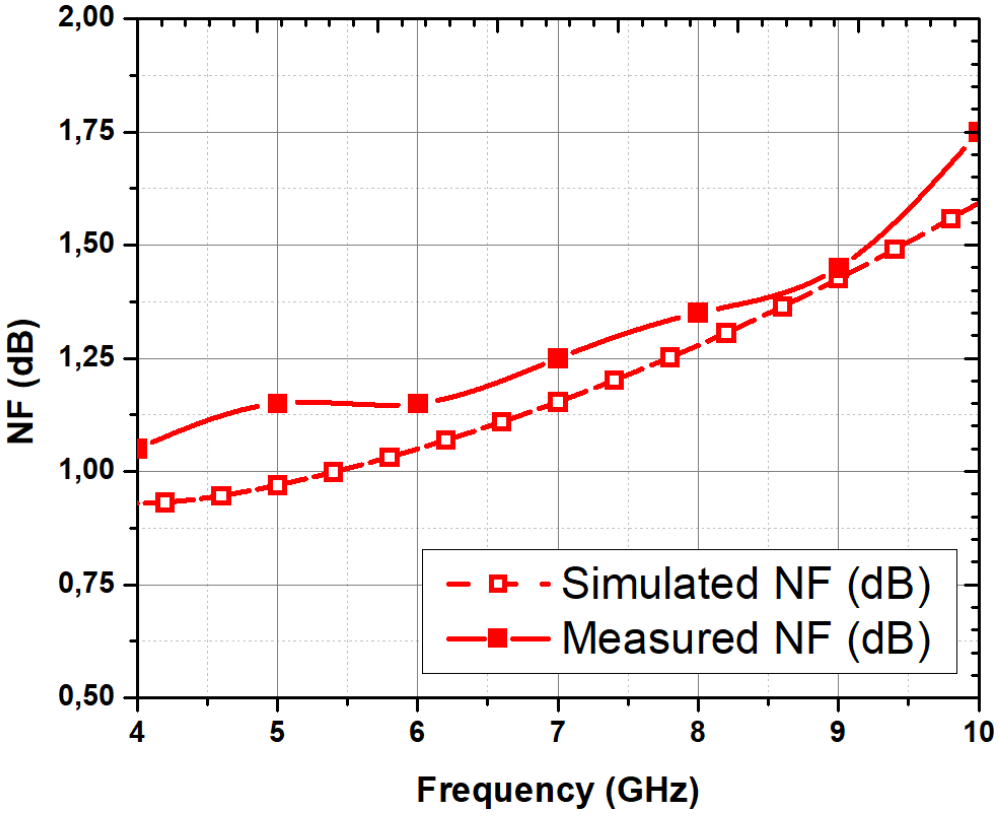

Figure 2.14 Measured and simulated noise figure result of the LNA.

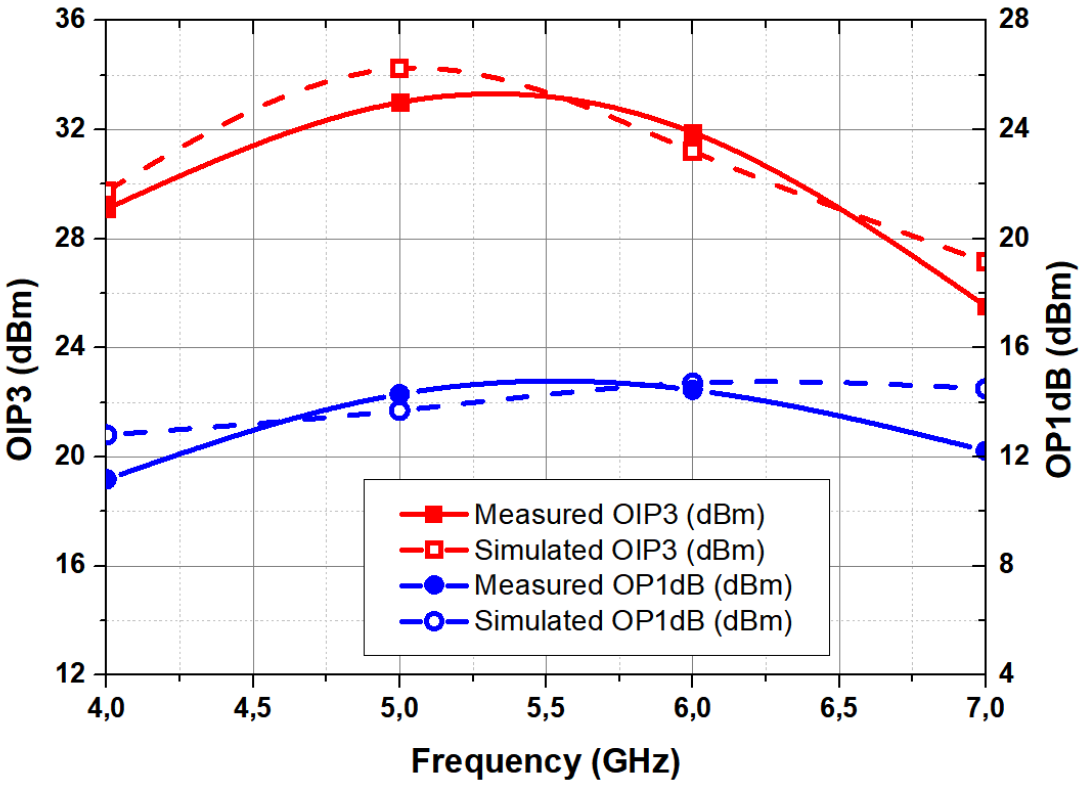

Figure 2.15 Measured and simulated OIP3 and OP1dB results of the LNA.

2.3.5 Comparison

Measurement results of this work are summarized in Table 2.1 and compared with the other state-of-the-art silicon-based LNAs (Crippa, Orcioni, Ricciardi & Turchetti, 2003; Han, Gil, Song, Han, Shin, Kim & Lee, 2005; Jha, Zheng, Masse, Hurwitz & Chaudhry, 2020; Madan, McPartlin, Masse, Vaillancourt & Cressler, 2012; Paulin, Cathelin, Bertrand, Monroy, More-He & Schwartzmann, 2016; Sturm, Popuri & Xiang, 2014; Subramanian, Krcmar, Deen & Boeck, 2008). Two different figures-of-merits are used for comparison. FoM_1 compares gain IIP3, f_c, NF, and DC power consumption (Sturm et al., 2014).

$$FoM_1 = \frac{Gain[abs] \times IIP3[mW] \times f_c[GHz]}{(F-1)[abs] \times P_{DC}[mW]}. \tag{2.2}$$

while FoM_2 compares gain, IP1dB, f_c, NF, and DC power consumption (Çaışkan, Kalyoncu, Yazici & Gurbuz, 2019).

$$FoM_2 = \frac{Gain[abs] \times IP1dB[mW] \times f_c[GHz]}{(F-1)[abs] \times P_{DC}[mW]}. \tag{2.3}$$

This work achieves one of the highest figures-of-merit, and lowest NF with respect to state-of-the-art SiGe BiCMOS LNAs and has one of the highest figure-of-merits compared to state-of-the-art Si-based LNAs.

Table 2.1 Comparison of State-of-the-art LNAs.

Reference	**This Work**	Sturm et al. 2014	Jha et al. 2020	Crippa et al. 2003	Madan et al. 2012	Paulin et al. 2016	Han et al. 2005	Subramanian et al. 2008
Technology	**130nm SiGe**	65nm CMOS	130nm SOI	250nm SiGe	180nm SOI	130nm SOI	180nm CMOS	180nm SiGe
Freq (GHz)	**6**	5.8	5.2	5	5	5.8	5.2	5.8
NF (dB)	**1.15**	1.9	0.6	2.2	0.95	1.34	1.1	2
Gain (dB)	**27.7**	30	10.4	12.8	11	9	16.5	18.8
IIP3 (dBm)	**4.2**	-10.3	12	11.6	5	12.7	-4	-6
IP1dB (dBm)	**-12.2**	-21.6	N/A	-6.2	-7	-2	-19.9	-14.5
Area (mm^2)	**0.75**	0.03	0.6	N/A	0.29	0.85	0.22	0.72
P_{DC} (mW)	**98**	16	10	23.8	12	9.6	12.4	32.4
FoM_1 (GHz)	**312.78**	61.64	609.95	87.84	67.84	251.5	25.87	5.83
FoM_2 (GHz)	**7.17**	4.57	-	1.46	4.28	8.52	0.66	0.82

2.4 Wideband Low Noise Amplifiers in 130nm SOI CMOS

2.4.1 Input Matching

One of the most demanded specifications of an LNA is having wideband input and output matching without compromising the power gain and noise performance. A wideband output matching can be achieved very easily for the LNAs by using a shunt 50-Ω at the output side without hurting the gain too much and increasing the NF a lot if the gain of the LNA is very high. On the other hand, using a shunt 50-Ω at the output side also degrades the linearity performance of the LNA; therefore, it may not be the optimal solution for wideband applications. Apart from the matching of the output side, input matching of the LNA is more problematic, in general. The complexity of the input matching comes from the necessity of having both power matching and noise matching at the same time. For an inductively degenerated common-source (CS) device, the input impedance is given in Eqn. (2.4) and from the Eqn. (2.4) it can be seen that the input of the CS device can be power matched by properly selecting the degeneration inductor, L_s, however, this method does not guarantee noise matching. To have a noise matching and achieve the lowest possible NF, device size should also be scaled properly to have a Y_{opt} equal to Y_s as shown in Eqn. (2.5).

$$Z_{in} = \frac{1}{j\omega C_{GS}} + j\omega L_s + \frac{g_m L_s}{C_{GS}}. \tag{2.4}$$

$$F = F_{min} + \frac{R_n}{G_s}|Y_s - Y_{opt}|^2. \tag{2.5}$$

Many techniques have been demonstrated in the literature to achieve wideband input matching. One of the most commonly used techniques is resistive feedback topology which utilizes a resistor that is connected between the gate and drain nodes of the CS device to decrease the input impedance by creating a feedback loop as

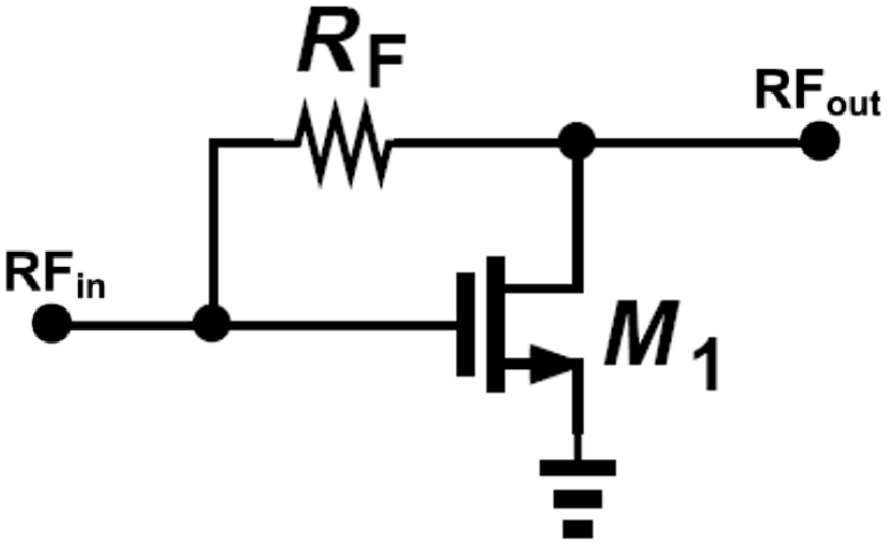

Figure 2.16 Common-source amplifier with resistive feedback.

shown in Fig. 2.16. The most significant disadvantage of this topology is that the feedback resistor creates noise at the input side of the LNA, thus, increasing the F_{min} effectively. With this topology, even though noise matching is established, the overall NF would get increased due to having a higher $\mathrm{NF_{min}}$.

Another commonly used topology is the common-gate amplifier (CG) topology, where the RF signal is fed to the amplifier from the FET device's source node, which is shown in Fig. 2.17. In this amplifier configuration, the input impedance can be found from Eqn. (2.6). According to Eqn. (2.6) input impedance of a CG amplifier can be set to 50-Ω by setting bias voltage and device size properly. However, this approach does not yield either the lowest possible $\mathrm{NF_{min}}$ or noise matching. Moreover, the CG configuration generally tends to have higher $\mathrm{NF_{min}}$ and lower power gain than the CS configuration. Therefore, even though CG amplifiers achieve very wide input matching, they suffer from high NF and low gain, which makes this amplifier topology unfavorable when the noise performance of the overall receiver system is considered.

$$Z_{in} = \frac{r_o}{1 + g_m r_o}. \tag{2.6}$$

Finally, the most commonly used technique is implementing an input matching network to achieve power and noise matching at the same time. By implementing a matching network, high gain and noise matching are achievable; however, due

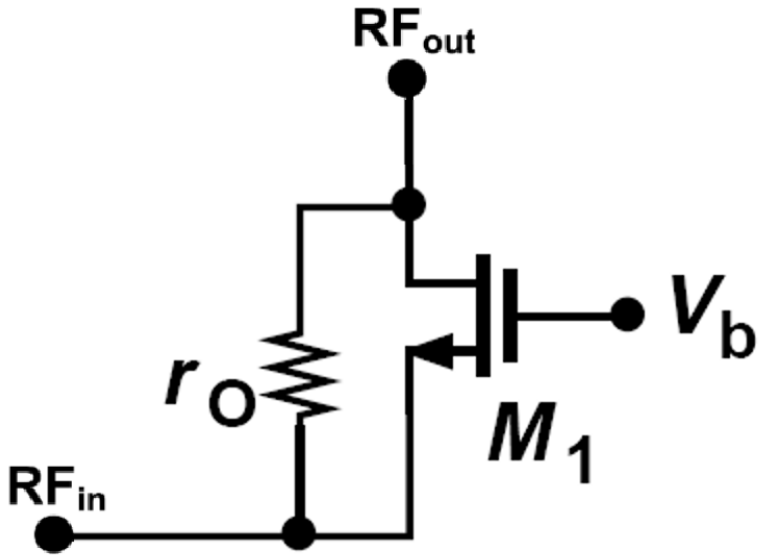

Figure 2.17 Common-gate amplifier topology.

to the lossy behavior of the on-chip inductors and capacitors, matching networks cause losses and increase the NF. Moreover, to have an input matching over a wide bandwidth, a matching network should consist of several components, which means higher complexity matching networks must be designed for wider bandwidths. This situation results in the utilization of more on-chip passive components, which leads to increased NF, lower gain, larger die area, and cost. Due to the disadvantages of on-chip matching networks, in this work, off-chip wirebonds are used in the input matching network, and on-chip inductors are mostly avoided to have the best noise performance over a very wide bandwidth. 3D visualization of the series gate wirebond, WB_G, and series source wirebonds, WB_S, are shown shown in Fig. 2.18. Due to the design choice of having around 130 pH inductance at the source node, 4 wirebonds are parallel connected to decrease the effective inductance value at the source node. The used wirebonds can be modeled as a 3^{rd} order low-pass filter with capacitor-inductor-capacitor configuration as shown in Fig. 2.19. The EM simulated wirebonds are modeled according to the wirebond model, and their modeled capacitance and inductance values are given in Table 2.2. The approximate length for the gate wirebond is around 2.5 mm and 0.4mm for the source wirebonds.

Table 2.2 Lumped component values for lumped wirebond model.

Wirebond Name	**Number of Wirebond**	$\mathbf{C_{package}}$	$\mathbf{C_{pad}}$	$\mathbf{L_{wirebond}}$
Gate Wirebond	1	225 fF	2 nH	130 fF
Source Wirebond	4	N/A	170 pH	130 fF

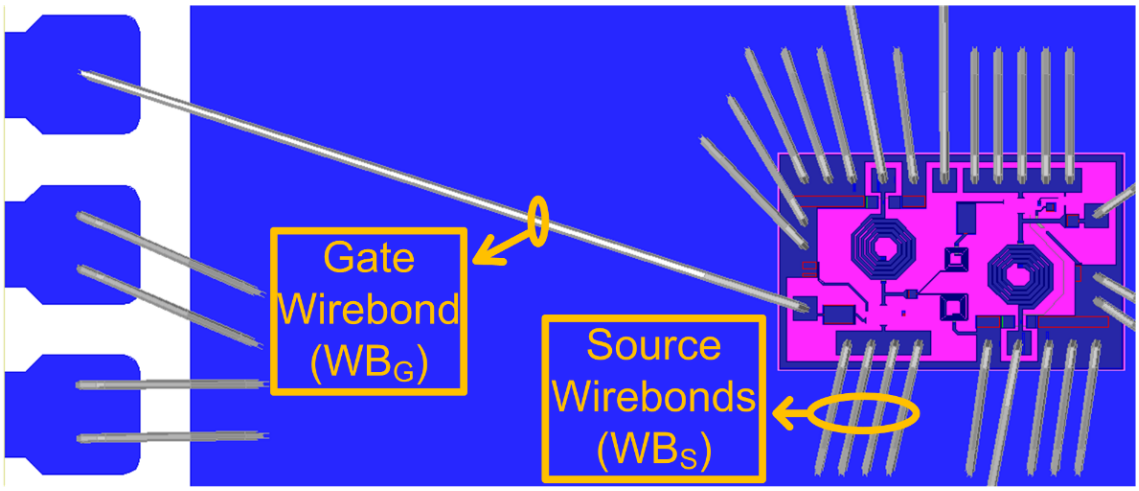

Figure 2.18 Wirebonds in the input matching network.

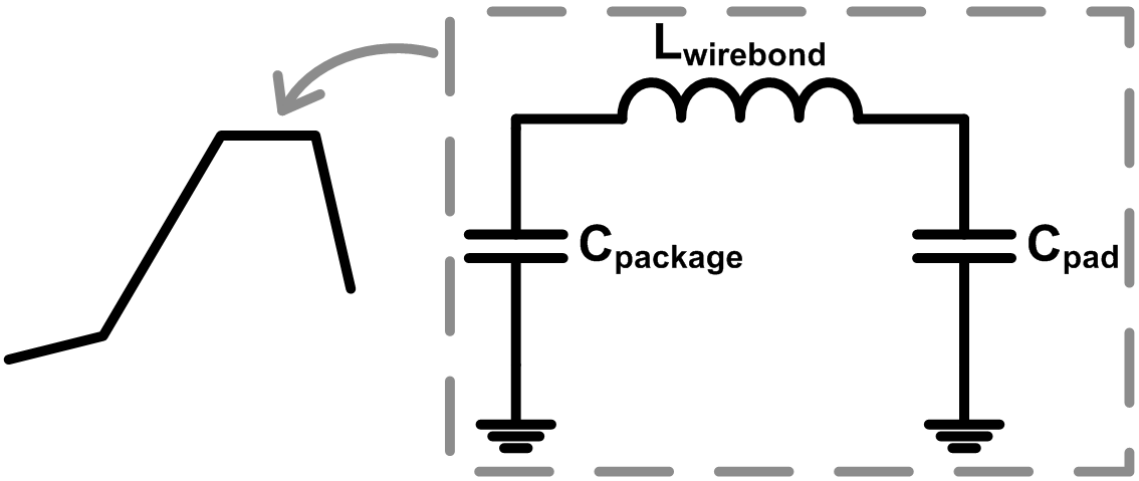

Figure 2.19 Wirebond lumped component model.

2.4.2 Amplifier Design

Since the linearity of a receiver is a critical aspect due to the existence of in-band interferers, LNA's linearity performance becomes more important. Hence, in this work, two different LNA versions are designed, which utilize different OIP3 improvement methods. These two versions share the main amplifier block; however, they use different auxiliary amplifiers to cancel 3^{rd} order inter-modulation products (IM3). The schematic of the main amplifier block is shown in Fig. 2.20. In Fig. 2.20 wirebonds are shown with a symbol of an inductor with a box, and the equivalent inductance of the wirebonds is modeled and written.

The amplifier stage consists of a two-stage cascode amplifier to have a high gain which is critical when the noise suppression and the overall NF of the receiver are considered. Due to the noise penalty of cascode topology with respect to the CS topology, all other noise sources' effects are minimized by having an optimized

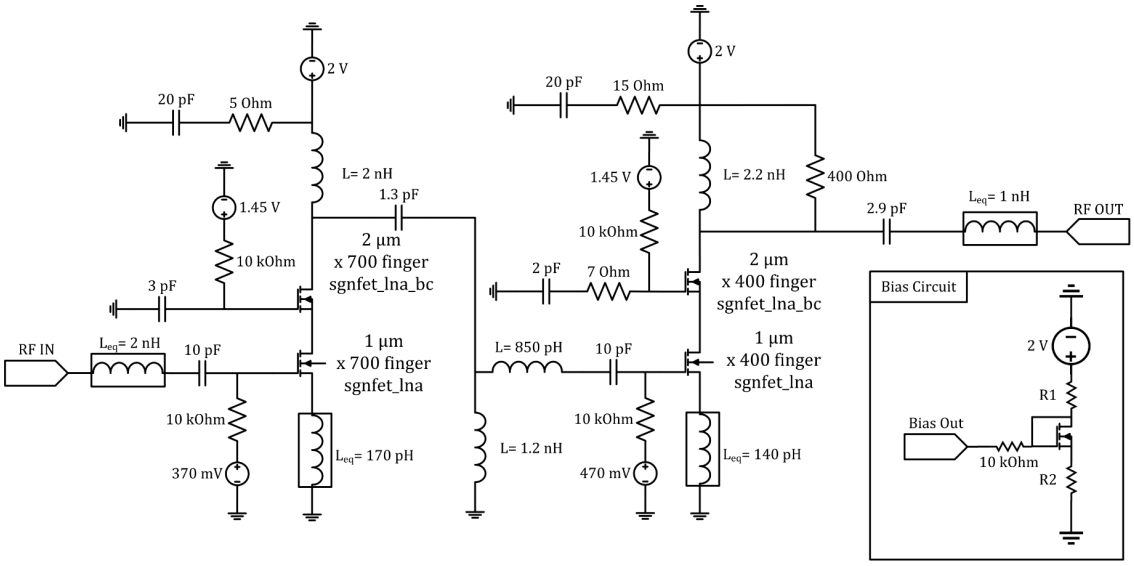

Figure 2.20 Amplifier stage of the designed SOI LNAs.

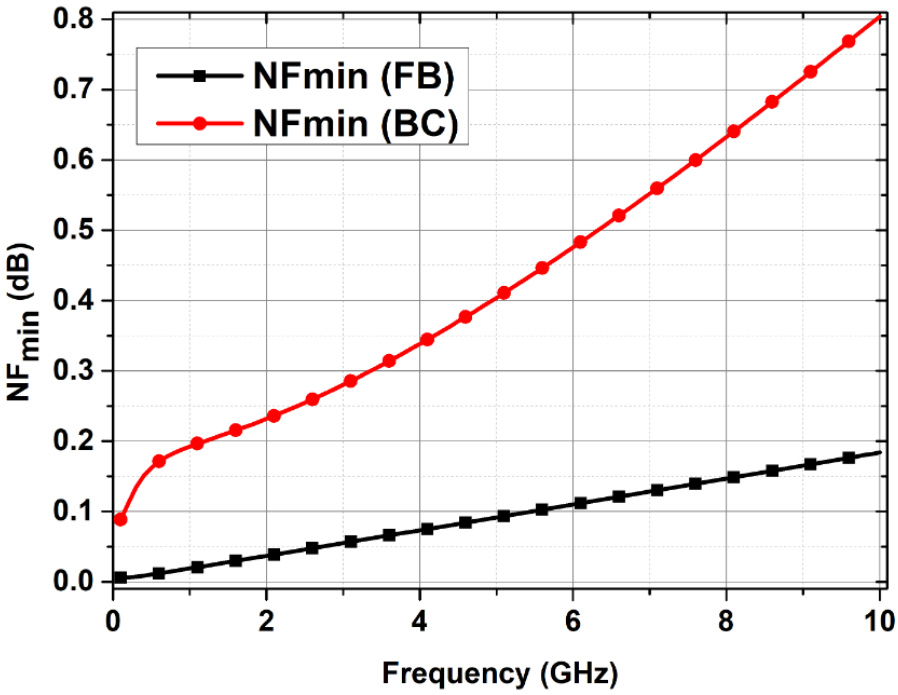

Figure 2.21 NF_{min} of FB and BC FETs at their respective optimum current density.

design. First of all, cascode amplifiers' CS devices are designed by using the floating-body (FB) transistors instead of body-contacted (BC) transistors since the floating-body transistors achieve higher f_T and f_{max} due to lacking parasitic capacitances of the body node. Therefore, this transistor type is more advantageous for LNAs due to having lower NF_{min} as shown in Fig. 2.21. where transistors are biased such that the minimum possible NF_{min} is obtained for each transistor type.

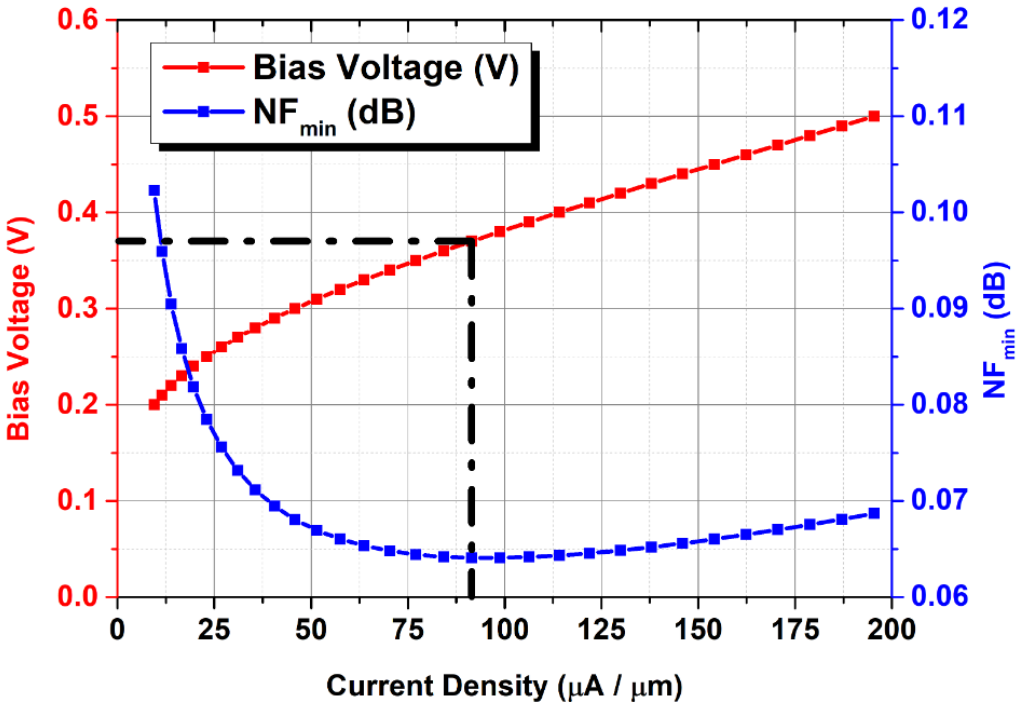

Figure 2.22 The relationship between the NF_{min}, bias voltage and the current density of FB FET.

Secondly, the bias voltage of the first CS device is chosen accordingly after finding the optimum current density that makes it possible to obtain the lowest NF_{min}. The relationship between the NF_{min}, current density and the bias voltage is shown in Fig. 2.22.

For the selected bias voltage, the device size of the CS device should be selected for the best NF performance. Since the high-Q wirebonds are available for the input matching network, very low NF is achievable with the conventional noise and power matching method. However, due to the physical limitations, the maximum length and equivalent inductance of the wirebond at the input is limited, which may restrict the application of the conventional method. Because of this, the device size of the CS device is selected according to Eqn. (2.4). According to Eqn. (2.4) as the device size of the CS device increases (i.e., C_{GS} and g_m increase) real part of the input impedance remains constant; however, the imaginary part increases, which is similar to increasing the series gate inductance. A similar effect can also be realized by connecting an external capacitor between the gate and source nodes of the CS device, although, with this approach, the real part of the input impedance decreases, which is already smaller than 50-Ω in general and causes NF and power gain penalty. Therefore, in this work, the device size of the CS device of the first cascode stage is

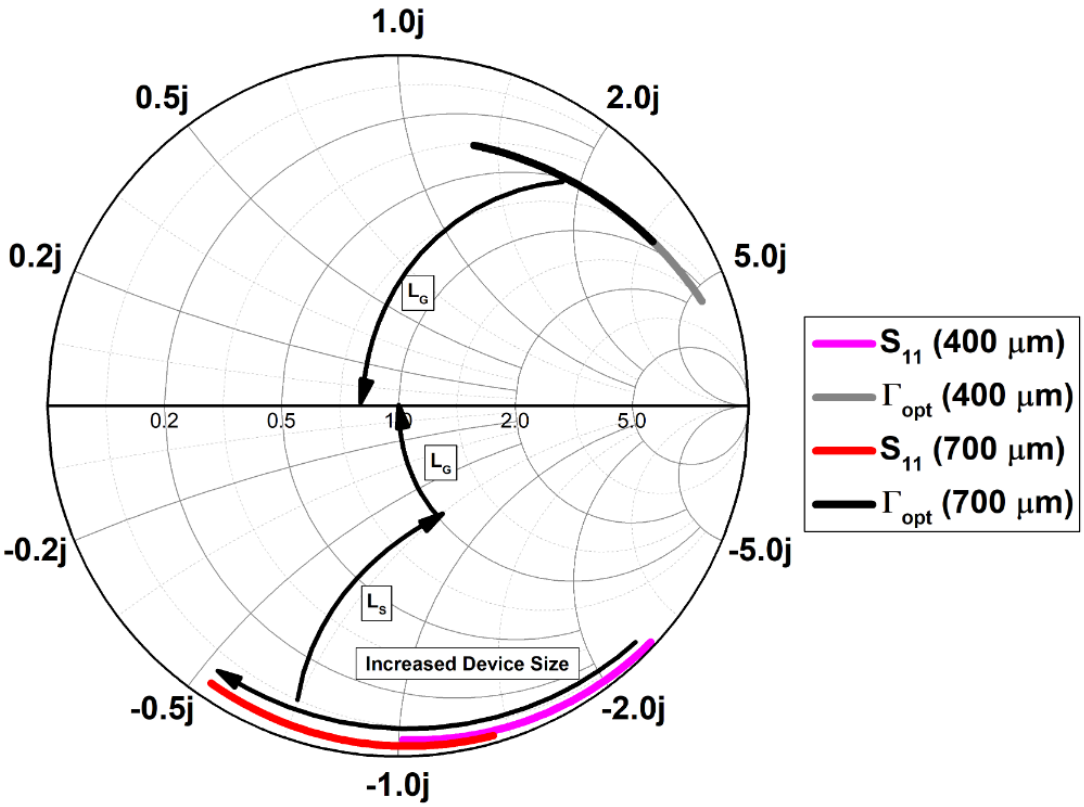

Figure 2.23 S_{11} and Γ_{opt} for CS devices with 700 μm and 400 μm device width.

selected as 700μm instead of 400μm, which is the optimum device size that places the Γ_{opt} of the center frequency on the R=1 cycle on the Smith Chart. S_{11} and Γ_{opt} of the CS device with a size of 700μm and 400μm are shown in Fig. 2.23.

Moreover, to increase the stability and the linearity performance of the LNA, wire-bonds are used at the source node of the CS devices, which act as degeneration inductors. Another improvement in the stability is achieved by using de-coupling resistors, which are connected in series to bypass capacitors are supply nodes and the gate node of the CG device at the second cascode amplifier. Due to de-coupling resistors, the Q-factor of the capacitors is significantly decreased, which introduces resistance-related loss to the node and decreases the chance of oscillation. The last stability improvement is obtained by choosing bypass capacitors at the gate node of the CG devices, not too large. If these bypass capacitors were chosen as very large capacitors, these gate nodes would be significantly RF-bypassed, which leads to higher power gain; however, choosing these capacitors as small capacitors creates a degeneration similar to degeneration at the source node of a CS device and improve the stability. Therefore, it can be stated that there is a trade-off between the power gain and stability when choosing these capacitors' sizes. In addition to stability, using small capacitors also improves the linearity of the amplifier, again, similar to the source degeneration case. Due to these reasons, 3 pF and 2 pF capacitors are

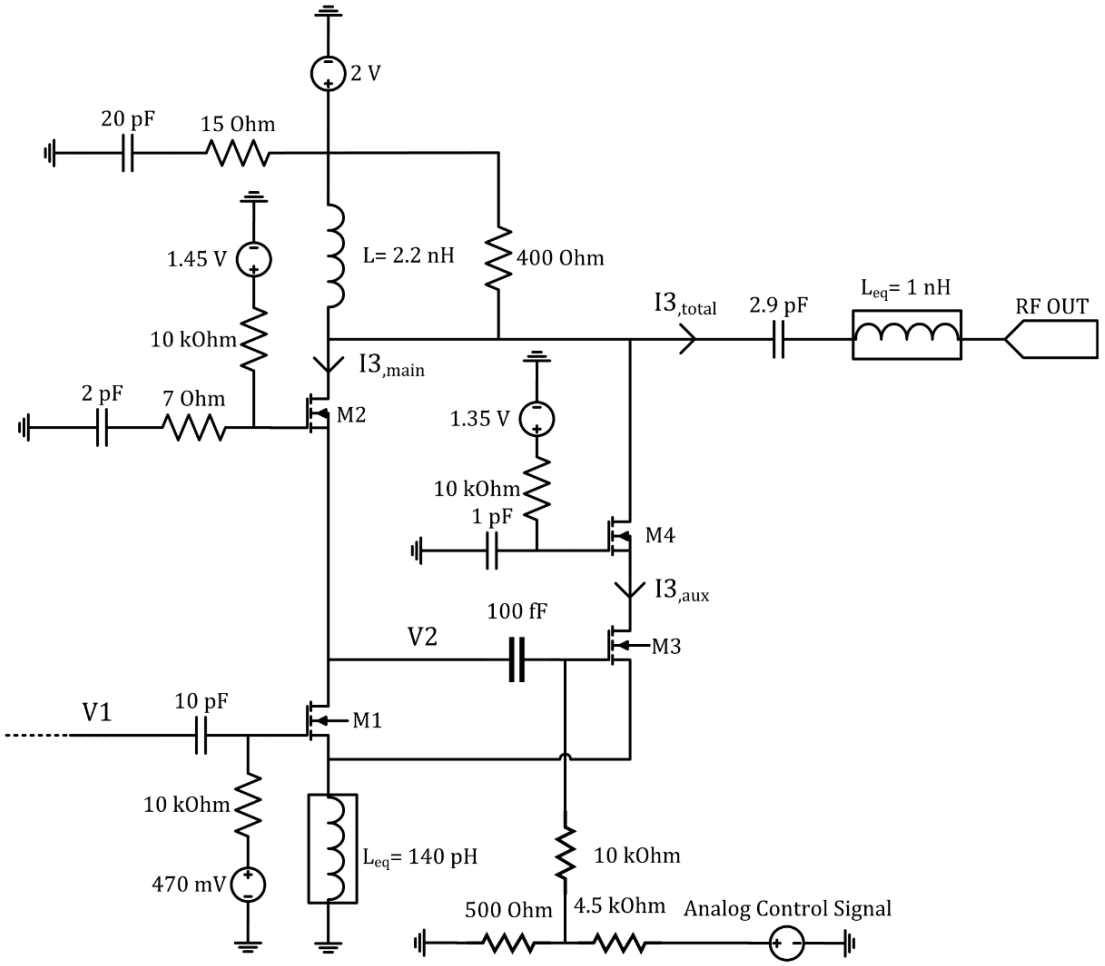

Figure 2.24 Cascode auxiliary post-distortion circuit with the second cascode amplifier stage.

used at the gate nodes as bypass capacitors.

2.4.3 Linearity Improvement

Two different improvement techniques are realized to improve the OIP3 performance and suppress the IM3 components. In the first technique, the post-distortion method has been used by designing an auxiliary cascode amplifier that is connected to the output of the LNA as shown in Fig. 2.24.

The generated current components of the M1 can be modeled by the Eqn. (2.7) where g_{m1} is the transconductance, $g_{m1}^{'}$ is the first-order derivative of g_{m1} and $g_{m1}^{''}$ is the second-order derivative of the g_{m1}. The inter-node voltage (V2) can be calculated by using the Eqn. (2.8). Assuming that M2 and M4 are linear transistors,

the current components of the M3 can be calculated by using the Eqn. (2.9). Finally, the fundamental tone and the 3^{rd} order signal component at the output can be found from Eqn. (2.10).

$$I_{main} = g_{m1}V1 + g_{m1}^{'}V1^2 + g_{m1}^{''}V1^3. \tag{2.7}$$

$$V2 = \frac{g_{m1}V1 + g_{m1}^{'}V1^2 + g_{m1}^{''}V1^3}{g_{m2}}. \tag{2.8}$$

$$I_{aux} = g_{m3}V2 + g_{m3}^{'}V2^2 + g_{m3}^{''}V2^3. \tag{2.9}$$

$$I1_{total} = g_{m1}(1 - \frac{g_{m3}}{g_{m2}})V1. \tag{2.10a}$$

$$I3_{total} = (g_{m1}^{''}(1 - \frac{g_{m3}}{g_{m2}}) - g_{m3}^{''}(\frac{g_{m1}}{g_{m2}})^3 - g_{m3}^{'}\frac{2g_{m1}^{'}g_{m1}}{g_{m2}^2})V1^3. \tag{2.10b}$$

Eqn. (2.10) indicates that $I3_{total}$ can be cancelled out by carefully selecting the g_{m2} and g_{m3}. However, this method also introduces small gain loss, which can not be avoided. Although, the gain loss can be minimized by selecting a small g_{m3} and an appropriate g_{m2}. The 3^{rd} order current components of the current at the output of the auxiliary circuit, main amplifier, and the whole LNA is shown in Fig. 2.25.

Since the g_m and parasitic capacitances depend on the frequency for high-frequency RF amplifiers, this post-distortion yields strong IM3 cancellation for a limited frequency range. To achieve a strong IM3 cancellation over a wide bandwidth between the 2 - 5 GHz, g_{m3} should be adjustable and set for the frequency of operation. This can be achieved through several methods. First of all, several devices can be connected with switches and form a transistor bank where switches are controlled digitally and required g_{m3} is obtained by turning on or off the switches. This method can be applied by dividing the frequency range into smaller ranges, and for each range, an appropriate g_{m3} would be selected. Afterward, the transistor bank can be

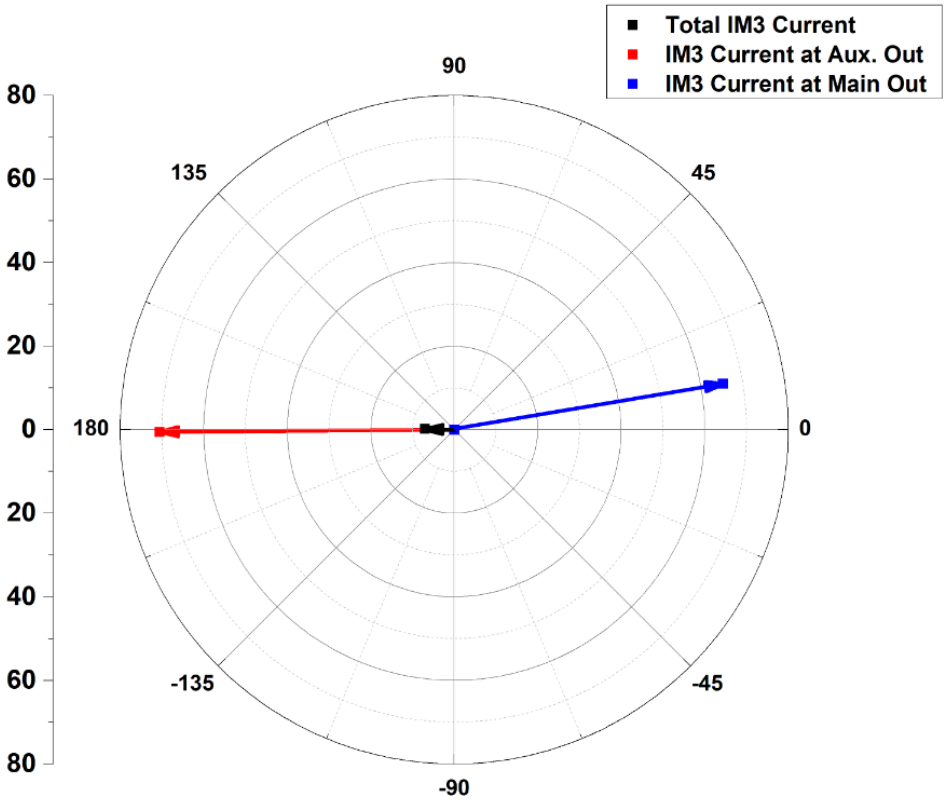

Figure 2.25 IM3 current components at the output of the main, auxiliary, and the overall amplifier.

designed to obtain several states where all frequency sub-ranges and g_{m3}s are aimed to be covered. However, this method comes with a trade-off between the high design complexity and OIP3 performance. If the frequency sub-ranges are chosen as very narrow, the number of states for the transistor bank will increase significantly. On the other hand, if the frequency sub-ranges are chosen widely, the whole sub-range could not benefit from the IM3 cancellation equally since for the selected g_{m3}, IM3 gets perfectly canceled out for only a single frequency in that sub-range.

Another method to alter the g_{m3} is by changing the DC operating conditions of the M3. In this work, M3's operating condition is aimed to be adjusted by externally applying the bias voltage to M3's gate. An external control signal is resistively voltage divided with a ratio of 1:10 as shown in Fig. 2.24 to have better control over the applied gate voltage. The circuit is simulated with and without the cascode amplifier post-distortion technique by applying a two-tone test. The spacing between the tones is selected as 10 MHz, and for the post-distortion case, the best control voltages for the auxiliary circuit are applied. The results are shown in Fig. 2.26.

Apart from the cascode auxiliary post-distortion technique, another post-distortion technique with diode-connected FET is also realized. Similar to cascode auxiliary variation, the diode connected technique also includes an additional circuitry that is

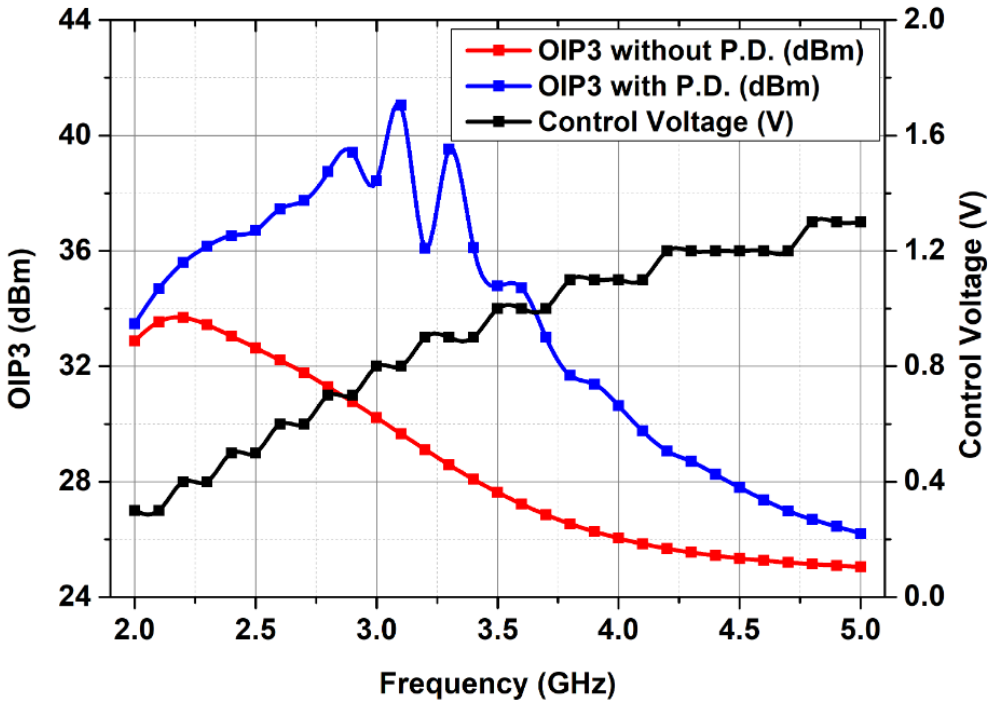

Figure 2.26 Simulated OIP3 with and without cascode auxiliary post-distortion technique.

connected to the inter-node of the second cascode amplifier stage. Although, since the additional circuit is diode-connected, sampling and the mixing node are the same, which was not the case for the cascode auxiliary version. Additionally, even though it is called a diode-connected circuit, it is only RF-wise diode-connected. In reality, FET's gate and drain nodes are separated in DC with a DC block capacitor. The schematic of the diode-connected auxiliary post-distortion technique is shown in Fig. 2.27.

Similar to the cascode auxiliary version, for the diode-connected auxiliary version, the generated current components of the M1 can be modeled by the Eqn. (2.7) where g_{m1} is the transconductance, $g_{m1}^{'}$ is the first-order derivative of g_{m1} and $g_{m1}^{''}$ is the second-order derivative of the g_{m1}. However, due to having a diode-connected device at the inter-node, the inter-node voltage is slightly different from the other case, and to find the inter-node voltage (V2), the Eqn. (2.11) can be used. Assuming that M2 is a linear transistor, the current components of the M3 can be calculated by again using the Eqn. (2.9). Finally, the fundamental tone and the 3^{rd} order signal component at the output can be found from Eqn. (2.12).

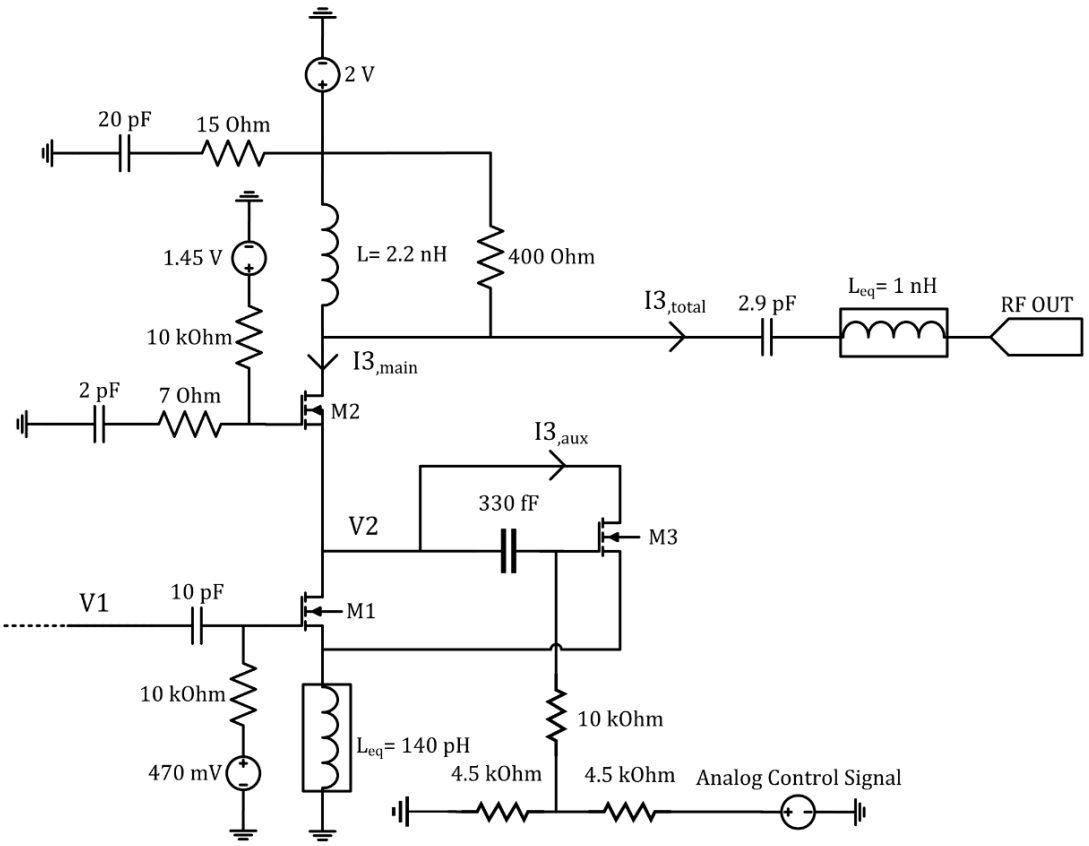

Figure 2.27 Diode-connected auxiliary post-distortion circuit with the second cascode amplifier stage.

$$V2 = \frac{g_{m1}V1 + g_{m1}^{'}V1^2 + g_{m1}^{''}V1^3}{g_{m2} + g_{m3}}. \tag{2.11}$$

$$I1_{total} = g_{m1}(1 - \frac{g_{m2}}{g_{m2} + g_{m3}})V1. \tag{2.12a}$$

$$I3_{total} = (g_{m1}^{''}(1 - \frac{g_{m3}}{g_{m2} + g_{m3}}) - g_{m3}^{''}(\frac{g_{m1}}{g_{m2} + g_{m3}})^3 - g_{m3}^{'}\frac{2g_{m1}^{'}g_{m1}}{(g_{m2} + g_{m3})^2})V1^3. \tag{2.12b}$$

Eqn. (2.12) indicates that $I3_{total}$ can be cancelled out by carefully selecting the g_{m2} and g_{m3}. However, this method also introduces small gain loss, which can not be avoided. Although, the gain loss can be minimized by selecting a small g_{m3} and an appropriate g_{m2}.

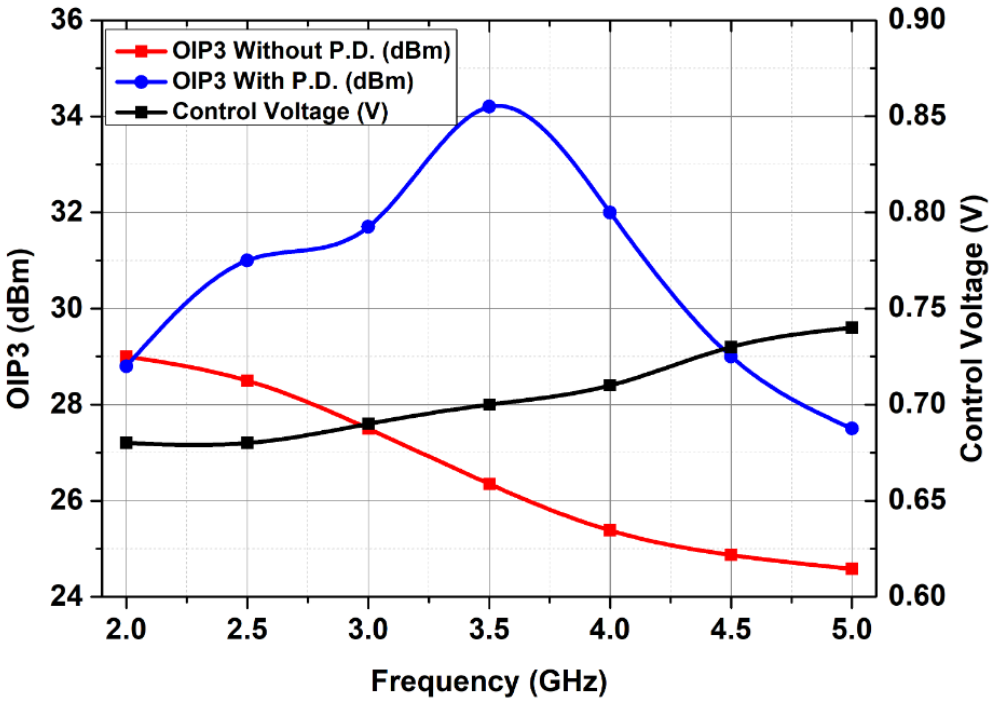

Figure 2.28 Simulated OIP3 with and without diode-connected auxiliary post-distortion technique.

Similar to the cascode auxiliary case, IM3 cancellation depends on the frequency of operation. Control of the g_{m3} through an analog control signal is also preferred in this version to obtain a strong IM3 cancellation over a wide bandwidth. An external control signal is resistively voltage divided with a ratio of 1:2 as shown in Fig. 2.27 to have better control over the applied gate voltage. The circuit is simulated with and without the cascode amplifier post-distortion technique by applying a two-tone test. The spacing between the tones is selected as 10 MHz, and for the post-distortion case, the best control voltages for the auxiliary circuit are applied. The results are shown in Fig. 2.28.

2.4.4 Measurement Results

Both versions of the LNAs are sent for tape-out and fabricated in GlobalFoundries 130 nm SOI CMOS technology. The chip layouts of the designed LNAs are similar because LNAs only have different auxiliary circuits. Therefore, only the chip layout of the cascode auxiliary LNA version is shown in Fig. 2.29. Total die area is 0.64

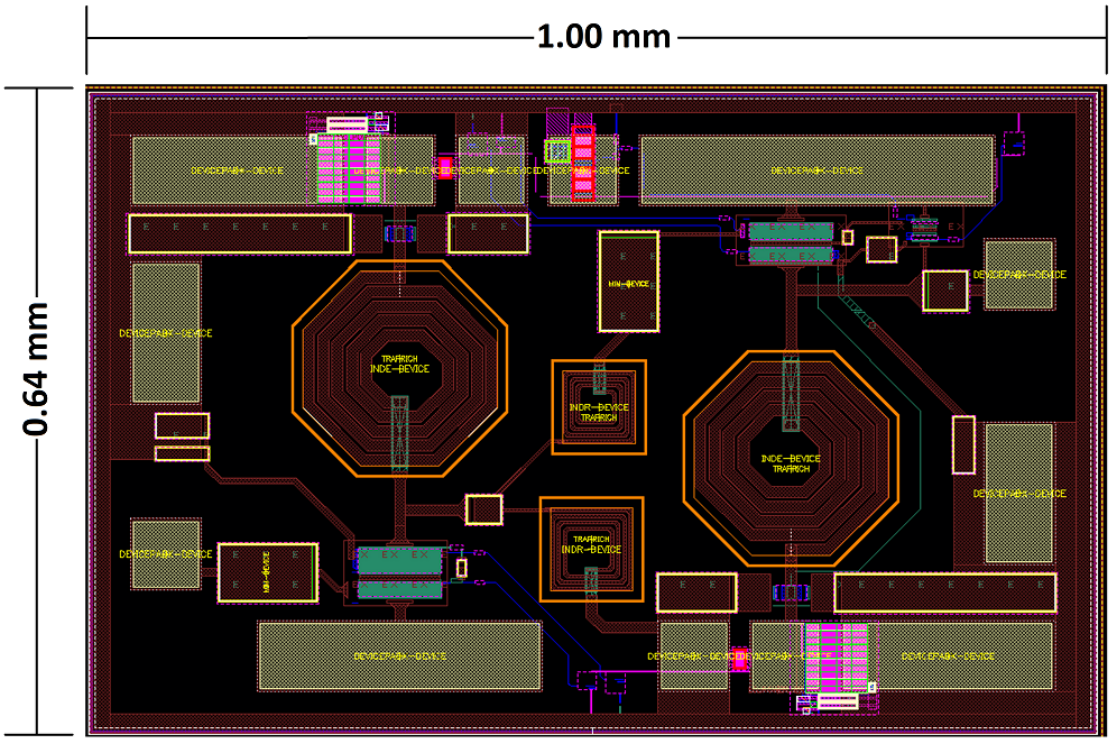

Figure 2.29 Die layout of the SOI LNA.

mm^2 with pads and 0.32 mm^2 without pads. The fabricated chips are packaged with 4 x 4 mm^2 QFN packages, and the inside of the QFN package is visualized in 3D and shown in Fig. 2.30. For the measurement, LNA packages are soldered on the PCB where the PCB substrate is Rogers RO4350B with 250 μm thickness, 2.48 relative permittivity (ϵ), and 17.5 μm copper thickness. LNAs' inputs and outputs are routed with 50-Ω transmission lines to the sides of the PCB, where end-launch connectors are located. Moreover, reference transmission lines are also included on the PCB for the measurement of the trace and connector losses and for the tru calibration for the S-parameter measurement. The photographs of the PCBs are shown in Fig. 2.31. Bypass capacitors of 10 nF, 10 nF, and 100 nF capacitors are used in order to bypass the DC lines on the PCB.

The S-parameters are measured from 1 GHz to 10 GHz by using Keysight N5224A PNA. The measurement setup for the S-parameters are shown in Fig 2.32. Noise figure measurement is conducted for the 2-5 GHz region by using Keysight E4448A PSA and 346A noise source. Noise figure measurement setup is shown in Fig 2.33. OP1dB performance of the LNA is measured from 2 GHz to 5 GHz by using Keysight E8257D PSG and E4448A PSA. However, due to the limitation in the measurement setup, the two-tone test was only applicable from 3.5 to 5 GHz; therefore, OIP3 measurement is only conducted for this frequency range. The measurement setup for linearity is shown in Fig. 2.34.

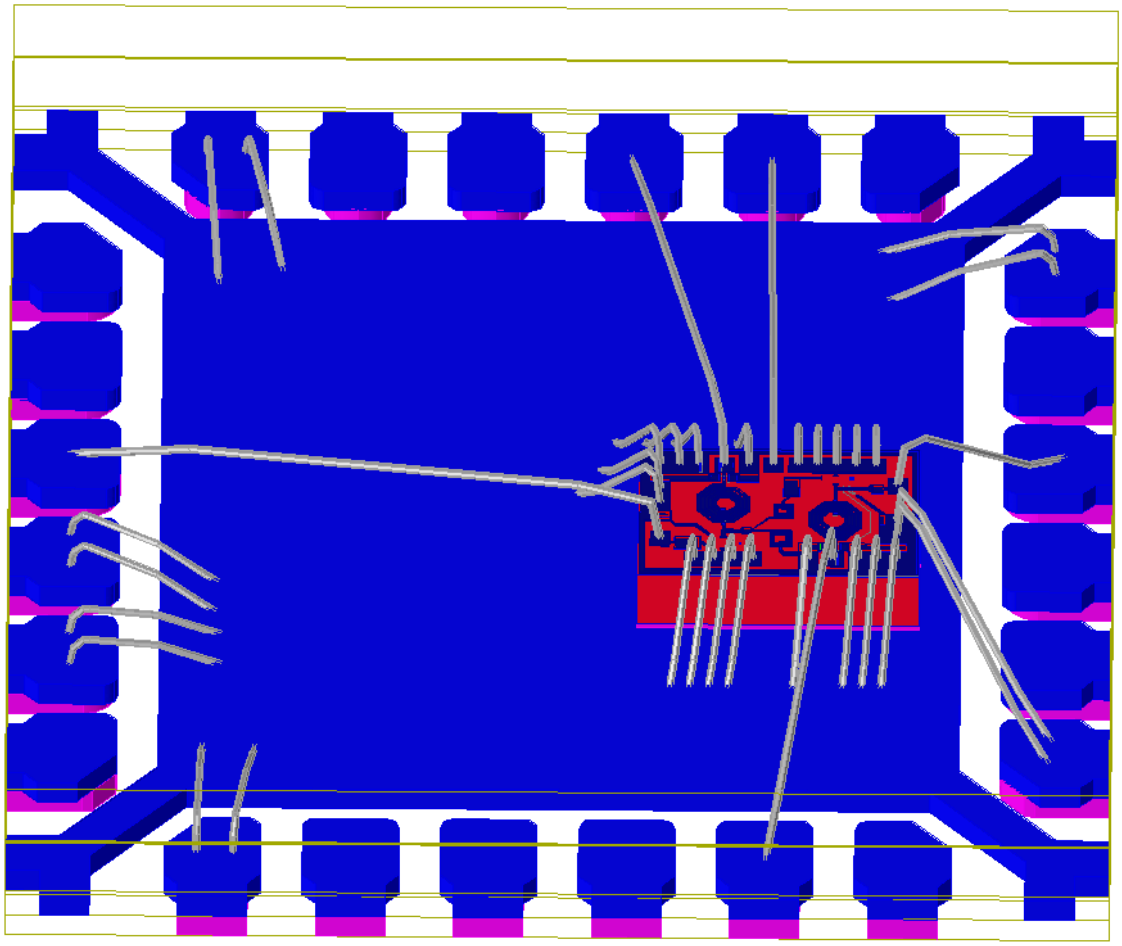

Figure 2.30 3D visualization of the die inside 4 x 4 mm^2 QFN package.

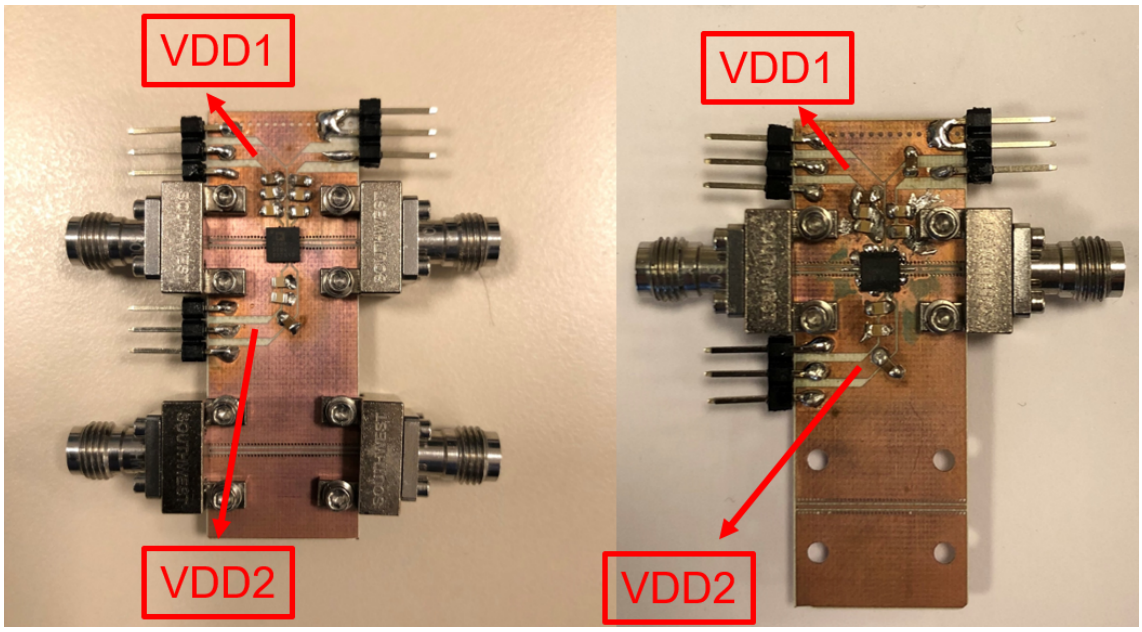

Figure 2.31 Photographs of the PCBs: (a) Cascode auxiliary (Version 1). (b) Diode-connected auxiliary (Version 2).

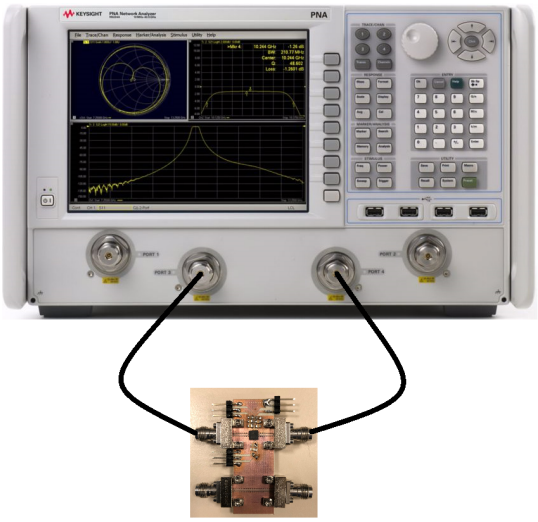

Figure 2.32 S-parameter measurement setup of the SOI LNAs.

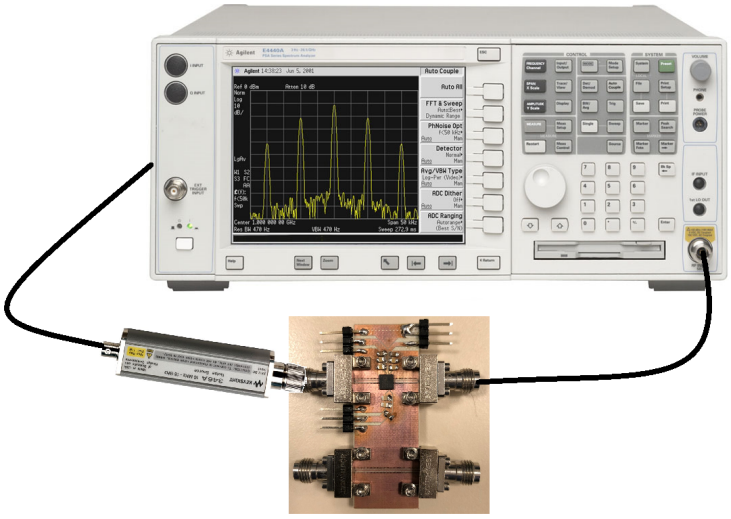

Figure 2.33 Noise figure measurement setup of the SOI LNAs.

S_{11} and S_{22} measurement results of the LNAs are shown in Fig. 2.35 and Fig 2.36, and input and output matchings are better than -10 dB between 2.2 - 5.3 GHz. The measurement result of the output matching was similar to its simulation result for both versions. On the other hand, for both LNAs, a frequency shift has been observed at the input side. Input matching's higher frequency limit had been shifted from 6.3 GHz to 5.3 GHz. The measured small-signal gain (S_{21}) has reached 30.5 dB at 3.5 GHz and achieves a 3-dB bandwidth between 2.1 GHz and 4.5 GHz for both versions, as shown in Fig. 2.37.

The noise figure reached its lowest value, 0.85 dB at 2.5 GHz. NF is smaller than 1 dB between the 2 GHz and 3.5 GHz, and the NF is smaller than 1.55 dB inside the matched frequency region. Moreover, an NF increase has been observed in the high-frequency region due to the input matching shift from 6.3 GHz to 5.3 GHz.

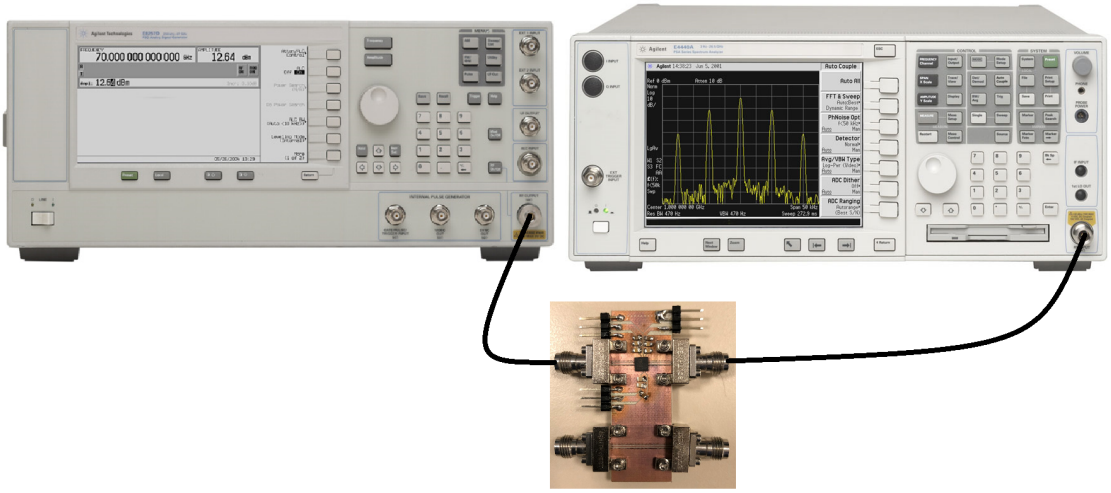

Figure 2.34 OIP3 and OP1dB measurement setup of the SOI LNAs.

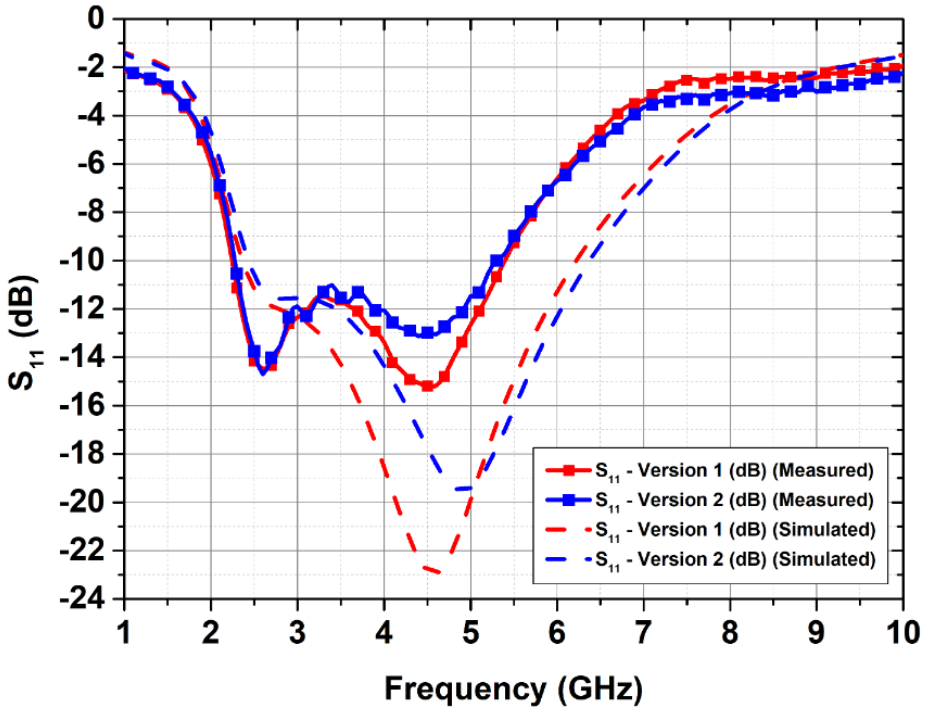

Figure 2.35 Measured and simulated S_{11} of the both SOI LNA versions.

The NF measurement and simulation results can be seen in Fig. 2.38.

The OP1dB was measured as 13.1 dBm at 3.5 GHz, and it is higher than 12 dB inside the matched frequency region. OP1dB measurement and simulation results are shown in Fig. 2.39.

Finally, OIP3 measurement is done by applying two tones centered around the center frequency, and the frequency spacing between the tones was selected as 10

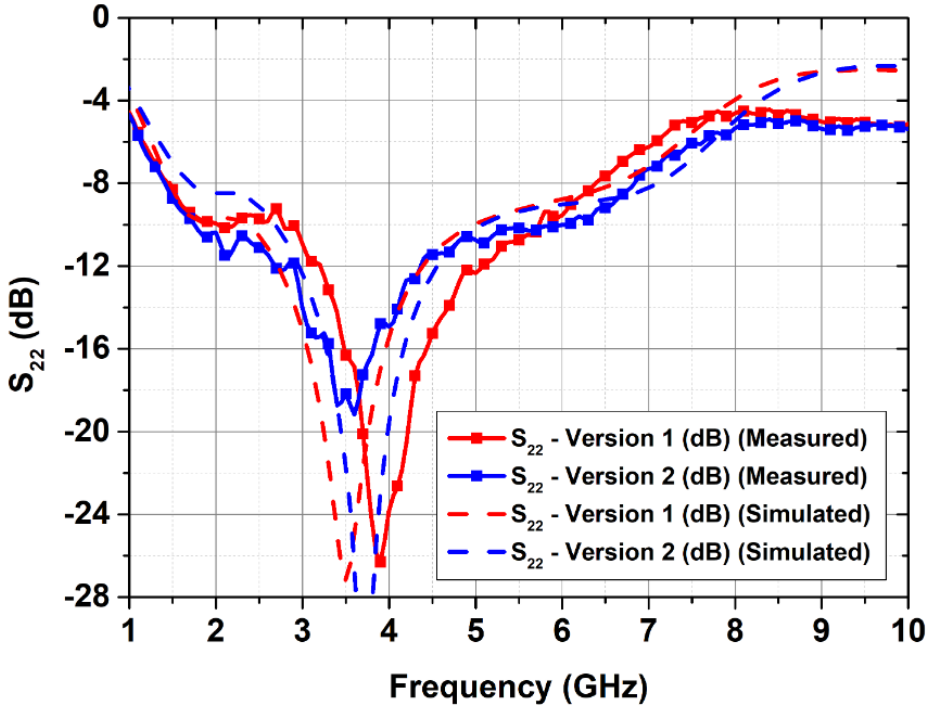

Figure 2.36 Measured and simulated S_{22} of the both SOI LNA versions.

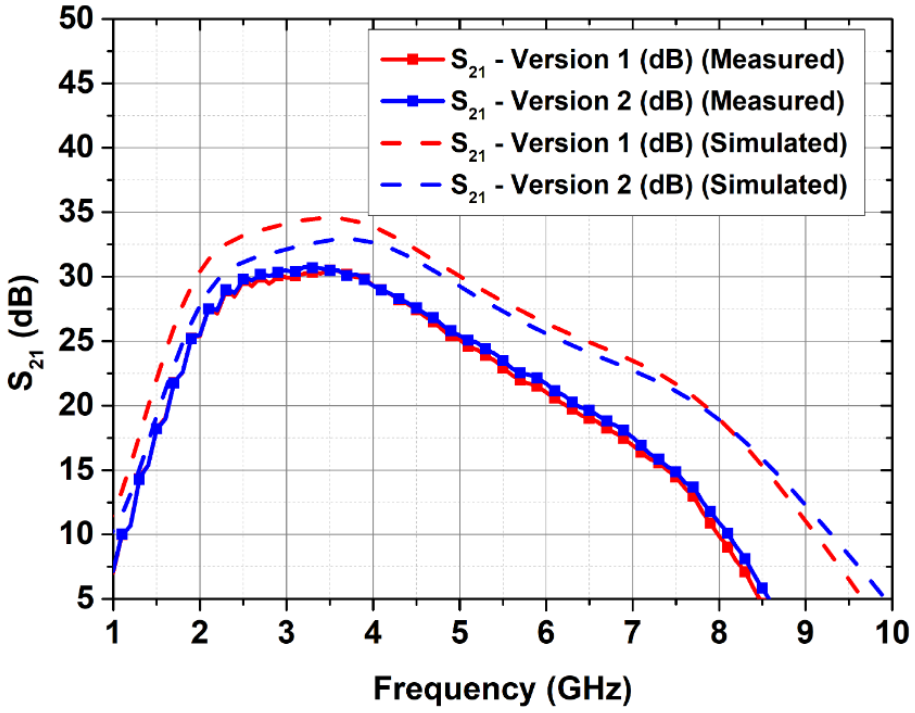

Figure 2.37 Measured and simulated S_{21} of the both SOI LNA versions.

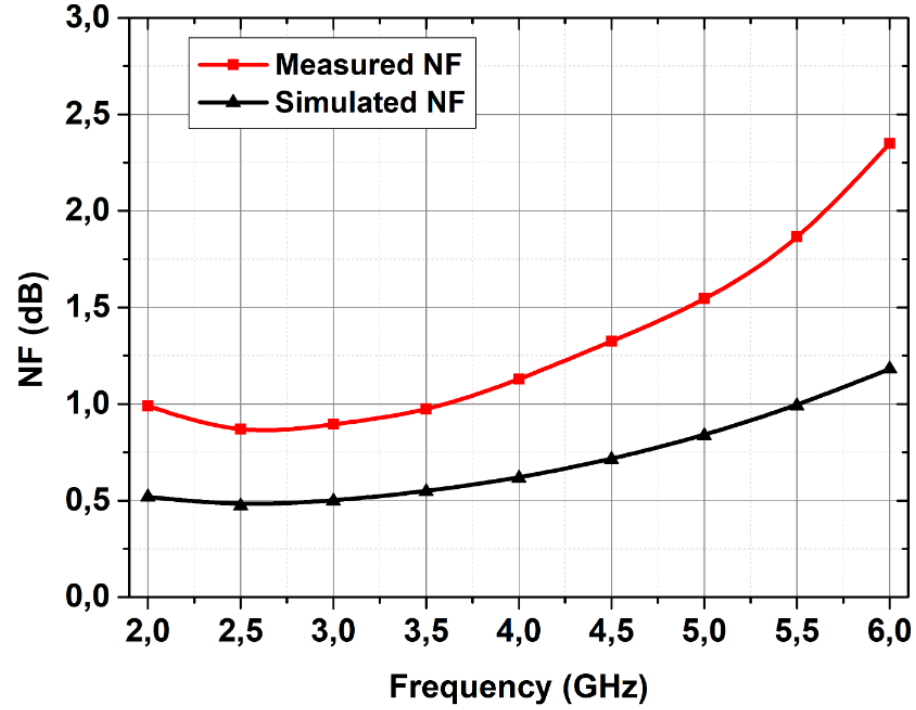

Figure 2.38 Measured and simulated NF result of the SOI LNAs.

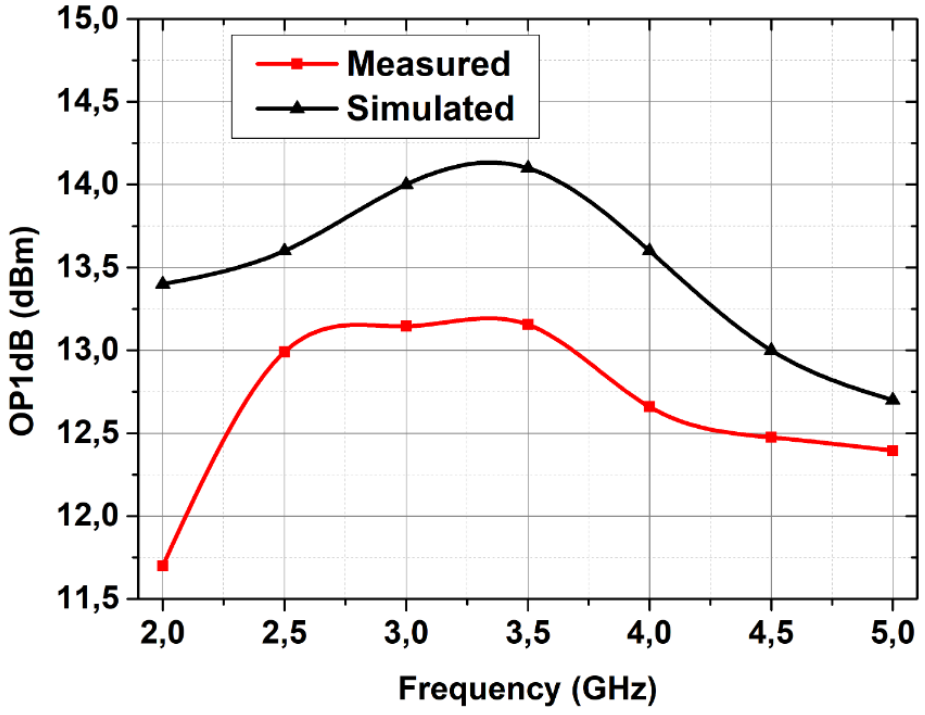

Figure 2.39 Measured and simulated OP1dB results of the SOI LNAs.

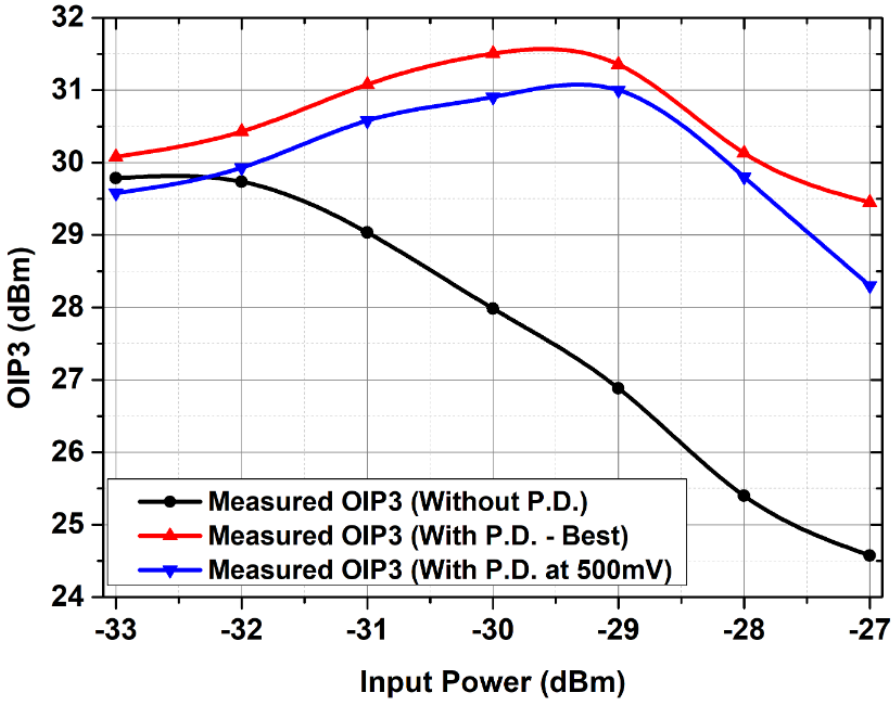

Figure 2.40 Cascode auxiliary LNA's OIP3 at different input powers at 3.5 GHz.

MHz for all measurement cases. For the LNA with the cascode auxiliary, OIP3 was first measured at different input powers at 3.5 GHz by using the Eqn. (2.13) for the lower frequency P_1 and P_3. The result of OIP3 measurement at different input powers at 3.5 GHz is shown in Fig. 2.40 and the externally applied control voltage values which are used to obtain the best OIP3 performance at the specific input power level is shown in Fig. 2.41. Since the suppression of 3^{rd} order intermodulation products is more important for the high input power cases, OIP3 has been measured between 3.5 - 5 GHz at -27 dBm input power, and the measurement's result is shown in Fig. 2.42 and the externally applied control voltage values which are used to obtain the best OIP3 performance at the specific center frequency is shown in Fig. 2.43.

$$OIP3 = P_1 + \frac{P_1 - P_3}{2}. \tag{2.13}$$

Similar to the first version, for the LNA with the diode-connected auxiliary, OIP3 has been firstly measured at different input powers at 3.5 GHz and found by using the Eqn. (2.13) again for the lower frequency P_1 and P_3. The result of OIP3 measurement at different input powers at 3.5 GHz is shown in Fig. 2.44 and the

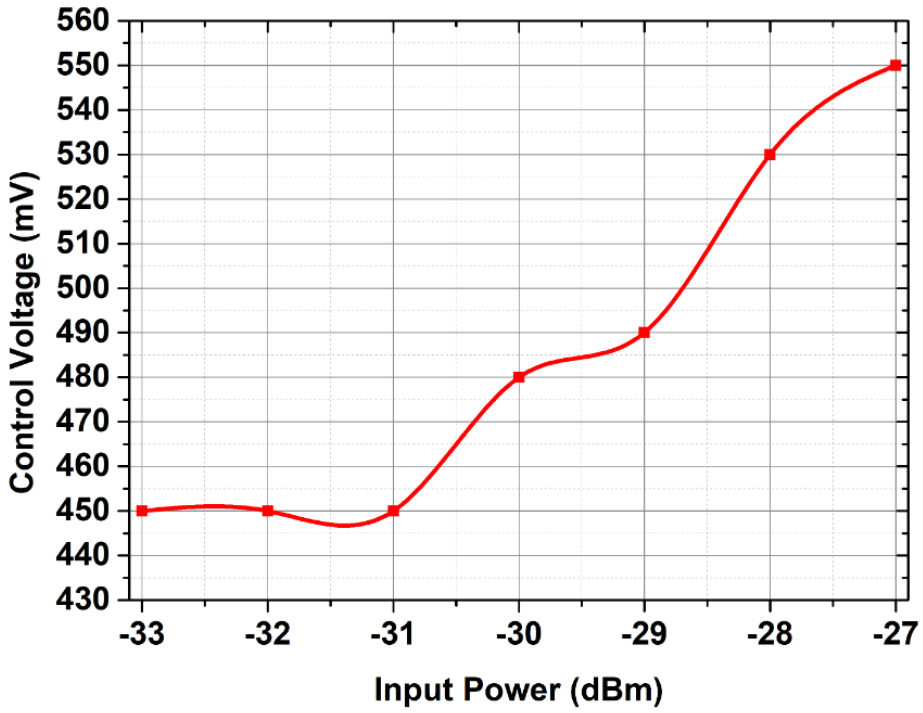

Figure 2.41 Applied external control voltage for the cascode auxiliary LNA at different input powers at 3.5 GHz.

externally applied control voltage values which are used to obtain the best OIP3 performance at the specific input power level is shown in Fig. 2.45. Similarly, OIP3 has been measured between 3.5 - 5 GHz at -27 dBm input power, and the measurement's result is shown in Fig. 2.46 and the externally applied control voltage values which are used to obtain the best OIP3 performance at the specific center frequency is shown in Fig. 2.47.

Since both post-distortion techniques require changing the control voltage according to the center frequency and the input power level, real-life applications of these methods become less feasible. Therefore, a post-distortion technique with a constant control voltage should be realized, and for this purpose, diode-connected auxiliary LNA's OIP3 is measured for both lower and higher frequency P_1 and P_3 between 3.5 - 5 GHz region at different input power levels for a control voltage of 720 mV. The results of the OIP3 measurement are shown in Fig. 2.48, 2.49, 2.50, 2.51.

Moreover, the reported LNA performed a stable operation, and no oscillation was observed when the LNA's output was analyzed with the spectrum analyzer.

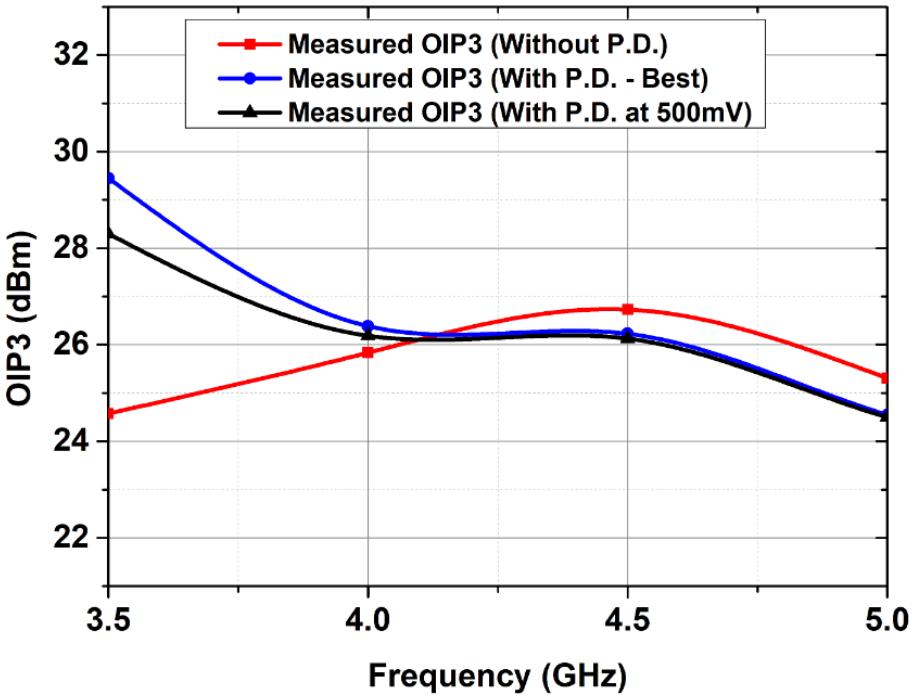

Figure 2.42 Cascode auxiliary LNA's OIP3 at different center frequencies at -27 dBm input power.

2.4.5 Comparison

Measurement results of this work are summarized in Table 2.3 and compared with the other state-of-the-art CMOS LNAs (Alam & DeGroat, 2006; An, Wagner & Ellinger, 2018; Fan, Zhang & SÁnchez-Sinencio, 2008; Lee, Wang & Wang, 2012; Lin, Wang, Lee & Chen, 2014; Muhamad, Soin, Ramiah, Noh & Chong, 2013; Noori, Sanner & Yanduru, 2015; Reddy, Sammeta, Kumari, Quadir & Jain, 2019; Song, Kim, Han, Choi, Park & Kim, 2008; Vanukuru, Dutta, Swaminathan, Choppalli, Wolf, Jaffe, Tan, Logan, Monaghan & Joseph, 2020; Zhan & Taylor, 2006). Two different figures-of-merits are used for comparison. FoM_1 compares gain IIP3, f_c, NF, and DC power consumption (Sturm et al., 2014).

$$FoM_1 = \frac{Gain[abs] \times IIP3[mW] \times f_c[GHz]}{(F-1)[abs] \times P_{DC}[mW]}. \tag{2.14}$$

while FoM_3 compares gain, bandwidth, f_c, NF, and DC power consumption.

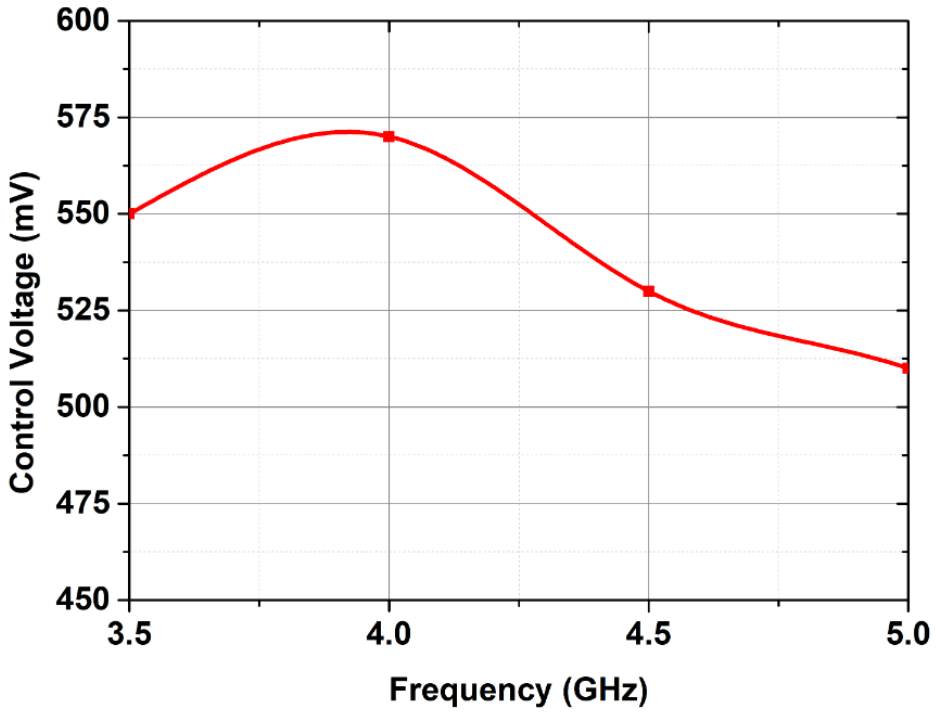

Figure 2.43 Applied external control voltage for the cascode auxiliary LNA at different center frequencies at -27 dBm input power.

$$FoM_3 = \frac{Gain[abs] \times BW[GHz]}{(F-1)[abs] \times P_{DC}[mW] \times f_c[GHz]}. \tag{2.15}$$

This work achieves the highest figure-of-merit among the wideband LNAs in 130 nm technology and has one of the lowest NF with respect to state-of-the-art CMOS LNAs.

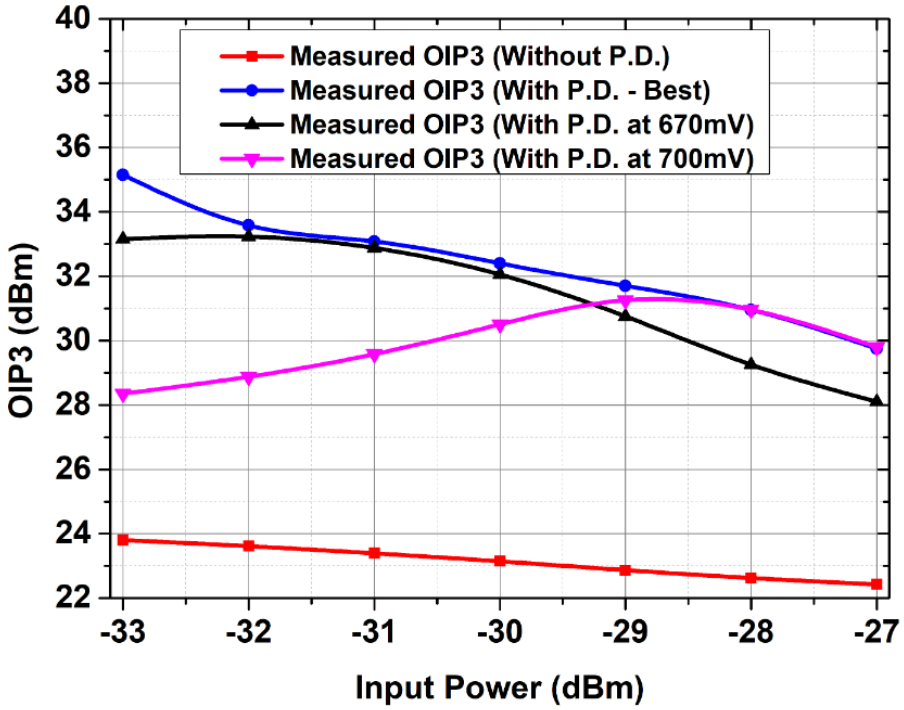

Figure 2.44 Diode-connected auxiliary LNA's OIP3 at different input powers at 3.5 GHz.

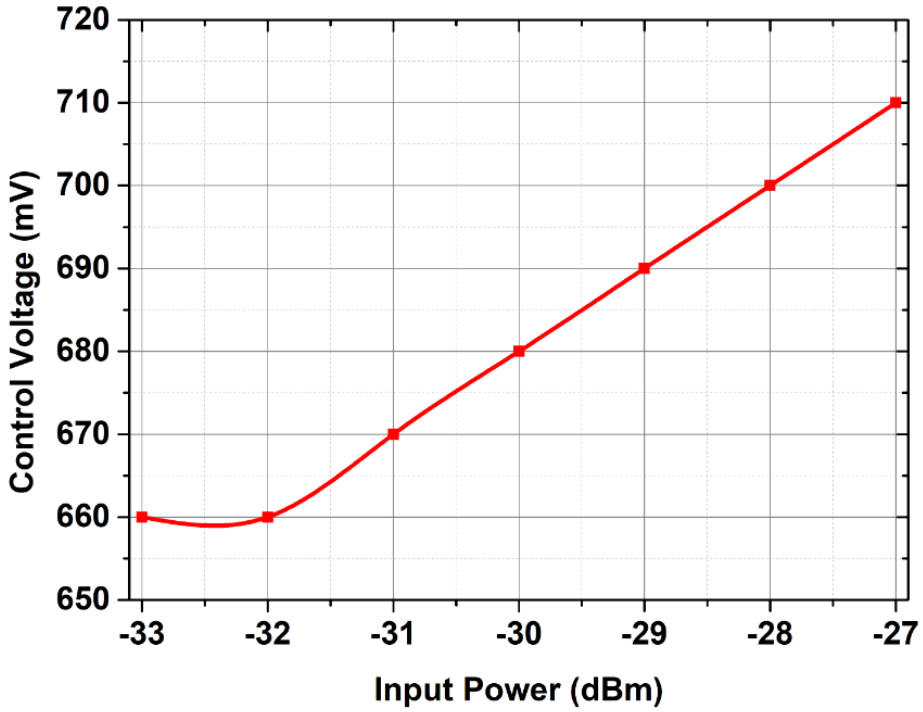

Figure 2.45 Applied external control voltage for the diode-connected auxiliary LNA at different input powers at 3.5 GHz.

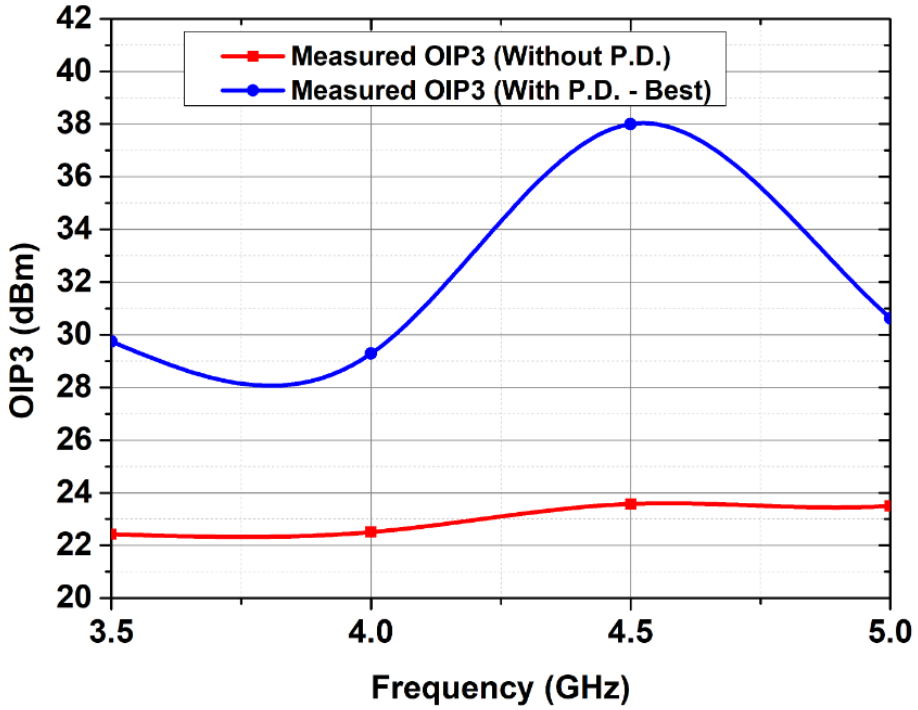

Figure 2.46 Diode-connected auxiliary LNA's OIP3 at different center frequencies at -27 dBm input power.

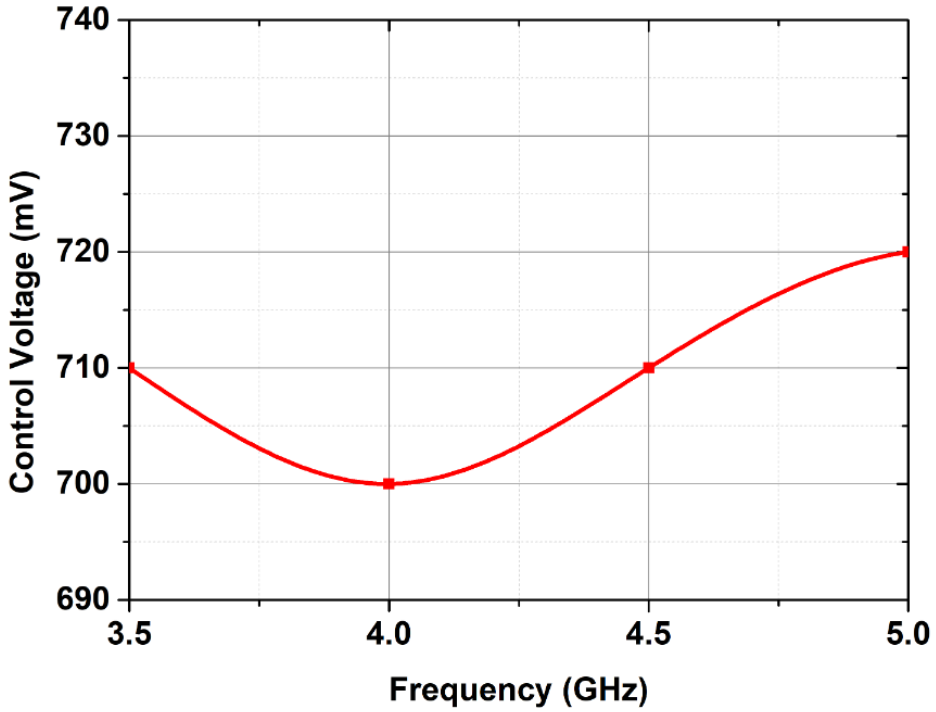

Figure 2.47 Applied external control voltage for the diode-connected auxiliary LNA at different center frequencies at -27 dBm input power.

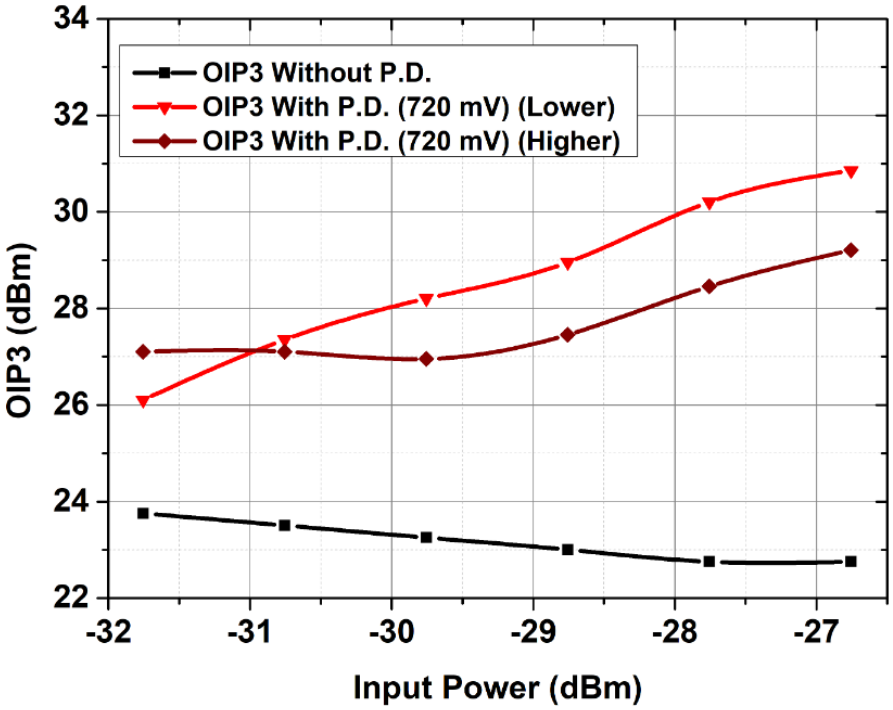

Figure 2.48 Diode-connected auxiliary LNA's OIP3 at different input powers at 3.5 GHz for lower and higher P_1 and P_3.

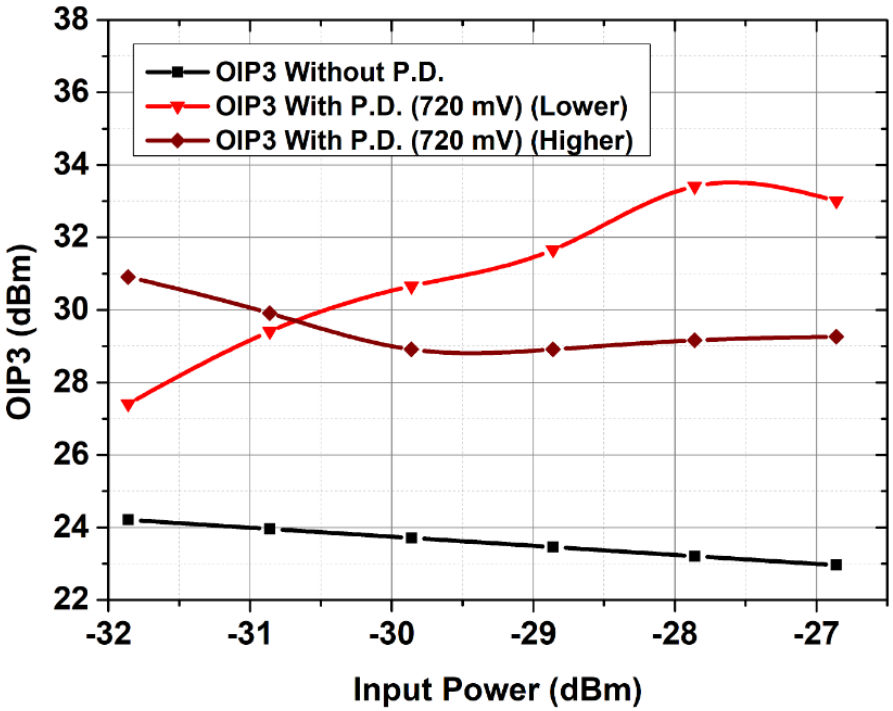

Figure 2.49 Diode-connected auxiliary LNA's OIP3 at different input powers at 4.0 GHz for lower and higher P_1 and P_3.

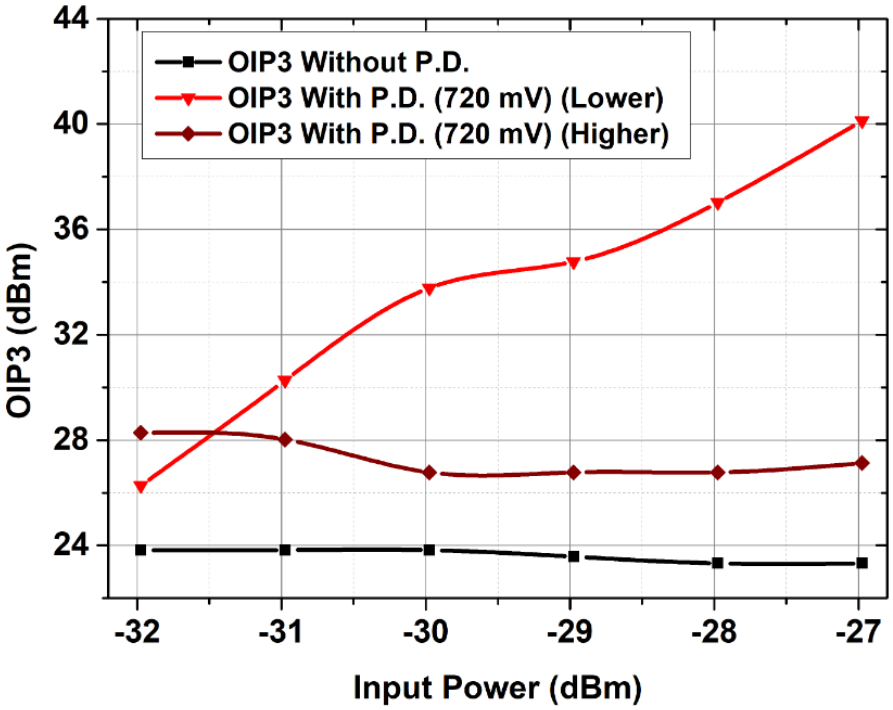

Figure 2.50 Diode-connected auxiliary LNA's OIP3 at different input powers at 4.5 GHz for lower and higher P_1 and P_3.

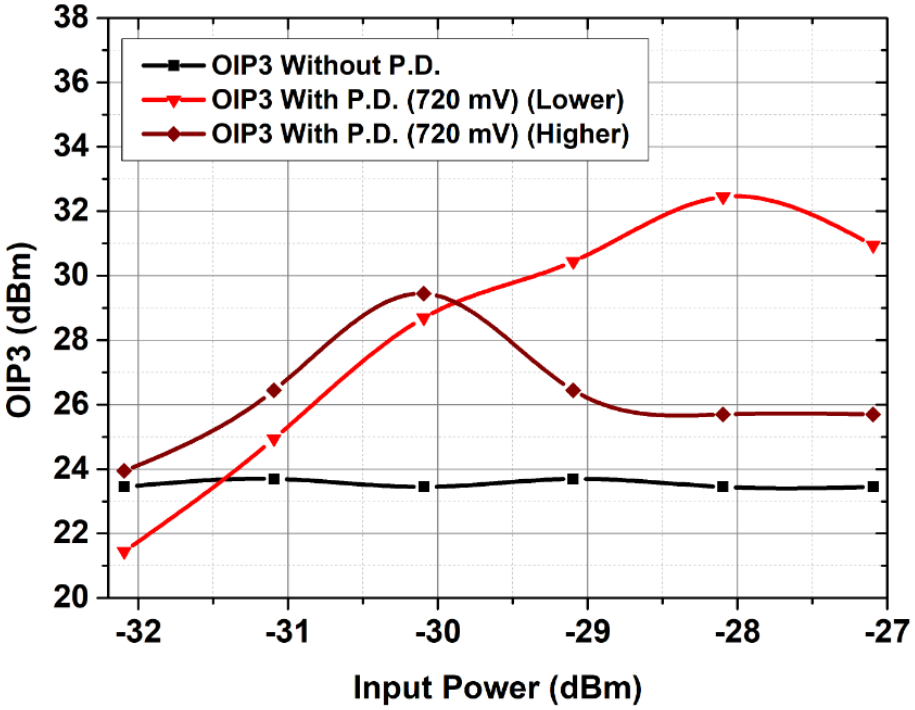

Figure 2.51 Diode-connected auxiliary LNA's OIP3 at different input powers at 5.0 GHz for lower and higher P_1 and P_3.

Table 2.3 Comparison of State-of-the-art LNAs.

Reference	**BW (GHz)**	**Gain (dB)**	**NF (dB)**	**IIP3 (dBm)**	**Power (mW)**	**Technology**	FoM_1	FoM_3
(An et al., 2018)	2.8-12.8	12.5	2.9	5.1	11.7	45nm SOI	2.52	3.23
(Lin et al., 2014)	3-10	11.5	2.3	-0.2	18	180nm CMOS	0.44	0.48
(Fan et al., 2008)**	2.15-2.3	8.6	1.92	-2.55	16.2	350nm CMOS	0.16	0.01
(Alam & DeGroat, 2006)*	2.41-2.52	18.9	2	2.42	6.45	180nm CMOS	13.26	0.59
(Vanukuru et al., 2020)	2.3-2.65	19.5	0.85	1.5	6.25	130nm CMOS	16.56	2.34
(Muhamad et al., 2013)**	2.32-2.48	18.56	1.85	-7.8	8	130nm CMOS	0.97	0.06
(Song et al., 2008)	2.1-2.35	16.6	1.07	-5.3	7.5	130nm CMOS	1.14	0.13
(Lee et al., 2012)**	0.2-2.6	24	1.9	-3	9	90nm CMOS	9.03	15.48
(Zhan & Taylor, 2006)	0.5-8.2	25	1.9	-16	42	90nm CMOS	0.12	0.22
(Noori et al., 2015)	1.8-2.2	11	0.8	4.6	6.6	130nm SOI	4.58	0.92
(Reddy et al., 2019)	2.4-2.6	16.27	1.7	-0.87	1.44	130nm CMOS	16.28	1.3
Cascode Auxiliary	2.2-5.0	30.5	0.85	1	246	130nm SOI	5.00	3.89
Diode-connected Auxiliary	2.2-5.0	30.5	0.85	5	246	130nm SOI	11.20	8.71

*: EM Simulation, **: Differential

3. VOLTAGE VARIABLE ATTENUATORS FOR SUB-6 GHZ 5G RECEIVER SYSTEMS

3.1 Introduction

In this chapter, analyses, design steps, and implementation results of voltage variable attenuators will be discussed in detail. In section 3.2, attenuator fundamentals, attenuator topologies, and their advantages and disadvantages will be covered. In section 2.3, a wideband voltage variable attenuator designed and fabricated in 130nm SOI CMOS technology will be presented. Finally, in section 2.4, a 130nm SOI CMOS high power ultra-high precision voltage variable attenuator's design steps, analyses, and results will be discussed in detail.

3.2 Attenutor Fundamentals

Many transmitters and receiver systems, especially phased array systems, require an amplitude control block to set the power level of the received or transmitted signal. These control blocks are expected to provide high precision amplitude control capability while also employing low phase errors. For the amplitude control purpose, VGAs and attenuators are widely used. However, VGAs are not suitable for wideband applications and suffer from low linearity performance and DC power consumption. Therefore, attenuators are more favorable due to their wideband frequency range, better power handling capability, and lower RMS phase and amplitude error.

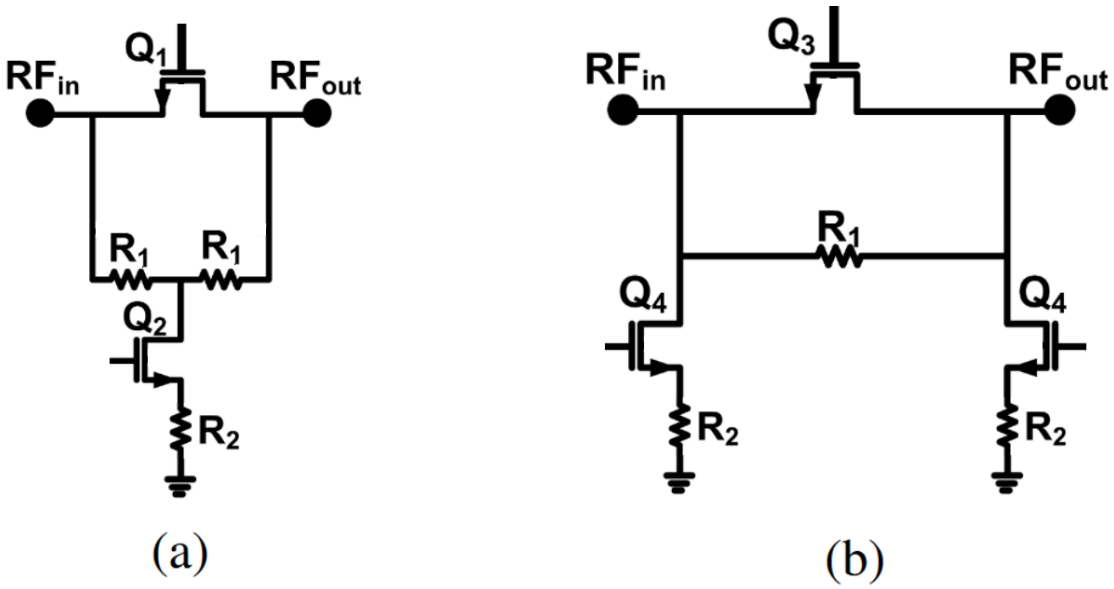

Figure 3.1 Attenuator network types: (a) T-type. (b) π-type.

3.2.1 Digital Step Attenuators

Frequently used attenuator topologies are mainly categorized as digital and analog controlled attenuators. Most common digitally controlled attenuator types are switch-type π/T attenuators (Davulcu, Caliskan, Kalyoncu, Kaynak & Gurbuz, 2016; Ku & Hong, 2010; Li, Zhang, Li, Gao, Wang, Song & Xu, 2022; Song, Cho & Cressler, 2018; Yuan, Mu & Guo, 2018). These attenuator networks achieve attenuation by switching the signal between a low loss path and a resistive path. Digital step attenuators commonly consist of π-type or T-type attenuator networks or utilize both attenuator types in the different attenuation stages of the same attenuator circuit. π and T-type attenuator networks are shown in Fig. 3.1. Assuming MOS switches are ideal, for the π-type attenuator networks, attenuation-resistance relationship is given in (3.1). Additionally, attenuation-resistance relationship for the T-type attenuator networks is given in (3.2).

$$R_1 = \frac{Z_0}{2} \times \frac{10^{Att/10} - 1}{10^{Att/20}} \qquad R_2 = Z_0 \frac{10^{Att/20} + 1}{10^{Att/20} - 1} \tag{3.1}$$

$$R_1 = Z_0 \frac{10^{Att/20} - 1}{10^{Att/20} + 1} \qquad R_2 = 2 \times Z_0 \frac{10^{Att/20}}{10^{Att/10} - 1} \tag{3.2}$$

Common design practice is designing attenuation stages in a binary fashion in order to cover a wide range of attenuation levels while achieving a low RMS amplitude error which is a performance criterion that focuses on how much the obtained attenuation level differentiates from the ideal attenuation level for each attenuation step. RMS amplitude error can be calculated by using the formula given in (3.3). As a shortcoming of implementing many attenuation stages, the IL and the die area increase significantly with each attenuation stage and its switches.

$$\sqrt{\frac{\sum_{i=2}^{2^N}(Att_{i,real} - Att_{i,ideal})^2}{2^N - 1}} \tag{3.3}$$

Moreover, recently published switch-type attenuators (Davulcu et al., 2016; Song et al., 2018; Yuan et al., 2018) utilize parallel inductor arms for amplitude correction and lower RMS phase errors, which is another performance criterion that mainly focuses on how much the phase shift changes as the attenuation level of the attenuator change. Ideally, zero phase shift is not expected from the attenuators, but the amount of the phase shift should be constant for all attenuation states for all frequencies. RMS phase error for the attenuators can be calculated by using the formula given in (3.4).

$$\sqrt{\frac{\sum_{i=1}^{2^N}(\triangle\phi_{i,real} - \triangle\phi_{i,avg})^2}{2^N}} \tag{3.4}$$

3.2.2 Voltage Variable Attenuator

In addition to digital step attenuators, another commonly used attenuator topology is the VVA topology which utilizes an analog control signal to control the attenuation level. The main advantage of this attenuator type is that this topology consists of only one stage of the attenuation network. Due to having a single attenuation stage, this attenuator topology introduces less IL than the other attenuator topologies, as well as less phase error. Moreover, voltage variable attenuators are capable of having any attenuation value inside a range due to controlling the attenuation level with an analog signal instead of a digital one. Therefore, for VVAs, it is not possible to define fixed attenuation states as it is defined for digital step attenuators and

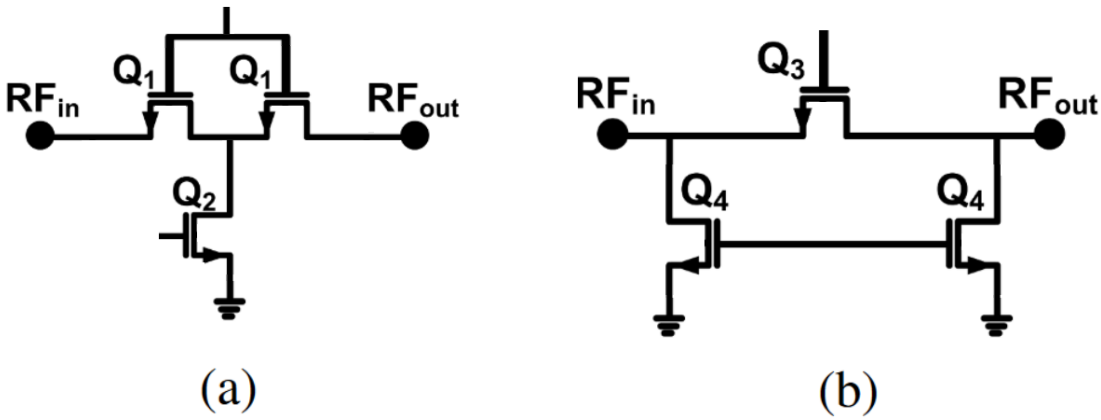

Figure 3.2 VVA network types: (a) T-type. (b) π-type.

consequently, RMS amplitude and phase errors can not be defined and calculated for VVAs.

There are two approaches for realizing VVAs: PIN diodes and FET devices. PIN diode-based VVAs realized on PCB have been reported in (Jang, 2003; Sun, Choi & van der Weide, 2005), but these attenuators exhibit DC power consumption which changes according to the selected attenuation level. On the other hand, FET device VVAs generally utilize two different attenuation networks which are π-type and T-type networks (Daoud & Shastry, 2006; Franzwa, Ellis, Nelson, Granger-Jones & Valenti, 2012; Granger-Jones, Nelson & Franzwa, 2011; Poitrenaud, Lefebvre, Tranchant & Camiade, 2006). These networks are designed with fixed resistors for fixed attenuators and digital step attenuators; however, in VVAs, these resistors are replaced with FET devices, and these devices' channel resistances are utilized to obtain the attenuation level that is wanted. π-type and T-type VVA networks are shown in Fig. 3.2.

Since the channel resistance of FET devices is linked to the applied gate voltage value, a FET's resistance can be controlled in an analog manner through its applied gate voltage. If the gate voltages of the series and shunt FETs are set accordingly to obtain the resistance value that is required for the wanted attenuation level, attenuation level and 50-Ω matching are both obtained at the same time. The required resistance values with respect to attenuation level are given in (3.1) and (3.2) for π-type and T-type networks and the relationship between the applied gate voltage and channel resistance is given in (3.5).

$$R_{chn} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})} \tag{3.5}$$

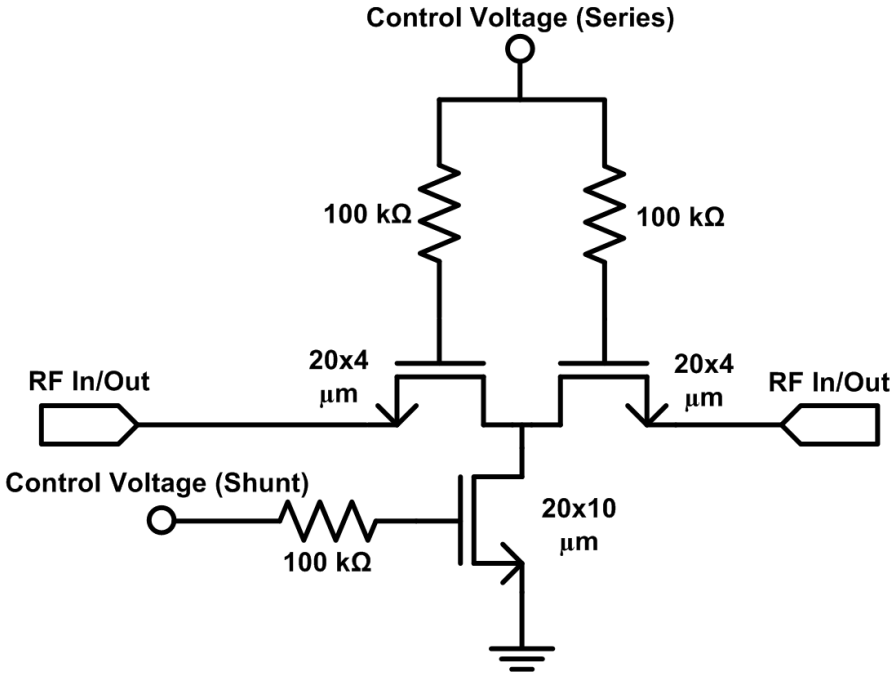

Figure 3.3 Schematic of the designed VVA.

3.3 A Wideband High Precision VVA

3.3.1 Design of the VVA

The designed VVA consists of a single-stage attenuator block with voltage-controlled FETs, as shown in Fig. 3.3. Gate voltages of the FETs shown in Fig. 3.3 are controlled between 0 V and 3.3 V in an analog manner to alter the channel resistances of the FETs accordingly to obtain the desired attenuation level.

The attenuator network type should be carefully selected to obtain a high amplitude control resolution over a wide bandwidth while also covering an extensive attenuation range. As shown in Fig. 3.4 π-type attenuator's series arm resistance should be able to vary from 12 Ω to 1.2 kΩ to achieve an attenuation range of 32 dB without an impedance mismatch. On the other hand, the T-type attenuator network's series arm resistance varies from 5.8 Ω to 48 Ω for the same attenuation operation. Even though the resistance range of the π-type network's series resistor can be covered by varying the gate voltage of the series FET, the FET's C_{off} capacitance can be problematic for the high attenuation states at the high frequencies.

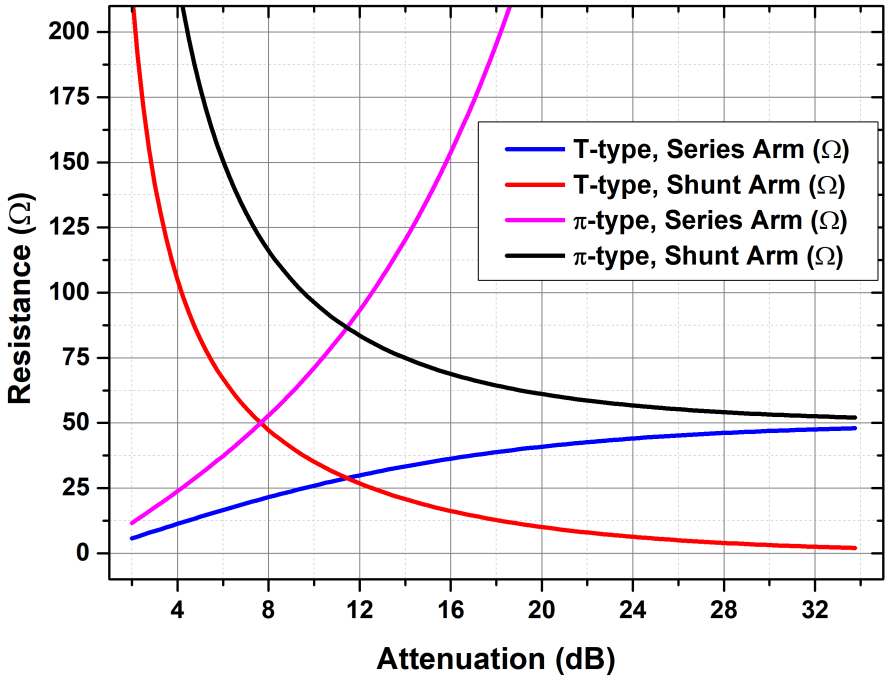

Figure 3.4 T and π-type attenuator resistor values for different attenuation states.

A π-type attenuation network with equivalent FET models is shown in Fig. 3.5. In this type of attenuation network, the series device's channel resistance may need to increase up to a few kΩ; however, at high frequencies C_{off2} starts to dominate the impedance of the series FET and the attenuation amount decreases in magnitude. Moreover, the phase of the S_{21} changes dramatically as the C_{off2} dominates the R_{chn2} and cause the signal flow over the C_{off2} instead of the R_{chn2} therefore, creating a phase shift as shown in (3.6)-(3.8).

$$Z_{shunt/series} = \frac{R_{chn1/2}}{1 + j\omega C_{off1/2} R_{chn1/2}} \tag{3.6}$$

$$\frac{V_{out}}{V_{in}} = \frac{\frac{Z_0 Z_{shunt}}{Z_0 + Z_{shunt}}}{\frac{Z_0 Z_{shunt}}{Z_0 + Z_{shunt}} + Z_{series}} \tag{3.7}$$

$$\frac{V_{out}}{V_{in}} = \left(\frac{R_{chn2}(R_{chn1} + Z_0(1 + j\omega C_{off1} R_{chn1}))}{Z_0 R_{chn1}(1 + j\omega C_{off2} R_{chn2})} + 1\right)^{-1} \tag{3.8}$$

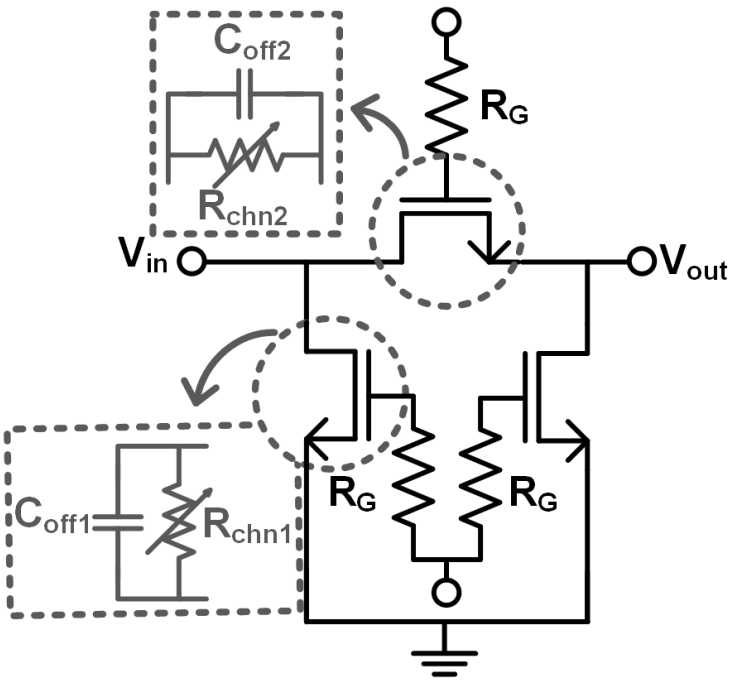

Figure 3.5 π-type attenuator network with equivalent FET models.

C_{off1} can be assumed as a negligible capacitance since the minimum required shunt arm resistance is larger than 50 Ω for all attenuation states; thus, a relatively smaller FET can be used at the shunt arm. This reasoning can be proved by designing π and T-type attenuators with carefully selected device sizes according to the relationship between the R_{on} (the minimum R_{chn} obtained when V_{GS} = 3.3 V) and the FET device size as shown in Fig. 3.6.

The T-type network consists of a shunt device with a 200 μm device width and two series devices with 80 μm device width to cover the whole resistance ranges. For the π-type attenuator, shunt devices' sizes are chosen as 7 μm, and the series device's size is chosen as 40μm. The selected shunt devices size also validates the assumption about the C_{off1} since the value of the C_{off1} is around 2.5 fF as shown in Fig. 3.6. Both attenuation networks are simulated on the schematic level for 16 dB and 32 dB attenuation range cases where 64 and 128 states are used, respectively. The attenuation states are defined by carefully selecting the gate voltages of the series and shunt devices to obtain the required resistance values. RMS amplitude and phase errors of these two attenuation networks are shown in Fig. 3.7 and Fig. 3.8. The simulation result validates the better VVA compatibility of the T-type network over the π-type network because of the high resistance variance at the series arm of the π-type network. Due to the low RMS amplitude and phase error, a T-type attenuation network has been used in this work.

Finally, to reduce the harmful effects of the parasitic capacitances of the FETs,

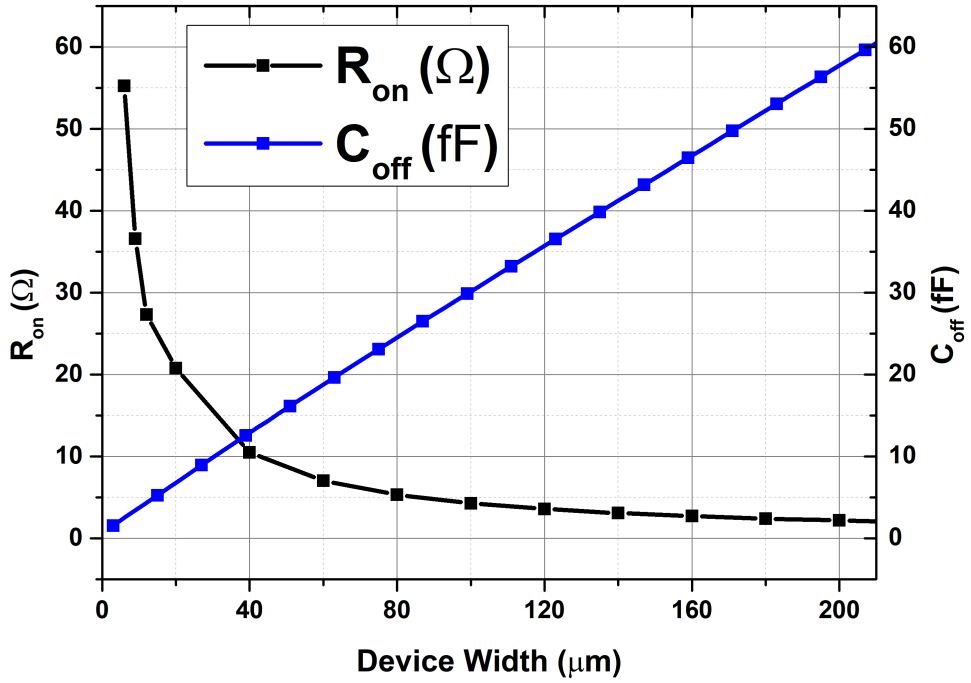

Figure 3.6 R_{on} and C_{off} - FET width relationship at V_{GS}=3.3 V.

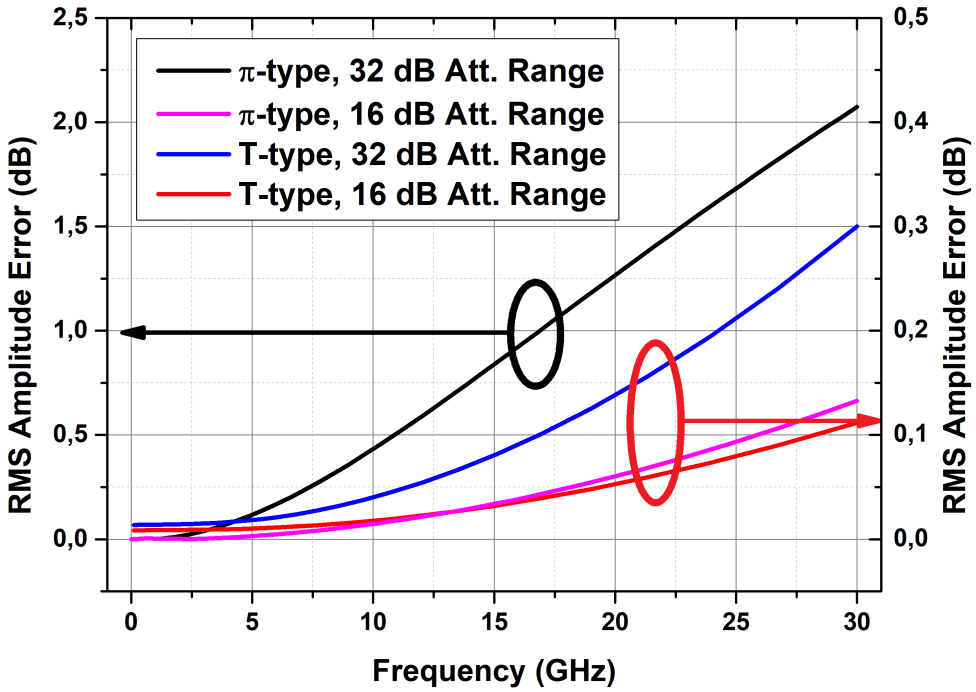

Figure 3.7 RMS amplitude errors of π and T-type attenuators for 16 dB and 32 dB attenuation range cases.

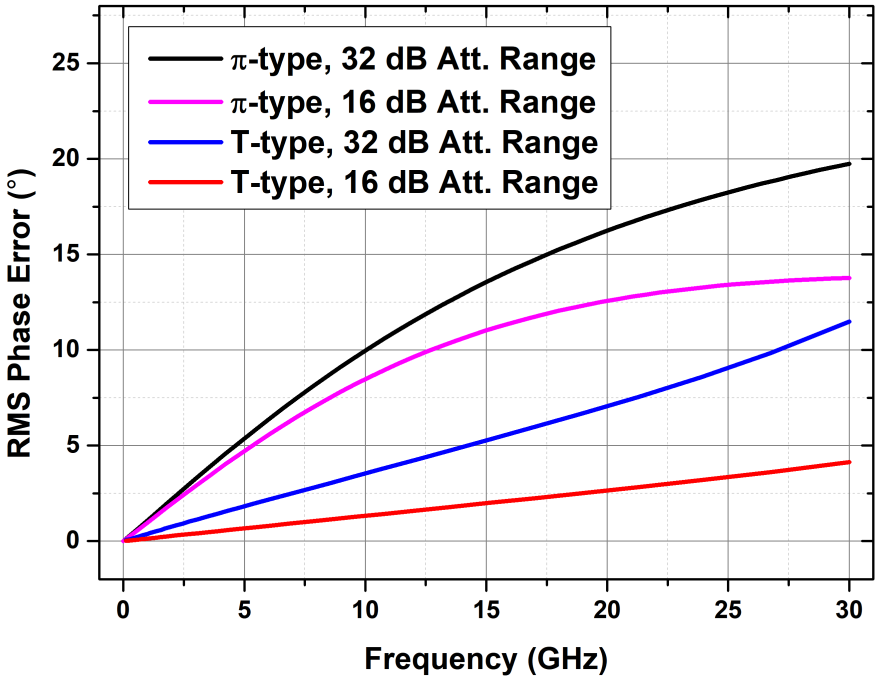

Figure 3.8 RMS phase errors of π and T-type attenuators for 16 dB and 32 dB attenuation range cases.

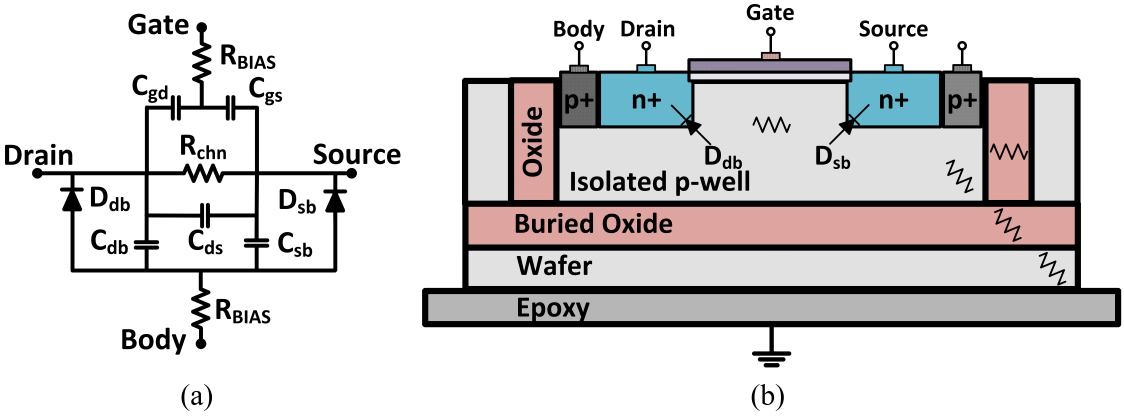

Figure 3.9 (a) SOI NMOS parasitics model with bias resistors. (b) SOI NMOS cross section.

gate and body nodes are biased through high impedance resistors, as shown in Fig. 3.9. By using these resistors, the effects of the parasitic shunt capacitors and body-source/drain junction diodes have been significantly decreased, and additional signal losses are avoided. To further decrease the signal losses through the junction diodes and decrease the threshold voltage, body nodes have been biased with -2.5 V through the bias resistances.

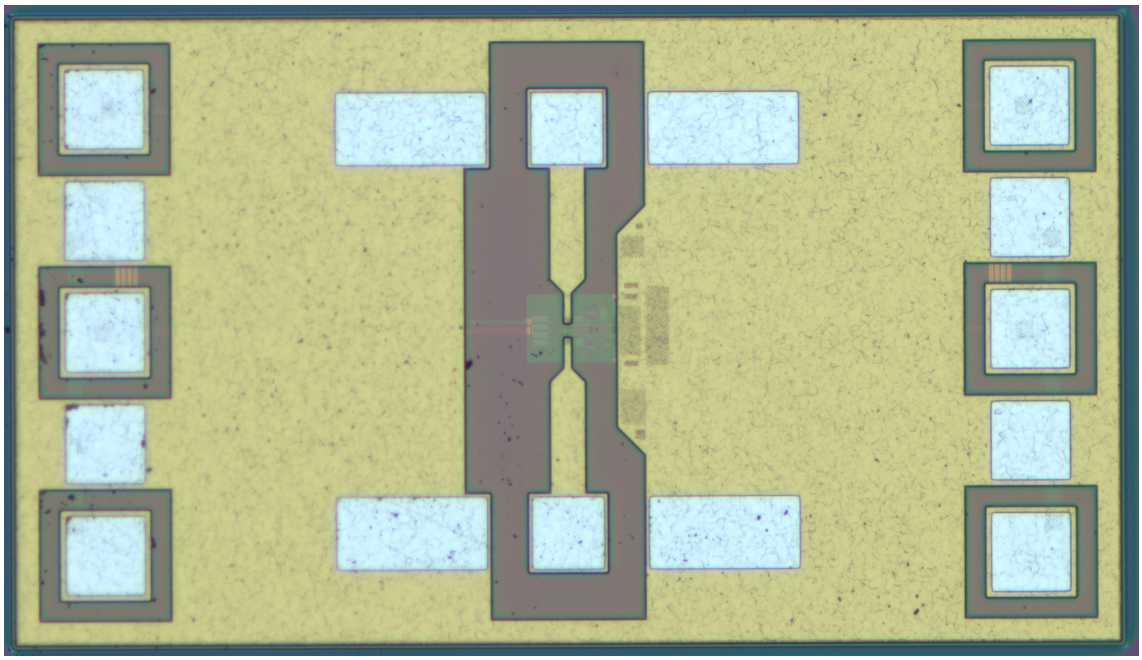

Figure 3.10 Chip photograph of the wideband VVA.

3.3.2 Measurement Results

In this work, GlobalFoundries 130nm SOI CMOS technology has been used. The chip photograph of the reported VVA is shown in Fig. 3.10. The chip area without pads is 0.0048 mm^2. The S-parameters are measured from DC to 40 GHz with Cascade Microtech 40 GHz GSG probes by using Keysight N5224A PNA. The measurement setup for the S-parameters are shown in Fig 3.11.

The measured and simulated IL values are shown in Fig. 3.12. The IL is smaller than 1.7 dB inside the whole bandwidth. Furthermore, the reported VVA is measured for a 16 dB attenuation range where 64 attenuation states are defined. The minimum attenuation step is chosen as 0.25 dB, and the steps are defined by using the FETs' gate voltage - channel resistance behavior. The return losses of both ports are shown in Fig. 3.13 and the VVA achieves wideband input and output impedance matching for all attenuation steps between DC - 40 GHz frequency range.

Attenuation steps do not overlap at any state between DC - 40 GHz range, and flat attenuation behavior is obtained up to 30 GHz as shown in Fig. 3.14. For a fair comparison with digital controlled attenuators, RMS amplitude and phase errors are calculated for a 16 dB attenuation range cases with 64 steps, respectively and shown in Fig. 3.15 and Fig. 3.16. The VVA achieves a 6-bit attenuation operation with an RMS amplitude error $<$ 0.25 dB between DC - 27 GHz for the 16 dB attenuation range. For the 16 dB attenuation range, RMS phase error $<$ 14° inside the whole

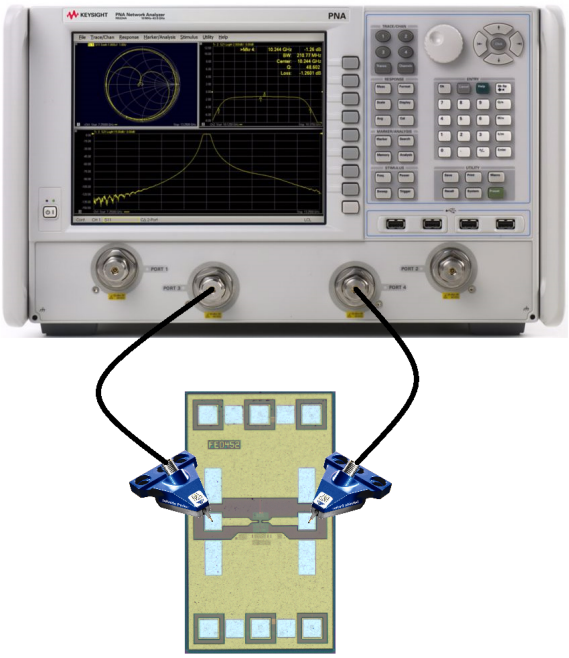

Figure 3.11 S-parameter measurement setup of the wideband VVA.

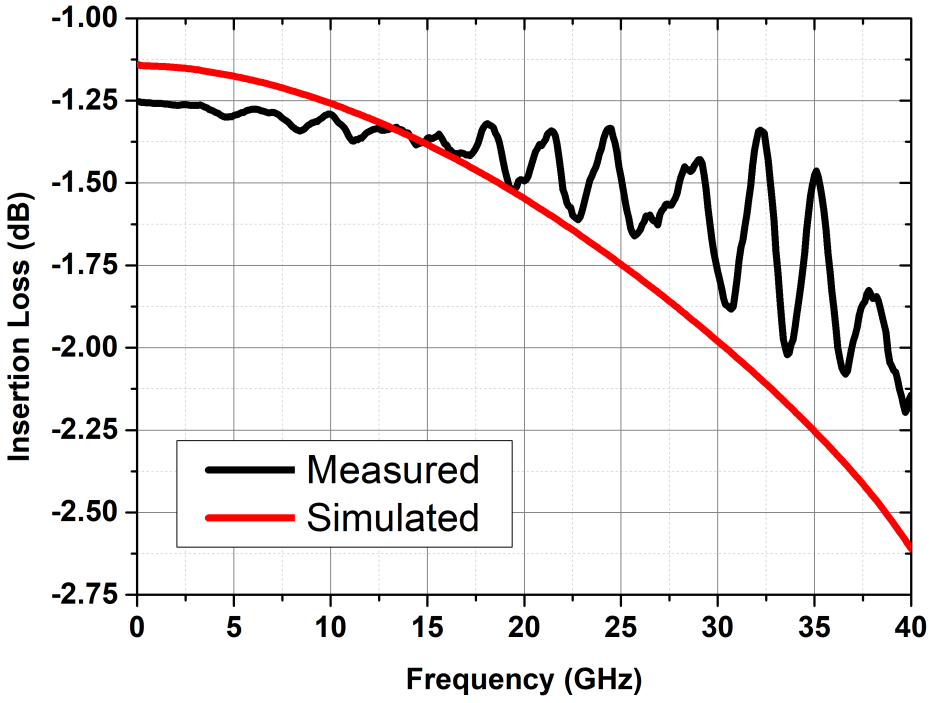

Figure 3.12 Measured and simulated IL of the VVA.

bandwidth.

IIP3 simulation is done by applying two tones between the 1 - 30 GHz range with a frequency spacing of 10 MHz. The highest IIP3 is recorded as 42.2 dBm at 1 GHz,

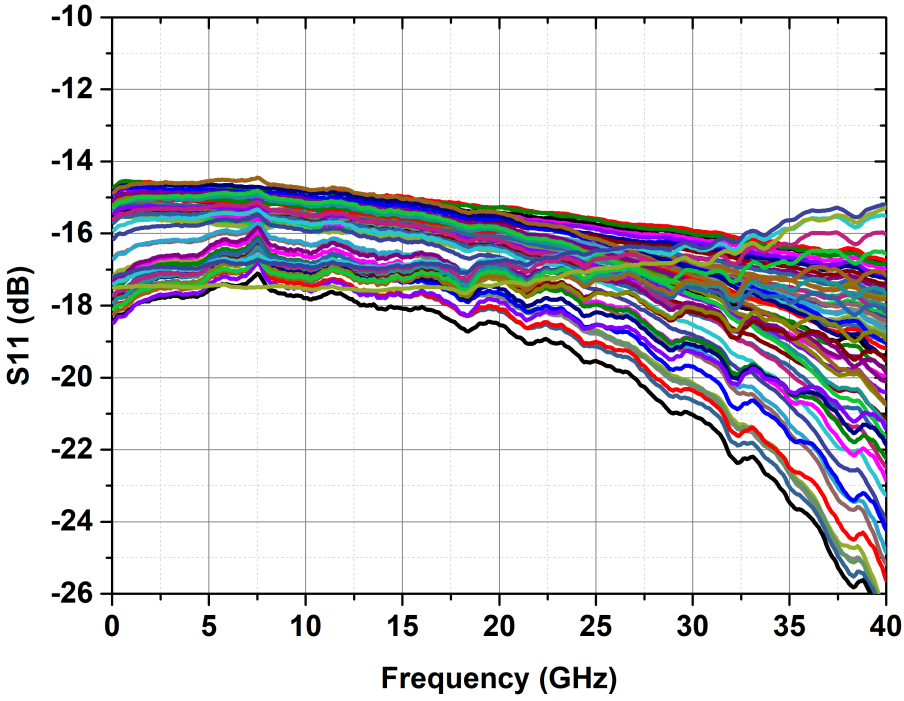

Figure 3.13 Return losses of the input and output ports of the VVA.

and the IIP3 > 39.6 dBm for the whole bandwidth, which ensures a highly linear operation. Finally, the IP1dB simulation is done by applying a single tone between the 1 - 30 GHz range. Inside the whole bandwidth IP1dB > 11.4 dBm, and the IP1dB reaches its maximum value of 12.3 dBm at 30 GHz. The linearity simulation results are shown in Fig. 3.17.

3.3.3 Comparison

The simulation results of this work are summarized in Table 3.1 and compared with the other state-of-the-art attenuators. The reported VVA achieves the lowest IL and has one of the best IIP3 performances among the other works. The VVA has been able to cover the widest bandwidth ranges for the 16 dB attenuation range when compared to published VVAs with similar attenuation ranges. Compared with switch-type attenuators, the reported VVA achieves one of the best RMS amplitude error performances while occupying a significantly smaller active die area.

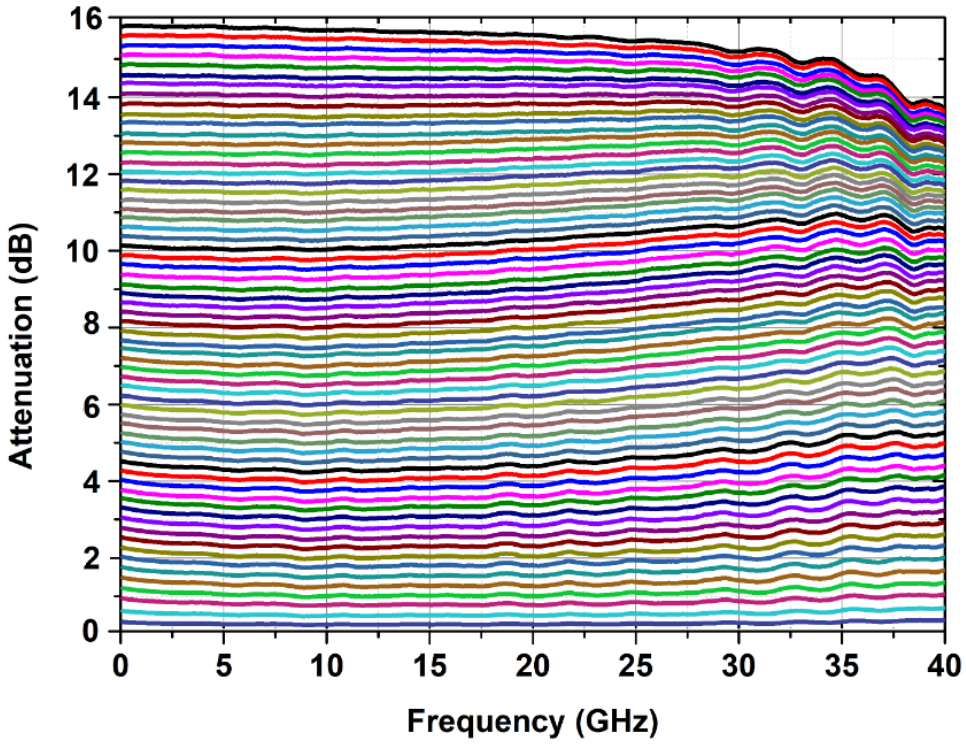

Figure 3.14 Measured 64 different attenuation states of the VVA.

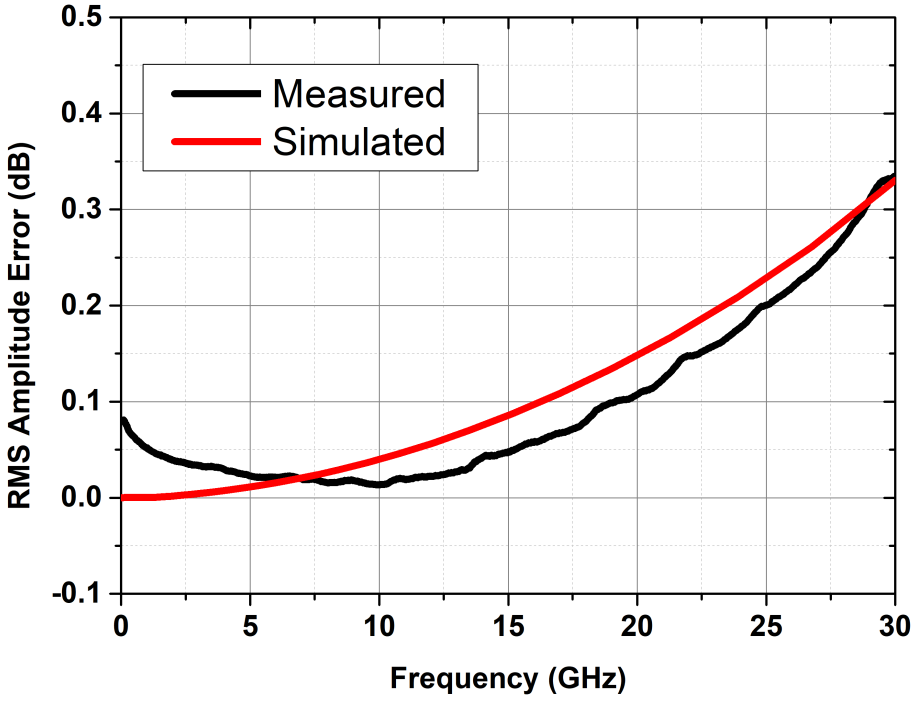

Figure 3.15 RMS amplitude errors of the reported VVA for 16 dB attenuation range.

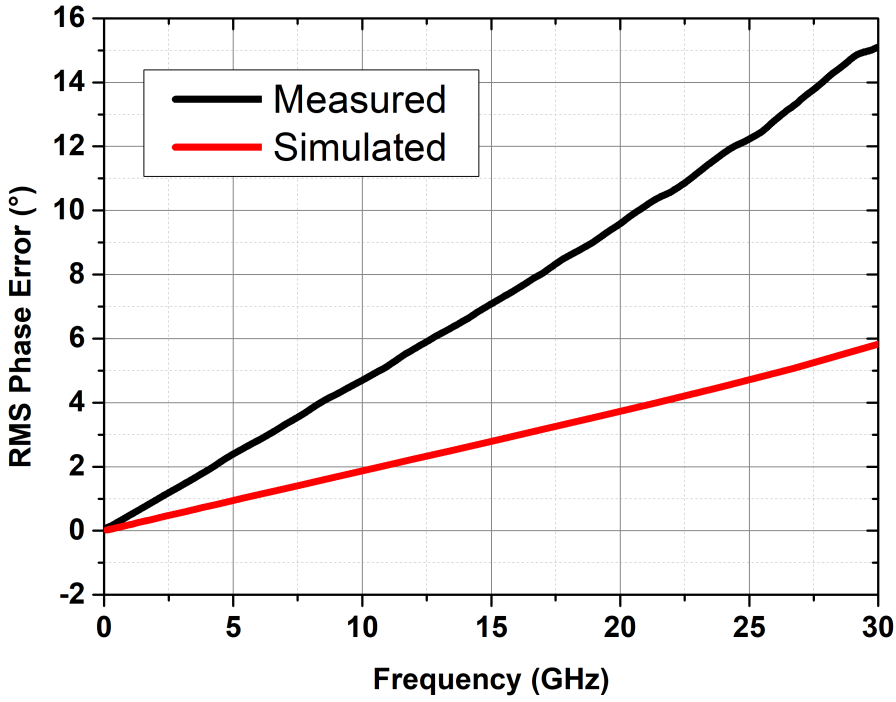

Figure 3.16 RMS phase errors of the reported VVA for 16 dB attenuation range.

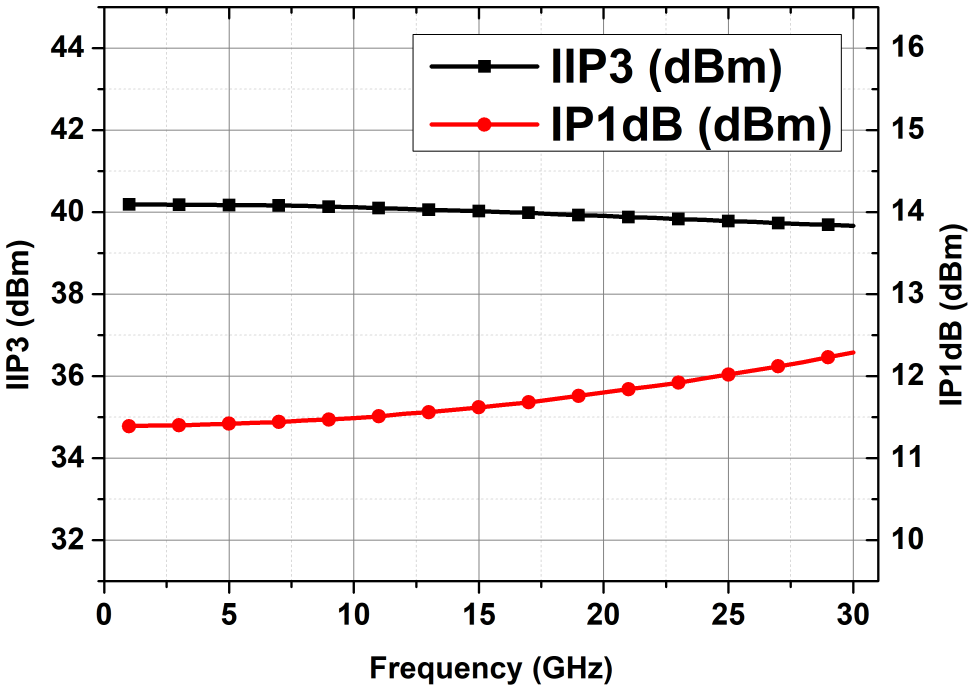

Figure 3.17 IIP3 and IP1dB simulation results between 1 - 30 GHz.

Table 3.1 Comparison Table of the Attenuators

Reference	Bandwidth (GHz)	Att. Range (dB)	IL (dB)	RMS Amp. Error (dB)	RMS Phase Error (°)	IIP3 (dBm)	IP1dB (dBm)	Area (mm^2)	Topology	Technology
Davulcu et al. 2016	6 - 12.5	16.5	<12.7	<0.26	<3.5	N/A	12.5	0.29	Switched π/T	250nm SiGe BiCMOS
Li et al. 2022	DC - 28	15.9	<6.6	<0.15	<0.8	N/A	>10.9	0.044	Switched π/ brid. T	55nm CMOS
Song et al. 2018	DC - 20	31.5	<7.2	<0.37	<4	>25	>10	0.14	Switched T	130nm SiGe BiCMOS
Ku & Hong 2010	DC - 14	31.5	<10	<0.5	<4.2*	29	15	0.5	Switched π/T	180nm CMOS
Franzwa et al. 2012	0.05 - 16	25	<5	N/A	N/A	>38	N/A	N/A	VVA	SOI CMOS
Granger-Jones et al. 2011	0.05 - 4	34	<4.2	N/A	N/A	>47	N/A	N/A	VVA	SOI CMOS
Daoud & Shastry 2006	24 - 32	12	<3	N/A	N/A	N/A	0	0.4**	VVA	150 nm GaAs
Poitrenaud et al. 2006	5 - 30	25	<6.5	N/A	N/A	>30	>25	N/A	VVA	700nm GaAs
This Work	**DC - 27**	**16**	**<1.7**	**<0.25**	**<14**	**>39.7**	**>11.4**	**0.0048**	**VVA**	**130nm SOI CMOS**

*: Approximated from graph, **: Area with pads.

3.4 An Ultra-High Precision Closed-Loop VVA

3.4.1 Design of the VVA

Controlling the attenuation levels of the VVAs tends to be complicated because of the necessity of applying two external analog control signals to have the desired attenuation level as well as 50-Ω matching. Moreover, the required voltage values change due to die-to-die process variation and temperature variation, which degrades the feasibility of determining and applying fixed voltage values. Because of these problems of the VVAs, additional control blocks should be implemented to ease the control of VVA.

There are several proposed control block methodologies in the literature. Firstly, a linear-in-dB attenuation-control voltage behavior can be obtained by using several parallel connected devices and applying different body voltages such that all devices have different threshold voltages. Due to having different threshold voltages, each device contributes a different conductance to the total conductance such that the total conductance matches with the required conductance of the respective attenuation level for that control voltage (Maoz, 1990). This method simplifies the control of the VVA since attenuation becomes linear-in-dB with respect to one of the control voltages; however, the other control voltage still should be applied properly to have 50-Ω matching. Additionally, process and temperature variations are not compensated with this method.

A more advanced method is realized by the implementation of a closed-loop (Dogan, Meyer & Niknejad, 2008). In this method, one of the control signals is applied externally, and the other control signal is generated by the resistance sensing network such that VVA's input and output impedances are 50-Ω. A dummy attenuator is implemented, which uses the same external and internal control voltages as the real attenuator to realize this technique. This dummy attenuator is connected to a resistance sensing circuit that generates the internal control voltage, which ensures the dummy attenuator's impedance is 50-Ω as well as the real attenuator. This method simplifies the control of the VVA significantly since it ensures 50-Ω matching and decreases the number of required control voltages. On the other hand, this method still suffers from the process and temperature variations since the relationship between the attenuation level and external control voltage can vary even though 50-Ω

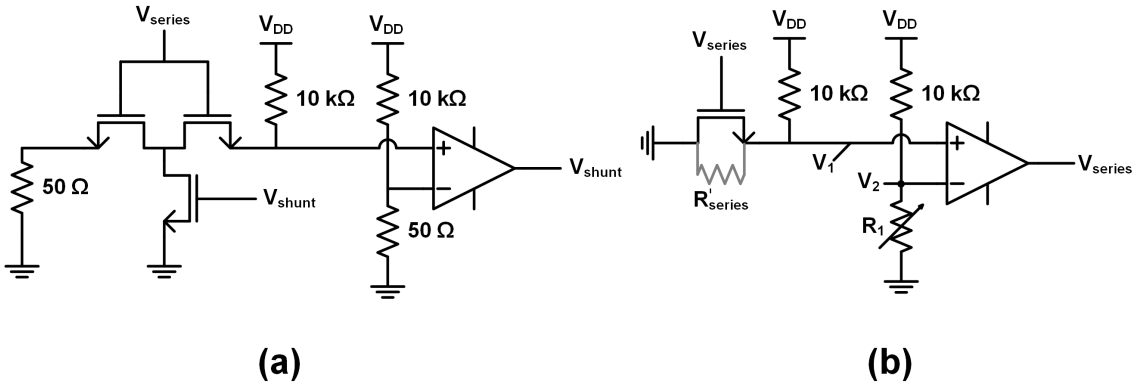

Figure 3.18 Control closed-loops for the VVA: (a) 50-Ω matching. (b) Series device resistance.

is ensured.

In this work, a novel process and temperature tolerant ultra-high precision high power VVA is proposed. The relationship between the attenuation level and control voltage should be completely transistor independent to obtain a process and temperature tolerance. First of all, 50-Ω matching is obtained by implementing a closed-loop network for the control voltage of the shunt device, which is similar to previous work in the literature (Dogan et al., 2008). Moreover, instead of controlling the gate voltage of the series device to alter the series device's resistance, the series device's resistance is directly controlled, and the corresponding control voltage is generated. For this purpose, another resistance sensing network is implemented for the series device; however, this resistance sensing network senses the resistance of the series device instead of the whole attenuator and generates a control voltage to push or pull the channel resistance, R'_{series}, of the series device to be equal to the desired resistance value, R_1. The designed attenuator resistance sensing and device resistance sensing network are shown in Fig. 3.18.

As the attenuation network type, T-type network is preferred since the series device's resistance has a better linear-in-dB relationship with the attenuation level with respect to π-type network as shown in Fig. 3.19. In addition to this, T-type attenuation networks inherently consists of two series devices, which increases the power handling capability and boosts the IP1dB performance since it allows a voltage division between the series devices. For further power handling improvement, process' high power transistors are used in this work. The schematic of the VVA is shown in Fig. 3.20.

Since the attenuation level of the VVA is controlled by altering the series devices' channel resistance by changing the resistance of R_1, a practical method to change the resistance of R_1 is needed. The resistance of R_1 can be changed by using a resistor

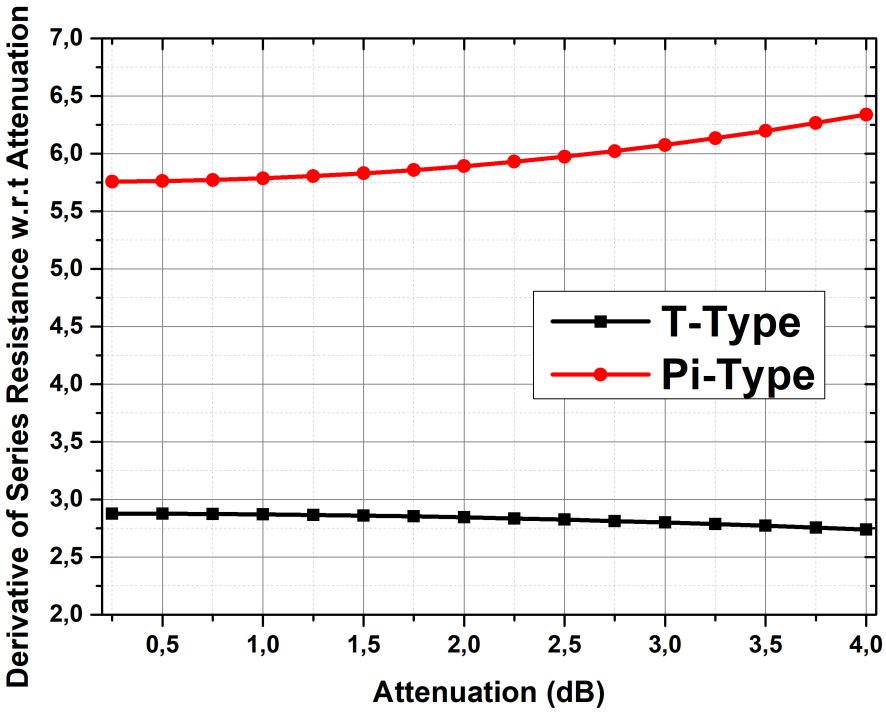

Figure 3.19 Derivative of the series device's resistance with respect to attenuation level.

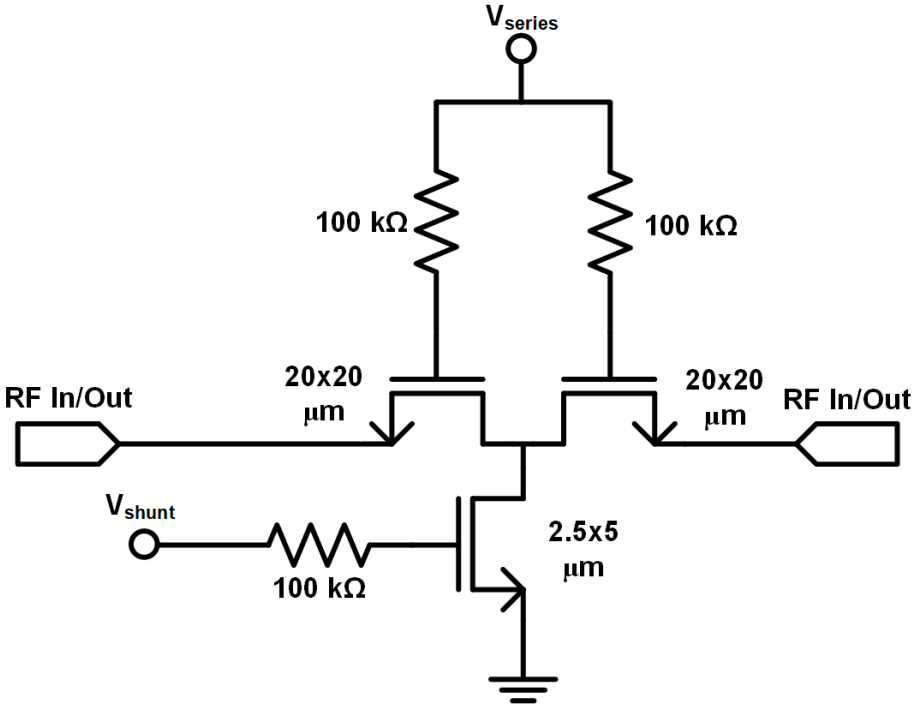

Figure 3.20 The schematic of the ultra-high precision VVA.

bank and switches such that for each attenuation state, the equivalent resistance of R_1 is obtained. This method may be feasible in theory; however, since the R_1

generally has a small resistance value, switches in this resistor bank should be very large, which increases the die area tremendously. Additionally, with the process and temperature variations, switches' performances would get affected, which leads to an unwanted change of resistance of R_1. Therefore, instead of implementing resistor bank topology, the branch with 10-kΩ resistor and R_1 is replaced with a voltage source. The reason for this method is that the resistance value of the series device in the T-type attenuator network is significantly smaller than 10-kΩ, in general. Therefore, the voltage at the negative input of the Op-Amp (V_2) can be formulated as in Eqn. (3.9) which is linear with the value of R_1 . Hence, the dummy series device's resistance can be pushed to the desired value without a reference resistor, and the $R^{'}_{series}$ can be found from Eqn. (3.10). It should be noted that to obtain ultra-high precision, required voltage steps can be as low as 10 - 100 μV; therefore, 8 stacked devices that are individually identical to the actual series device (R_{series}) are used to form the dummy series device ($R^{'}_{series}$) to increase the voltage step for better control. Hence, the multiplier (M) in the Eqn. (3.10) is equal to 8.

$$V_2 = \frac{V_{DD}}{10k\Omega} \times R_1. \tag{3.9}$$

$$R^{'}_{series} = R_{series} \times M = V_2 \times \frac{10k\Omega}{V_{DD}} \tag{3.10}$$

3.4.2 Design of the Sub-Blocks

One of the most important sub-blocks of the resistance sensing networks is the operational amplifiers (Op-Amp). Since the voltage difference between the positive and negative inputs is wanted to be very small, Op-Amps used in these loops should have a very high gain. In addition to this, input voltages of the Op-Amps in the resistance sensing networks are very close to 0 V; therefore, folded-cascode topology with PMOS inputs is preferred in this work. The schematic of the designed Op-Amp is shown in Fig. 3.21.

In addition to Op-Amp, an internal DAC is implemented to create the analog control voltage V_2 very precisely. Therefore, a 16-bit DAC with R-2R topology is designed, and the schematic of the DAC is shown in Fig. 3.22. Since the whole range of the

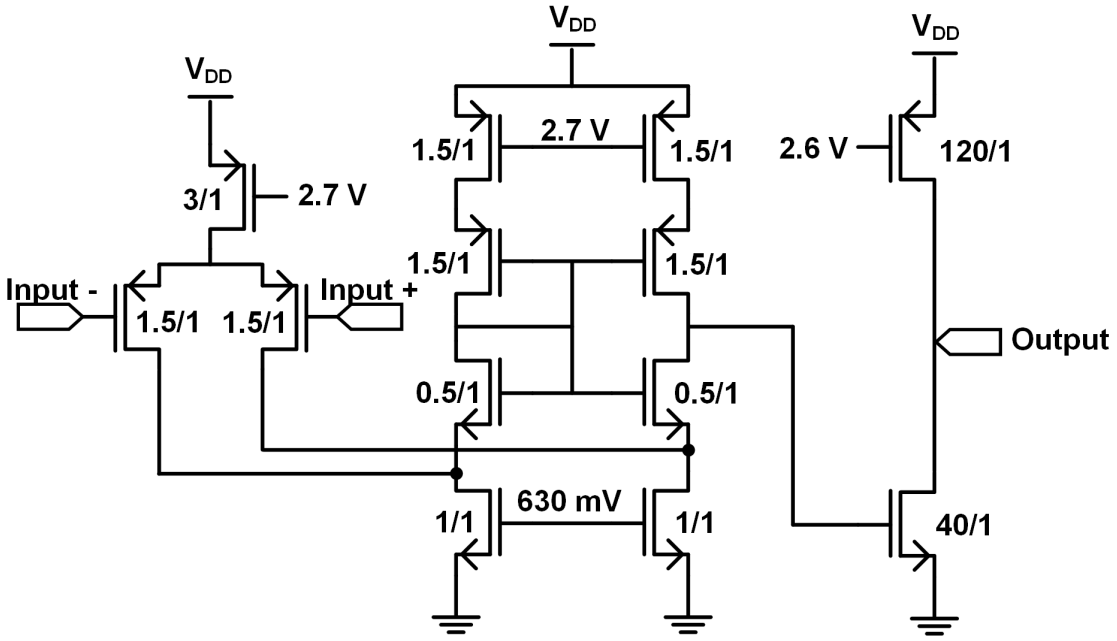

Figure 3.21 Schematic of the folded-cascode Op-Amp.

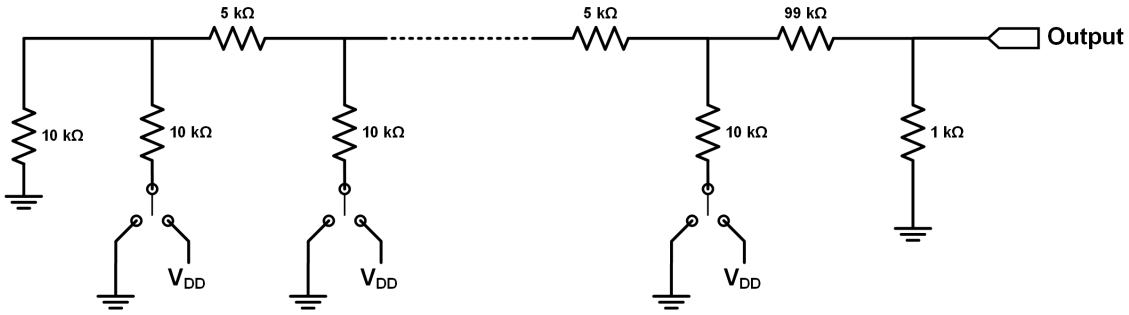

Figure 3.22 Schematic of 16-bit R-2R DAC.

DAC is from GND to V_{DD} which is 3.3 V, a resistive voltage divider with a 1:100 ratio is implemented to use the range of the DAC more effectively since linear-in-dB attenuation is only obtained for $V_2 < 31.7$ mV.

Finally, a 16-bit shift register is designed for the digital interface of the VVA, which converts serial input to parallel output, driving the 16-bit DAC. The schematic of the shift register is shown in Fig. 3.23.

3.4.3 Simulation Results

In this work, GlobalFoundries 130nm SOI CMOS technology has been used. Die layout is EM simulated by using Keysight's ADS Momentum software, and the die layout of the designed VVA is shown in Fig. 3.24. The total die area with pads is

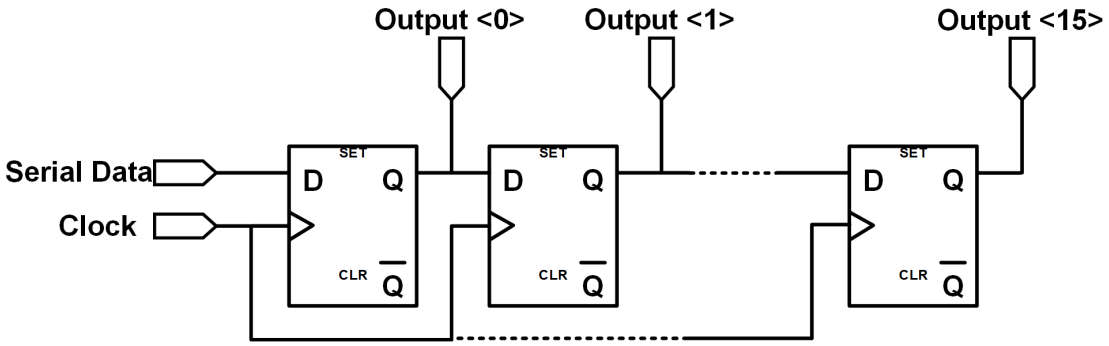

Figure 3.23 Schematic of 16-bit shift register.

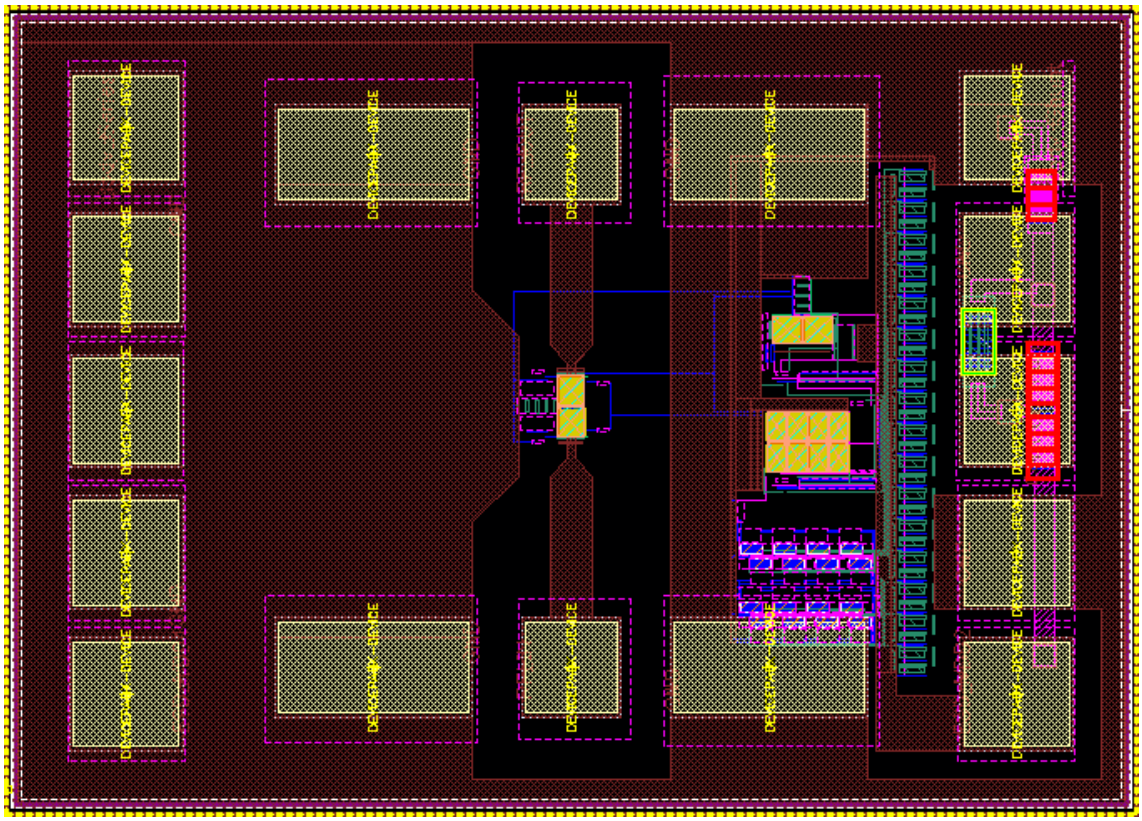

Figure 3.24 Die layout of the ultra-high precision VVA.

0.46 mm^2.

The simulated IL is smaller than 0.6 dB and the attenuation levels and S_{11} with respect to the digital code for different frequencies are shown in Fig. 3.25. In addition to frequency, the designed VVA is simulated for different supply voltage (V_{DD}) and temperature values at 1 GHz and simulation results are shown in Fig. 3.26. and Fig. 3.27.

Finally, the compression point (IP1dB) simulation is done by applying a single tone at 0.1, 1, and 10 GHz. Inside the whole bandwidth IP1dB $>$ 36.3 dBm and the linearity simulation results are shown in Table. 3.2.

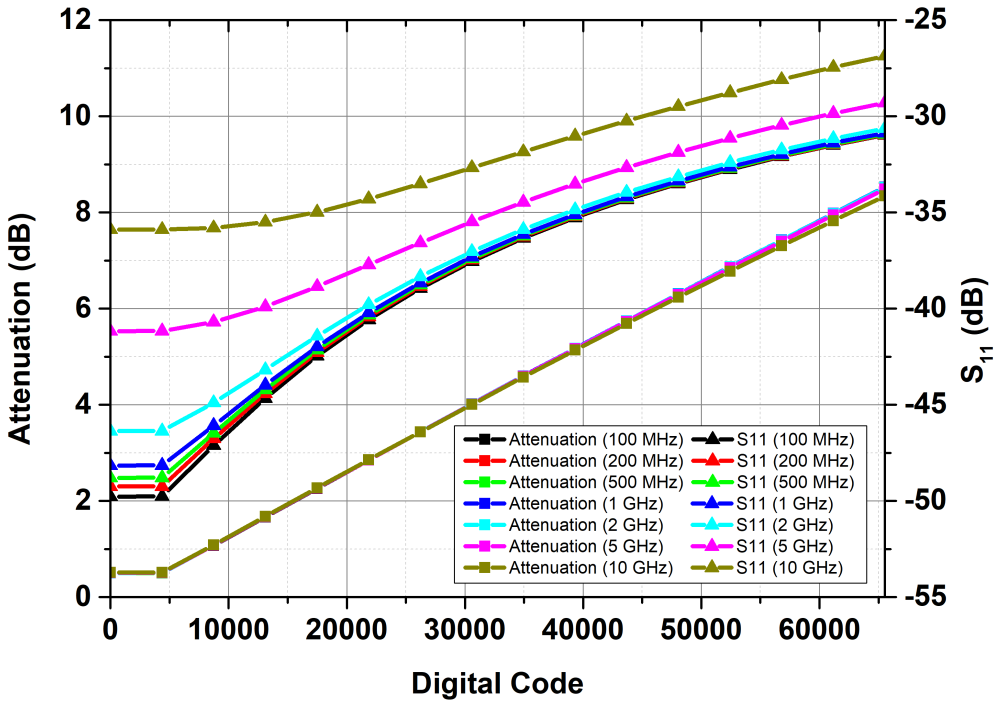

Figure 3.25 Simulated attenuation and S_{11} of the high precision VVA for different frequencies.

Table 3.2 Simulated IP1dB of the VVA for different frequencies.

Frequency (GHz)	IP1dB (dBm)
0.1	36.3
1	36.6
10	36.8

3.4.4 Conclusion

The designed high precision VVA achieves a very low IL of 0.6 dB and has a very high IP1dB performance of 36.3 dBm. The VVA has been able to achieve a very small attenuation step of 0.12 mdB/bit with its novel design methodology and closed control loops. Moreover, the VVA achieves an 8 dB attenuation range over DC - 10 GHz bandwidth while occupying a die area of 0.46 mm^2 with pads.

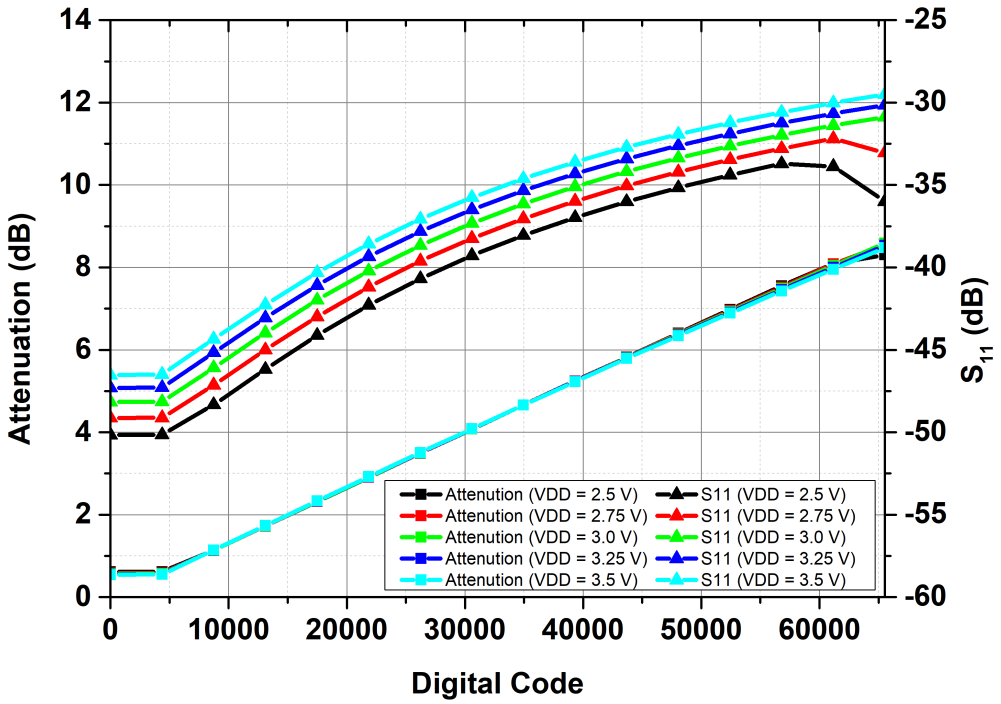

Figure 3.26 Simulated attenuation and S_{11} of the high precision VVA for different supply voltages at 1 GHz.

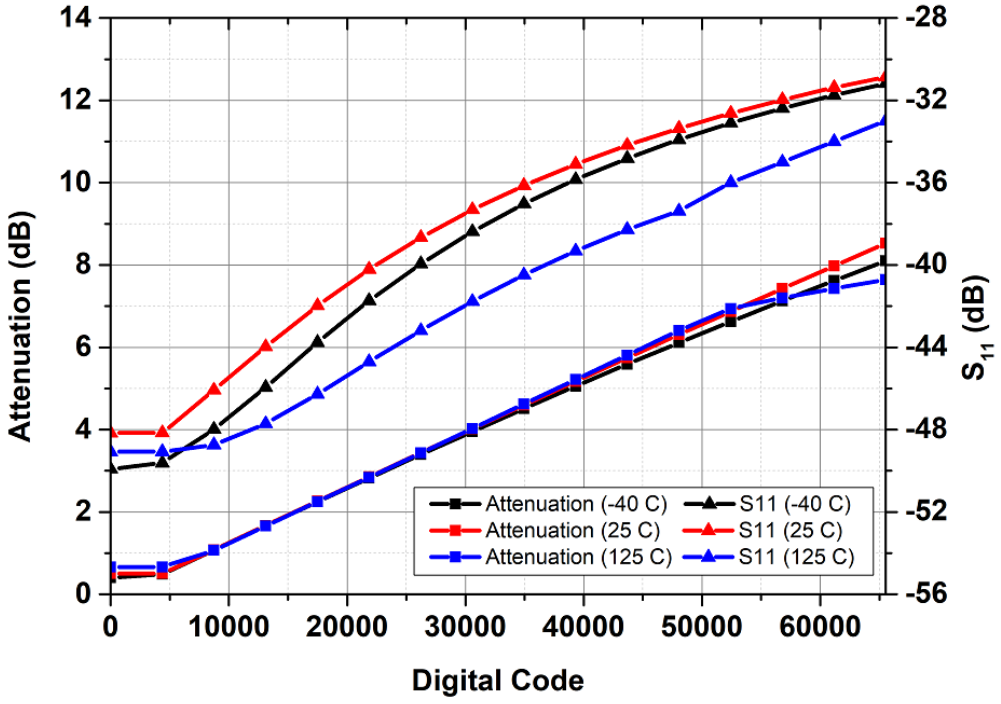

Figure 3.27 Simulated attenuation and S_{11} of the high precision VVA for different temperatures at 1 GHz.

4. CONCLUSION AND FUTURE WORK

4.1 Summary of Work

The next generation of communication systems (5G) is expected to require more challenging demands compared to 4G in the case of increased data rates, spectral efficiency, communication distance, and lower cost and latency. These highly demanding requirements can be achieved by employing new technologies, methods, and topologies.

In this thesis, a two-stage cascode SiGe BiCMOS LNA is designed and fabricated in IHP 130 nm SiGe BiCMOS technology. The reported LNA employs HBTs of the SiGe technology, which achieve f_T and f_{max} of 250 and 340 GHz. The designed LNA is on-wafer measured with GSG probes, and the LNA's performance is recorded as 27.7 dB gain and 1.15 dB NF while also reaching 31.9 dBm OIP3 and 14.5 dBm OP1dB. Moreover, reported LNA occupies 0.75 mm^2 of die area and consumes 98 mW DC power while operating. In addition to LNA designed with HBTs, two other LNAs are designed with GlobalFoundries' 130 nm SOI CMOS technology which employs FETs with f_T and f_{max} of 220 and 250 GHz. The reported LNAs have a gain of 30.5 dB and 0.85 dB NF. Furthermore, cascode-auxiliary LNA's OIP3 performance reaches 31.5 dBm while diode-connected auxiliary LNA's OIP3 reaches 35.5 dBm. Both LNAs are packaged with 4 x 4 mm^2 QFN packages and consume 246 mW DC power while operating.

In addition to LNAs, two novel attenuators are also designed with GlobalFoundries' 130 nm SOI CMOS technology. The first VVA is designed to cover a very wide bandwidth of DC - 27 GHz while also achieving a wide attenuation range of 16 dB with 0.25 dB steps with a single attenuator stage. Due to consisting of a single stage, this VVA achieves a very low IL of 1.7 dB and occupies a 0.0048 mm^2 die

area. The second VVA aims for ultra-high precision attenuation operation where 0.12 mdB/bit operation is achieved between DC - 10 GHz frequency range. It also employs high-power devices and with optimized device sizing IP1dB is simulated as 36.3 dBm. The total die area of the second VVA is 0.46 mm^2 with pads.

4.2 Future Work

In the near future, ultra-high precision VVA should be prepared for tape-out, and after the fabrication, measurements should be completed to verify the simulation results. In a more distant future, the linearity performance of this VVA can be improved by adding stacked devices which makes voltage division across the device possible and improves the IP1dB performance. Furthermore, wide-band VVA has room for improvement of control easiness by implementing internal DACs and digital circuitry with an attenuation-control voltage look-up table. The look-up table and DACs can be utilized such that required voltage values are applied when the wanted attenuation level is specified. Finally, post-distortion circuits of the SOI CMOS LNAs can be further optimized for more effective IM3 cancellation.

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