4X1 MIMO COMPACT HALF DUPLEX RF T/R MODULE WITH HIGH RESOLUTION IN 130 NM SIGE BICMOS FOR 5G APPLICATIONS

by
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Submitted to the Graduate School of Engineering and Natural Sciences
in partial fulfilment of
the requirements for the degree of Doctor of Philosophy

Sabancı University
July 2021

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Approved by:

Date of Approval: July 14, 2021

ABSTRACT

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ABDURRAHMAN BURAK

EE, PhD Thesis, 2021

Dissertation Supervisor: Prof. Yaşar GÜRBÜZ

Keywords: 5G, beamforming, phased array, TX/RX, SiGe BiCMOS

This thesis focuses on the design and implementation of a radio frequency (RF) integrated transmit/receive (T/R) module for the next-generation 5G communication. To achieve the performance requirements of the 5G communication, such as high data rate and low latency, new design methodologies are needed such as multiple-input and multiple-output (MIMO), and millimeter-wave (mm-wave) based circuits. Moreover, low power dissipation and low area are also essential performance requirements for the next-generation communication to decrease the cost of the system. One of the requirements of 5G is a data rate up to 25 Gb/s. In order to meet this requirement, the bandwidth of communication must be increased, which is possible with mm-wave circuitry. However, a higher attenuation in the atmosphere occurs in mm-wave frequency. In order to compensate for this attenuation, MIMO half-duplex phased arrays can be realized to create a beam-steering with a desired gain.

This thesis presents four-element TX/RX circuits and a single-channel TRX for creating a beamformer for MIMO-based systems. Both ICs designed with SiGe BiCMOS technology for 5G applications specifically for 26 GHz.

First, four-element TX and RX channels are realized to create a 5G communication scheme at the mm-wave frequencies. These four-channel elements are based on sub-blocks: low noise amplifier (LNA), power amplifier (PA), phase shifter (PS), attenuator (ATT), variable gain amplifier (VGA), Wilkinson combiner, and serial peripheral interface (SPI). The designed circuitry achieved a 6-b phase control and 4-b amplitude control. To the best of the authors' knowledge, the designed module

achieved the highest phase and amplitude resolution, along with the highest amplitude range, and the lowest RMS amplitude error in the literature. Moreover, the designed module achieved 15.5 dB RX gain, 25.5 dB TX gain, 4.5 dB NF, 9.5 dBm OP1dB, and 50 mW power consumption which are acceptable performances with respect to the state-of-the-art.

Second, after realizing the four-element TX and RX channels, we realized that parameters such as, power consumption and area can be improved. These improvements will create a massive advantage while creating a phased array system. Also, we realized that we can increase the module's functionality by increasing the phase and amplitude resolution and adding a self built-in test to check whether the channel is working or not. Single-channel TRX is implemented with higher phase and amplitude resolution and lower chip area and power consumption. To achieve the aforementioned performance, two new techniques were performed. First, to decide the mode of operation, conventional switch topology, asymmetric switches, and switchless LNA and PA are realized. Second, phase and amplitude will be adjusted with a single block for the first time. The current steering technique will be used for both phase and amplitude resolution in a single block. Since the asymmetric switch and switchless topology consume less area with lower insertion-loss performances and the vector modulator performs the phase and amplitude settings with the single block, the area and the power consumption of the overall module will be reduced. Based on the measurement results, the designed circuitry achieved 7-bit phase and 6-bit amplitude resolution, which corresponds to the highest phase and amplitude resolution in the literature. While achieving the highest phase and amplitude resolution, the lowest RMS phase and amplitude error are also achieved with a single block. Moreover, the designed circuitry achieved 19 dB gain in RX mode, 20 dB gain in TX mode, 5 dB NF, and 11.5 dBm OP1dB are also achieved, which are enough to create a 5G communication scheme.

ÖZET

5G UYGULAMALARI İÇİN 130 NM SIGE BICMOS'TA YÜKSEK ÇÖZÜNÜRLÜKLÜ 4X1 MIMO KOMPAKT YARIM DUPLEKS RF T/R MODÜLÜ

ABDURRAHMAN BURAK

Elektronik Mühendisliği 2021

Tez Danışmanı: Prof. Dr. Yaşar GÜRBÜZ

Anahtar Kelimeler: 5G, hüzmeleme, faz dizi anten, TX/RX, SiGe BiCMOS

Bu tez, yeni nesil 5G iletişimi için radyo frekansında (RF) entegre gönderme/alma (T/R) modülünün tasarımı ve gerçeklenmesi üzerinedir. 5G iletişiminde yer alan yüksek veri hızı ve düşük gecikme süresi gibi performans gereksinimlerine ulaşmak için çoklu giriş ve çoklu çıkış (MIMO), milimetre dalga (mm dalga) gibi yeni metodolojilere ihtiyaç vardır. Düşük güç kaybı ve düşük alan da sistemin maliyetini düşürmek için yeni nesil iletişim için önemli performans gereksinimlerindendir. 5G'nin gereksinimlerinden biri, 25 Gb/sn'ye kadar veri hızıdır. Bu gereksinimi karşılamak için, mm dalga devresi ile mümkün olan iletişimin bant genişliği arttırılmalıdır. Bununla birlikte, atmosferde daha yüksek bir zayıflama mm-dalga frekansında meydana gelir. Bu zayıflamayı telafi etmek için, istenen kazançlı bir ışın yönlendirmesi oluşturmak için MIMO yarı çift yönlü faz dizileri gerçekleştirilebilir.

Bu tez, MIMO tabanlı sistemler için bir huzme oluşturucu oluşturmak için dört elemanlı TX/RX devreleri ve tek kanallı TRX devrelerini sunar. Her iki tasarım da 26 GHz'de 5G uygulamaları için SiGe entegre devreleri şeklinde tasarlanmıştır.

Tezde ilk olarak, mm dalga frekanslarında bir 5G iletişim şeması oluşturmak için iki ayrı dört kanallı TX ve RX tasarımları gerçekleştirilmiştir. Bu dört kanallı elemanlar alt bloklara dayanmaktadır: düşük gürültülü kuvvetlendirici (LNA), güç kuvvetlendiric (PA), faz kaydırıcı (PS), zayıflatıcı (ATT), değişken kazançlı kuvvetlendirici (VGA), Wilkinson birleştirici ve seri çevresel arabirim (SPI). Tasar-

lanan devre, 6-b faz kontrolü ve 4-b genlik kontrolü sağlamıştır. Yazarların bildiği kadarıyla, tasarlanan modül, literatürdeki en yüksek genlik aralığı ve en düşük RMS genlik hatası ile birlikte en yüksek faz ve genlik çözünürlüğünü elde etmiştir. Ayrıca tasarlanan modül, son teknolojiye göre kabul edilebilir performanslar olan 15.5 dB RX kazancı, 25.5 dB TX kazancı, 4.5 dB NF, 9.5 dBm OP1dB ve 50 mW güç tüketimi elde etmiştir.

Tezde ikinci olarak, dört elementli TX ve RX kanallarını gerçekleştirdikten sonra güç tüketimi ve alan gibi parametrelerin iyileştirilebileceğini fark ettik. Bu iyileştirmeler, faz dizileri sistemi oluştururken büyük bir avantaj yaratacaktır. Ayrıca faz ve genlik çözünürlüğünü artırarak ve kanalın çalışıp çalışmadığını kontrol etmek için kendi kendine yerleşik bir test ekleyerek modülün işlevselliğini artırabileceğimizi fark ettik. Bu doğrultuda, tek kanallı TRX, daha yüksek faz ve genlik çözünürlüğü ve daha düşük çip alanı ve güç tüketimi ile gerçekleştirilmiştir. Yukarıda belirtilen performansları elde etmek için iki yeni teknik uygulandı. İlk olarak, çalışma moduna karar vermek için geleneksel anahtar topolojisi, asimetrik anahtarlar ve anahtarsız LNA ve PA ile gerçekleştirildi. İkinci olarak, faz ve genlik literatürde ilk defa tek blok ile ayarlanacaktır. Akım yönlendirme tekniği, tek bir blokta hem faz hem de genlik çözünürlüğü için kullanılacaktır. Asimetrik anahtar ve anahtarsız topoloji daha düşük ekleme-kayıp performansları ile daha az alan tükettiğinden ve vektör modülatörü faz ve genlik ayarlarını tek blok ile yaptığından, tüm modülün alanı ve güç tüketimi azalacaktır. Ölçüm sonuçlarına göre tasarlanan devrede literatürdeki en yüksek faz ve genlik çözünürlüğüne karşılık gelen 7 bit faz ve 6 bit genlik çözünürlüğü elde edilmiştir. En yüksek faz ve genlik çözünürlüğü elde edilirken, en düşük RMS faz ve genlik hatası da tek bir blok ile elde edilmiştir. Ayrıca tasarlanan devrede RX modunda 19 dB kazanç, TX modunda 20 dB kazanç, 5 dB NF ve 11.5 dBm OP1dB de elde edilmiş olup, bunlar 5G iletişim şeması oluşturmak için yeterlidir.

ACKNOWLEDGEMENTS

First of all, I would like to thank my supervisor Prof. Yaşar GÜRBÜZ, for his invaluable guidance over the past nine years. I am also thankful his confidence on me and his support, dedication and endless support. His vast expertise and support have made this thesis possible and I enjoyed working with him.

In addition to my thesis advisor, I would also like to thank my thesis jury members, Prof. Erkay SAVAŞ, Asst. Prof. Erdinç ÖZTÜRK, Prof. Serkan TOPALOĞLU, Assoc. Prof. Ahmet ÖNCÜ for their valuable time to spare in my thesis committee and for their precious comments, advice, and feedback.

I am very thankful my friends and colleagues Ilker Kalyoncu and Şeyma Kalyoncu for their friendship and endless supoort over the last years. I would like to thank Dr. Melik YAZICI, Hamza KANDİŞ, Işık Berke GÜNGÖR, and Tahsin Alper ÖZKAN for their contribution on this work.

I also want to thank to my friends and colleagues at the Sabanci University Microelectronics Research Group (SUMER), Dr. Omer CEYLAN, Cerin Ninan KUNNATHARAYIL, Umut Barış GÖĞEBAKAN, Kutay ALTINTAŞ, Cengizhan KANA, Ali Bahadır ÖZDÖL, Erkut GÜROL, Ajten FEJZULLAHU, and Nezih Kaan VEZİROĞLU for their friendship which makes the working environment comfortable for me and keep me motivated, the former members of SUMER Eşref TÜRKMEN, Emre Can DURMAZ, Alper GÜNER, and Atia SHAFIQUE, Elif Gül ARSOY for their support and guidance. I also thank the laboratory specialist, Ali Kasal since he did not complain about my endless wirebonding, flip-chipping, and PCB requests. I am also grateful to Ahmet Can, Metin, Onur, Ozan, and Recep and many others for their friendship throughout the years in high school and university.

I would like to thank my parents Huriye and Erdal and my sister Betül for their unconditional love. Also I would like to thank my dear wife, Betül for her unconditional love and endless support. I would not come that far without her support and the sacrifices her made.

Fianlly, I would like to thank ASELSAN for supporting my thesis dissertation. Also I would like to thank Scientific and Technological Research Council of Turkey (TÜBİTAK) BIDEB 2211-A program for supporting me with scholarships throughout my studies.

Eşime ve aileme...
To my wife and my family...

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LIST OF ABBREVIATIONS

AF: Array Factor
AM: Amplitude Modulation
ASYM: Asymmetric Switch
ATT: Attenuator
BPSK: Binary Phase Shift Keying
CB: Common-Base
CE: Common-Emitter
COTS: Custom Off-The-Shelf
CPWG: Co-Planar Waveguide with lower Ground plane
DBF: Digital Beam Forming
EIRP: Equivalent Isotropically Radiated Power
FM: Frequency Modulation
fMax: Maximum Oscillation Frequency
FOM: Figure-of-Merit
fT: Maximum Transit Frequency
GaAs: Gallium-Arsenide
HD: Half-Duplex
HP: High Pass
IC: Integrated Circuit
IHP: Innovations for High-Performance Microelectronics
IIP3: Input-Referred Third-Order Intercept Point
IL: Insertion Loss
IMD: Intermodulation Distortion
InP: Indium phosphide
iNMOS: Isolated NMOS
IP1dB: Input 1-dB Compression Point
LNA: Low Noise Amplifier
LO: Local Oscillator
LP: Low Pass
LTE: Long-Term Evolution

MIM: Metal-Insulator-Metal
MIMO: Multiple-Input Multiple-Output
MMIC: Monolithic Microwave Integrated Circuits
mm-Wave: Millimeter-wave
NF: Noise Figure
OIP3: Output-Referred Third-Order Intercept Point
OP1dB: Output 1-dB Compression Point
PA: Power Amplifier
PAE: Power-Added-Efficiency
PS: Phase Shifter
QAM: Quadrature Amplitude Modulation
RADAR: Radio Detecting And Ranging
RF: Radio Frequency
RMS: Root Mean Square
RX: Receiver
SAW Surface Acoustic Wave
SiGe: Silicon-Germanium
SNR: Signal-to-Noise Ratio
SPDT: Single-Pole Double-Throw
SPI: Serial Peripheral Interface
T/R: Transmit/Receive
TDD: Time Division Duplex
TX: Transmitter
VGA: Variable Gain Amplifier
VM: Vector Modulator

1. INTRODUCTION

1.1 A Brief History of Mobile Communication

The concept of mobile communications is based on the predicted solutions of Maxwell equations which is the propogation of electromagnetic waves is at the speed of light in the mid-1860s (Maxwell (1873)). This predicted solution is verified by Marconi's first radiotelegraph in the 1880s (Ramsay (1958)). In 1947, the theory of mobile communication had firstly introduced by the Bell System (AT&T) as a "broadband urban mobile system" (Shannon (1948)). The first cellular communication system (1G) is implemented in 1983 by Bell laboratories. It is based on sending and receiving analog voice via analog modulation techniques, circuit switching, and frequency division multiple access (FDMA) (Blecher (1980)). Almost every ten years, due to the demands for applications and the bandwidth requirement for mobile communication, new cellular communication systems were developed continuously (Onoe (2016)).

Historically, the second generation (2G) is implemented in 1991. Unlike 1G, the primary services are in the digital domain. The bandwidth of the cellular communication is increased from 1.9 kbps to 14.4 kbps (Rahnema (1993)). Moreover, Short Message Service (SMS) and Multimedia Message Service (MMS) were also introduced in 2G. The dominant services in 2G are Code Division Multiple Acces (CDMA) and Time Division Multiple Access (TDMA) (Gilhousen, Jacobs, Padovani, Viterbi, Weaver & Wheatley (1991); Rahnema (1993)). These new applications in 2G have a worldwide success which leads to new demands. As a result, third-generation (3G) cellular communication was introduced in 2002. New applications such as mobile internet, video call, and online gaming are also realized thanks to the several Mbps bandwidths and wideband CDMA services (Dahlman, Gudmundson, Nilsson & Skold (1998)). In the early 2010s, there are several reasons to introduce the

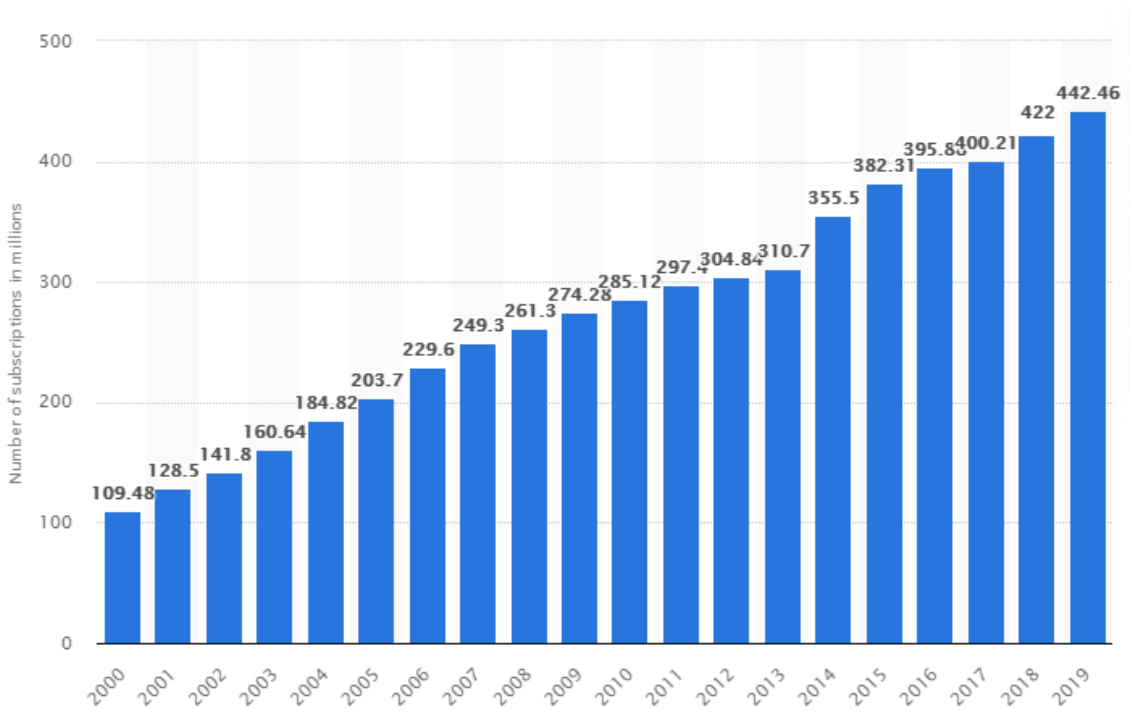


Figure 1.1 The number of mobile cellular subscriptions in USA from 2000 to 2019 (O'Dea (2021))

	Various generations				
Technology	**1G**	**2G**	**2.5G**	**3G**	**4G**
Design began	1970	1980	1985	1990	2000
Implementation	1984	1991	1999	2002	2012–2015
Service	Analogue voice	Digital voice	High-capacity packets, MMS	High-capacity broadband data	Higher capacity, completely IP, Multimedia
Multiple access	FDMA	TDMA, CDMA	TDMA, CDMA	CDMA	OFDMA
Standards	AMPS, TACS, NMT	CDMA, GSM, PDC	GPRS, EDGE	WCDMA, CDMA2000	Single standard
Bandwidth	1.9 kbps	14.4 kbps	384 kbps	2 Mbps	200 Mbps
Core network	PSTN	PSTN	PSTN, Packet network	Packet network	Internet

Figure 1.2 History of 1G, 2G, 3G, and 4G standards (Rao (2012))

fourth generation (4G) cellular communication. Firstly, as shown in Fig. 1.1, from the 1G, the number of cellular subscribers is increased exponentially (O'Dea (2021)). There was a growing demand for broadband Internet access (Bogdan-Martin (2021)). Also, like 3G, new applications such as HD video streaming and mobile multimedia demands a hundred Mbps data rates (Khan, Qadeer, Ansari & Waheed (2009)). In 2000, International Telecommunication Union - Radiocommunication Sector (ITUR) targeted new bandwidths for mobile communications for 4G: 100 Mbps for mobile

communication and 1 Gbps for immobile, fixed communication networks (Li, Li, Lee, Lee, Mazzarese, Clerckx & Li (2010)). In order to achieve these data, new methodologies such as the Orthogonal FDMA (OFDMA) were employed (Han & Lee (2005)). Moreover, the core network for 4G is the Internet Protocol (IP) packet switching. The standard definitions of mobile communications are summarized in Fig. (1.2).

1.2 The Fifth Generation Cellular Communication

Although 4G LTE has outstanding achievement in terms of bandwidth, latency, applications such as internet-of-things (IoT), machine-to-machine communications, wearable electronics, autonomous cars/drones, smart cities, and remote medical services require higher speed, low latency, high data rates, better robustness, and energy efficiency. These applications cannot be realized with 4G LTE. As a result, 5G comes into existence to create a solution to achieve these applications (Andrews, Buzzi, Choi, Hanly, Lozano, Soong & Zhang (2014); Boccardi, Heath, Lozano, Marzetta & Popovski (2014); Rappaport, Sun, Mayzus, Zhao, Azar, Wang, Wong, Schulz, Samimi & Gutierrez (2013)).

ITU set some milestones for the 5G technology by taking account of these applications. Since the number of connected devices to the Internet will increase too much with the IoT, the higher data rate is a necessity for 5G communication. Therefore, the peak downlink data rate of up to 25 Gb/s, an uplink data rate of up to 10 Gb/s are set as a goal (Romano (2019)). These requirements mean that 25 bits/s/Hz uplinks spectral efficiency and 10 bits/s/Hz downlink spectral efficiency. Another requirement for this type of application is the number of simultaneous connections. The minimum requirement for this number is set at 1 million per km^2. For the applications such as smart cities, remote medical services autonomous cars/drones, latency is the crucial factor. The maximum latency is set as 1 ms (Niknejad, Thyagarajan, Alon, Wang & Hull (2015)). Moreover, cost efficiency must be 10 times better than 4G. The requirements of 5G is summarized in Fig. 1.3 (Romano (2019)).

In order to meet these requirements, five disruptive technological changes in communication are expected. First, unlike the 4G, instead of base-centric communications, device-centric architectures are expected (Andrews (2013)). Second, to increase the data rates, it is inevitable that mm-wave will be used (Rappaport et al. (2011)).

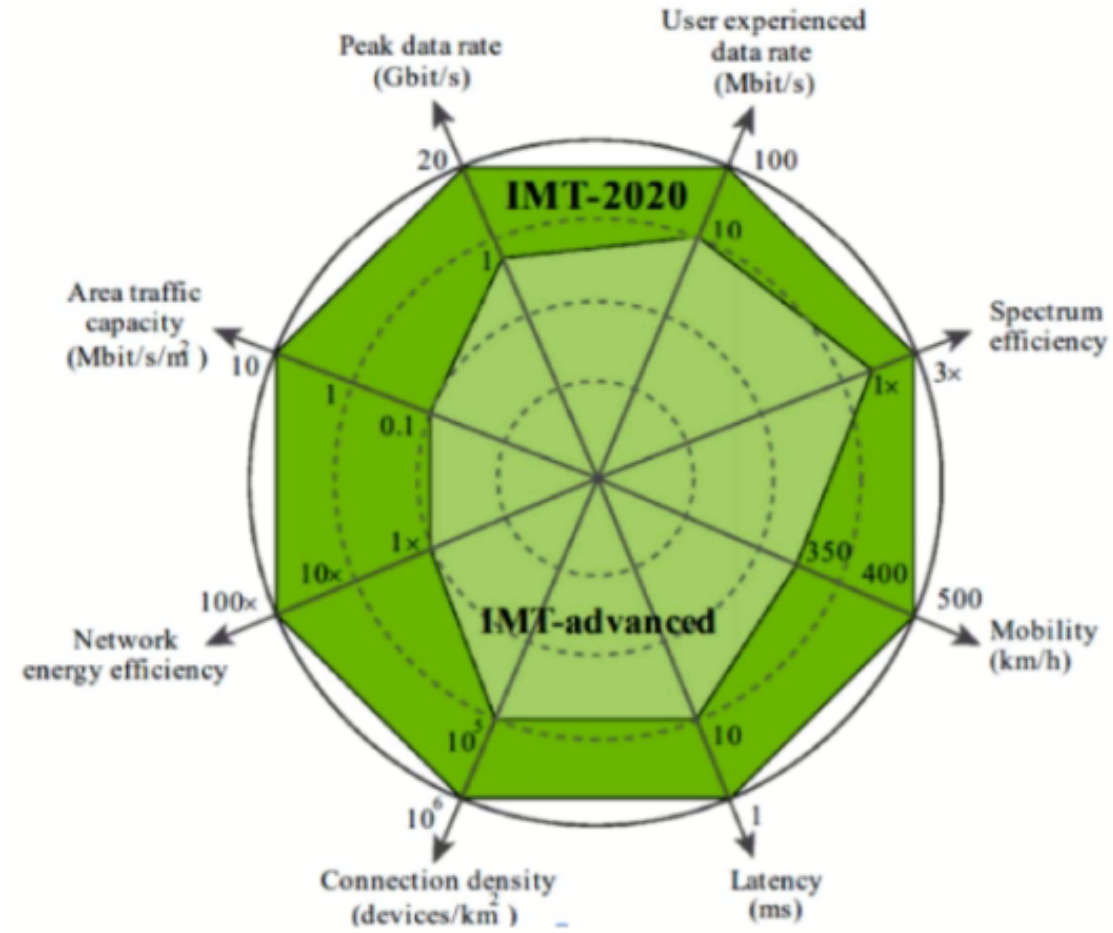


Figure 1.3 The requirements of 5G (Romano (2019))

Third, massive MIMO creates an excellent opportunity to compensate for the atmospheric attenuation and multi-beam (Rusek, Persson, Lau, Larsson, Marzetta, Edfors & Tufvesson (2013)). Fourth, device-to-device communication will be available, and it will create an opportunity for more intelligent devices (Boccardi et al. (2014)). Lastly, there will be support for a machine-to-machine connection which will create a massive number of connected devices (Oliveira, Pereira, Misoczki, Aranha, Borges, Nogueira, Wangham, Wu & Liu (2018)).

As mentioned previously, data rates up to 25 Gb/s can be achieved with mm-wave (30-300 GHz) circuits. Therefore, it is expected that 5G phased arrays will operate in mm-wave frequencies. Moreover, thanks to mm-wave carrier frequencies, larger bandwidth allocations will be available. Higher data rates can only be possible with the larger bandwidth. Service providers can use beyond the present 20 MHz channels used by 4G customers. However, due to the operating frequency of these circuits, as shown in Fig. 1.4, the atmospheric attenuation of the signal will be high (Rappaport et al. (2011)).

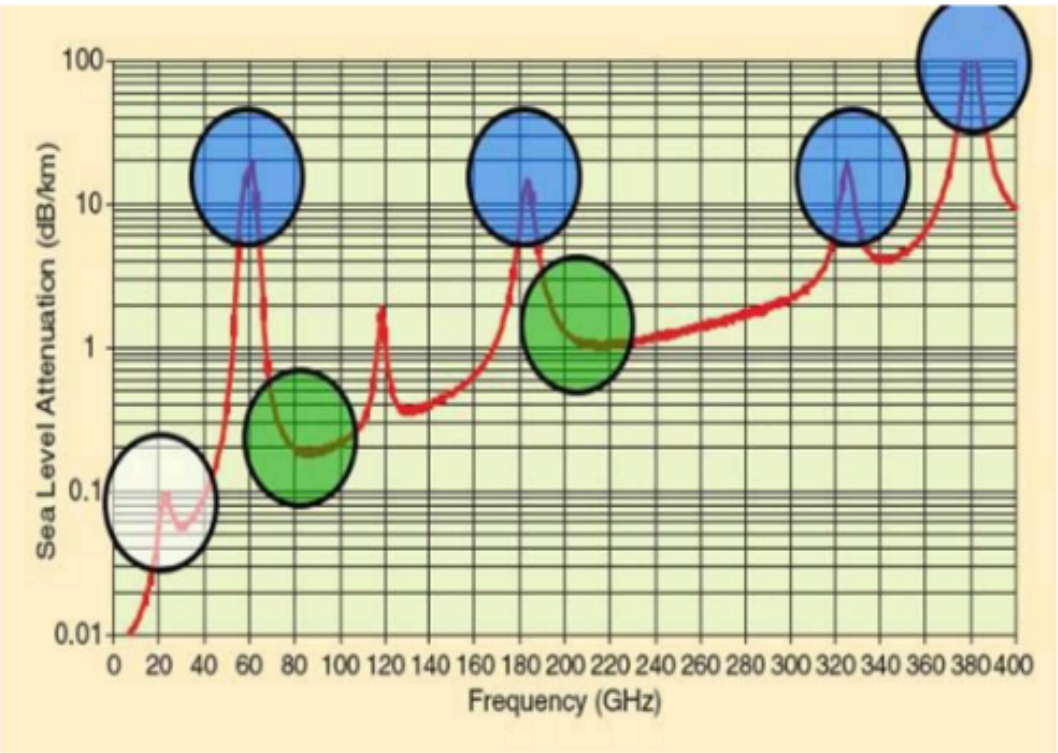


Figure 1.4 Atmospheric attenuation across mm-wave frequencies in dB/km (Rappaport et al. (2011))

Moreover, mm-wave frequencies are more susceptible to outside effects such as the weather and obstacles too much. MIMO (multiple-input, multiple-output) phased arrays are offered as a solution to overcome the high attenuation problem. It also offers a multi-user connection at the same time (Rusek et al. (2013)). Also, today's cell sizes in an urban environment are around 200 meters which will not create a high attenuation, especially for 28 GHz and 38 GHz. It is shown that the atmospheric attenuation is 1.4 dB at 28 GHz over 200 meters (Qingling & Li (2006)). Taking everything into account, MIMO phased arrays at mm-wave frequencies will be an excellent candidate to create a communication scheme for 5G applications with high data rates.

Since the designed phased arrays will be a part of 1 million devices per km^2, phased arrays' power consumption and cost will also be crucial. The more power and cost-efficient designs will be one step ahead of all other designs since it will increase the duration of the battery time (Agiwal, Roy & Saxena (2016)).

1.3 Thesis Overview

This thesis aims to design and implement a radio frequency (RF) integrated transmit/receive (T/R) module for the next-generation 5G communication. To reach the performance requirements of the 5G communication, the bandwidth of the communication must be increased, which is possible with millimeter-wave (mm-wave) circuitry. As explained previously, MIMO will be designed in the mm-wave to compensate for higher attenuation in the atmosphere that occurs in mm-wave frequency. Furthermore, low power dissipation and low area are also essential performance requirements for the next-generation communication to decrease the cost of the system. In this thesis, two different ICs, MIMO four channel TX and RX and single channel TRX, will be realized to create a 5G communication system.

First, four-channel high-performance beamformer transmitter and receiver ICs with 6-b phase control and 4-b amplitude control capabilities are designed. In both ICs, 6-b phase shifter, a 3-b variable gain amplifier, 1-b attenuator, Wilkinson combiner/divider, and serial peripheral interface are employed. A low noise amplifier is employed on the receiver side, and on the transmitter side, the power amplifier is employed. To achieve high phase resolution, an I/Q vector-based phase shifter with the integration of DAC is realized. A 3-b linear-in-dB VGA is another example of the integration of DAC with the RF circuitry. To extend the amplitude range of the IC, a 1-bit attenuator is realized. The designed low noise amplifier is based on a cascode topology, and simultaneous power and noise matching are employed. The designed power amplifier is also based on the cascode topology. To reach high linearity, the number of transistors is optimized, and it is biased in Class-A. Four-channel separate transmitter and receiver are developed to target 5G phased-array communication systems.

Second, a single-channel transmit-receive IC module with improved functionality such as 7-b phase resolution, 6-b amplitude resolution, and built-in self-test is realized. Besides the functionality, power consumption and the area are also improved in the design by realizing a high-resolution phase and amplitude controller in a single block for the first time in the literature. Instead of conventional switch topology, asymmetric switch topology and switchless LNA/PA topology are employed to minimize the area and improve the NF and the linearity of the module. The designed phase and amplitude controller is based on the vector-sum phase shifter topology with the integration of DACs. Two different versions of DACs are realized to realize phase and amplitude control simultaneously. While one version of the DAC is

distributing the current between I and Q vectors to set the phase of the signal, the second version of the DAC determines the current level of both vectors to determine the amplitude of the signal. A series-shunt-based single pole double throw switch is also realized to determine the mode of operation. The designed amplifiers are based on the cascode topology. The power consumption of both amplifiers decreased in return for an acceptable NF and linearity loss.

1.4 Thesis Organization

The next chapter will explain the fundamentals of phased array systems. It will explain the fundamentals of MIMO phased arrays. At the end of this chapter, the current state-of-the-art 5G phased arrays, and 5G MIMO ICs will be presented.

In chapter 3, the analysis, design, and measurements of four-element MIMO TX and RX will be covered. First, the design procedure of each sub-block, which is employed in four-channel TX and RX, will be explained. Then, each sub-block's simulation and measurement results will be covered, and each one of them compared with the state-of-the-art. When we combine each sub-block, we will build four-element TX and RX beamformers. The simulation and measurement results of both ICs will be provided in this chapter as well.

In chapter 4, the analysis, design, and measurements of single-channel half-duplex TRX will be covered. Similar to chapter 3, the design procedure of each sub-block, which is employed in single-channel TRX, will be explained. Then, the simulation and measurement results of each sub-block will be covered, and each one of them compared with the state-of-the-art. This chapter will be concluded with the simulation and measurement results of single-channel TRX.

In the last chapter, this dissertation will summarize the findings and the impacts of both works. Moreover, this chapter also provides future works to transform from four-element TX and RX or single-channel TRX to phased array systems.

2. BACKGROUND

Radio Detection and Ranging (RADAR) history begin with the invention of "Telemobiloskop," a device operating at 650 MHz by German Cristian Hülsmeyer in May 1904. It is developed until World War II by different scientists, such as Nicola Tesla and Guglielmo Marconi (Guarnieri (2010)). The first version of RADAR was based on mechanical rotation. Although, mechanically scanned RADARs achieved hundreds of scans per minute and improved the performance, the mechanically scanned RADAR system is replaced with the electronically scanned arrays, which are called" phased arrays" to decrease the possibility of mechanical failure (Reed, Henry & Cosby (1997)) while increasing the performance.

2.1 Phased Array RADARs

2.1.1 Operating Principles

Fig. 2.1 depicts the block diagram of the phased array system in a receiver mode. Assume that the distance between each antenna is d, the ϕ is the angle where the signal comes from a source with that angle and the distance to reach the signal at N^{th} element can be found as (2.1).

$$x = N * d * sin(\theta) \tag{2.1}$$

That equation shows us that each antenna receives the signal with different time delays or phase shifts. In the following section, the comparison of these two phenomena will be covered.

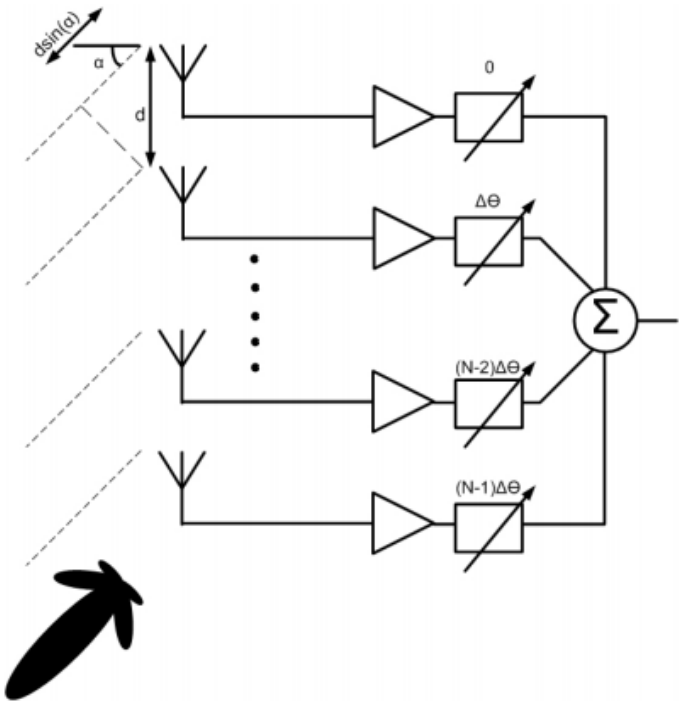


Figure 2.1 Basic receiver block diagram of phased array system.

2.1.1.1 Time Delay vs. Phase Shifting

Time delay of each radiating element can be found from dividing the distance to the speed of the light (2.2).

$$t = \frac{N * d * sin(\theta)}{c}(\phi) \tag{2.2}$$

The phase difference of each radiating element can be found from the multiplication of the carrier frequency with the time delay (2.3).

$$\phi = w_c * t \tag{2.3}$$

That phase difference can be rewritten as (2.4).

$$\phi = 2\pi * \frac{d * (\theta)}{\lambda} \tag{2.4}$$

These time delay and phase difference equations will be used for defining transmitted or received signals. The received or transmitted signal at the N_{th} element can be

defined as (2.5).

$$
\begin{aligned}
S_0(t) &= A * cos(w * t + \phi_0(t)) \\
S_N(t) &= S_0(t - N\delta\phi) \\
S_N(t) &= A * cos(w - (t - N * \delta t) + (\phi(t - N\delta\phi)))
\end{aligned}
\tag{2.5}
$$

This is the summary of the working principle of phased arrays. Based on these equations, two different solutions can be performed: Time delay-based phased arrays and phase shifter-based phased arrays. Time delay-based phased arrays are not dependent on the frequency. Therefore, they are generally wideband solutions. However, their insertion-loss is enormous, and therefore they are not generally select as a solution. The alternative way, which the one based on phase shifters, is the dominant one to create a beamformer (Pozar (1994)).

2.1.1.2 Beam Steering and Array Factor

In phased array systems, by adjusting the phase of each radiating element, the main beam direction can be steered. The angle between the main beam direction and the phased array is dependent on the distance between each radiating antenna element and the incremental phase shift of each channel. There is an optimum distance between each antenna to obtain the best directivity of the antenna, which is $\lambda/2$.

The radiation pattern of an array can be calculated by multiplying the array factor and antenna element(Balanis (2016)). Normalized array factor of a long(L» λ) and uniform linear antenna array can be found from (2.6).

$$
AF = \frac{sin(N\frac{\phi}{2})}{N * sin(\frac{\phi}{2}}
\tag{2.6}
$$

Where N is the number of the antenna elements, from that equation, we can say that the more antenna we used, the narrower main beam we will obtain. As a drawback, more side lobe levels appear in the one period of the signal.

From these equations, we can say that there are some advantages of using phased arrays as receivers or transmitters. From the receiver side, if we have a gain called G, for the array number N, the overall summed power of the received signal can be

written as (2.7).

$$S_{received} = N^2 * G * S_{in} \tag{2.7}$$

The summed noise of the receiver side can be found from (2.8).

$$Noise_{sum} = N * G * (Noise_{antenna} + Noise_{receiver}) \tag{2.8}$$

It means that the SNR of the receiver side will increase in the ratio of N. It means the more radiating element leads the higher SNR. From the transmitter side, we can say that the summed transmitted power to the environment is directly dependent on the square of N (Mailloux (2017)).

2.1.2 Phased Array Architectures

In the literature, there are two different ways to categorize the phased array architectures. The antenna feeding is realized in the first categorization type of phased array systems: Passive phased arrays and Active phased arrays. Based on the phase-shifting functionality is realized is another categorization type of the phased array systems: Analog beamforming, Digital beamforming, and Hybrid beamforming.

2.1.2.1 Passive Phased Arrays

The Block diagram of the passive phased arrays is shown in Fig. 2.2. Passive phased arrays consist of a single PA and single LNA. In order to transmit with high power and receive with low noise, in other words, to maintain high bandwidth over the communication scheme, high output power PA in transmit mode and lower noise performance LNA in receiver mode are needed. PA and LNA are connected to multiple passive phase shifters and radiating elements via a circulator. The main advantage of using this type of phased array is the lowest power consumption. The main drawback of this type of phase shifter is that they are more prone to PA and LNA failure, and they have a high loss (Parker & Zimmermann (2002)).

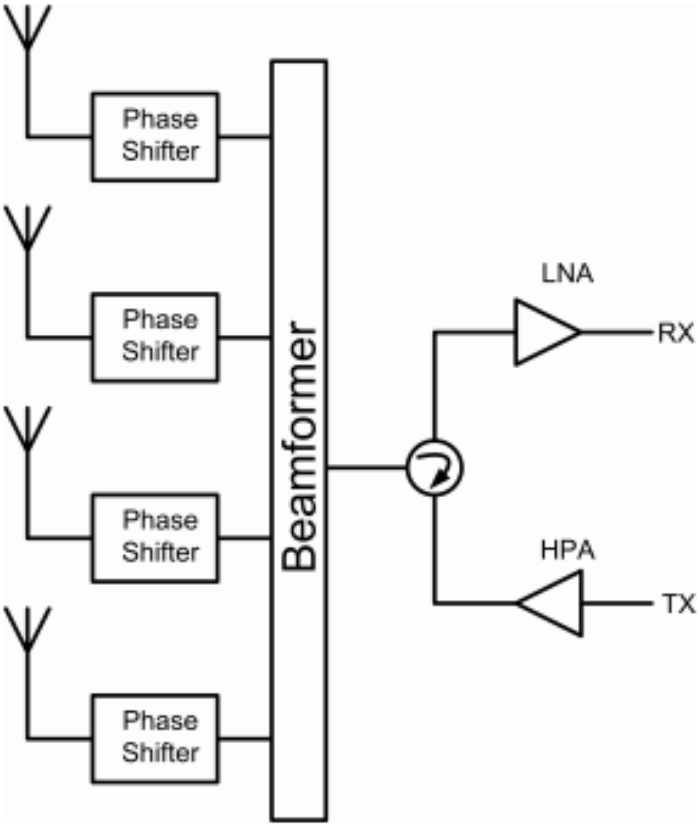


Figure 2.2 Block diagram of passive phased array.

2.1.2.2 Active Phased Arrays

Fig. 2.3 shows the block diagram of the active phased arrays. Each radiating element has an active transmit/receive (T/R) module, including PA, LNA, PS, and switches. The main advantage of active phased arrays is that the whole structure will not fail if one LNA or PA fails. The overall system has higher gain with respect to the passive phased arrays. The main disadvantage of this type of array is that it consumes higher power with respect to the passive phased arrays (Parker & Zimmermann (2002)).

2.1.2.3 Phased Arrays based Beamforming Techniques

Beamforming is the process of generating the desired beam shape in phased arrays. This can be realized in three ways: Analog, digital, and hybrid beamforming. In analog beamforming, as shown in Fig. 2.4a, a single mixer and an ADC are employed with T/R modules. Among other methods, the lowest power consumption is

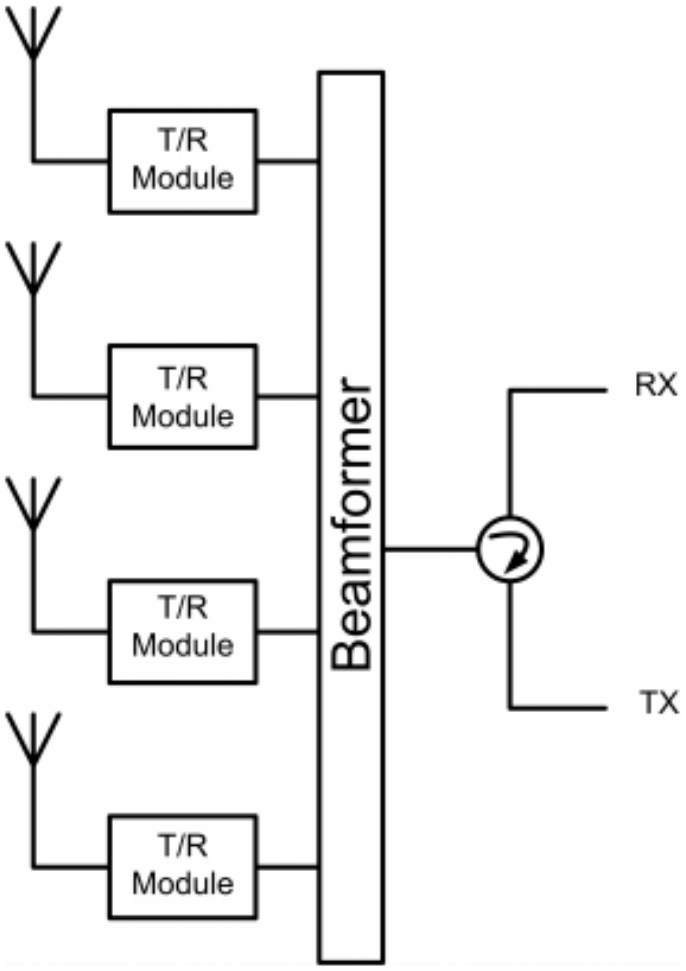


Figure 2.3 Block diagram of active phased array.

achieved with that method (Roth, Pirzadeh, Swindlehurst & Nossek (2018)). However, phase or time shift operations bring some challenges since they are realized in the RF domain. The drawbacks of this type of beamforming are narrow RF bandwidth, which increases with the number of beams (Venkateswaran & van der Veen (2010); Via, Santamaria, Elvira & Eickhoff (2010)). In digital beamforming, as shown in Fig. 2.4b, each channel has its mixer and ADC. Therefore, the power consumption increases dramatically. On the other hand, this type of beamforming supports multi-beam operation, which is necessary for the base stations. Moreover, since the phase and amplitude of the signal are adjusted in the IF domain, higher resolution can be achieved with this beamforming (Yang, Yu, Lan, Zhang, Zhou & Hong (2018); Zhang, Wu & Fang (2011)).

In hybrid beamforming, each channel cannot create its beam. However, since multiple ADCs/mixers are connected to more than one RF channel, multi-beam is supported in hybrid beamforming (Han, I, Xu & Rowell (2015); Molisch, Ratnam, Han,

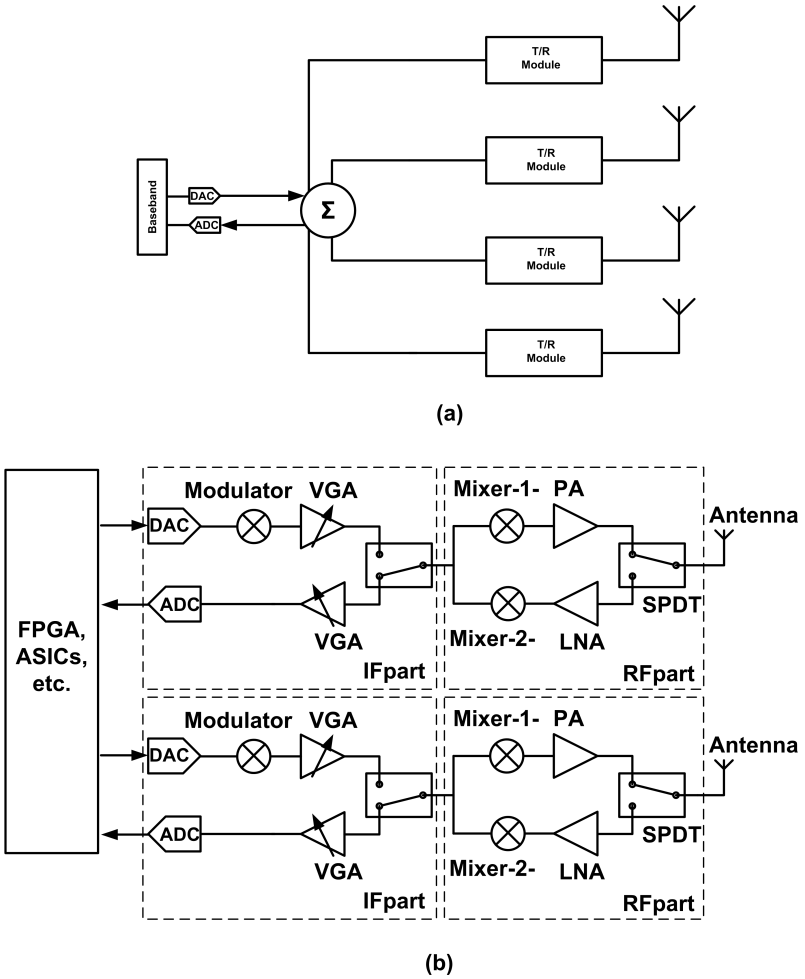


Figure 2.4 Beamforming architectures a) Analog b) Digital

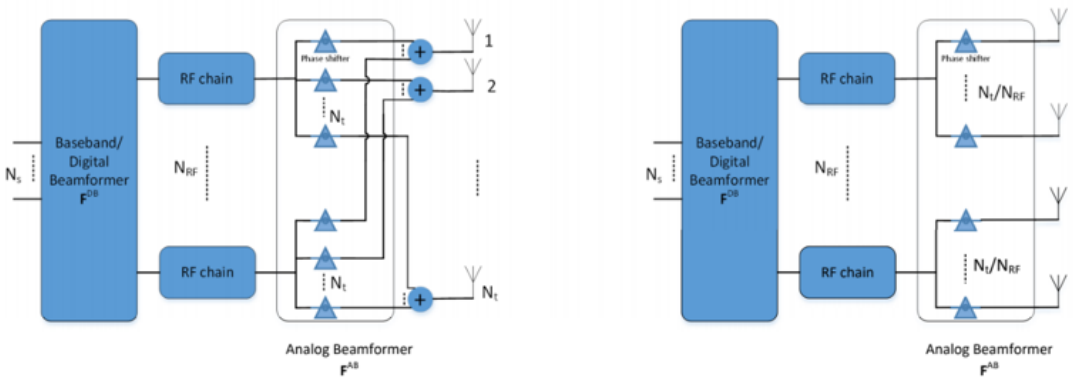


Figure 2.5 Hybrid beamforming architectures a) Fully-connected b) Sub-connected (Ahmed et al. (2018))

Li, Nguyen, Li & Haneda (2017); Méndez-Rial, Rusu, González-Prelcic, Alkhateeb & Heath (2016); Sohrabi & Yu (2016). For this approach, as shown in Fig. 2.5, two types of structure are realized: Fully-connected hybrid structure and Sub-connected hybrid structure. In a fully connected hybrid structure, assume A is the number

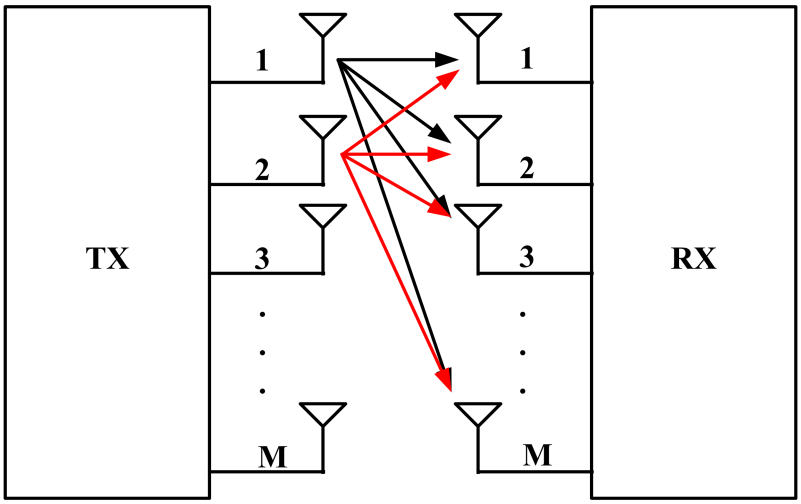


Figure 2.6 MxM MIMO System

of desired beam directions. Each ADC/mixer is connected to the A number of the phase shifter. It will increase the power consumption. On the other hand, it will increase spectral efficiency. In a sub-connected hybrid structure, each ADC/mixer chain is connected to A/N_{rf}, where N_{rf} is the number of RF channels, which will cost as A number of the phase shifter, overall. Although less power consumption is achieved with this type of beamforming, the gain of the beamformer is multiplied with $1/N_{rf}$ (Ahmed et al. (2018)).

2.2 MIMO Channel

To meet 5G requirements, it is inevitable that phased arrays will play an important role. As explained previously, to reach high data rates, up to 10 Gbps, circuits operate at the mm-wave frequencies are another requirement. Since the atmospheric attenuation is high at mm-wave frequencies, MIMO technologies with high antenna gain are the key variables. Multi-beam multiplexing technologies can reach high data rates in 5G (Rusek et al. (2013)). In MIMO channels, both transmit and receive antennas can be connected to the channel. In this way, the channel capacity increases thanks to the degree of freedom in gain and multi-beamforming. An example of the MxM MIMO system is shown in Fig. 2.6. M different multi-beam with lower beam gain or single beam with a higher beam gain can be realized with this structure.

2.2.1 MIMO Channel Link Capacity

The maximum channel capacity of the single channel is calculated by the Shannon-Hartley theorem, which is expressed as:

$$C = B * \log_2(1 + SNR) \tag{2.9}$$

where C is the channel capacity, B is the bandwidth. SNR is the ratio between the power of the signal and the noise of the signal (Pierce (2014); Shannon (1948)). It is known that noise can be written as:

$$N = k * T * B \tag{2.10}$$

When we combine these two equations, there is an optimum point for the bandwidth of the signal to reach the maximum channel link capacity which can be found from:

$$\frac{dC}{dB} = \log_2(1 + S/N) + \frac{-1}{N+S}\log_2(e) = 0 \tag{2.11}$$

where S is calculated from Friis equation as:

$$S = P_t * G_t * \frac{c}{4 * pi * f_c * d} * G_r \tag{2.12}$$

where P_t is the transmitted power, G_t and G_r are the gain of the transmitter and receiver, respectively, and d is the communication distance (Friis (1946)). It is obvious that the channel link capacity is directly proportional to P_t, G_t, and G_r and inversely proportional to d.

Suppose we assume that transmitted power is 0 dBm, with the transmitted gain as 100 and the received gain as 10, the bandwidth of the channel vs. the channel link capacity can be seen from the Fig. 2.7. The highest channel link capacity is achieved when the bandwidth is selected as 170 MHz at the center of 28 GHz.

When we consider the spatial multiplexing, a multiplexing technique in MIMO communications, the channel link capacity becomes:

$$C = B * \log_2(det(I + \frac{SNR}{n} H^N * H)) \tag{2.13}$$

where I is the unit matrix, n is the number of channels, and H is a time invariant channel matrix, which explains the correlation between MIMO channels. If the

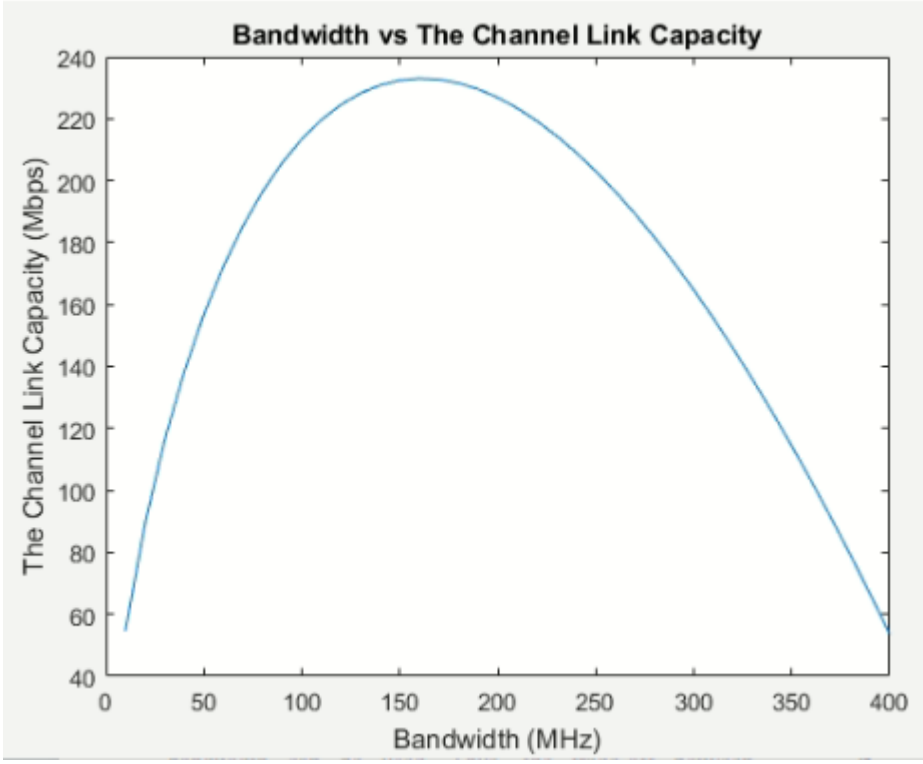


Figure 2.7 The channel link capacity vs the selected bandwidth of the channel.

spatial correlation equals to 1, the channel link capacity summarizes as:

$$C = B * \log_2(1 + n * SNR) \tag{2.14}$$

if the spatial correlation equals to 0, the channel link capacity summarizes as:

$$C = B * n * \log_2(1 + \frac{SNR}{n}) \tag{2.15}$$

. These equations show us using the n number of MIMO channels will directly increase the channel link capacity (Chiurtu, Rimoldi & Telatar (2001); Tokgoz & Okada (2019)).

Suppose we assume that transmitted power is 0 dBm, with the transmitted gain as 100 and the received gain as 10, the bandwidth of the channel vs. the channel link capacity can be seen from the Fig. 2.8. The highest channel link capacity is achieved when the bandwidth is selected as 1.7 GHz at the center of 28 GHz. As can be seen from this figure, ten times higher channel link capacity is achieved with MIMO with ten channels.

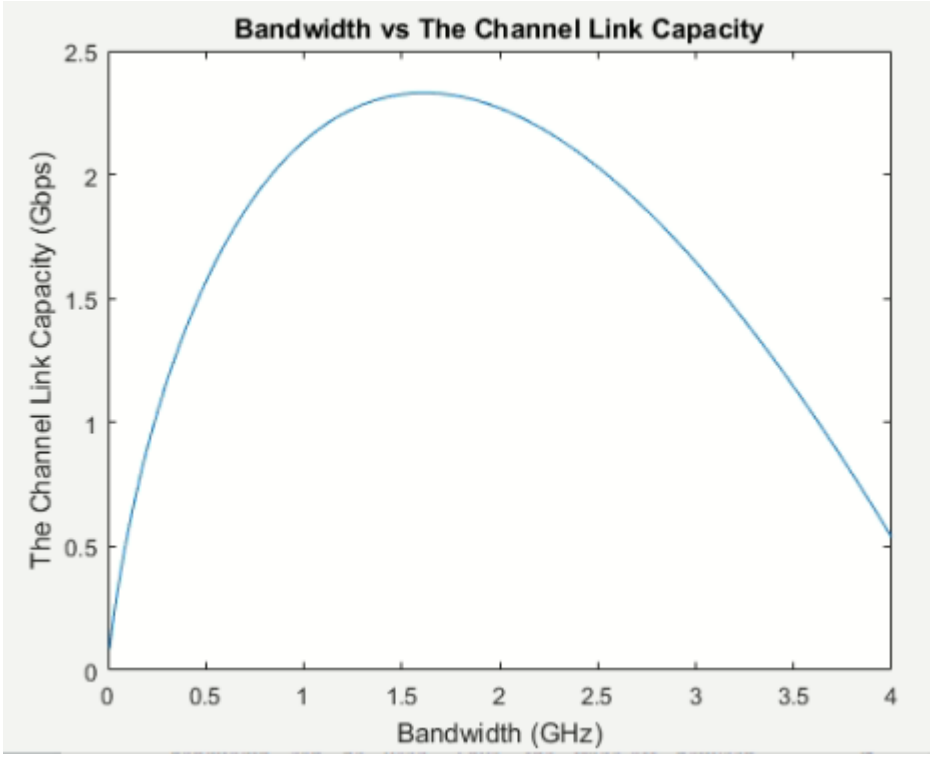


Figure 2.8 The channel link capacity vs the selected bandwidth of the channel for the MIMO system.

2.2.2 Potentials with massive MIMO

Besides increasing the data rate of the communication scheme, MIMOs are also preferred since they are increasing the number of simultaneous communication. In MIMO-based systems, with respect to omnidirectional phased arrays, multiple antennas create an opportunity to build a communication scheme separately (Ikhlef (2014); Larsson, Edfors, Tufvesson & Marzetta (2014)).

Massive MIMOs also decrease the power consumption of the overall module. In the classical array designs, which consist of a few antennas, to transmit very high output power to the environment, power amplifiers with high power consumptions are needed. Since a similar performance is achieved with the higher number of channels, the power consumption of PAs decreases from hundred watts to hundred milliwatts (Björnson, Sanguinetti, Hoydis & Debbah (2015); Larsson et al. (2014)).

Massive MIMOs reduce the latency on the air interface. In the classical array designs, the primary source of the latency is fading. In massive MIMO systems, fading is no longer exists since massive MIMOs are based on the law of large numbers. This law also hardens the channel, which means that each user has the relatively same gain, and whole bandwidth can be given to each user at the same time (Gunnarsson,

Flordelis, Van der Perre & Tufvesson (2018); Larsson et al. (2014)).

Massive MIMOs increase the robustness against intentional or unintentional jamming. Massive MIMOs achieve a more secure system because the number of antennas increases at the base station. It enables an opportunity to cancel unintentional or intentional signals that reduce the channel link capacity or broke the communication scheme (Larsson et al. (2014); Li, He, Jiang & Liu (2016)).

2.3 Phased Array Systems for 5G Communications and Existing

Literature

A significant amount of research has been demonstrated on 5G mm-Wave transceivers, especially for the 26/28 GHz bands, both by academia and industry.

(Kibaroglu, Sayginer, Phelps & Rebeiz (2018)) achieves 18 Gbps with 16-QAM from 5 meters and 9 Gbps with 64-QAM from 300 meters. In this work, 4TRX combined to form a half-duplex circuitry. Each receiver channel has 26 dB gain while consuming 150 mW and each transmitter channel has 20 dB gain while consuming 220 mW. The phase resolution of that work is selected as 6-bit. (Pang, Wu, Wang, Dome, Kato, Huang, Tharayil Narayanan, Liu, Liu, Nakamura, Fujimura, Kawabuchi, Kubozoe, Miura, Matsumoto, Li, Oshima, Motoi, Hori, Kunihiro, Kaneko, Shirane & Okada (2019)) consists of 4 TRX units. It achieves 15 Gb/s with 64-QAM while it has a 12 dB receiver gain and 10 dB transmitter gain. The power consumptions of (Pang et al. (2019)) are 148 mW in receiver mode and 299 mW in transmitter mode. From the IBM, (Sadhu, Tousi, Hallin, Sahl, Reynolds, Renstrom, Sjogren, Haapalahti, Mazor, Bokinge, Weibull, Bengtsson, Carlinger, Westesson, Thillberg, Rexberg, Yeck, Gu, Ferriss, Liu, Friedman & Valdes-Garcia (2017)) achieves 20.64 Gbps with 128 TRX channels. It uses a 256 QAM modulation. 5-bit phase resolution is achieved in that work. While each receiver channel consumes 103.1 mW, each transmitter channel consumes 143.8 mW. (Kodak & Rebeiz (2016)) achieves 4.1 Gbps with 16-QAM modulation. The receiver part of Kodak & Rebeiz (2016) achieves 16 dB gain while the transmitter part of that work achieves 16.5 dB gain. The power consumptions of (Kodak & Rebeiz (2016)) are 54 mW and 100 mW in receiver and transmitter mode, respectively. (Yamamoto, Tsutsumi, Maruyama, Fujiwara, Hagiwara, Osawa & Shimozawa (2018)) presents the functionality of their work in terms of phase and amplitude resolution. It achieves 6-bit phase resolution

and 6-bit amplitude control with 13.7 dB RX gain and 16.9 dB TX gain. Kalyoncu, Burak & Gurbuz (2020) demonstrates a receiver channel with a 130 nm Sige BiCMOS technology that achieves 6-bit phase resolution and analog gain control. Gao & Rebeiz (2020) also demonstrates a TRX with 45 nm CMOS SOI which achieves a 3- 3.6 dB NF in the receiver chain.

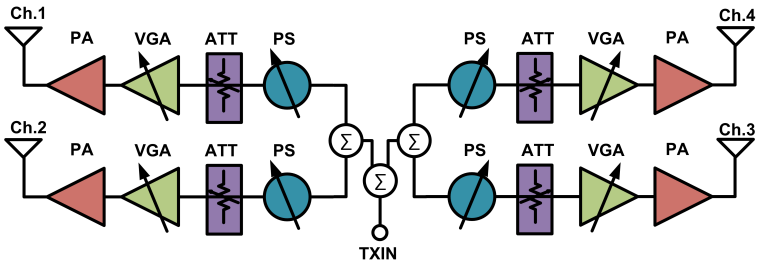


Figure 3.1 The block diagram of 4x1 TX MIMO

3. FOUR ELEMENT TX AND RX MODULES FOR 5G CELLULAR COMMUNICATION

In this chapter, the design procedure of each sub-block for 4x1 MIMO TX and RX channels will be explained. Four-channel TX and RX beamformers are designed in a 0.13-μm SiGe BiCMOS technology. LNA, VGA, PS, ATT, SPI, and Wilkinson combiner employ in four-channel RX beamformer. PA, VGA, PS, ATT, SPI, and Wilkinson combiner use in four-channel TX beamformer. Both TX and RX modules were designed according to the 5G band in 24-28 GHz.

3.1 Design Procedure of Building Blocks

The block diagram of four-channel TX is shown in Fig. 3.1. 4x1 TX MIMO consists of 6-b PS, 1-b ATT, 3-b VGA, PA, Wilkinson combiner, and an SPI. The designed PS adjusts the signal's phase, and VGA and ATT adjust the signal's amplitude. The designed PA transmits the signal to the environment with high power. These four blocks create a single channel. Each IC consists of four channels, and three Wilkinson combiner combines these channels. An SPI is used for determining the control voltages of PS, VGA, and ATT.

The order of each sub-block is determined concerning the linearity performance of

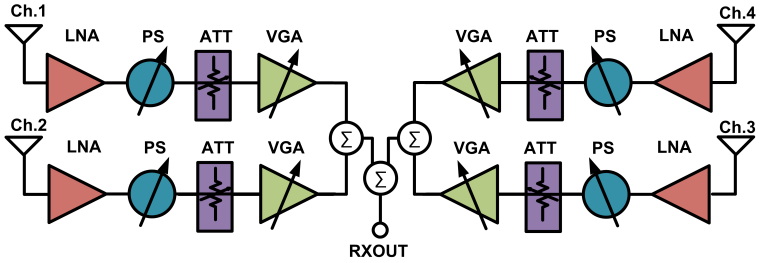


Figure 3.2 The block diagram of 4x1 RX MIMO

the transmitter. Since PAs provide the highest output power, the last sub-block for TX modules is PAs. The ATT is placed before the VGA to ensure that the input and the output return losses of VGA and PS will not deteriorate their amplitude and phase performance. The order between VGA and PS is prioritized concerning the linearity performance of each sub-block. Since VGA has a higher linearity performance than the PS, it is placed before the power amplifier to increase the linearity performance of the TX module.

The block diagram of the designed RX is shown in Fig. 3.2. 4x1 RX MIMO consists of 6-b PS, 1-b ATT, 3-b VGA, LNA, Wilkinson combiner, and an SPI. All sub-blocks in RX except the LNA work the same way as explained in the TX part. The designed LNA receives the signal from the environment and amplifies it without adding too much noise.

The order of each sub-block is determined with respect to the noise figure and linearity performance of the receiver. Since LNAs provide the lowest noise figure, the first sub-block for RX modules is LNAs. The order between ATT, VGA, and PS is prioritized for the linearity performance of each sub-block. Although the designed PS has the highest NF performance among others, to achieve the linearity performance (IP_{1dB}) > -25 dBm, the PS is placed after the LNA. LNA suppresses the NF of the PS. The ATT is placed before the VGA to ensure that the input and the output return losses of VGA and PS will not deteriorate their amplitude and phase performance.

3.1.1 Variable Gain Amplifier

In order to adjust the amplitude level of the signal, phased-array beamformer channels use passive and active circuits: attenuators and variable gain amplifiers, respectively. The main objective of these two blocks is to adjust the signal level without

changing the signal phase. Although ideally, their phase error is zero, in reality, their phase errors exist. In this beamformer, we realize both VGA and attenuator. We used both sub-blocks because, at the low gain setting levels, the phase error of the VGAs increases a lot. In the literature, many works have focused on variable-gain amplifiers for 5G beamforming applications (Cho, Song, Fleetwood & Cressler (2018); Lee, Park & Hong (2019); Sadhu, Bulzacchelli & Valdes-Garcia (2016)).

In this work, we use a single-stage cascode amplifier configuration with current-steering BJT as the VGA. The schematic of the VGA is shown in Fig. 3.3. There is a trade-off between gain, linearity, and power consumption. To optimize this trade-off, the CE and CB transistors are sized eight times the unit device. The unit size of the current-steering device is selected as 32 to make sure that we have linear-in-dB amplitude control. The current-steering transistor is connected as diode-connected. The voltage level of the diode-connected transistor is determined with a current steering DAC as shown in Fig. 3.3. In DAC, we create the reference voltage for the current generator transistor, which is called M_{0-7}. The width of each transistor is given in Fig. 3.3. There is a trade-off between the transistor number and the current generation error. Since we are using less amplitude resolution, we can decrease the number of transistors and increase each transistor's width to ensure that we are supplying the same current level. However, that way leads to a high error level in terms of current. Eventually, it decreases the amplitude performance of the VGA.

Since we have eight control voltages for the DAC, the multiplexer with 3-bit control is employed to set the corresponding amplitude shift to the corresponding current values. The block diagram of the multiplexer is shown in Fig. 3.3.

We obtain 7-dB attenuation with the VGA design. The amplitude step of the VGA is selected as 1-dB.

3.1.2 Attenuator

In the literature, there are two dominant different passive networks to design attenuators: T-type attenuator and Π-type attenuator (Burak, Çalışkan, Yazici & Gurbuz (2021)). The attenuation capability of T-type networks is less than Π-type networks because they have one path to the ground. On the other hand, the phase error of T-type networks is less than Π-type networks. Since we achieved a 7-dB attenuation level with the VGA, we need an 8-dB attenuation network to achieve a 15-dB attenuation level for the module. Therefore we choose a Π-type attenuation

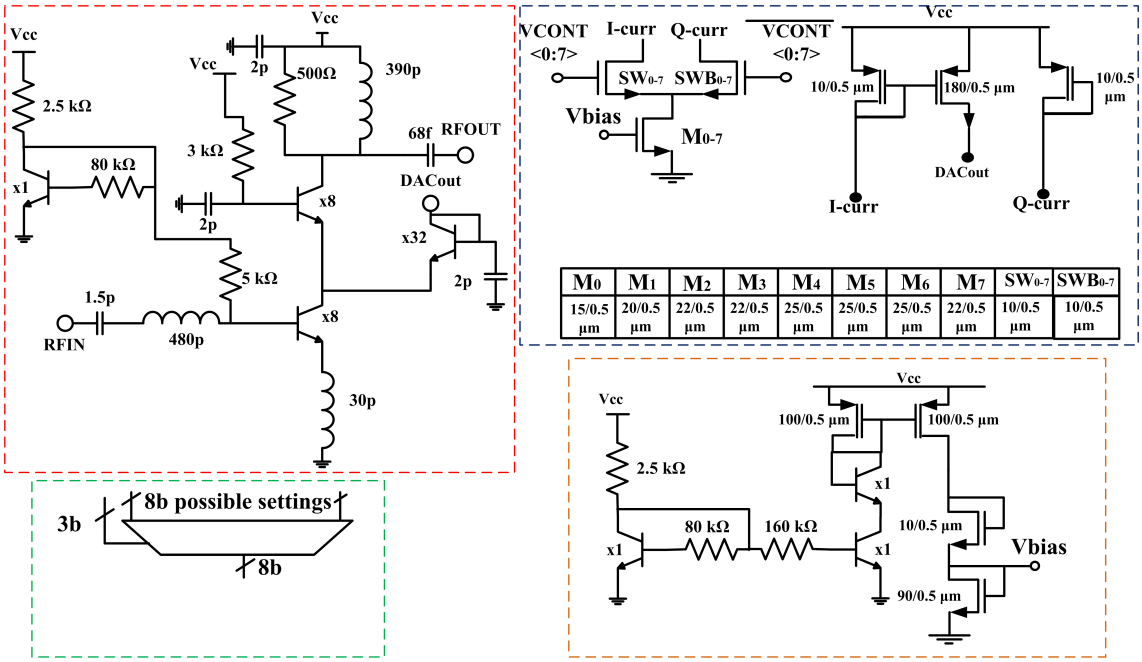


Figure 3.3 Top Left: The schematic of VGA, Bottom Left: The diagram of MUX, Top-right: The schematic of current steering DAC, Bottom-left: The schematic of the circuitry for the reference voltage.

network.

The schematic of the Π-type attenuator network is shown in Fig. 3.4. The width and length of the series transistor are selected as 40 μm/9 μm. The width and length of the shunt transistor are selected as 20 μm/0.13 μm. The shunt resistance value is selected as 145-ohm. In order to decrease the phase error of the attenuator, the L-R-L network is realized as explained in (Davulcu, Burak & Gurbuz (2020)). The value of inductance and resistance for the L-R-L network is selected as 140p and 85-ohm, respectively. The simulation results depict that 8-dB attenuation is achieved with 0.3-degree phase error.

3.1.3 Phase Shifter

The block diagram of the designed PS is shown in Fig. 3.5. To create a differential signal, a balun is employed. There are two ways to design a Balun: Active and Passive. Since active Baluns have lower linearity performance, higher power consumption than the passive Baluns, transformer-based passive baluns are employed. In the literature, transformer baluns are widely utilized and well-explained (Long (2000)). While a single turn top-metal-2 trace realized the 225 pH primary coil, a

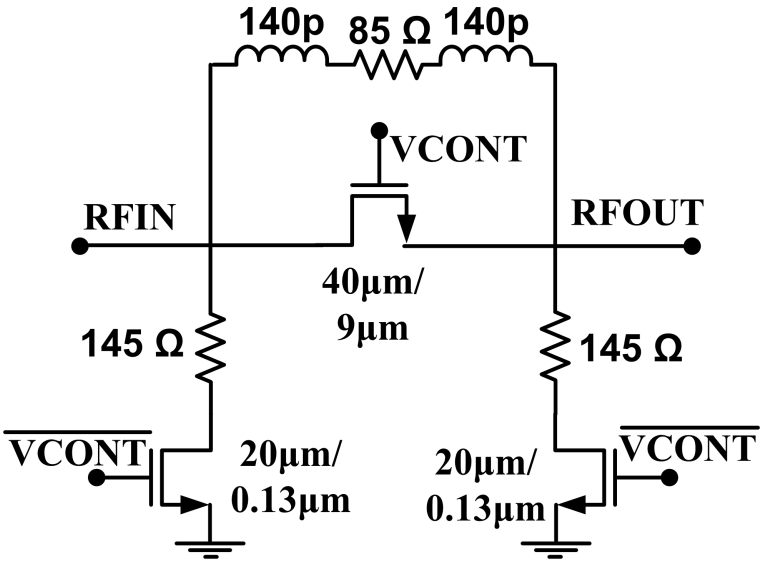


Figure 3.4 The schematic of ATT

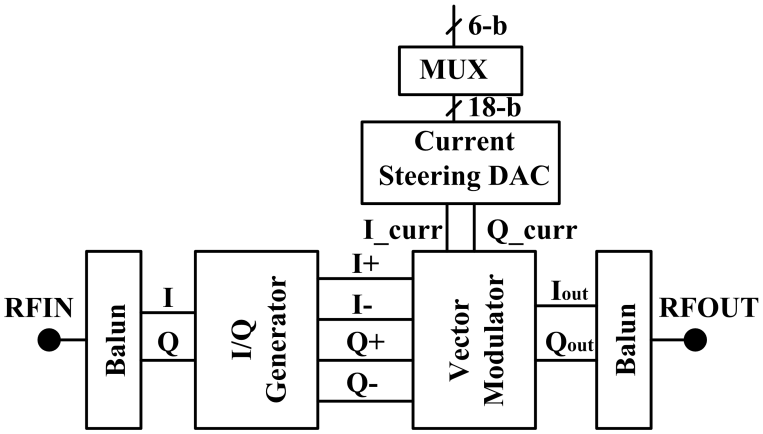
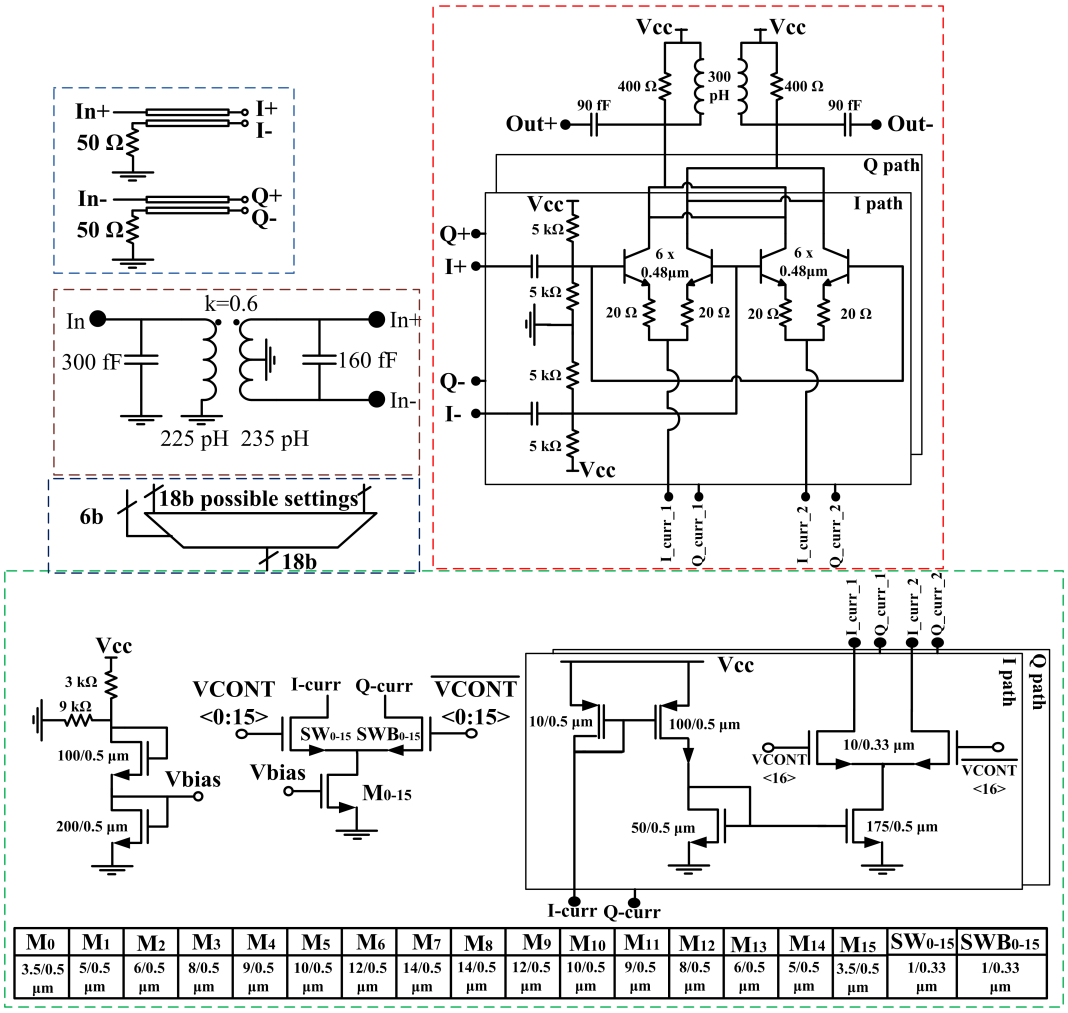


Figure 3.5 The block diagram of PS

single-turn top-metal-1 trace realized the 235 pH secondary coil. 300 fF and 160 fF capacitances were realized to perform matching. The overall balun has a $<$ 1.8 dB simulation loss in the 24-28 GHz band.

An I/Q generator follows the balun. In the literature, there are different techniques to create in-phase and quadrature signals (Behbahani, Kishigami, Leete & Abidi (2001); Frye, Kapur & Melville (2003); Kim, Kang, Koh & Rebeiz (2012a); Kodama, Ishikawa, Oshima & Tanaka (2010)). In this design, two lumped quadrature hybrid couplers are used as shown in Fig. 3.6. This method has better insertion-loss performance than the most common technique: RC polyphase filter. The drawback of this method is the area and higher phase error compared with the RC polyphase filter. Since we prioritize the insertion-loss and noise figure, we designed an IQ generator by two lumped quadrature hybrid couplers.

After obtaining IQ signals, the gilbert-cell core amplifies these four signals with

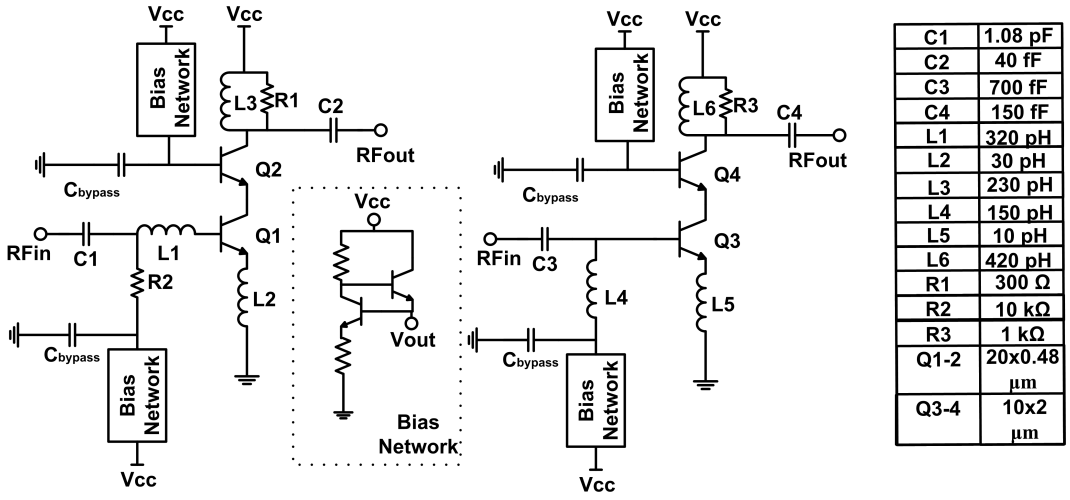


M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12	M13	M14	M15	SW0-15	SWB0-15
3.5/0.5 µm	5/0.5 µm	6/0.5 µm	8/0.5 µm	9/0.5 µm	10/0.5 µm	12/0.5 µm	14/0.5 µm	14/0.5 µm	12/0.5 µm	10/0.5 µm	9/0.5 µm	8/0.5 µm	6/0.5 µm	5/0.5 µm	3.5/0.5 µm	1/0.33 µm	1/0.33 µm

Figure 3.6 The highlighted version of each block of PS: Top-left: Hybrid coupler, Middle-left top: The schematic of Balun, Middle-left bottom: The diagram of MUX, Top-right: The schematic of Gilbert-cell core, Bottom: The schematic of current steering DAC.

different gain settings to obtain the phase shift. The schematic of the gilbert-core is shown in Fig. 3.6. The HBT sizes are 6x0.48 μm, and they are biased for a maximum tail current of 6 mA. 300 pH with 90fF is used for matching the output to 100 Ω. In order to widen the bandwidth of matching, 400 Ω resistor is employed. The balun follows the output of the gilbert-cell to combine these two signals.

The most important part of the IQ-based phase shifter is determining the tail current values of the gilbert-cell core. In this work, in order to determine the current values 16-bit current steering DAC is used. In DAC, we create the reference voltage for the current generator transistor, which is called M_{0-15}. The width of each transistor is given in Fig. 3.6. There is a trade-off between the transistor number and the current generation error. Since we are using less number phase resolution, we can decrease the number of transistors. We can increase the width of each transistor to make sure that we are supplying the same current level. However, that way leads to a



C1	1.08 pF
C2	40 fF
C3	700 fF
C4	150 fF
L1	320 pH
L2	30 pH
L3	230 pH
L4	150 pH
L5	10 pH
L6	420 pH
R1	300 Ω
R2	10 kΩ
R3	1 kΩ
Q1-2	20x0.48 µm
Q3-4	10x2 µm

Figure 3.7 The schematic of LNA and PA

high error level in terms of current. Eventually, it decreases the phase performance of the phase shifter.

Since we have 18 control voltages for the DAC, the multiplexer with 6-bit control is employed to set the corresponding phase shift to the corresponding current values. The block diagram of the multiplexer is shown in Fig. 3.6.

3.1.4 Low Noise Amplifier and Power Amplifier

The schematic of the low noise amplifier and power amplifier is shown in Fig. 3.7. The topology of both circuitry is selected as a single-stage cascode. In order to obtain simultaneous power and noise matching at 26 GHz, the transistor size for the LNA is selected as 20 x 0.48 μm. To match the input of the LNA to 50-ohm, 320 pH series inductance from the base with 1.08 pF series capacitance and the emitter, 30 pH inductance is employed. To match the output to 50-ohm, 259 pH shunt inductance parallel with 300-ohm and series with 40-fF is realized. To supply the LNA with a single supply voltage, bias networks are also used. In the literature, some works also exist for 5G receiver applications (Chen, Gao, Leenaerts, Milosevic & Baltus (2016a); Jacobsson, Aspemyr, Bao, Mercha & Carchon (2006); Li, El-Aassar, Kumar, Boenke & Rebeiz (2018); Yeh, Walker, Balboni & Floyd (2017)). The simulated stand-alone noise figure of LNA is 2.1 dB with a 13 dB gain. The power consumption of the LNA is 9 mW from the 1.8V V_{cc} supply.

The main objective of the power amplifier is to obtain high output power. Therefore, in this technology, transistor size with higher emitter width is selected. The

transistor size for the PA is selected as 10 x 2 μm. To match the input of the LNA to 50-ohm, 150 pH shunt inductance from the base with 0.7 pF series capacitance is used. There is a trade-off between the gain of the PA with the value of the emitter inductance. The higher emitter inductance also improves the input matching of PA. In this design, the gain is prioritized. The emitter inductance is selected as 10 pH to increase the gain of the amplifier. To match the output to 50-ohm, 420 pH shunt inductance parallel with 1k-ohm and series with 150-fF is realized. To supply the PA with a single supply voltage, bias networks are also used. In the literature, some works also exist for 5G transmitter applications (Mortazavi & Koh (2016); Sarkar & Floyd (2017); Shakib, Elkholy, Dunworth, Aparin & Entesari (2017); Shakib, Park, Dunworth, Aparin & Entesari (2016)). The simulated stand-alone output power of PA is 12 dBm with a 15 dB gain. The power consumption of the PA is 20 mW.

3.1.5 Serial Peripheral Interface

A digital control circuit is designed to set the amplitude and phase information of the TX and RX circuitry and realize with IHP 0.13μm SiGe BiCMOS digital standard library. This circuit is a series peripheral interface(SPI), an asynchronous serial communication standard and rising edge triggered. In this circuit, there are four different input bits, clock, load, serial data, reset, and 4x10 output bits directly connected to the bit information of the phase shifter, attenuator, and variable gain amplifier each channel. There are three different modes to load the serial data to the output: Fast-switching, Standard, Standard with saving the memory. In fast-switching mode, the load bit must be set to high, and after four clock cycles, serial data is shifted to the register. Suppose the MSB of the register is set to high. In that case, the following 3-bit information is used as the memory location and corresponding information set for all channels. The load bit must be set to high in the normal mode, and after 13 clock cycles, serial data is shifted to the register. Suppose the MSB of the register is set to low. In that case, the following 2-bit information is used as the channel location, and the following 10-bit information is set for the corresponding phase shifter, variable gain amplifier, and attenuator. In the standard mode with saving the memory, the load bit must be set to high. After 17 clock cycles, serial data is shifted to the register. Suppose the MSB of the register is set to low. In that case, the following 2-bit information is used as the channel location, and the following 10-bit information is set for the corresponding phase shifter, variable gain amplifier, and attenuator. If the 14^{th} bit of the register is set to high, the following 3-bit information is used as the memory location, and

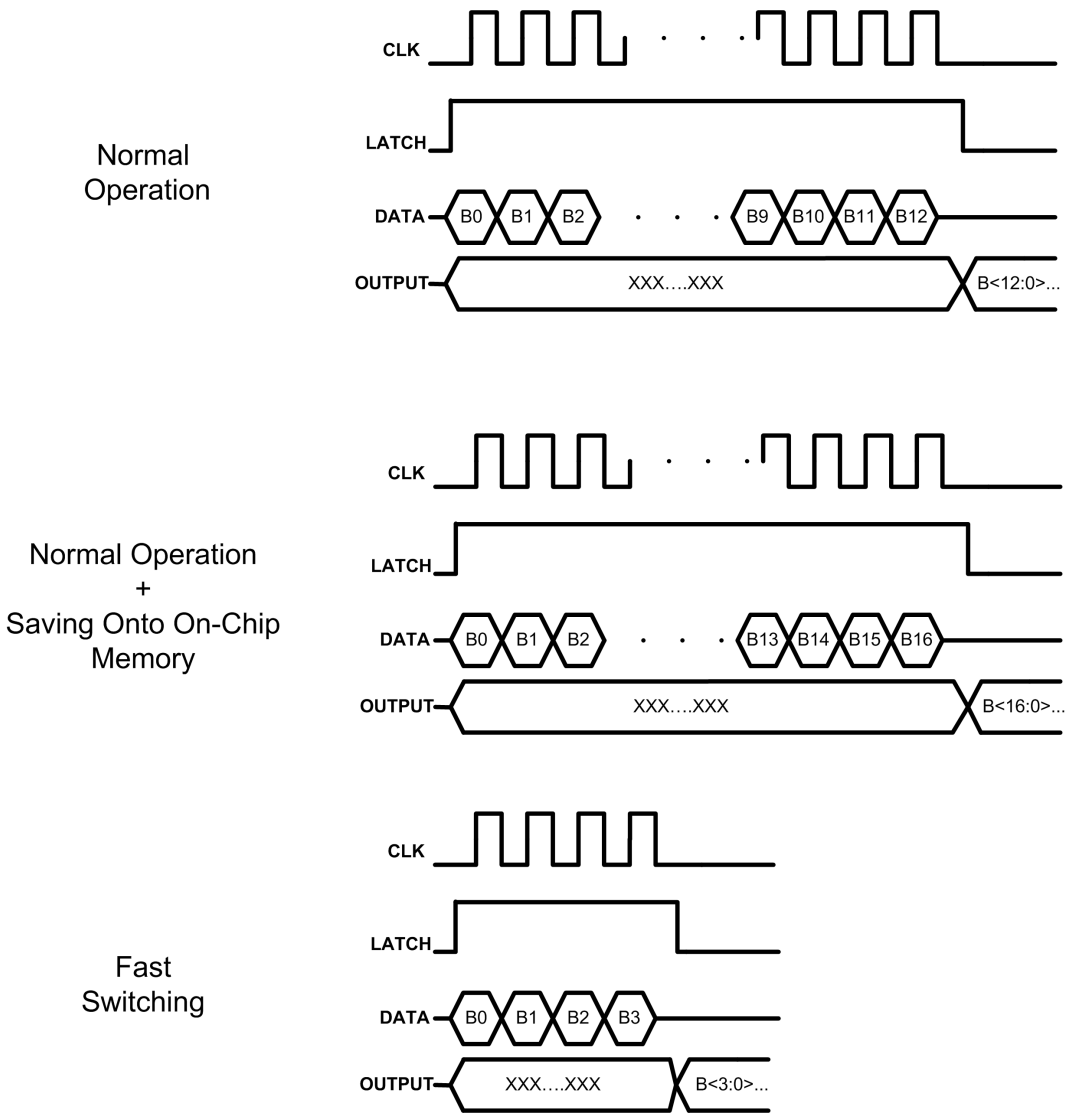


Figure 3.8 The timing diagram of each mode for the designed SPI.

the phase and amplitude settings will be written to the memory. Fig. 3.8 shows the timing diagram of each mode.

3.1.6 Wilkinson Combiner

A conventional Wilkinson combiner was designed using a Top-Metal-2-Metal-3 transmission line. The layout of the Wilkinson combiner is selected concerning the layout of other sub-blocks to reduce the overall die area. The designed Wilkinson combiner has an EM simulated 1 dB insertion loss. The role of the Wilkinson combiner is to combine the received signals from each receiver channel divide the signal into four transmitter channels to transmit to the environment.

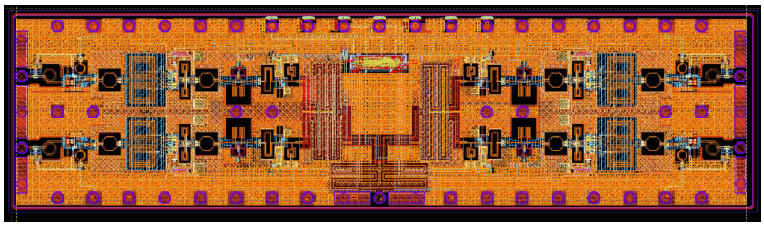


Figure 3.9 The layout of 4x1 RX MIMO

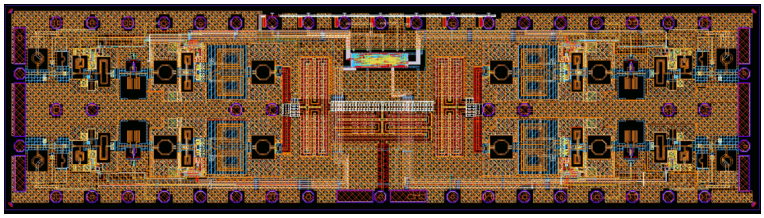


Figure 3.10 The layout of 4x1 TX MIMO

3.1.7 Overall Layouts

The overall layout of 4x1 RX MIMO and 4x1 TX MIMO are shown in Fig. 3.9 and Fig. 3.10 respectively. The size of both ICs is 5.17 mm x 1.35 mm. The pad distribution is suitable for both probe measurement and flip-chip measurement.

The simulation and measurement results of both TX and RX beamformers will be given in the following sub-sections. In the end, we will compare these ICs with the state-of-the-art modules from the literature.

3.2 Measurement Results

3.2.1 Measurement Setups

Pad-to-pad S-parameters were measured with 100-μm Infinity probes using a Keysight PNA 5224 network analyzer. The output power of the network analyzer ports was set to -30 dBm to ensure that the LNA operates in the linear region. In order to move the reference planes to the probe tips, short-open-load-thru (SOLT) calibration was performed using the impedance standard substrate ISS 101-190. The

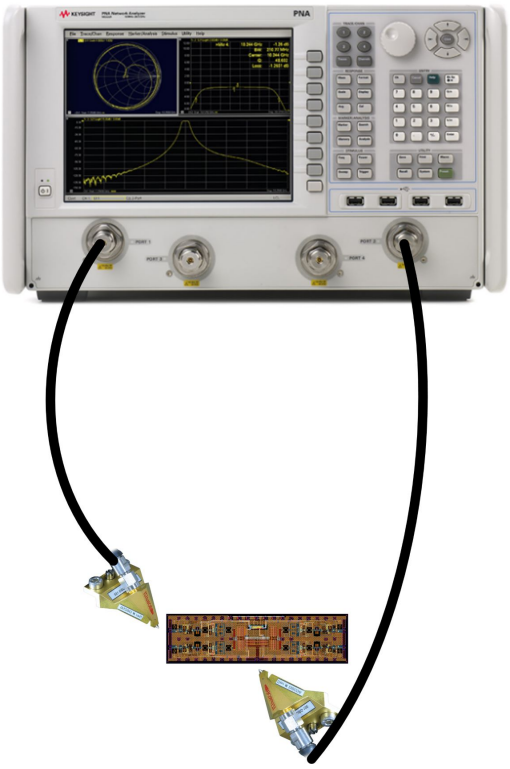


Figure 3.11 S-parameter measurement setup for MIMOs.

measurement setup for S-parameter measurement is shown in Fig. 3.11.

The linearity measurement setup for the 1-dB compression point is shown in Fig. 3.12. The 1-dB compression point of the ICs was measured with a single-tone test at 26 GHz using the Agilent E8257D analog signal generator. First, a source power calibration was performed with a Keysight E4417A power meter and Keysight 8487D power sensor over a GPIB connection. Then, the receiver power calibration was performed with a thru connection between the probes.

The two-tone measurement setup is shown in Fig. 3.13. The two-tone measurement was performed to evaluate the input third-order intercept point (IIP3). The spacing of the two tones is selected as 10 MHz. In order to measure the third harmonic product, two different signal source is employed (ZVA67 and Agilent E8257D). These two different signal sources combine with a bidirectional coupler. Then, the received power was measured with a Keysight E4448A PSA spectrum analyzer with a thru connection.

NF measurements were performed using the Y-factor method, with a Keysight E4448A PSA spectrum analyzer and 346CK01 noise source. The NF measurement setup is shown in Fig. 3.14. The cable that connects the device-under-test (DUT) to the PSA was included in the calibration phase. During the measurement phase, the measured NF includes the effects of the cable before the DUT, the probe at DUT's

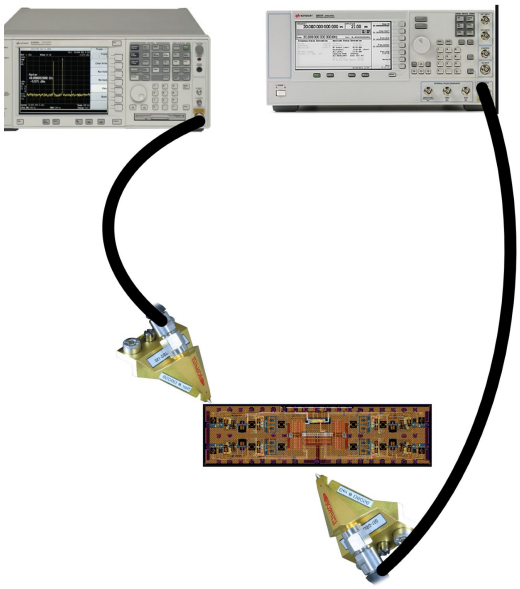


Figure 3.12 1-dB compression point measurement setup for MIMOs.

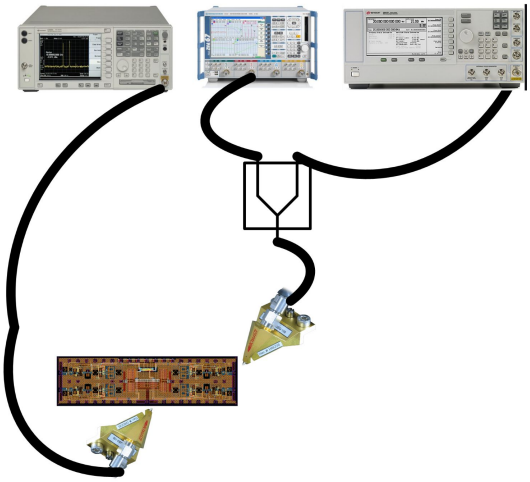


Figure 3.13 Two tone measurement setup for RX MIMO.

input, the DUT itself, the loss of the Wilkinson combiner, and the probe at DUT's output. These effects were removed from the measured NF using their measured insertion losses.

3.2.2 Four Channel RX Module

Four-channel RX is realized in a 0.13-μm SiGe BiCMOS technology. Fig. 3.15 depicts the die photo of 4 channel RX. The power consumption of the RX module is 0.2 W from the single 2.5 V source. Although the wider measurement results will

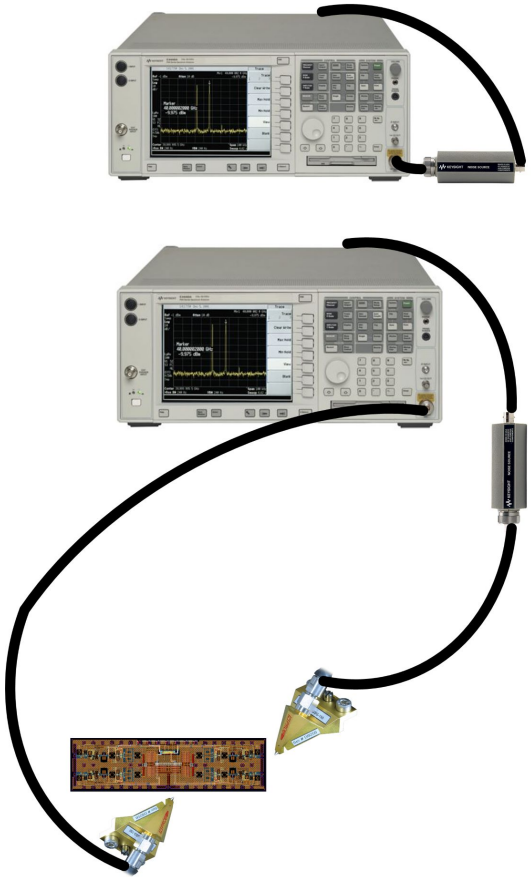


Figure 3.14 Noise figure measurement setup for RX MIMO.

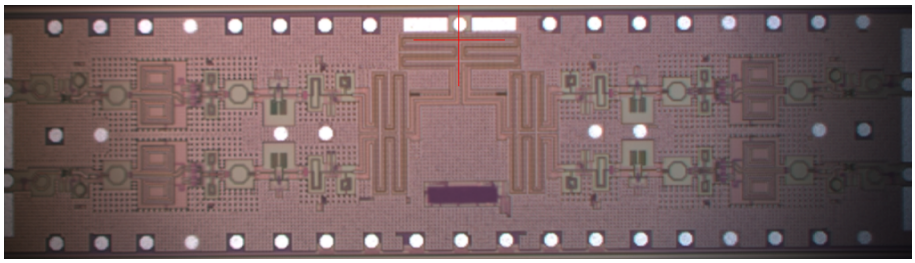


Figure 3.15 The die photograph of 4x1 RX MIMO

be given, the RX module was designed according to the 5G band in 24- 28 GHz. The designed RX module is suitable for the probe and flip-chip measurement.

The critical parameters for the receiver chain are overall and single-channel gain, the input-referred 1-dB compression, the input-referred third-order compression point, noise figure, phase, and amplitude responses. In the following subsections, the measurement result of each critical parameter will be given. Moreover, the comparison of the realized RX module with the state-of-the-art will be given at the end.

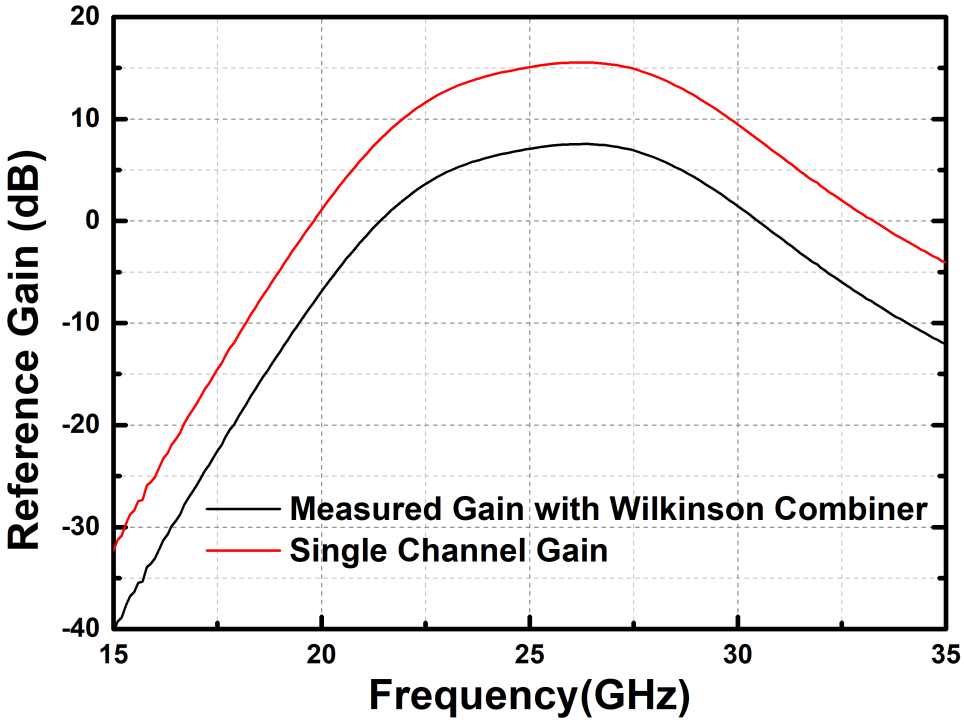


Figure 3.16 The measured gain of 4x1 RX MIMO at the reference state

3.2.2.1 Noise Figure and Gain Performance

The measured gain of the 4x1 MIMO RX module with Wilkinson combiner is shown in Fig. 3.16. Since the Wilkinson combiner has an 8-dB loss in simulations, the gain of the single-channel RX is also shown in the same graph. The measured peak gain at 26 GHz is 15.3 dB. The 3-dB bandwidth of the RX module is higher than 7.5 GHz.

The measured NF of the RX is shown in Fig. 3.17. An NF of 4.3 dB was measured at 26 GHz. Across the 3-dB bandwidth of the RX, its measured NF is less than 4.6 dB.

3.2.2.2 Linearity Performance

The measured IP1dB is -25 dBm. It can be seen in Fig. 3.18, together with IP1dB across frequencies.

As shown in Fig. 3.18, -15 dBm IIP3 value is measured at 26 GHz. Moreover, IIP3 across frequencies is also shown in Fig. 3.18.

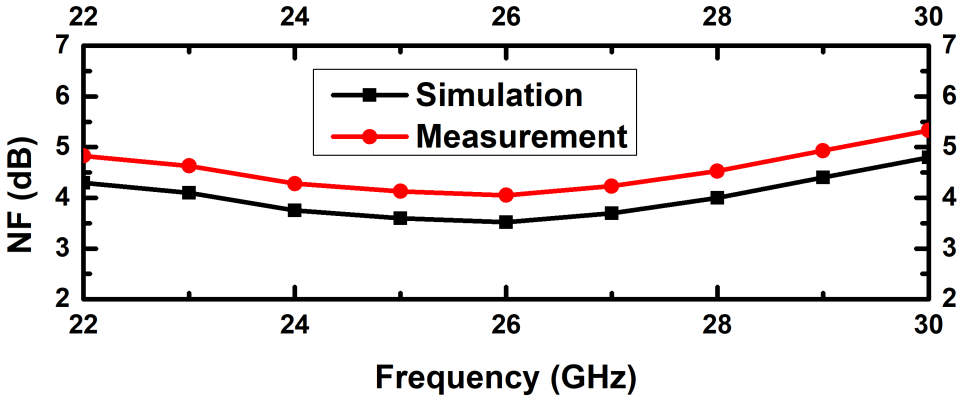


Figure 3.17 The measured noise figure of 4x1 RX MIMO at the reference state

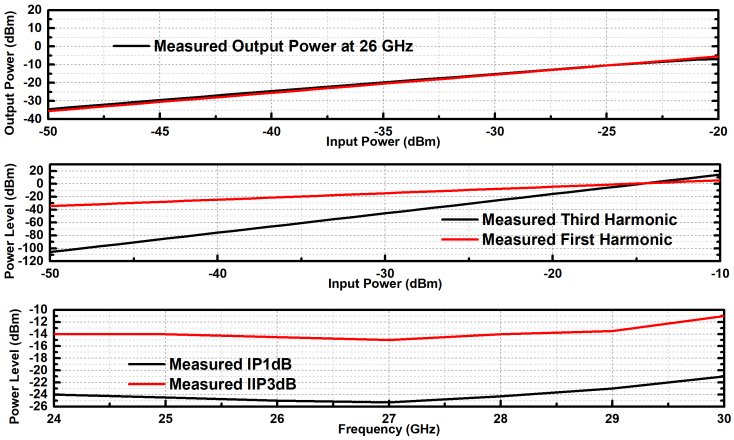


Figure 3.18 The measured IP1dB and IIP3dB of 4x1 RX MIMO at the 26 GHz and the measured IP1dB and IIP3dB of 4x1 MIMO between 24-30 GHz.

3.2.2.3 Amplitude Response

The measured input and output reflection coefficients during the amplitude response are shown in Fig. 3.19 and Fig. 3.20, respectively. As shown in this figure, the measured input and output coefficients do not vary while switching the signal's phase. The measured reflection coefficients depict S11 < -10 dB in 26–35 GHz and S22 < -10 dB in 24–40 GHz.

The measured phase responses for all the amplitude states are shown in Fig. 3.21. The phase response of the signal varies between -5 degrees to 5 degrees in the frequency of interest. Although this behavior is relatively higher than the state-of-

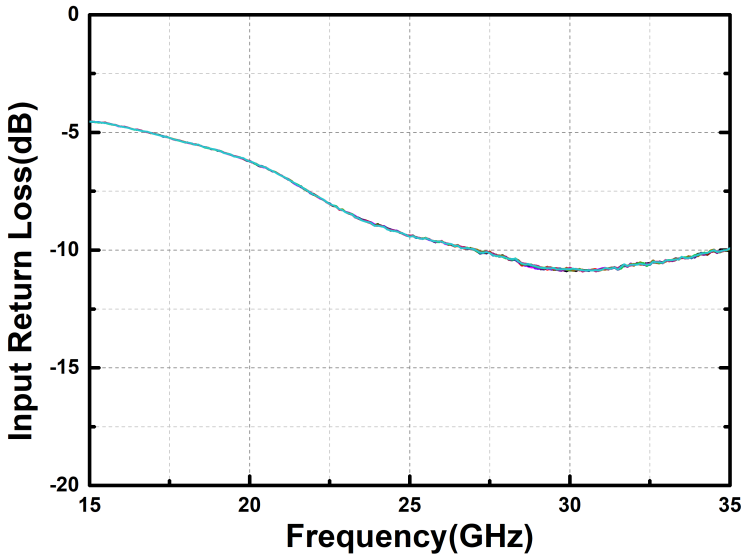


Figure 3.19 The measured input reflection coefficients while changing the amplitude of the signal for the 4x1 RX MIMO.

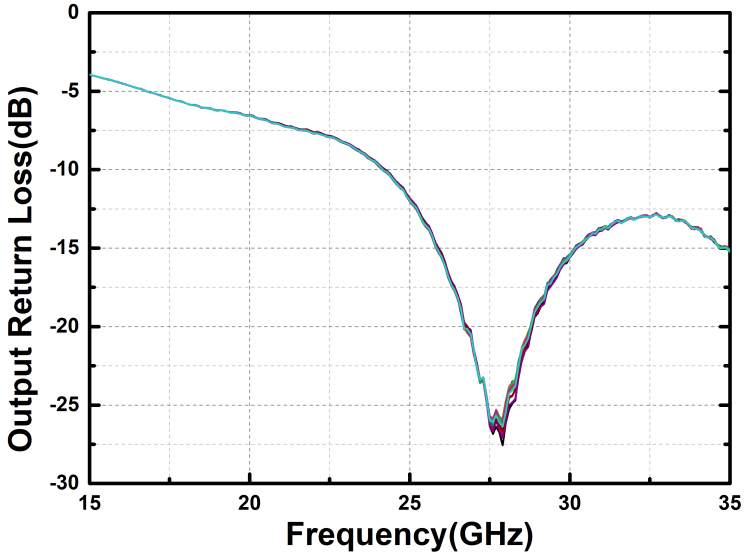


Figure 3.20 The measured output reflection coefficients while changing the amplitude of the signal for the 4x1 RX MIMO.

the-art response, the phase shifter can be used as a calibration.

Fig. 3.22 depicts the relative amplitude shifts of the TX module. Since the designed variable gain amplifier and attenuator have a 4-b amplitude configuration with a 16-dB amplitude range, each amplitude response with a 1-dB difference is plotted. All amplitude states were inspected distinctly. Moreover, amplitude responses do not overlap and do not have dead zones in the frequency of the interest. Fig. 3.23 shows the RMS phase error and RMS amplitude error of the 4-b variable gain amplifier and attenuator. The minimum RMS phase error is obtained at 20.3 GHz as 1.1 degrees. Between 24-28 GHz, RMS phase error was measured as <4.3 degrees. Moreover,

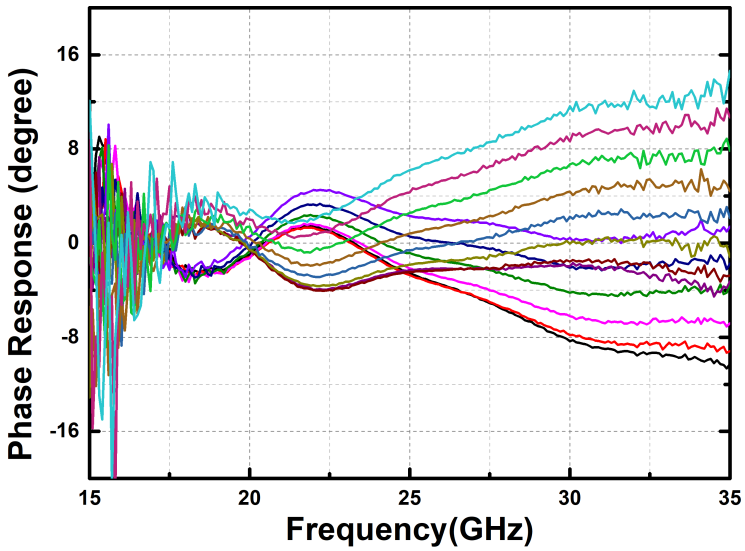


Figure 3.21 The measured phase response of 3-bit VGA and 1-bit attenuator of 4x1 RX MIMO.

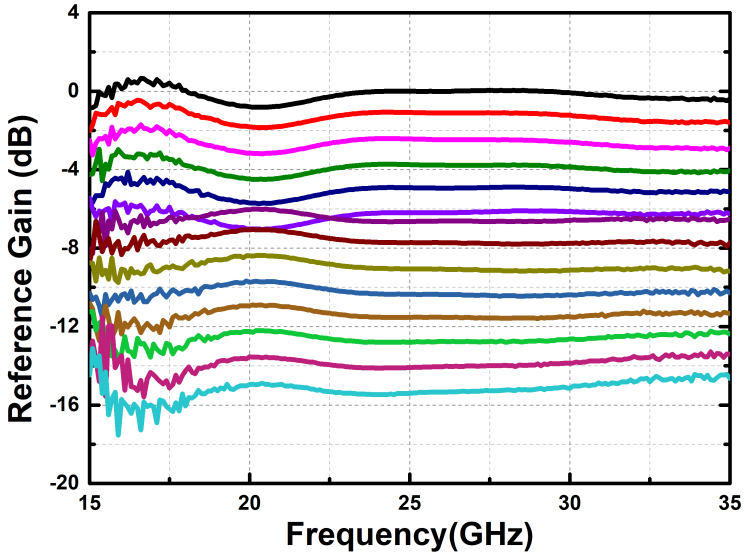


Figure 3.22 The measured 4-bit amplitude response of 4x1 RX MIMO.

RMS amplitude error is measured at less than 0.27 dB in between 24-28 GHz. The measurement results depict that the state-of-the-art amplitude response achieved for the RX module.

3.2.2.4 Phase Response

The measured input and output reflection coefficients during the phase response are shown in Fig. 3.24 and Fig. 3.25, respectively. Similar to the amplitude response,

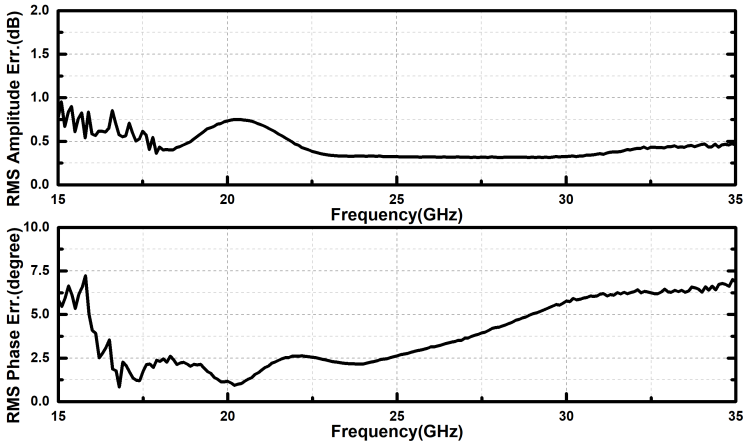


Figure 3.23 The measured RMS phase and amplitude error of the 4-bit amplitude response of 4x1 RX MIMO.

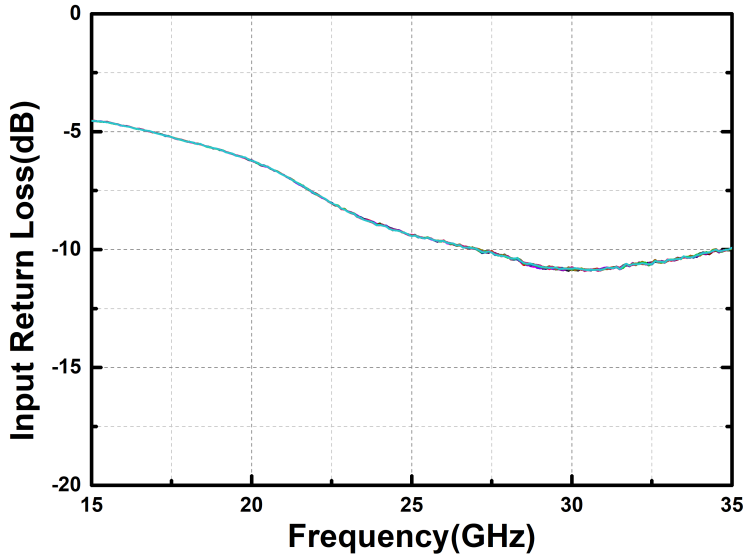


Figure 3.24 The measured input reflection coefficients while changing the phase of the signal for the 4x1 RX MIMO.

the measured input and output coefficients do not vary while switching the signal's phase. The measured reflection coefficients depict S11 < -10 dB in 26–35 GHz and S22 < -10 dB in 24–40 GHz.

The measured gains for all the phase states are shown in Fig. 3.26. The average gain peaks at 26.3 GHz with a value of 15.2 dB. The 3-dB bandwidth of the RX module with the average gain is measured between 22 and 32 GHz. The gain variation across different phase states was measured to be ±1 dB. These results verify that in terms of gain behavior, the performance of the phase shifter meets the state-of-the-art performance requirements.

Fig. 3.27 depicts the relative phase shifts of the RX module. Since the designed phase shifter has 6-b configuration, each phase response with 5.6 degree difference

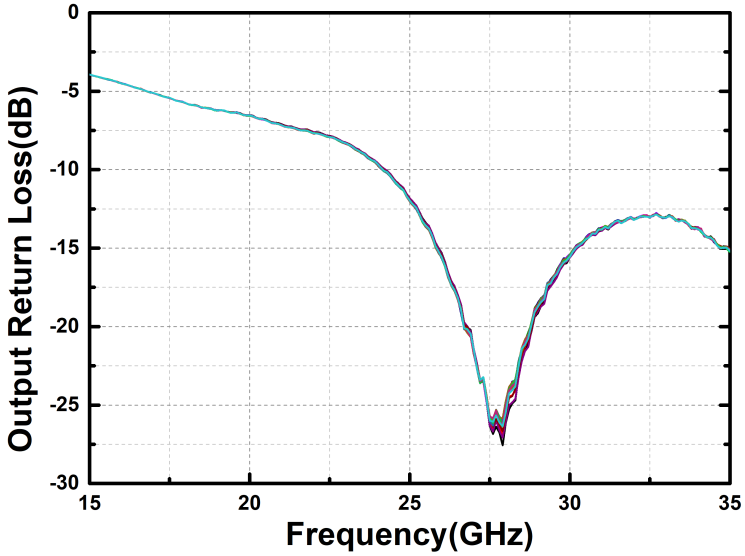


Figure 3.25 The measured output reflection coefficients while changing the phase of the signal for the 4x1 RX MIMO.

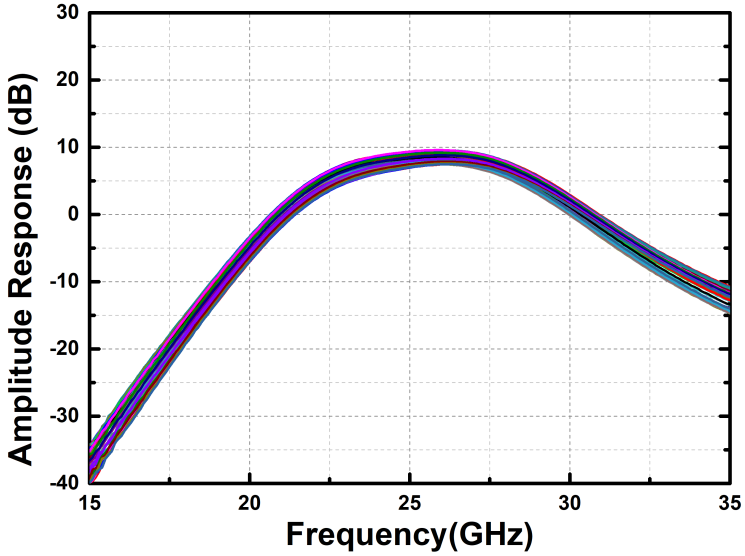


Figure 3.26 The measured amplitude response of 6-bit PS of 4x1 RX MIMO.

is plotted. All phase states were inspected, distinctly. Moreover, phase responses does not overlap and does not have dead zones in the frequency of the interest. Fig. 3.28 shows the RMS phase error and RMS amplitude error of the 6-b phase shifter. The minimum RMS phase error is obtained at 26 GHz as 1.9 degrees. Between 24-28 GHz <2.6 degrees, RMS phase error was measured. Moreover, RMS amplitude error is measured less than 0.8 dB in between 24-28 GHz. The measurement results depict that the state-of-the-art phase response achieved for the RX module.

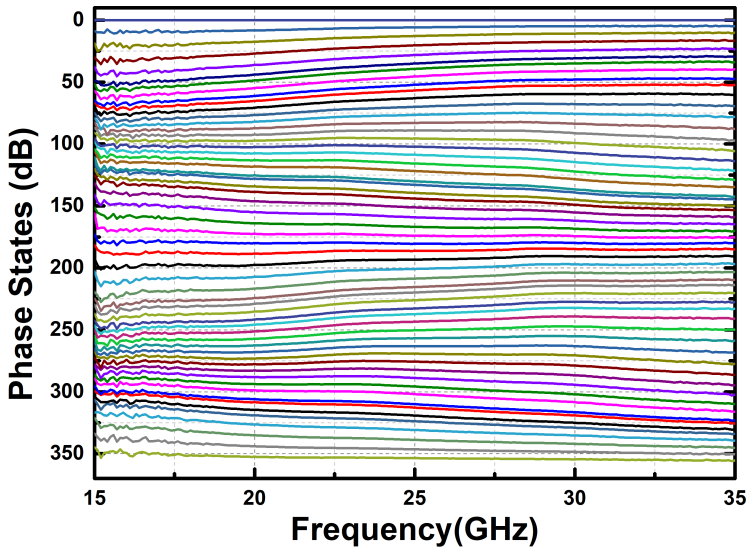


Figure 3.27 The measured 6-bit phase response of 4x1 RX MIMO.

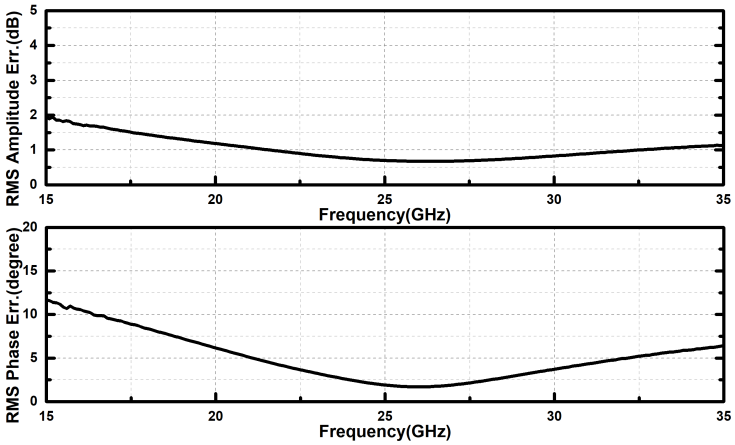


Figure 3.28 The measured RMS phase and amplitude error of the 6-bit phase response of 4x1 RX MIMO.

3.2.2.5 Comparison

Table 3.1 shows the comparison between our work with the state-of-the-art RX channels (Gao & Rebeiz (2020); Garg & Natarajan (2017); Kalyoncu et al. (2020); Kibaroglu, Sayginer & Rebeiz (2018); Kim, Park, Song, Moon, Kim, Kim, Chang & Ho (2018a); Kodak & Rebeiz (2016); Sadhu et al. (2017); Shakib, Elkholy, Dunworth, Aparin & Entesari (2019)). Thanks to the integration of DAC with the I/Q-based phase shifter, the presented work achieves the highest phase resolution and the lowest RMS amplitude error. Moreover, a 1-bit attenuator enhances the amplitude range of the designed receiver, and our design achieved the highest amplitude range. Further, our work achieves the third-best noise figure and third-best power consumption. Although our work has moderate gain performance, we believe

that such a gain performance is enough for MIMO operation. To the best of our knowledge, it is almost impossible to obtain a signal which is higher than -25 dBm from the environment. Therefore, we also believe that our work achieves the linearity requirement as well. In summary, our work meets all requirements for 5G receiver channels.

Table 3.1 Comparison of our RX channel work with the state-of-the-art RX channels.

References	**This Work**	**Kalyoncu 2020**	**Kodak 2016**	**Sadhu 2017**	**Kibaroglu 2018**	**Kim 2018**	**Garg 2017**	**Shakib 2019**	**Li 2020**
Process	**130 nm SiGe**	130 nm SiGe	45 nm SOI	130 nm SiGe	180 nm SiGe	28 nm	65 nm	40 nm	45 nm SOI
3-dB BW [GHz]	**22-29**	22-27	26-28	27-28.5	28-32	25.8-28	26-30	27-30	22-44
Phase Res.[bit]	**6**	6	5	6	6	4	5	3	5
Amp. Range[dB]	**16**	6	6	8	14	12	0	16	8
Gain [dB]	**15.5**	28.5	12.2	30	20	13.5	9.5	16.8	26.2
Amp. Res.	**4**	Analog	5	4	-	-	-	3	4
NF [dB]	**4.5**	3.3	4	6	4.6	6.2	5.5	5.5	3
IP1dB [dBm]	**-25**	-30	-8.2	-25.5	-24	-25	-22	-16	-25.4
IIP3dB[dBm]	**-15**	-	0	-12	-15	-	-	-8.5	-18
PDC [mW]	**50**	48	42	103	130	50	10	32	112
Area[mm^2]	**1.75**	1.33	1.75	2.6	1.2	0.5	0.32	0.99	1.89
RMS Amp. Err. [dB]	**0.3**	1	0.6	0.5	-		-	0.5	1.9
RMS ° Err. [deg.]	**2.6**	0.2	4	3.4	7	1.5	0.3	10	6

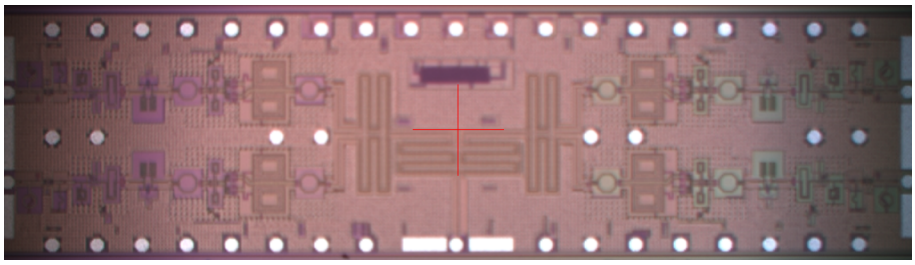


Figure 3.29 The die photograph of 4x1 TX MIMO

3.2.3 Four Channel TX Module

Four-channel TX is realized in a 0.13-μm SiGe BiCMOS technology. Fig. 3.29 depicts the die photo of 4 channel TX. The power consumption of the RX module is 0.387 W from the single 2.5 V source. Although the wider measurement results will be given, the TX module was designed according to the 5G band in 24- 28 GHz. The designed TX module is suitable for the probe and flip-chip measurement.

The critical parameters for the transmitter chain are the overall and single-channel gain, the output-referred 1-dB compression, phase, and amplitude responses. In the following subsections, the measurement result of each critical parameter will be given. Moreover, the comparison of the realized TX module with the state-of-the-art will be given at the end.

The measured gain of the 4x1 MIMO TX module with Wilkinson combiner is shown in Fig. 3.30. Since the Wilkinson combiner has an 8-dB loss in simulations, the gain of the single-channel TX is obtained from adding 8-dB to the measurement results, which is also shown in the same graph. The measured peak gain at 26 GHz is 26.2 dB. The 3-dB bandwidth of the TX module is higher than 7 GHz. The measured OP1dB of the TX module is 9.5 dBm at the center frequency. This can be seen in Fig. 3.31, together with OP1dB across frequencies.

3.2.3.1 Amplitude Response

The measured input and output reflection coefficients during the amplitude response are shown in Fig. 3.32 and Fig. 3.33, respectively. As shown in these figures, the measured input and output coefficients do not vary while switching the signal's phase. The measured reflection coefficients depicts that S11 $<$ -10 dB in 19–31 GHz and S22 $<$ -10 dB in 22–27 GHz.

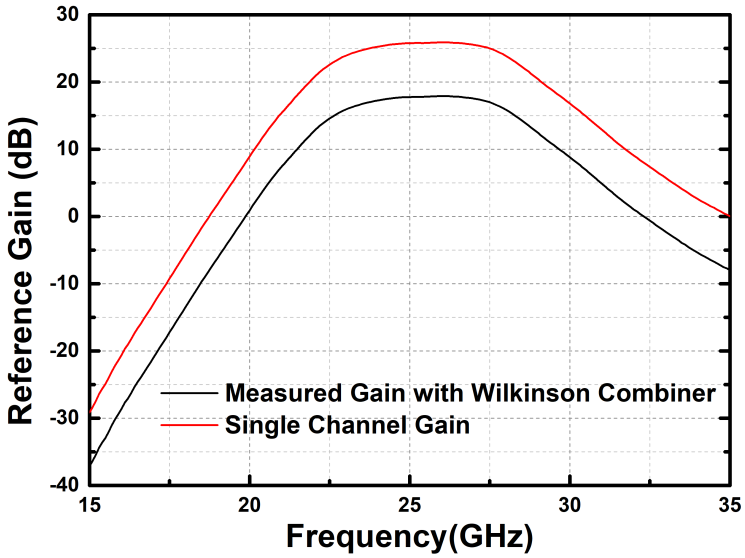


Figure 3.30 The measured gain of 4x1 TX MIMO at the reference state

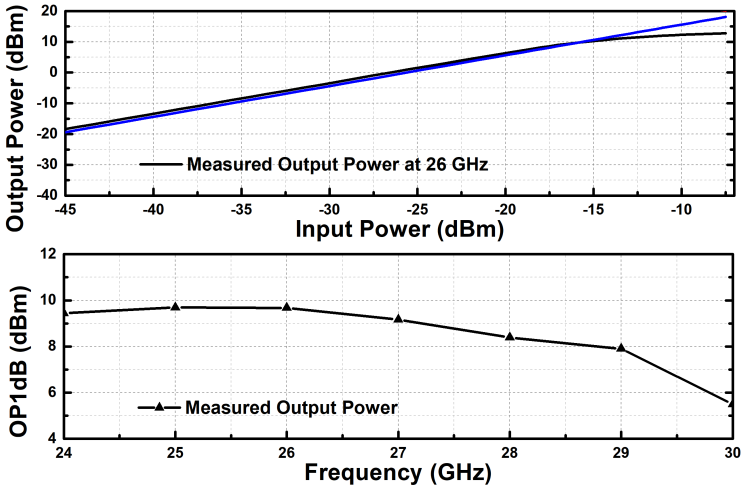


Figure 3.31 The measured linearity of 4x1 TX MIMO at the 26 GHz and the measured linearity of 4x1 MIMO between 24-30 GHz.

The measured phase responses for all the amplitude states are shown in Fig. 3.34. The phase response of the signal varies between -5 degrees to 5 degrees in the frequency of interest. Although this behavior is relatively higher than the state-of-the-art response, the phase shifter can be used as a calibration.

Fig. 3.35 depicts the relative amplitude shifts of the TX module. Since the designed variable gain amplifier and attenuator have a 4-b amplitude configuration with a 16-dB amplitude range, each amplitude response with a 1-dB difference is plotted. All amplitude states were inspected distinctly. Moreover, amplitude responses do not overlap and do not have dead zones in the frequency of the interest.

Fig. 3.36 shows the RMS phase error and RMS amplitude error of the 4-b variable

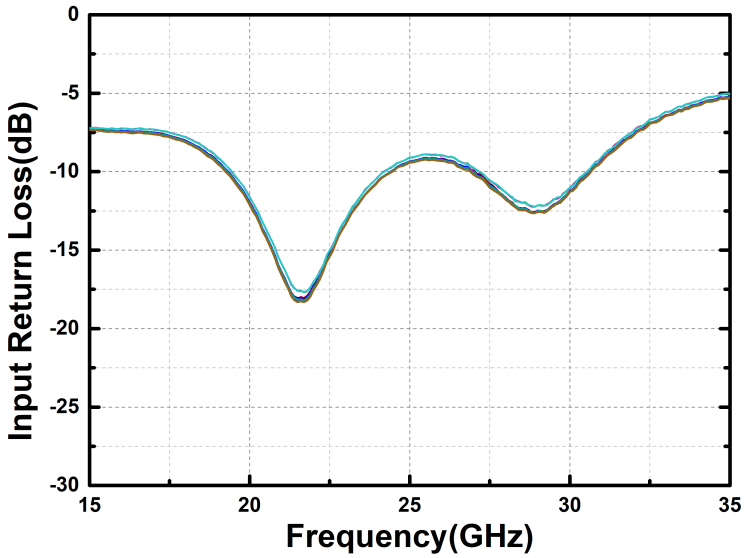


Figure 3.32 The measured input reflection coefficients while changing the amplitude of the signal for the 4x1 TX MIMO.

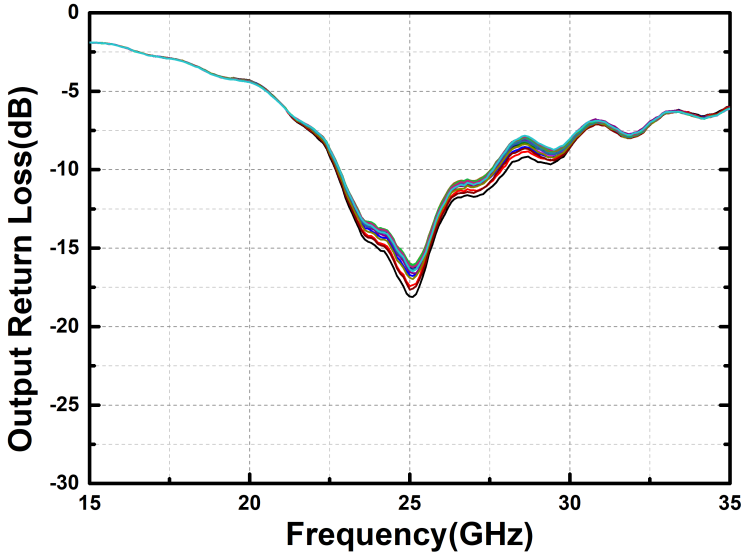


Figure 3.33 The measured output reflection coefficients while changing the amplitude of the signal for the 4x1 TX MIMO.

gain amplifier and attenuator. The minimum RMS phase error is obtained at 21 GHz as 1 degree. Between 24-28 GHz <5 degrees, RMS phase error was measured. Moreover, RMS amplitude error is measured less than 0.3 dB in between 24-28 GHz. The measurement results depict that the state-of-the-art amplitude response achieved for the TX module.

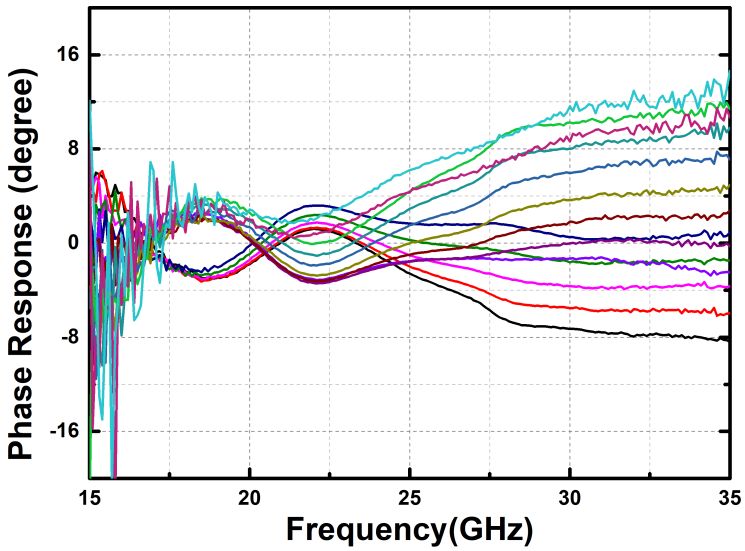


Figure 3.34 The measured phase response of 3-bit VGA and 1-bit attenuator of 4x1 TX MIMO.

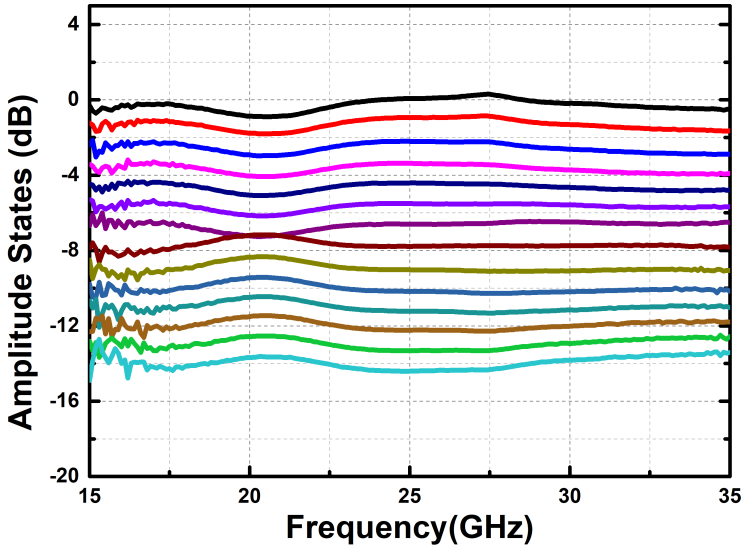


Figure 3.35 The measured 4-bit amplitude response of 4x1 TX MIMO.

3.2.3.2 Phase Response

The measured input and output reflection coefficients during the phase response are shown in Fig. 3.37 and Fig. 3.38, respectively. Similar to the amplitude response, the measured input/output coefficients do not vary while switching the signal's phase. The measured reflection coefficients depict S11 < -10 dB in 19–31 GHz and S22 < -10 dB in 22–27 GHz.

The measured gains for all the phase states are shown in Fig. 3.39. The average gain peaks at 26 GHz with a value of 26.3 dB. The 3-dB bandwidth of the TX module

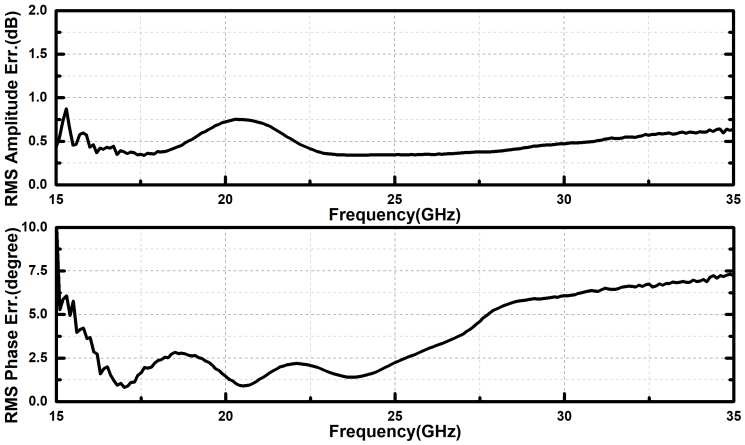


Figure 3.36 The measured RMS phase and amplitude error of the 4-bit amplitude response of 4x1 TX MIMO.

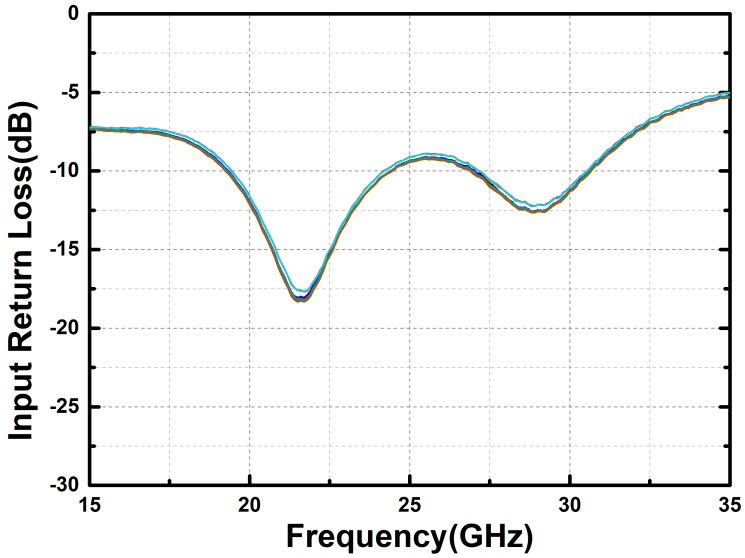


Figure 3.37 The measured input reflection coefficients while changing the phase of the signal for the 4x1 TX MIMO.

with the average gain is measured between 21 and 29 GHz. The gain variation across different phase states was measured to be ±1.2 dB. These results verify that in terms of gain behavior, the performance of the phase shifter meets the state-of-the-art performance requirements.

Fig. 3.40 depicts the relative phase shifts of the TX module. Since the designed phase shifter has a 6-b configuration, each phase response with a 5.6-degree difference is plotted. All phase states were inspected distinctly. Moreover, phase responses do not overlap and do not have dead zones in the frequency of the interest.

Fig. 3.41 shows the RMS phase error and RMS amplitude error of the 6-b phase shifter. The minimum RMS phase error is obtained at 25.5 GHz as 2 degrees. Between 24-28 GHz <3.3 degrees, RMS phase error was measured. Moreover, RMS

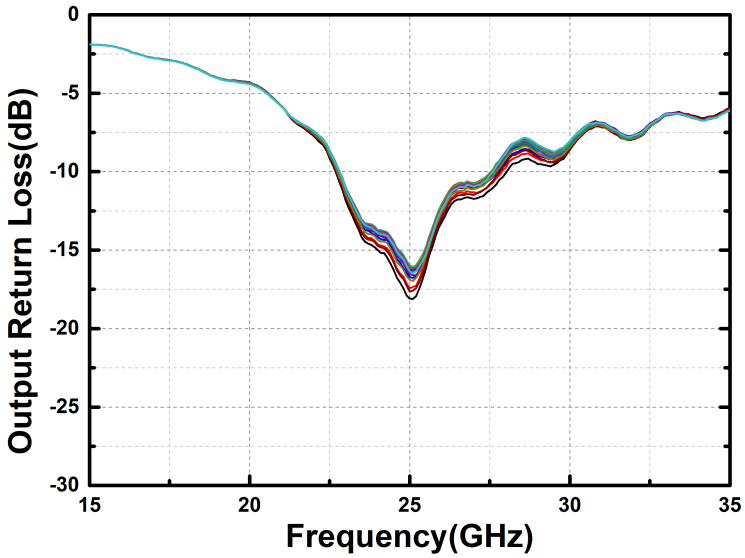


Figure 3.38 The measured output reflection coefficients while changing the phase of the signal for the 4x1 TX MIMO.

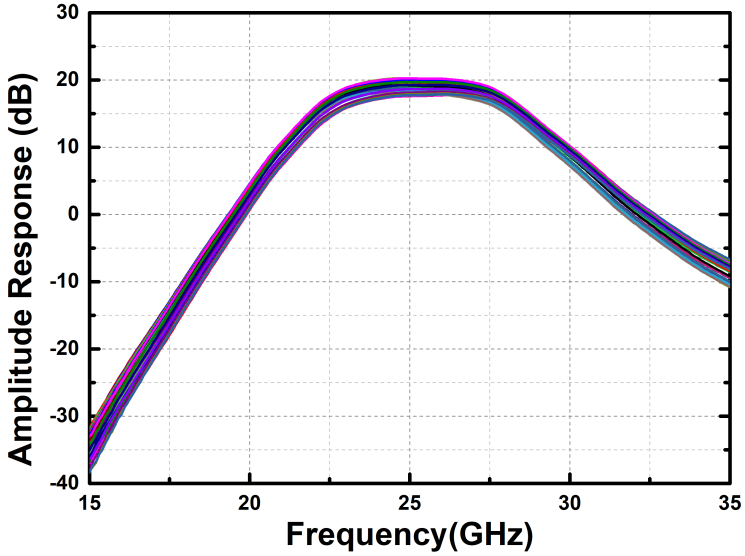


Figure 3.39 The measured amplitude response of 6-bit PS of 4x1 TX MIMO.

amplitude error is measured less than 0.8 dB in between 24-28 GHz. The measurement results depict that the state-of-the-art phase response achieved for the TX module.

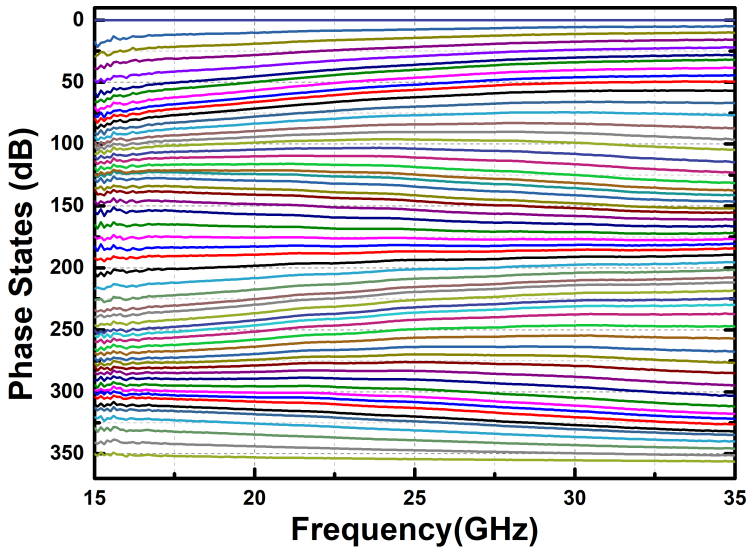


Figure 3.40 The measured 6-bit phase response of 4x1 TX MIMO.

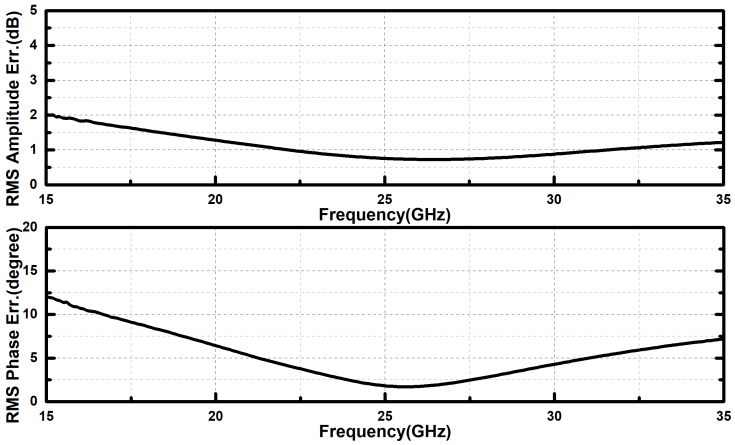


Figure 3.41 The measured RMS phase and amplitude error of the 6-bit phase response of 4x1 TX MIMO.

3.2.3.3 Comparison

Table 3.2 shows the comparison between our work with the state-of-the-art TX channels (Chen, Lin, Liu, Liao, Nien, Lu, Tsai, Huang & Wang (2018); Cho, Lee, Park, Park, Lee, Kim, Lee, Kim, Park, Park, An, Son & Yang (2019); Garg & Natarajan (2017); Kibaroglu et al. (2018); Kim et al. (2018a); Kim, Park, Song, Moon, Kim, Kim, Chang & Ho (2018b); Kodak & Rebeiz (2016)). The presented work achieves the second-highest amplitude range, the lowest RMS phase error, and the lowest RMS amplitude error. In this work, the designed phase shifter integrates the vector sum topology with the DAC, which leads to the lowest RMS phase and amplitude error. Our work achieved the second-highest amplitude range since we integrate a 1-bit attenuator with the variable gain amplifier. Further, since we

optimize the number of transistors in the PA part, our work achieves the lowest power consumption with an acceptable linearity performance. Although our work has moderate gain performance, we believe that such a gain performance is enough for MIMO operation.

Table 3.2 Comparison of our TX channel work with the state-of-the-art TX channels.

References	**This Work**	**Kim (2018)**	**Garg (2017)**	**Kim (2018)**	**Kibaroglu (2018)**	**Kodak (2018)**	**Chun (2018)**	**Cho (2019)**
Process	**130 nm SiGe BiCMOS**	130 nm SiGe BiCMOS	180 nm SiGe BiCMOS	28 nm CMOS	180 nm SiGe BiCMOS	45 nm CMOS	65 nm CMOS	28 nm CMOS
3-dB BW [GHz]	**22-29**	27-28.5	28-32	25.8-28	28-32	24-30	36-40	26.5-29.5
Phase Resolution[bit]	**6**	5	6	3	6	5	5	4
Amplitude Range[dB]	**16**	8	14	9	14	6	20	-
Gain [dB]	**25.5**	32	20	48	20	16.5	40	24
Amplitude Resolution	**4**	4	-	-	-	5	4	4
OP1dB [dBm]	**9.5**	13.5	10.5	9.5	10.5	8	12	16
PDC per. chan. [mW]	**97**	143.8	200	680	800	100	1000	102
Area per. chan.[mm^2]	**1.75**	5	1.2	7.3	1.2	3	8.5	1.9
RMS Amplitude Err. [dB]	**0.38**	0.5	-	-	0.5	0.8	2	-
RMS Phase Err. [degree]	**2.8**	3.4	7	7	5	4	5.5	-

Table 4.1 The specifications for half duplex module.

Requirements	Specification
Operating Frequency	24-28 GHz
Bit # of phase controller in VM	7-bit
Bit # of amplitude controller in VM	7-bit
RX gain	20 dB
TX gain	23 dB
RF input and output return losses	<-10 dB
IP1dB	-25 dBm
OP1dB	12 dBm
RMS Phase Error for VM	0.8 degree
RMS Amplitude Error for VM	0.1 dB
Noise Figure	2.5 dB
RX Power Consumption	30 mW
The die size	1.75 mm^2
TX Power Consumption	100 mW

4. SINGLE ELEMENT TRX MODULE FOR 5G CELLULAR COMMUNICATION

In this chapter, the design of three single-channel TX-RX modules will be explained. These modules are two different versions of single-channel TX and RX based on the asymmetric switch and single-channel TX and RX based on the single-pole-double-throw switch. The aim of these designs is the realization of the TX-RX module in a single channel with a lower area than the design presented in chapter 3. Moreover, the power consumption of these modules will also be lower than the previous design. Although these modules have less power consumption and lower area than the previous design, the functionality of these modules will be the same.

The simulation and measurement results of each sub-block employed to realize modules will be presented in this chapter. The specifications of these designs are shown in Table 4.1. To meet these requirements, we need to design an LNA, PA, vector modulator(VM), Wilkinson combiner, asymmetric switch, single-pole-double-throw switch(SPDT), and serial peripheral interface(SPI).

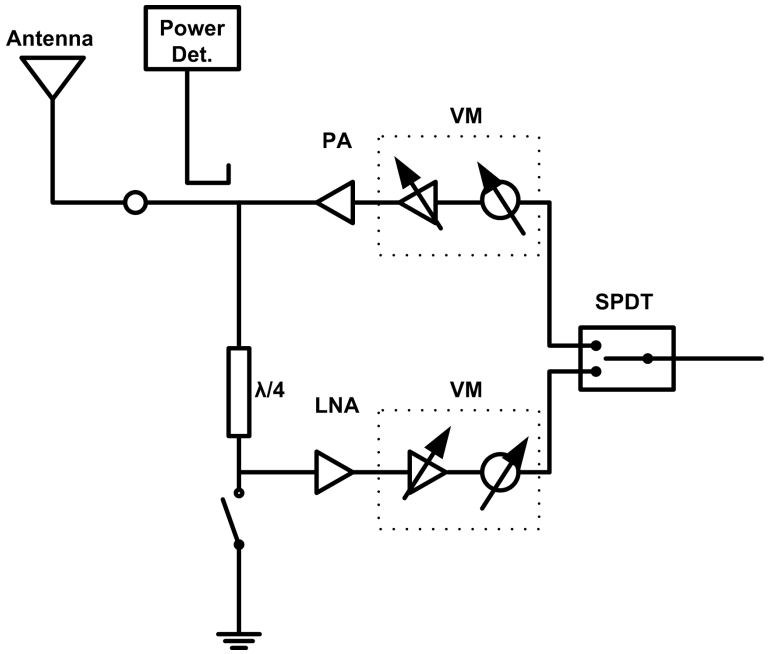


Figure 4.1 The block diagram of single channel based on asymmetric switch.

4.1 Design Procedure of Building Blocks

In this part, the design procedure of each sub-block for single-channel TX-RX modules will be explained. Single-channel TX-RX beamformers are designed in a 130-nm SiGe BiCMOS technology. ASYM, SPDT, LNA, PA, VM, SPI, and Wilkinson combiner employ single-channel TX-RX beamformers. The only difference between these two modules is that one module is based on the asymmetric switch. Therefore asymmetric switch is employed while combining TX and RX paths. The other TX-RX beamformer is based on the SPDT switch, and therefore SPDT switch is employed while combining TX and RX paths. Both TX and RX modules were designed according to the 5G band in 24-28 GHz.

The block diagram of single-channel based on the asymmetric switch and single-channel based on SPDT switch is shown in Fig. 4.1 and Fig. 4.2, respectively. In RX mode, after the switch operation, the designed LNA amplifies the signal. The designed VM adjusts the signal's phase and amplitude. Finally, the SPDT takes the signal and directs the signal as an output. In TX mode, the input signal is connected to the input of the VM. The designed VM adjusts the phase and amplitude of the signal. The designed PA transmits the signal to the environment with high power. These four blocks create a single channel. Three Wilkinson combiners will be used to combine these channels and will form a 4-channel TRX module. An SPI is used for determining the control voltages of VM.

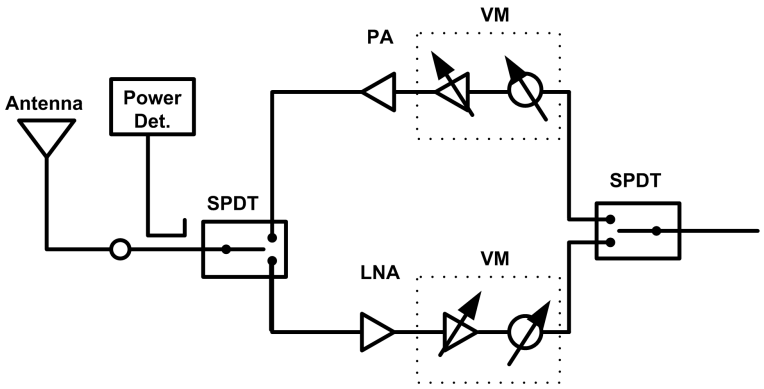


Figure 4.2 The block diagram of single channel based on SPDT switch.

The order of each sub-block is determined concerning their functionalities to meet the noise figure and linearity performance of the channel. In order to switch the mode of operation, we need to use switches as the first block as the last block. For both switches, the insertion-loss parameter is the most critical. Since LNAs provide the lowest noise figure, the first sub-block after the switches in RX mode is LNA. The main specifications for LNA are obtaining the lowest noise figure while achieving the required linearity performance, IP_{1dB} -25 dBm, as possible as the lowest power consumption and die area to minimize the cost of the overall die. After that, VM is employed to adjust the amplitude and phase of the signal. This block is prioritized for the phase and amplitude resolution performance. Since we want to achieve high phase and amplitude resolution with the same block, the overall die area and power consumption will decrease. Moreover, the noise figure, linearity performances are also noteworthy to not increase the overall noise figure enormously or decrease overall linearity. Then the final switch is used to conclude the RX channel. Since PAs provides the highest output power, the last sub-block before switches in the TX path is the PA. Although the most critical parameter is to achieve the highest output power, the efficiency of the PA is crucial for the overall module. Therefore, we try to minimize the power consumption of the PA while achieving the necessary output power level. In this section, the design methodology of each sub-block will be explained.

4.1.1 Vector Modulator

The block diagram of the designed VM is shown in Fig. 4.3. It consists of an input balun, I-Q quadrature generator, gilbert-cell core, current-steering DAC, output balun. The VM design is a similar version of the PS design in the third chapter.

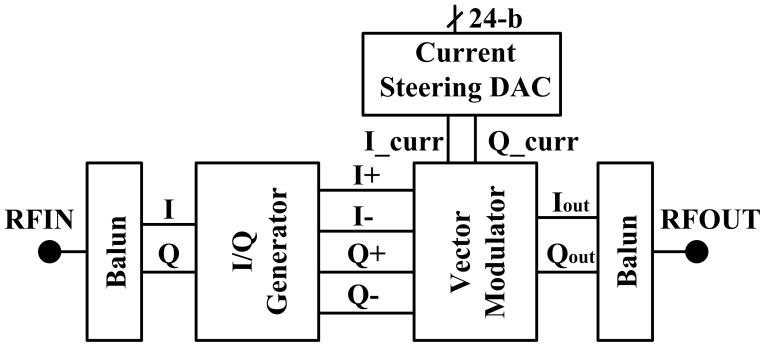


Figure 4.3 The block diagram of the designed vector modulator.

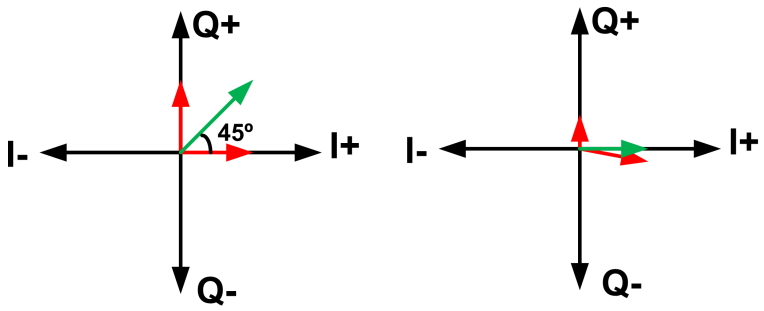
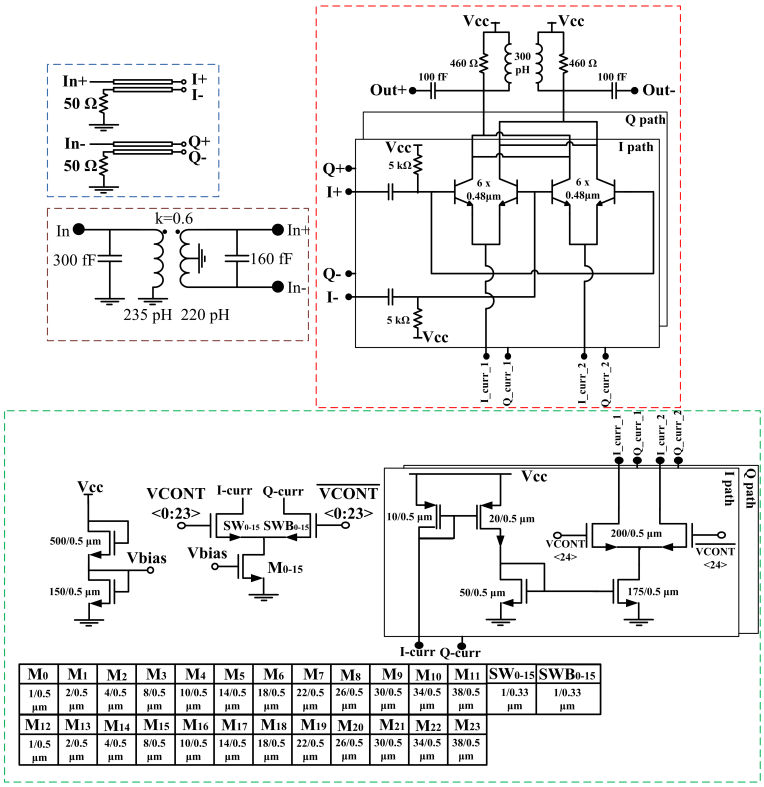


Figure 4.4 The working principle of vector modulator to obtain phase(Left) and amplitude(Right) states.

The working principle of VM is explained below. A transformer is employed to create two differential signals with a low amplitude error. These two signals with a 180-degree phase shift follow the quadrature generator. Four quadrature vectors (I+, I-, Q+, Q-) are realized in that passive circuitry. These four signals amplify with the gilbert-cell cores. The critical part for the gilbert-cell cores, the bias voltages, will determine the weight of each quadrature signal. That way, we will determine the phase and amplitude shift operation. To determine the bias voltages, we need to use current-steering DACs. After obtaining weighted signals, an output balun will sum these two signals and finalize the VM's operation.

Fig. 4.4 is shown to illustrate the phase and amplitude shift. For example, to obtain the desired 45-degree, the amplitude levels of I+ and Q+ must be the same. Moreover, to obtain the phase shift without an amplitude error, the amplitude of added vector must be the same with respect to the signal at the reference state. To obtain the desired amplitude setting with respect to the reference state, the amplitude level of the quadrature level will be adjusted. When the amplitude level of the quadrature vector is decreased, there will be a phase error. To handle that phase error, another quadrature vector will be used.



M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	SW0-15	SWB0-15
1/0.5 μm	2/0.5 μm	4/0.5 μm	8/0.5 μm	10/0.5 μm	14/0.5 μm	18/0.5 μm	22/0.5 μm	26/0.5 μm	30/0.5 μm	34/0.5 μm	38/0.5 μm	1/0.33 μm	1/0.33 μm

M12	M13	M14	M15	M16	M17	M18	M19	M20	M21	M22	M23
1/0.5 μm	2/0.5 μm	4/0.5 μm	8/0.5 μm	10/0.5 μm	14/0.5 μm	18/0.5 μm	22/0.5 μm	26/0.5 μm	30/0.5 μm	34/0.5 μm	38/0.5 μm

Figure 4.5 The highlighted version of each block of VM: Top-left: Hybrid coupler, Middle-left top: The schematic of Balun, Top-right: The schematic of Gilbert-cell core, Bottom: The schematic of current steering DAC.

4.1.1.1 Baluns

In order to create a two differential signal, passive and active baluns can be used. Active baluns have minor phase errors and provide gain, but passive baluns are preferred due to their power consumption. Ideally, passive baluns perform an equal power split and produce two signals that are 180-degree out of phase. In other words, single-ended (unbalanced) signal transforms into the differential (balanced) signal.

For a balun, the critical performance parameters are its amplitude balance, phase balance, insertion loss, and return loss. There is no amplitude difference in the ideal case, insertion loss, and perfectly matched 50-ohm. The phase difference between these two signals is 180-degree, ideally. Therefore, in reality, we try to design a balun with the lowest possible insertion-loss amplitude difference. Moreover, we try to design a balun with as possible as close to the 180-degree phase shift. The amplitude and phase balance performance of a balun can be represented by the common-mode rejection ratio (CMRR) of the balun, which is defined as in (4.1). A high CMRR translates to low amplitude and phase imbalance and is desirable for

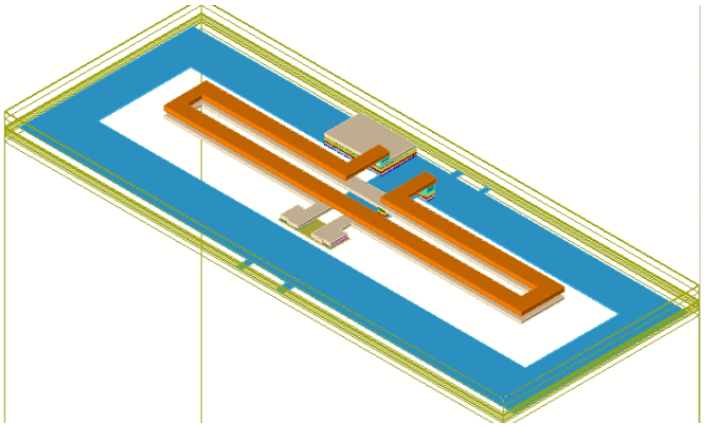


Figure 4.6 The layout of the designed balun.

common-mode noise reduction (Eisenstadt, Stengel & Thompson (2006)).

$$CMRR(dB) = 20log10(\frac{S_{21} - S_{31}}{S_{21} + S_{31}}) \tag{4.1}$$

In the literature, there are three major passive transformer balun topologies: Marchand balun, LC balun, and broadside coupled transformer balun (Long (2000)). Since Marchand balun is based on the wavelength and we need high LC-based baluns, they will occupy a larger area at the frequency of interest than broadside coupled transformer balun. It is realized with two inductor coils. The schematic of the designed balun is shown in Fig. 4.5. The primary coil is realized with top-metal-2, and it utilizes 235 pH. The secondary coil is realized with top-metal-1, and it utilizes 220 pH. The layout of the input and output balun is shown in Fig. 4.6. The reason we have that dimension is that we want to decrease the overall die area. We are expecting the y-direction of other blocks will be the same as the designed balun. That is why we choose the y-size of transformer balun as high as possible. The simulated amplitude imbalance, phase imbalance, and IL performance of the balun are shown in Fig. 4.7 and Fig. 4.8, respectively and the CMRR is shown in Fig. 4.9. The maximum amplitude imbalance is around 0.5 dB at the desired frequency. The maximum phase imbalance is around 0.2 degrees; the maximum IL is around 1.8 dB. The minimum simulated CMRR is 26 dB.

4.1.1.2 I/Q Geneator

An I/Q generator follows the balun. In the literature, there are different techniques to create in-phase and quadrature signals (Behbahani et al. (2001); Frye et al. (2003);

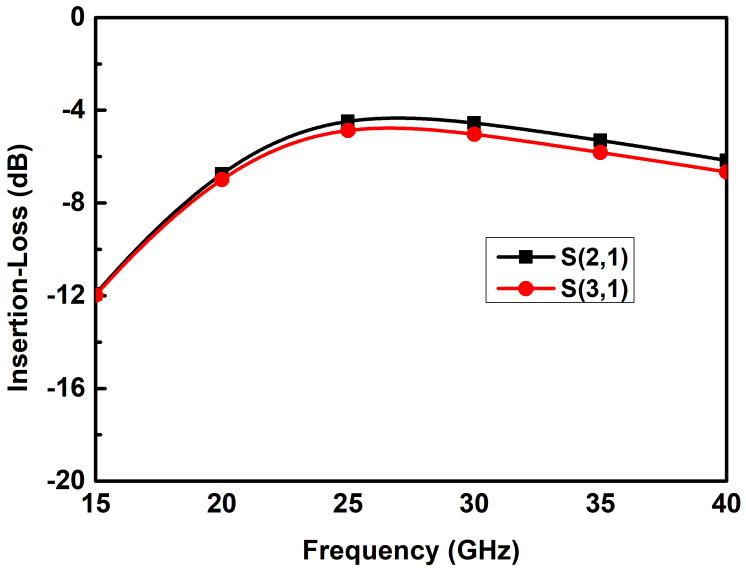


Figure 4.7 The amplitude imbalance of the designed balun.

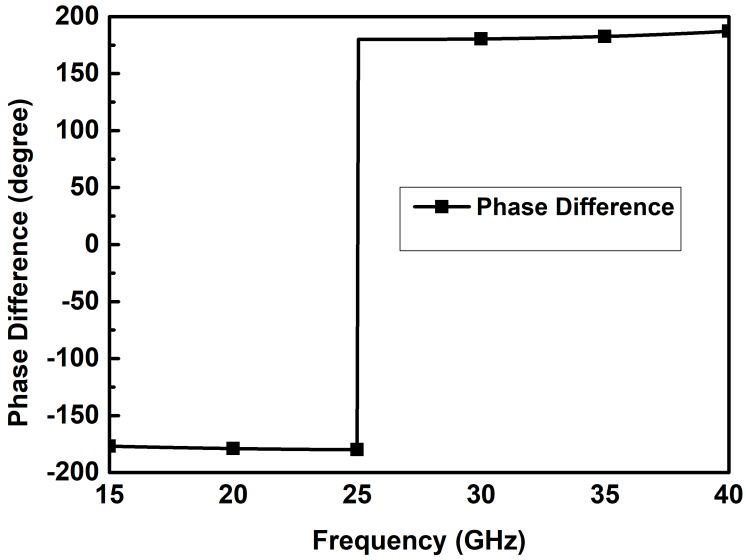


Figure 4.8 The phase imbalance of the designed balun.

Kim, Kang, Koh & Rebeiz (2012b); Kodama et al. (2010)). In this design, two lumped quadrature hybrid couplers are used as shown in Fig. 4.5. The layout of the quadrature hybrid coupler with the designed input balun is shown in Fig. 4.10. This method has better insertion-loss performance than the most common technique: RC polyphase filter. This method is based on the transmission lines. The first drawback of this method is the area because it is based on $\lambda/4$. The second drawback of this method is higher phase error compared with the RC polyphase filter. Since we prioritize the insertion-loss and noise figure, we obtained an IQ generator by two lumped quadrature hybrid couplers.

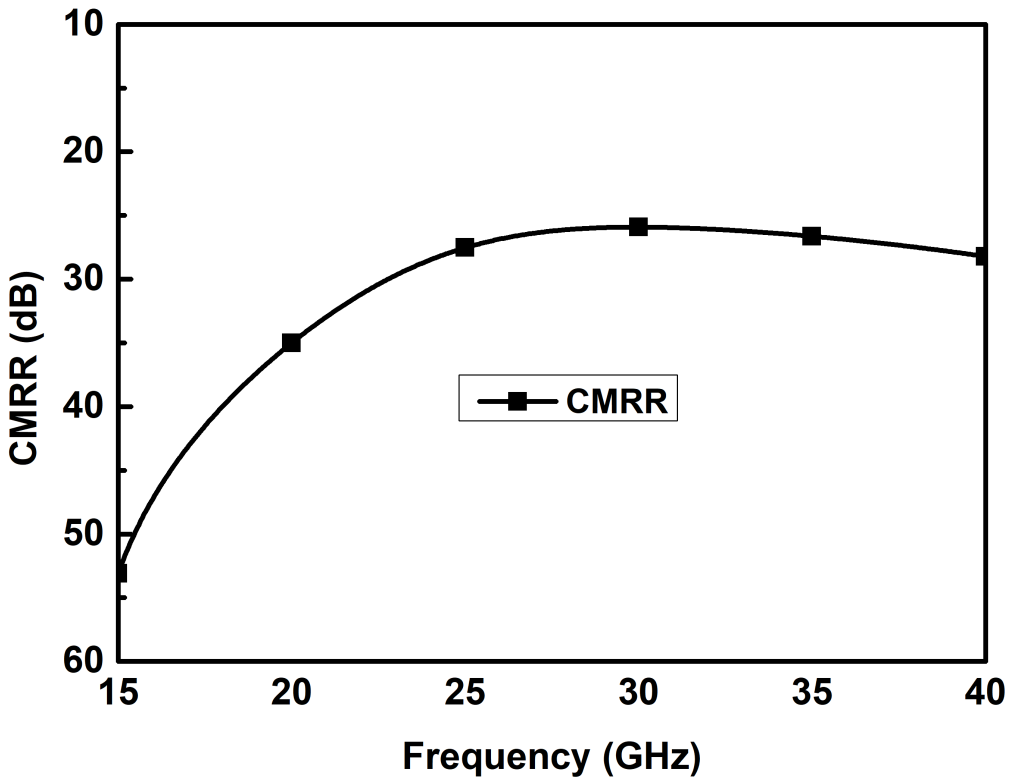


Figure 4.9 The CMRR result of the designed balun.

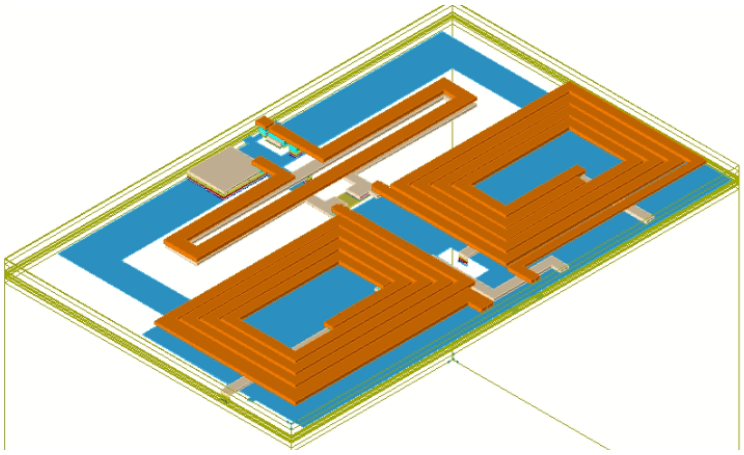


Figure 4.10 The layout of the designed balun with the I/Q generator.

4.1.1.3 Gilbert-Cell Core

After obtaining IQ signals, the gilbert-cell core amplifies these four signals with different gain settings to obtain the phase shift. The schematic of the gilbert-core is shown in Fig. 4.5. The HBT sizes are 6x0.48 μm, and they are biased for a maximum tail current of 5.4 mA. 300 pH with 100fF is used for matching the output to 100 Ω. In order to widen the bandwidth of matching, 460 Ω is employed. The balun follows the output of the gilbert-cell to combine these two signals.

4.1.1.4 Current-Steering DAC

The most important part of the VM is determining the tail current values of the gilbert-cell core. In this work, in order to determine the current values, 42-bit current steering DAC is used. In DAC, we create the reference voltage for the current generator transistor, which is called M_{0-23}. These 24 transistors will be used to adjust the phase of the signal. Then after two current mirrors, M_{24-41} is used to determine the ratio of the last current mirror. In that way, we will adjust the amplitude level of the signal. The width of each transistor is given in Fig. 4.5. There is a trade-off between the transistor number and the current generation error. Since we are using less number phase and amplitude resolution, we can decrease the number of transistors. We can increase the width of each transistor to make sure that we are supplying the same current level. However, that way leads to a high error level in terms of current. Eventually, it decreases the phase performance of the phase shifter.

4.1.1.5 Measurement Results

Starting from this block, all measurements performed in SUMER group with our lab facilities. The measurement setups for S-parameters, P1dB, NF, and IIP3 are explained in Chapter 3. The same measurement setups is also used while measuring each sub-blocks. S-parameter measurement of VM is realized with a Keysight PNA network analyzer. First, SOLT calibration of network analyzer until the probe is performed with the calibration substrate. Then the S-parameter measurements were performed while switching the required information from the FPGA. The die photo of the stand-alone VM is shown in Fig. 4.11.

The S-parameter measurement results of the designed VM at the reference state are shown in Fig. 4.12 and Fig. 4.13. The measured gain value at the reference state is 0 dB. Although the measured input return loss is below -10 dB, the measured output return loss is below -6 dB at the desired frequency. If we design the following block concerning that output return loss value, it will not cause an additional loss.

Fig. 4.14 shows the measured relative phase states at the reference state, and the measured RMS phase and amplitude error are shown in Fig. 4.15. 7-bit phase resolution is achieved with 1-degree RMS phase error and 0.1 dB RMS amplitude error.

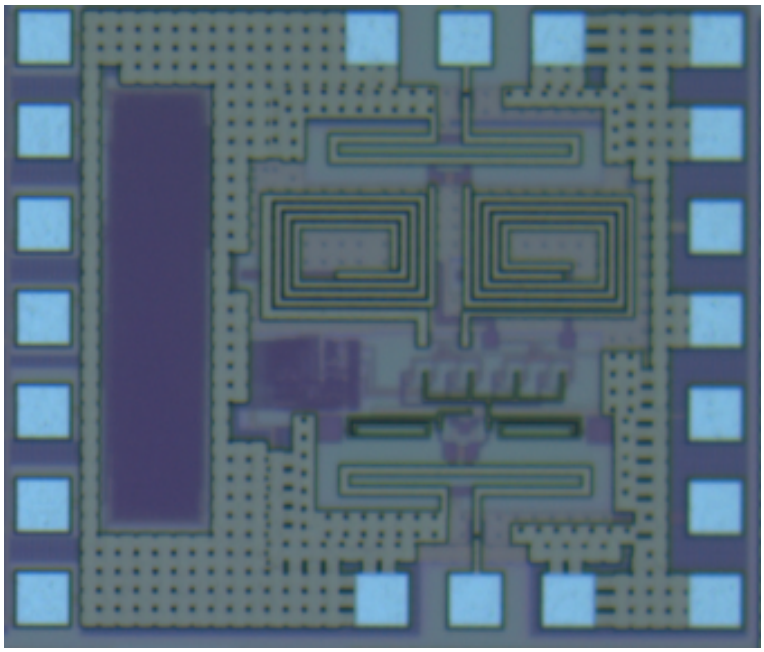


Figure 4.11 The die photo of the designed VM.

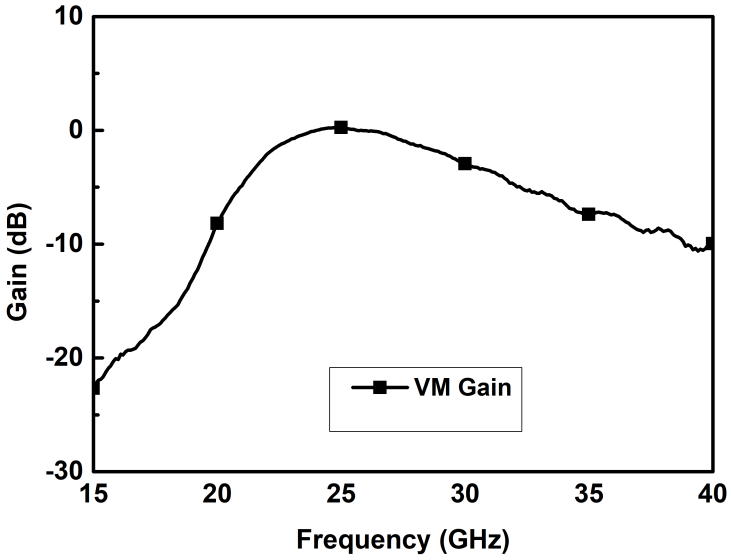


Figure 4.12 The measured gain of VM at the reference state.

Fig. 4.16 shows the measured relative phase states at the lowest amplitude state, and the measured RMS phase and amplitude error at that state is shown in Fig. 4.17. A similar performance is also obtained at that gain reference. 7-bit phase resolution is achieved with 1-degree RMS phase error and 0.1 dB RMS amplitude error. Both results prove that we can achieve similar results in each gain settings.

Fig. 4.18 shows the measured relative amplitude states. The measured RMS amplitude and RMS phase error are also shown in Fig. 4.19. 24-dB amplitude range is achieved with 0.6 degrees RMS phase error and 0.1 dB RMS amplitude error. Moreover, 6-bit amplitude resolution is also achieved.

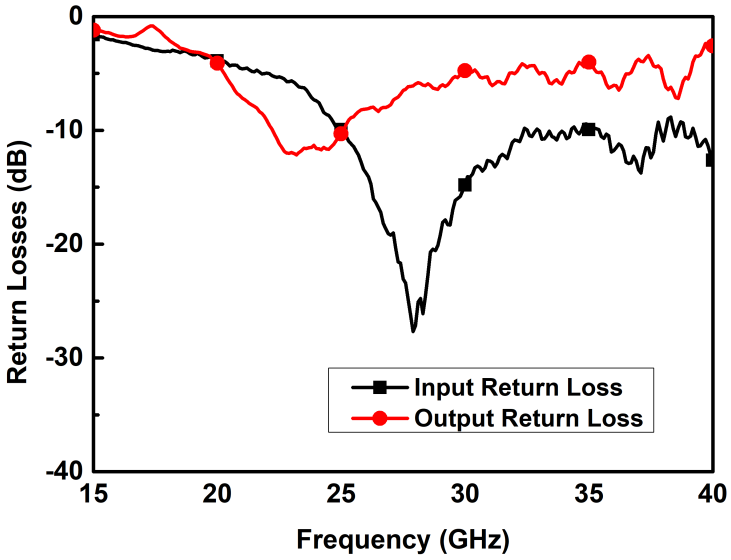


Figure 4.13 The measured input and output return losses of VM at the reference state.

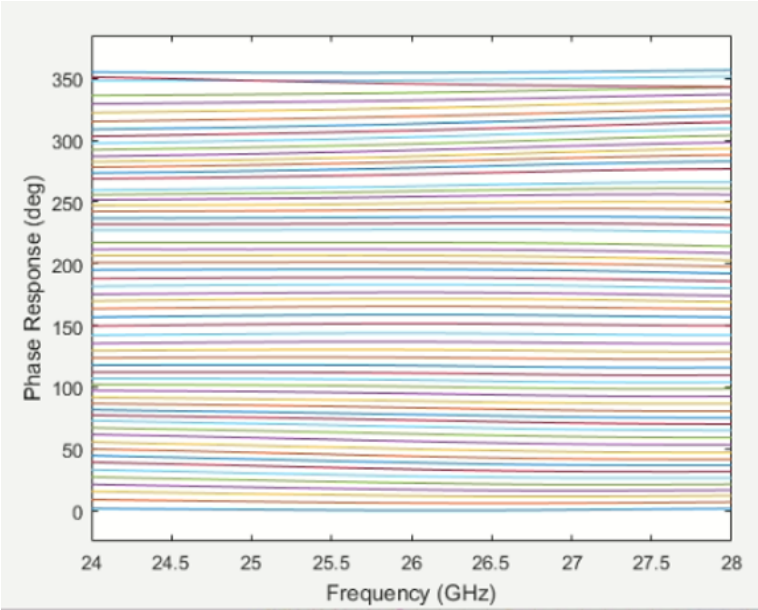


Figure 4.14 The measured relative phase states of VM at the reference state.

The comparison of our work with the state-of-the-art is also shown in Table 4.2 (Akbar & Mortazawi (2017); Byeon, Lee, Lee & Son (2019); Kalyoncu, Burak, Kaynak & Gurbuz (2019); Park, Jeong & Hong (2021); Singh, Mondal & Paramesh (2019)). Our work performs the phase and amplitude shift in a single block, and it achieved the lowest RMS phase and RMS amplitude error and the state-of-the-art phase and amplitude resolution in the literature.

Table 4.2 The comparison of the VM with the state-of-the-art works.

References	**This Work**	**Kalyoncu (2018)**	**Akbar (2017)**	**Park (2021)**	**Singh (2019)**	**Byeon (2019)**
Process	**130 nm SiGe BiCMOS**	130 nm SiGe BiCMOS	130 nm CMOS	65 nm CMOS	65 nm CMOS	130 nm SiGe BiCMOS
Frequency [GHz]	**28**	28	28	30	26	28
Phase Resolution	**7**	8	6	4	5	-
Amplitude Resolution	**6**	-	-	2	-	2
Amplitude Range [dB]	**16**	-	-	17.4	-	5
RMS Phase Err. [degree]	**0.6**	0.2	2.6	2.9	1.18	-
RMS Amp. Err. [dB]	**0.1**	0.2	0.31	0.4	-	-
Gain [dB]	**0**	-0.5	-5	-2.8	5.75	21.2
PDC [mW]	**9**	23	136	18	30.5	8
Size [mm^2]	**0.36**	0.45	0.3	0.21	0.31	0.17

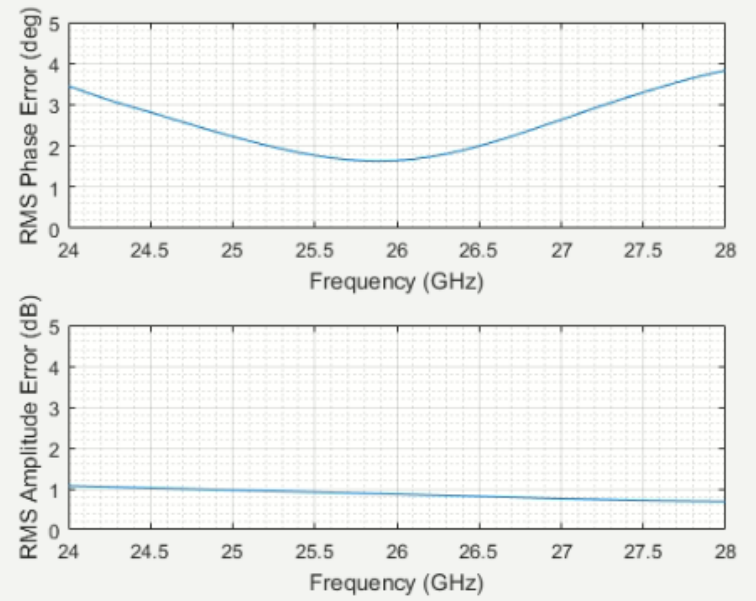


Figure 4.15 The measured RMS phase and amplitude error of VM at the reference state.

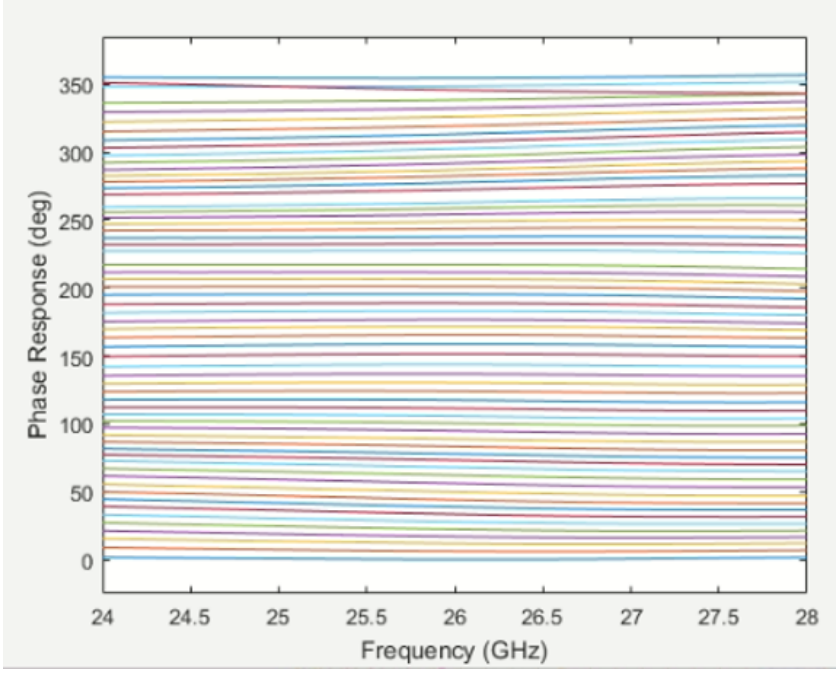


Figure 4.16 The measured relative phase states of VM at the lowest amplitude state.

4.1.2 Asymmetric Switch

Traditionally, to change the mode of operation in the T/R module, SPDTs with a series-shunt connection is employed. While connecting one part of the transmitter or receiver to the antenna, the other part is connected to the ground. Ron resistances of CMOS lead to an insertion-loss in both sides (Hettak, Ross, Wight & Morin (2011); Li, Ustundag, Kumar, Boenke, Kodak & Rebeiz (2018)). In asymmetric switches,

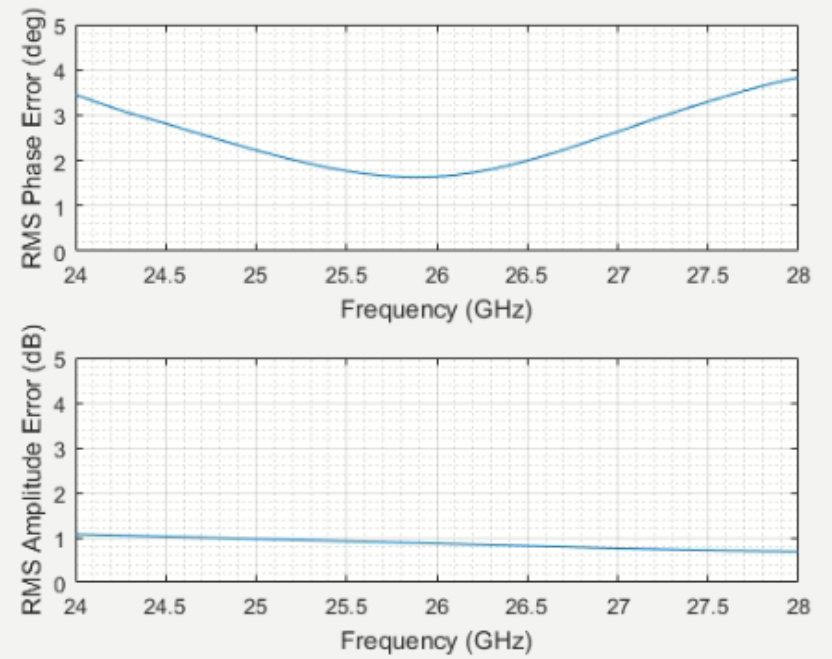


Figure 4.17 The measured RMS phase and amplitude error of VM at the lowest amplitude state.

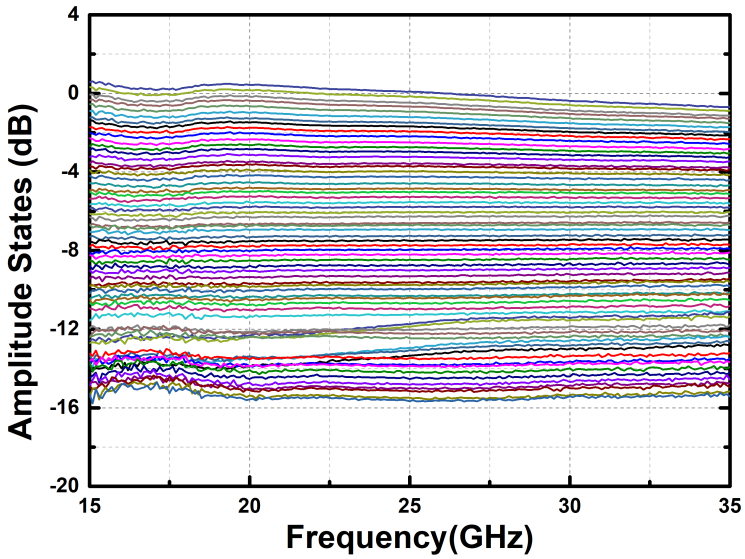


Figure 4.18 The measured relative amplitude states of VM.

as shown in Fig. 4.20, switch operation is combined with the previous RF block to decrease the insertion loss of the switch for a single signal path.

In the receiver mode, the power amplifier will be in the" OFF" mode by zeroing supply voltages to create a high impedance. Since $\lambda/4$ length through connection equals a short circuit in RF, LNA will directly connect to the antenna. The shunt switch must be" OFF" to create a high impedance in the receiver mode.

A low noise amplifier will be in the" OFF" mode in the transmitter mode to create

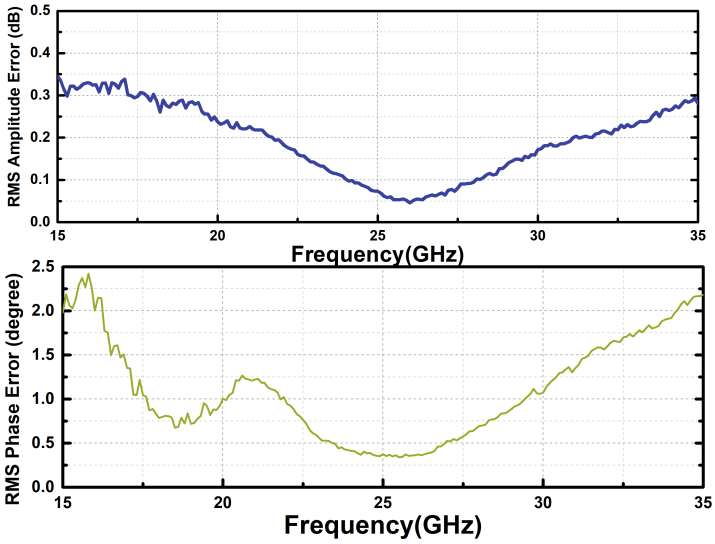


Figure 4.19 The measured RMS phase and amplitude error of VM while switching the amplitude states.

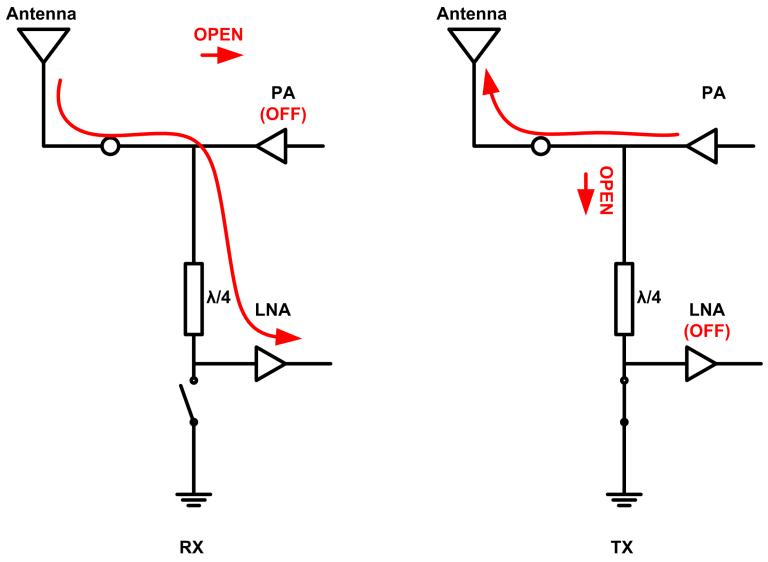


Figure 4.20 Mode of operation for the proposed asymmetric switch.

a high impedance. Since shorted $\lambda/4$ length creates a high impedance, the output of the PA is directly connected to the antenna. Although $\lambda/4$ leads to an insertion-loss in the receiver mode, a direct connection to the PA output does not lead to performance degradation in terms of the output power.

Fig. 4.21 shows the schematic of the designed asymmetric switch. The insertion loss of SPDT is inversely proportional to the number of transistors of the transistors. When the number of transistors increases, the insertion loss of the SPDT is improved. However, this improvement leads to a lower isolation performance. Consequently, an optimized number of the transistor is chosen.

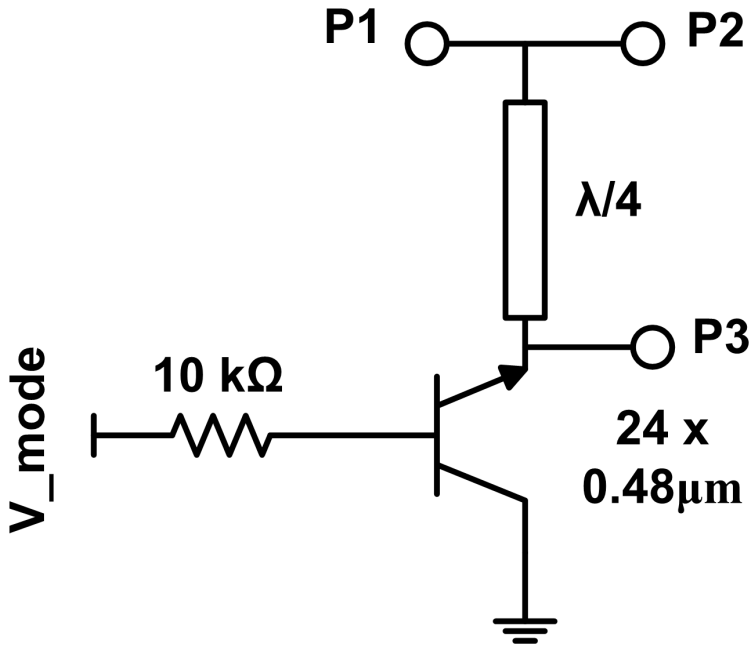


Figure 4.21 The schematic of the designed asymmetric switch.

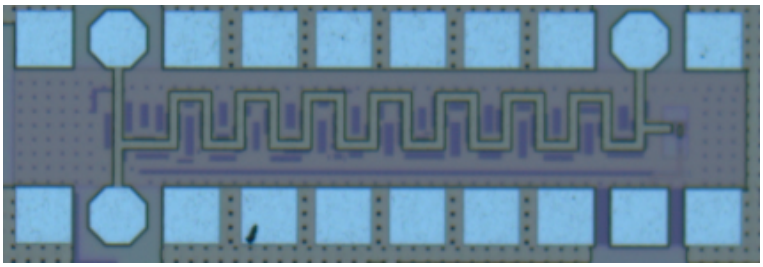


Figure 4.22 The die photo of the designed asymmetric switch.

4.1.2.1 Simulation and Measurement Results

The die photo of the asymmetric switch is shown in Fig. 4.22. The realized asymmetric switch achieves 1.65-1.68 dB insertion loss in TX mode as shown in Fig. 4.23. The input and the output return losses are below <-15 dB in RX mode. The realized asymmetric switch achieves 1.14-1.17 dB insertion loss in TX mode as shown in Fig. 4.24. The input and the output return losses are below <-18 dB in RX mode.

S-parameter measurement of ASYM is realized with a Keysight PNA network analyzer. First, SOLT calibration of network analyzer until the probe is performed with the calibration substrate. Then the S-parameter measurements were performed while switching the mode of operation. The IL value over the $\lambda/4$, is measured as 1.6 dB and the IL value over the direct connection is measured as 1.05 dB as shown from Fig. 4.24 and Fig. 4.23, respectively. The measured input and output return losses for both modes are shown in Fig. 4.24 and Fig. 4.23, respectively.

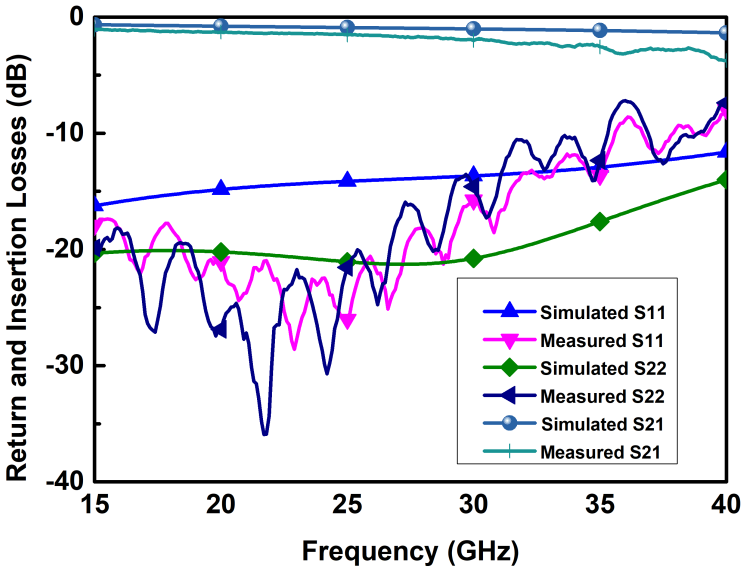


Figure 4.23 S-parameter simulation and measurement results of the asymmetric switch in TX mode.

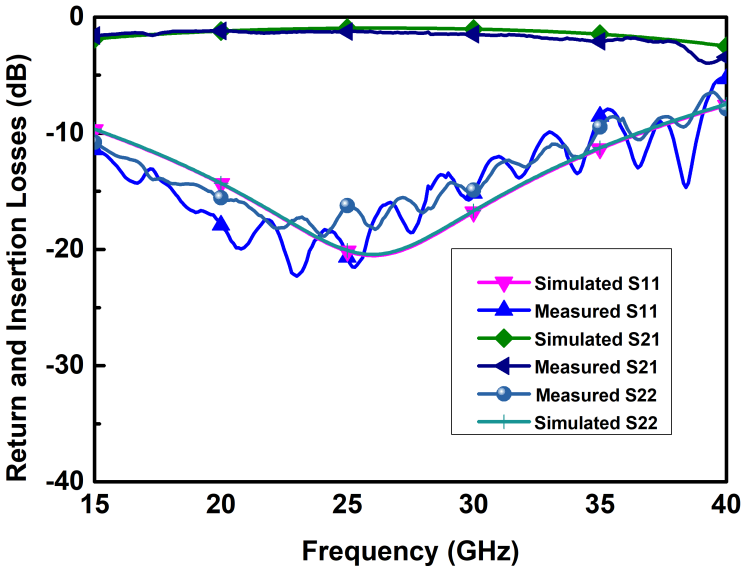


Figure 4.24 S-parameter simulation and measurement results of the asymmetric switch in RX mode.

We try to perform the linearity measurement of the ASYM. Our equipment can supply the output power until 15 dBm. After that point, we cannot increase the input power of the switch. Since our design is based on passive structures, generally, it is valid for all switch designs. We could not measure the IP_{1dB} of the ASYM.

4.1.3 Single-Pole-Double-Throw Switch

In designed modules, HBT based SPDT switches are used to switch between TX and RX modes. Fig. 4.25 shows the schematic of the designed SPDT switch. The realized switch is a series-shunt-based topology. When the first control voltage is high, Q1 and Q4 operate in the deep triode region. In contrast, Q2 and Q3 operate in the cut-off region. In that mode, port1 and port2 are connected with low resistance values, and port3 is isolated. When the second control voltage is high, Q2 and Q3 operate in the deep triode region. In contrast, Q1 and Q4 operate in the cut-off region. In that mode, port1 and port3 are connected with low resistance values, and port2 is isolated. The isolation performance of the SPDT is improved by using Q3 and Q4 transistors by grounding the unused port.

The insertion loss of SPDT is inversely proportional to the number of transistors of the Q1 and Q2 transistors. When the number of transistors increases, the insertion loss of the SPDT is improved. However, this improvement does not continue linearly. Consequently, the best number of the transistor is chosen.

4.1.3.1 Simulation and Measurement Results

The simulation results of realized SPDT switch achieves $<$ 1.77 dB insertion loss as shown in Fig. 4.26. The simulated input and the output return losses are below $<$ 20 dB, as shown in Fig. 4.27.

S-parameter measurement of SPDT is realized with a Keysight PNA network analyzer. First, SOLT calibration of network analyzer until the probe is performed with the calibration substrate. Then the S-parameter measurements were performed while switching the mode of operation. The die photo of the stand-alone SPDT is shown in Fig. 4.28. The IL value of the SPDT is measured as 2.7 dB as shown from Fig. 4.26. The measured input and output return losses are shown in Fig. 4.27.

We try to perform the linearity measurement of the SPDT. Our equipment can supply the output power until 15 dBm. After that point, we cannot increase the input power of the switch. Since our design is based on passive structures, generally, it is valid for all switch designs. We could not measure the IP_{1dB} of the SPDT. We

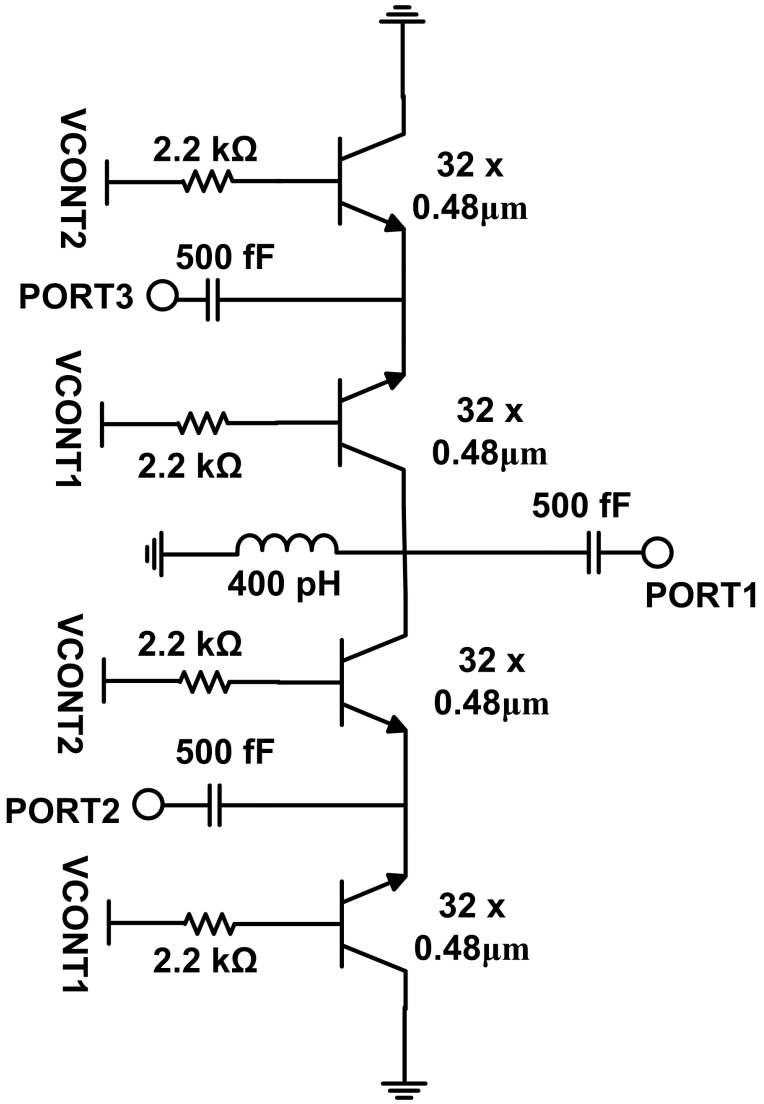


Figure 4.25 The schematic of the designed SPDT.

can say that the IP_{1dB} of the SPDT is higher than 15 dBm.

The comparison of our works with the state-of-the-art is also shown in Table 4.3 (Li et al. (2018); Parlak & Buckwalter (2011); Trinh, Kao, Chiu & Karmakar (2019); Yang et al. (2018); Yu, Ma, Meng, Yeo, Shyam, Zhang & Verma (2017)). The measured SPDT work has good results in terms of bandwidth, isolation, and power handling capability. However, the insertion loss of the SPDT is high. The measured ASYM work has good results in insertion loss, bandwidth, and power handling capability. However, the isolation of that switch is low.

4.1.4 Low Noise Amplifier and Power Amplifier

Table 4.3 The comparison of out SPDT and ASYM with the state-of-the-art

References	**ASYM Work**	**SPDT Work**	**Parlak (2011)**	**Li (2018)**	**Yu (2017)**	**Jang (2018)**	**Trinh (2019)**
Process	**130 nm SiGe BiCMOS**	**130 nm SiGe BiCMOS**	45 nm CMOS SOI	45 nm CMOS SOI	130nm SOI	65nm CMOS	150nm GaAs HEMT
Frequency [GHz]	**15-40**	**15-40**	28	33	28	22	28
IL [dB]	**<1.3**	**<3.3**	2.8	<1	2.4	2.65	3.5
Isolation [dB]	**>10**	**>30**	16.2	>20	10.2	17.9	10.5
IP1dB [dBm]	**>15 dBm**	**>15 dBm**	-12	29.5	-3	N/A	-11.8

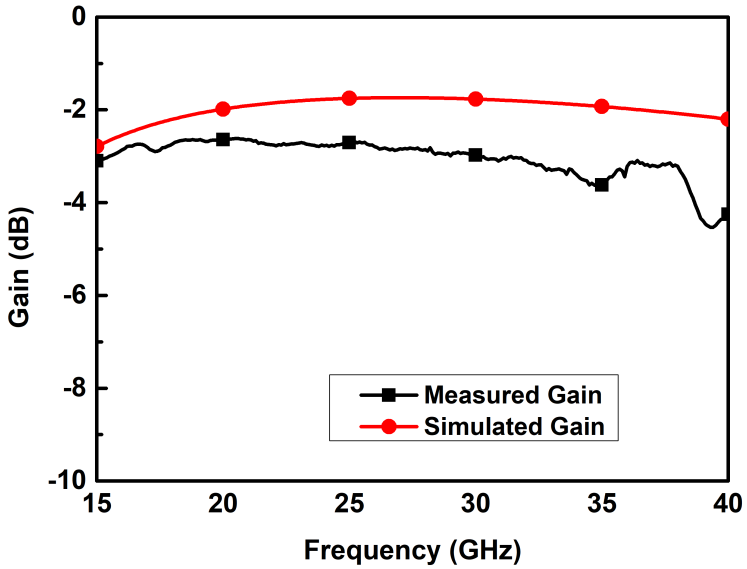


Figure 4.26 The simulated and measured insertion-loss of the designed SPDT.

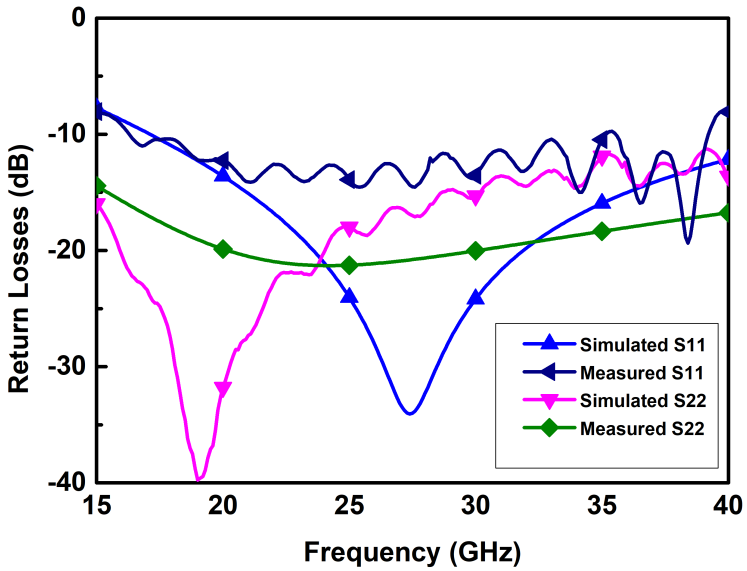


Figure 4.27 The simulation and measurement return-losses results of the designed SPDT.

Colleague Hamza Kandis designed the low noise amplifier. The schematic of the LNA is shown in Fig. 4.29. Although the common-emitter amplifiers have better noise figure performance, a single-stage cascode topology is selected due to the advantage of high gain and high isolation. In order to obtain simultaneous power and noise matching at 26 GHz, the number of the transistor for the LNA is selected as 20 x 0.48 μm. To decrease the size of the LNA in the x-direction, the input matching was performed with the 400 pH shunt inductance with 120 fF series capacitance. The emitter inductance value is selected as 50 pH. To match the output to 50-ohm, 300 pH shunt inductance parallel with 300-ohm and series with 140-fF is realized.

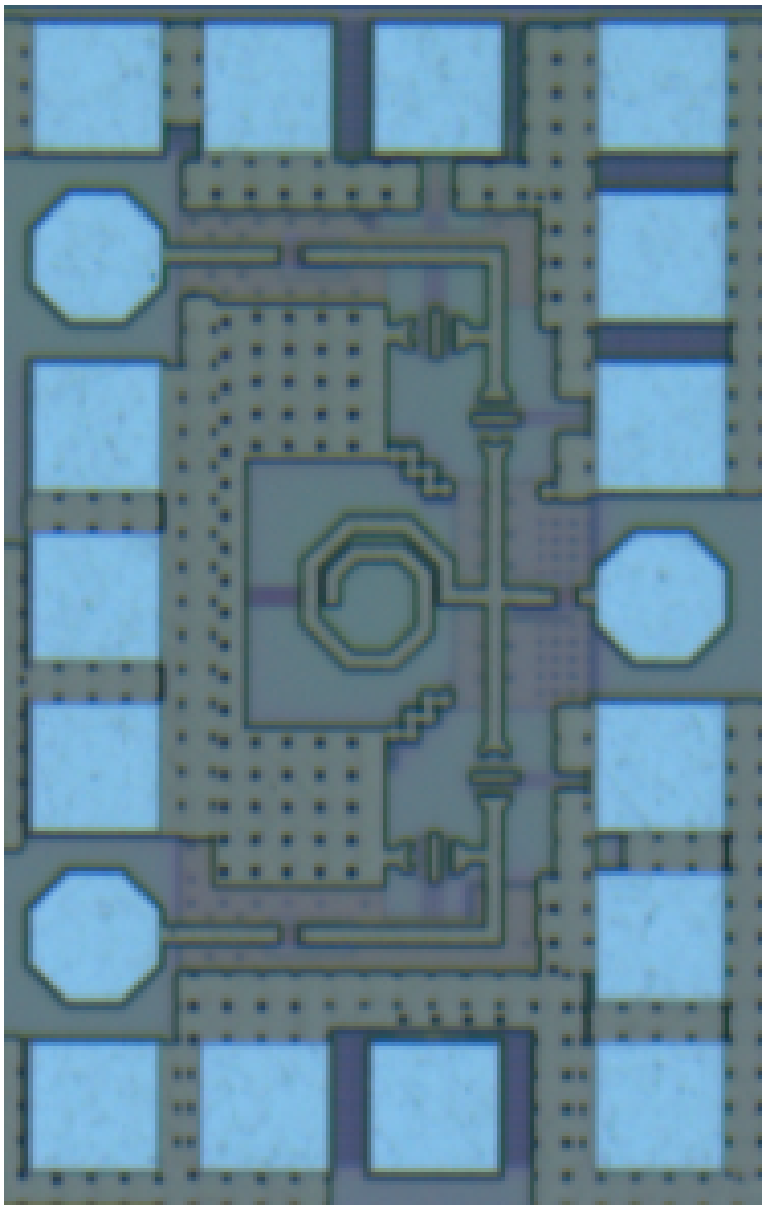
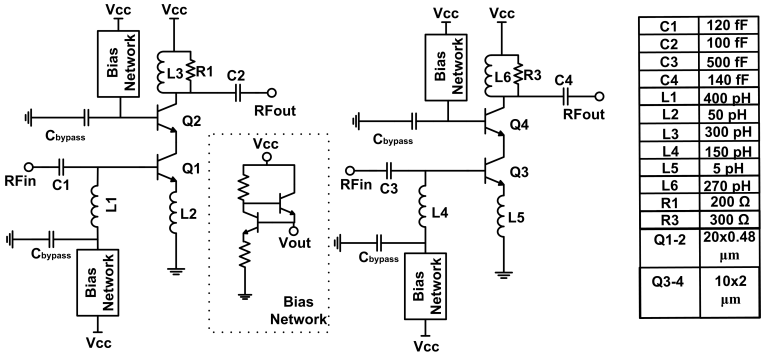


Figure 4.28 The die photo of the designed SPDT.



C1	120 fF
C2	100 fF
C3	500 fF
C4	140 fF
L1	400 pH
L2	50 pH
L3	300 pH
L4	150 pH
L5	5 pH
L6	270 pH
R1	200 Ω
R3	300 Ω
Q1-2	20x0.48 μm
Q3-4	10x2 μm

Figure 4.29 The schematic of the designed LNA(left) and PA(right).

Colleague Isık Berke Gungor designed the power amplifier. The schematic of the PA is shown in Fig. 4.29. The topology of the circuitry is selected as a single-stage

cascode due to the advantage of high gain and high isolation. The main objective of the power amplifier is to obtain high output power. Therefore, to achieve high output power in this technology, transistor size with higher emitter width is selected. The number of transistors for the PA is selected as 10 x 2 μm. To decrease the size of the PA in the x-direction, the input matching was performed with the 230 pH shunt inductance with 500 fF series capacitance. There is a trade-off between the gain of the PA with the value of the emitter inductance. The advantage of the higher emitter inductance is that better matching performance. Since we match the input of the power amplifier to the previous sub-block, we preferred to use the lowest possible emitter inductance value, which equals 5 pH from the emitter connection of the transistor to the ground. To match the output to 50-ohm, 400 pH shunt inductance parallel with 300-ohm and series with 140-fF is realized.

4.1.4.1 Simulation and Measurement Results

In the literature, some works also exist for 5G receiver applications (Chen et al. (2016a); Chen, Gao, Leenaerts, Milosevic & Baltus (2016b); Cui & Long (2020); El-Aassar & Rebeiz (2020); Jacobsson et al. (2006); Keshavarz Hedayati, Abdipour, Sarraf Shirazi, Cetintepe & Staszewski (2018); Li et al. (2018); Nawaz, Albrecht & Çağrı Ulusoy (2019); Yeh et al. (2017)). As shown in Fig. 4.31 and Fig. 4.32, the simulated stand-alone noise figure of LNA is $<$ 2.92 dB with $>$ 12.3 dB gain in the frequency of the interest. The power consumption of the LNA is 5.4 mW.

S-parameter measurement of LNA is realized with a Keysight PNA network analyzer. The die photo of the stand-alone LNA is shown in Fig. 4.30. The measured gain value of the LNA is measured as 10.84 dB at the center frequency, and the measured gain result is shown in Fig. 4.31. The measured input and output return losses are shown in Fig. 4.33.

Fig. 4.34 shows the linearity measurement of the LNA. The measured IP_{1dB} of LNA is -6 dBm. Fig. 4.32 shows the measured NF of the designed LNA. The measured NF of LNA is 3.08 dB. In summary, our LNA achieves the state-of-the-art measurement results with 10.84 dB gain, 3.08 dB NF, and -6 dBm IP_{1dB}.

Two different figures of merit (FOM) are introduced to determine the performance of the LNAs. Both have a contribution of gain, NF, and power consumption, but first FOM takes IP_{1dB} into account, whereas the second FOM uses IIP_3. These FOMs are given in (4.2) and (4.3). S21, IP_{1dB} and IIP_3 are converted into the

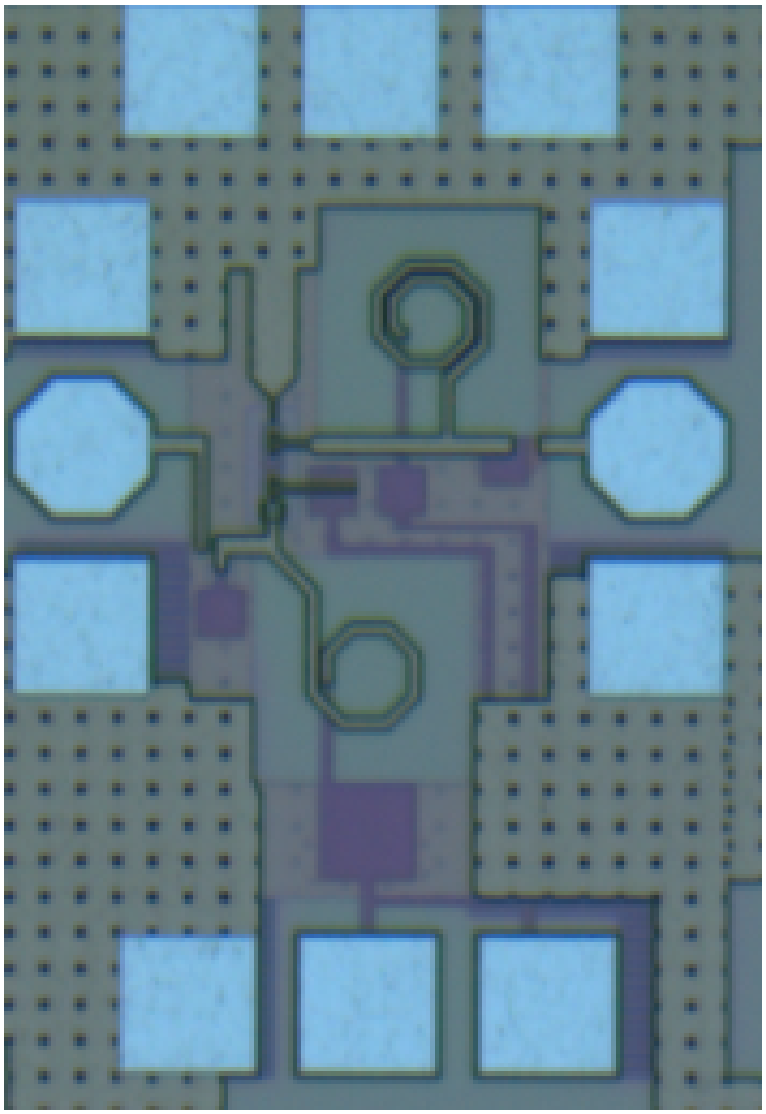


Figure 4.30 The die photo of the designed LNA.

linear scale, and noise factor is used, which is in linear scale instead of noise figure which is in decibels. Table 4.4 compares the designed LNA with the state-of-the-art. The designed LNA achieves the lowest power consumption and the lowest area. Moreover, our LNA achieved state-of-the-art FOM and NF in the literature.

$$FOM_1 = \frac{S21(lin) \times IP_{1dB}(lin)}{P_{DC}(mW) \times (F-1)} \tag{4.2}$$

$$FOM_2 = \frac{S21(lin) \times IIP_3(lin)}{P_{DC}(mW) \times (F-1)} \tag{4.3}$$

Table 4.4 The comparison of the designed LNA with the state-of-the-art LNAs.

References	**This Work**	**Nawaz (2019)**	**Keshavarz (2018)**	**El-Aassar (2020)**	**Cui (2020)**	**Chen (2019)**
Process	**130 nm SiGe BiCMOS**	130 nm SiGe BiCMOS	28nm CMOS	22nm FDSOI	22nm FDSOI	65 nm CMOS
Center Frequency [GHz]	**28**	28	33	28	22	28
NF [dB]	**3.08**	2.8	4.9	2.4	2.65	3.5
Gain [dB]	**10.84**	16.2	18.6	10.2	17.9	10.5
IP1dB [dBm]	**-6**	-12	-25.5	-3	N/A	-11.8
IIP3 [dBm]	**4**	N/A	N/A	7.5	-14.4	-1
PDC [mW]	**5.4**	8.2	9.7	15	5.6	5.4
Area [mm^2]	**0.01**	0.23	0.23	0.26	0.17	0.25
FOM1	**0.547**	0.35	0.01	0.47	-	0.11
FOM2	**5.47**	-	-	5.32	0.48	1.33

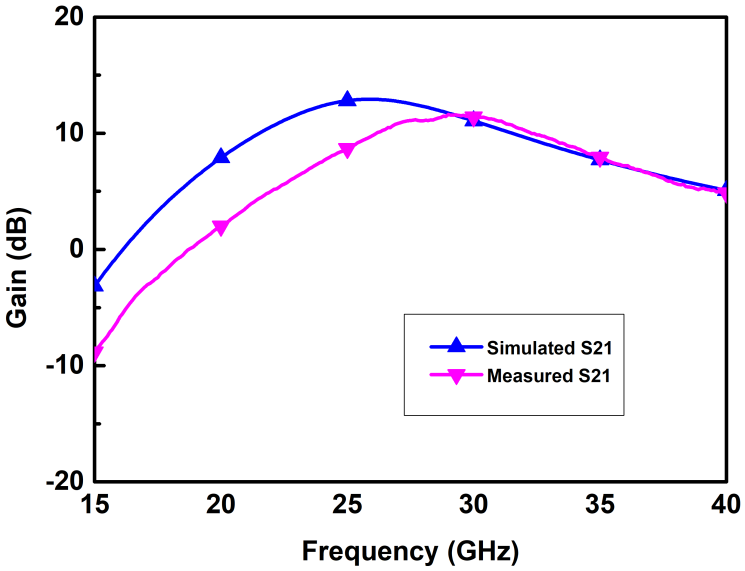


Figure 4.31 The measurement and simulation gain result of the designed LNA.

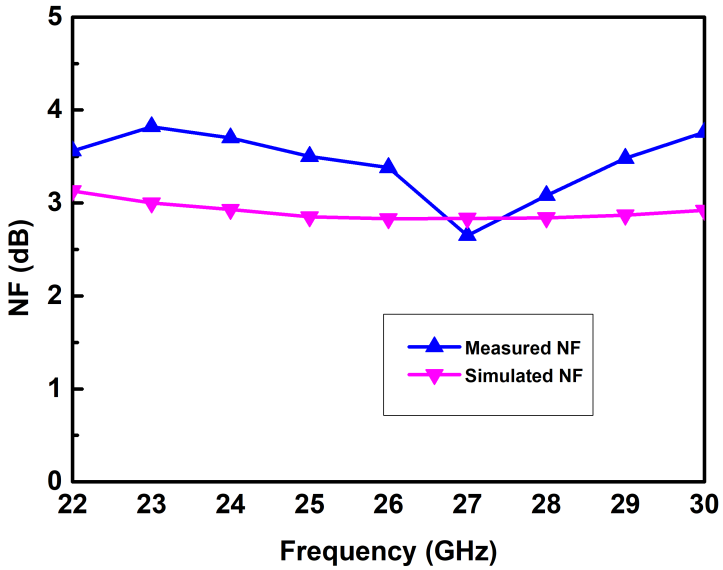


Figure 4.32 The measurement and simulation NF result of the designed LNA.

In the literature, some PA works also exist for 5G transmitter applications (Mortazavi & Koh (2016); Sarkar & Floyd (2017); Shakib et al. (2019,1)). The die photo of the designed PA is shown in Fig. 4.35. As shown in Fig. 4.38 and Fig. 4.36, the simulated stand-alone output power of PA is 14.7 dBm with a $>$ 15.1 dB gain. The power consumption of the PA is 16 mW. The input and output return losses of the designed PA are shown in Fig. 4.37.

Table 4.5 shows the comparison of our work with the state-of-the-art power amplifiers work in the literature Ali, Agarwal, Gopal & Heo (2019); Mortazavi & Koh (2016); Sarkar & Floyd (2017); Vigilante & Reynaert (2018); Wan, Zhang, Li & Wang (2021). Our work achieved comparable gain, PAE, P1dB values, and the

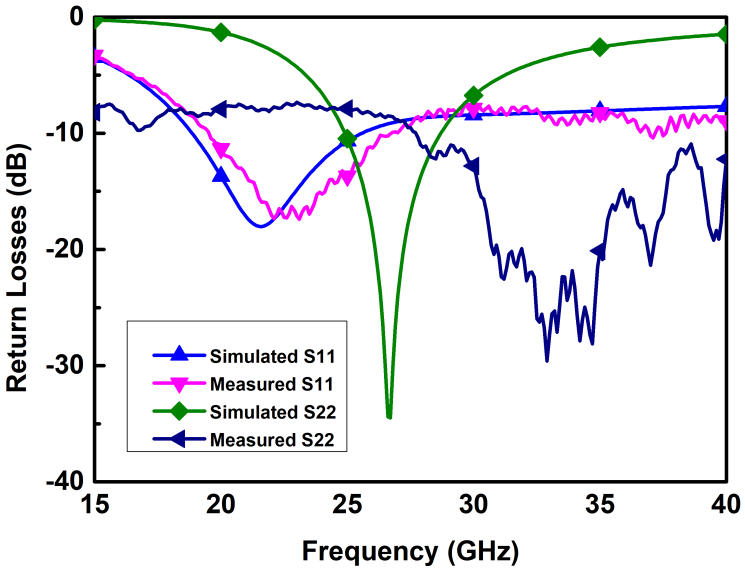


Figure 4.33 The measurement and simulation return loss result of the designed LNA.

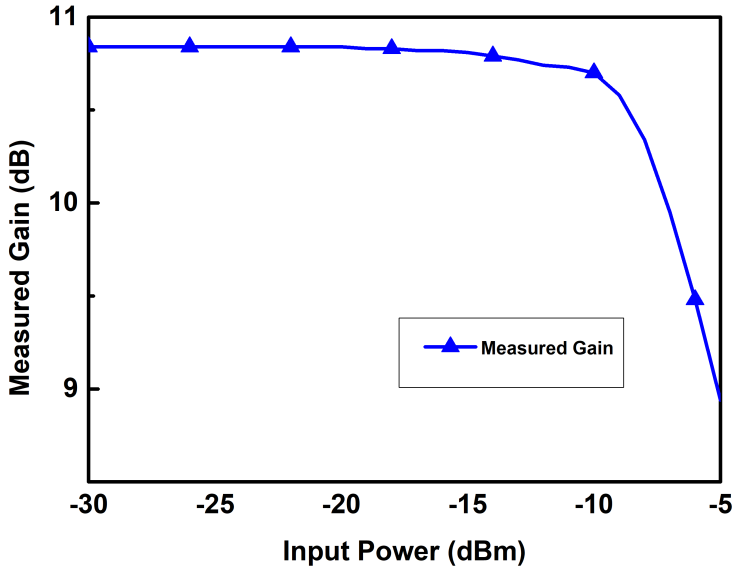


Figure 4.34 The measured input power vs. gain result of the designed LNA.

best area performance in the literature. We believe that our work will satisfy the requirements of 5G communication.

4.1.5 Serial Peripheral Interface

A digital control circuit is designed to set the amplitude and phase information of the VM circuitry and realize with IHP 0.13μm SiGe BiCMOS digital standard library. The layout of the SPI is shown in Fig. 4.39. The die area of the SPI is 0.8 mm^2. This

Table 4.5 The comparison of the designed PA with the state-of-the-art PAs.

References	**This Work**	**Mortazawi (2016)**	**Sarkar (2017)**	**Vigilante (2018)**	**Sheikh (2019)**	**Wan (2021)**
Process	**130 nm SiGe BiCMOS**	130 nm SiGe BiCMOS	130 nm SiGe BiCMOS	28 nm CMOS	65 nm CMOS	130 nm SiGe BiCMOS
Frequency [GHz]	**28**	24	28	30	29	35
PAE	**%26**	%50	%33.8	%39.5	%46.4	%27
OP1dB [dBm]	**14.7**	16	15.1	13.4	13.2	22.6
Gain [dB]	**16.65**	21	15	20.8	10	35
Size [mm^2]	**0.1**	0.6	0.445	0.16	0.12	0.48

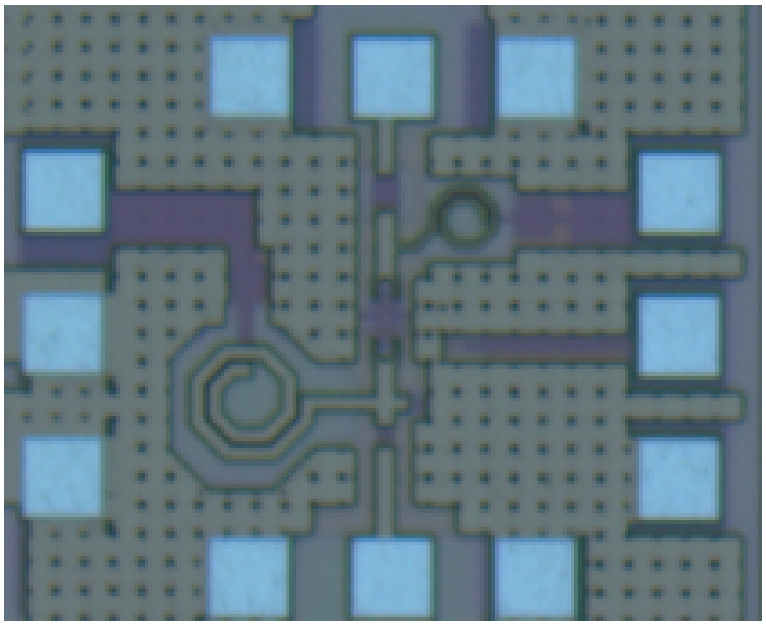


Figure 4.35 The die photo of the designed PA.

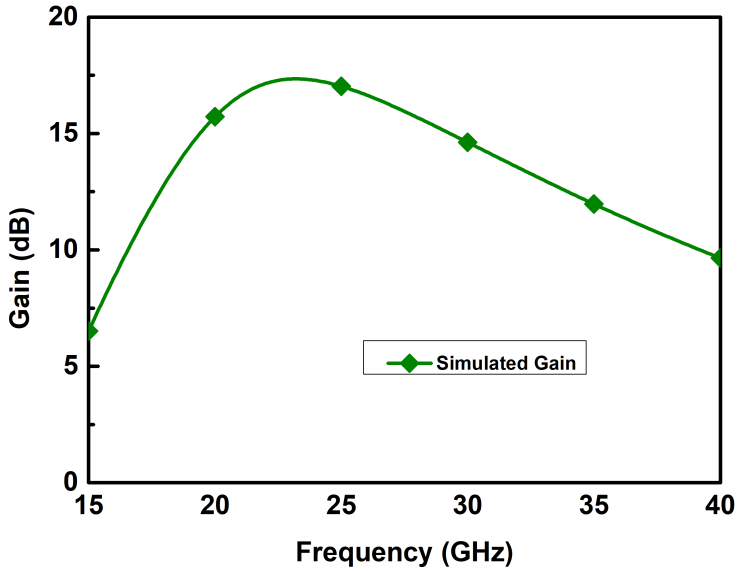


Figure 4.36 The gain simulation result of the designed PA.

circuit is a series peripheral interface(SPI), an asynchronous serial communication standard and rising edge triggered. In this circuit, there are four different input bits, clock, load, serial data, reset, and 42 output bits directly connected to the bit information of the VM. The load bit must be set to high, and after 42 clock cycles, serial data is shifted to the register. This data set the phase and amplitude information of the VM. Fig. 4.40 shows the timing diagram of the SPI.

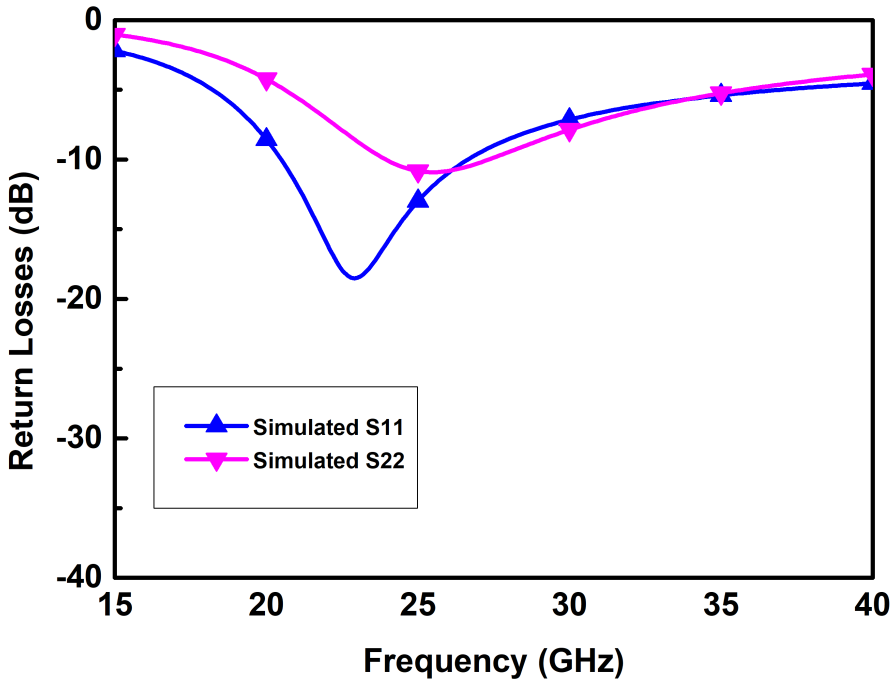


Figure 4.37 The simulation result of input and output return losses of the designed PA.

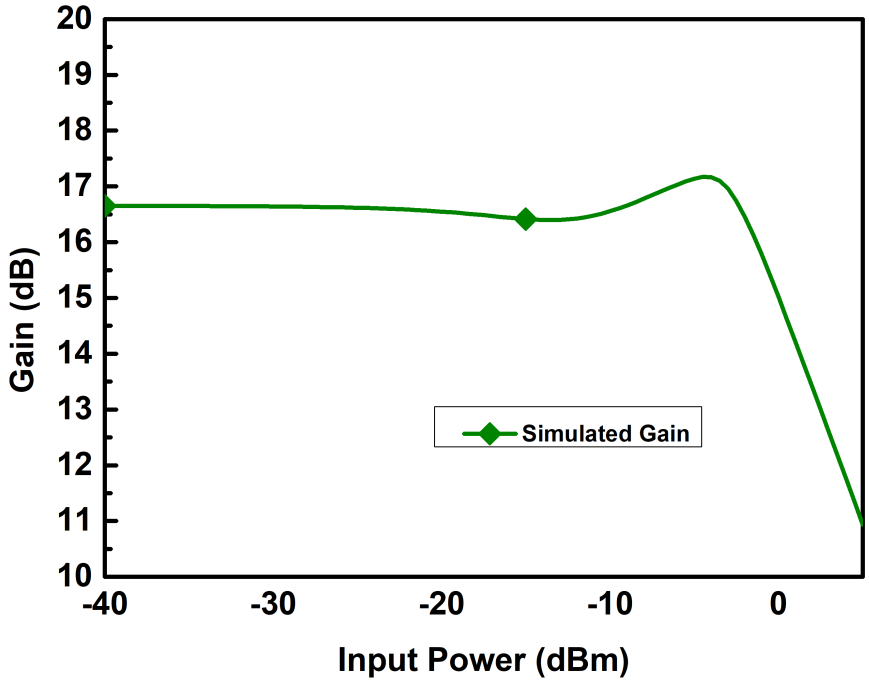


Figure 4.38 The linearity simulation result of the designed PA.

4.1.6 Power Detector and 20-dB Coupler

A 20-dB directional coupler is designed to sense the output power with the power detector. These two blocks will be used for a built-in self-test. A conventional

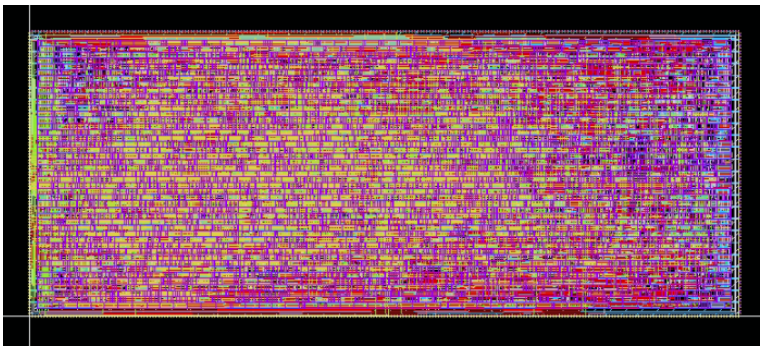


Figure 4.39 The layout of the designed SPI.

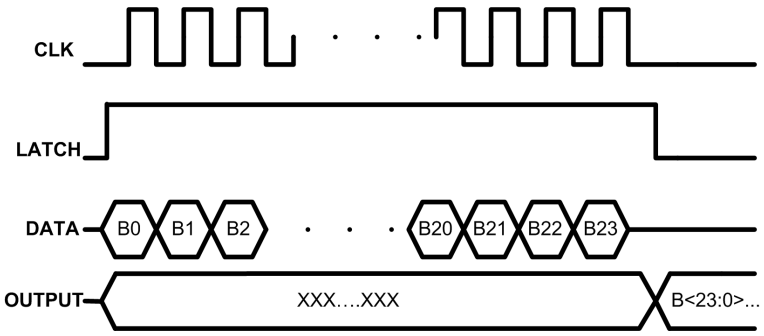


Figure 4.40 The explanation of each mode for SPI.

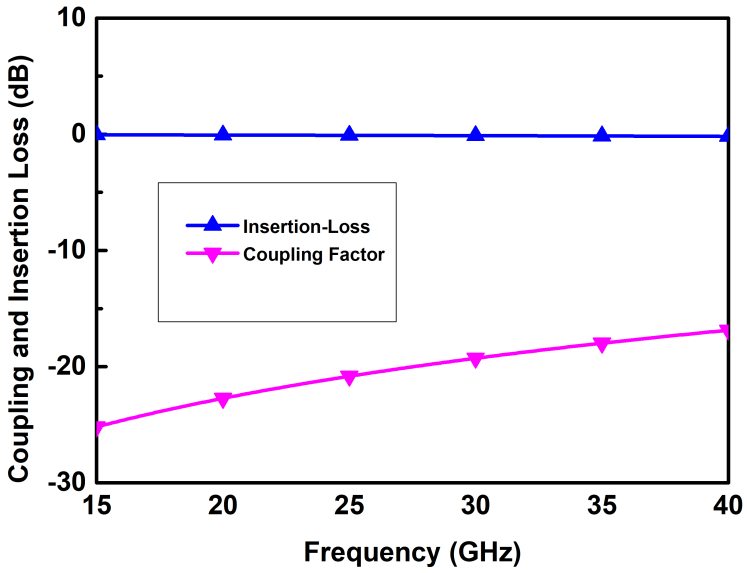


Figure 4.41 The simulation result of the insertion-loss and coupling factor of designed coupler.

directional coupler topology is used to realize a 20-dB coupler. The simulation result of the directional coupler and the layout of the directional coupler is shown in Fig. 4.41, Fig. 4.42, and Fig. 4.43, respectively.

The coupled RF signal is sensed with the power detector. The schematic of the power detector is shown in Fig. 4.44. Since it is not placed in the signal path,

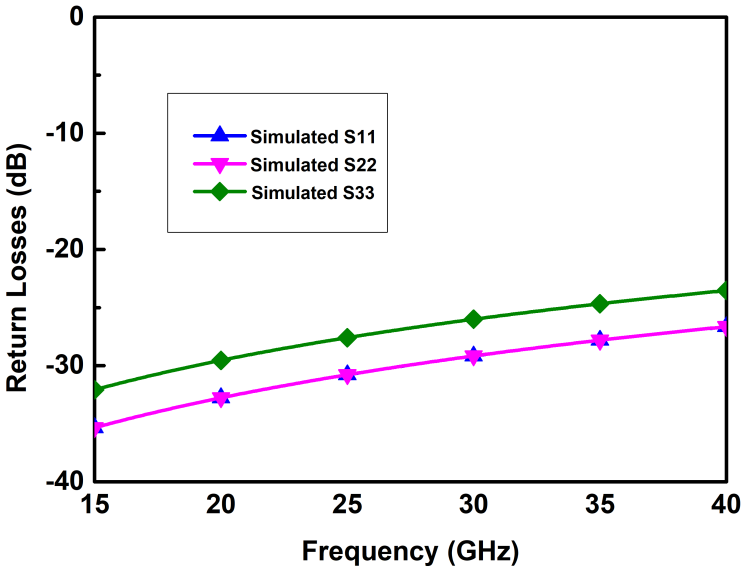


Figure 4.42 The simulation result of the return losses of designed coupler.

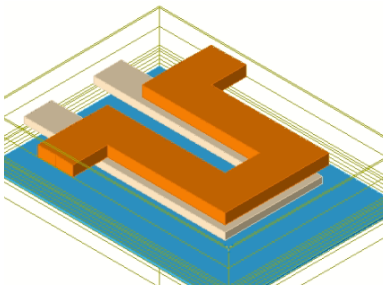


Figure 4.43 The layout of the designed coupler.

we did not check the input return loss of the power detector. The DC output is generated concerning the input power. The simulation result of the DC output vs. the input power is shown in Fig. 4.45. A similar performance is also obtained when we measure the DC output vs. the input power. The measurement result is also shown in Fig. 4.45.

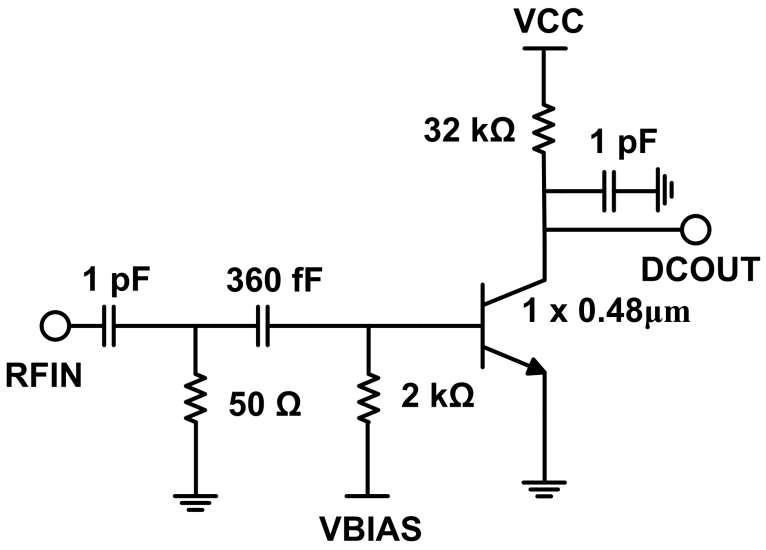


Figure 4.44 The schematic of the designed power detector.

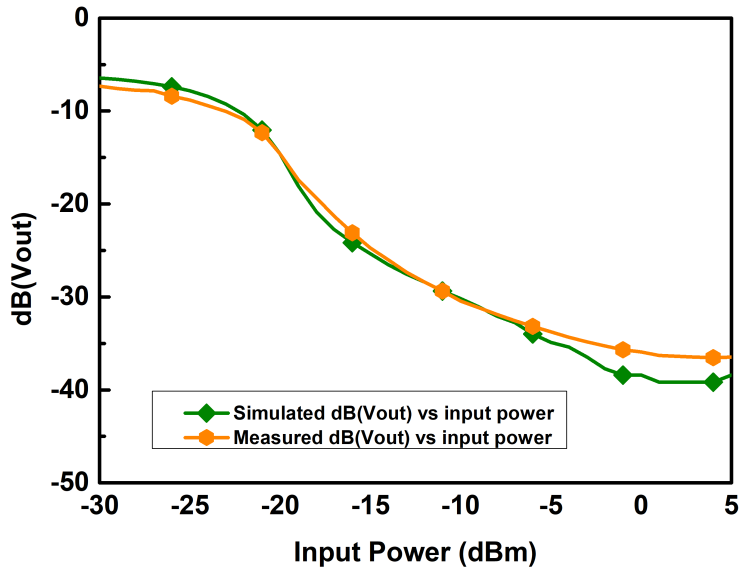


Figure 4.45 The simulation and measurement results of the DC output vs the input power of the designed power detector.

4.1.7 Wilkinson Combiner

Three conventional Wilkinson combiners were designed using a Top-Metal-2-Metal-1 transmission line to build a 1:4 Wilkinson combiner. The layout of the Wilkinson combiner is selected concerning the layout of other sub-blocks to reduce the overall die area. The die photo of the Wilkinson combiner is shown in Fig. 4.46. The die area of the Wilkinson combiner is 0.12 mm^2. The designed Wilkinson combiner has an EM simulated 1 dB insertion loss. The stand-alone measurement of the Wilkinson combiner is also realized, and the IL of the Wilkinson combiner is measured as 2

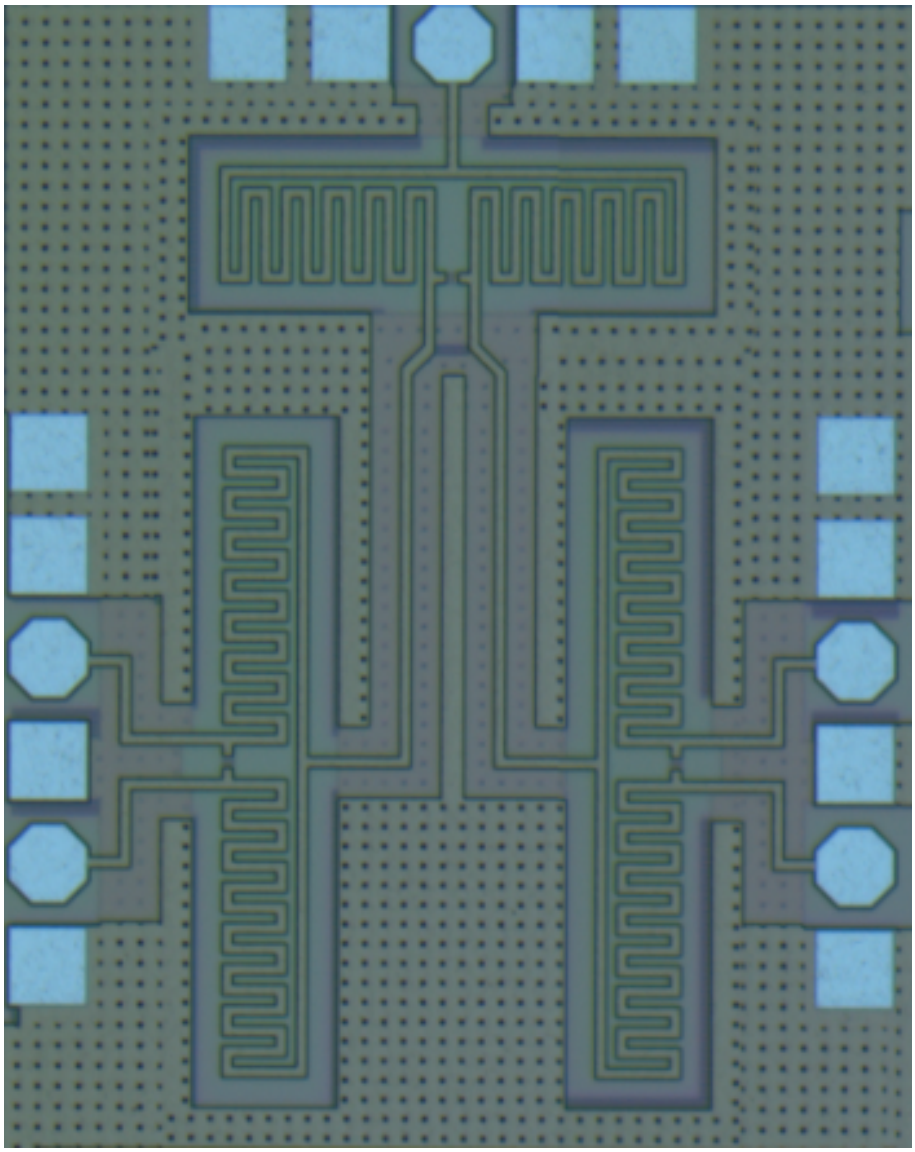


Figure 4.46 The die photo of the designed wilkinson combiner.

dB. The role of the Wilkinson combiner is to combine the received signals from each receiver channel divide the signal into four transmitter channels to transmit to the environment.

4.1.8 Combined LNA and PA

In order to increase the NF performance of the RX channel, we realized that we could redesign LNA and PA, and we can improve the NF performance of RX mode. Ideally, when we turn off the PA, high impedance occurs at that terminal of the asymmetric switch, and LNA will be connected to the antenna directly. However,

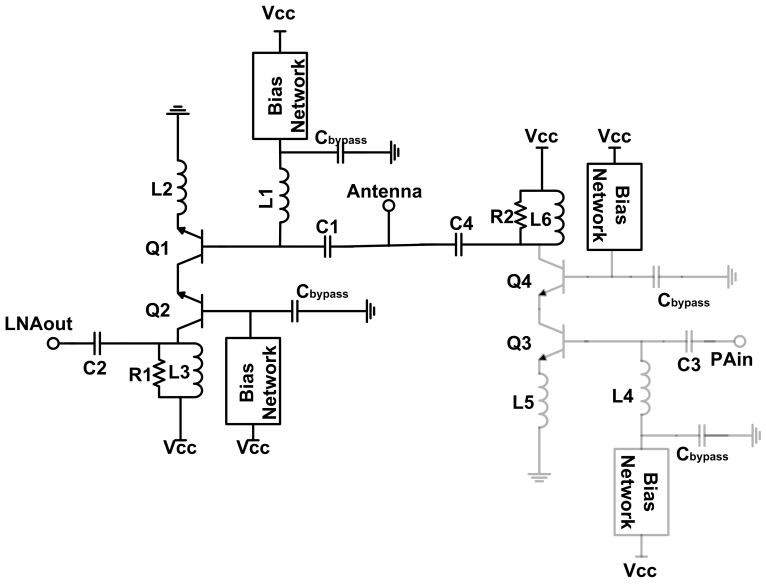


Figure 4.47 The impedance that occurs when the PA is in OFF mode.

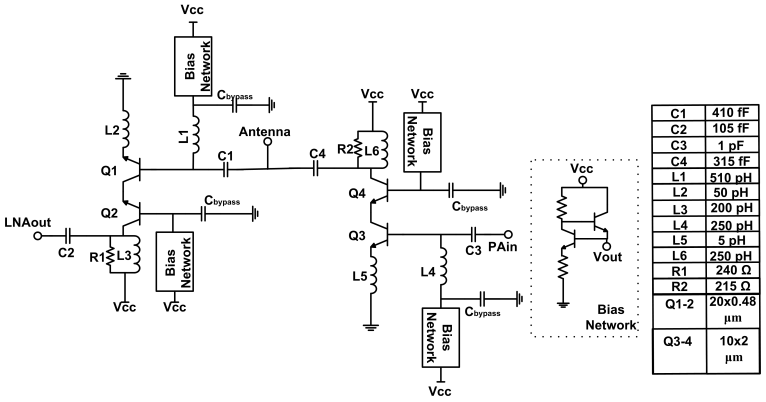


Figure 4.48 The impedance that occurs when the PA is in OFF mode.

in reality, as shown in Fig. 4.47, the impedance of that port will be the output matching network of PA. To minimize the NF value in RX mode, we need to design the output matching of the PA with the input matching of the LNA simultaneously. Therefore, instead of using the asymmetric switch, we will connect the input of the LNA with the output of the PA as shown in Fig. 4.48. Simultaneous, step-by-step matching was performed for better linearity and NF performance.

The schematic of the LNA with the PA is shown in Fig. 4.48. Single-stage cascode topology is selected for both of them. The input matching of the LNA is also a part of PA's output matching. The output matching of the PA is also a part of the input matching of the LNA. The overall layout of the LNA with the PA is shown in Fig. 4.49.

The stand-alone NF performance is shown in Fig. 4.50. The designed LNA has a 4.7 dB NF performance at the center frequency, 23.2 dB gain performance. The

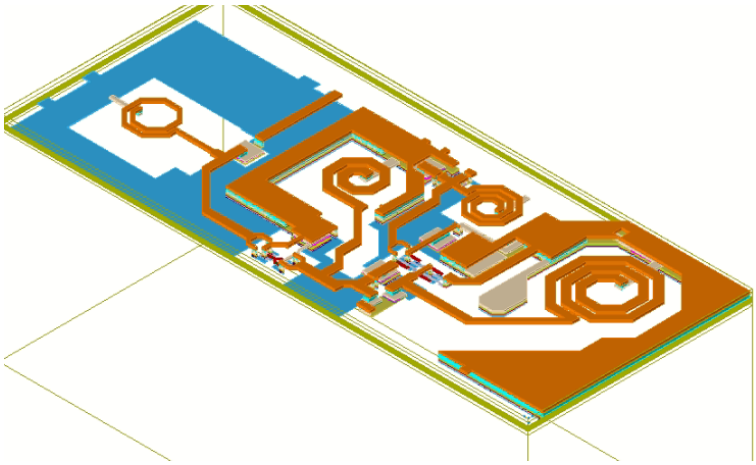


Figure 4.49 The layout of the designed LNA and PA.

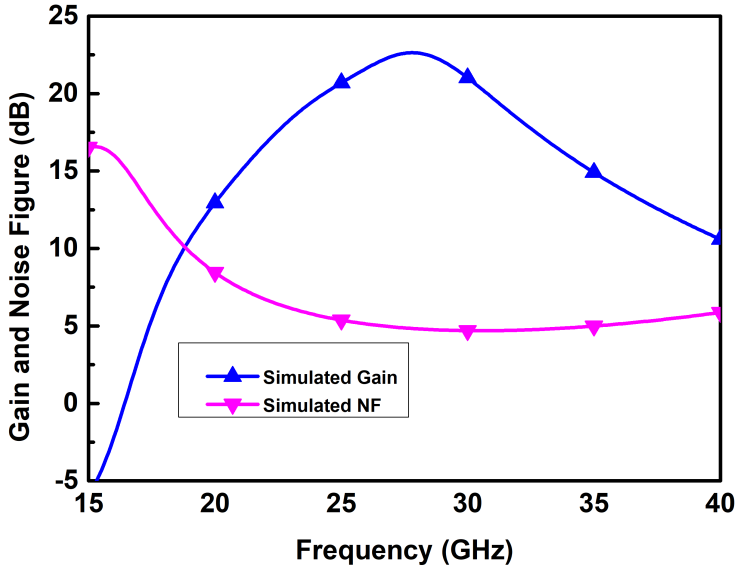


Figure 4.50 The gain and NF simulation results of the designed LNAPA in RX mode.

simulated reflection coefficients depict S11 < -10 dB in 22.3–28.3 GHz and S22 < -10 dB in 24.9–30.4 GHz as shown in Fig. 4.51.

The stand-alone PA performance is shown in Fig. 4.52, Fig. 4.53, and Fig. 4.54. The designed PA has an 11.7 dBm linearity performance at the center frequency, 21.55 dB gain performance. The simulated reflection coefficients depicts that S11 < -10 dB in 24.4–30.9 GHz and S22 < -10 dB in 23.7–30.1 GHz.

4.1.9 Overall Layouts

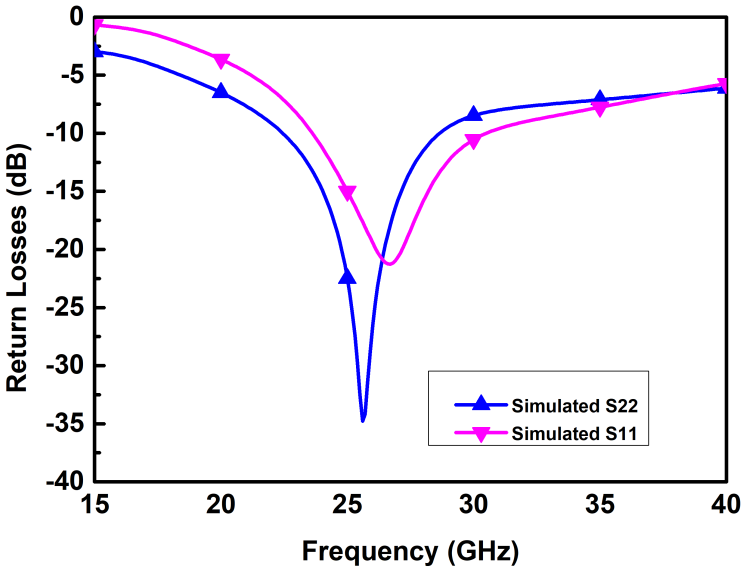


Figure 4.51 The simulation results of input and output return losses of the designed LNAPA in RX mode.

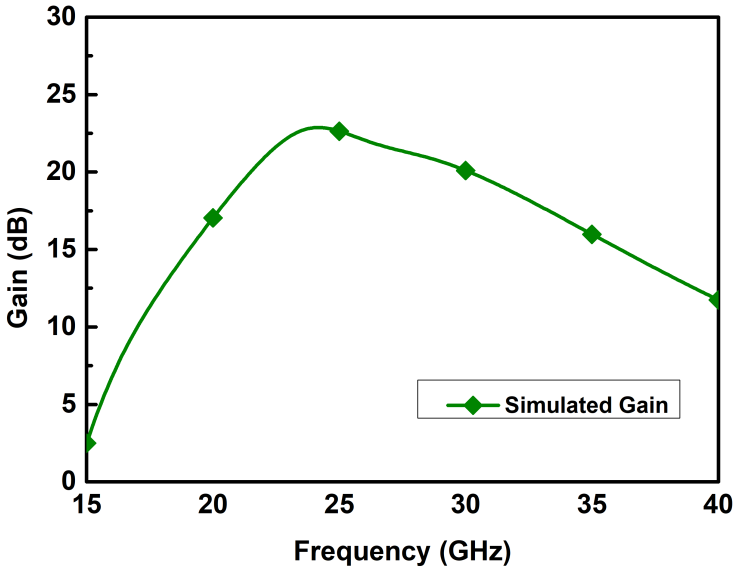


Figure 4.52 The gain simulation result of the designed LNAPA in TX mode.

Three different versions of the single-channel TX/RX module are taped out by using these sub-blocks. Each one of them includes VM, SPDT, SPI, LNA, PD, and 20-dB coupler. The first version of the designed single channel TX/RX module has an SPDT while combining these two channels. The layout of the designed first version is shown in Fig. 4.55. While selecting the mode of operation, SPDTs are employed. In RX mode, the received signal connects the input to the LNA via an SPDT. To increase the gain of the channel, another LNA is used. To change the phase and amplitude of the signal, VM is realized, and another SPDT is realized to finalize the receiver part of the TX-RX channel. In TX mode, the signal is connected to VM

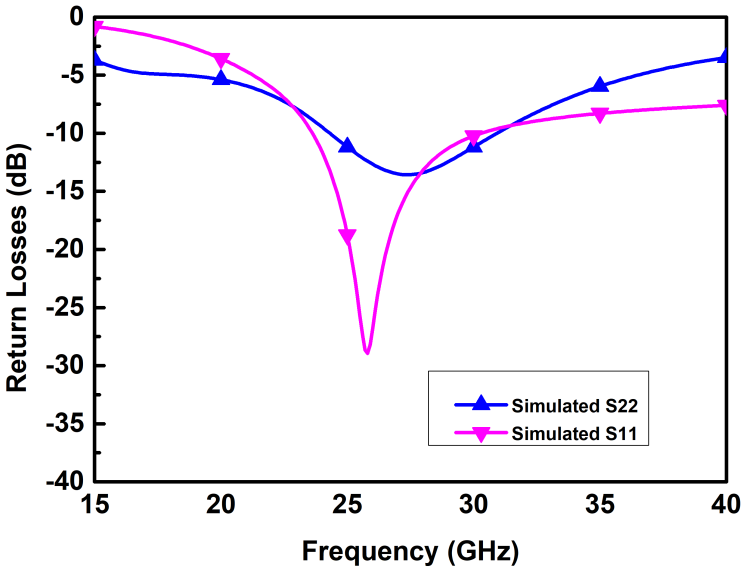


Figure 4.53 The simulation results of input and output return losses of the designed LNAPA in TX mode.

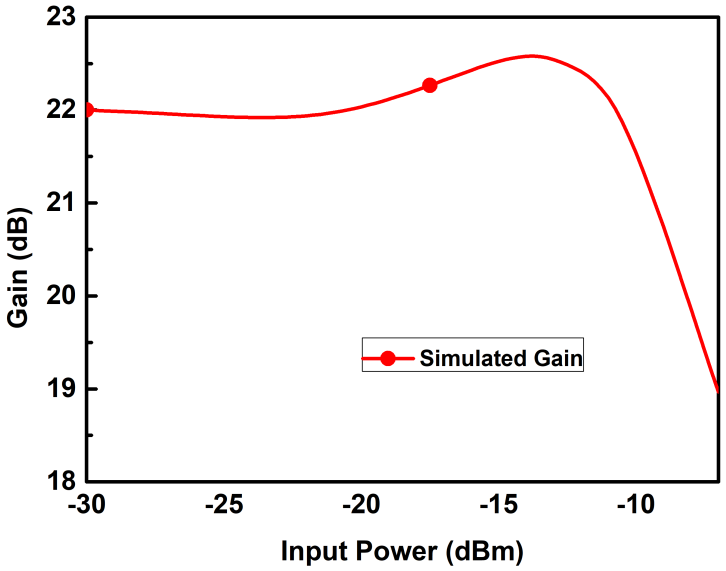


Figure 4.54 The linearity simulation result of the designed LNAPA in TX mode.

via an SPDT. The designed LNA is realized as a driver amplifier before the PA. The designed PA transmits the power to the environment via an SPDT.

The layout of the designed second version is shown in Fig. 4.56. The difference between the first and second versions is that an asymmetric switch is employed instead of SPDT to decrease the insertion loss in both modes. The drawback of using this type of switch is that they lack isolation.

The layout of the designed third version is shown in Fig. 4.57. Although realizing the overall channel with an asymmetric switch has benefits, the lack of isolation between

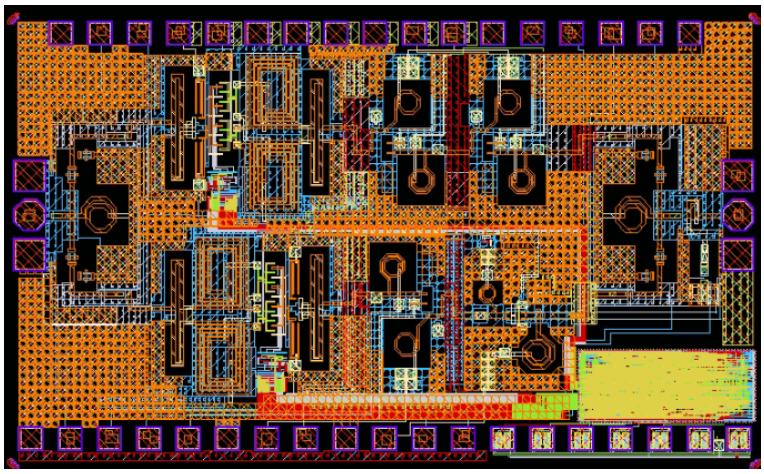


Figure 4.55 The layout of the first designed version of TX/RX channel.

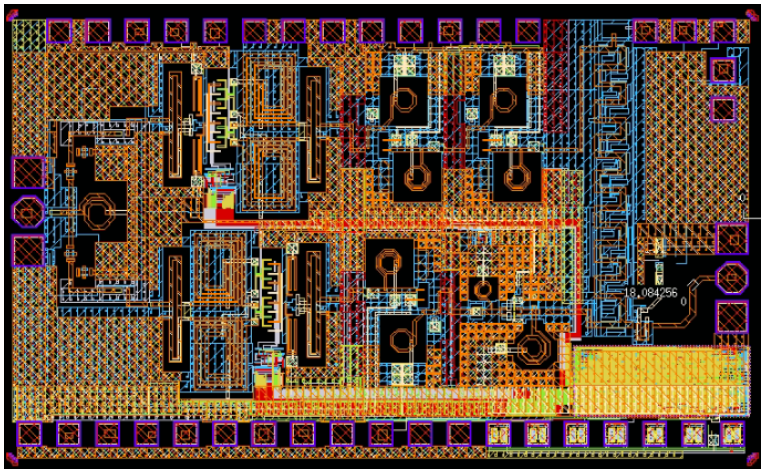


Figure 4.56 The layout of the second designed version of TX/RX channel.

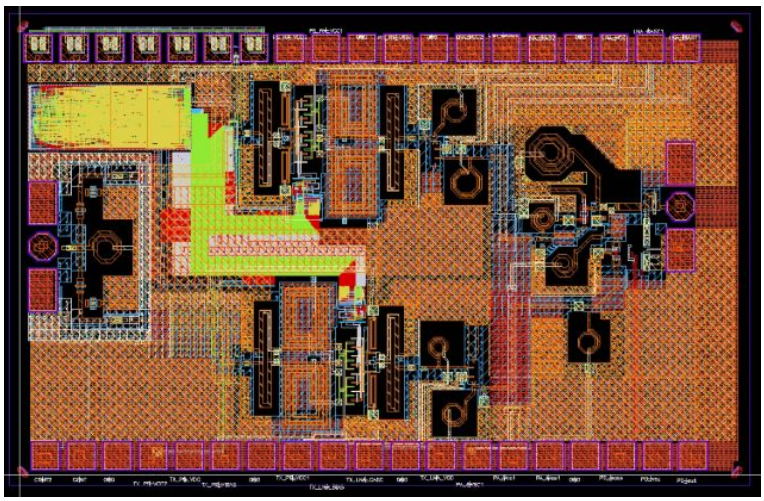


Figure 4.57 The layout of the third designed version of TX/RX channel.

ports leads to a performance loss. To compromise this performance loss, another TX-RX channel design with the switchless LNA-PA. Instead of using switches, the mode of operation will be decided by turning on or off the designed sub-blocks.

5. CONCLUSION AND FUTURE WORK

5.1 Summary of Work

5G mobile communication systems require higher data rates, lower latency, higher spectral efficiency, and lower cost efficiency than the 4G LTE mobile communication systems. To achieve such extreme requirements, new techniques such as mm-wave frequencies, multiple-input-multiple-output, phased array transceivers are needed.

In this thesis, four-channel TX and four-channel RX to realize 5G MIMO applications and three different single-channel TX/RX modules to form a 5G beamforming system with the lower cost are implemented in 130-nm SiGe BiCMOS. In four-channel RX and TX, single-stage cascode LNA, single-stage cascode PA, single bit attenuator, VGA based on the current steering technique with the integration of DACs, PS based on the vector sum technique with the integration of DAC are realized. Integration of these sub-blocks forms four-channel TX and RX system with 6-b phase control, 4-b amplitude control, 4.5 dB NF, and 9.7 dBm output power. Moreover, the lowest RMS phase and amplitude error are achieved, leading to a lower sidelobe level for the phased array systems while creating the beamforming. These circuits can be used in 5G base stations or mobile phones. Since it is realized in 130-nm SiGe BiCMOS technology, this die will be cheaper than the III-V counterparts. It achieved high phase and amplitude resolution, which means the number of needed dies for a sharper beam will decrease. With the integration of the antenna, this die will achieve tens of Gbps data rates which is higher than the requirements of 5G applications.

After realizing the first die, to decrease the cost and increase the functionality of the die, a single channel TX/RX is realized with 7-b phase resolution and 6-b amplitude resolution. The achieved NF value is 4.7 dB, and the output power of the PA is

11.7 dBm while consuming less power than the first design. 7-b phase and 6-b amplitude resolution are achieved in a single block which enables to achieve the lowest RMS phase and amplitude error, better than the first design and the best in the literature. It lowers side lobes in the phased array system. Since higher output power is achieved, the data rate of the system will be higher than the first design. Better functionalities with the higher linearity and the lower power consumption make that die a better candidate for a 5G phased array system after creating a four-channel version. This die is also realized with 130-nm SiGe BiCMOS, which means a cheaper design with respect to III-V counterparts and can be easily used commercially.

5.2 Future Work

In the short term, the measurements of single-channel TX/RX explained in Chapter 4 must be done to verify the simulation results. Although each sub-block is measured and verified separately, we might observe some measurement differences while we form a channel. A PCB board must be designed and fabricated to measure the designed single channels. After verifying a single channel, a four-channel version of the TX/RX chip can be developed. To connect each channel, we can use designed Wilkinson combiners. This die can be integrated with the antenna, and a communication scheme can be formed. From the transmitter side, data can be sent via the antenna and to the receiver side. This measurement will prove that the designed circuitry is an excellent candidate to meet 5G data-rate requirements cheaply.

In the long term, we can integrate the measured four-channel TX, and RX explained in Chapter 3 with the upconverter mixer and downconverter mixer to form a complete system 5G beamforming with the integration of baseband. Then, we can connect an antenna to form a communication scheme, and we can measure the bit rate of the system. Such a system can be used in base stations, mobile phones, or any desired hardware to realize 5G applications.

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APPENDIX A

List of Publications

During my post-graduate period, I was the author and co-author of nine journal papers and five conference papers. Moreover, we already submitted six conference papers and we plan to submit four journal papers and one conference paper in a short term. You can find the list of publications during my post-graduate period in Sabanci University with SUMER group under the supervision of Prof. Yaşar GÜRBÜZ below.

JOURNALS

Burak, A., Çalışkan, C., Yazici, M., & Gurbuz, Y. (2021). "X-band 6-bit SiGe BiCMOS Multifunctional chip with +12 dbm Ip1db and flat-gain response". IEEE Transactions on Circuits and Systems II: Express Briefs,68(1), 126–130. doi:10.1109/TCSII.2020.3008769

Davulcu, M.,Burak, A., & Gurbuz, Y. (2020). "A 7-bit reverse-saturated sige hbt discrete gain stepattenuator".IEEE Transactions on Circuits and Systems II: Express Briefs,67(4), 665–669. doi:10.1109/TCSII.2019.2922418

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Ustundag, B., Turkmen, E.,Burak, A., Gungor, B., Kandis, H., Cetindogan, B., Gurbuz, Y. (2020). "Front-end blocks of a w-band dicke radiometer in sige bicmos technology". IEEE Transactions on Circuits and Systems II: Express Briefs,67(11), 2417–2421. doi:10.1109/TCSII.2020.2968313

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CONFERENCE PROCEEDINGS

Ozkan, T. A.,Burak, A., Kalyoncu, I., Kaynak, M., & Gurbuz, Y. (2021). "A high-gain sige bicmos lna for 5g in-band full-duplex applications". In 2020 15th european microwave integrated circuits conference (eumic)(pp. 53–56).

Kandis, H.,Burak, A., Yazici, M., Kaynak, M., & Gurbuz, Y. (2020). "A 7-bit 0.22 db step variable attenuator with flat states and low phase variation at 1.5–13.5 ghz using inmos switches". In 2020 ieee international symposium on circuits and systems (iscas)(pp. 1–4). doi:10.1109/ISCAS45731.2020.91811653

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PLANNED OR SUBMITTED PAPERS

Çalışkan, C. & Burak, A. & Yazici, M. & Öznazlı, N. & Gurbuz, Y. (2021) "Wide-

band 6-Bit SiGe BiCMOS T/R ModuleCore-Chip for X-Band Phased-Arrays" (Submitted to EuMW 2021).

Ozdol, A. B. & Kandis, H. & Burak, A. & Kaynak, M. & Gurbuz, Y. "A 5 GHz 0.98 dB NF Highly Linear LNA in 130 nm SiGe Technology" (Submitted to EuMW 2021).

Mahmud, M. H. & Burak, A. & Çalışkan, C. & Ozkan, T. A. & Ozdol, A. B. & Yazici, M. & Gurbuz, Y. "A Highly Linear SiGe BiCMOS Gilbert-Cell based Downconversion Mixer for 5G Applications" (Submitted to EuMW 2021).

Kandis, H. & Burak, A. & Kana, C. & Gurbuz, Y. "A Phase Coherent DC-25 GHz 6-bit SiGe BiCMOS Step Attenuator with IP1dB >20 dBm" (Submitted to EuMW 2021).

Burak, A. & Altintas, K. & Yazici, M. & Gurbuz, Y. "LNA Designs for 5G Receiver Applications" (Submitted to APMC 2021).

Burak, A. & Kalyoncu, I. & Kandis, H. & Gungor I.B. & Yazici, M. & Gurbuz, Y. "5G MIMO TX and RX with a high phase and amplitude resolution" (Planned to Submit).

Burak, A. & Yazici, M. & Gurbuz, Y. "Design of Simultaneous Phase and Amplitude Controller in a Single Block for 5G Applications" (Planned to Submit).

Burak, A. & Kandis, H. & Gungor, I.B. & Yazici, M. & Gurbuz, Y. "Design of TR Module for 5G Application with a Switchless LNAPA". (Planned to Submit).

Ozkan, T.A. & Guner, A. & Burak, A. & Yazici, M. & Gurbuz, Y. "Electrical Balance Duplexer Based In Band Full Duplex System for 5G Communication Systems". (Planned to Submit)

Burak, A. & Kalyoncu, I. & Yazici, M. & Gurbuz, Y. "A novel asymmetric switch design for 5G Applications". (Planned to submit to the conference).