BIDIRECTIONAL COMMON-PATH FOR 8-TO-24 GHz LOW NOISE SiGe BiCMOS T/R MODULE CORE-CHIP

by
CAN ÇALIŞKAN

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Approved by:

Prof. Yaşar GÜRBÜZ
(Thesis Supervisor) .....

Prof. Erkay SAVAŞ .....

Asst. Prof. Ömer CEYLAN .....

Assoc. Prof. Serkan TOPALOĞLU .....

Asst. Prof. Tufan KARALAR .....

Approval Date: July 19, 2019

ABSTRACT

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CAN ÇALIŞKAN

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Dissertation Supervisor: Prof. Yaşar GÜRBÜZ

Keywords: Transceiver, Bidirectional control, Wideband, Noise figure, BiCMOS integrated circuits.

This thesis is based on the design of an 8-to-24 GHz low noise SiGe BiCMOS Transmitter/Receiver (T/R) Module core-chip in a small area by bidirectional common-path. The next-generation phased array systems require multi-functionality and multi-band operation to form multi-purpose integrated circuits. Wide bandwidth becomes a requirement for the system in various applications, such as electronic warfare, due to leading cheaper and lighter system solutions. Although III-V technologies can satisfy the high-frequency specifications, they are expensive and have a large area. The silicon-based technologies promise high integration capability with low cost, but they sacrifice from the performance to result in desired bandwidth. The presented dissertation targets system and circuit level solutions on the described content. The wideband core-chip utilized a bidirectional common path to surpass the bandwidth limitations. The bidirectionality enhances the bandwidth, noise, gain and area of the transceiver by the removal of the repetitive blocks in the unidirectional common chain. This approach allows succeeding desired bandwidth and compactness without sacrificing from the other high-frequency parameters. The realized core-chip has 31.5 and 32 dB midband gain for the receiver and transmitter respectively, with a + 2.1 dB /GHz of positive slope. Its RMS phase and amplitude errors are lower than 5.6^0 and 0.8 dB, respectively for 4-bit of resolution. The receiver noise figure is lower than 5 dB for the defined bandwidth while dissipating 112 mW of power in a 5.5 mm^2 area. The presented results verify the advantage of the favored architecture and might replace the III-V based counterparts.

ÖZET

8-ile-24 GHz DÜŞÜK GÜRÜLTÜLÜ SiGe BiCMOS V/A MODÜLÜ ÇEKİRDEK ÇİPİ İÇİN İKİ YÖNLÜ ORTAK-HAT

CAN ÇALIŞKAN

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Anahtar Kelimeler: Alıcı/verici, İki-yönlü kontrol, Geniş bant, Gürültü figürü, BiCMOS entegre devreleri.

Bu doktora tezi 8-24 GHz arasında çalışan düşük gürültülü SiGe BiCMOS Verici/Alıcı (V/A) modülü çekirdek çipinin iki yönlü ortak hat kullanımıyla küçük alanda gerçeklenmesine dayanmaktadır. Yeni nesil faz dizili sistemleri çok amaçlı entegre devreler elde etme amacıyla çok fonksiyonluluk ve farklı bantlarda çalışmaya uyumluluk aramaktadır. Geniş bant aralığı, elektronik harp gibi birçok farklı uygulamada daha ucuz ve hafif çözümler önerebildiği için, aranan bir özelliktir. III-V temelli teknolojiler istenilen özellikleri sağlayabilse de maliyetleri yüksek, alanları da büyüktür. Silikon temelli teknolojiler yüksek entegrasyon becerisini düşük maliyetle gösterebilmesinin yanı sıra, istenilen bant aralığını yakalayabilmek için performansından feragat etmektedir. Bu doktora tezi belirtilen kapsamlarda sistem ve devre seviyesi çözümler içermektedir. Gerçeklenen geniş bantlı çekirdek çipi, iki-yönlü ortak hat kullanarak bant aralığını limitini aşmıştır. İki-yönlü sinyal akışı alıcı/vericinin bant genişliğini, gürültüsünü, kazancını ve alanını, tek-yönlü ortak hattındaki tekrarlı alt blok kullanımını engelleyerek, iyileştirmektedir. Belirtilen yaklaşım hedeflenen bant aralığı ve küçük alana, diğer özelliklerinden feragat etmeden başarabilmiştir. Gerçeklenen çekirdek çipi, alıcı/verici hatları için sırasıyla 31.5 dB ve 32 dB'lik bant ortası kazanca, +2.1 dB/GHz'lik pozitif eğimle erişmiştir. 4-bitlik çözünürlüğe sahip çipin RMS faz/genlik hatası sırasıyla 5.6^0 ve 0.8 dB'dir. 5.5 mm^2'lik alanda 112 mW güç tüketen çipin alıcı gürültü faktörü bant boyunca 5 dB'den düşüktür. Gösterilen sonuçlar, tercih edilen mimarinin üstünlüğünü onaylamakta olup, III-V benzerlerinin yerini alabileceğini doğrulamaktadır.

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Aileme...

To my family...

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1. INTRODUCTION

The basic concept of Radio Detection and Ranging (RADAR) was presented as an invention named “Telemobiloscop” in 1904 by Christian Hulsmeyer, but they had started to be widely used as a system during the early years of the World War II. Throughout the years the technology had improved and extended its market beyond military applications, such as the automotive industry, and weather monitoring. Smaller and cheaper RADAR systems can be implemented by the help of improvements in the semiconductor industry, which can lead to a broadened market size (Neuchter 2000).

1.1. Phased Array RADARs

The recent generation RADAR systems are introduced for both commercial and military applications where the phased arrays are one of the basic concepts of them. Compared to single antenna element-based structures, phased arrays utilize several antenna elements that can be controlled properly. Figure 1. 1 demonstrates a basic view of an array-based system. If the phase of each radiating element can be controlled properly, the main beam can be steered from its initial direction electronically. Hence, they can conclude different processes in a short period, which leads to higher data rate, higher tracking-scanning capability and higher functionality (Kopp 2005).

Coherent addition of signals can result in a higher Signal-to-Noise (SNR) ratio for the receiver chain because the noise generated by each element is uncorrelated with the others. A similar mechanism works for the transmitter chain too; each element is controlled to steer the beam, while the signal flow is in the reverse direction. The output power of each element (P_t) is going to add up for the transmitter chain, hence the total

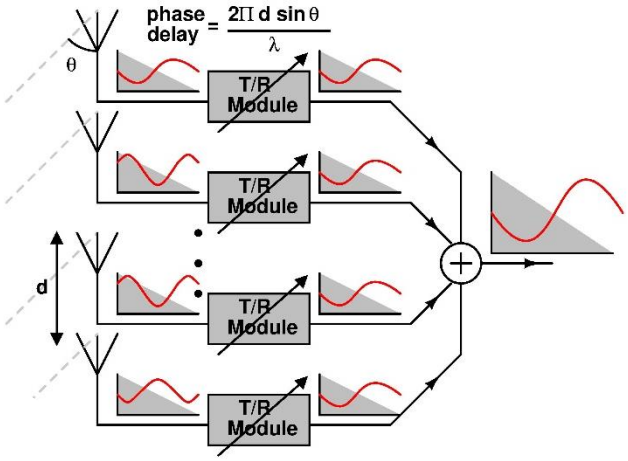


Figure 1. 1 A phased array example with several elements.

$$R_{MAX} = \sqrt[4]{\frac{N^3 P_t G^2 \lambda^2 \sigma}{(4\pi)^3 P_{min}}} \quad (1)$$

output power of the phased array will be "$N*P_t$"; "N" represents the number of elements that exist in the system (Jeon *et al*. 2005). The maximum RADAR range, R_{MAX} in (1), is one of the basic parameters of the system. It defines the maximum distance between the system and an object with a cross-sectional area of σ; P_{min} defines the minimum detectable signal, G stands for transmitting antenna gain and λ is the wavelength of the operating frequency (Balanis 2005). As shown in (1), the range of the system can be improved by increasing the transmitting power. However, this results in higher power dissipation and higher heating rate per element. N is as significant as the other parameters to improve the R_{MAX}. The system performance can be improved by implementing thousands of on-chip T/R modules. This enables multi-functional phased array systems that are lighter, and cheaper compared to earlier generations of RADAR systems.

The phased array systems are categorized considering their feeding and beamforming mechanisms. Fig.1 represents an active phased array, where each element has its amplification, phase, and amplitude control. Passive phased array systems depend on amplification after adding signals of each element. Therefore, passive phased array systems include a single amplification stage, where phase control is done for each chain before the signal formation. Compared to passive ones, active phased arrays have better sensitivity due to including an amplification stage before the phase controlling unit and signal formation. Similarly, the output power of a passive phased array is lower compared

to active counterpart, due to including lossy elements after the transmitter amplifier.

Phase control can be preferred to be done in Intermediate Frequency (IF) to avoid possible high loss of the block in radio frequency (RF), with the expense of increased area. Additionally, mixers and Analog-to-Digital Converters (ADC) can be utilized in a digital beamformer to vary the phase. However, each element should include the mentioned blocks which result in increased power consumption. The summation of all signals before the mixer is named as an All-RF approach, which is suitable for the on-chip application due to having the capability of achieving high RF performance in a small area with a low cost (Çalışkan 2014). Therefore, the T/R modules become one of the most essential blocks for an All-RF based approach because of determining the main RF performances of a phased array system.

1.2. T/R Module

The basic features of a T/R module vary regarding the feeding mechanism of the phased array system. In an All-RF based system, the T/R modules include the Low Noise Amplifier (LNA), Power Amplifier (PA), Single-Pole-Double-Throw (SPDT) switch, Phase Shifter (PS) and Attenuator. LNA is the main amplification block of the receiver (RX), and it is usually preferred as the first block of the chain; it determines the sensitivity of RX by introducing low noise to the system. According to Friis' noise equation presented in (2), a high gain level enables suppression of the noise generated by the incoming blocks. Therefore, succeeding a low noise factor (F) with a high gain is a crucial target for the LNA. PA is the essential amplification block of the transmitter chain (TX). It mainly controls the gain and output power of the chain. Even if they are the main amplification blocks of the specified chains, the expectations from PA are different than LNA because of the aims of the TX, such as output power, linearity, and efficiency. SPDT is the block that is responsible for selecting the appropriate signal path of the module while guaranteeing low path loss and high isolation between chains. PS is the

$$F_T = F_1 + \frac{F_2-1}{G_1} + \frac{F_3-1}{G_1 G_2} + \cdots + \frac{F_N-1}{G_1 G_2 \cdots G_{N-1}} \quad (2)$$

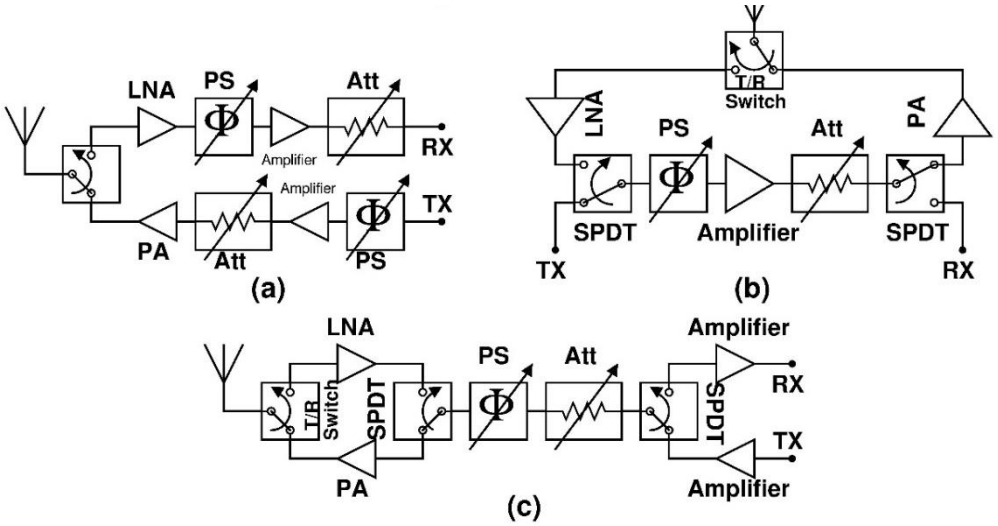


Figure 1. 2 Various T/R module architectures; (a) the separated architecture, (b) the combined path, (c) the bidirectional common-chain.

phase controlling block of the module; its performance is critical for the system since the beam steering is established by varying the phase. Additionally, its gain and dynamic range should be coherent with the remaining sub-blocks. The attenuator can be utilized for different purposes such as beam formation, amplitude adjustment, dynamic range improvements and/or gain error correction that is caused by the PS at various phase states. Some modules may include Variable Gain Amplifier (VGA) instead of an Attenuator or introduce additional amplification blocks considering the loss of passive components. The main idea is to maximize the RF performance of the module and boost the system features without sacrificing the compactness, which is a trade-off for the T/R modules. Hence, different module architectures exist regarding various system expectations as presented in Figure 1. 2.

The RX and TX of a module may require different features, which results in various sub-block requirements. Hence, the transceiver chains can be separated from each other as presented in Figure 1. 2 (a), and it is named as the separated architecture. The duplication of blocks contradicts with the compactness and concludes with increased power consumption, although high RX and TX performances can be achieved. SPDT switches can are introduced as a signal path controller, which can result in architecture as Figure 1. 2 (b). It combines the common blocks of RX and TX. Generally, the common-path or so-called Common-Chain (CC) is consisting of PS, Attenuator, SPDT, and an amplifier. The number of blocks and their features can differ regarding the performance

specifications of the system. As the RF expectations increase, more complex solutions might be required for the blocks in CC. When the total number of blocks and compactness is considered, the approach in Figure 1. 2 (c) is more complicated. It promises a superior performance by utilizing the bidirectionality. As a drawback, it requires new design approaches to satisfy both bidirectionality properties in CC and the system expectations (Bentini et al 2014). Besides its complexity, lower power and smaller T/R modules might be achieved by favoring the bidirectional architecture.

1.2.1. Technologies Preferred for T/R Modules

The technology for on-chip T/R modules can be various because of the strict system requirements. When the RF features are decided to be the primary metric, III-V based semiconductor devices promise the best performance compared to Si-based devices. However, the designs with III-V technologies may consume a large area. Moreover, they have a low yield. Hence, the T/R modules that are designed by utilizing the III-V devices, might oppose the compactness and low-cost specifications of the system, besides of their superior RF performances. For instance, new generation phased arrays may require up to 10^6 modules, where the number of elements might be limited to 10^5 at most when III-V technologies are preferred (Jeon et al. 2005). However high performance can still be required, especially for military applications. The GaN technology is trying to pass the area limits of GaAs by taking advantage of their high-power capabilities. They can eliminate the need for the limiter and additional isolator circuitries in GaAs due to being more resistant to higher power inputs. As a result, GaN technology may promise about %40 area reduction in the front-end part of the system (Rebeiz et al 2017).

The improvements in Si-based technologies lead them to be a candidate for the T/R modules, not because of their high performance, but for their high integration capability and low cost, which may broaden the phased array market towards commercial applications. The T/R modules with Silicon technology can include RF, analog, digital, control circuitries and bias networks in a single die with low power consumption. This leads to reduced power, area, and cost of the system, dramatically. However, their RF performance is not as good as the III-V counterparts; i.e. limited breakdown voltages, so low output power for the Silicon. The recent enhancements in SiGe BiCMOS

Table 1. 1 Comparison of III-V and Si-Based technologies

	(Ommic 2018)	(Northropgrumman 2015)	(Ums-gaas 2018)	(Ommic 2018)	(IHP 2018)	(IHP 2018)
Foundry	Ommic	Northrop Grumman	UMS	Ommic	IHP	IHP
Technology	GaN	GaN	GaN	GaAs	SiGe BiCMOS	SiGe BiCMOS
Emitter Width (Gate Length) [µm]	0.1	0.2	0.25	0.125	0.25	0.13
Collector-Emitter (Drain -Source) Breakdown Voltage (V)	25	28	> 100	6	2.2	1.65
β	-	-	-	-	150	900
G_m **[mS /mm]**	650	350	300	700	-	-
f_t **[GHz]**	110	60	30	150	110	230
f_{max} **[GHz]**	160	200	-	250	180	340

technology enabled its Heterojunction Bipolar Transistor (HBTs) have similar small-signal RF performances compared to III-V devices, without sacrificing high integration capability and low area consumption.

Table 1. 1 compares the basic features of various integrated circuit (IC) technologies. The foundries in the provided tables are not related to each other. III-V based technologies have higher breakdown voltage levels compared to Si-based counterparts, which results in higher output power levels. Similarly, lower noise levels can be achieved by utilizing III-V devices due to having higher carrier mobility. It should be noted that different III-V devices exist that are dedicated to specific applications; the III-V devices that can exceed 300 GHz of transition frequency (f_t) are not included in the presented table for brevity.

1.2.2. Trends in T/R Modules

The recent trends in T/R modules can be classified into two groups; the technological enhancements and the architectural improvements. When the system requirements are considered, the next generation expectations from T/R modules depend on higher performance and more functionality in a small area with a low cost. In this chapter, the recent trends in T/R modules are going to summarized regarding the mentioned contents.

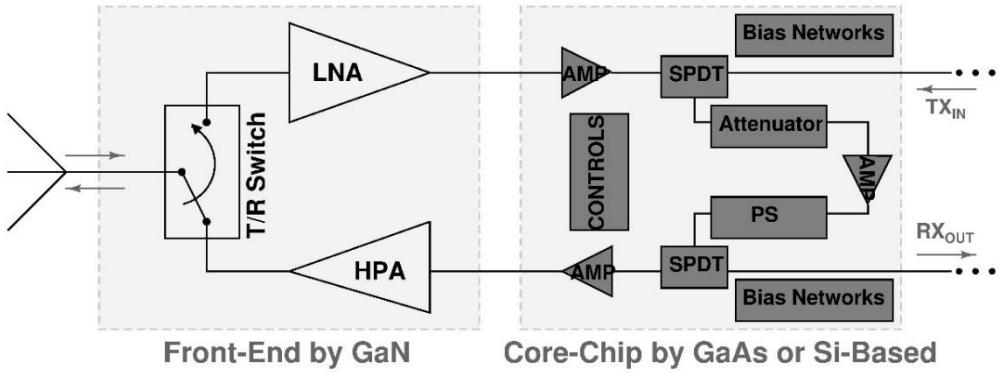


Figure 1. 3 Block diagram of a T/R module with multiple technologies.

The enhancements in the IC technology updated both phased array system expectations and sub-block level requirements, which created different ways to improve the system performance. In the new generation of T/R modules, the superior feature of each technology is used to catch the targets instead of attempting to achieve all system metrics from a single technology. GaN promises the best noise, gain and output power features among others. Hence the front-end part, which is composed of LNA, PA, and SPDT, is devised to be designed by GaN in next-generation T/R modules. When the front-end section is excluded from the module, the remaining part is responsible for the rest of the RF performances and signal formation. This part is called “core-chip” and it can be designed by GaAs technology, because of promising an adequate level of RF performance. In other meaning, GaN and GaAs technology are planned to be utilized together to form a new T/R module generation, as presented in Figure 1. 3 (Bentini et al 2014). Despite that, the improved performance of Si-based devices, especially HBTs, reflects them as being a significant candidate for the core-chip concept because of their high integration capability. Figure 1. 4 (a) and (b) demonstrates the integration of GaAs-based front-end and SiGe BiCMOS based core-chip, while Figure 1. 4 (c) shows a 768-element phased array at X-Band that utilized the described integration (Rebeiz et al 2017). This work validates that SiGe and CMOS technologies can be preferred more in new generation T/R modules.

Besides the technological improvements, improving the resolution of the T/R module is one of the trends for the next-generation systems. The directivity and

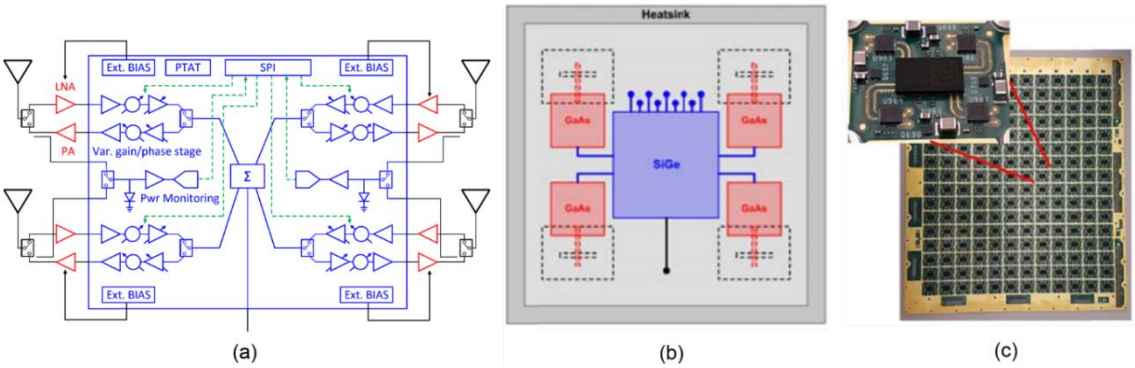


Figure 1. 4 a) Block diagram of core-chip and RF front-end b) SiGe and GaAs chips in the phased array c) X-Band 768-element phased array (Rebeiz et al 2017).

accurate control of the antenna beam are critical parameters for the system because they are defining the detecting and tracking capability of the module. As the phase resolution of the system is improved, higher beam directivity and lower side-lobe levels can be observed. Similarly, high attenuator resolution is required to have more control over the side-lobe levels. This can be achieved by increasing the number of elements in the system, without improving the resolution. However, it would result in an increased area, weight and cost of the system. Hence, an enhanced resolution is a trend in the next generation of modules not only for the sake of higher performance but also to decrease the cost of the system (Mailloux 2005). As a drawback of improved resolution for PS and Attenuator, their loss contribution on the core-chip would be higher. This dramatically lowers the remaining performance of the system, such as gain, sensitivity, and transmitting power.

Treating each chain of the module separately is one of the approaches that is preferred in the next generation of the modules, to overcome the drawbacks of the high phase and amplitude resolution. The phase range of PS is defined as 360^0 because of the periodic behavior of a sinusoidal signal. However, the attenuation range is decided through various specifications. The range of the attenuator might be chosen to correct the amplitude error of the PS while it can be also determined by considering beam tapering. So, its range is not as solid as PS. The increased attenuation range means better beam tapering. However, the attenuator loss gets high as the range increased. This deteriorates the sensitivity of the RX. Therefore, some T/R modules prefer to divide the attenuator into sub-sections. They add the high attenuation bit only to the TX chain to improve the RX features (McQuiddy 1991). The new generation modules may also prefer including the high attenuation bits at the RX instead of TX. Within this way, the RX can still operate

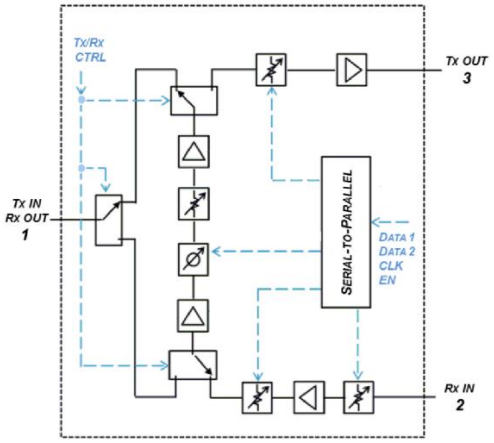


Figure 1. 5 Common-path based core-chip example with separated attenuator range (Bentini et al 2014).

at high input signal levels, without being saturated when the high attenuation bit is activated. However, the NF of the core-chip might be higher because of this approach. The side-effects of the attenuator on RX can be suppressed if the core-chip is cascaded with III-V based front-ends. Besides, it can be told that the range of the attenuator is chosen based on the application. The range and the least significant bit (LSB) of the attenuator are generally defined through binary decimals, but they can be updated regarding the system specifications. Figure 1. 5 presents a common-path based core-chip example, which divided the attenuator into several sub-sections considering the specifications of each chain. An additional attenuation block is placed in CC to tolerate the unexpected errors (Bentini et al 2014). Besides the mentioned updates, the amplifiers in CC do not only compensate for the loss of the path anymore but also add further features such as enhancing the dynamic range or caring the gain flatness to improve the system performance further. However, the described specifications make the amplification blocks more complex due to including contradictory parameters. As a result, the core-chip and the CC become more complicated in the new generation phased array systems.

The next-generation phased array systems tend to satisfy the multiple functionality requirement at a wide frequency range. The goal is to have a single chip that is valid for all applications. This will reduce the total cost due to not requiring additional chipsets for various frequency bands. The systems are desired to generate independent multiple beams at various frequencies, simultaneously (Jeon et al. 2005). Additionally, wideband

performance is also expected for single beam operations or satellite communications, which will decrease unnecessary repetition of designs for different bands (Sayginer 2016). Similarly, it is also a requirement of electronic measure and countermeasure systems; the new generation phased arrays should detect and track multiple objects at the same time, while "hiding" becomes another parameter for the system. For that purpose, frequency and/or beam hopping features are expected to be included in the system as a method for anti-jamming; changing the frequency of operation to a new band can cause a problem for the detection mechanism. The jammer should detect the object by transmitting high power with the highest directivity from a far range. However, if the object decides to change its operating frequency to a new band, the jammer should re-search the object, which will reduce its detection range. Additionally, the object can be hidden from the jammers due to higher path loss at higher frequency (Saarnisaari 2017). Therefore, multi-band operation can be named as one of the major targets of the new generation of T/R modules. When the integration capabilities of IC technologies are considered, the SiGe and CMOS can be preferred for RF and digital beamforming phased arrays, which can broaden their market towards commercial applications. However, Si-based technologies have limited bandwidth due to including passive structures with low Q-factors. Hence, multi-band operation is remaining as a major challenge for silicon technologies.

1.3. Positively Sloped X-Band Core-Chip

As a member of Prof. Yaşar Gürbüz's SÜMER group, I was involved in a transceiver project and designed a positively sloped 6-bit T/R module core-chip for X-Band phased array applications by utilizing IHP Microelectronics' 0.25 μm SiGe BiCMOS technology. The core-chip favored an unidirectional common-chain, where the signal direction is determined by proper switching between RX and TX chains. It includes active equalizer amplifiers to tolerate the high loss by introducing a linearly increasing gain over the defined frequency range. 6-bit phase and amplitude resolutions are achieved by utilizing vector-sum type PS, T-and-π type attenuator, respectively. The X-Band core-chip is submitted to the journal of "Transactions on Circuits and Systems: Regular Papers" and it is under revision. In this section the core-chip, its sub-blocks, and the

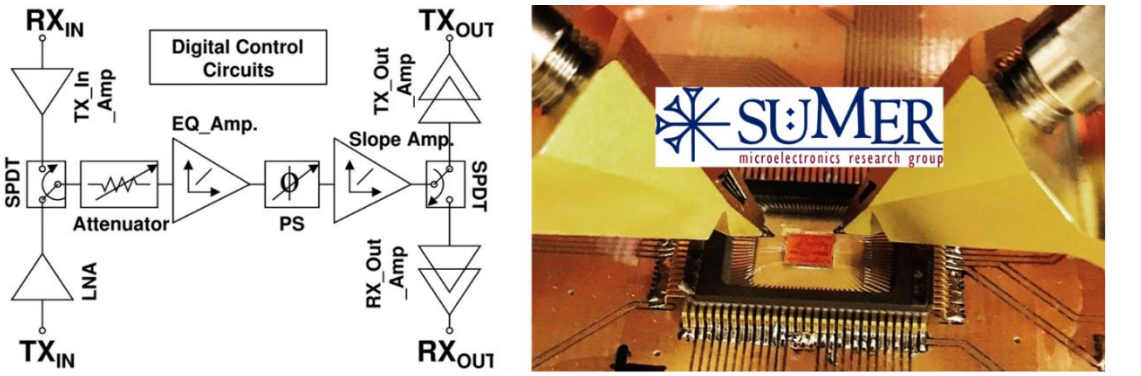


Figure 1. 6 The block diagram and the top-view of the measured positively sloped X-Band 6-bit core-chip.

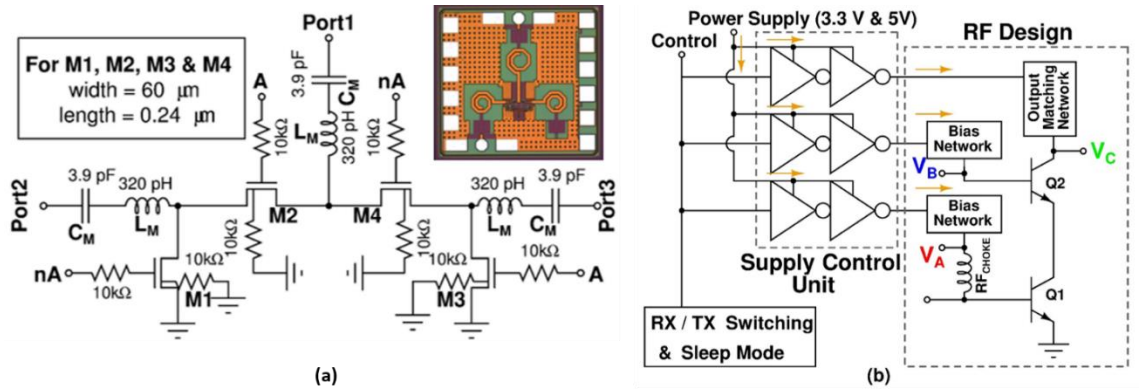


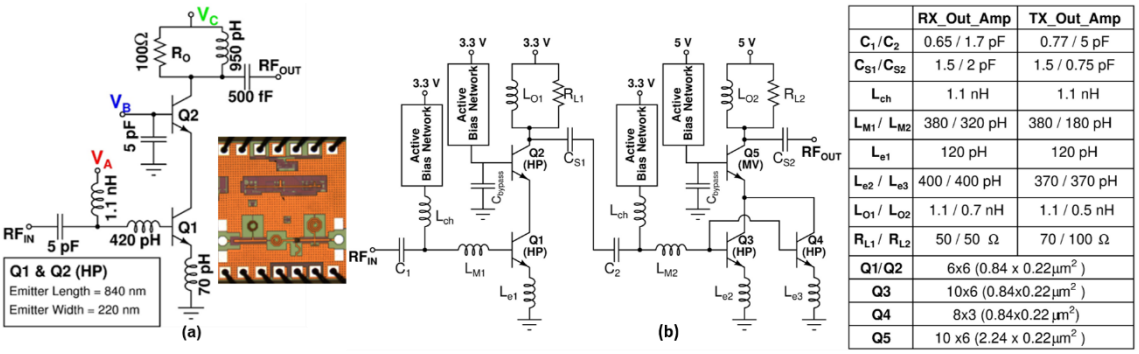
Figure 1. 7 (a) The block diagram of the SPDT switch. (b) The block diagram of the SCU with a basic amplifier.

measurement results are presented; the block-diagram and top view of the core-chip are presented in Figure 1. 6; it covers 18.61 (4.465 x 4.169) mm^2 of area.

1.3.1. The Sub-Blocks of the Positively Sloped X-Band Core-Chip

The measured X-Band SiGe BiCMOS core-chip aimed high phase resolution which might have side-effects such as low gain, narrow bandwidth, high NF, and limited dynamic range. The high resolution also leads to a negatively sloped loss, which results in sharp gain drops and limits the 3-dB BW of the system. Hence, each of the sub-block in the core-chip is designed by considering their gain characteristics.

The SPDT switches are responsible for determining the signal direction of the design. The series-shunt topology is preferred shown in Figure 1. 7 (a), due to its



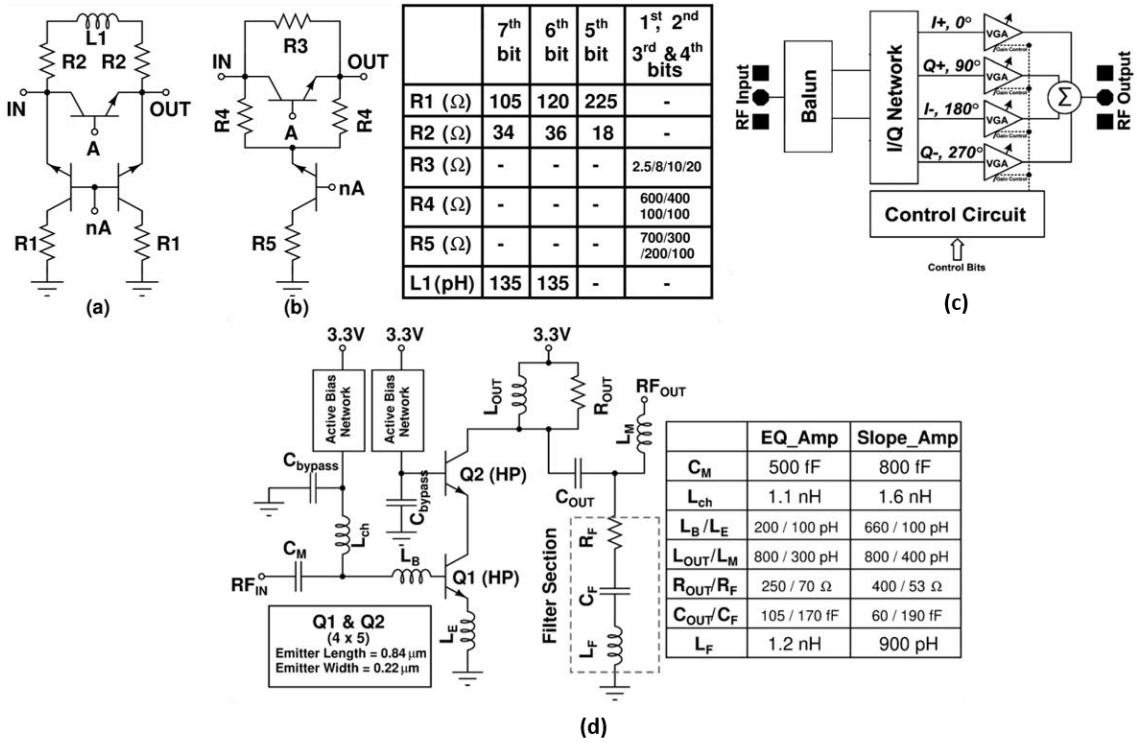
	RX_Out_Amp	TX_Out_Amp
C_1/C_2	0.65 / 1.7 pF	0.77 / 5 pF
C_{S1}/C_{S2}	1.5 / 2 pF	1.5 / 0.75 pF
L_{ch}	1.1 nH	1.1 nH
L_{M1} / L_{M2}	380 / 320 pH	380 / 180 pH
L_{e1}	120 pH	120 pH
L_{e2} / L_{e3}	400 / 400 pH	370 / 370 pH
L_{O1} / L_{O2}	1.1 / 0.7 nH	1.1 / 0.5 nH
R_{L1} / R_{L2}	50 / 50 Ω	70 / 100 Ω
Q1/Q2	6x6 (0.84 x 0.22μm^2)	
Q3	10x6 (0.84x0.22μm^2)	
Q4	8x3 (0.84x0.22 μm^2)	
Q5	10 x6 (2.24 x 0.22μm^2)	

Figure 1. 8 The schematics of (a) the amplifier at the input of the TX, (b) the amplifiers at the outputs of RX and TX.

simplicity, compactness and zero-power consumption. The signal is controlled by switching the isolated-NMOS (iNMOS) transistors on-and-off properly, where the device sizes are decided by considering the loss of the signal path (Ozeren et al 2016). Different than the conventional approach, small-sized devices are preferred to minimize the capacitive parasitic effects.

The core-chip is designed considering a half-duplex system. Therefore, some of the amplification stages might be unused, when a chain is selected; i.e. TX amplifiers will still dissipate power even if the RX chain is chosen. To prevent unnecessary power consumption, the control bits of the SPDT switches are synchronized with supply controller units (SCU). They are composed of buffer networks and connected to the bias nodes of an amplification stage. Figure 1. 7 (b) presents a basic block diagram of an SCU utilized within an amplification stage.

The core-chip includes multiple amplification stages to succeed in the desired level of gain and output power. Each signal path includes two separate amplifiers, which are placed at the input and output of the chain; i.e. an LNA and a high dynamic range amplifier for the RX chain. The amplifiers utilized in the inputs of the RX and TX chains, preferred single-stage amplification, while two-stage cascode amplifier topology is favored for the output amplifiers, to achieve the desired gain. The cascode topology is favored in all amplifiers, because of its high stability. The LNA includes a bypass mode to improve its dynamic range (Turkmen 2018). The schematic view of the TX input amplifier and output amplifiers are shown in Figure 1. 8.



	7th bit	6th bit	5th bit	1st, 2nd 3rd & 4th bits
R1 (Ω)	105	120	225	-
R2 (Ω)	34	36	18	-
R3 (Ω)	-	-	-	2.5/8/10/20
R4 (Ω)	-	-	-	600/400 100/100
R5 (Ω)	-	-	-	700/300 /200/100
L1(pH)	135	135	-	-

	EQ_Amp	Slope_Amp
C_M	500 fF	800 fF
L_{ch}	1.1 nH	1.6 nH
L_B/L_E	200 / 100 pH	660 / 100 pH
L_{OUT}/L_M	800 / 300 pH	800 / 400 pH
R_{OUT}/R_F	250 / 70 Ω	400 / 53 Ω
C_{OUT}/C_F	105 / 170 fF	60 / 190 fF
L_F	1.2 nH	900 pH

Figure 1. 9 The block diagrams of (a) π-type attenuator bit, (b) T-type attenuator bit, (c) PS, (d) the *EQ_Amp* and *Slope_Amp*.

The amplitude of the core-chip is controlled by the T-and-π type attenuator sections as in Figure 1. 9 (a) and (b), where the networks are switched by HBTs. The bits include phase compensation inductors (Davulcu 2016), to tolerate the phase error between attenuation steps. An additional bit (7th bit - 0.25 dB) is added to the attenuator for tuning purposes. The phase control of the core-chip is done by an active phase shifter. It generates four orthonormal reference vectors (*I*± and *Q*±) by utilizing a transformer and second-order polyphase filter. They are cascaded with four VGAs to control the amplitude of the I/Q vectors as shown in Figure 1. 9 (c) (Cetindogan 2017). The phase and amplitude of the core-chip can be controlled both by parallel pads and an integrated SPI controller.

The described sub-blocks have negatively sloped gain characteristics, which limits the operating bandwidth of the system. Therefore, two separate amplifiers are introduced to the CC of the X-Band core-chip to tolerate the gain fall; one of the amplifiers (*EQ_Amp*) is responsible to balance the gain drop of the sub-blocks, where the second amplifier (*Slope_Amp*) determines the final gain characteristic. The difference between

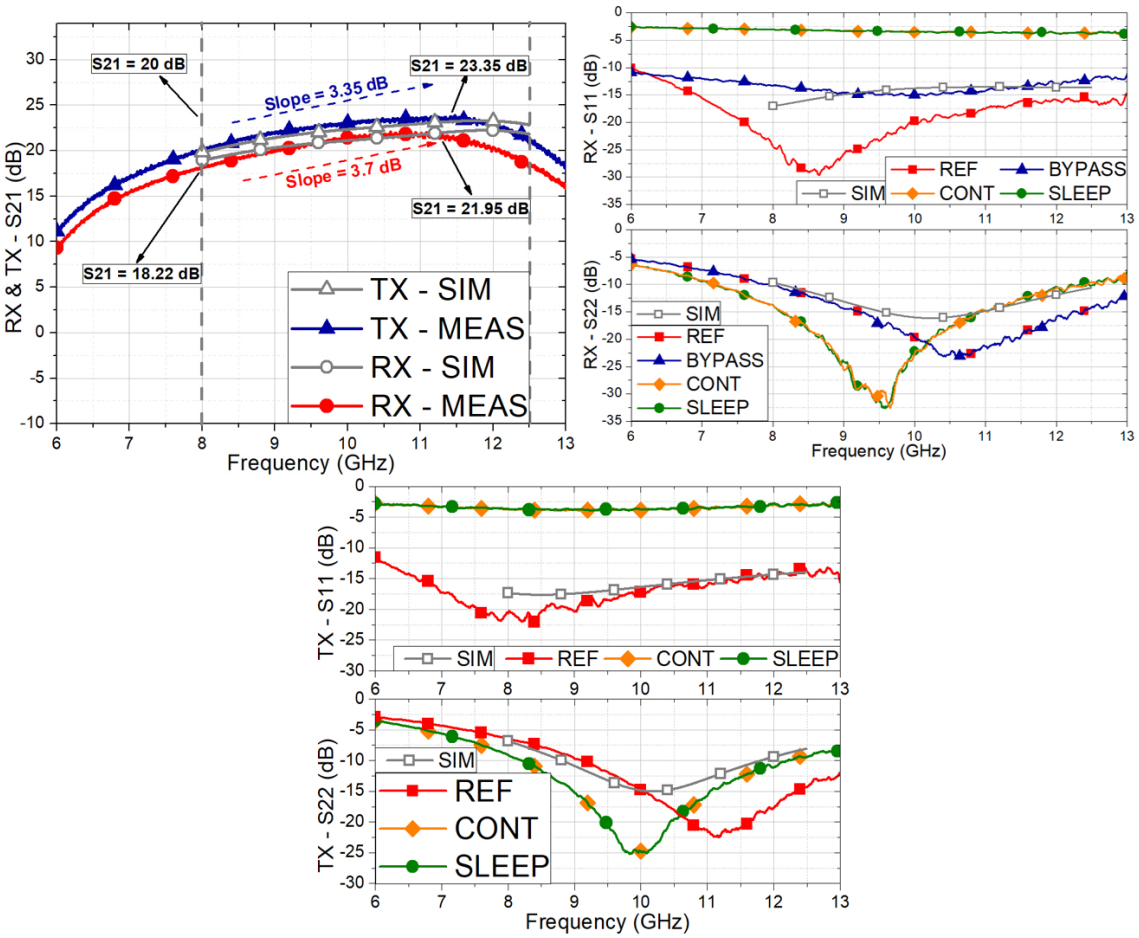


Figure 1. 10 The measured S-parameters of the X-Band core-chip for RX and TX.

these amplifiers is their gain slopes. The amplifiers combine cascode amplifier topology with a filter network as in Figure 1. 9 (d), to succeed a positively sloped gain in a compact area. The *EQ_Amp* is accepted as a letter in "Transactions on Circuits and Systems II: Express Briefs". The detailed information about the *EQ_Amp* can be founded in (Çalışkan 2019). The remaining non-linear gain-slope behavior is neutralized by the passive equalizers that are designed for each chain specifically.

1.3.2. The Measurements of the Positively Sloped X-Band Core-Chip

The gain and impedance matching performances are summarized in Figure 1. 10. The core-chip has 22-and-23.35 dB of peak gains with + 3.7 dB/GHz and + 3.35 dB/GHz of slopes achieved for RX and TX chains, respectively. Additionally, the core-chip presented a linear gain characteristic between 6-to-12.5 GHz with an adequate level of

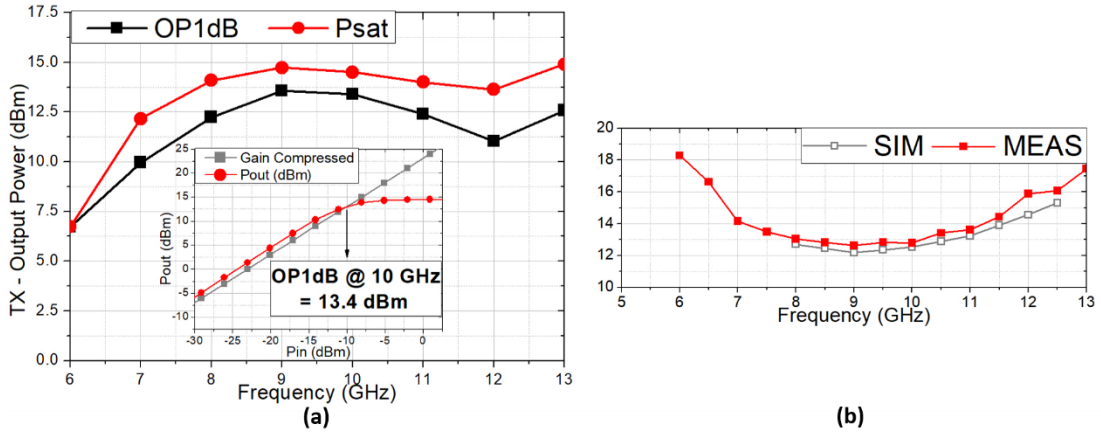


Figure 1. 11 The measured (a) OP1dB of the TX, (b) NF of the RX.

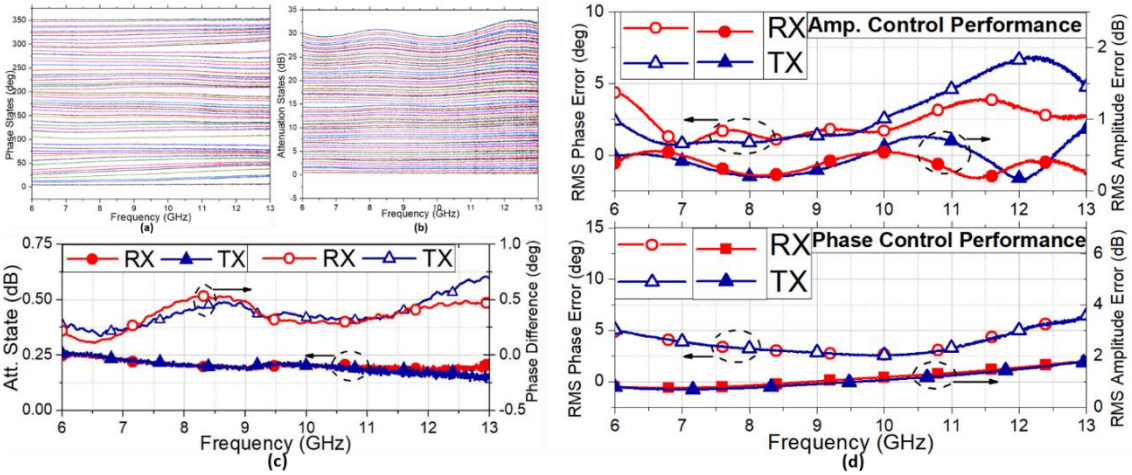


Figure 1. 12 The measured (a) phase states, (b) attenuation states, (c) optional attenuation bit, and (d) RMS phae and amplitude errors of the core-chip.

impedance termination throughout the defined bandwidth. The RX has a measured NF of 12.8 dB, while the TX has 13.4 dBm of output-referred compression point (OP1dB) as shown in Figure 1. 11.

The core-chip has a 6-bit of phase and amplitude resolution, and it states are shown in Figure 1. 12 (a) and (b). The performance of the optional 7th bit of the attenuator is shown in Figure 1. 12 (c). The root-mean-square (RMS) phase and amplitude errors of the core-chip are 2.6^0 and 0.25 dB, respectively, which are presented in Figure 1. 12 (d). During small-signal operation, the X-Band core-chip dissipates 411 and 400 mW of power during RX and TX modes, respectively. To the best of my knowledge, the presented work is the first SiGe BiCMOS core-chip that achieved a positively sloped high gain with a 6-bit phase and amplitude resolution. Among similar works in literature,

Table 1. 2 Comparison of X-Band core-chip with similar works

	(Heijningen 2006) *	(M/A-COM 2010)	(Sim et al 2015)	(Gharibdoust et al 2012)	(Sim et al 2013) *	(Jeong et al 2013)	(Carosi et al 2009)	(Cao et al 2017)	(Lohmiller et al 2017)	(Liu et al 2016)	**This Work**
Tech.	0.25 µm GaAs	GaAs	0.13 µm CMOS	0.18 µm CMOS	0.13 µm CMOS	0.25 µm SiGe	0.25 µm SiGe	0.25 µm SiGe	0.25 µm SiGe	0.13 µm SiGe	0.25 µm SiGe
Freq. [GHz]	8.5 - 11.5	8.5 - 11	9 - 10	8.5 - 10	8.5 - 10.5	8 - 11	9 - 10.5	8 - 10	8 - 12	9 - 11	8 - 12
RX/TX Gain [dB]	27 / -	21 / 19	9 / 12	12 / 12	3.5 /3.5	20 / 30	17 / 17	11 / 15	17.7 / 17.8	25 / 22	21.95 / 23.35
Gain Slope [dB/GHz]	Flat	± 1	Flat	± 2	- 1.5	- 8	± 4	± 1	± 1	-4	+ 3.7 / + 3.35
# of bits PS/Att.	6 / 5	6 / 5	6 / 5	6 / 5	6 / 5	5 / 5	5 / 5	3 / -	6 / 6	5 / -	6 / 7
RMS Phase /Amp. Error [^{0}/dB]	5^0 / -	1.5^0 / 0.3	2.3^0 / 0.4	2.3^0 / 0.25	2.3^0 / 0.3	2.3^0 / 1.5	2.3^0 / 1	2.3^0 / 3	2.3^0 / 0.25	2.3^0 / -	2.6^0 / 0.25
RX / TX OP1dB [dBm]	13 / 19	17.5 / 23.5	- / 11	11 / 11.5	6.5 / 6.5	- / 18	- / 12	-14 / 13	-3 / 13	6 / 28	11.7 / 13.4
RX NF [dB]	2.5	5.2	-	8.5	7.5	9	10	3.5	9.8	3	12.8
RX / TX DC Power Diss. [mW]	-	2100	800 / 800	670 / 640	150 / 150	1500 / 1500	800 / 800	25 / 150	330 / 790	352 /4128†	411 / 400
Area [mm^2]	20	-	2.8	12.8	1.2	8.4	15.99	12	9	15.6	18.61

*Multifunctional Chip. † Power dissipation at OP1dB point.

the X-band core-chip has the highest functionality and high RF performance without sacrificing from power consumption. The performance of the described positively sloped X-Band core chip is summarized in Table 1. 2.

The X-Band core-chip achieved remarkable performances among Si-based designs, but it covers close to 19 mm^2 of area. Additionally, the RX NF is measured as 12.8 dB minimum, although it achieved more than 20 dB of gain for both chains. As mentioned, the GaN and GaAs technologies promise high output power, while smaller area and lower power consumption can be achieved by Si-based designs. Moreover, small-signal gains of the amplifiers are close to each other regardless of the technology. However, III-V devices conclude with lower RX noise figure (NF), even they utilized a similar CC to the Si-based modules. This leads to cascading SiGe based core-chips with an III-V based front-end blocks to satisfy the requirements. Besides its drawbacks and single band of operation, the X-Band core-chip achieved remarkable RF performance among the other SiGe core-chips. The designed X-Band core-chips' RF performance, its weaknesses, and technological limitations become motivation sources of the presented dissertation.

1.4. The Challenges and Limitations of the SiGe Core-Chip

The next-generation phased array systems expect better RF performances without sacrificing the basic requirements such as the integration capability, area, and cost. Recently, different core-chips are presented for various applications, but they have sacrificed from some of these parameters. For instance, some core-chips with high phase and amplitude resolution have sacrificed NF and output power. Additionally, they concluded with higher power consumption and a large area. The Si-based core-chips can follow the recent trends in phased array core-chips to some extent. However, their BW is limited, even the NF, output power and total area are sacrificed. It is because of the increased complexity of the chains and technological limitations. The operating frequency of both HBT and CMOS transistors can be improved throughout the years. However, their breakdown voltages are going to be reduced, which will reflect as lower output power for the core-chip. Additionally, the on-chip inductors in silicon have low Q-factor due to having a conductive substrate. This is another restriction for the operating bandwidth of Si-based designs. Moreover, the bandwidth of the III-V technologies is wider, because of their high quality factor (Q-factor) of the passive devices, which results in low loss and wide operational bandwidth. Moreover, the area of the Si-based core-chips might not shrink much after the technological enhancements due to being mainly defined by the size of the inductors (Hansen 2003). In summary, achieving a multi-band core-chip with a low NF in a small area is remaining as a significant challenge for the Si-based technologies to reach the next generation trends in phased array systems.

2. 8-to-24 GHz LOW NOISE SiGe BiCMOS BIDIRECTIONAL CORE-CHIP

In this thesis, a wideband SiGe BiCMOS T/R module core-chip design is realized. It is aiming to surpass the bandwidth limitations of the next generation phased array systems by utilizing a bidirectional common-path. The preferred architecture, its sub-block measurements, and post-layout simulations are explained throughout this chapter.

The T/R module core-chip architecture that targets 8-to-24 band of operational bandwidth in 0.13 µm SiGe BiCMOS technology, is presented in Figure 2. 1. The core-chip aimed low NF, a positively sloped high gain and low power consumption in a compact area by favoring a bidirectional signal path. The goal is to achieve similar RF performances with III-V counterparts from the X-to-K band. The unidirectional approach may require several sub-blocks in CC that can increase power consumption, total area and especially the dependency on frequency. Hence, the bidirectional signal path is preferred to reduce the mentioned parameters at the expense of the raised complexity. The core-chip is consuming 112 mW of power and achieved about 31.5 dB and 32 dB of midband gain for RX and TX, respectively. If a conventional core-chip is planned to be cascaded with III-V based RF front-ends, the system may suffer from a high negative slope. Therefore, the realized multi-band core-chip targeted a + 2.1 dB/GHz gain slope throughout the defined bandwidth, to conclude with a flat gain for the system. Within this way, the 3-dB gain-bandwidth the phased array system would be improved. The design has lower than 5 dB NF for RX while targeting 4-bit of resolution. The attenuation range is 30 dB. 6 ± 2.5 dBm of output-referred compression point (OP1dB) is obtained from the TX throughout the BW. Higher output power levels might be achieved by sacrificing the BW. The core-chip depends on a half-duplex system. Therefore, the design includes proper switching and power supply circuitries that enable on-off states regarding the selected chain in a 5.5 mm^2 area.

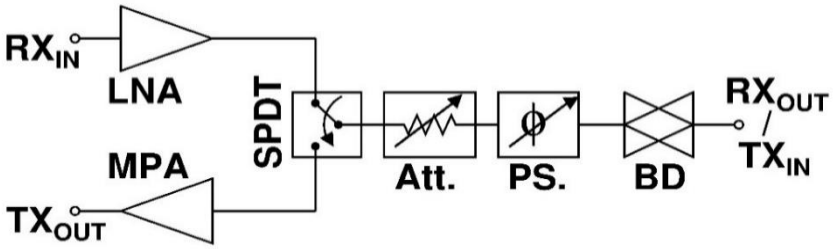


Figure 2. 1 Block diagram of the 8-to-24 GHz SiGe BiCMOS T/R module core-chip.

Table 2. 1 Comparison of Wideband T/R modules with various technologies

	(Bentini 2014)	(Jeong 2018) *	(Sim et al 2015)	(Sim et al 2013)*	(Cho et al 2014) *	(Sayginer et al 2016)	**This Work**
Technology	0.18 µm GaAs	0.25 µm GaAs	0.13 µm CMOS	0.13 µm CMOS	0.13 µm CMOS	0.13 µm SiGe	0.13 µm SiGe
Architecture	Common - Path	Bidirect.	Bidirect.	Bidirect.	Bidirect.	Receiver Only	Bidirect.
Freq. [GHz]	6 - 18	6 - 18	9 - 10	8.5 - 10.5	8 - 16	2 - 16	8 - 24
# of channels	1	1	4	1	1	2 / 4 / 8	1
RX/TX Gain [dB] (avg.)	21 / 18	11	12 / 9	3.5 / 3.5	-1 /-1	9	**31.5 / 32**
Phase Range	360^0	255 psec.**	360^0	360^0	198. 4 psec**	360^0	360^0
Att. Range [dB]	> 40	23.75	31	31	31.5	-	30
Phase & Att. Resolution (bit)	4 / 5	8 / 7	6 / 5	6 / 5	7 / 6	5 / -	4 / 4
RMS phase / att. Error	13^0 / 0.8	1.7 psec / 1	2.3^0 / 0.4	4.3^0 / 0.3	1.56 psec / -	< 8.5^0 / 1	5.6^0 / 0.8
NF @ RX [dB]	8	18	-	7.5	-	11.9	< 5
OP1dB @ TX [dBm]	17	16.5	11	6.5	-	-7	6
Power con. (W)	- / 1.25	1.6	0.8	0.15	0.28	0.25	0.112
Area [mm^2]	25.8	20	11	1.2	3.9	5	5.5

*: Multifunctional chip, instead of Core-Chip. **: Utilized TTD, not PS.

Table 2. 1 compares some wideband and bidirectional core-chip examples in the literature, with the realized wideband design. (Jeong et al 2018) and (Cho et al 2014) are bidirectional designs. However, they do not include RF front-end blocks, such as LNA, PA (or Medium Power Amplifier - MPA for the core-chip) and SPDT. Moreover, they include True Time Delay (TTD) instead of PS. (Sayginer 2016) presents a programmable phased array receiver that can generate multiple beams, simultaneously. (Sim et al 2015) and (Sim et al 2013) are utilizing a bidirectional signal path. However, both designs are suffering from narrow bandwidth. The core-chip in this dissertation aimed to exceed the presented frequency and performance limitations of the Si-based technology. The design targets various metrics that are contradicting each other. Hence, the wideband core-chip is realized by considering a priority list. The area and power consumption are sacrificed for some blocks to success the desired band of operation, gain, and NF.

The wideband core-chip includes an SPDT switch that selects the appropriate signal path, as in Figure 2.1. The switch is designed by considering the compactness and wideband expectations of the core-chip. Additionally, it should provide an adequate level of isolation between LNA and MPA, to block any possible signal leakage. The front-end blocks should be turned on-and-off coherently with the SPDT, to prevent unnecessary power dissipation in the half-duplex core-chip. Similarly, the signal direction of the CC should be updated regarding the control signal of the SPDT. The described control mechanism is enabled by integrated supply control units (SCU) that are introduced to each of the amplifiers.

The Bidirectional Amplifier (BDA) is one of the crucial blocks of the presented wideband core-chip, due to providing amplification in a bidirectional way. It decreases the number of blocks in the core-chip and tolerates the loss of the CC. Moreover, it is responsible for the design's positively sloped gain. The BDA achieved these targets with low power consumption in a compact area.

LNA and MPA are the two front-end amplification blocks of the core-chip. LNA is the amplifier that dominates the gain and NF of the RX, while the MPA determines the gain and output power of the TX. The prior aim of both amplifiers is to have a wide BW. The MPA has similar specifications with the LNA except for the output power, which should not differ much over the frequency. The impedance at the output terminal affects the maximum output power of an amplifier. However, the impedance for maximum output power may not be 50 Ω, which creates a trade-off between proper impedance matching and output power. Additionally, the SiGe-based MPA cannot reach the output power levels of a GaN PA, due to its breakdown limitations. The TX of the core-chip can be cascaded with an III-V based PA to satisfy the system requirements. Hence, the MPA is designed by considering its compatibility with a GaN PA.

The amplitude and phase control of the wideband core-chip is enabled by the attenuator and PS, respectively. They are in the CC of the core-chip. Hence, they should be compatible with the bidirectional signal path as the BDA. The wideband core-chip has a 4-bit of amplitude and phase resolution. The control of those blocks is enabled by the help of integrated digital circuitries. The results show that the core-chip can target for higher resolution.

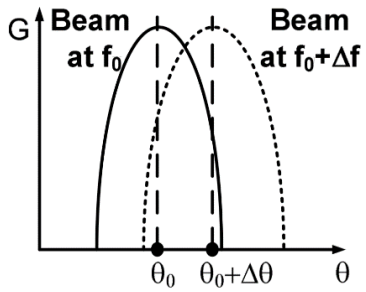


Figure 2. 2 An antenna pattern representation including the effect of beam squint (Garakoui et al 2011).

The design includes a phase shifter, which has a narrow instantaneous bandwidth. Some applications that target multi-band of operation, such as modules for jamming, utilize TTD block instead of a PS, due to the phenomena called “beam squint”. The variation of the antenna beam direction as the frequency changes is called beam squint, which is limiting the bandwidth of the system as demonstrated in Figure 2. 2 (Garakoui et al 2011). The phased arrays that are targeting narrowband applications can utilize PS in their system. A wideband PS might be required for a narrowband system that is aiming to operate at a wide frequency range (Chu et al 2011). The TTD elements can provide a wide instantaneous bandwidth where the design of a wideband PS would not support the defined condition. Ideally, the PS has a constant phase characteristic over the frequency. On the other hand, TTD elements introduce constant time delay versus frequency. Therefore, they have a low beam squint during beam steering, which enables wideband arrays (ChoJeong et al 2014). This reflects a delay specification instead of phase for some core-chip application, as shown in Table 2.1.

Si-based technologies have some difficulties with implementing TTD, due to including multiple switches and limited Q-factor of the passives. Additionally, transmission line-based TTDs can consume large areas and have limited delay range. The artificial transmission lines can succeed in higher delay ranges at the expense of limited bandwidth. However, the applications such as jammers require high TTD resolution, delay range and output power as presented in (Jeong et al 2018). The III-V technology can provide passives with high Q-factor and lower switching losses that can conclude a high delay ranged wideband TTD elements, with the expense of cost and area. Therefore, the wideband core-chip depends on the phase shift instead of the time delay. Besides, the core-chip blocks are designed by considering their group delay (GD) flatness, and relative

time delay variations to demonstrate its compatibility with the time-delay systems.

This thesis realized an X-to-K band T/R module core-chip in SiGe BiCMOS technology that can be utilized in wideband phased array applications. To the best of my knowledge, multi-band T/R module core-chip that covers X, Ku and K band in SiGe BiCMOS technology has not been reported in the literature. It presents close to 30 dB of midband gain for both RX and TX, 4-bit phase and amplitude resolution for both chains and maximum 5 dB RX NF with a 16 GHz of bandwidth, which is not demonstrated in SiGe technology before. Additionally, the core-chip is consuming 112 mW of power in a 5.5 mm^2 area. Therefore, it can lead to cheaper and more compact phased array systems.

2.1. Passive Components in the Core-Chip

The wideband core-chip is designed by regarding 8-to-24 GHz of bandwidth. This is equal to 100% of fractional BW when the 16 GHz is selected as the center frequency. The extremely wide bandwidth expectation requires new passive component design approaches to validate the ideal schematic design results. The technology offers seven (five thin and two thick) metal layers, and a Metal-Insulator-Metal (MIM) capacitor with a high quality factor (Q-factor). MIM capacitor's bottom connection is at Metal 5 for a lower shunt parasitic capacitance, where the upper metal is contacted by Top Metal-1. It is modeled by the technology provider. The process features are introduced to the electromagnetic (EM) simulators and the lumped components, except resistors, are simulated with the surrounding components (inductors, ground layers, etc.) for verification and higher accuracy. The DC blocking capacitors are critical for the sub-blocks. They might act as an RF component at the lower end of the bandwidth if small values are preferred. At the same time, large DC blocking capacitors' shunt parasitic would affect the high-frequency behavior of the core-chip dramatically. To avoid the mentioned problems, the small-sized series matching capacitors are utilized to prevent any unnecessary addition of DC blocking capacitors. This concern is also addressed in the following sections.

The two top metal layers are dedicated to inductors, which are custom-designed in

SONNET and ADS Momentum. The area of a block (also the core-chip) is mainly determined by the sizes and the number of the inductors. Therefore, their values, layouts, and box sizes are as significant as their Q-factor. It should be noted that adequate separation between inductors is required, to prevent mutual coupling between them. This limits the smallest area that can be achieved from a single block. Similarly, the floorplan of the core-chip should be done by considering the coupling between blocks. Therefore, the compactness of the sub-blocks and core-chip is limited.

The Q-factor of an inductor defines the loss of the component, which can emphasize both capacitive and resistive effects. The top metal layers of the technology provide higher conductivity and lower shunt parasitic, due to being thick and being away from the substrate. Figure 2. 3 (a) demonstrates a 1 nH of an inductor that is designed in SONNET. The top metal width is chosen as 10 µm to minimize the resistive parasitic effects, while the distance between metals is selected as 5 µm to have small fringe capacitance between metal layers. The box size is determined by preferring 40 µm distance from the inductor sides, which is 0.066 mm^2. As shown in Figure 2. 4 (a) the presented design has about 1 nH inductance, but it varies at about 0.4 nH between 8 GHz and 24 GHz. This is a significant problem for the wide bandwidth target. The inductors should provide a flat response to achieve the desired performance from the blocks. Hence, the top metal width can be reduced to minimize the substrate coupling, which is also going to shrink the box size. For that purpose, the top metal thickness can be decreased to 2 µm, the minimum value the technology can provide. This concludes with a high series parasitic resistance, so increased loss.

The realized wideband core-chip considers different inductor designs to both enhance their flatness over frequency and shrink their size. Figure 2. 3 (b) demonstrates one of the approaches that can be applied to shrink the size of the inductor. The inductor utilized two top metal layers for a spiral design and connect them in a parallel manner to decrease its parasitic resistance. The described method can give rise to smaller inductors by minimizing the drawbacks of the 2 µm metal thickness. After EM simulations, the inductance variation between 8-to-24 GHz is founded as 0.3 nH, even if the parallel top metals introduce shunt and mutual fringe capacitance. Additionally, the total box size is 63% lower than the initial case, as shown in Figure 2. 3 (a). As a third method, the top

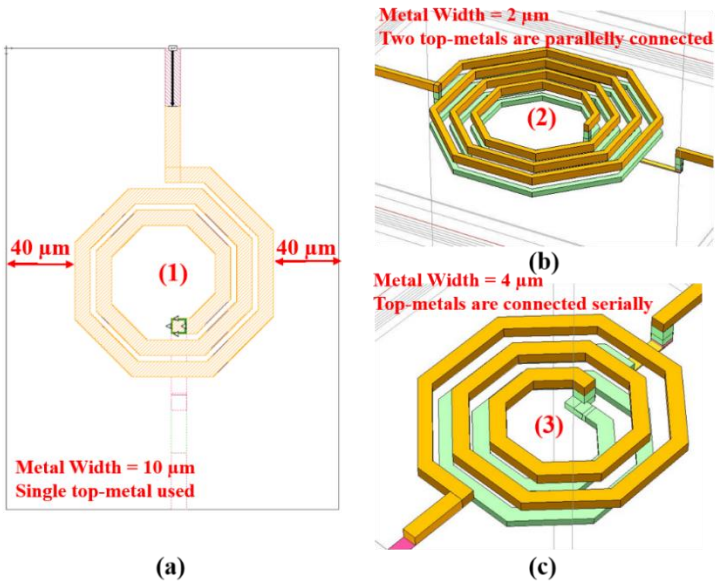


Figure 2. 3 Three different inductor designs; a) single top metal with 10 µm thickness b) two top metals parallelly connected c) two top metals serially connected.

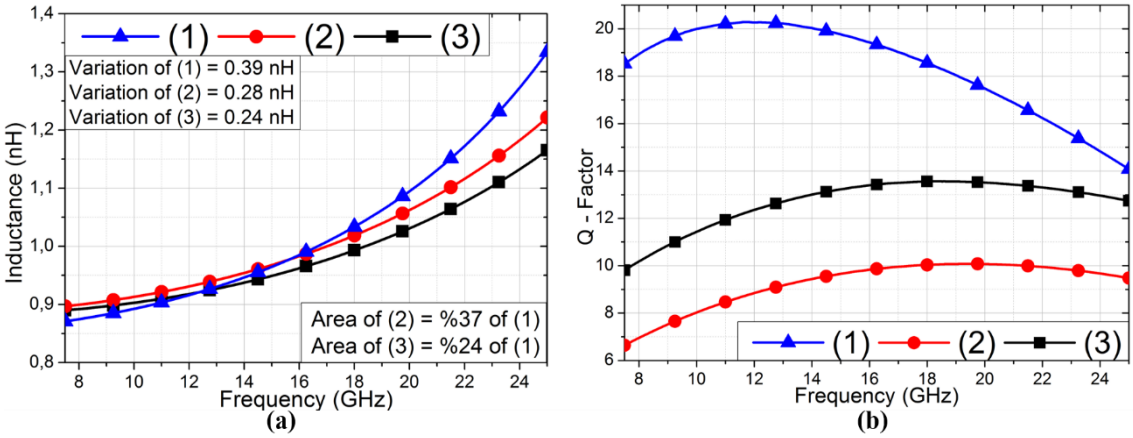


Figure 2. 4 Comparison of different inductor designs; a) Inductance variation and total box size variation b) Q-factor comparison of three inductors.

metals can be connected in series to form a smaller inductor, as presented in Figure 2. 3 (c). Compared to a parallelly connected case, the metal thickness is doubled to balance the increased series parasitic resistance. Serially connecting the top metals resulted in an improved Q-factor and inductance flatness, which is 0.24 nH. Moreover, when the case (1) is considered, the serially connected top metals concluded in about 75% smaller box size. The Q-factors of the three inductors are shown in Figure 2. 4 (b).

Inductors may have different purposes and their specifications may vary. So the utilization of two top metal layers in series or parallel would not be the best cases. For

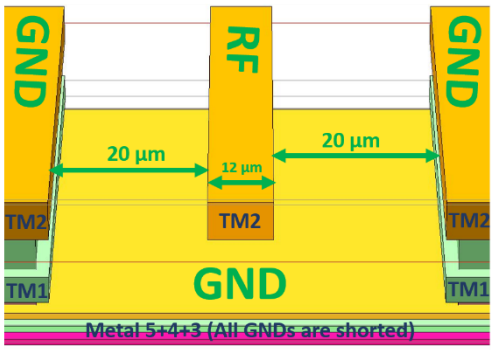


Figure 2. 5 The cross-section of the guided microstrip transmission line.

instance, the inductors that are series to the signal path can require high Q-factor with low series resistance. Therefore, the blocks of core-chip include inductors as small as possible by using two described approaches, if they do not contradict with the block specifications.

The transmission lines utilized in the core-chip should be also considered carefully since their effect would change the frequency behavior of the design. To avoid any interference from nearby components or blocks, the guided microstrip lines are preferred throughout the design, as shown in Figure 2. 5. The ground layers are placed 20 µm away from the signal line, which is at Top Metal 2; a large gap to consider the line as a coplanar waveguide. Normally, the return path of a microstrip line is preferred to be away from the RF line, to decrease the shunt parasitic capacitance. However, the wideband core-chip has a compact area and includes several bias networks, digital controls, and electrostatic discharge (ESD) protection lines. Therefore, preferring Metal-1 as the microstrip transmission line's return path would result in routing problems. Additionally, the ground distribution is a significant concern of the core-chip. Any parasitic at ground terminations would affect the high-frequency performance dramatically. As a result, it would be beneficial to dedicate multiple metal layers for ground terminations. Regarding the mentioned concerns, Metal-1 and Metal-2 are dedicated to bias networks, their routings, digital control, and ESD protection lines' routing, while Metal-3, 4 and 5 are utilized for uniform ground distribution. Top Metal 1 and Top Metal 2 are used for grounding too, but these layers also include RF lines, capacitors, and inductors, which prevent uniform ground distribution. As a drawback, the gap between the RF line and its return path becomes smaller, which concludes with an increased capacitive effect.

2.2. Single-Pole-Double-Throw (SPDT) Switch

The wideband core-chip presented in this dissertation has a bidirectional CC that is connected to the front-end blocks by the Single-Pole-Double-Throw (SPDT) switch. An ideal SPDT switch should have almost zero insertion loss on the selected signal direction while isolating the unused path from the remaining parts with no power consumption.

Various switch designs are presented in the literature that are targeting the basic switch features. The series-shunt topology is one of the most common architecture in SPDT designs, mainly due to its simplicity and compactness (Dinc et al 2012). Besides its advantages, it has high loss and limited isolation due to the imperfect nature of the NMOS devices in SiGe technology. The design can be improved by adding LC tank circuitries to the transistors that resonate at the frequency of interest. They present lower loss and higher isolation at the expense of increased area (Ozeren et al 2016). The quarter-wavelength (*λ/4*) transmission lines can also be introduced to succeed in high-performance switch design. In this approach, one of the *λ/4* transmission lines is grounded, when one signal path is selected. This creates an almost ideal open circuit at the other end of the transmission line, which results in high isolation for the SPDT. The isolation and the insertion loss of those kinds of SPDTs are limited by the open-and-short terminations of the transmission lines (so the transistors). The disadvantage of this approach is a consequence of its nature; its highly dependent on the frequency of interest. Moreover, it might cover large areas if the design targets low center frequency (Davulcu et al 2017). Therefore, this topology is usually favored at higher frequencies, such as the W-or-D band. The active switch designs can also be candidates for the wideband core-chips, as presented in (Comeau et al 2006). It utilizes two common-collector amplifiers, while the signal path is controlled by turning the amplifiers on and off. The loss of the described SPDT design is lower than the passive topologies, due to utilizing amplifiers with the expense of increased power consumption and reduced dynamic range. When the performances of the mentioned architectures are considered, the series-shunt topology is chosen to be utilized in the wideband core-chip design, due to promising a wide bandwidth, flat insertion loss and almost-zero power dissipation in a compact area. The

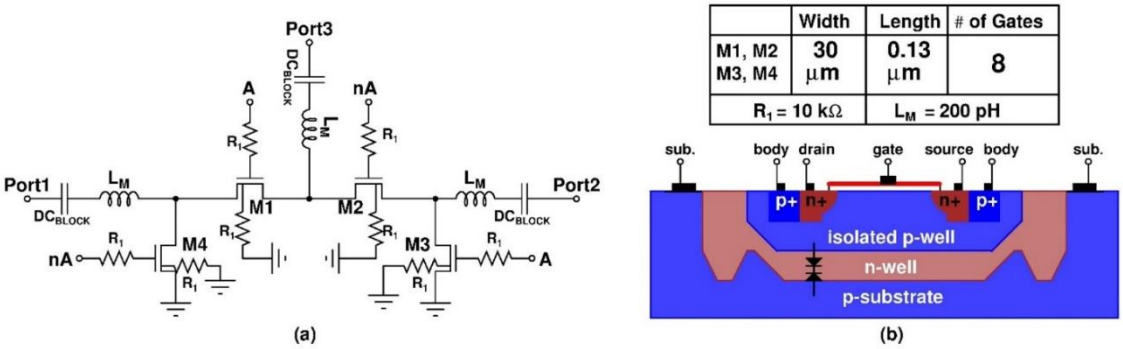


Figure 2. 6 (a) The block diagram of the SPDT. (b) The cross-section of the iNMOS.

block diagram of the designed series-shunt topology is presented in Figure 2. 6.

The series-shunt topology is based on switching the transistors according to the selected signal path. When the transistors M1 and M3 are turned on, the signal at Port-1 can be transferred to the Port-3. At the same time, M2 and M4 should be turned off to prevent any signal leakage to ground and the Port-2; M3 grounds any possible signal leakage that is introduced from Port-2. The insertion loss and the isolation of the topology are determined through the on-and-off channel resistances of the transistors and the substrate conductivity. The SPDT switch is designed by utilizing isolated-NMOS (iNMOS) devices, where the channel is formed inside a p-well that is newly formed. It is isolated from the p-well of the substrate by an n-well boundary. The possibility of RF signal leakage to the p-well substrate is reduced by forming the device inside an n-well pool. The cross-section of the described transistor can be seen in Figure 2. 6 (b). The n-well is connected to a high voltage as a reverse bias to the pn-diodes. For similar purposes, the body and the gate terminals of the device are connected by a 10 kΩ resistance (R_1), which is defined as the "floating gate and body technique" (Dinc et al 2012).

In the conventional design approach, the sizes of the iNMOS devices are chosen to minimize the insertion loss of the switch. However, the transistors parasitic capacitances also become larger as their sizes increased. Hence, the loss of the SPDT starts to be dominated by the parasitic capacitance of the large transistor. Moreover, its loss starts to be dependent on frequency, which concludes with a negative slope. This is a major problem for an SPDT switch that aims wide bandwidth. As a solution, the device sizes might be favored as small for a low on-and-off mode parasitic capacitances. Within the described way, the SPDT's insertion loss will be less variant over the frequency. So

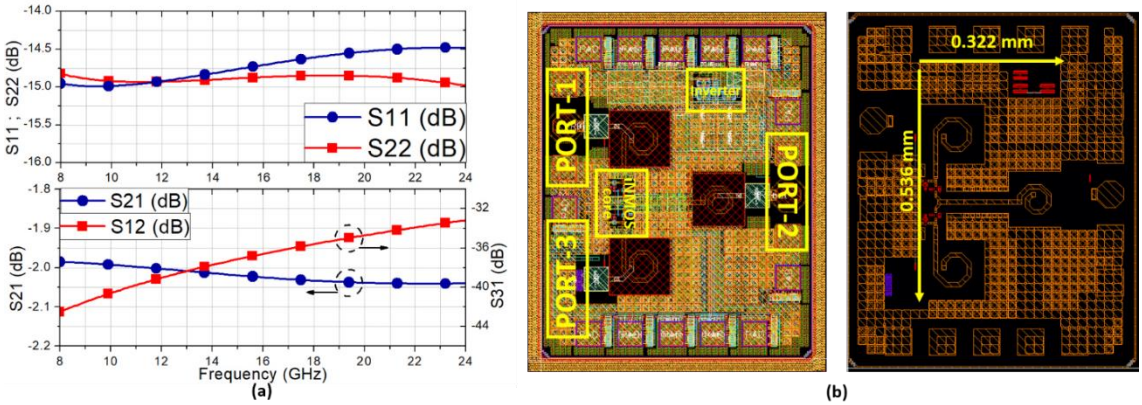


Figure 2. 7 (a) The post-layout S-parameters, (b) The top view of the SPDT switch.

the designed switch's loss is sacrificed (increased resistance) to conclude with a flat response and almost constant terminal impedance over the defined BW. The inductors in the SPDT, L_M, are utilized to resonate the parasitic capacitance of the transistors and properly match the impedance of all ports. It should be noted that L_M also brings a frequency dependency. Hence, it is designed by considering the trade-off between the impedance termination and the frequency dependency.

Figure 2. 7 (a) presents the post-layout S-parameter simulation results of the SPDT switch. It has 2 dB of flat loss with more than 32 dB of isolation. These results confirm that the design is appropriate for the wideband core-chip. Any variation in on-and-off mode parasitic values of iNMOS devices is going to affect the loss, its slope, and isolation of the switch. The output-referred compression point (OP1dB) of the switch is simulated as + 15.27 dBm. Figure 2. 7 (b) demonstrates the top view of the SPDT switch, which is ready for the fabrication. The "Port-3" is terminated with 50 Ω to simplify the measurements. Additionally, the iNMOS devices are controlled by integrated inverters, to decrease the number of required pads. When the pads and DC blocking capacitors are excluded, the SPDT switch has an area of 0.18 mm^2. The DC blocking capacitors are removed during the integration to the wideband core-chip.

2.3. The Bidirectional Amplifier (BDA)

The bidirectional amplifier (BDA) is one of the significant blocks of the wideband

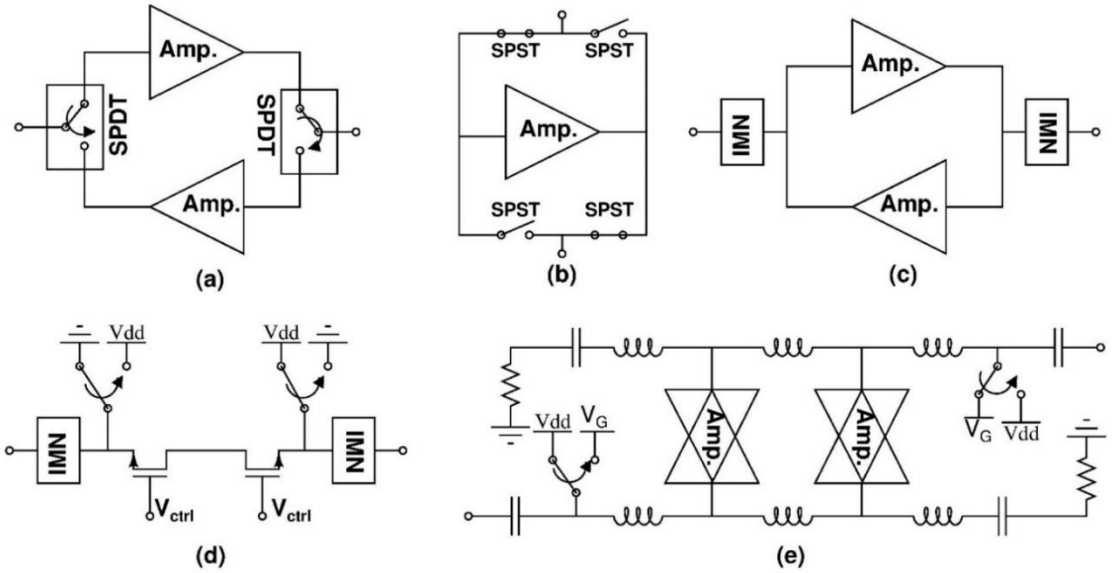


Figure 2. 8 Various methods for bidirectionality in an amplifier; (a) switching between two amplifiers, (b) single amplifier with four switches, (c) Common IMN topology, (d) Common IMN with a single amplifier, (e) the distributed BDA.

core-chip. The drawbacks of the other blocks, such as negative gain slope, high loss, and NF, is suppressed by the BDA. Moreover, the BW expectations of the core-chip are realized, without sacrificing from low power dissipation, and compactness of the block.

The BDA architectures can be categorized into five groups as in Figure 2. 8, regarding the bidirectionality formation. The architecture in Figure 2. 8 (a) utilizes two separate amplifiers to form a BDA. Two SPDT switches are utilized to determine the signal direction with the expense of increased area, power consumption and limited bandwidth (Cho et al 2013). The number of amplifiers can be reduced to one as in Figure 2. 8 (b), to conclude with a smaller area and lower power consumption. However, the design might still suffer from low gain and high NF, due to an increased number of single-pole-single-throw (SPST) switches. Some of the designs favor common impedance matching networks (IMN) as in Figure 2. 8 (c), to improve compactness, gain and NF features. They mainly depend on quarter-wavelength (λ/4) transmission lines, which dominates the BDA area. Therefore, they are preferable for higher frequencies (Kumar et al 2017). Although common IMNs can be introduced to a single amplification stage, which has a proper supply switching mechanism shown in Figure 2. 8 (d), they have a narrow band of operation (Yang et al 2004).

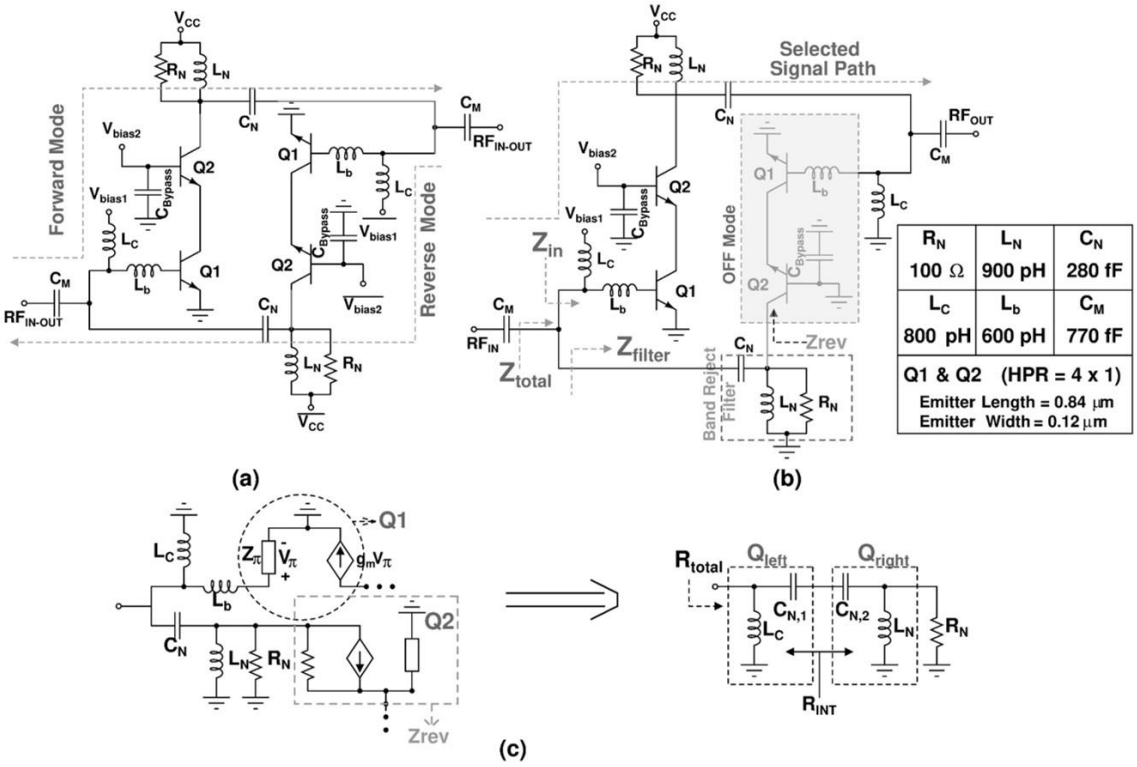


Figure 2. 9 a) Schematic of the BDA. b) Signal flow of the BDA during forward-mode. c) The small-signal model of Q1.

The distributed networks as in Figure 2. 8 (e) are one of the most preferred topologies for the BDAs, and notable performances have been presented in the literature. Alizadeh demonstrated a 2-to-12 GHz distributed BDA implemented in 180 nm CMOS technology. The design has 10 dB gain while dissipating 380 mW of power in 1.89 mm^2 area (Alizadeh et al 2019). Cho achieved 17 GHz of bandwidth with 10 dB gain, a maximum of 6.5 dB NF in 0.81 mm^2 of an area by utilizing 130 nm CMOS technology (Cho et al 2013). The mentioned works have a common feature; they have flat gain. The wideband core-chip target wide operation bandwidth while including multiple sub-blocks. Therefore, cascading multiple sub-blocks might conclude with a complicated non-linear and/or negatively sloped gain characteristic (Çalışkan et al 2019), which contradicts with the expectations. The BDA that is integrated into the core-chip, should have low output power and group delay (GD) variation over the frequency. Within these metrics, it might be compatible with a wideband radar system. Because of the described concerns, a common IMN network without λ/4 lines favored for the presented BDA.

2.3.1. The BDA Design Procedure

The BDA should be capable of operating in both signal directions with high stability. High isolation between terminals can be obtained by preferring the cascode topology, due to reduced Miller capacitance (Çalışkan et al 2019). However, the noise and power dissipation are sacrificed compared to common-emitter based amplifier. As shown in Figure 2. 9 (a), the BDA is composed of two cascode amplifiers that are connected back-to-front. When a signal path is selected, one of the amplification stages is turned on while the other one turned off. Figure 2. 9 (b) summarizes the schematic view during the forward-mode.

Wide bandwidth, positively sloped gain, low power dissipation, and small area are some of the expected features of the BDA. These contradicting specifications forced each part of the design has multiple functionalities. The LC-type network is introduced as the output matching networks of the amplifier for proper impedance termination. At the same time, it works as a band-reject filter for the forward-mode. The attenuation of the filter is high at the lower end of the bandwidth, which guides the amplifier to have a positively sloped gain. The values of the reactive components (L_N, C_N, and R_N) are determined by the resonance frequency (ω_0) that is chosen as 10 GHz.

The design procedure depends on a significant assumption; the amplification stage should have high on-and-off mode output impedances. Within this way, their effect on the filter can be neglected. The conventional noise-and-power matching technique utilizes the largely-sized high-performance (HPR) *HBT* devices, which produce in having low and highly reactive amplifier terminations. Therefore, a conventional amplifier might conclude with limited BW and high-power dissipation. In the realized BDA, the size of the HBTs is favored as small as possible with the expense of reduced gain. An emitter degeneration inductor is not utilized to tolerate the gain drop. The mentioned approach results with high input (Z_π) and output (Z_{rev}) impedances for the cascode stage. For the determined bias conditions, the input-output impedances of a single cascode stage are 6 kΩ and 1 MΩ, respectively (extracted from DC simulations and process documentation). The supply voltages of the amplifiers are determined through the breakdown level of the HPR HBTs, while the base bias of the *Q1* is selected for a peak f_t around 250 GHz.

The input impedance of the *Q1* can be simplified to a shunt L_C for the forward-mode of operation, because of neglecting the effect of Z_π. Assuming high Z_π and Z_{rev} simplifies the small-signal model of the forward mode *Q1* as in Figure 2. 9 (c). As shown, the band-reject filter is converted to a π-type network, where L_C is utilized as an RF-choke inductor for the bias of *Q1*. The component values of the band-reject filter are already determined for a 10 GHz of ω_0 (900 pH of L_N and 280 fF of C_N), where L_C can be calculated from the following impedance transformations;

$$L_C = \frac{R_{total}}{\omega_o Q_{left}}; L_N = \frac{R_N}{\omega_o Q_{right}} \tag{3}$$

$$C_{N,1} = \frac{Q_{left}}{\omega_o R_{INT}};\ C_{N,2} = \frac{Q_{right}}{\omega_o R_{INT}} \tag{4}$$

where

$$Q_{right} = \sqrt{\frac{R_N}{R_{INT}} - 1}\,; Q_{left} = \sqrt{\frac{R_{total}}{R_{INT}} - 1} \tag{5}$$

Q_{right} can be calculated to extract the R_{INT} impedance. Later, R_{INT} will be utilized to find Q_{left} and L_C, respectively. For the mentioned steps, R_N can be assumed as 100 Ω; higher values are going to result with improved gain with the expense of declined bandwidth as will be explained. Within the provided component values, L_C can be founded as 773 pH.

The BDA should provide a wideband matching performance. Hence, Z_{total} should also be analyzed to observe the effect of each component on bandwidth. The equation (6) presents the impedance of the filter (Z_{filter}) when a high Z_{rev} is assumed. As presented, the real part of the Z_{filter} is mainly determined by the R_N. Z_{filter} is in parallel with the amplifier's input impedance (Z_{in}), which makes Z_{total} more complicated. To simplify the calculations, L_N is neglected at this step of the calculations due to acting as a high impedance node. Assuming high L_N reduces (6) into "R_N -$(j/\omega C_N)$" and Z_{total} can be founded as in (7).

The $\Re(Z_{total})$ is mainly determined by R_N, which is multiplied with a frequency

$$Z_{filter} \cong \frac{\omega^2 R_N L_N^2}{R_N^2+(\omega L_N)^2} + j\frac{(\omega L_N)^2-(R_N)^2(\omega^2 C_N L_N-1)}{\left[R_N^2+(\omega L_N)^2\right](\omega C_N)} \tag{6}$$

$$Z_{total} \cong \frac{R_N(\omega^2 L_C C_N)^2}{(\omega C_N R_N)^2+(\omega^2 L_C C_N-1)^2} + j\frac{\omega^3 L_C C_N\left(R_N^2 C_N-L_C\right)+(\omega L_C)}{(\omega C_N R_N)^2+(\omega^2 L_C C_N-1)^2} \tag{7}$$

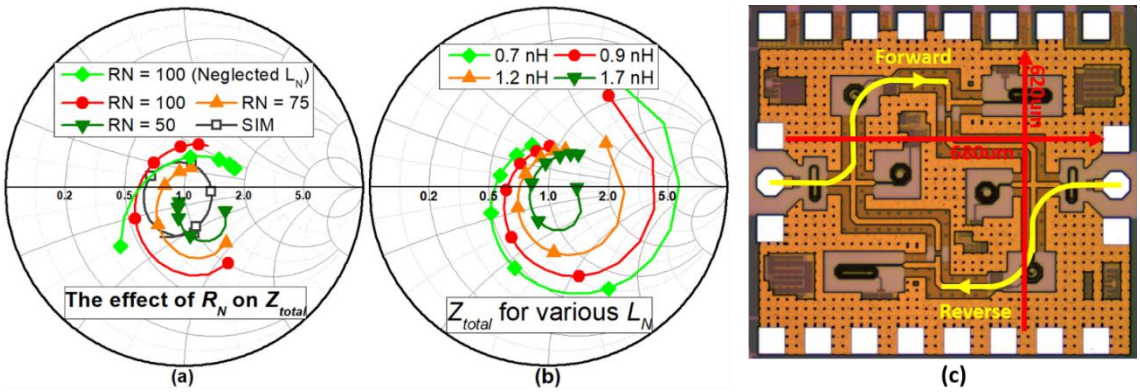


Figure 2. 10 The effects of (a) R_N, (b) L_N on Zotal. (c) Top-view of the BDA.

dependent term. Therefore, Z_{total} has a circle-like behavior on the Smith Chart, which can be seen in Figure 2. 10 (a) and (b). Moreover, $\Im(Z_{total})$ includes a ωL_C term, which causes (7) always have a positive imaginary part. It can be suppressed by using the DC blocking capacitor, C_M, also as a matching component. The described design procedure validates wideband 50 Ω termination, where the radius of the circle is mainly determined by R_N.

It should be noted that neglecting a component might appear significant calculation and simulation variations. Because the component might have a negligible impact on one band of operation while having a dramatic impact on the remaining part of the band. Therefore, further simplifications on provided equations are not feasible. Figure 2. 10 (a) presents calculated Z_{total} with and without neglecting L_N for R_N values of 100 Ω, 75 Ω and 50 Ω. As shown, neglecting L_N resulted in a shifted Z_{total}, even if it has approximately the same 50 Ω surrounding circle radius. Beyond this, the calculations are validated with the simulations, which included HBT models of the technology and ideal lumped components.

Considering the trade-off between impedance termination and gain, R_N is preferred as 100 Ω. A 50 Ω of R_N might appear a better return loss for BDA with the expense of reduced gain. As shown in Figure 2. 10 (a) the radius of the Z_{total} circle shrinks as R_N decrease. Figure 2. 10 (b) demonstrates the effect of the L_N on Z_{total}, while other components remained the same. As shown, L_N should be selected as high as possible for a wideband of operation. The inductance of a spiral inductor can be controlled through various parameters, such as the number of turns or inner radius. However, those parameters also increase the inductor's shunt parasitic capacitance, which deteriorates the

self-resonance frequency. Therefore, a lower L_N value (900 pH) is favored for the BDA design by sacrificing from the impedance termination. The input-output impedances for both forward-and-reverse modes of operations should be approximately the same, due to assuming a high Z_{rev}. Additionally, a series base inductor (L_b) is used to tolerate the capacitive effects of the cascode amplifier.

An SCU circuit is designed for the BDA, as for the X-Band core-chip in section 1. 3. 1; the block diagram of the SCU is shown in Figure 1. 7 (b). It is composed of buffers, which are designed by considering the current level of the bias points. Three buffer networks are required for a single cascode stage (six buffers in total). The design of these buffers is critical because the cascode transistors might exceed their breakdown limits during the switching if the order of the biases is not organized. To prevent that problem, the buffers are designed in a way that the "Vbias1" will be provided firstly, which is followed by "Vbias2" and "Vcc". When the signal direction is reversed, the biases are powered down in the reversed order. The current flows from the supply voltages of the buffers to the terminals of the cascode stages. The control signal, which determines the signal direction, is connected to the gate of six separate buffers (so SCU). The BDA in Figure 2. 10 (c) has 0.42 (0.62 x 0.68) mm^2 of area, including pads. During small-signal operations, the design dissipates 13.8 mW of power from 3.3 V of the supply voltage.

2.3.2. The Measurement Results of the BDA

R&S ZVA67 vector network analyzer is utilized for measuring the S-parameters of the fabricated BDA. The simulation-measurement comparison for S-parameters are presented in Figure 2. 11 (a); only forward-mode simulations are provided for brevity. The measurements are highly coherent with the simulations and they demonstrate almost the same behavior for both signal directions. The BDA has a measured 11.2 dB peak gain at about 21 GHz, with an adequate level of impedance termination throughout the BW. It succeeds a + 0.58 dB/BW of gain slope between 8-to-24 GHz. The block demonstrates maximum - 45 dB of S12 in the frequency of interest, which guarantees the adequate isolation between signal paths and stability of the BDA. The gain of the BDA can be improved by sacrificing from power consumption. As shown in Figure 2. 11 (b), the block can have a gain level up to 12.4 dB with the expense of increased power dissipation

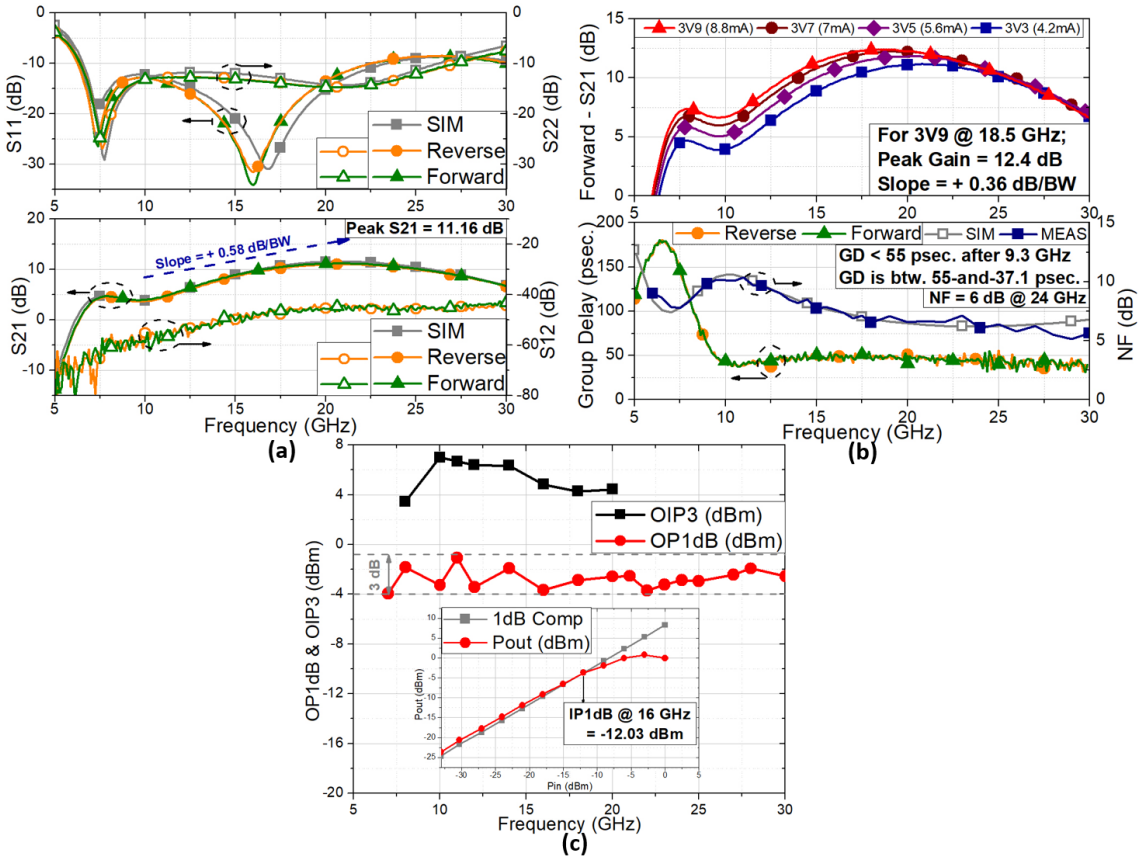


Figure 2. 11 (a) Simulated and measured S-parameters of the BDA. (b) Measured forward-mode gain for various collector currents, GD and NF of the BDA. (c) The OP1dB and OIP3 of the BDA for the defined frequency range.

and decline gain slope (+ 0.36 dB/BW). The gain drop after 21 GHz is because of non-ideal transmission lines and lumped components. This effect can be reduced by preferring a lower metal for the return path of the microstrip line. Although the wideband core-chip includes a phase shifter, the sub-blocks are designed by considering their group delay. The BDA has a mean 41 psec. of group delay with ± 9.1 psec. variation, which confirms that the design is valid for wideband systems.

Agilent E4448A spectrum analyzer and 346CK01 noise source are used to measure the BDA's NF performance, which is shown in Figure 2. 11 (b). As a result of having a positively sloped gain, the NF is decreasing as the frequency increase. It is measured as 6 dB at 24 GHz. The gain-drop around 10 GHz, which is a consequence of selected ω_0, resulted in a sudden peak in NF. It should be noted that the BDA is favored to tolerate the gain loss inside the core-chip. Within that way, NF will be still dominated by the LNA.

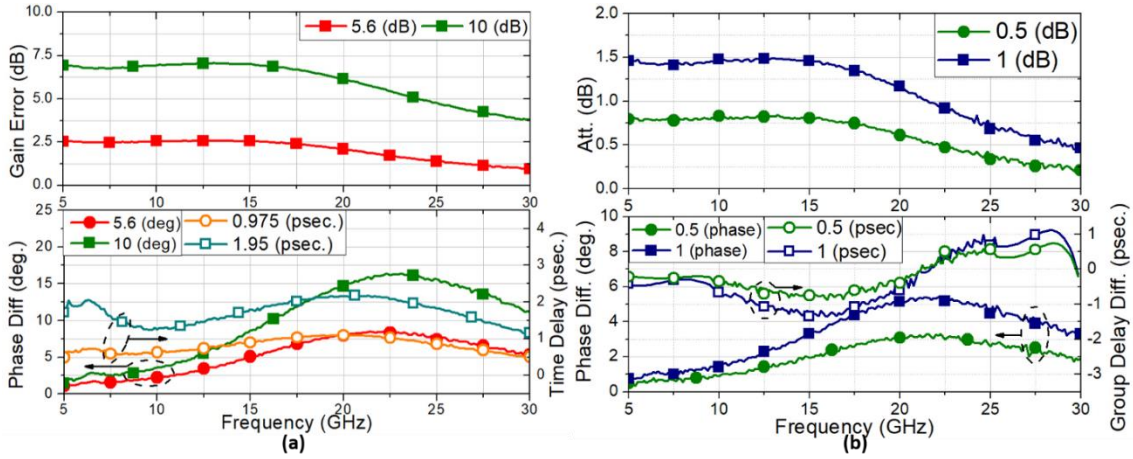


Figure 2. 12 (a) 5.6^0 and 10^0 of phase shift, 0.975 psec. and 1.95 psec. of time delays obtained from BDA including their gain error. (b) BDA with 0.5 dB and 1 dB of gain steps, including their phase and group delay difference.

Hence, the NF varies between 6-to-10 dB over the frequency might not deteriorate the NF of the receiver chain dramatically. Additionally, the NF of the BDA can be improved by designing inductors (especially L_b) with higher Q-factor.

The output power measurements of the BDA are done by the same spectrum analyzer and Agilent's E8257D analog signal generator. The BDA should have low output power variation over the frequency for its adaptability to wideband systems. Figure 2. 11 (c) summarizes the output-referred 1-dB compression point (OP1dB) and output-referred third-order intercept point (OIP3) features of the BDA. For OIP3 measurements Agilent's E8267D vector signal generator is used. It can generate a two-tone signal until 20 GHz. The measurements demonstrated that the BDA succeeds -2.38 ± 1.32 dBm of OP1dB. The current flow increases 7.8 mA at the compression point of 16 GHz. Moreover, it achieved a mean + 6 dBm of OIP3 when 40 MHz separated two-tone signals are applied.

The wideband core-chip includes multiple BDA stages, due to the high loss of the CC. The added BDAs can be also utilized as a phase (or delay) and amplitude controllers. For that purpose, the block can be updated to include a current steering mechanism, which can change the collector current accordingly. Although the presented BDA does not include that functionality, the measured BDA's current level can still be steered through its supply voltage. Figure 2. 12 (a) demonstrates the generated various attenuation, phase

and delay steps of the measured BDA. The PS and attenuator of the core-chip targets 22.5^0 and 2 dB of step size, respectively. Therefore, the BDA steps can be determined to improve the resolution or correct the errors of the core-chip. As an advantage of the preferred design procedure, the terminal impedances have negligible variations as the collector current changes.

The BDA's phase, gain, and delay can be controlled through its supply voltages. For a 10^0 of a phase shift, $\pm 7^0$ of variation over the frequency is observed. Therefore, controlling BDA for a high phase shift may not be feasible. Although some fluctuations observed for the 10^0 of phase shift, the BDA has a more tolerable performance for 5.6^0 of phase shift. It should be noted that the BDA is designed by considering low GD variation which contradicts with the flat phase shift expectation. Consequently, the generated phase shifts have a certain level of slope over frequency. In other meaning, the block might have high GD variation, if a flat phase shift is obtained. Therefore, the measured BDA can control time delay more accurately, as presented in Figure 2. 12 (a); 0.975 psec. and 1.95 psec. of time delays are obtained, which are equivalent to 5.6^0 and 11.25^0 of phase shift at 16 GHz. As shown, the measured BDA is more appropriate to be utilized as a time delay unit. Similarly, the current level of the BDA is varied to obtain 0.5 dB and 1 dB of gain controls. As shown in Figure 2. 12 (b), the BDA can generate almost flat attenuation steps over 8-to-24 GHz. Additionally, it has a low GD error between different amplitude states, which confirm its usage as an additional amplitude controller inside the core-chip.

2.3.3. The Comparison of the BDA with Similar Works in Literature

Various BDAs have been designed for different purposes; i.e. amplifier, switch. Table 2. 2 compares the presented BDA with similar works in literature. The provided references in Table 2. 2 are designed by utilizing 130 nm technology. When the gain level is considered, (Cho et al 2013) has a similar performance with the expense of increased area and power dissipation. (Sim et al 2013) demonstrated the smallest BDA in literature, but it has a low and flat gain with a 9 GHz of BW. Additionally, it consumes 68 mW of power. (Cho et al 2016) and (Song et al 2016) are designed as a switch and a combiner/divider respectively, but they utilized bidirectional distributed amplifier topology as (Cho et al 2013) and (Sim et al 2013). Series and shunt iNMOS devices are

Table 2. 2 Comparison of the BDA with similar works in the literature

	Tech. [130nm]	Freq. [GHz]	RL [dB]	Gain [dB] *	Slope [dB/BW]	Iso. [dB]	OP1dB [dBm]	IIP3 [dBm]	NF [dB]	GD Flat.[psec]	P_{DC} [mW]	Area [mm^2]
(Cho et al 2013)	CMOS	5-20	>10	11	Flat	-	6	5	6.5	± 25	68	0.82
(Sim et al 2013)	CMOS	5.5-14	>10	6.2	Flat	-	+7.4[ǂ]	-	6.3[ǂǂ]	-	43	0.23
(Cho et al 2016) [†]	SiGe	2-22	>9	6	+ 0.2	37	-1.2/ -7.5	-1.2/ -3.2	-	± 21	25	1.04
(Song et al 2016) [††]	SiGe	2-22	>7	9.6	Flat	>18	3.4	-	-	-	100	1.3
This Work	SiGe	7-30	>9	11.16	+ 0.58	45	-2.5	- 3.6	6	± 9.1	13.8	0.42

*max. Gain ** min. NF [ǂ]between 8.5-10.5 GHz [†]DPDT Switch [††]Divider/Combiner.

added to (Cho et al 2016) for generating a Double-Pole-Double- Throw (DPDT) switch from a BDA. The design might have comparable gain when the transistors are excluded, but its OP1dB is not flat. Although (Song et al 2016) demonstrated better OP1dB performance compared to (Cho et al 2016), it is consuming 0.1 W of power; about 7 times higher than the presented BDA. Among the mentioned works, the measured BDA achieved the best gain-BW performance without sacrificing its compactness and power dissipation. Moreover, it can still have an adequate level of performance on other RF features such as NF and GD features, which is crucial for wideband RF systems. The presented BDA is in minor revision as a letter in "Transactions on Circuits and Systems II: Express Briefs", which is called "A Switchless SiGe BiCMOS Bidirectional Amplifier for Wideband Radar Applications".

2.3.4. Updates for the BDA

The performance metrics of the BDA is extracted by considering the requirements of the specified core-chip. However, the block has multiple contradictory expectations. Hence, a performance priority list is generated; bidirectionality, bandwidth, positively sloped gain, compactness, and low power dissipation. During the design procedure, some of the specifications were sacrificed due to non-ideal effects. The power consumption can be categorized as one of them. It was close to 7.5 mW in ideal-simulations and the current level is increased to tolerate the loss of the passive components. Likewise, the gain is sacrificed for an improved impedance termination. If the ω_0 of the filter is favored at a lower frequency, the gain might have a more-linearly increasing characteristic. However,

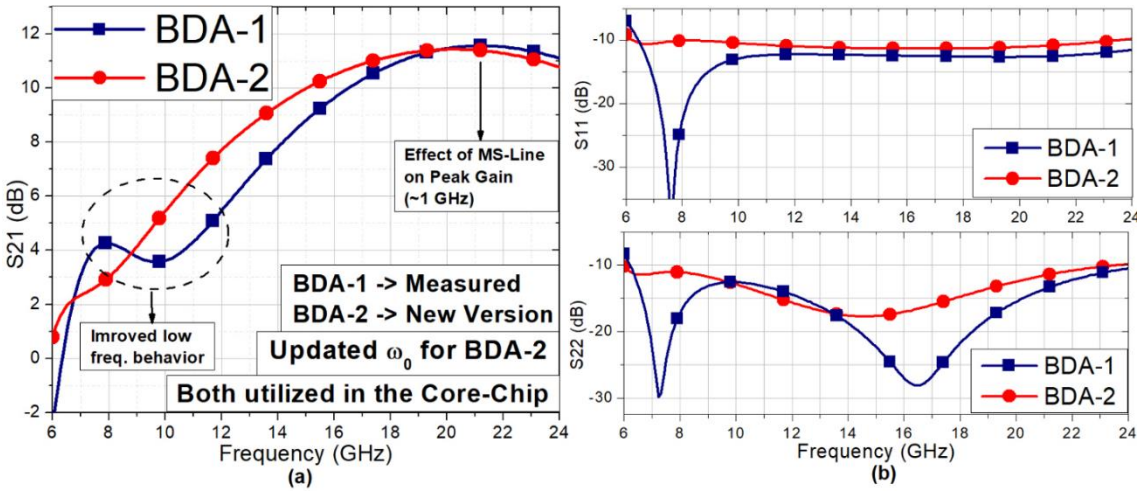


Figure 2. 13 The difference between two BDA version in terms of (a) S21, and (b) impedance matching performance.

the new ω_0 may require larger inductors, which might have high variations over the frequency and declined return loss performance. This might have significant effects on the core-chip, because of the BDAs effect on nearby blocks; the attenuator and PS are designed by considering an ideal 50 Ω. Therefore, their performance would vary over frequency when they are cascaded with a low-ω_0 BDA. Figure 2. 13 compares simulated the gain and matching performances of the presented BDA (BDA-1) and a new BDA that has a lower ω_0 (BDA-2). As shown, BDA-2 has an improved gain characteristic at X-Band with a deteriorated return loss; BDA-2 is also ready for fabrication, but only BDA-1 is fabricated as a prototype. In the core-chip, multiple BDAs are utilized; BDA-1 and BDA-2 are combined regarding the phase and amplitude performance of the core-chip, as will be mentioned in section 2. 6.

2.4. Attenuator

The amplitude control of the wideband core-chip is enabled by the attenuator in the CC. The beam sharpness control, side-lobes suppression, better null-points, and corrections for the amplitude errors of the PS are enabled by the attenuator (Davulcu et al 2016). These mentioned capabilities caused the attenuator to be a crucial block for a transceiver.

An ideal attenuator should vary the amplitude of the incoming signal without changing the phase component. The RMS phase and gain error values are two parameters that demonstrate the resolution performance of the block; (8) presents the RMS phase and gain error calculations for an *N*-bit Attenuator as a function of frequency, *f*. $\Delta\phi$ stands for the phase difference compared to the reference state. The ΔG symbolizes the gain/amplitude variation between each attenuation state. For an *N*-bit attenuator, 2^N attenuation states exist. The LSB is 2 dB for the designed 4-bit digital step attenuator and the range is chosen as 30 dB. The RMS amplitude error of an attenuator should be lower than its LSB/2, to obtain 2^N phase states properly. If the RMS amplitude error is between LSB/2 and LSB, some of the gain states will not able to be generated. However, it can still be counted as an N-bit attenuator, until RMS error does not exceed LSB. For example, the RMS amplitude error of a 4-bit attenuator should be lower than 1 dB to generate 16 phase states and the block will lose some of its states if its RMS amplitude error is higher than 1 dB.

The VGA is one of the topologies that is preferred for the amplitude control of the core-chip. It can provide gain, which is the main advantage compared to passive attenuators. The current steering methodology is a generally preferred method for a VGA, in which the collector current of a cascode amplifier is steered by additional transistors. When these transistors are turned on, the current of the amplifier decreases and the desired gain drop can be achieved. As a drawback, the VGAs might have high phase variation at different gain states, which contradicts with the ideal amplitude controller expectations. In addition to being unidirectional, the VGAs have limited dynamic range and high-power dissipation compared to attenuators. Moreover, they are unidirectional. The mentioned concerns limit the application areas of the VGAs, especially for wideband systems (Dogan et al 2008, Ku et al 2010).

The resistive-type passive attenuators are one of the generally preferred topologies due to their simplicity and wideband behavior. Different attenuator architectures can be

$$RMS\ Phase\ Error\ (f) = \sqrt{\frac{\sum_{n=1}^{N}\left(\Delta\phi_n(f)\right)^2}{N}} \quad ;$$

$$RMS\ Gain\ Error\ (f) = \sqrt{\frac{\sum_{n=1}^{N}\left(\Delta G_n(f)\right)^2}{N}} \tag{8}$$

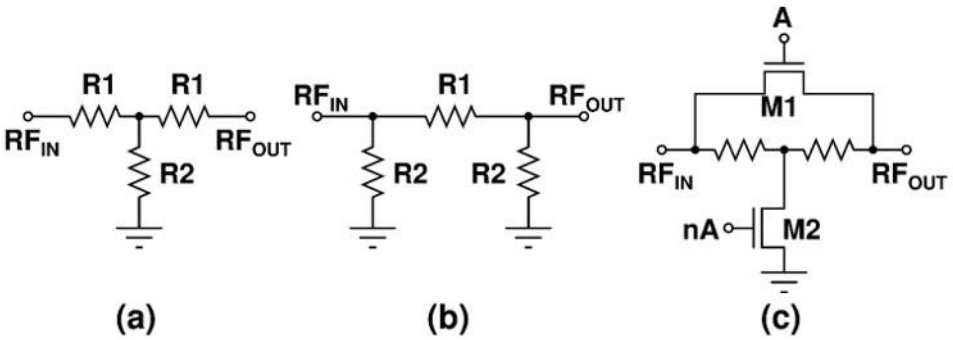


Figure 2. 14 Schematic view of a) T-type, b) π-type, c) Bridged T-type attenuators.

implemented by changing the order of the resistors, but the T-type and π-type attenuators provide reciprocal behavior as presented in Figure 2. 14 (a) and (b), respectively. Figure 2. 14 (c) demonstrates the bridged T-type attenuator, where the iNMOS transistors change the attenuation state (Ku et al 2010). A similar switching mechanism can be applied to the π-type network, which can provide higher attenuation steps due to including two ground termination. Besides the bridged T-type (or so-called switched path attenuators), distributed attenuators are also presented as an approach however they include quarter wavelength transmission lines, which can occupy a large area in core-chip (Min et al 2010). In the scope of this dissertation, a 4-bit 30 dB range digital step attenuator is designed by preferring Figure 2. 14 (c). The T-type networks are preferred for the attenuator design because of their compact area and bidirectional behavior.

2.4.1. The Design Procedure of the Attenuator

A fixed attenuation level of a T-type network is determined by the resistors R_1, R_2 and the desired load impedance Z_L as shown in (9) and (10). When M1 is on and M2 is off, the signal will flow through an equivalent resistance of M1 and the resistor for a high off-mode M2 impedance. A higher attenuation is going to be observed for the reversed case because the signal is going to see a ground termination. The values of the resistances are also chosen considering the input impedance presented in (9) when an on-

$$Attenuation = 20\log\left(\left[\frac{R_1}{Z_L}+1\right]\left[1+\frac{R_1}{R_2//(R_1+Z_L)}\right]\right) \quad (9)$$

$$Z_L = Z_L + [2R_1//R_{ON}] \quad (10)$$

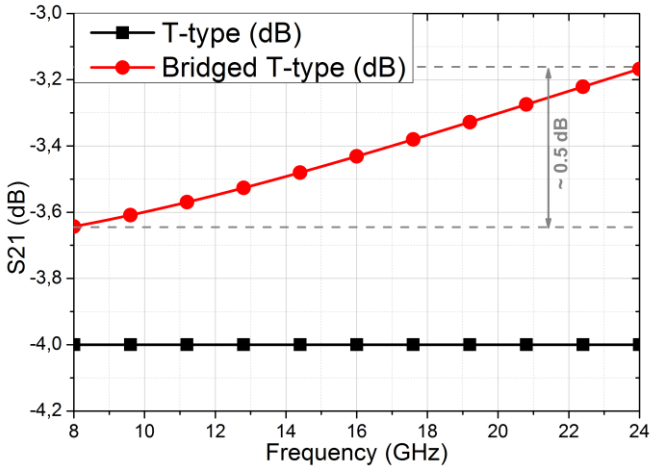


Figure 2. 15 Comparison of an ideal and a bridged T-type 4-dB attenuators.

mode resistance of M1 is assumed as R_{ON}; off-mode resistance of M2 is neglected due to its high value. The required R_1 and R_2 resistances for a 4-dB attenuator bit are calculated as 11.31 Ω and 104.8 Ω respectively, for ideal switch cases. Figure 2. 15 compares an ideal 4-dB and bridged-T type attenuator bits which utilize large iNMOS devices by preferring the calculated R_1 and R_2 values. As can be seen, an ideal 4 dB attenuator is coherent with the calculations, but a deviation is observed for the 4 dB bridged-T type attenuator. This is a consequence of the transistor's parasitic effects; finite off-mode resistance and large capacitive effects. The desired attenuation level decreased, due to increased insertion loss. Moreover, the attenuation level is highly dependent on frequency, which is a consequence of preferring large iNMOS devices. The resistive type passive attenuators deliver wide BW, where the dependence on frequency is mainly contributed by the parasitic capacitance of the iNMOS devices. The attenuator in T/R module core-chip should have 4-bit of operation through 8-to-24 GHz, therefore the parasitic effects should be minimized. The size of the switching devices in each attenuator bit is chosen considering their capacitive effects. This results in high on-and-off resistances for the transistors. As a drawback, the loss of each attenuation bit is high compared to the conventional approach.

In addition to its attenuation behavior, the phase difference is also another significant metric for the attenuator. When the losses of the attenuator bits are decreased by preferring larger iNMOS sizes, a certain amount of phase variation can be observed. This can be tolerated by some methodologies, such as the addition of a shunt inductance between each port. However, those approaches may increase the frequency dependency

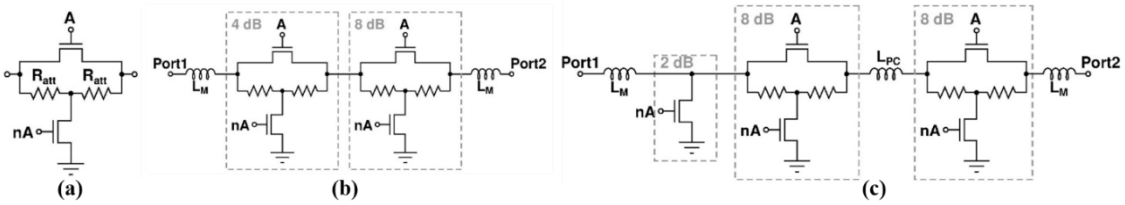


Figure 2. 16 The schematic views of the a) single T-type attenuator, b) 4-and-8 dB attenuation section, c) 2-and-16 dB attenuation section.

and area. The attenuator in the wideband core-chip has small transistors, which provided low phase variation. Therefore, no methodologies for phase compensation is applied.

The attenuator is divided into two sections to realize a core chip with a lower NF, as shown in Figure 2. 16. The bits utilized small devices for low amplitude and phase variation over frequency. This concluded with a design dominated by the on-resistance of the iNMOS devices and attenuation resistance (R_{att}). As a drawback, the attenuator sections are matched to a high impedance node during the reference mode. Although the first section, which cascades 4-and-8 dB of attenuation bits (Att-1), has an adequate level of impedance matching, the second section suffers from the described problem. Therefore, the schematic view of 2-and-16 dB (Att-2) of attenuators is updated as shown in Figure 2. 16 (c). As presented, the design does not include any series iNMOS device and R_{att} for 2 dB of attenuation, to lower the impedance during the reference mode. The Att-2 has an inductor (L_{PC}) to compensate for the shunt capacitance effects of the transistors. The series inductors in both sections (L_M) are utilized for matching purposes. The gate and body-floating techniques are utilized for all the iNMOS devices in the attenuator. The transistors are controlled through the inverters to simplify the measurements. Each attenuator section has DC blocking capacitors, which are going to be de-embedded during measurements. Their sizes are selected as 5 pF to have an almost ideal RF-short at 8 GHz, even it has a high shunt parasitic effect around 24 GHz.

The measurements and experiences from the technology demonstrated that the on-and-off mode parasitic of iNMOS devices can vary highly, which can limit the performance of the attenuator. For instance, an attenuation stage can achieve up to 12 dB of attenuation even it was designed for 20 dB. When device sizes are considered, the possible on mode parasitic resistive effects (R_{par}) is calculated and added to the terminals

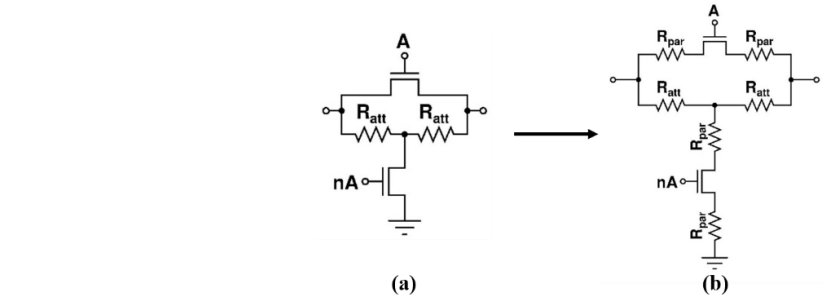


Figure 2. 17 R_{par} is added to the device ports. The schematic in (a) is converted to (b).

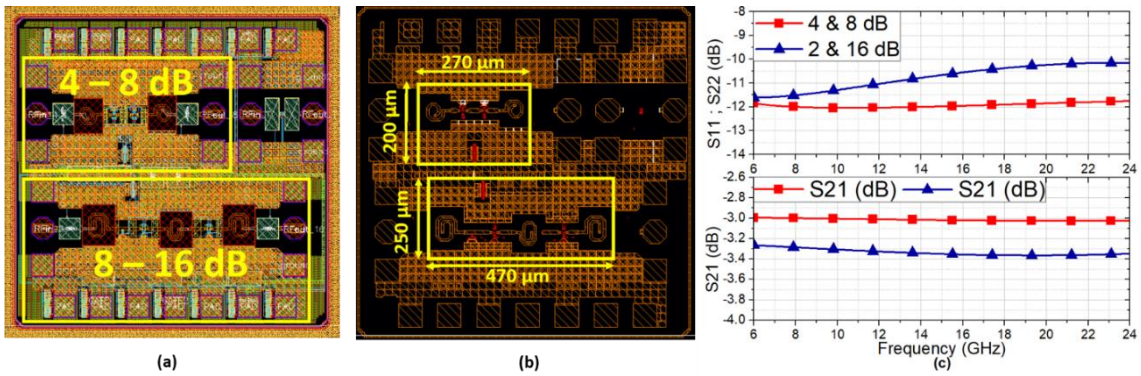


Figure 2. 18 (a) Top view of the attenuator. (b) The dimensions of the sections excluding pads. (c) Impedance terminations and S21 of the sections.

Table 2. 3 The component values of the attenuator bits with and without $R_{par.}$

	Without R_{par}			**With R_{par}**		
	M1 (µm)	**M2 (µm)**	**Ratt (Ω)**	**M1 (µm)**	**M2 (µm)**	**Ratt (Ω)**
2 dB	2.6	3	10	-	3.1	-
4 dB	6.15	6.15	10	7.2	7.2	10
8 dB	9.4	9.4	30	20	20	21
16 dB	21	21	40	24	24	20

of iNMOS devices regarding its size, as in Figure 2. 17. Table 2. 3 presents the component values of each section before and after including the parasitic. When the effect of R_{par} is included, larger device sizes are required to achieve the desired attenuation.

2.4.2. The Post-Layout Simulation Results

The attenuation sections are designed separately and EM simulations for each section. Figure 2. 18 (a) and (b) demonstrates the layout view of the designed attenuator sections. When the pads are excluded, the 4-bit attenuator is going to cover about 0.18 mm^2 of area. As in the BDA, similar design procedures are followed for transmission lines and inductors. Figure 2. 18 (c) presents the EM simulated S11 and S21 of the

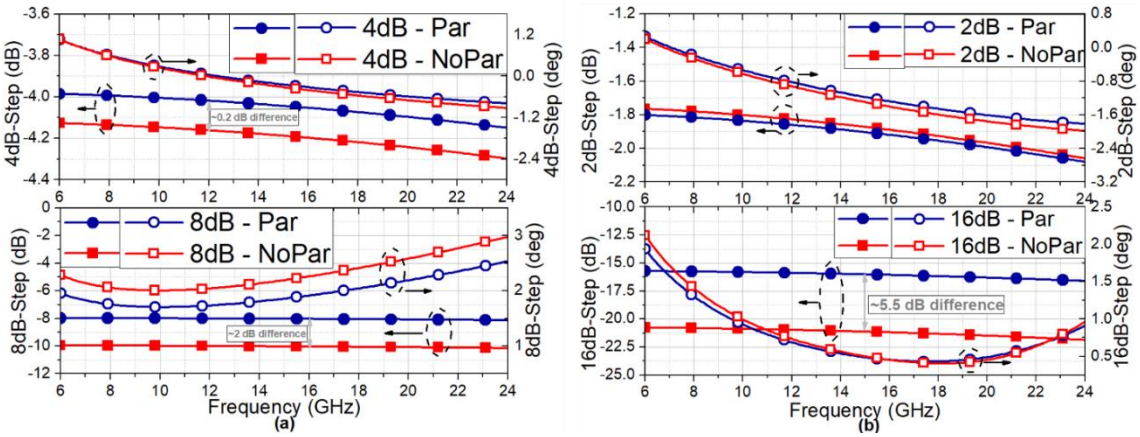


Figure 2. 19 The attenuation and phase differences of each individual bit.

designed attenuation sections including R_{par}. Only the S11 behavior is presented for brevity, due to reciprocal behavior of the designs. As mentioned previously, the Att-2 has larger iNMOS devices, which concluded with increased loss and deteriorated matching performance. However, it can still perform at an acceptable level.

The post-layout performances of each attenuation bit are presented in Figure 2. 19 for a 50 Ω termination. The performances of each major bit are shown with ("*Par*") and without the R_{par} ("*NoPar*"), to present the effect of R_{par} on Att-1 and Att-2. As shown, R_{par} has minor effects on 2 dB and 4 dB attenuators due to utilizing small device sizes. When R_{par} is neglected, the 8 dB and 16 dB of steps might result in 10 dB and 21 dB, respectively. At this point, it is not fully possible how will the R_{par} is going to vary, but the device sizes are chosen to prevent decreased attenuation range. Therefore, higher attenuation levels can be measured for all bits, which can be tolerated by sizing down the iNMOS devices or by changing the control voltage accordingly during measurements. Compared to the attenuation states, the phase differences of the bits do not vary highly with R_{par}, because of including a resistive parasitic.

Figure 2. 20 (a) and (b) demonstrate the 16-relative attenuation, phase states and time delay states respectively, while their RMS errors are shown in Figure 2. 20 (c); they are generated by including the effect of R_{par}. The design consists of two separate sections. Therefore, the 16 different states are generated by extrapolation. The presented results show that the attenuator can have a 4-bit of operation with a lower than 0.5 dB RMS attenuation error and a maximum 1.8^0 of RMS phase error, which verifies the block's

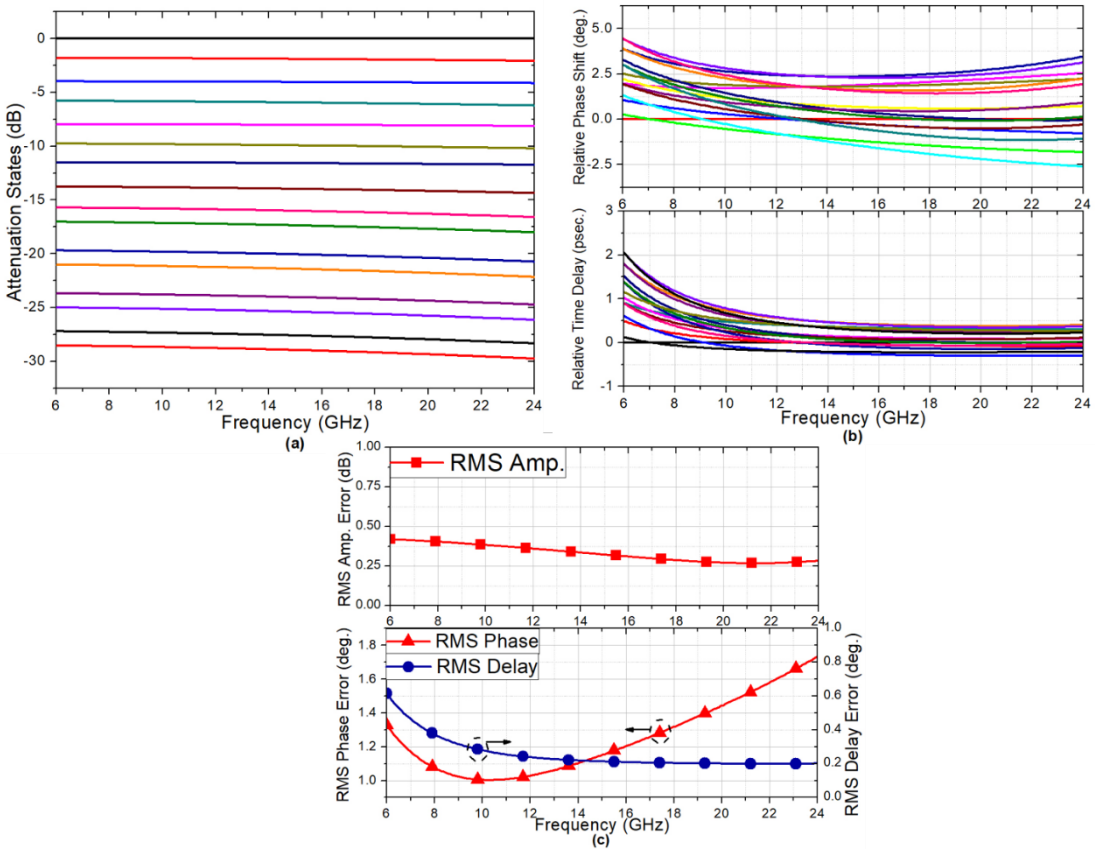


Figure 2. 20 The 16 a) attenuation states, b) relative phase and time delay states, and c) calculated RMS amplitude, phase and delay errors of the 4-bit attenuator.

compatibility to the wideband core-chip. The relative phase shifts of the attenuator are converted to time delays. As shown in Figure 2. 20, the maximum RMS delay error of the attenuator is 0.4 psec. at 8 GHz; 1.94 psec. is equivalent to 5.6^0 of phase shift at 8 GHz. This result confirms that the presented attenuator can also be introduced to a timed-array system, as the BDA. The design is submitted for fabrication on December'18, and the shipment will be done on September'19.

2.5. Phase Shifter

The beam steering mechanism of a radar system is enabled by the PS in the core-chip, as mentioned in section 1.1. The main purpose of an ideal PS is to vary the phase of the incoming signal without changing its magnitude. Various phase controlling methods

can be categorized into two groups; analog and digital phase shifters. The analog phase shifters can produce several phases for a defined phase range. The digital phase shifters generate phase states considering a dedicated step-size. In other meaning, the step-size of a binary-step PS is calculated by dividing 360^0 to 2^N, where "*N*" stands for the number of the bits. For a 4-bit PS, 16 different phase states exist with a 22.5^0 of step size (also LSB). The RMS phase and amplitude errors are also basic metrics for the PS.

The core-chip targets 4-bit of phase resolution for a wide frequency range, which is challenging due to the technological limits. III-V based technologies have passives with high-Q factors. As a result, they can realize wideband low loss PS circuits with high resolution. Active PSs in III-V technologies, which are not common, are generally preferred to shrink the total area of the passive PS without sacrificing the resolution. In silicon technology, the passive PSs suffer from high substrate coupling, therefore they are highly lossy and have limited bandwidth. The active PS topologies, especially vector sum type PS (VSPS), are utilized to overcome the bandwidth and resolution limits in Si-based technologies with the expense of increased complexity, power consumption, noise and reduced dynamic range (Koh et al 2010).

The vector sum type PS is not appropriate for the wideband core-chip design, because it is unidirectional. Additional switch networks can be utilized to generate a bidirectional VSPS, as applied for the amplifiers in Figure 2. 8 (a) or (b). However, this approach might end increased area, power consumption and possibly increased insertion loss. Hence, the desired resolution is planned to be achieved by passive structures. If all the bits are designed for a dedicated center frequency, the RMS phase error would be minimal only at a single point. This would result in a low RMS phase error for a limited bandwidth; the RMS phase error would have sharp rising at other frequencies (Çalışkan et al 2014).

The filter type PS is one of the best candidates for the wideband core-chip among other passive examples. The switched line method suffers from a large area and high amplitude error, while the return loss of the load-line method will vary at different phase states (Sarkas et al 2010). Low-Pass (LP) and High-Pass (HP) networks can be utilized to succeed in an expected phase difference (Morton et al 2008), as shown in Figure 2. 21. HP and LP networks should be designed for + ϕ and - ϕ of phase difference respectively,

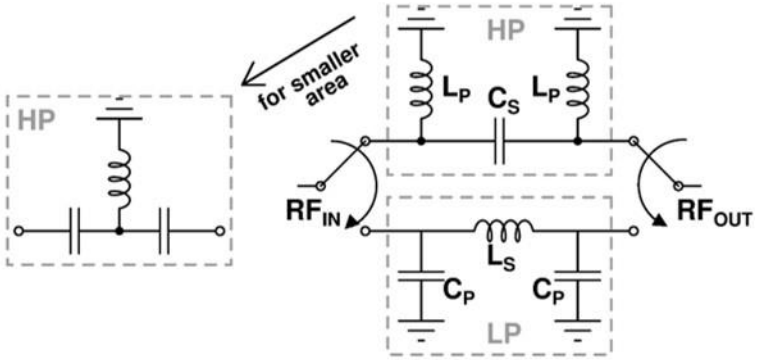


Figure 2. 21 Schematic view of a HP-LP type PS.

$$L_P = \frac{Z_L}{\omega\, tan\left(\frac{\phi}{2}\right)}\,;C_S = \frac{1}{\omega\, Z_L \sin(\phi)}\,;$$
$$L_S = \frac{Z_L sin(\phi)}{\omega}\,;C_P = \frac{tan\left(\frac{\phi}{2}\right)}{\omega Z_L} \qquad (11)$$

to conclude with a phase difference of 2ϕ. (11) demonstrates the expressions for the desired phase difference. It is obtained through the impedance calculations and the half-circuit model (Çalışkan et al 2014). Z_L stands for load impedance and ω is representing the angular frequency. The HP π-network has two inductors, which includes three inductors for a single PS bit. However, it can be converted to a T-type network by basic impedance transformation, to decrease the number inductors into two. A bypass path can be preferred as a filter, which might shrink the total area of the bit. Additionally, High-Pass (HP) and Low-Pass (LP) filters have similar phase behavior, which leads to a flat phase difference over frequency.

2.5.1. The Design Procedure of the PS

2.5.1.1. The Design of the Major Bits

The main target of the PS is to achieve a wideband 4-bit phase resolution, where the area is sacrificed for the desired performance. Instead of the HP-LP designs, the all-pass networks are favored to match the 16 GHz of bandwidth. The all-pass filter networks and their components' values are provided in Figure 2. 22. The required component values for HP-LP networks might not be feasible for some cases such as 22.5^0; i.e. 20 fF of C_P, and 5 nH of L_P 22.5^0 of phase difference. Therefore, a second-order filter network

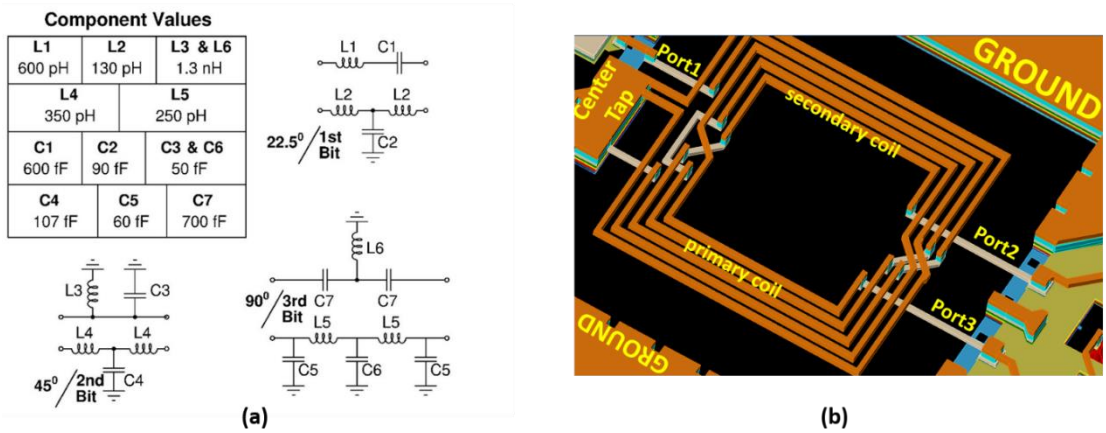


Figure 2. 22 (a) The block diagram of the filter networks with their component values. (b) The top view of the transformer.

is favored for the 90^0 phase shift (Liu et al 2016), while a center-taped transformer is preferred for the 180^0 of phase shift. These designs might result in an increased area, a price to pay for high RF features.

The RC poly-phase filters can also be an appropriate topology for the 3rd bit. The active phase shifters cascade transformer and poly-phase filters to generate accurate inphase-and-quadrature (I/Q) phase vectors. However, the order of the RC-filters should be increased for a 16 GHz of bandwidth, with the expense of an increased insertion loss. Alternatively, multiple transformers can be utilized to generate 90^0 of phase difference with the expense of increased area (Frye et al 2003). Considering the possible drawbacks of RC poly-phase filters and transformers, the all-pass filter networks are favored for the 90^0 of phase shift, as done for 1st and 2nd bits.

The transformers are favored for active PS designs due to their simplicity and almost flat 180^0 phase difference. For a transformer, the mutual inductance between coils (M) and coupling between windings (k_m) can be told as the two major metrics. Its insertion loss and impedance terminations highly dependent on these parameters (Long et al 2000). Different transformer architectures exist where each of them is designed by considering the capabilities of the implemented IC technology; i.e. the number of metals, and distance between top metal and substrate. Overlay type transformer can be a candidate for the PS, due to including two thick top metal layers in the implemented technology. However, one of the coils should be implemented in Top-Metal1 in the overlay method. This concludes an increased shunt capacitive effect and deteriorated bandwidth. The Rabjohn type

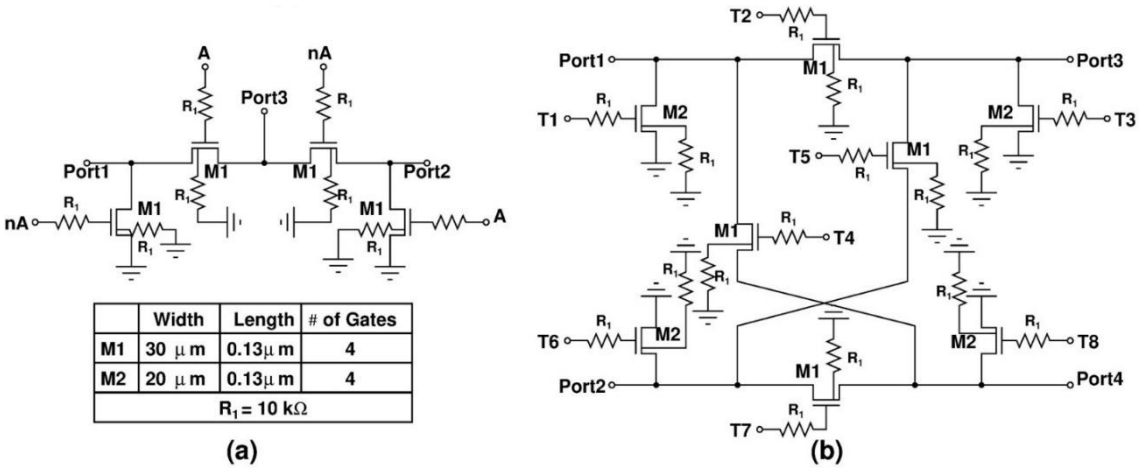
$$f_{pk} = \frac{R}{2\pi L_P \sqrt{1-k_m^2}} \quad (12)$$

transformer enhances the bandwidth by utilizing the Top-Metal 2 layer only. In the preferred technology, the distance between two Top-Metal 2 layers should be more than 2 µm, while the gap between top metals is about 2.8 µm. This results in a higher k_m, for the Rabjohn transformers compared to the Overlay type. As a result of its advantages at the frequency band of interest, the Rabjohn transformer is preferred as the balanced-unbalanced (balun) network for the PS with a 2:3 coil ratio. Figure 2. 22 (b) presents the 3D view of the designed transformer.

The impedance termination of the transformer can be determined by the primary coil as in (12) (Long et al 2000); f_{pk} stands for the frequency of interest, and R is the. L_P is behaving as a series inductor when one of its ports is grounded and the secondary coil is neglected. The inductance of the primary coil should be 860 pH for a 50 Ω matching around 20 GHz, where the imaginary part is neutralized by adding a series capacitor. The secondary coil is designed by considering the 2:3 ratio, and k_m. Additional shunt capacitors are added to the secondary coil ports for impedance matching. It should be noted that the transformer design requires iterative EM simulations, because of the high mutual coupling. Thanks to the symmetricity of the Rabjohn architecture, the physical and electrical centers of the secondary coil are almost the same. However, the turns of the coils caused a certain level of distance between the electrical center point and the nearest ground layer. The mentioned parasitic effect deteriorates balun performance dramatically. Hence, the balun layout is updated in a way that the center point is at the outer most ring. This method minimized the effect of the ground parasitic of the transformer.

2.5.1.2. The Switching Networks

The balun and filter networks presented in the previous section should be switched between each other accordingly, to end up with the desired phase difference. However, multiple switching network might conclude a high loss for the PS. Passive SPDT switches can be introduced between each bit, due to its simplicity and providing an adequate level of isolation between filters. When the loss of a passive SiGe BiCMOS SPDT switch is



	Width	Length	# of Gates
M1	30 μm	0.13μm	4
M2	20 μm	0.13μm	4
R_1 = 10 kΩ			

Figure 2. 23 The block diagram of (a) SPDT, (b) DPDT switches in PS.

considered, the insertion loss of a 4-bit PS would be higher than 15 dB, excluding the loss of the filters. This would affect the system performance dramatically and burden the amplifiers with a higher gain. As mentioned in section 2.2, the LC-resonator type or *λ/4* line-based SPDT switches can be preferred. However, they offer low loss for limited bandwidth in a large area (Davulcu et al 2017). Even if high insertion loss might be observed from the series-shunt SPDT switch, it is favored in PS design due to its simplicity, compact area, and zero power consumption. The SPDT switch designed for the PS is presented in Figure 2. 23 (a).

A 4-bit PS with eight SPDT switches would constitute a highly lossy sub-block. Hence, passive DPDT switches are decided to be utilized between filters. When two series-shunt type SPDT switches are cascaded with each other, the transmission line between filter networks is going to observe two series iNMOS devices. This ends up with a high loss for the PS, which can be lowered by preferring a DPDT switch as in Figure 2. 23 (b). The DPDT switch guarantees isolation by two shunt transistors on the signal path. The signal path formation for the DPDT is similar to the SPDT. For instance, the RF signal at Port2 can be transferred to Port3 by turning transistors T1, T5 and T8 on, while keeping remaining ones off. As mentioned in sections 2. 2 and 2. 4, the sizes of the devices are chosen to minimize its capacitive parasitic. Each signal path has two shunt and a series of a transistor. Therefore, the sizes of the shunt devices are selected as 20 μm, while series ones have a width of 30 μm. A 2-to-8 decoder is introduced for each DPDTs in the PS to simplify the control of the phase states. Similarly, the SPDTs are controlled through 1-bit of operation by a buffer network.

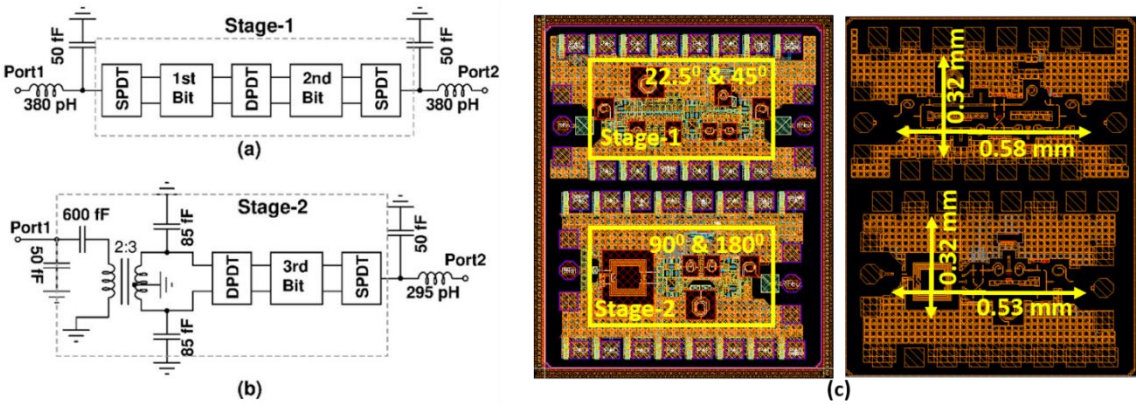


Figure 2. 24 The block diagram of the PS's (a) Stage-1, (b) Stage-2, (c) top-view.

2.5.1.3. The Order of the Bits

The insertion loss of the PS would exceed 15 dB, due to including multiple switches and highly lossy inductors. Therefore, the PS is divided into two separate sections for superior CC features as done for the attenuator. The first section ("PS Stage-1") is composed of 22.5^0 and 45^0 of phase shifting filters (1st and 2nd bits), while the Balun and 3rd bit are cascaded to form the second section ("PS Stage-2"). The matching networks (LC-tank circuit) added to the ports of both sections for a proper 50 Ω termination. Figure 2. 24 (a) and (b) presents the block diagram of the PS sections, while the layout view is shown in Figure 2. 24 (c). In total, the designed PS sections cover a 0.36 mm^2 area.

2.5.2. The Post-Layout Simulation Results

The EM simulations are done for both PS stages. Similar to the attenuator, R_{par} resistances that are scaled considering the iNMOS device size, are added to the PS. The design depends on reactive components. Therefore introducing parasitic resistances has a minor impact on the block's performance, compared to their effect on the attenuator. Figure 2. 25 summarizes the S-parameters of the PS stages. The insertion losses of the switches are close to 2 dB, which results in at least 6 dB of additional loss per stage. When the lossy reactive components considered, the insertion loss of the PS stages becomes about 10 dB at 16 GHz, as shown in Figure 2. 25 (a). Both PS sections have adequate impedance matching performance throughout the defined bandwidth.

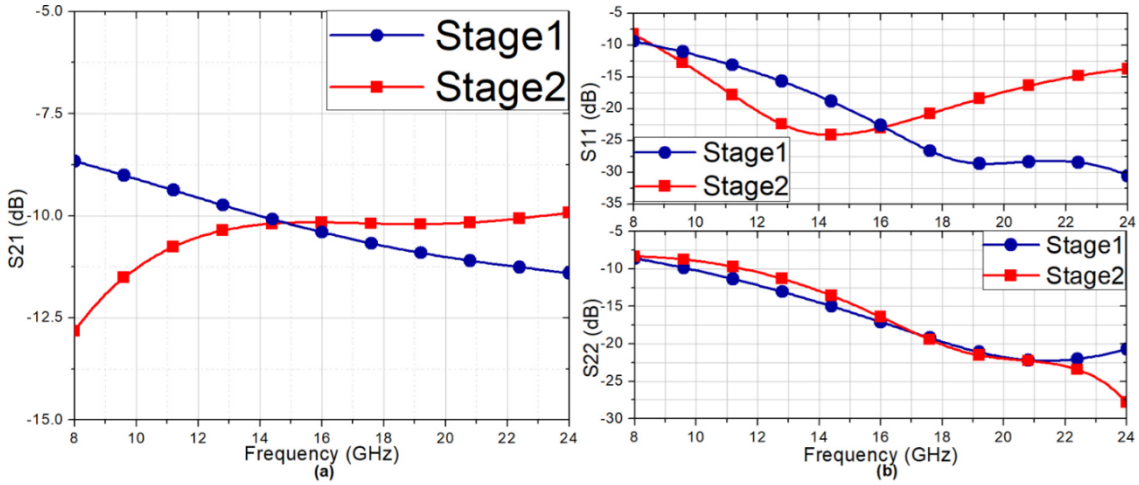


Figure 2. 25 The simulated (a) S21, and (b) S11-S22 of the PS stages.

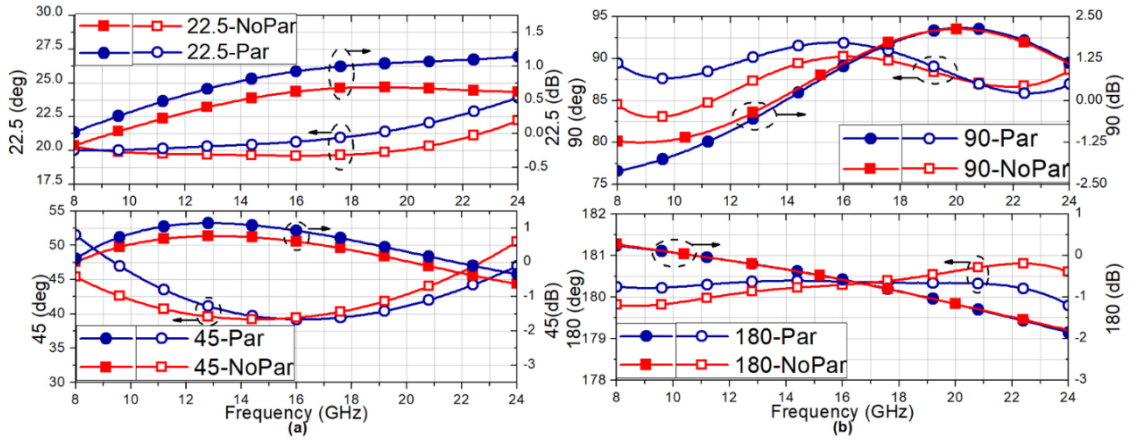


Figure 2. 26 The simulated major phase states and their amplitude errors (a) for Stage-1, and (b) for Stage-2, with (Par) and without (NoPar) the parasitic resistance.

Figure 2. 26 presents the post-layout simulation results of major PS phase states, including their amplitude errors. PS Stage-1 features demonstrated in Figure 2. 26 (a), while Figure 2. 26 (b) summarizes the obtained phase shifts from PS Stage-2. The stages are simulated with ("Par") and without ("NoPar") R_{par}, to show its effect on PS stages clearly. The RMS phase error of the PS is attempted to be lowered by preferring multiple center frequencies such as 12 GHz, 16 GHz, and 20 GHz. The 1st bit is tolerated with the increasing phase shift behavior of the 2nd bit, as can be seen from Figure 2. 26 (a). The center frequency is favored about 16 GHz for the 3rd bit, while the phase variation is minimized to ± 3.50. The 4th bit has ± 0.50 of variation over frequency, thanks to the balun topology. As a drawback, PS Stage-2 has higher amplitude errors compared to the PS Stage-1. Moreover, the R_{par} resistance has a minor impact on the performance of the PS bits, as shown in the related figures.

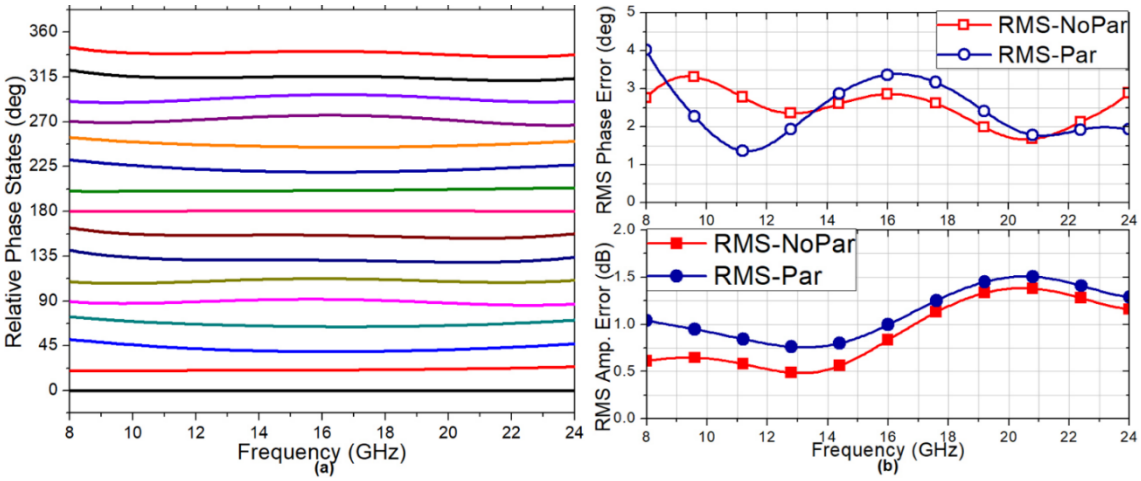


Figure 2. 27 The simulated (a) 16 phase states, and (b) Calculated RMS phase and amplitude errors of the PS.

The PS stages are designed independently because they are also included in the core-chip separately. Hence, each PS stage can generate 4 phase states; i.e. 0^0 (reference state), 22.5^0, 45^0, and 67.5^0 for Stage-1. The missing states are extrapolated by summing the existing ones, which are simulated with an ideal 50 Ω termination. Figure 2. 27 (a) presents the 16 separate phase states of the PS stages, while Figure 2. 27 (b) demonstrates their calculated RMS phase and amplitude errors with and without R_{par}. As shown, they are lower than 4^0 and 1.5 dB, which verifies that the design is compatible with the core-chip expectations. If a single center frequency was selected for all the filter networks, the PS would have a sharp phase error rising for the remaining parts of the band. As a result of preferring multiple center frequencies, the RMS phase error bandwidth is extended over the frequency. Moreover, a new bit might be added to the PS, due to having an RMS phase error lower than 5.6^0.

2.6. The Common-Chain (CC) of the Core-Chip

The common-chain (CC) is one of the most critical parts of the wideband core-chip, due to including BDA, attenuator, and PS, as in Figure 2. 28 (a). Each sub-block in the CC presented an adequate level of performance in a compact area. However, cascading them with each other to form CC is a crucial step in the core-chip design. An improper CC formation might result in degraded RF performances compared to the expectations

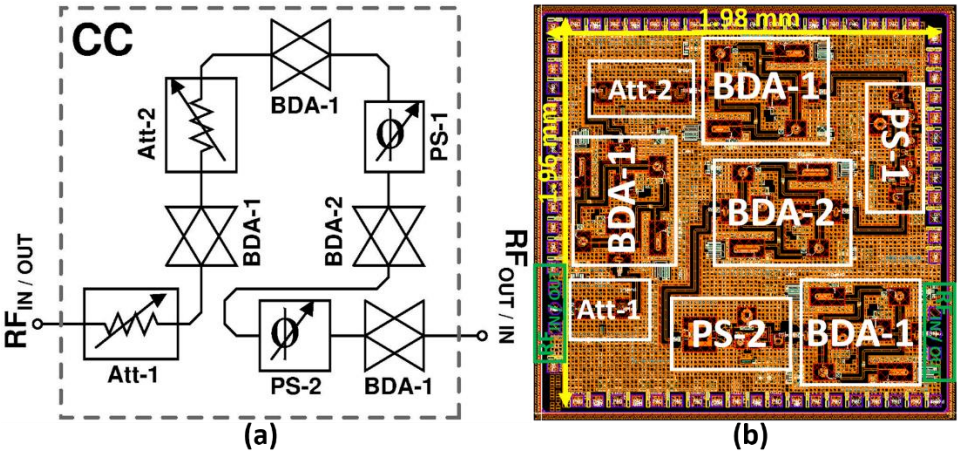


Figure 2. 28 (a) The block diagram of the CC. (b) The view of the CC.

from the sub-blocks. Figure 2. 28 (b) presents the layout view of the CC, that is submitted for fabrication in February 2019; the shipment time might be around November 2019. The chain covers 3.88 (1.98 x 1.96) mm^2 of an area (including pads) while dissipating about 55 mW of power during small-signal operation. In this section, the design procedure and the post-layout simulations of the CC are presented.

2.6.1. The Design Considerations of the CC

The insertion losses of the PS and attenuator are sacrificed to reach the desired bandwidth. Multiple BDAs are decided to be utilized in the CC, to tolerate the side-effects of the attenuator and PS. The BDA dissipates lower than 14 mW. Although additional BDAs would not be a burden for the CC, the area is sacrificed for improved performance. The average loss per PS and the attenuator section is close to 7 dB. Considering this, the number of the BDA in the CC is increased to four to suppress the lossy blocks' noise and to achieve the expected gain.

The PS and attenuator sections are simulated with an ideal 50 Ω terminations, which are replaced with non-ideal BDA impedances. Although the BDA's measured return loss performance is higher than 10 dB, its input-output impedances are varying over frequency. Because of the mentioned concern, the attenuator and PS's performances fluctuate. The PS and attenuator could be designed

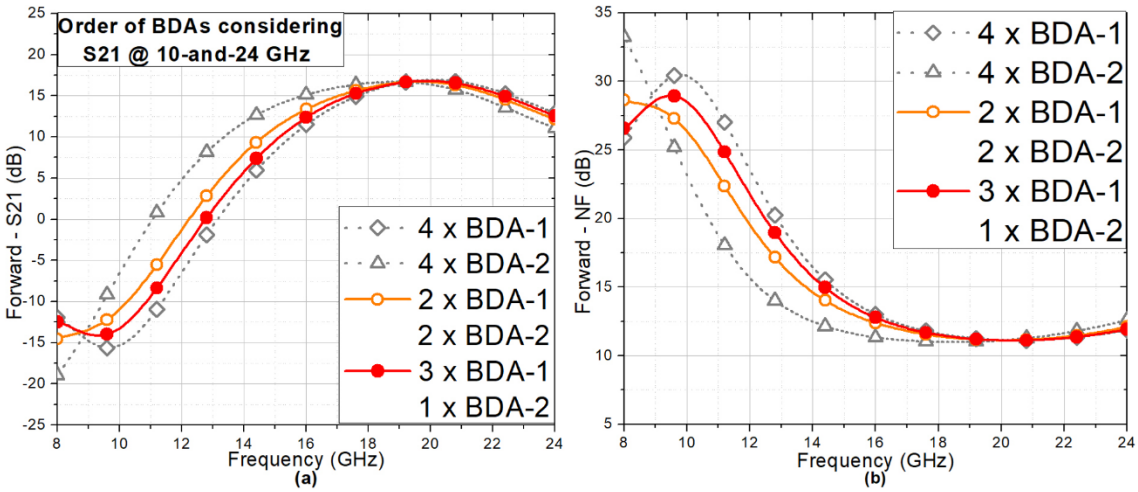


Figure 2. 29 The effect of various BDA-1 and BDA-2 combinations on (a) Forward-Mode S21, and (b) Forward-Mode NF.

regarding the BDA impedances if the core-chip expects a single band of operation. Unfortunately, this method does not apply to the multi-band design, due to not having a constant impedance from the BDA. The best way to avoid possible performance degradation from the attenuator and the PS is to terminate them with a BDA that has a better return loss. The non-linear gain behavior at 10 GHz for BDA-1 in section 2. 3 creates a trade-off between gain and phase/amplitude control for the CC. Figure 2. 29 (a) and (b) demonstrates the gain and NF performances of the CC for different BDA combinations during the forward-mode of operation. If four BDA-1s are favored in the CC, the gain drop at 10 GHz reaches close to 3 dB. This can be corrected by BDA-2 but the peak gain shifts around 1.5 GHz to lower frequencies. Hence, a combination of BDA-1 and BDA-2 is decided to be utilized in the CC. Introducing two BDA-1 and two BDA-2 into the CC results in an acceptable S21. However, this might lead to a poor amplitude and phase resolution scenario, due to terminating the related sections with the BDA-2. Therefore, cascading three BDA-1 and one BDA-2 with the remaining sub-blocks is preferred. Within this combination, the gain drop at 10 GHz is lowered down to 1.5 dB. A similar statement can be done for NF of the CC shown in Figure 2. 29 (b). It should be noted that the high NF of the CC is going to be suppressed by the LNA.

The order of the BDAs and attenuator/PS sections are a critical milestone for the CC. The attenuator sections are sensitive to the impedance variations, due to having lower return losses. Therefore, two BDA-1s are placed in between the attenuator sections, where

BDA-2 is placed in between the PS sections. The output of the LNA would saturate the first BDA in the CC. Hence, a lossy block (Att-1) is placed before the BDA-1. The PS stages are not favored for this purpose, due to their high loss (so high noise for the RX). The signal direction is enabled through the SCU units integrated to each of the BDAs, as stated in section 2. 3.

The floorplan of the CC is done by considering the compactness of the layout. The CC is going to be functional for both signal directions, while the measured BDA presents high isolation between forward-and-reverse mode of operations. However, the input of the CC is the output of the LNA and SPDT. When the power levels are considered, the distance between RF lines should be analyzed carefully because of having a compact area. The transmission lines of the left-most BDA-1 are close to the reverse-mode BDA-2. This can cause an oscillation problem for high RF power levels. For that purpose, deep-trench-isolation (DTI) layers are introduced between BDA-1 and BDA-2, to improve the isolation between amplifiers.

Each block that is submitted for fabrication includes two 5 pF of DC blocking capacitors. As mentioned, they have dramatic impacts on higher frequencies due to severe shunt parasitic capacitance. This problem is a consequence of the wide bandwidth expectation. The CC does not require additional DC isolation between blocks, because the PS and attenuator sections will be cascaded with the BDAs. The BDAs have series DC blocking capacitors that are also utilized as matching components. Removal of the unnecessary capacitors would improve the CC performance; the CC terminals are still isolated from DC.

2.6.2. The Post-Layout Simulation Results

Figure 2. 30 demonstrates the post-layout S-parameter simulations of the CC for both signal directions; the reference states of the attenuator and the PS are used during simulations. The EM simulation of the CC would give unphysical results or conclude with failure, due to its complex nature. Hence, the post-layout extractions and EM models of the blocks and transmission lines between blocks are introduced to the simulator separately, instead of simulating the whole CC. As shown in Figure 2. 30 (a), the CC

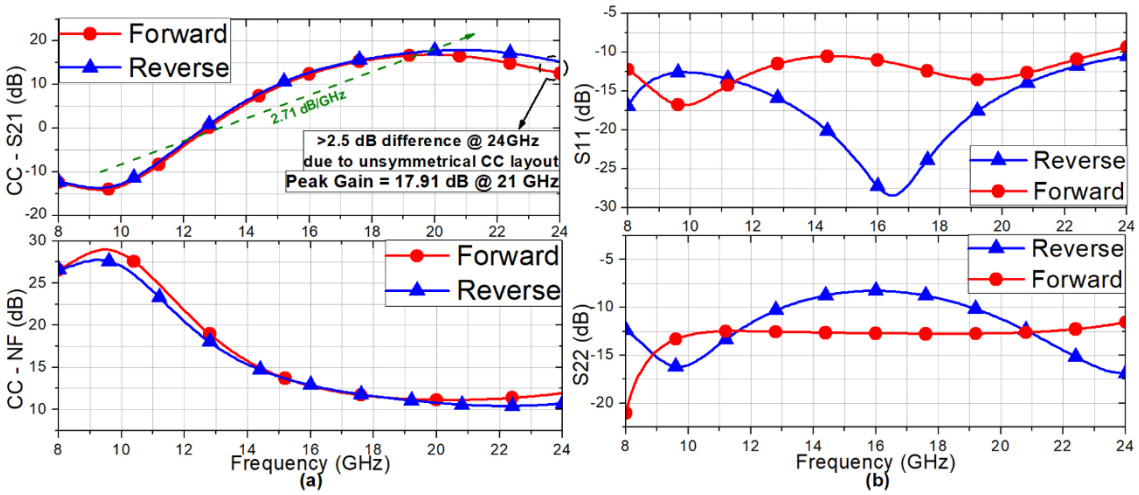


Figure 2. 30 (a) The forward-and-reverse mode S21 and NF performances of the CC. (b) The impedance matching performances of the CC for both signal directions.

presents almost identical gain and NF characteristics for both signal directions. The path has a 17.91 dB of peak gain at about 21 GHz, with a + 2.71 dB/GHz of a gain slope.

The compactness of the core-chip is one of the most significant targets, which also leads to a dense CC. Hence, the floorplan of CC is done by neglecting the symmetricity of the layout. The transmission lines added between blocks caused a performance variation between forward-and-reverse mode operations, especially after 20 GHz. The same performance for both signal directions could be achieved by sacrificing from the compactness. Figure 2. 30 (b) presents the CC's impedance matching for both signal directions. Independent from the unsymmetrical layout, the terminations of the CC vary due to having different blocks in the input-and-output terminals, which are the Att-1 and the BDA-1, respectively. Normally, the S11 of the forward-mode and the S22 of the reverse-mode of CC should be identical because they belong to the same block, Att-1. The variation on the defined term is a consequence of BDA-1's forward-reverse mode difference. This also affects the amplitude and phase controls of the CC, as will be explained.

Figure 2. 31 and Figure 2. 32 demonstrate a comparison of the simulated major attenuation and phase difference states of the CC. As mentioned before, the terminations of the blocks vary over frequency. This caused notable fluctuations, which are minimized with proper BDA-1 and BDA-2 ordering. 4-and-8 dB of attenuations in Figure 2. 31 are

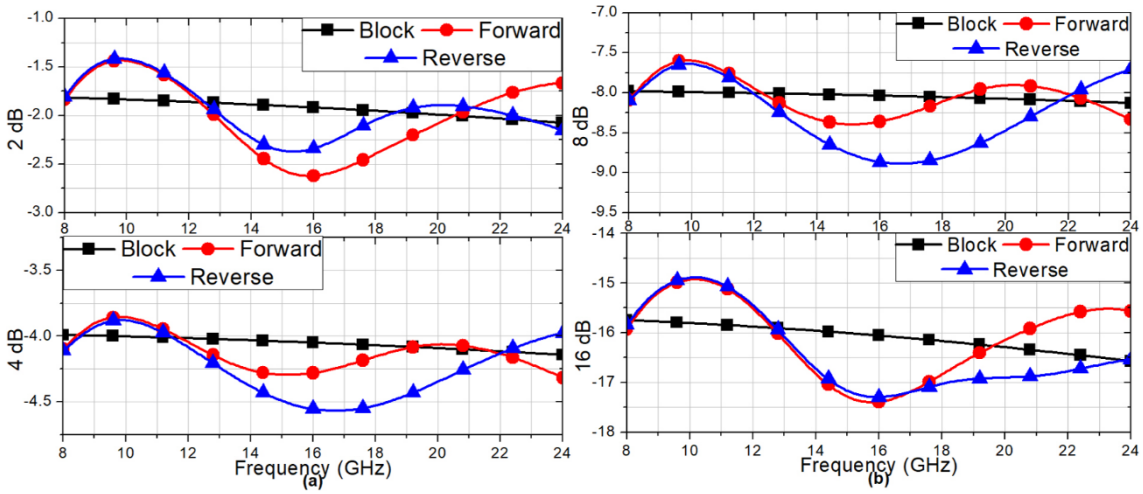


Figure 2. 31 Comparing the block level and the CC forward-reverse mode performances of (a) 2-and-4 dB, (b) 8-and-16 dB attenuations.

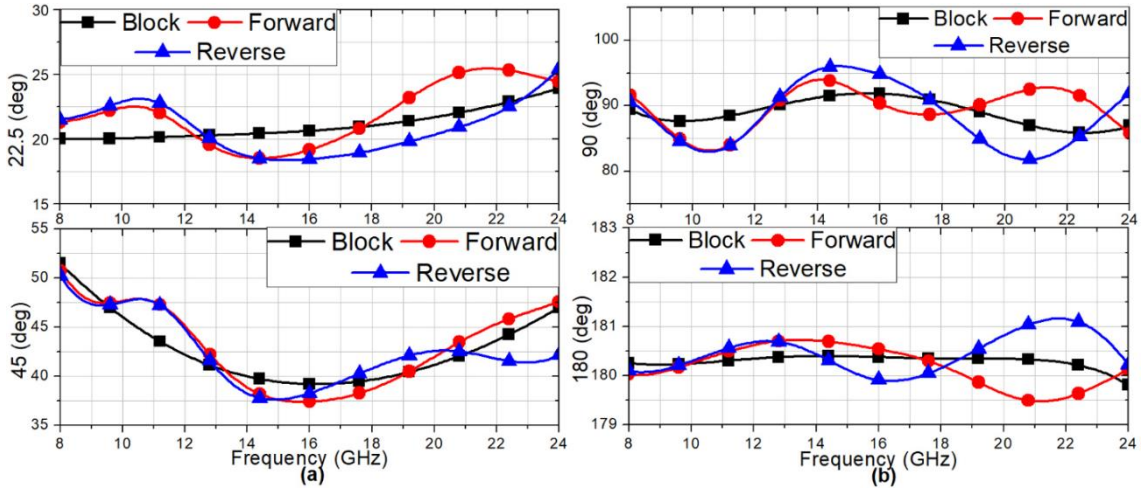


Figure 2. 32 Comparing the block level and the CC forward-reverse mode performances of (a) 22.5^0-and-44.5^0, (b) 90^0-and-180^0 phase differences.

obtained from Att-1, which is the reason for observing similar variations. A similar statement can be done for Att-2 (2-and-16 dB). The variations differ for forward and reverse modes after 16 GHz, due to the unsymmetrical layout. Figure 2 .32 presents the major phase states of the CC. The fluctuations in phase states are smaller compared to the attenuation states, due to providing better impedance terminations.

Figure 2. 33 and Figure 2. 34 show the phase and attenuation states of the CC including their RMS phase and amplitude errors, respectively. The CC succeeds in achieving 4-bit of phase and amplitude control with a positively sloped gain and low power dissipation in a compact area. Its RMS errors are simulated lower than 5.6^0 and 0.8

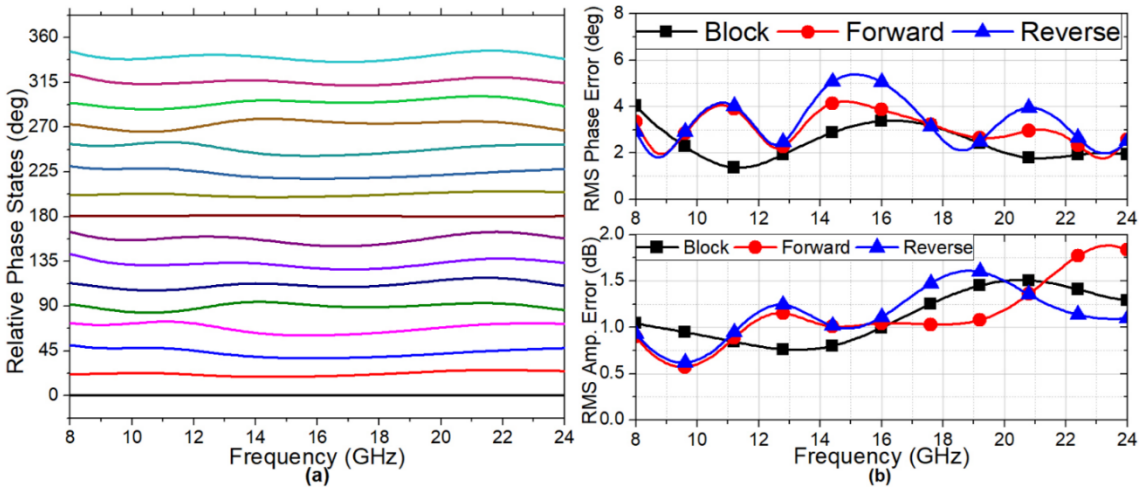


Figure 2. 33 (a) The relative phase states of the CC during forward mode. (b) The RMS phase and amplitude errors obtained during phase control of the CC for both signal direction, compared with block level performance.

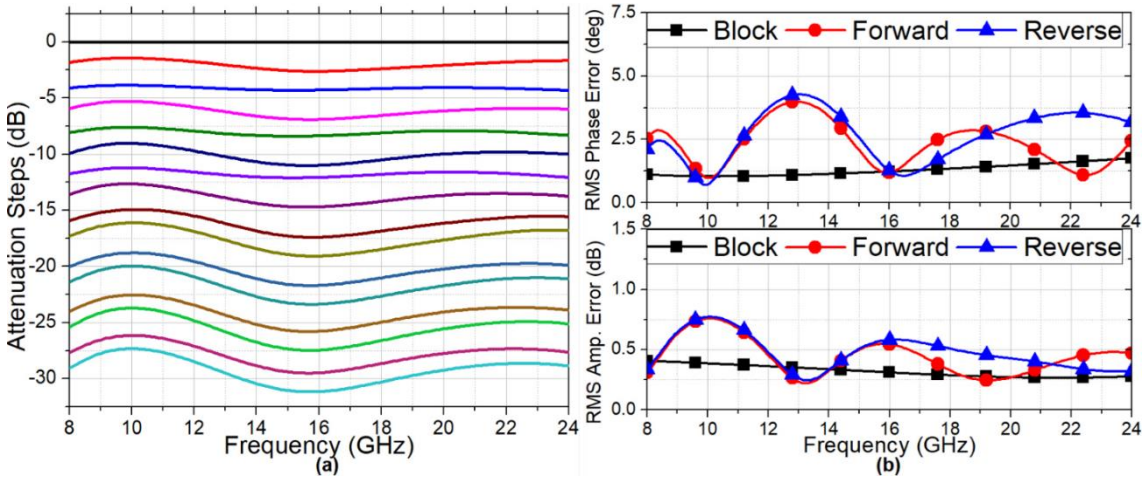


Figure 2. 34 (a) The relative attenuation states of the CC during forward mode. (b) The RMS phase and amplitude errors obtained during amplitude control of the CC for both signal direction, compared with block level performance.

dB during phase and amplitude controls, respectively. The NF of the CC is going to be suppressed by the LNA. The simulation results confirm that the CC has an adequate level of performance for additional phase and attenuation bits. To the best of my knowledge, the presented bidirectional CC (so-called multifunctional chip) achieved the best positively sloped gain-bandwidth performance with low power consumption in a compact area. Moreover, the recent results show that the presented 4-bit of phase and amplitude control can be improved due to having low RMS phase and amplitude errors, respectively.

2.7. Low Noise Amplifier (LNA) and Medium Power Amplifier (MPA)

LNA and Medium Power Amplifier (MPA) are the two unidirectional front-end amplification blocks of the presented wideband core-chip. LNA dominates the gain and NF of the RX, while MPA is responsible for the gain and output power of the TX. The prior aim of both amplifiers is to have a wide operating frequency. Therefore, some of the remaining features are relaxed for succeeding the desired RF performance, such as output power.

2.7.1. The Design Procedure of a Wideband LNA

Various methodologies can be applied to improve the bandwidth of an amplifier. As mentioned in the section. 2. 3, distributed amplifiers can be considered as one approach to enhance the BW by sacrificing the area and power consumption. A resistive feedback mechanism can also be preferred for wide operation bandwidth with the expense of increased NF and decreased gain (Saha et al 2012, Chen et al 2010). The wideband T/R core-chip includes lossy and noisy PS and Attenuator blocks. Hence, LNA should have high gain throughout the bandwidth to tolerate their effects. As a result, the resistive feedback approach is not an appropriate design method for the desired LNA. A non-resistive feedback mechanism demonstrated in (Hu et al 2004), but it suffers from mismatched input terminal and high NF. The conventional noise-and-power matching technique can be favored, but it results in a narrow bandwidth. When a single band of operation is concerned, LNA designs that have NF between 1.2 - 1.4 dB is presented at X-Band (Kuo et al 2006, Kanar et al 2014). Regarding the limits of the mentioned works in the literature, a new LNA design methodology should be applied for achieving wide bandwidth without sacrificing the gain and NF.

The generally favored simultaneous noise-and-power matching technique depends on utilizing an emitter degeneration inductor and a series base inductor. The bias point of the HBT is chosen for the lowest minimum NF (NF_{min}) condition, where their sizes are selected to match the optimum source resistance to 50 Ω as shown in (13). When the

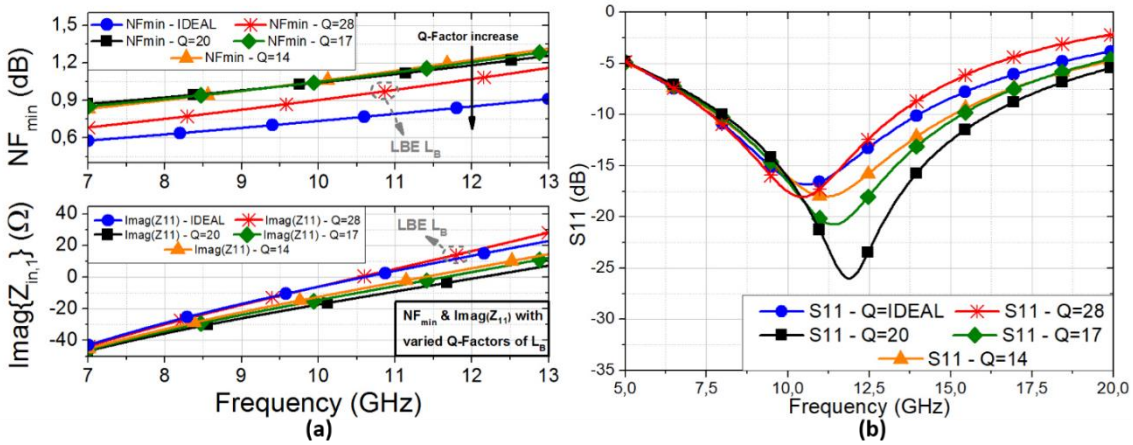


Figure 2. 35 The effect of the L_b on (a) NF_{min} and Imag $\{Z_{in,1}\}$, (b) S11 of a conventional amplifier, (with various Q-factors).

$$F = F_{\min} + \frac{R_n}{G_S}\left[\left(G_S - G_{S,opt}\right)^2 + \left(B_S - B_{S,opt}\right)^2\right] \tag{13}$$

$$Z_{in,1} = \frac{g_m L_e}{C_\pi} + j\omega L_e + \frac{1}{j\omega C_\pi} \tag{14}$$

amplifier's input impedance ($Z_{in,1}$) in (14) is analyzed, its real part is can be determined by an emitter degeneration inductor; *gm* stands for the transconductance of the HBT and a capacitive effect is assumed for Z_π. The imaginary part of the $Z_{in,1}$ and the susceptance (B_s) of the F is neutralized by the series base inductor (L_b), which is the reason for mentioning this method as simultaneous noise-and-power matching technique. Unfortunately, this approach highly depends on the Q-factor of the on-chip inductors. Figure 2. 35 (a) and (b) present the impact of the *Lb*'s Q-factor on NF_{min}, Imag $\{Z_{in,1}\}$ and S11 of the amplifier. As shown, non-ideal L_b deteriorates NF and wideband performances of the amplifier. More importantly, the design performance is being limited to a single band of operation which conflicts with the expectations of the presented core-chip.

The large-sized transistors, which are chosen considering the noise match, create low impedance between the base and collector terminals of the HBT in a CE amplification stage. As a result, the input and output impedances of the stage can be matched simultaneously by the emitter degeneration inductor and an output matching network. The described methodology improves the bandwidth due to the removal of a frequency dependent component, L_b. This is also verified through calculations by utilizing the small-signal model in Figure 2. 36 (a). The analyses are done for a CE amplifier because the

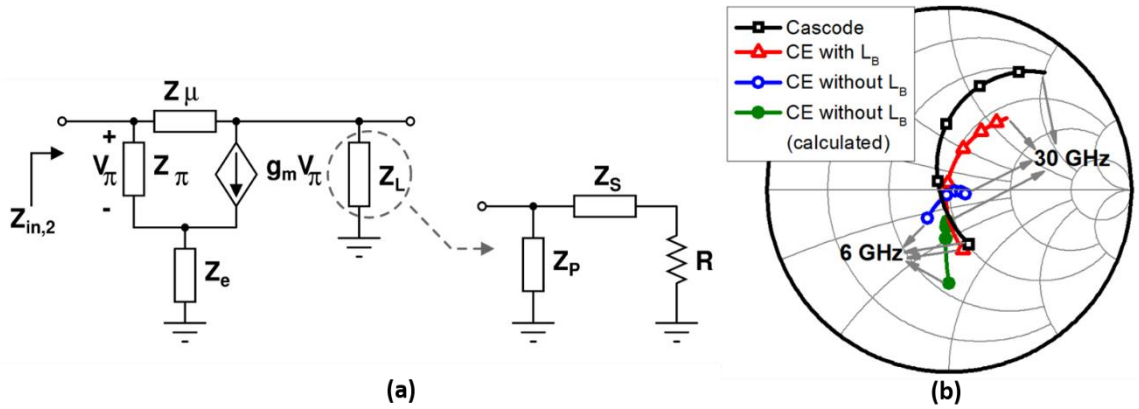


Figure 2. 36 (a) The small signal model of a CE amplifier. (b) The input impedance comparison of the three different amplifier topologies and calculated $Z_{in,2}$.

cascode topology cancels the Miller effect (so Z_μ). Z_μ is assumed to be capacitive (C_μ) taking the size of the devices (low r_π) into account. Additionally, Z_e and Z_p are considered as inductive, where Z_s is capacitive. These assumptions are done by regarding an emitter degeneration inductor and a basic LC-tank circuit for the output terminal. The new design method's input impedance ($Z_{in,2}$) is presented in (15). As shown, the impedance can be matched to 50 Ω by selecting L_P and C_S properly. L_P should be chosen as high as possible to dominate the R^2C_S term, which suppresses the negative imaginary. (15) can be simplified by considering the frequency of interest as (16) and (17), to calculate the component values easily. The analyses are also verified through simulations. Figure 2. 36 (b) compares the described method with conventional cascode and conventional CE amplifiers. As proved, the presented design procedure improves the BW of an amplifier.

The mentioned design procedure also enhances the noise performance of the amplifier. The thermal noise factors of the described method (F_1) and conventional CE

$$Z_{in,2} \cong \frac{g_m L_e}{C_\pi}\left(1-\frac{C_\mu}{C_\pi}\right)-\frac{g_m C_\mu (R^2 C_S - L_P)}{\omega^2 L_P C_S C_\pi^2}$$
$$+\frac{1}{j\omega C_\pi}\left[1+\frac{\omega^2 g_m^2 C_\mu L_e\left(L_e+\frac{R^2C_S-L_P}{\omega^2 L_P C_S}\right)}{C_\pi}\right]+j\omega L_e \quad (15)$$

$$C_S \cong g_m C_\mu \Re\{Z_{in,1}\} \quad (16)$$

$$\Re\{Z_{in,2}\} \cong \Re\{Z_{in,1}\}\left(1-\frac{C_\mu}{C_\pi}\right) \quad (17)$$

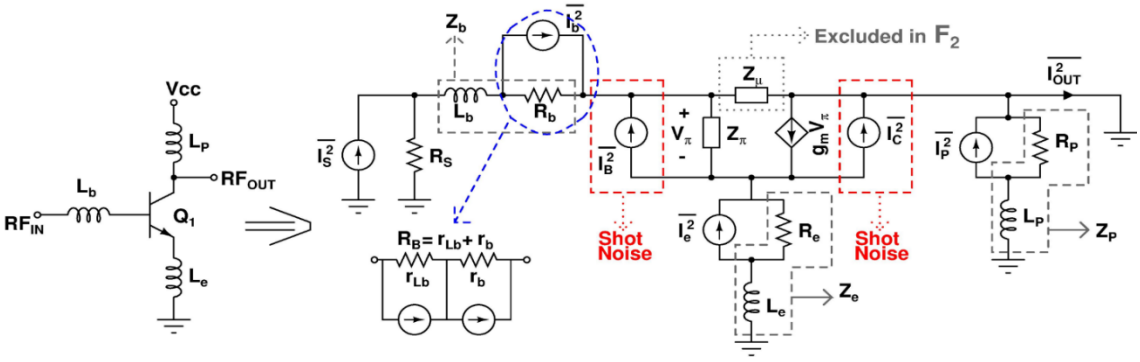


Figure 2. 37 Small signal model of the CE amplifier with noise sources.

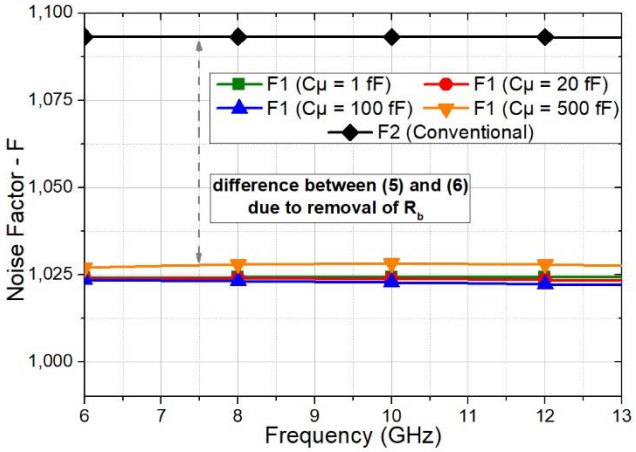


Figure 2. 38 Calculated F_1 and F_2 in (5) and (6) for various Z_μ values.

$$F_1(\omega) \cong 1 + \frac{r_b}{R_S} + \frac{R_e}{R_S}\left[\frac{R_S + r_b + g_m Z_\pi (R_S + r_b + Z_\mu)}{Z_\pi + Z_e + g_m Z_\pi (Z_e - Z_\mu)}\right]^2 + \frac{R_P\left(Z_\mu^2 (R_S + r_b)^2 + (r_b + R_S + Z_\mu)^2 [(g_m Z_\pi + 1) Z_e + Z_\pi]^2\right)}{Z_P^2 R_S [Z_\pi + Z_e + g_m Z_\pi (Z_e - Z_\mu)]^2} \quad (18)$$

$$F_2(\omega) \cong 1 + \frac{R_b}{R_S} + \frac{R_e}{R_S} + \frac{R_P [g_m Z_\pi Z_e + Z_e + Z_\pi + Z_b + R_S]^2}{(g_m^2 Z_\pi^2 R_S) Z_P^2} \quad (19)$$

amplifier (F_2) are calculated as in (18) and (19) respectively, by utilizing the small-signal in Figure 2. 37**.** The shot noise effects are excluded due to being uncorrelated with the thermal noise sources. In the conventional approach, the series base resistance is a consequence of the summation of the L_b's parasitic resistance (r_{Lb}) and HBT's base resistance (r_b). The noise of the CE amplifier is going to be lower by favoring the described design technique, due to the removal of the L_b. Figure 2. 38 compares the calculated F_1 and F_2, and it is verified that the noise performance is improved by excluding the resistive effect. C_μ can also be optimized for lower noise performance.

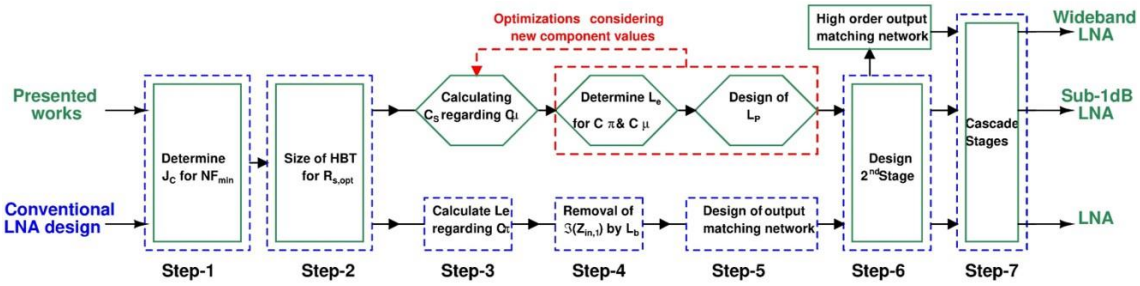


Figure 2. 39 The design flows for the described and conventional methods.

The design flow for the described approach and the conventional method is summarized in Figure 2. 39. As in the conventional design procedure, the bias conditions and the size of the devices are determined by considering the noise performance. The largely sized HBTs are going to create a high C_μ, which enables an impedance matching without requiring L_b. The output matching for the CE amplifier is done, where the C_S is determined by C_μ as in (16). The load impedance should satisfy the $L_P > R^2C_S$ condition to minimize the imaginary part of $Z_{in,2}$. L_e is decided by considering C_μ and C_μ. After the design of L_P, an optimization between Step-3 and Step-5 might be required due to the low impedance node between the amplifier terminals. When the desired level of impedance matching is achieved, the design of the second stage (Step-6) can be done. It is designed by following the conventional steps for the cascode amplifier. If wideband performance is desired a higher-order matching network is utilized for the output terminal.

2.7.2. The Measurements of the Sub-1dB and Wideband LNA

Two different amplifiers are designed to demonstrate the impact of the new design procedure on various aspects; one optimized for a low noise performance (sub-1dB LNA), while the other one targets wideband performance (wideband LNA). They favored two-stage amplification for a higher gain profile. The first stage (CE stage) is designed by the explained design procedure, where the second stage favored the conventional cascode design for higher gain and stability. Both sub-1dB and wideband LNAs in Figure 2. 40 are designed by following the same design steps. The high-order matching network of the wideband LNA is the difference between two amplifiers. To the best of my knowledge, the measured sub-1dB LNA achieved the best NF and gain performances (shown in Figure 2. 41 (a) and (b)) in SiGe BiCMOS technology. Similarly, the wideband

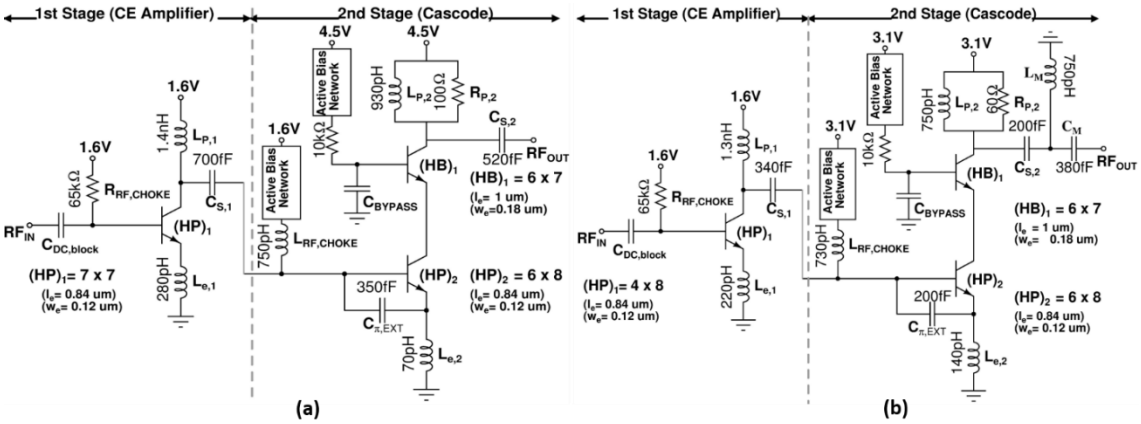


Figure 2. 40 The schematic views of (a) the sub-1dB, and (b) the wideband LNAs.

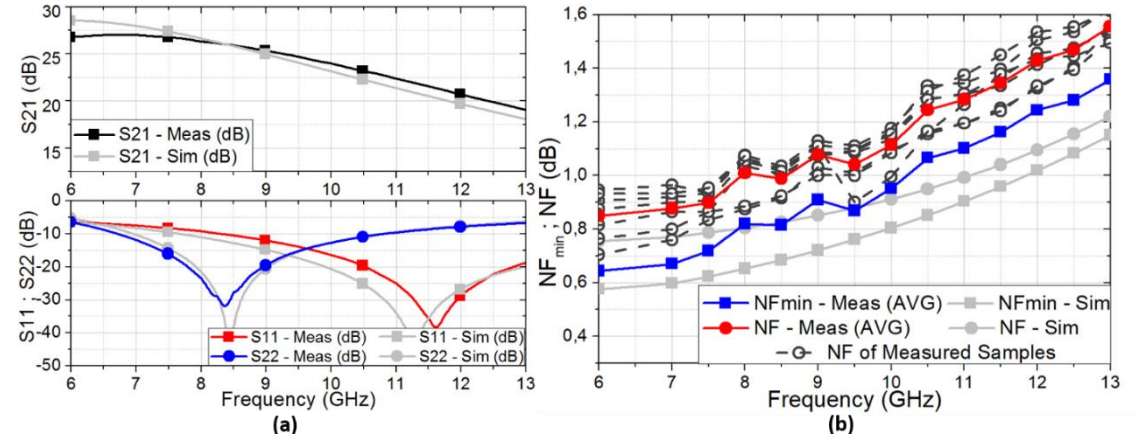


Figure 2. 41 The sub-1dB LNA's (a) S-parameters, (b) NF_{min} and NF.

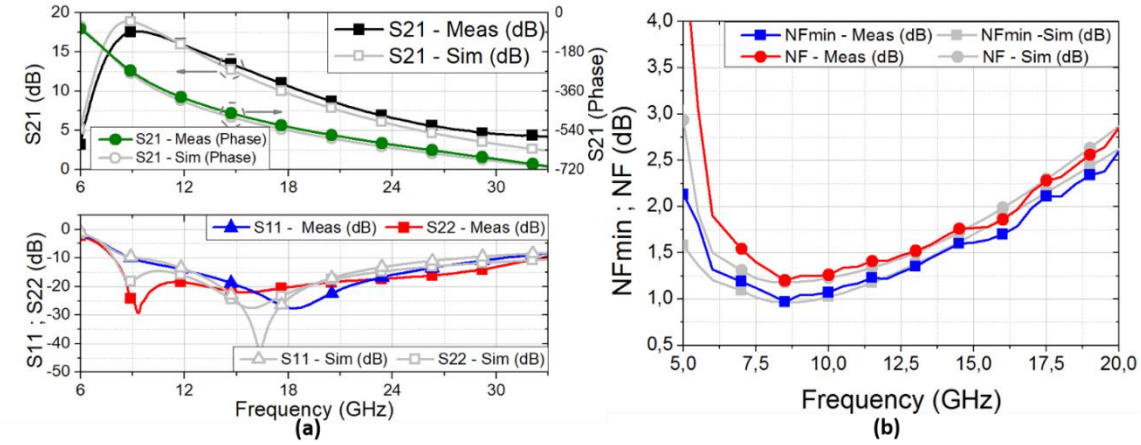


Figure 2. 42 The wideband LNA's (a) S-parameters, (b) NF_{min} and NF.

LNA realized the lowest NF in the literature that targets similar bandwidth and gain. Figure 2. 42 (a) and (b) presents the simulated-measured S-parameters and NF of the wideband LNA, respectively. A wideband amplifier should provide an almost flat output power for the defined bandwidth. Figure 2. 43 shows the input-referred compression point (IP1dB) and input-referred third-order intercept point (IIP3) of the wideband amplifier. As presented, the wideband LNA provides 5-to-8 dBm of OP1dB performance

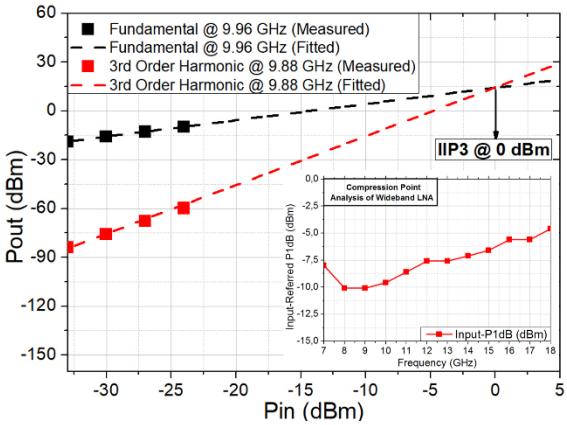


Figure 2. 43 The wideband LNA's measured IIP3 and IP1dB performances.

Table 2. 4 Comparison of the Sub-1dB LNA with similar works in the literature

	Tech.	Freq. [GHz]	NF [dB]	Gain [dB]	IP_{1dB} [dBm]	Power [mW]	Area [mm^2]	FOM
Sub-1dB LNA	0.13µ SiGe	8.5	0.98	26	-17.3	62	0.795	0.20
(Manohar et al 2014)	0.15µ pHEMT	10	1	28	-20	80	-	0.12
(Yau et al 1994)	0.25µ GaAs	10	1.1	17	-	-	9.362	-
(Kuo et al 2006)	0.13µ SiGe	10	1.36	19.5	-10	15	0.526	1.71
(Lohmiller et al 2017)	0.18µ SiGe	10	1.25	24.2	-19	32.8	0.458	0.18
(VIPER-RF 2015)	pHEMT GaAs	9	1	23	-7.5	240	1.5	0.36
(Sayginer et al 2016)	0.1µ InP	9.8	1.4(min.)	9	-	0.6	1.8	-

Table 2. 5 Comparison of the wideband LNA with similar works in the literature

	Tech.	Freq. [GHz]	NF* [dB]	Gain [dB]	BW_{3dB} [GHz]	BW_{RL} [GHz]	Gain Var./BW [dB/GHz]	IP_{1dB} [dBm]	Power [mW]	Area [mm^2]
WB LNA	0.13µ SiGe	8 - 20	3	14	4	12$^{\downarrow}$	0.7	-7.5	48.5	0.69
(Saha et al 2012)	0.13µ SiGe	3 - 26	6.5	9	23	20	0.04	-5.6	33	0.48
(Chen et al 2010)	0.2µ GaN	1 - 25	4.6	13	24	23	0.125	4.5	900	1.44
(Inanlou et al 2014)	0.13µ SiGe	10 - 22	4.4	15.5	12	5	0.25	-37.5	4	0.68
(Howard et al 2012)	0.13µ SiGe	8 - 18	6	16	6.5	3.5	0.5	-25	37.4	0.1†
(Jeong 2018)	0.18µ SiGe	8 - 16	8.1	17.8	3	9	1.56	-11.7	42	1.17

* max. NF for defined range are presented. $^{\downarrow}$Actual RL BW is between 8-to-35 GHz. † area excluding pads

between 7-to-18 GHz, which confirm its compatibility with wideband systems. Table 2. 4 and Table 2. 5 presents a comparison of the mentioned designs with similar works in the literature. The presented results are published as a journal in "Transactions on Circuits and Systems I: Regular Papers", named as "Sub-1-dB and Wideband SiGe BiCMOS Low-Noise Amplifiers for X-Band Applications". The first stage (CE amplifier) is also

published (Early Access) as a letter in “Transactions on Circuits and Systems II: Express Briefs” as “Ultra Low Noise Amplifier for X-Band SiGe BiCMOS Phased Array Applications”.

2.7.3. The Simulation Results of the Wideband LNA

The described design procedure is implemented and the measurements verified its wideband and low noise performances. However, the designs are realized considering X-Band applications, where the upper limit is favored as 20 GHz. Therefore, the presented works should be redesigned considering the targets of the dissertation. The measured wideband and sub-1dB LNAs are one of the significant motivation sources of the implemented wideband core-chip design.

The wideband core-chip targeted mean 5 dB of NF and close to 20 dB of gain for RX. The LNA that is mentioned in the previous section can be favored in the wideband core-chip. When the performance of the CC is considered, the wideband LNA's gain should be 7 dB higher. Otherwise, the RX would exceed the 5 dB mean NF target. Therefore, a new wideband two-stage amplifier is designed as presented in Figure 2. 44. It is designed by following the design procedure stated in this section. The bias point of the CE amplifier is updated for an improved gain at higher frequencies. Additionally, the second stage is designed considering the slope of the CC and stability of the block.

The simulation results of the new LNA are presented in Figure 2. 45, which are obtained by utilizing the ideal lumped components except for the HBTs; estimated series parasitic effects for the lumped components are included. The wideband LNA achieved 20 dB of gain at 16 GHz with a low noise profile and an adequate level of impedance matching. The block dissipates 56.77 mW of power during small-signal operation. The design’s output power simulations are summarized in Figure 2. 46 (a) and (b). The block's OP1dB point at +10.55 dBm at 15 GHz. As shown in Figure 2. 46 (b), the variation of the OP1dB point over frequency is in the range of ± 2.5 dB. The presented LNA has a sharp negative gain slope, which is going to be compensated by the positive gain slope of the CC. When the simulation-measurement coherency of the presented blocks is

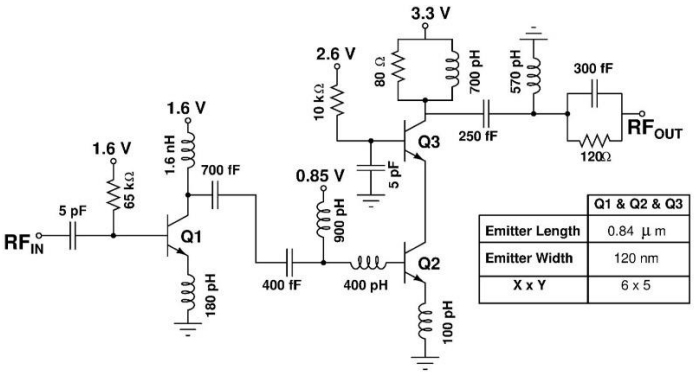


Figure 2. 44 The schematic view of the new wideband two-stage LNA.

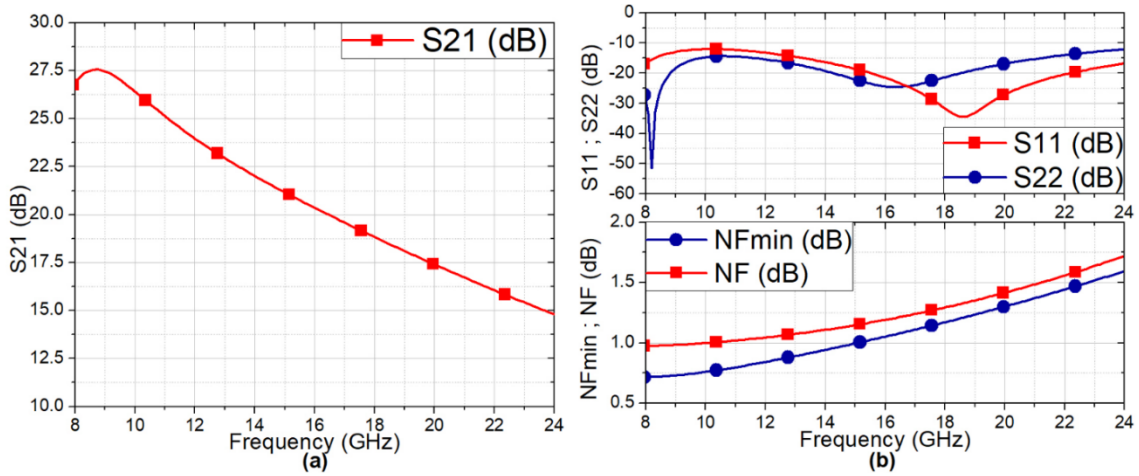


Figure 2. 45 a) The S21, (b) Input-output matching and NF of the LNA.

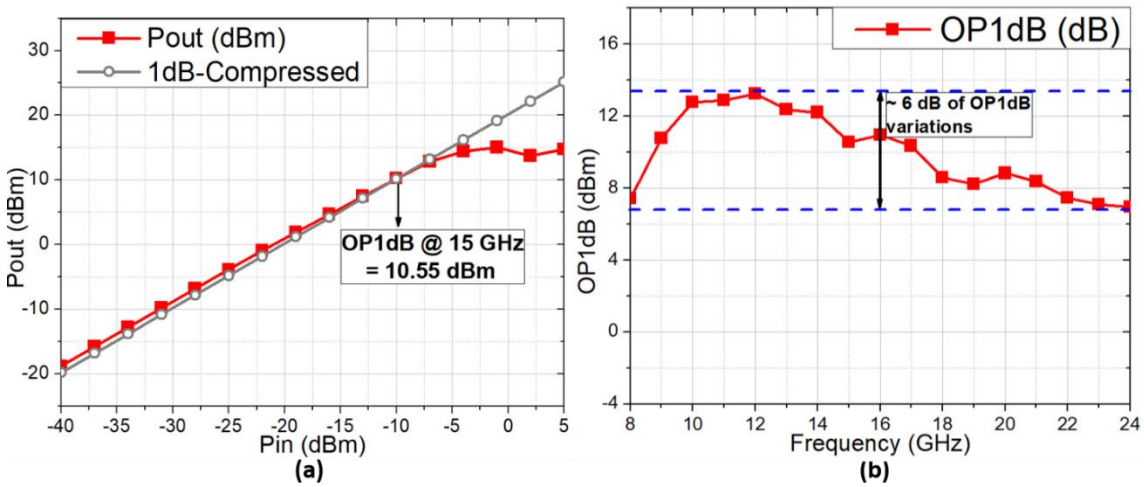


Figure 2. 46 OP1dB of the LNA (a) at 15 GHz, (b) at various frequencies.

considered, the wideband LNA is compatible with the wideband core-chip expectations.

The presented wideband LNA targets high gain in two-stage amplification. The first stage is a CE amplifier, which has a mismatched input impedance (unnaturalized imaginary part). Hence, stability analyses should be done carefully. When the S-

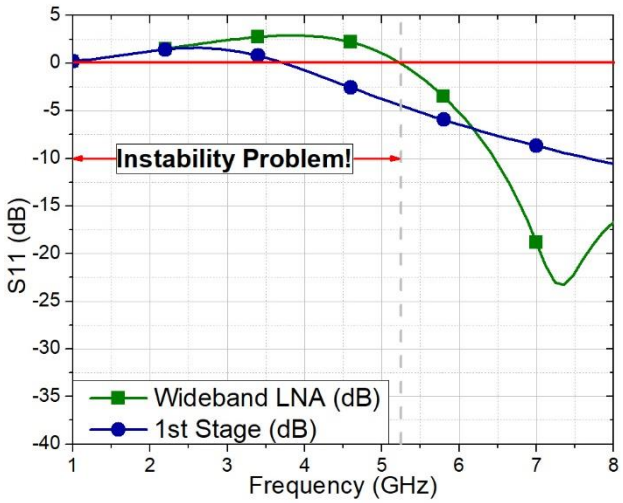


Figure 2. 47 The S11 of the CE stage and wideband LNA at low frequencies.

parameter simulations of the wideband LNA are extended to lower frequencies, a peak that extends above 0 dB, is observed for the S11 as in Figure 2. 47. This can be named as a stability problem. At the final two-stage design case, S11 exceed the 0-dB limit up to 5.2 GHz. This is a result of having a high gain and inappropriate terminal matching simultaneously. The S11 and S22 should be lower than 0 dB at all frequencies for unconditional stability. However, these results do not mean that the wideband LNA is unstable. It is still stable, but not unconditionally. Because of the mentioned concern, the design steps should be followed carefully. The problem can be solved by preferring a lower gain for the CE stage and higher NF (same for the core-chip). It should be also noted that the design includes several ideal components, such as inductors, which are going to be replaced with EM simulated custom-designed equivalents. This might suppress the described effect. The measured LNAs presented in section 2. 7. 2 also aimed for high gain, and both are unconditionally stable.

2.7.4. The Simulation Results of the Wideband MPA

The MPA has similar specifications with the LNA except for the output power. It should provide adequate performance for the core-chip, and its output power should not differ much in the operating frequency range. The impedance at the output terminal affects the maximum output power that an amplifier can achieve, which can be calculated by utilizing Load-Pull analysis. However, the impedance for maximum output power may

not be 50 Ω, which creates a trade-off between the frequency range and the output power. Hence, it is sacrificed to obtain a wideband-matched MPA with flat output power. (Harir et al 2014) presented 27 dBm of output power by using 0.18 µm SiGe HBTs and transformers with a poor impedance matching. The MPA of SÜMER group integrated a transformer to improve the matching performance and operating bandwidth throughout the X-Band by sacrificing area (Çalışkan et al 2016). When the measured performances provided in section 2. 7. 2 are considered, the wideband LNA is also appropriate for the MPA design, due to having an acceptable level of OP1dB flatness. The LNA's simulated output power can be improved further by updating design considerations from NF to output power. It should be also noted that if the presented core-chip will be cascaded with a GaN-based RF front-end, the MPA's output power should be close to 15 dBm. It is required to drive a PA that succeeds about 40 dBm output power with approximately 25 dB gain of linear gain. The simulations of the LNA are also utilized as the MPA to realize the presented core-chip.

2.8. 8-to-24 GHz Low Noise Bidirectional Core-Chip

In this section, the X-to-K band core chip's simulation results are provided. The block diagram of the design is presented in Figure 2. 48 (a). The simulations are done by regarding the possible performance variations, such as added parasitic resistive and capacitive effects, for the blocks that are not measured yet. These variations created different scenarios, which cause degraded gain, gain slope, NF and OP1dB of the wideband core-chip.

2.8.1. The RX Performance with New and Former LNA

The sub-blocks are designed by considering the wideband, low noise and compactness targets, to realize the wideband core-chip presented in Figure 2. 48 (a). The design procedures for the BDA and LNA are verified through measurements, where the attenuator, PS and CC sections are submitted for the fabrication. As mentioned in section 2. 7. 3, the LNA is redesigned in the schematic level, considering the operating range of

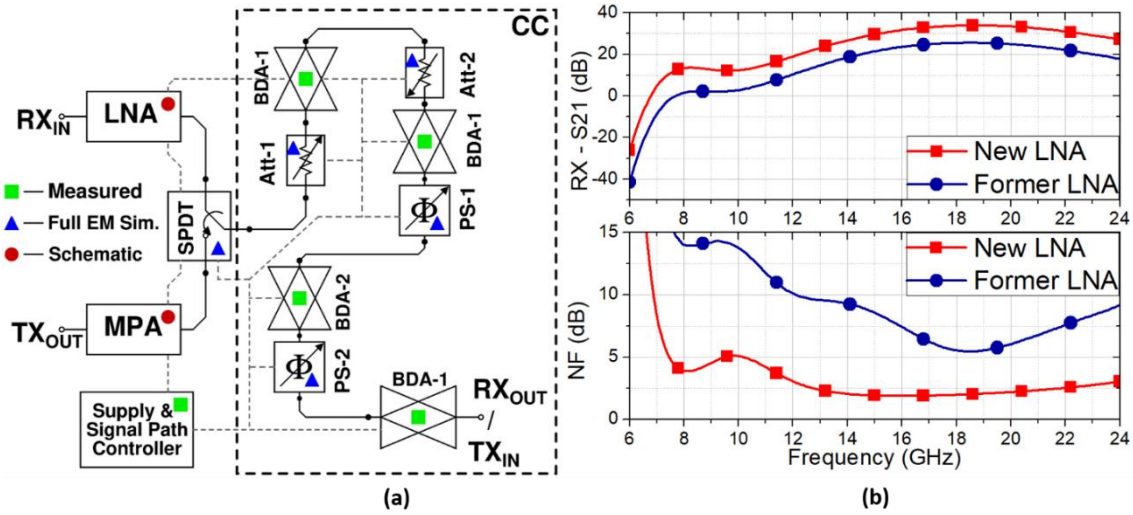


Figure 2. 48 (a) The block diagram of the X-to-K Band T/R module core chip. (b) RX gain and NF with Former and New LNA.

the wideband core-chip. It is also utilized as the MPA for the TX, to give an insight into the core-chip's output power. The measurement and simulation coherency of the measured wideband LNA ("Former LNA") guarantees the performance of the newly designed schematic level LNA ("New LNA"). The effect of both LNAs on RX's gain and NF performances are presented in Figure 2. 48 (b). The core-chip has a positive gain slope, which results in a lower gain at X-Band if Former LNA is favored. The CC has high loss and NF, especially at X-Band. This leads to a more than 10 dB NF for a core-chip scenario with the Former LNA. However, the core-chip with a maximum of 5 dB RX NF can be realized by utilizing the New LNA, without sacrificing from the power consumption and area. The simulated-measured gain difference of the Former LNA is added as a parameter to the New LNA (named as "*Amp*" in the results).

2.8.2. The Performance with Possible Scenarios

The performance of the core-chip may differ during the measurements, due to unintended parasitic effects. They can affect the gain, gain slope, NF and OP1dB performances of the design. Therefore, these various effects are defined and added to the post-layout simulations of the core-chip. In this section, the possible core-chip performance scenarios are presented, regarding the specified parasitic effects.

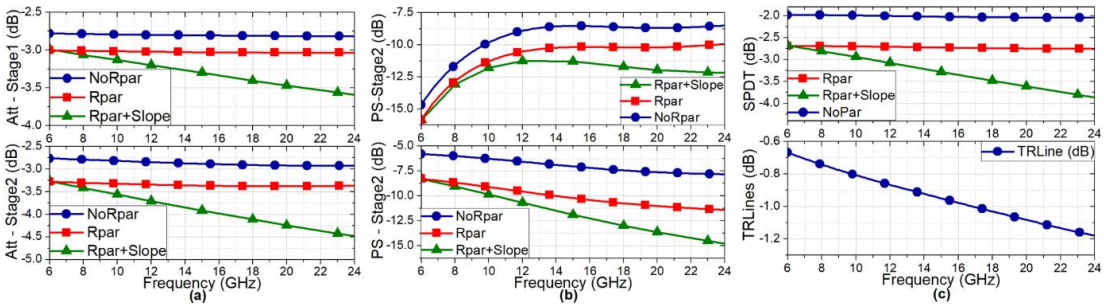


Figure 2. 49 (a) Attenuator, (b) PS, (c) SPDT and *TRLine* losses with added effects.

The iNMOS devices with various dimensions are utilized for the SPDT, attenuator and the PS. As mentioned in related sections, a series of parasitic resistance ("*Rpar*") added to the terminals of the iNMOS transistors considering previous measurements. The iNMOS devices of the 0.13 µm SiGe BiCMOS technology have not been measured yet during the period of this dissertation. Therefore, it is not easy to estimate the possible performance variation for the blocks and also for the wideband core-chip. However, various performance scenarios can be simulated. Similar to the *Rpar*, the parasitic capacitance of an iNMOS might also vary. A possible loss slope can be calculated and added to the simulations. For this purpose, the X-Band SPDT (shown in section 1. 3. 1) switch's loss slope (- 0.0625 dB/GHz) is added to the block simulations, which are named as "*Rpar + Slope*" in the related results. The loss slope is calculated considering the number of iNMOSs and their sizes. Figure 2. 49 demonstrates the described scenarios for the SPDT, attenuator, and the PS compared to the "no calculated parasitic" case ("*NoRpar*"). These effects are also valid as a parameter in the core-chip simulations. Figure 2. 49 (c) also presents the total loss of the guided microstrip transmission lines' (*TRLines*) insertion loss utilized in the wideband core-chip.

The gain and NF of the RX are presented in Figure 2. 50 (a) and (b) respectively for the defined scenarios. These simulations are done in the reference phase and attenuation states of the core-chip. The best-case simulation ("*NoPar*") includes simulated post-layout block performances, except LNA. The worst-case ("*Rpar + Amp + Slope*") takes all of the possible parasitic effects into account. It should be noted that the calculated effects might be pessimistic. The gain-slope effects of iNMOS devices are extracted from the 0.25 µm technology of the same foundry. As shown, the RX gain and its slope drops because of the added effects. However, the chain can still perform 8 dB gain at 8 GHz with a positive slope until 18 GHz, in the worst case. The gain drop also

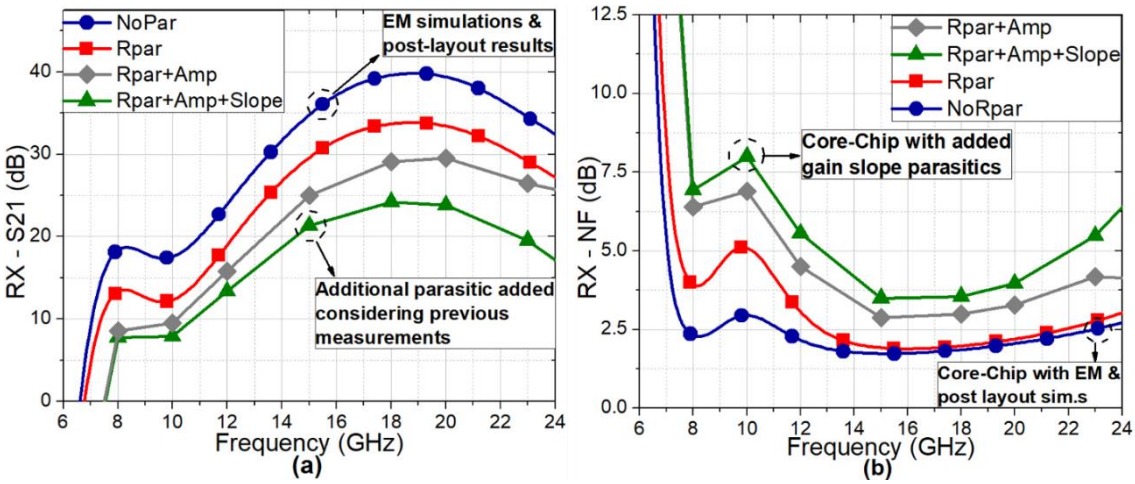


Figure 2. 50 RX (a) gain, and (b) NF for the defined parasitic effect scenarios.

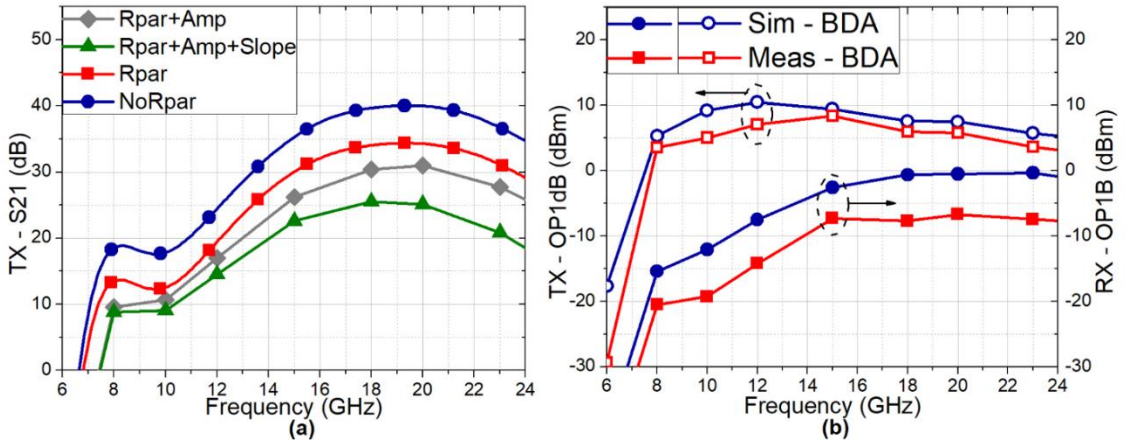


Figure 2. 51 (a) TX gain for different added parasitic scenarios. (b) TX and RX OP1B performance for the simulated and measured BDA.

affected the NF performance especially at X-Band and resulted in about 5.5 dB of mean NF in the worst-case scenario. As shown, the design can satisfy the wideband core-chip expectations even in the worst case. The TX gain is similar to the RX chain, due to including the same blocks as shown in Figure 2. 51 (a); the only difference is the signal path direction.

Similar to the reference mode gains of the RX and TX chains, the OP1dB of the core-chip is calculated as demonstrated in Figure 2. 51 (b). Two different scenarios are considered during the OP1dB simulations; the simulated ("*Sim - BDA*") and the measured ("*Meas - BDA*") BDA. These cases analyzed due to the deviated BDA OP1dB performance during measurements. It is simulated as 3.8 ± 0.52 dBm and measured as -2.38 ± 1.32 dBm. The BDA has a flat OP1dB over frequency, but the simulation-

measurement difference is close to 6 dB. As a result, the output power of the BDA is limited, especially at low frequencies. If the BDA is updated to have an OP1dB as simulated, the core-chip can provide a TX OP1dB up to + 10 dBm, as shown in Figure 2. 51 (b). As mentioned, the LNA is also utilized as the MPA to give insight into the TX performance. The output power of the TX drop is related to both the LNA and BDA. If LNA is replaced with a proper MPA, the TX OP1dB might be improved.

The OP1dB of the RX chain is presented in Figure 2. 51 (b), for the same defined cases. The behavior of the RX OP1dB is similar to its gain characteristic; the IP1dB would be almost flat as expected. Different than the TX, the OP1dB of the RX is degraded due to the high output power of the LNA. At 15 GHz, the LNA can provide up to about 10 dBm of output power. When the loss of the SPDT and Att-1 is considered, the first BDA-1 would saturate due to high RF power. Additionally, the output power of a BDA might be high for the next BDA although the CC includes multiple passive blocks. As a result of the mentioned cases, the output power of the RX is limited. If the Att-1 is switched with PS-Stage2, the input power for the BDA-1 would drop. This can improve the OP1dB by about 4.2 dB, with the expense of a deteriorated NF by 5.8 dB at 15 GHz. The CC block ordering is determined by considering the core-chip expectations, where the NF has a higher priority on RX output power. Hence, the BDA dynamic range might be improved as for the TX, instead of changing the core-chip's floorplan.

2.8.3. The Performance Summary of the Core-Chip

The gain and impedance matching performances of the simulated wideband core-chip are summarized in Figure 2. 52 for the reference phase and attenuation states, besides the possible parasitic effect scenarios stated in the previous sub-sections. The "*Rpar*" takes possible LNA and iNMOS performance degradation into account. The CC is designed by regarding the added *Rpar* resistance to iNMOS devices. When the simulations with *Rpar* effects are considered, the core-chip promised 31.5 dB and 32 dB gain for RX and TX at 16 GHz, respectively. The peak RX gain is obtained at 18.7 GHz as 33.85 dB, while it is 34.36 dB at 19.4 GHz for the TX. Both chains promise positive gain slope until about 20 GHz, which are + 2.1 dB/GHz and + 2.15 dB/GHz respectively. These results are at an adequate level to support wide bandwidth requirements of a phased

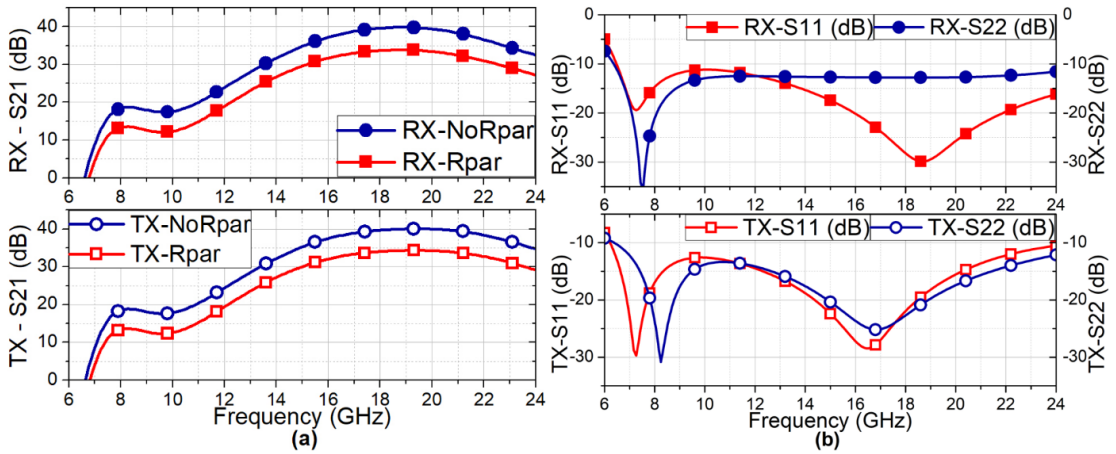


Figure 2. 52 The reference mode (a) gain, and (b) return loss for RX and TX.

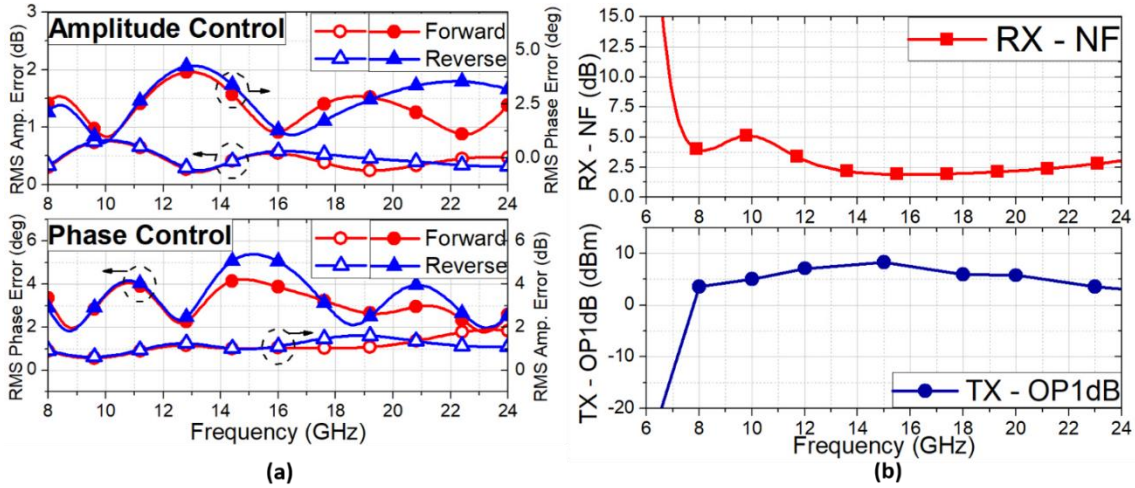


Figure 2. 53 (a) The RMS phase and amplitude errors of the core-chip during amplitude and phase control, (b) RX NF and TX OP1dB during reference mode of operation.

array T/R module. The difference between chains (especially at the higher end of the BW) is because of the forward-and-reverse mode variations and transmission line routing. The gain drop after 20 GHz is due to the BDAs as addressed in section 2. 3. 2. Figure 2. 52 (b) demonstrates the matching performance of the core-chip. The impedance terminations are independent of the iNMOS devices (so the *Rpar*), due to being determined by SiGe HBT based blocks. This reflected as a single possible scenario for the impedance terminations. As shown, they satisfy the wideband requirement of the design.

Figure 2. 53 (a) summarizes the RMS phase and amplitude errors of the core-chip during phase and amplitude control. The design can provide 4-bit of phase and amplitude resolution with a lower than 5.6^0 and 0.8 dB of RMS phase and amplitude error, respectively. These results present that the core-chip can be still improved for a higher

phase and amplitude resolution. The wideband core-chip achieved less than 5 dB of NF between 8-to-24 GHz, as shown in Figure 2. 53 (b). This demonstrates that the core-chip can satisfy the NF expectation, even if its peak gain is dropped by about 15 dB. Additionally, the design has about 6 ± 2.5 dBm of OP1dB as in Figure 2. 53 (b), and it can be enhanced by updating the BDA and MPA designs. The wideband core-chip successes these results while dissipating about 112 mW of power; a level that is lower than the similar works in literature. The Former LNA consumes about 0.69 mm^2 of area, including pads. Therefore, the total area of the MPA and LNA can be assumed as 1.6 mm^2 including the possible gap between blocks. According to this assumption, the core-chip might cover about 5.5 mm^2, which is almost 30% of the X-Band core-chip.

The realized core-chip targeted an X-to-K band performance with a low noise profile and low power consumption in a compact area. As presented in this section, the core-chip achieved lower than 5 dB mean NF with a positively sloped gain in simulations. These performances are remarkable for a wideband radar system. Its RMS phase and amplitude errors guarantee a 4-bit of phase and amplitude resolution, which can be even improved further. Even if the output power of the core-chip might need an update for enhanced performance, it confirms the desired targets can be achieved in SiGe BiCMOS technology with the realized design approaches. Moreover, the mentioned features are achieved without sacrificing from power consumption and area. Therefore, the presented design satisfies the cost, weight, compactness, and high-performance expectations of the next generation T/R module systems.

3. CONCLUSION

In this dissertation, a wideband low noise SiGe BiCMOS T/R module core-chip is realized by utilizing a bidirectional CC. The next-generation phased array systems require wide operational bandwidth for improving system integrity and functionality. The T/R module core-chips are one of the most significant elements of the system, due to determining the main RF features. The system expectations can be satisfied by utilizing III-V technology. Besides their superior wideband RF performances, III-V based core-chips are expensive and cover a large area compared to Si-based designs. Moreover, the Si-based T/R module core-chips are capable of implementing various circuits on a single substrate without performance degradation.

This work demonstrates an 8-to-24 GHz low noise T/R module core-chip in SiGe BiCMOS technology. The bandwidth limitations of the SiGe technology is surpassed by implementing a bidirectional common-chain. Additionally, the bidirectionality of the design improved the compactness, with the expense of increased complexity. The presented work is composed of an SPDT switch, BDAs, attenuator, PS, LNA, and MPA. The BDA integrated an IMN and a filter to produce a positively sloped gain in the defined frequency range. It has a measured 11.2 peak gain with a + 0.58 dB/GHz slope. Its OP1dB is -2.38 dBm, which is flat throughout the bandwidth. Similarly, it has a low GD variation (± 9.1 psec), which is a critical metric for the time-delay based systems. The block dissipates 13.8 mW of power in an 0.42 mm^2 of area (including pads). The measured features validate the BDA's suitability to the wideband core-chip. The LNA utilizes a novel design approach to satisfy the low noise requirement of the core-chip. The two prototypes have measured sub-1dB NF and 12 GHz bandwidth performances. The design procedure is applied to a new LNA design to match the core-chip's center frequency. LNA is also utilized as an MPA for the TX, due to providing a low OP1dB variation around + 10 dBm. The CC of the core-chip has a bidirectional 4-bit phase and amplitude control

with a 30 dB of attenuation range. The attenuator and PS are divided into sections, whose noise is suppressed by the utilization of multiple BDAs. The CC has 17.91 dB simulated (post-layout) peak gain and 2.71 dB/GHz of a slope in 3.88 mm^2 of an area including pads.

The wideband core-chip is simulated after verifying the performance of the blocks through their measurements and post-layout simulations. The RX and TX have 33.85 dB and 34.36 dB of simulated peak gain while dissipating 112 mW of power. The gain characteristics of both chains are positively sloped, which are critical for improving 3 dB gain-bandwidth of the system (+ 2.1 dB/GHz for RX, and + 2.15 dB/GHz for TX). The 4-bit core-chip's RMS phase and amplitude errors are lower than 5.6^0 and 0.8 dB, respectively. The core-chip has 6 + 2.5 dBm of OP1dB and a maximum 5 dB NF between 8-to-24 GHz in a 5.5 mm^2 area. To the best of my knowledge, the core-chip promises the best noise and positively sloped gain features with low power consumption in a compact area. In light of foregoing, the realized core-chip demonstrated the wideband phased array expectations can be satisfied in SiGe BiCMOS technology and be a significant candidate for the system instead of the III-V based designs.

3.1. Future Works

The block-level performances demonstrated that the bidirectional common-chain succeeded wide bandwidth in a compact area. The 8-to-24 GHz core-chip is a proof of concept design and validated its potential usage in phased array systems. When the recent results are considered, some new functionalities can be added to the core-chip to improve its features further in terms of gain, output power, phase/amplitude resolution, and area.

The BDA has a critical impact on the wideband core-chip in terms of not only gain and NF, but also area and power consumption. As mentioned, the transmission lines' return path utilizes multiple stacked metals for proper ground distribution in the core-chip. This caused an increased shunt capacitive parasitic and degraded performance of the blocks, especially BDA. The non-linear gain drop of the BDA above 20 GHz can be improved by utilizing only Metal-3 as the return path. It should be noted that improper

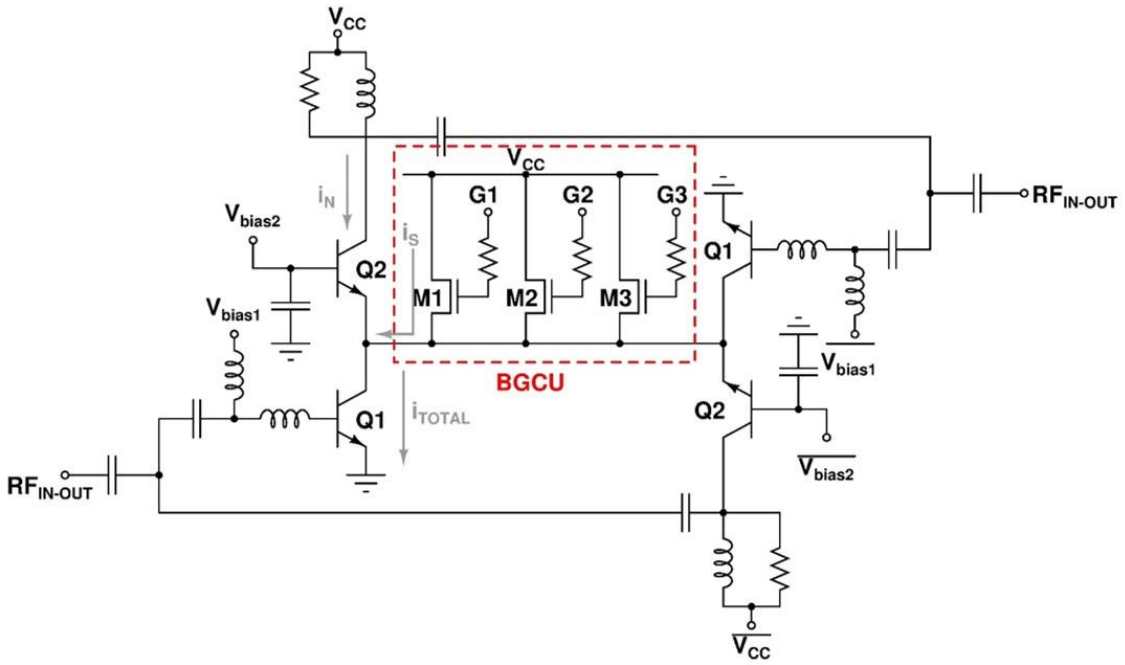


Figure 3. 1 The block diagram of the BVGA

ground distribution might also produce a similar response. Therefore, a trade-off exists between return path metal and ground distribution. The impedance termination of the BDA can be also enhanced, which would smooth the phase and attenuation fluctuations.

The output power of the core-chip is one of the points that need to be enhanced. The weakness of the design is a consequence of measuring a deteriorated BDA OP1dB. The OP1dB of the TX can be improved by increasing the BDA's gain, especially for X-Band. This approach would not be a burden for the core-chip, which is dissipating low power. A similar statement can be done for the RX, due to the BDA's limited input-referred P1dB, as declared in section 2. 8. 2.

The 4-bit wideband core-chip presented low RMS phase and amplitude errors while utilizing four BDA. When the measured gain, phase, and delay ranges of the BDA are considered, a controlling mechanism can be added to the design as new functionality. This can be obtained by introducing current-steering iNMOS devices as in Figure 3. 1. When the Bidirectional Gain Control Unit (BGCU) is turned on, the main current of the branch (i_{TOTAL}) will be divided into i_N and i_S, which determines the phase or attenuation difference. As an advantage of this method, the impedance termination of the amplifier might not differ much during the phase/gain control. The described functionality is going

to convert the BDA into a Bidirectional Variable Gain/Phase Amplifier (BVGA/BVPA). The measurements in Figure 2. 12 verify the possible usage of this method. Each BDA can be assigned to generate a new LSB for phase, amplitude or even delay control. They can be also utilized to correct the errors of the related blocks. However, the iNMOSs' effect on the cascode amplifiers is not considered during measurements. Therefore, the size of the BGCU might be the limiting factor for the BVGA or BVPA. As a solution for the mentioned problem, a single LSB (such as 0.5 dB of attenuation) can be assigned to multiple BDAs for a reduced iNMOS parasitic. Besides, the core-chip might target for 5-bit or 6-bit of phase and amplitude resolution by introducing the specified method, without sacrificing from area and power.

The wideband core-chip's area is calculated by regarding the "Former LNA". Some of its inductors are as in Figure 2. 3 (a) and (b). Additionally, the block is designed without an area specification. Therefore, the core-chip's area can be improved further. Similarly, the BDA has an area of 0.42 mm^2, which is small for a single-stage amplifier. However, the block covers at least 40 % of the CC area, due to utilizing four BDAs. Hence, improving its gain might result in the removal of a BDA, so lower NF, lower power dissipation and a smaller area for the core-chip.

The wideband systems may require TTD units instead of phase shifters, as mentioned before. It is shown that the sub-blocks are compatible with the delay-based architecture. Generally, the TTD blocks have a high and negatively sloped loss. When the results are considered, the side effects of the TTD can be suppressed with the presented wideband core-chip.

BIBLIOGRAPHY

Alizadeh, Amirreza, Masoud Meghdadi, Majid Yaghoobi, and Ali Medi. "Design of a 2–12-GHz Bidirectional Distributed Amplifier in a 0.18-μm CMOS Technology." IEEE Transactions on Microwave Theory and Techniques 67, no. 2 (December 13, 2018): 754-64.

Balanis, Constantine A. Antenna Theory: Analysis and Design. Chichester, West Sussex, New Jersey: Wiley Blackwell, 2016.

Bentini, Andrea, Mauro Ferrari, Patrick E. Longhi, Eric Marzolf, Joel Moron, and Remy Leblanc. "A 6-18 GHz GaAs Multifunctional Chip for Transmit/Receive Modules." 2014 11th European Radar Conference, December 18, 2014, 605-08.

Cao, Rui, Zhuang Li, Xiaohui Tao, and Lei Sang. "A Compact X-band Four-channel SiGe BiCMOS T/R Chipset for Digital Array Radar Applications." 2017 IEEE MTT-S International Microwave Symposium (IMS), October 05, 2017, 1979-982.

Carosi, D., Bettidi, A., Nanni, A., Marescialli, L., and Cetronio, A. "A Mixed-Signal X-band SiGe Multi-Function Control MMIC for Phased Array Radar Applications" 2009 European Microwave Conference (EuMC), October 30, 2009.

Cetindogan, Barbaros, Berktug Ustundag, Abdurrahman Burak, Matthias Wietstruck, Mehmet Kaynak, and Yasar Gurbuz. "A 5–13 GHz 6-bit Vector-sum Phase Shifter with 3.5 DBm IP1dB in 0.25-μm SiGe BiCMOS." 2017 IEEE Asia Pacific Microwave Conference (APMC), 2017. Accessed January 11, 2018.

Chen, Mingqi, William Sutton, Ioulia Smorchkova, Benjamin Heying, Wen-Ben Luo, Vincent Gambin, Floyd Oshita, Roger Tsai, Michael Wojtowicz, Reynold Kagiwada, Aaron Oki, and Jenshan Lin. "A 1–25 GHz GaN HEMT MMIC Low-Noise Amplifier." IEEE Microwave and Wireless Components Letters 20, no. 10 (August 26, 2010): 563-65.

Cho, Moon-Kyu, Ickhyun Song, Jeong-Geun Kim, and John D. Cressler. "An Active Bi-Directional SiGe DPDT Switch With Multi-Octave Bandwidth." IEEE Microwave and Wireless Components Letters 26, no. 4 (March 09, 2016): 279-81.

Cho, Moon-Kyu, Jang-Hoon Han, Jin-Hyun Kim, and Jeong-Geun Kim. "An X/Ku-band Bi-directional True Time Delay T/R Chipset in 0.13 μm CMOS Technology." 2014 IEEE MTT-S International Microwave Symposium (IMS2014), July 10, 2014, 1-3.

Cho, Moon-Kyu, Jeong-Geun Kim, and Donghyun Baek. "A Switchless CMOS Bi-Directional Distributed Gain Amplifier With Multi-Octave Bandwidth." IEEE Microwave and Wireless Components Letters 23, no. 11 (September 24, 2013): 611-13.

Chu, Ta-Shun, and Hossein Hashemi. "True-Time-Delay-Based Multi-Beam Arrays." IEEE Transactions on Microwave Theory and Techniques 61, no. 8 (July 03, 2013): 3072-082.

Comeau, Jonathan P., Matt A. Morton, John D. Cressler, John Papapolymerou, and Mark Mitchell. "A High-Linearity 5-bit, X-band SiGe HBT Phase Shifter." 2006 IEEE MTT-S International Microwave Symposium Digest, November 20, 2006, 1668-671.

Çalışkan, Can. 2014. “High Dynamic Range Low Noise Amplifier and Wideband Hybrid Phase Shifter for SiGe BiCMOS Phased Array T/R Modules”, M.Sc Thesis, Sabanci University.

Çalışkan, Can, Abdurrahman Burak, Esref Turkmen, Melik Yazici, and Yasar Gurbuz. "Active Positive Sloped Equalizer for X-Band SiGe BiCMOS Phased Array Applications." IEEE Transactions on Circuits and Systems II: Express Briefs (Early Access), January 30, 2019, 1.

Çalışkan, Can, Abdurrahman Burak, Esref Turkmen, Melik Yazici, and Yasar Gurbuz. "Active Positive Sloped Equalizer for X-Band SiGe BiCMOS Phased Array

Applications." IEEE Transactions on Circuits and Systems II: Express Briefs, January 30, 2019, 1.

Çalışkan, Can, Ilker Kalyoncu, Emre Ozeren, Mehmet Kaynak, and Yasar Gurbuz. "A Wideband Low Noise SiGe Medium Power Amplifier for X-Band Phased Array Applications." 2016 11th European Microwave Integrated Circuits Conference (EuMIC), December 08, 2016.

Çalışkan, Can, Ilker Kalyoncu, Melik Yazici, and Yasar Gurbuz. "Sub-1-dB and Wideband SiGe BiCMOS Low-Noise Amplifiers for X -Band Applications." IEEE Transactions on Circuits and Systems I: Regular Papers 66, no. 4 (December 25, 2018): 1419-430.

Davulcu, Murat, Can Çalışkan, Ilker Kalyoncu, Mehmet Kaynak, and Yasar Gurbuz. "7-Bit SiGe-BiCMOS Step Attenuator for X-Band Phased-Array RADAR Applications." IEEE Microwave and Wireless Components Letters 26, no. 8 (July 27, 2016): 598-600.

Davulcu, Murat, Emre Ozeren, Mehmet Kaynak, and Yasar Gurbuz. "A New 5–13 GHz Slow-Wave SPDT Switch With Reverse-Saturated SiGe HBTs." IEEE Microwave and Wireless Components Letters 27, no. 6 (May 23, 2017): 581-83.

Dinc, Tolga, Samet Zihir, and Yasar Gurbuz. "A Fully Integrated, Highly Linear CMOS T/R Switch for X-Band Phased Array Radars." International Journal of Circuit Theory and Applications 42, no. 3 (December 15, 2012): 296-308.

Dogan, Hakan, Robert G. Meyer, and Ali M. Niknejad. "Analysis and Design of RF CMOS Attenuators." IEEE Journal of Solid-State Circuits 43, no. 10 (October 07, 2008): 2269-283.

Frye, R.c., S. Kapur, and R.c. Melville. "A 2-GHz Quadrature Hybrid Implemented in CMOS Technology." IEEE Journal of Solid-State Circuits 38, no. 3 (March 2003): 550-555.

Garakoui, S. K., Klumperink, E. A. M., Nauta, B., van Vliet F. E. 2011. “Phased-array antenna beam squinting related to frequency dependency of delay circuits”, 41st European Microwave Conference 2011, 1304-1307.

Gharibdoust, Kiarash, Naser Mousavi, Milad Kalantari, Mohsen Moezzi, and Ali Medi. "A Fully Integrated 0.18-µm CMOS Transceiver Chip for X-Band Phased-Array Systems." IEEE Transactions on Microwave Theory and Techniques 60, no. 7 (May 17, 2012): 2192-202.

Hansen, K. "Wireless RF Design Challenges." IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, 2003, June 28, 2003, 3-7.

Harir, Eyal, and Eran Socher. "0.5W X-band SiGe PA with Integrated Double-tuned Transformers." 2013 IEEE MTT-S International Microwave Symposium Digest (MTT), January 06, 2014.

Heijningen, M., A. Boer, J.a. Hoogland, M. Wanum, A.p. Hek, F.e. Vliet, and H. Brouzes. "Multi Function and High Power Amplifier Chipset for X-Band Phased Array Frontends." 2006 European Microwave Integrated Circuits Conference, 2006. Accessed January 15, 2007.

Howard, D. C., P. K. Saha, S. Shankar, R. M. Diestelhorst, T. D. England, N. E. Lourenco, E. Kenyon, and J. D. Cressler. "An 8–16 GHz SiGe Low Noise Amplifier With Performance Tuning Capability for Mitigation of Radiation-Induced Performance Loss." IEEE Transactions on Nuclear Science 59, no. 6 (December 2012): 2837-846.

Ihp-microelectronics.com. “Low-Volume & Multi-Project Service”. Innovations for High Performance Microelectronics. Accessed August 08, 2019. https://www.ihp-microelectronics.com/en/services/mpw-prototyping/sigec-bicmos-technologies.html

Inanlou, Farzad, Christopher T. Coen, and John D. Cressler. "A 1.0 V, 10–22 GHz, 4 MW LNA Utilizing Weakly Saturated SiGe HBTs for Single-Chip, Low-Power, Remote Sensing Applications." IEEE Microwave and Wireless Components Letters 24, no. 12 (October 21, 2014): 890-92.

Jeon, Sanggeun, Yu-Jiu Wang, Hua Wang, Florian Bohn, Arun Natarajan, Aydin Babakhani, and Ali Hajimiri. "A Scalable 6-to-18GHz Concurrent Dual-Band Quad-Beam Phased-Array Receiver in CMOS." IEEE International Solid-State Circuits Conference 2008 - Digest of Technical Papers, January 9, 2009, 186-605.

Jeong, J.c., and I.b. Yom. "X-band High Power SiGe BiCMOS Multi-function Chip for Active Phased Array Radars." Electronics Letters 47, no. 10 (May 12, 2011): 618-19.

Jeong, Jin-Cheol, In-Bok Yom, Jae-Duk Kim, Wang-Yong Lee, and Chang-Hoon Lee. "A 6–18-GHz GaAs Multifunction Chip With 8-bit True Time Delay and 7-bit Amplitude Control." IEEE Transactions on Microwave Theory and Techniques 66, no. 5 (January 8, 2018): 2220-230.

Kanar, Tumay, and Gabriel M. Rebeiz. "X- and K-Band SiGe HBT LNAs With 1.2- and 2.2-dB Mean Noise Figures." IEEE Transactions on Microwave Theory and Techniques 62, no. 10 (August 1, 2014): 2381-389.

Koh, K., and G. Rebeiz. "A 6-18 GHz 5-Bit Active Phase Shifter." 2010 IEEE MTT-S International Microwave Symposium, July 23, 2010. doi:10.1109/mwsym.2010.5517540.

Kopp, and Carlo. "AEW&C - Phased Array Technology Parts 1 and 2." Australian Aviation. January 1, 2005. Accessed August 08, 2019. http://www.ausairpower.net/aew-aesa.html.

Ku, Bon-Hyun, and Songcheol Hong. "6-bit CMOS Digital Attenuators With Low Phase Variations for X-Band Phased-Array Systems." IEEE Transactions on Microwave Theory and Techniques 58, no. 7 (May 24, 2010): 1651-663.

Kumar, Thangarasu Bharatha, Kaixue Ma, and Kiat Seng Yeo. "A 60-GHz Coplanar Waveguide-Based Bidirectional LNA in SiGe BiCMOS." IEEE Microwave and Wireless Components Letters 27, no. 8 (July 20, 2017): 742-44.

Kuo, W.-M.l., Qingqing Liang, J.d. Cressler, and M.a. Mitchell. "An X-Band SiGe LNA with 1.36 dB Mean Noise Figure for Monolithic Phased Array Transmit/Receive Radar Modules." IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, 2006, July 10, 2006.

Liu, Chao, Qiang Li, Yihu Li, Xiao-Dong Deng, Xiang Li, Haitao Liu, and Yong-Zhong Xiong. "A Fully Integrated X-Band Phased-Array Transceiver in 0.13- SiGe BiCMOS Technology." IEEE Transactions on Microwave Theory and Techniques 64, no. 2 (December 17, 2016): 575-84.

Liu, Liang, Andreas R. Alt, Hansruedi Benedickter, and C. R. Bolognesi. "InP-HEMT X-band Low-Noise Amplifier With Ultralow 0.6-mW Power Consumption." IEEE Electron Device Letters 33, no. 2 (December 23, 2012): 209-11.

Lohmiller, Peter, Rolf Reber, Patrick Schuh, Martin Oppermann, and Sebastien Chartier. "SiGe BiCMOS X-band Transceiver-chip for Phased-array Systems." 2017 European Radar Conference (EURAD), January 8, 2018. doi:10.23919/eurad.2017.8249233.

Long, J.r. "Monolithic Transformers for Silicon RF IC Design." IEEE Journal of Solid-State Circuits 35, no. 9 (September 2000): 1368-382.

M / A – COM Tech, XZ1002-BD 8.5-11.0 GHz GaAs MMIC Core Chip, Asia, 2010, pp. 1-11.

Ma, Desheng, Fa Foster Dai, Richard C. Jaeger, and J. David Irwin. "An 8-18 GHz Wideband SiGe BiCMOS Low Noise Amplifier." 2009 IEEE MTT-S International Microwave Symposium Digest, July 17, 2009.

Mailloux, R. J. 2005. Phased Array Antenna Handbook. Massachusetts: Artech House Antennas and Propagation Library.

Manohar, S., and V. S. R. Kirty. "An Ultra Low Noise Amplifier at X Band." IEEE MTT-S International Microwave and RF Conference, March 27, 2014.

Mcquiddy, D.N., R.L. Gassner, P. Hull, J.S. Mason, and J.M. Bedinger. "Transmit/receive Module Technology for X-band Active Array Radar." Proceedings of the IEEE 79, no. 3 (March 1991): 308-41.

Min, Byung-Wook, and Gabriel M. Rebeiz. "A 10–50-GHz CMOS Distributed Step Attenuator With Low Loss and Low Phase Imbalance." IEEE Journal of Solid-State Circuits 42, no. 11 (October 22, 2007): 2547-554.

Morton, M.a., J.d. Cressler, J.p. Comeau, J. Papapolymerou, and M. Mitchell. "5 Bit, Silicon-based, X-band Phase Shifter Using a Hybrid Pi/t High-pass/low-pass Topology." IET Microwaves, Antennas & Propagation 2, no. 1 (February 08, 2008): 19-22.

Neuchter, P. "Silicon Based Monolithic Integrated Microwave Systems-present Limitations and Future Aspects." Topical Meetings on Silicon Monolithic Integrated Circuits in RF Systems. Digest of Papers (Cat. No.00EX397), 2000, 19-22.

Nortropgrumman.com. “Microelectronics Products & Services”. Northrop Grumman. Accessed August 08, 2019. http://www.northropgrumman.com/BusinessVentures/Microelectronics/Documents/pageDocs/FoundryFlysheet.pdf

Ommic.com. “OMMIC Foundry Services”. OMMIC Innovating with III-V’s. Accessed August 08, 2019. http://www.ommic.com/site/mpw-4

Ozeren, Emre, Arin Can Ulku, Ilker Kalyoncu, Can Caliskan, Murat Davulcu, Mehmet Kaynak, and Yasar Gurbuz. "A Wideband High Isolation CMOS T/R Switch for X-band Phased Array Radar Systems." 2016 IEEE 16th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), April 04, 2016.

Rebeiz, Gabriel M., and Lee M. Paulsen. "Advances in Low-cost Phased Arrays Using Silicon Technologies." 2017 IEEE International Symposium on Antennas and Propagation & USNC/URSI National Radio Science Meeting, October 19, 2017.

Saarnisaari, Harri, and Timo Braysy. "Future Military Mobile Radio Communication Systems from Electronic Warfare Perspective." 2017 International Conference on Military Communications and Information Systems (ICMCIS), June 26, 2017.

Saha, Prabir K., Subramaniam Shankar, Rob Schmid, Richie Mills, and John D. Cressler. "Analysis and Design of a 3-26 GHz Low-noise Amplifier in SiGe HBT Technology." 2012 IEEE Radio and Wireless Symposium, April 03, 2012.

Sarkas, I. 2010. “Analysis and Design of W-band Phase Shifters”, M.Sc Thesis, University of Toronto.

Sayginer, Mustafa, and Gabriel M. Rebeiz. "An Eight-Element 2–16-GHz Programmable Phased Array Receiver With One, Two, or Four Simultaneous Beams in SiGe BiCMOS." IEEE Transactions on Microwave Theory and Techniques 64, no. 12 (November 09, 2016): 4585-597.

Sim, Sanghoon, Byungjoo Kang, Jeong-Geun Kim, Jong-Hoon Chun, Brian Jang, and Laurence Jeon. "A Four-channel Bi-directional CMOS Core Chip for X-band Phased Array T/R Modules." 2015 IEEE Radar Conference (RadarCon), June 25, 2015, 1198-201.

Sim, Sanghoon, Laurence Jeon, and Jeong-Geun Kim. "A Compact X-Band Bi-Directional Phased-Array T/R Chipset in 0.13 µm CMOS Technology." IEEE Transactions on Microwave Theory and Techniques 61, no. 1 (December 19, 2013): 562-569.

Song, Ickhyun, Moon-Kyu Cho, Jeong-Geun Kim, Glenn Hopkins, Mark Mitchell, and John D. Cressler. "A 2–22 GHz Wideband Active Bi-directional Power Divider/combiner in 130 Nm SiGe BiCMOS Technology." 2016 IEEE MTT-S International Microwave Symposium (IMS), August 11, 2016.

Turkmen, Esref, Abdurrahman Burak, Can Caliskan, Ilker Kalyoncu, and Yasar Gurbuz. "A SiGe BiCMOS Bypass Low-Noise Amplifier for X-Band Phased Array RADARs." 2018 Asia-Pacific Microwave Conference (APMC), January 17, 2019.

Ums-gaas.com. “Foundry Services”. United Monolithic Semiconductors. Accessed August 08, 2019. https://www.ums-gaas.com/wp-content/uploads/2018/01/Brochure_Foundry_2017-1.pdf

VIPER-RF, VRFA0026-BD X-Band GaAs MMIC Low Noise Amplifier, 1st ed., U.K., 2015, pp. 1–4.

Yamagata, Masashi, and Hossein Hashemi. "A Differential X/Ku-Band Low Noise Amplifier in 0.13-µm CMOS Technology." IEEE Microwave and Wireless Components Letters 17, no. 12 (December 04, 2007): 888-90. doi:10.1109/lmwc.2007.910511.

Yang, J.m., R. Lai, Y.h. Chung, M. Nishimoto, M. Battung, W. Lee, and R. Kagiwada. "Compact Ka-band Bi-directional Amplifier for Low-cost Electronic Scanning Array Antenna." IEEE Journal of Solid-State Circuits 39, no. 10 (September 27, 2004): 1716-719.

Yau, W., H. Kanber, C.s. Wu, B.m. Paine, S. Bar, Z. Bardai, S. Janesch, D. Kaputa, and W. Fabian. "Design Translation of an X-band Multifunction PHEMT MMIC." 1994 IEEE MTT-S International Microwave Symposium Digest (Cat. No.94CH3389-4), May 1994.