Intrinsic Stress-Induced Self-Assembly of Multilayer Thin Films for Fabrication of Three-Dimensional Micro Devices

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Submitted to the Graduate School of Engineering and Natural Sciences
in partial fulfillment of
the requirements for the degree of
Master of Science

Sabancı University
December 2018

Intrinsic Stress-Induced Self-Assembly of Multilayer Thin Films for Fabrication of Three-Dimensional Micro Devices

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DATE OF APPROVAL: 14/12/2018

ABSTRACT

INTRINSIC STRESS-INDUCED SELF-ASSEMBLY OF MULTILAYER THIN FILMS FOR FABRICATION OF THREE DIMENSIONAL MICRO DEVICES

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Electronics Engineering, Master's Thesis, 2018

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Keywords: intrinsic stress, metal thin-film, residual stress, internal stress, self-assembly, bending, RF-MEMS, inductor, *Q* factor, roll-up, micro cantilever, fixed-free beam

This work reports on the process technology development for fabrication of three-dimensional (3D), on-chip micro devices based on self-assembly using intrinsic stresses otherwise referred to as residual or internal stresses in thin films. Stress-induced bending in different cantilever designs were modelled at various film thicknesses using finite element analysis (FEA) method and bending conditions were optimized. Intrinsic stress-induced bending mechanism is verified by fabrication of bi-layer metallic micro cantilever structures with varying stress conditions which reach bending angles of up to 137° and possibly more upon release. By modulating the loading mode (tensile or compressive) along the beam length, complex out-of-plane wavy cantilevers with multiple upward and/or downward bends were realized. The fabrication and modelling results display large overlap which further demonstrates the applicability of intrinsic stress-induced bending as a controllable technology towards fabrication of out-of-plane 3D micro components. Additionally, as a potential application to RF-MEMS inductors, stress-induced self-assembly of thin films into single and multiple-turn vertical inductors with ring and spiral geometry was investigated, and performance improvement was verified using coupled multi-physics simulation tools. Structures after transverse bending display higher *Q* factor and self-resonance frequency (f_{SR}) as compared to inductor configurations in planar geometry with the same turn-density. Simulation results indicate that, performance increase of approximately 100% in both *Q* factor and resonance frequency can be achieved for ring and spiral inductors.

ÖZET

ÜÇ BOYUTLU MİKRO CİHAZLARIN ÜRETİMİ İÇİN ÇOK KATMANLI İNCE FILMLERİN İÇ STRES KYANAKLI KENDİLİĞİNDEN MONTAJI

RAYAN BAJWA

Elektronik Mühendisliği, Yüksek Lisans Tezi, 2018

Tez danışmanı: Yrd. Doç. Dr. Murat Kaya Yapici

Anahtar Kelimeler: iç stres, metal ince film, artık stres, iç stres, kendinden montaj, bükme, RF-MEMS, indüktör, Q faktörü, roll-up (sarmak, yuvarlamak), mikro konsol, sabit kiriş

Bu çalışma, üç boyutlu (3B) çip üstü mikro cihazların kendinden montaja dayalı iç stresleri kullanan, aksi halde ince filmlerde artık ya da iç stresler olarak adlandırılan kendiliğinden oluşturmaya dayalı mikroişlemlerin üretilmesi için süreç teknolojisinin gelişimini bildirmektedir. Desenli ince filmlerde gerilme kaynaklı bükülme, sonlu elemanlar analizi yöntemi kullanılarak çeşitli kalınlıklarda modellenmiştir ve sonuçta bükülme koşulları optimize edilmiştir. İçsel strese bağlı bükülme mekanizması, iki tabakalı metalik mikro konsol yapılarının, değişen stres koşullarına sahip, 137°'ye kadar bükülme açılarına ulaşan ve muhtemelen serbest bırakıldıktan sonra bükülmesiyle doğrulanmaktadır. Kiriş uzunluğu boyunca yükleme modunun (gerilmeye karşı basınç) modüle edilmesiyle, çoklu yukarı ve / veya aşağı kıvrımlara sahip karmaşık düzlemsel dalgalı konsollar gerçekleştirildi. Üretim ve modelleme sonuçları, düzlemsel 3B mikro bileşenlerin üretimine yönelik kontrol edilebilir bir teknoloji olarak içsel stres kaynaklı bükmenin uygulanabilirliğini göstermektedir. Ayrıca, RF-MEMS indüktörlerine potansiyel bir uygulama olarak, ince filmlerin stres kaynaklı kendiliğinden montajını, halka ve spiral geometrili tek ve çok türlü dikey indüktörlere monte etmekteyiz ve birleşik çoklu fizik simülasyon araçlarını kullanarak performans iyileştirmesini doğrulamaktayız. Enine bükülme sonrası yapılar, aynı dönüş yoğunluğuna sahip düzlemsel geometride indüktör konfigürasyonlarına kıyasla daha yüksek Q faktörü ve kendi kendine rezonans frekansı gösterir. Simülasyon sonuçları, hem Q faktörü hem de rezonans frekansında yaklaşık %100'lük bir performans artışının halka ve spiral indüktörler için elde edilebileceğini göstermektedir.

In dedication to my parents for all the sacrifice they have made trying to make me a better person and to my other family members for their love and support!

ACKNOWLEDGEMENTS

I would like to express my deepest appreciation to my supervisor Dr. Murat Kaya Yapici for his patience, encouragement and guidance. I am grateful to him for giving me an opportunity to be a part of SU-MEMS, I could not have imagined a better advisor and mentor. Without his guidance and persistent help this thesis would not have been possible. My sincere gratitude is extended to my committee members, Dr. Burak Kelleci and Dr. Burc Misirlioglu for their valuable time, review and comments on the thesis. Special thanks to all my lab mates and my friends here at Sabanci. I would also like to extend my appreciation to my family especially to my parents and my wife for their constant support, prayers and encouragement.

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CHAPTER 1

Introduction

Three-dimensional micro/nanostructures promise realization of various on-chip devices [1-3] which have superior performance. However, fabrication challenges of 3D devices is the primary technological limitation against their implementation. Conventionally, planar microelectronic process technologies involve stacking of materials on substrate surfaces using standard microfabrication techniques (i.e. lithography, deposition and etching). These methods typically limit the thickness in z-direction and shape of the final device geometry follows the same aerial (xy) profile along the z-direction. To solve this issue and achieve complex 3D structures with conventional techniques, layer-by-layer lithography and electroplating techniques have been used [4] which still provide partial solution to the problem of fabricating complex three-dimensional micro/nanostructures.

Alternatively, MEMS technologies have emerged as a breakthrough in the field of micro/nano fabrication over the past few decades which allows fabricating 3-dimensional out-of-plane structures using different micromachining techniques. Consequently, the ability to produce 3D devices at microscale has led MEMS to become one of the leading technologies for different micro level applications including sensing and actuation, RF electronics and various micro-optics applications etc.

The motivation of this thesis is to advance the state-of-the-art in MEMS 3D fabrication by developing controllable self-assembly processes based on intrinsic stresses in patterned thin films. Upon thin film deposition, intrinsic stresses build inside the material causing the film to either contract or expand when released from the supporting substrate. The concept could be further extended to multi-layer thin films where each layer with different stress conditions could generate a stress gradient along the thickness of multi-layer film. Likewise, when released from the substrate, multi-layer film can bend either in upward or downward direction depending upon the nature of stress gradient. The work

presented here reports on the process technology development for controllable bending of patterned multi-layer thin films. For that, bi-layer micro cantilevers with different geometrical specifications were designed and their behavior under internal stress was studied through simulations and experiments. Both simulation and fabrication results showed huge agreement and revealed controllable bending of microcantilevers with bending angles ranging from 15º to 155 º depending upon the length and thickness values of bi-metallic cantilevers. Additionally, by modulating the stress conditions along beam length, complex wavy structures were also realized promising the compatibility of the process with complex 3D microstructures. To demonstrate the utility of this concept, the concept was applied to RF inductors converting conventional planar inductors into out-of-plane 3D inductors. The bending of inductors indicated significant improvement in performance parameters of inductor (i.e. *Q*-factor and resonance frequency) due to reduced proximity effects from the substrate.

The development of intrinsic-stress induced self-assembly technology and its application to device fabrication is described in this thesis in 6 main sections. In the first section, a review on primary application areas that can benefit from 3D microfabrication is described. Next, different process technologies to develop on-chip 3D components are summarized (chapter 3). Then, a detailed discussion on intrinsic stress induced self-assembly and its applications is provided in chapter 4. Following this, in chapter 5, efforts on achieving intrinsic stress based controllable self-assembly are discussed. Progressively, chapter 6 explains intrinsic stress induced self-assembled RF MEMS inductors as a potential application to proposed process technology and finally, in chapter 7, a conclusion to this work is provided.

CHAPTER 2

3D MEMS Devices and Applications

In this section, some of the primary application areas of 3-dimensional MEMS fabrication are described.

2.1. Sensing and Actuation

Potentially, out-of-plane fabrication techniques enables realization of many on-chip sensing elements including flow sensors, pressure sensors, inertial sensors (accelerometer and gyroscope) and AFM probe tips. These on-chip sensors fabricated through different micromachining techniques rule out conventional sensing devices due to their smaller size, faster response and better uniformity.

3-dimensional vertical MEMS hot wire anemometers (HWA) for flow sensing applications were reported in [4]. Anemometers for flow sensing application include a straight hot wire mounted on top of two vertical supporting beams. With fluid flow, the temperature of hot wire changes and hence velocity can be estimated. The proposed microstructure involved the use of polymer material (polyimide) as supporting beams for hot wire element of anemometer. The structures were first fabricated in planar fashion on substrate and then elevated into vertical direction using plastic deformation magnetic assembly (PDMA, to be discussed in later section) as shown in Fig. 1a.

Another class of vertical anemometers for shear stress measurement was discussed in [5]. The planar anemometer structures were first fabricated on SOI (silicon on insulator) wafer with aluminum metal as wire element. Combination of isotropic and anisotropic dry etching was performed to remove bulk of material from underneath the microstructure to create thin free standing structure. A separate silicon wafer was used to create sensor holding chips by creating anisotropic etched holes in substrate. Horizontal anemometer

structures were then fixed into holes of sensor holding chip resulting into vertical shaped sensors as shown in Fig. 1b.

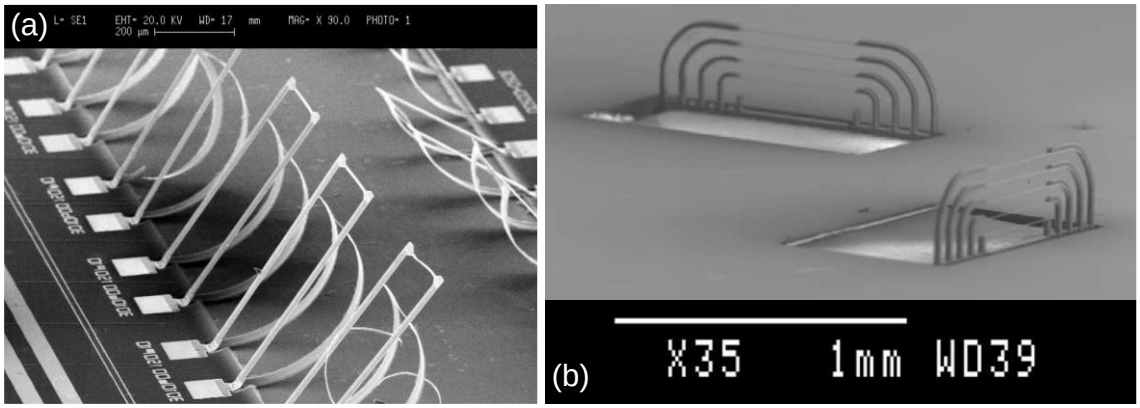

Fig. 1. Hot wire on-chip anemometers; (a) PDMA based [4] (b) Horizontal anemometers fixed in sensor holding chips [5].

Haircell sensors naturally found in animals act as vibration, touch, pressure, flow and acoustic sensors. Efforts to produce out-of-plane artificial haircell type sensors (AHCTS) were also put together for various sensing applications [6-7]. Haircell shaped sensors consisted of piezoresistive strain gauge were fabricated on silicon substrate. PDMA was used to bend the structures into vertical position (Fig. 2a). Subject to application, the deflection in haircell type sensor was translated into electrical domain by means of piezoresistive strain gauge [6].

An approach to develop haircell type sensors using 3-D carbon nanotube (CNT) bundles was also proposed [7]. The design contained three CNT bundles; one main CNT bundle in middle and other two neighbor CNT bundles (smaller in height than the main bundle) on each side of main bundle. Under normal loading conditions, main bundle is deflected more than the surrounding neighbor CNT bundles due to the larger height and hence distance between these bundles varies (fig. 2b). The change in distance is further translated in to variation of resistance between these bundles which acts as a major sensing mechanism in these CNT based haircell type sensors.

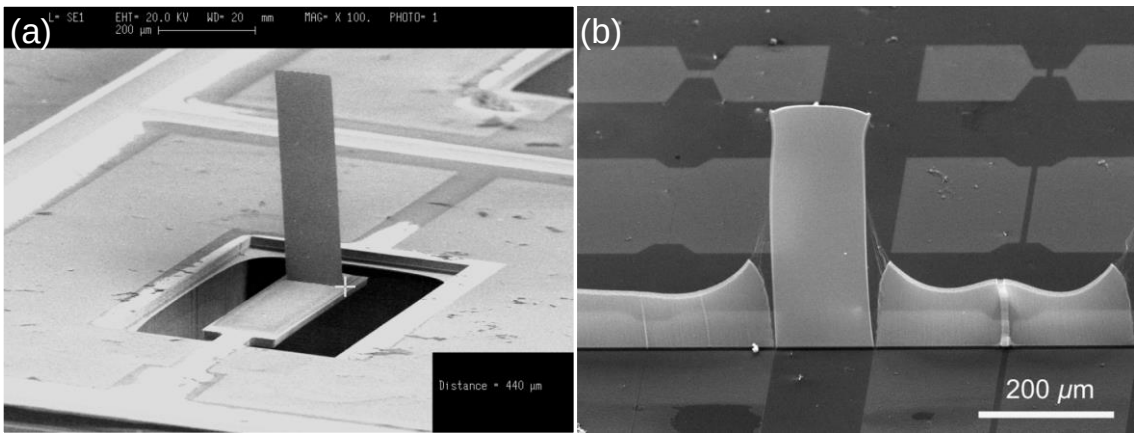

Fig. 2. Haircell type flow sensor; (a) PDMA based [6] (b) using carbon nanotube bundles [7].

Inertial sensors were also developed using 3D fabrication techniques (bulk micromachining) for different applications including gyroscopes and accelerometers etc. [8-10]. Earliest batch fabricated silicon based accelerometers were reported in 1979 [1]. The device composed of 3mm long and weighing 0.02g free standing cantilever fabricated using bulk etching of silicon underneath the cantilever. The device was able to measure accelerations ranging from 0.02g to 50g. The sensing mechanism involves the use of piezoresistive material mounted on cantilever beam which translates the accelerating loads (causing deflection in cantilever) into resistance change [1].

Similarly, many other attempts to produce accelerometers based on different working principles (piezoresistive, resonant and capacitive etc.) were reported in [8, 11-12]. A high resolution high sensitivity capacitive accelerometer for micro-gravity applications can be seen in Fig. 3. The design consists of double-sided fixed suspended cantilever beam on silicon substrate surrounded by parallel electrodes. The cavity underneath the suspended structure is created using bulk etching of silicon, allowing the beam to vibrate in z-direction (under loading conditions). Under acceleration, the beam vibrates, in return changing the capacitance linked with neighboring electrodes. This capacitance change is then recorded to estimate the acceleration.

The evolution of MEMS 3D fabrication techniques has enabled us to create high aspect ratio out-of-plane structures. These high aspect-ratio structures can be used to produce sharp tips for various surface scanning applications. Atomic force microscopes (AFM)

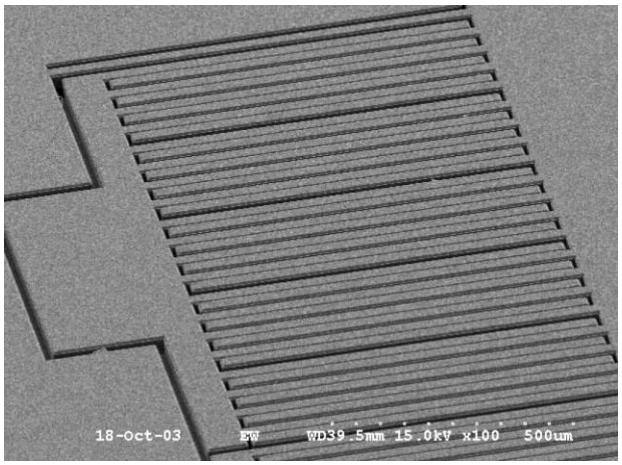

Fig. 3. A bulk micromachined capacitive silicon based accelerometer [12].

use such sharp tips for surface imaging [13-16]. One of the earliest attempts to produce atomically sharp silicon tips with radius of less than a nanometer is elaborated in [17]. Silicon out-of-plane cone-type structures were first prepared using bulk etching of silicon. Thermal oxidation of silicon cones resulted in thinning of the microstructures with their tips shrinking to a uniform radius with value of less than 1 nm. Thermally grown oxide was then removed using HF etching to achieve sharp silicon tips.

Likewise, sharp silicon tips for atomic force microscopy applications were produced using isotropic KOH etching of silicon followed by thermal oxidation technique (for sharpening of tips) [13]. The aim was to produce a free standing silicon cantilever with a sharp tip at its one end. The method proposed an additional step of boron implantation prior to thermal oxidation sharpening step to create a doped layer of silicon. This doped layer acts as an etch stop layer for silicon etching (while shaping and releasing the cantilever). This technique gives better controllability of the process, since the geometrical dimensions of cantilever and the tip are defined by boron doped region, and can be varied simply by varying doping parameters. Fig. 4 shows various sharp silicon tips for AFM application.

In similar fashion, different actuating elements (magnetic, piezoelectric, electrostatic, thermal) could also be realized using 3D microfabrication techniques for various applications including micro mirrors for beam scanning and micro robotic manipulators etc. [18-20]. A complex design of mems micromirror using bimorphs to achieve scanning angles of ± 30° was proposed in [21]. A planar structure lying on sacrificial layer consisted of 2D square micromirror connected with 4 bimorph structures at its 4

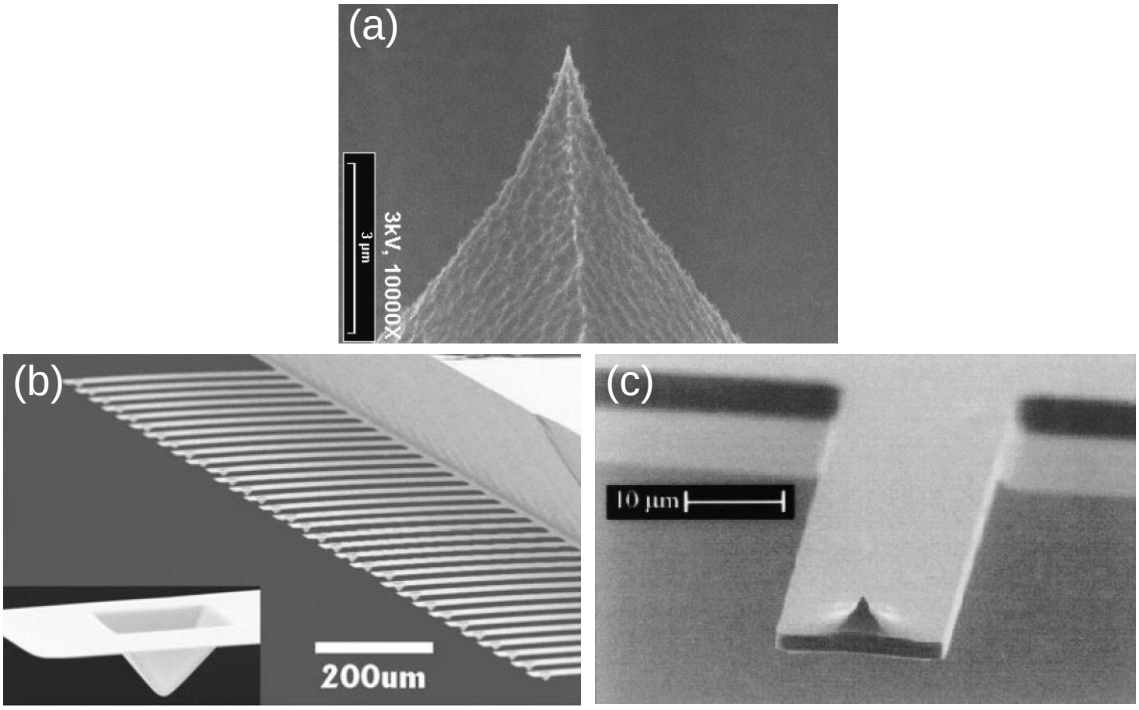

Fig. 4. Bulk micromachined silicon AFM probe tips [13-15].

distal ends. The bimorph structures were consisted of oxide (low thermal expansion coefficient) and aluminum layers (high thermal expansion coefficient) and act as thermal actuators. The bimorphs were anchored to substrate from one end which upon release elevates the whole planar structure in z-direction due to residual stress induced bending in bimorphs (due to mismatch in thermal expansion coefficients of bimorph layers) (Fig. 5). The elevation of more than 600 µm creates enough room for micromirror plate to scan large angles. Differential heating of bimorphs changes their bending angles and hence beam scanning in different directions can be achieved.

2.2. RF Passive devices

Integrated circuits and systems continue to be among the leading fields, for many RF engineers, scientists and research teams around the globe. With newly emerging wireless communication demands such as 5G, realization of fully integrated systems with high performance on-chip components is critical. Likewise, the integration of many high performance passive devices like inductors, capacitors and transformers is very important since they serve as the fundamental building blocks of many RF circuits and their performance largely affects the overall circuit specifications [22-26]. Fortunately, the evolution of silicon-based process technologies has allowed, to a large extent, the fabrication of high quality passive components using some 3D fabrication techniques.

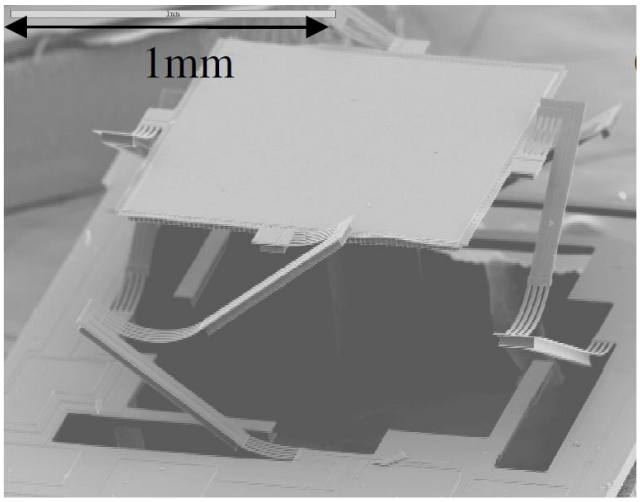

Fig. 5. Elevated MEMS micromirror formed using deformation in bimorphs [21].

Among the passive components, on-chip inductors and transformers are important elements in RF design and they are used in many circuits including low noise amplifiers (LNAs) [22-23], voltage-controlled oscillators (VCO) [24], impedance matching circuits [27], DC isolation circuits [28] and in baluns for power conversion between single-ended and differential-ended circuits [29-30].

In standard CMOS processes, microelectronic devices are fabricated on a substrate material (e.g. silicon, gallium arsenide) and existence of this underlying substrate severely degrades the performance of passive components because of substrate coupling and flux leakage [31]. MEMS, however, has allowed to fabricate out-of-plane 3D on-chip components using different micromachining techniques to decrease substrate proximity effects as well as the overall area requirements [32-33].

A simple method to produce double layer tunable on-chip inductor using bulk etching of substrate was proposed [34]. First, 600 μm thick silicon nitride was deposited on silicon substrate acting as a bottom layer of inductor. Next, a gold metal was deposited and patterned acting as top metal layer. Final step involved anisotropic etching of silicon using KOH where nitride film served as a mask. A 300 μm deep cavity was formed which reduced the substrate parasitics significantly and a quality factor of more than 15 was achieved for such inductors (Fig. 6).

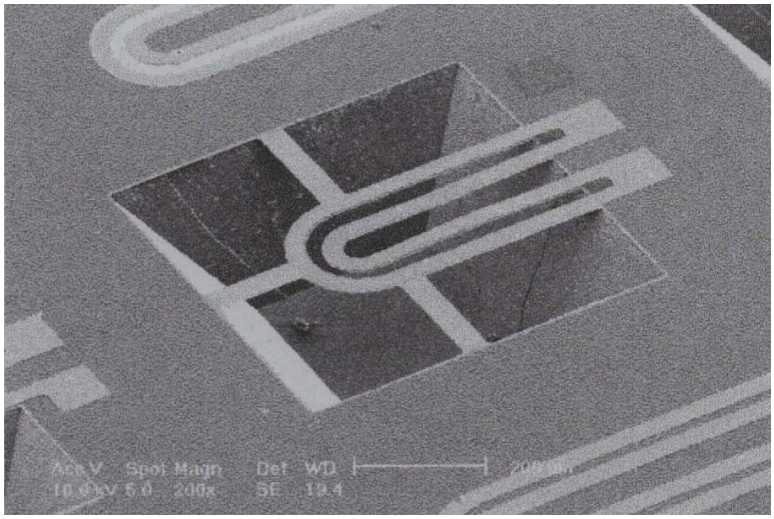

Fig. 6. A high Q on-chip inductor with cavity underneath to avoid substrate proximity affects [34].

CHAPTER. 3

MEMS Based 3D Microfabrication Methods

Fabrication of out-of-plane 3D on-chip components generally involve different MEMS micromachining techniques. The micromachining can be further classified into two types; 1- Bulk Micromachining, 2- Surface Micromachining. As the name suggests, the bulk micromachining process requires removal of substrate material in bulk using either isotropic or anisotropic etching (to be discussed in next section). The surface micromachining, contrarily, involves fabrication of microstructures on substrate by depositing and patterning new materials on the substrate using different techniques including lithography, etching, deposition and sacrificial release etc. As opposed to bulk micromachining, surface micromachining does not require bulk etching of the substrate material. The two classes of micromachining are discussed in details in the following sections:

3.1. Bulk Micromachining

Bulk micromachining is an important class for 3D MEMS fabrication technique and has various applications especially in the area of silicon based sensors and actuators [35]. Bulk etching is commonly used to fabricate free standing structures (cantilevers, diaphragms etc.). It can also be used to create complex 3D structures including holes, cavities and other high aspect ratio structures. However, bulk micromachining can be applied to any substrate (i.e. gallium arsenide, silicon or glass etc.) but most of the applications to this technique link with silicon due to its electrical and mechanical properties, making it compatible with many microfabrication applications (e.g. microelectronics and micromechanics etc.), hence promising the system integration [36-37].

Bulk micromachining technique can be categorized into two parts depending on the nature of etching (either isotropic or anisotropic) which directly translates the etch profile of the material (Fig. 7). If the etch rate is uniform in each direction then etch is considered to be isotropic, however, if there is a difference in etch rates with respect to direction or an orientation of substrate material then the etching is known to be anisotropic. Fig. 7 explains the idea of isotropic and anisotropic etching. Moreover, different nature of etchants is also available for both isotropic and anisotropic etching requirements. Etchant could be in the form of liquid (e.g. HF, KOH and HCL etc.) or gas (e.g. SF_6, CF_4 and XeF_2 etc.) [38]. The former is called as wet etching, whereas the later one is named as dry etching. To elaborate on the concept of bulk micromachining, we will be considering silicon substrate as a target material in the next sections.

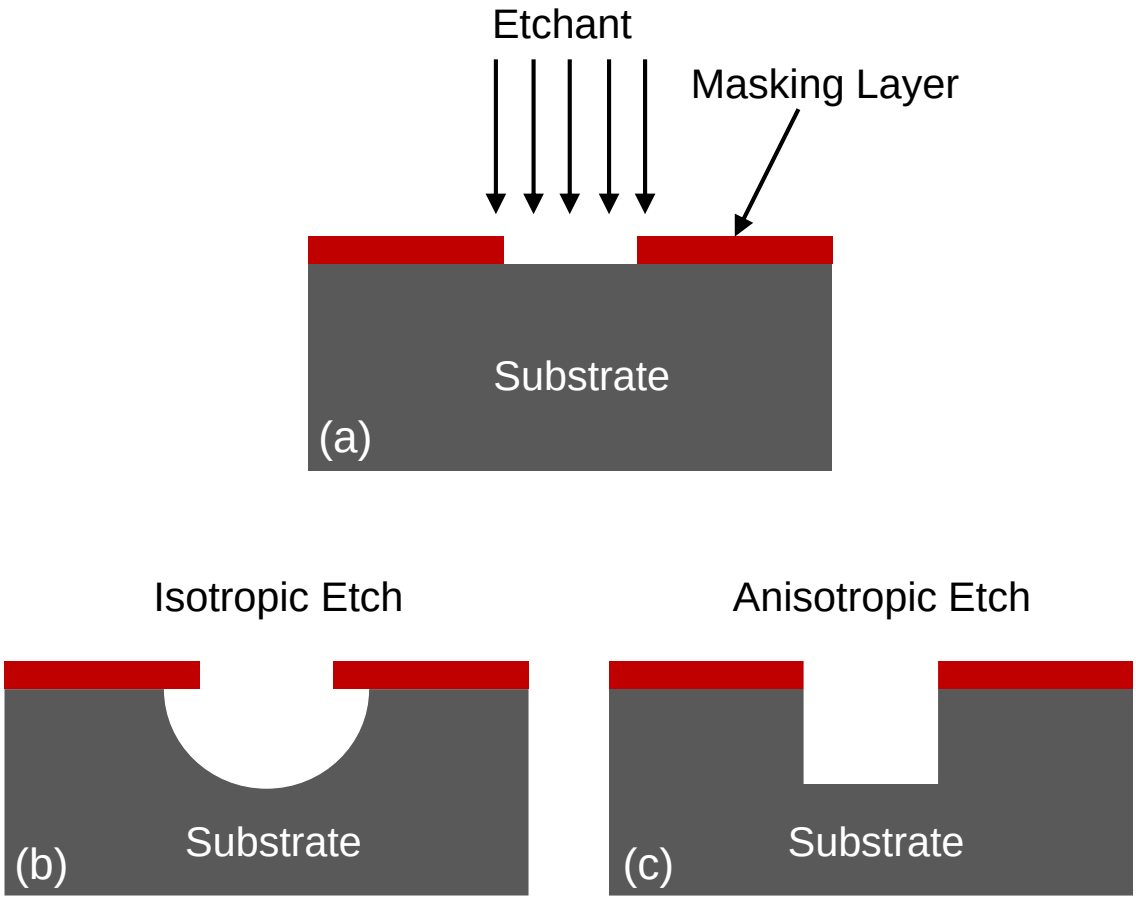

Fig. 7. Difference between isotropic and anisotropic etching; (a) Substrate before etching (b) Isotropic etch profile (c) Anisotropic etch profile.

3.1.1. Wet etching of silicon

Wet etching of any material is usually considered to be isotropic because it involves

immersion of material into the etchant (liquid form). Thus, material is exposed to etchant from every side creating an isotropic etch profile. However, silicon being a crystalline material shows different etch rates in different crystal directions (for some specific wet silicon etchants). Etch rate along <111> direction is lowest as compared to etch rates in other directions e.g. <100> and <110> directions. The etch rates for silicon in 30% KOH solution are 0.797 μm min^{-1}, 1.445 μm min^{-1} and 0.005 μm min^{-1} for crystal directions of <100>, <110> and <111> respectively [39]. Since etching in <111> direction is very slow as compared to other directions, the etching of <111> plane can be safely ignored [40]. The difference in etch rates generates an anisotropic etch profile (for <100> silicon wafer) with sidewalls at an angle of 54.7º [39] [40]. Likewise, it can be seen that opening in the mask *w* describes the final etch profile of silicon wafer also known as self-limiting stable profile (SLSP) [40]. The final etch profile (if the etch is not manually stopped) is either a hole or a blind end cavity terminating to a point or a line depending on the size of opening on the mask. Different obtainable anisotropic etch profiles for <100> silicon wafer using KOH are shown in Fig. 8. This method of bulk anisotropic etching of silicon can be used to fabricate various suspended structures and membranes for sensing and actuating applications Fig. 9.

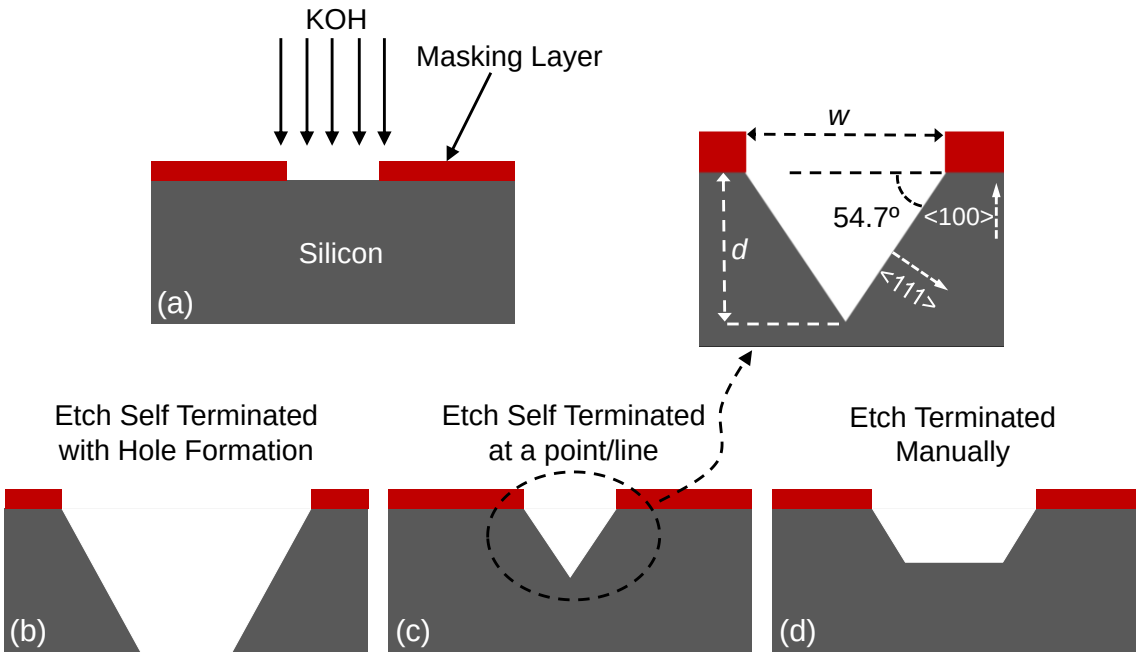

Fig. 8. Anisotropic etching of silicon; (a) Silicon substrate before etching (b) Self-limiting stable profile with formation of hole (c) Self-limiting stable profile terminating at a point/line (d) Etching manually stopped after some time to achieve a desired etch depth.

The reason for different etching rates for silicon along different crystal directions is still not completely revealed. However, since the silicon wet etchants etch the silicon by first oxidizing it and then removing the oxide using oxide etching components present in the etchant, it can be assumed that the difference in the etch rates is due to the different oxidizing rates in different crystalline directions. Although, this is just an assumption and no particular evidence explaining such phenomenon exists in literature [40].

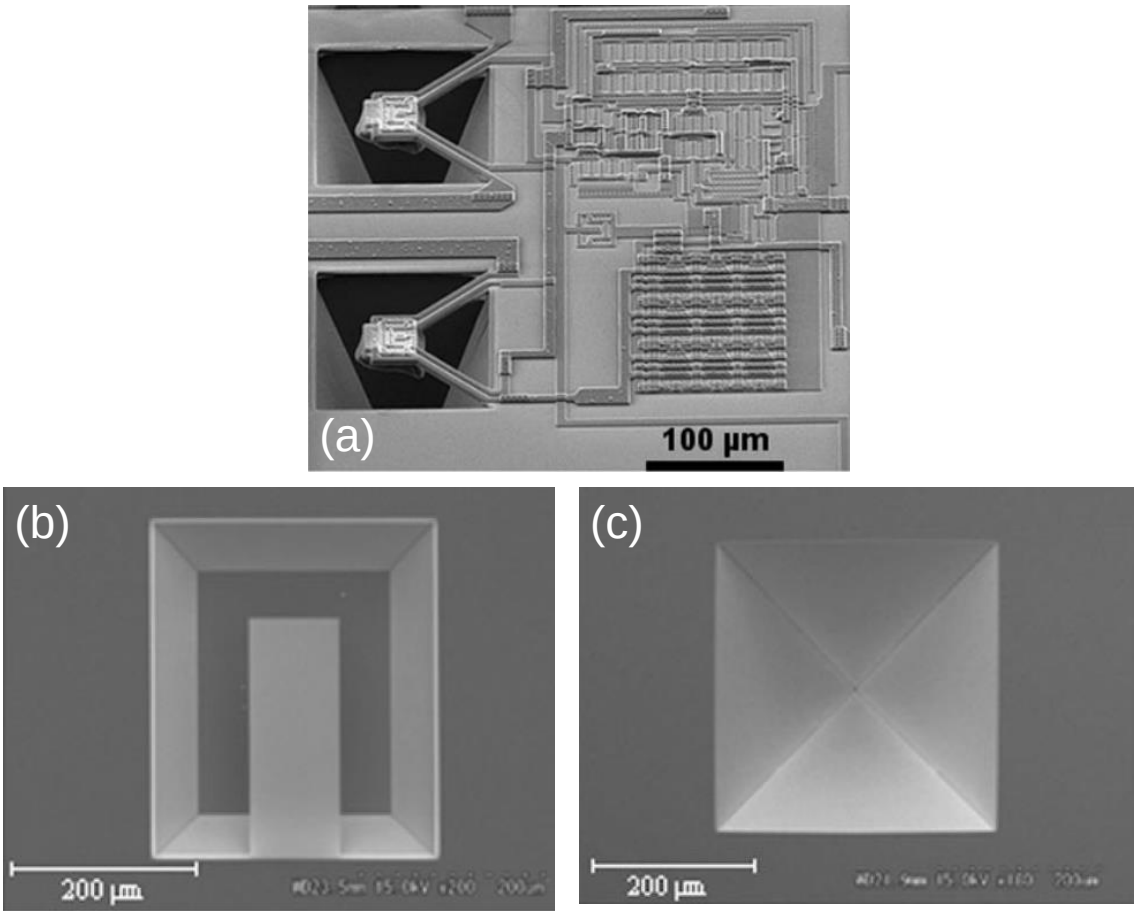

Fig. 9. (a) Anisotropically etched silicon beam in CMOS based microelectronics circuitry [35]; (b) Anisotropically etched free standing cantilever [41]; (c) SLSP anisotropic etch profile of silicon terminating at a point [41].

The etchants frequently used for anisotropic etching of silicon are EDP (ethylene diamine pyrocatechol) and KOH (potassium hydroxide). EDP has negligible etch rates for silicon dioxide and silicon nitride providing higher selectivity for cases where oxide or nitride is used as a mask. However, this higher selectivity could also cause problems in etching when silicon has thin layer of grown native oxide on it stopping the etchant to reach silicon surface. The selectivity of KOH, on the other hand, is smaller than that of EDP with etch rate of few angstroms for oxide.

Other than these conventional methods, there have also been attempts to create anisotropic etching profiles of silicon irrespective of its crystalline nature. Since the side walls are always at 54.7º, there is an aspect ratio limitation for KOH based silicon etching and the depth of etch cannot exceed a particular value and usually comparable to feature size of the structure. To overcome these limitations, a method to develop high aspect ratio silicon microstructures with vertical sidewalls was proposed [42]. The etchant used in this method was a mixed solution of HF (hydrofluoric acid), H_2O_2 (hydrogen peroxide) and EtOH. The process used the concept of metal-assisted chemical etching which states that a thin layer of noble metal deposited on silicon substrate acts as a catalyst in chemical etching. Accordingly, the etch rate on silicon surface underneath the metal gets much higher as compared to the surface with no metal coverage forcing noble metal (gold) to sink into the silicon substrate. Finally, the metal is etched away as the desired depth of silicon structures are achieved. This technique is used to create high aspect ratio structures such as silicon microwires etc. The work reported 60 μm deep cavities with feature size of just 2 μm Fig. 10.

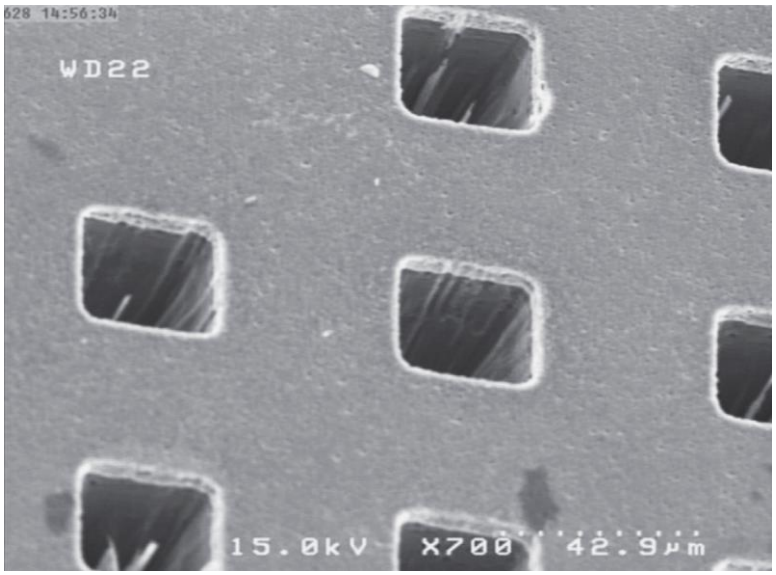

Fig. 10. Metal assisted silicon anisotropic etch to create 60 μm deep cavities [42].

Similarly, isotropic etch of silicon is also possible using many wet etchants. Typically, HNA is used for isotropic etching of silicon consisting of hydrofluoric acid (H), nitric acid (N) and acetic acid (A). Different ratios of these acids in HNA solution are possible hence resulting in different etch rates. Practically, anisotropic wet etch of silicon is more popular due to its vast range of applications, however, isotropic etching can still be used

in combination with anisotropic etching to obtain complex 3D microstructures for various applications [43].

3.1.2. Dry etching of silicon

Dry or gaseous phase etching of silicon plays a significant role for the applications where anisotropic etch is required. The process has gained a lot of attention in bulk micromachined 3D fabrication technology due to variety of advantages it has to offer including faster etch rates, capability of working at room temperature, dry process (involvement of liquid which usually causes problems related to surface tension and stiction) and etch selectivity etc. Dry etching is a plasma based etching technique and works at lower pressure values. The etch profile can be controlled in dry etching and can be varied from isotropic and anisotropic by changing its parameters e.g. pressure, temperature, power and etchant type etc. [40].

A new class of dry etching also known as deep reactive ion etching (DRIE) for creating anisotropic etch profiles with nearly vertical side walls for high aspect ratio microstructure applications was proposed by Robert Bosch and Texas Instruments collectively [44-45]. The multiple step etch process starts with etching of silicon to create a trench. Next, a thin passivation layer is deposited on both side walls and bottom surface of the trench. Passivation layer is then removed from bottom surface of the trench using ion milling technique while keeping the side walls unaltered (due to anisotropic nature of ion milling in vertical direction). Passivation of these side walls prevents the etching of silicon in horizontal direction in subsequent silicon etch steps. The combination of passivation and etch steps are repeated until the desired depth is achieved. Various structures fabricated through gaseous phase etching can be seen in Fig. 11.

Isotropic etch of silicon can also be achieved using gaseous phase etch process. XeF_2 and BrF_3 are typical etchants for applications where isotropic dry etch is required. However, isotropic dry etch is not used very commonly since isotropic etching using wet etchants is also possible providing an equivalent cheap solution as compared to expensive dry etch process.

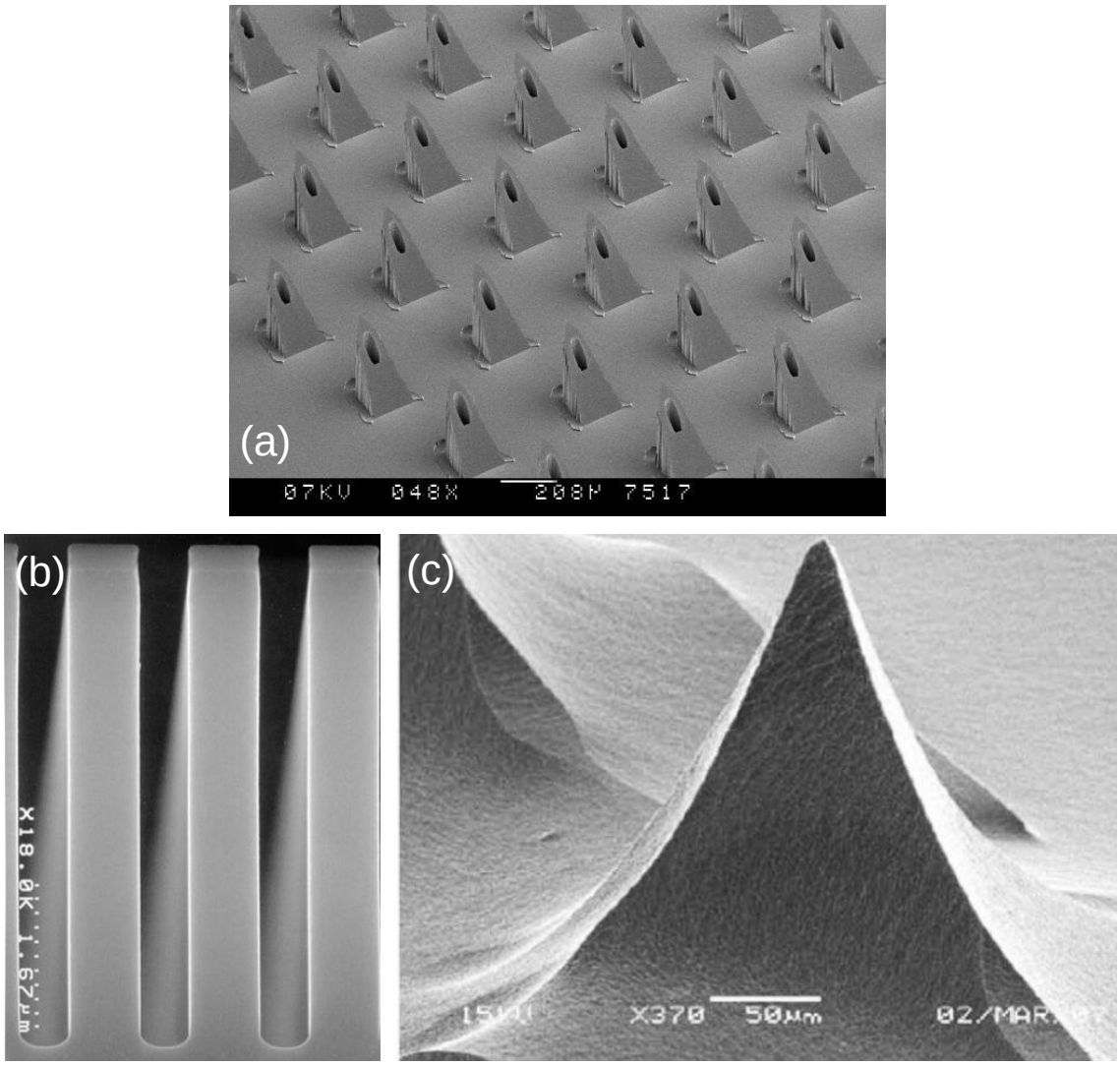

Fig. 11. (a) An array of hollow microneedles formed using dry etching [46]; (b) Deep trench structures created through DRIE [47]; (c) Silicon needles create using DRIE with no passivation step [48].

3.2. Surface Micromachining

Surface micromachining is a MEMS fabrication technique responsible for developing microstructures near the surface of substrate using different types of patterned thin films. Unlike bulk micromachining, this technique is used to create microstructures coming out of the substrate using deposited films. The technique of bulk micromachining is completely dependent on substrate etching whereas surface micromachining involves fabrication of microstructures by adding different materials to the substrate hence provides better compatibility as well as wider range of applications.

Surface micromachining is responsible for creating out-of-plane micro components using different techniques including self-assembly, various photoresist processing

techniques and electroplating etc. [49]. The concept of sacrificial layer plays a vital role in every surface micromachining technique which involves fabrication of suspended 3D elements on substrate. The concept was first proposed in 1960s to create free standing surface micromachined structures where resonant gate transistor was fabricated using vibrating suspended gold beam [50]. Sacrificial layer is usually a thin layer of material (oxide, photoresist, aluminum etc.) deposited and patterned on substrate. Next, a structural layer is deposited on top of the sacrificial layer and patterned in such a way that the parts which are aimed to be suspended lie on sacrificial layer whereas other parts serve as anchor points and are directly connected to substrate through the via holes created in sacrificial layer patterning step. Removal of sacrificial layer (often named as sacrificial etch or sacrificial release) in the end of whole process results in free suspended microstructures. Fig. 12 explains the idea of sacrificial layer for developing free standing microcantilever.

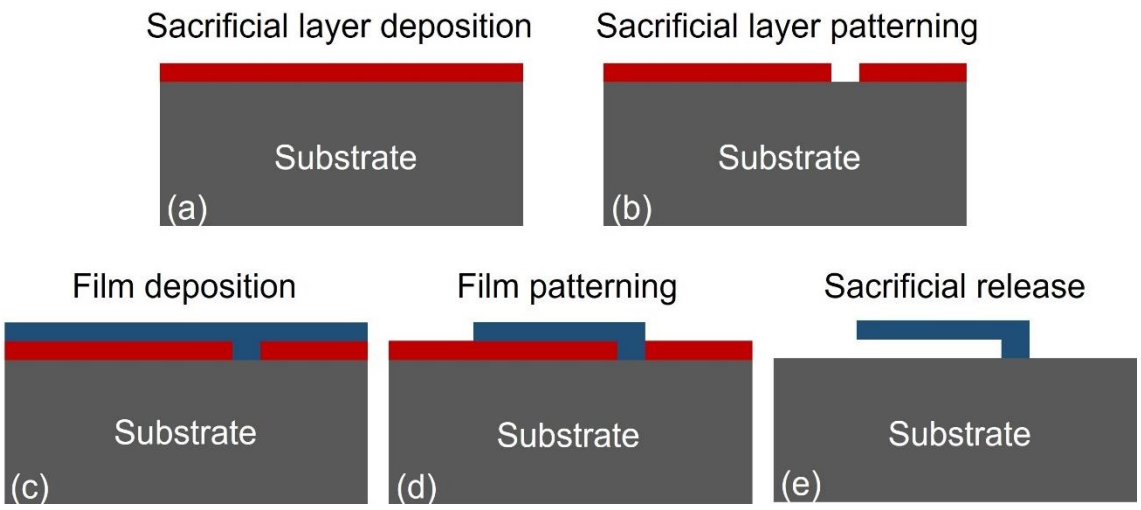

Fig. 12. Cross-section view of sacrificial release process to create suspended cantilever: (a) Sacrificial layer coated substrate; (b) Sacrificial layer patterning; (c) Structural film deposition; (d) Structural film patterning; (e) Sacrificial etch to release the cantilever.

The material and etchant selectivity is also crucial in sacrificial release based processes because sacrificial layers are not part of final device and hence they should not affect or degrade the actual properties of device in any way. Consequently, there are few considerations for choosing the etchants in sacrificial layer based microfabrication processes; 1- The sacrificial layer and its etchant should no etch any other layer in process, 2- The materials and etchants used in the process should not affect the sacrificial layer [40].

The suspended structures obtained using sacrificial release process are often subjected to various post processes to achieve complex out-of-plane structures for different applications e.g. high performance on-chip inductors [51], microhinges for actuating applications [52], self-assembled flow sensors [53] and micromirrors [54] etc. The processes to develop these high performance out-of-plane 3D on-chip elements are discussed in detail as follows:

3.2.1. Self-Assembly

Self-assembly can be defined as organization of structure into a specific shape without involvement of some external human intervention [55]. Self-assembly technique can be applied to suspended micromachined microstructures to transform them into complex shaped 3D structures. Self-assembly can be achieved through various methods e.g. magnetic self-assembly [56], stress induced self-assembly [57], thermal self-assembly [58] and self-assembly using surface tension [59] etc.

A technique named as PDMA (plastic deformation magnetic assembly) was proposed by Zou *et al*. to convert 2D suspended structures into magnetically assembled 3D out-of-plane vertical structures [56]. The idea was elaborated on suspended gold microcantilevers. The portion of gold cantilever was covered with magnetic material ($Ni_{80}Fe_{20}$) using electroplating. Next, a magnetic field in the vertical direction was generated through an external source to magnetize the magnetic material. As an intrinsic property of magnetic field, magnetic material experienced a force in the direction away from the substrate causing a torque generation in $Ni_{80}Fe_{20}$ coated gold cantilever. The torque caused the beam to rotate and angle of rotation was proportional to the amount of external magnetic field. Interestingly, gold being a ductile material, undergoes plastic deformation (from flexible region to plastic region) when the bending angle exceeds a threshold value (due to increased stress in gold beam). Hence, permanent deformation in the beam can be achieved converting conventional 2D cantilever to convert it into a vertical beam. The concept is useful for various applications including high *Q*-factor vertical inductors (Fig. 13).

Use of surface tension to convert planar inductors into self-assembled vertical inductors with high *Q*-factor was proposed [60]. Horizontal structures were first fabricated using standard sacrificial layer based surface micromachining techniques. Before sacrificial layer etching, solder pads were placed between the anchored point and

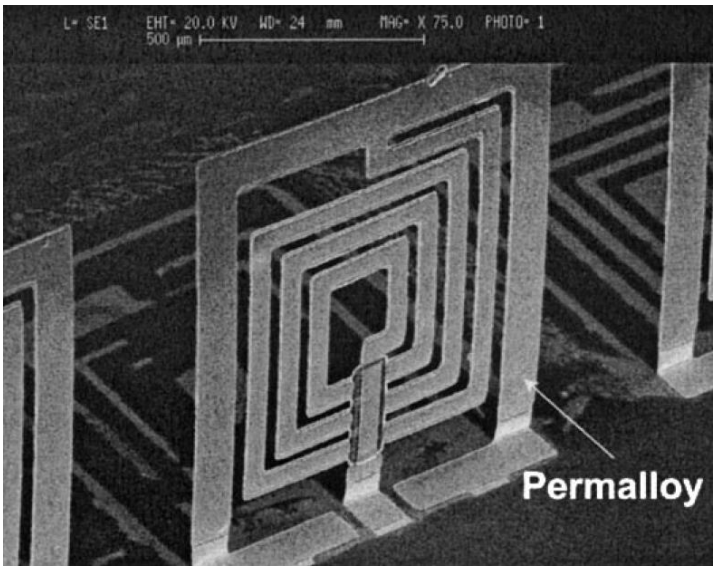

Fig. 13. Vertical inductor fabricated using plastic deformation magnetic assembly (PDMA) [56].

the part which is to be released. Solder pads acted as a connection point between two parts of microstructure since there is no direct mechanical connection between anchored point and the released portion of structure. Afterwards, sacrificial layer was removed to make free standing suspended structures joined to anchor point through solder pads. Next, the solder pads were melted by heating the substrate. Accordingly, melted solder pads were contracted due to increased surface tension and hence acting as hinge drive for underlying planar structures inducing rotation in the structures. The solder pads were then cooled down to preserve the achieved bending angles and vertical out-of-plane inductors were realized (Fig. 14).

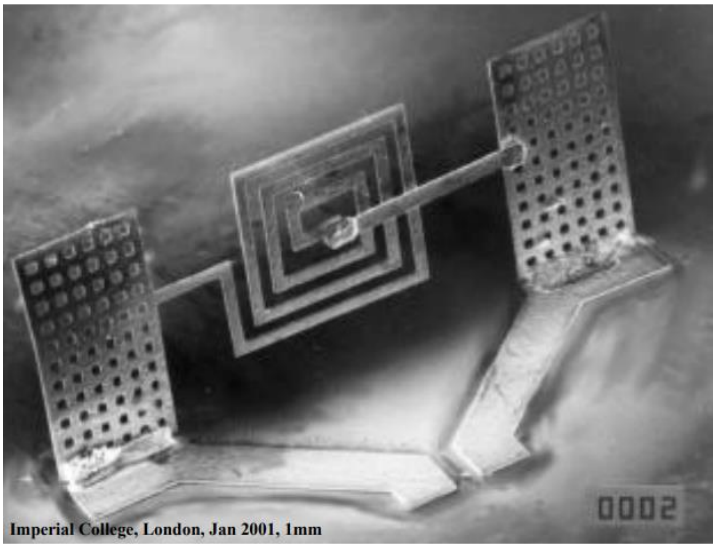

Fig. 14. Self-assembled inductor using surface tension of solder pads [60].

Similar method of surface tension induced self-assembly was used to fabricate out-of-plane micromirrors [61]. However, this process used SOI (silicon on insulator) to develop silicon based micromirrors where sandwiched silicon oxide layer between two silicon layers of SOI was used as a sacrificial layer. Top thin silicon layer of SOI was patterned to create the geometry of desired micromirrors. Photoresist material was used to connect anchor point with suspended part of microstructure prior to sacrificial release process. Melting of photoresist caused upward bending in the released part of structure due to increased surface tension of photoresist material. Fig. 15 shows 45º micromirrors constructed using this technique.

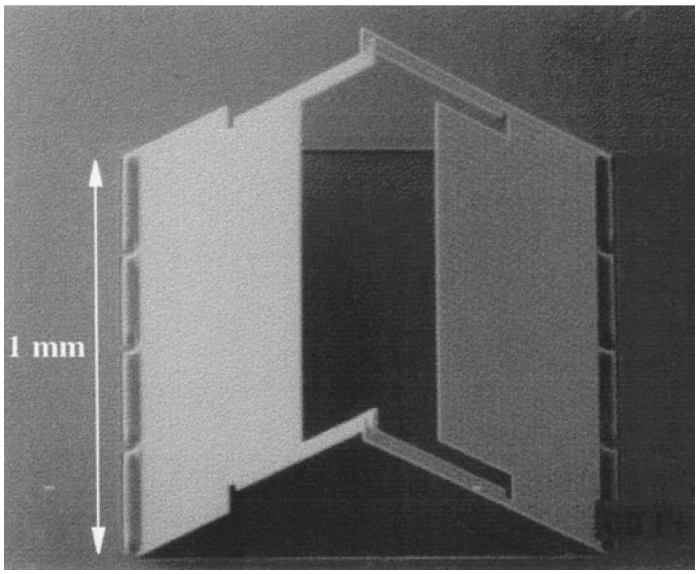

Fig. 15. Self-assembled MEMS micromirrors using surface tension of photoresist material [61].

Thermally induced self-assembly is also a promising technique to batch fabricate 3D on-chip components [58, 62]. First a structural layer of silicon oxide was deposited and patterned on a silicon substrate. Patterned polyimide material was used to act as a hinge on top of silicon oxide microplates. Isotropic silicon dry etching was performed to release the oxide plates. Furthermore, polyimide hinges were heated in the furnace which caused them to compress and hence they forced the overall suspended microplate to bend away from the substrate. The bending angle was observed to increase with the increase in temperature and hence vertical profile of microplates was also achieved (fig. 16).

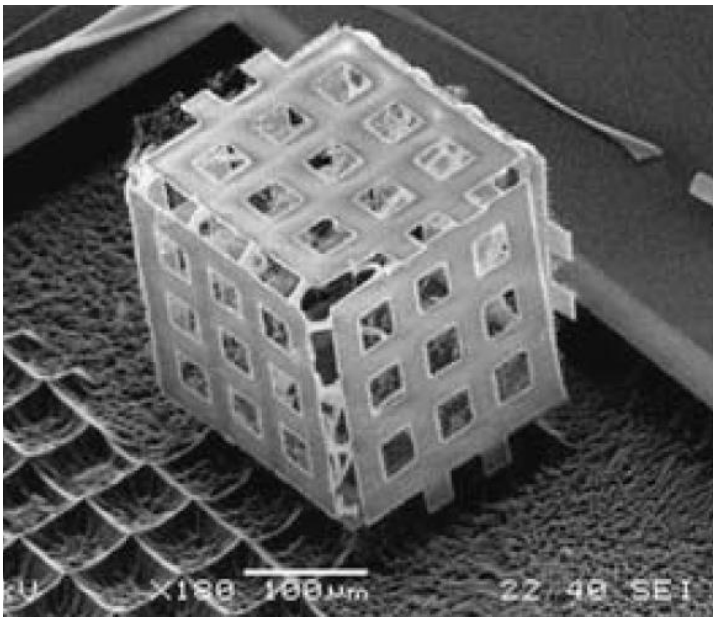

Fig. 16. Thermally induced self-assembly to form cage type structure [62].

Other methods to achieve self-assembly include self-assembly due to intrinsic stress in patterned thin films which is considered to be very promising technique for developing complex 3D microstructures for various on-chip applications [32, 57]. Various attempts to realize self-assembly using internal stress are described in detail in Chapter 3.

3.2.2. Thick Photoresist Processing

Since the development of thick photoresist materials such as SU-8, there have been a lot of attempts to produce high aspect ratio out-of-plane on-chip components using these thick materials especially SU-8 photoresist [63]. SU-8 is capable of making high aspect ratio microstructures where aspect ratio can go up to 100:1. Since SU-8 is quite rigid material as compared to other photoresists, it can be even used as a structural layer for many on-chip application requiring 3D structures. However, this rigid behavior also makes it harder to remove from the substrate and long cleaning methods are required to strip off the residuals of SU-8 photoresist from substrate.

A method to produce high aspect ratio inclined structures using SU-8 was proposed in [64]. The idea was to expose SU-8 with UV light at some inclination angle as well as some rotation to form complex 3D structures Fig. 17. A substrate covered with SU-8 was covered with the lithography mask and hard contract was ensured to avoid leakage of any UV light into undesired area. Next, UV exposure was done at an angle of around 30º. Developing of such patterned photoresist resulted in inclined microneedles (Fig. 17a).

Similarly, introduction of substrate rotation along with inclined UV exposure, inverted cone type microstructures can be realized (Fig. 17b).

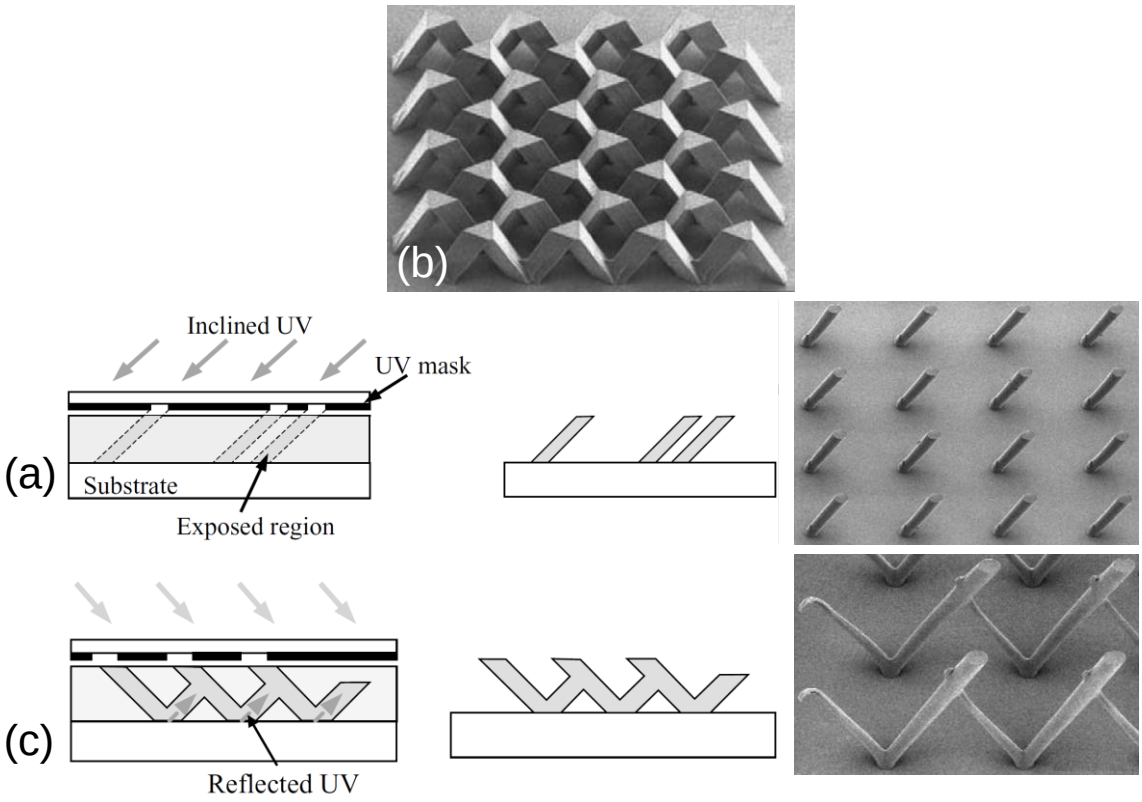

Fig. 17. (a) Inclined UV photolithography on SU-8 to form inclined structures; (b) Inclined UV exposure with wafer rotation; (c) Affects Reflected UV light with in the photoresist layer [64].

Additionally, effect of reflected UV light at the interface of substrate and SU-8 was studied since the UV light exposure is not normal to the substrate. For nominal exposure dose, the reflected UV light inside photoresist layer appeared to be too weak hence avoiding formation of any additional undesired structure. However, if the exposure dose is too high, it could force reflected UV light to expose the photoresist in its path hence producing complex shapes. Likewise, this idea was used to form an array of internally linked microwires (Fig. 17c).

Correspondingly, thick photoresists also finds various applications in the field of RF-MEMS. A thick photoresist based process to create on-chip inductors with thick metal layers was proposed [65]. Single layer SU-8 and multilayered AZ4562 and AZ9260 were used as resist material to obtain thickness of 70 µm, 75 µm and 81 µm respectively. These photoresist materials served as mold for electrodeposition of copper. Afterwards, 200 nm copper layer was deposited in the trenches to serve as a seed layer. Photoresist mold was

removed followed by electrodeposition of copper to realize thick metal inductors (Fig. 18). Inductors with thick metal layers resulted in higher *Q*-factor with the maximum value of 23 at 0.4 GHz.

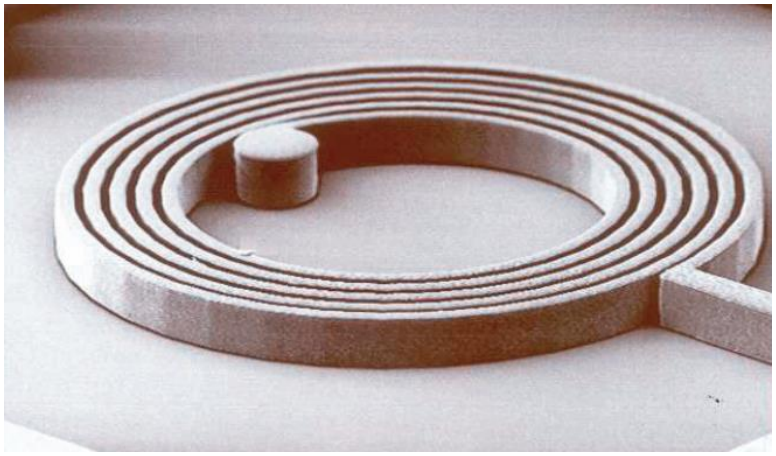

Fig. 18. Thick metal inductor using thick photoresist mold [65].

Similarly, an attempt to develop on-chip transformer elevated above substrate in order to reduce substrate proximity affects was made [66-67]. A thick photo resist was used to create sacrificial metal mold which was further used to fabricate the transformers at elevation ranging from 10 μm to 65 μm depending on the thickness of the resist (AZ9262). In same work, an inductor with elevation of 100 μm above from the substrate was also developed. Fig. 19 shows various on-chip inductors and transformers built using thick photoresist.

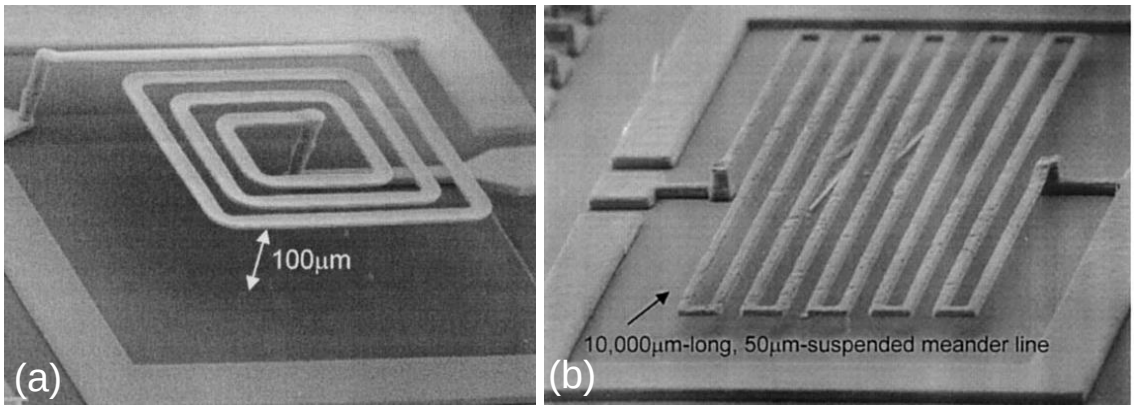

Fig. 19. Inductors at elevated heights using thick photoresist processing [67]: (a) 100 μm high suspended spiral inductor; (b) 50 μm elevated meander inductor.

Another approach based on thick photoresist processing was implemented to develop air-core solenoid on-chip inductors [68]. First, a bottom layer of metal was deposited and patterned on oxide coated silicon substrate. Next, a 40 μm thick photoresist SJR 5740

was spun and patterned as a thick rectangular block on top of bottom conductors. The photoresist was then cured at 120º for 6 hours where it reflowed and changed its shape. After curing, the corners of photoresist became smooth and it attained a bell-shaped profile. Likewise, top conductors were patterned on top of photoresist to form a solenoid with polymeric core. The photoresist was then removed in the end using acetone to finally achieve air-core solenoid inductor Fig. 20.

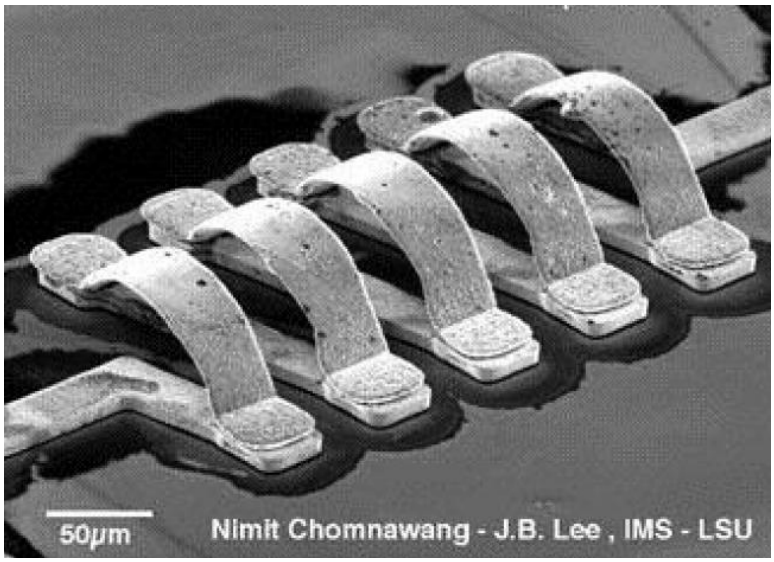

Fig. 20. Air core solenoid inductor fabricated using thick photoresist reflow technique [68].

CHAPTER 4

Internal Stresses in Thin Films and Self-Assembly

4.1. Concept of Internal Stress in Thin Films

When a layer of thin metal film is deposited on a substrate, tensile or compressive residual stresses are likely to develop in the deposited film which can cause the film to either contract or expand when released from the supporting substrate [69-71]. The type of intrinsic stress in the film, depends largely on the material properties, as well as the deposition technique (i.e. sputtering, evaporation etc.) and the actual deposition conditions (i.e. temperature, pressure, ambient gas etc.).

Internal stresses can build up in thin films due to various reasons and can be categorized into two major types; 1- The stress in thin films occurring during the thin film growth also known as intrinsic stress of the material. These intrinsic stress values are totally dependent on grain growth mechanisms of thin films where various factors (grain boundaries and grain size etc.) could play their role as the deposition of thin film progresses. For instance, in the early stages of thin film deposition, the film starts with the growth of isolated grain islands. As the deposition continues, the gap between different grain islands starts to decrease and hence cohesion of two adjacent grain islands occur. Likewise, strain is developed in thin films as the grain islands reshape to link with surrounding grain islands causing a net tensile stress in the film [72]. Due to complex factors governing the intrinsic stresses of thin film, there is no direct way to calculate intrinsic stresses in thin films. However, stress values can be estimated to some extent using different thin film models found in literature [73]. 2- The stresses occurring in thin films due to thermal coefficients of expansion of materials known as residual stresses in thin films. Since the evaporation is carried out at elevated temperature, the material being evaporated having some finite value of thermal expansion coefficient expands during the deposition. After deposition, the temperature starts decreasing hence forcing the thin film

to shrink itself corresponding to the thermal expansion coefficient associated with the respective material. Since the thin film cannot compress due to presence of underlying substrate, an overall compressive stress builds up in the thin film. The residual stresses due to thermal expansion can be estimated using different models since the deposition temperature and thermal coefficient of material and substrate are known.

By engineering stress gradients in multi-layer structures such that differing magnitudes and/or modes of residual stress (i.e. tensile or compressive) exist in each layer, effective transverse bending of the entire structure in either upward or downward direction can be achieved (Fig. 21). Accordingly, increasing tensile stress gradients from the sacrificial layer to the top surface of the thin-film stack will cause upward bending of the film upon release (Fig. 21a); and, tensile stress gradients increasing towards the sacrificial layer will result in downward bending (Fig. 21b). Opposite behavior is observed for compressive stress gradients, where increasing stress towards the sacrificial layer cause upward bending (Fig. 21c); and increasing stress away from the sacrificial layer cause downward bending (Fig. 21d).

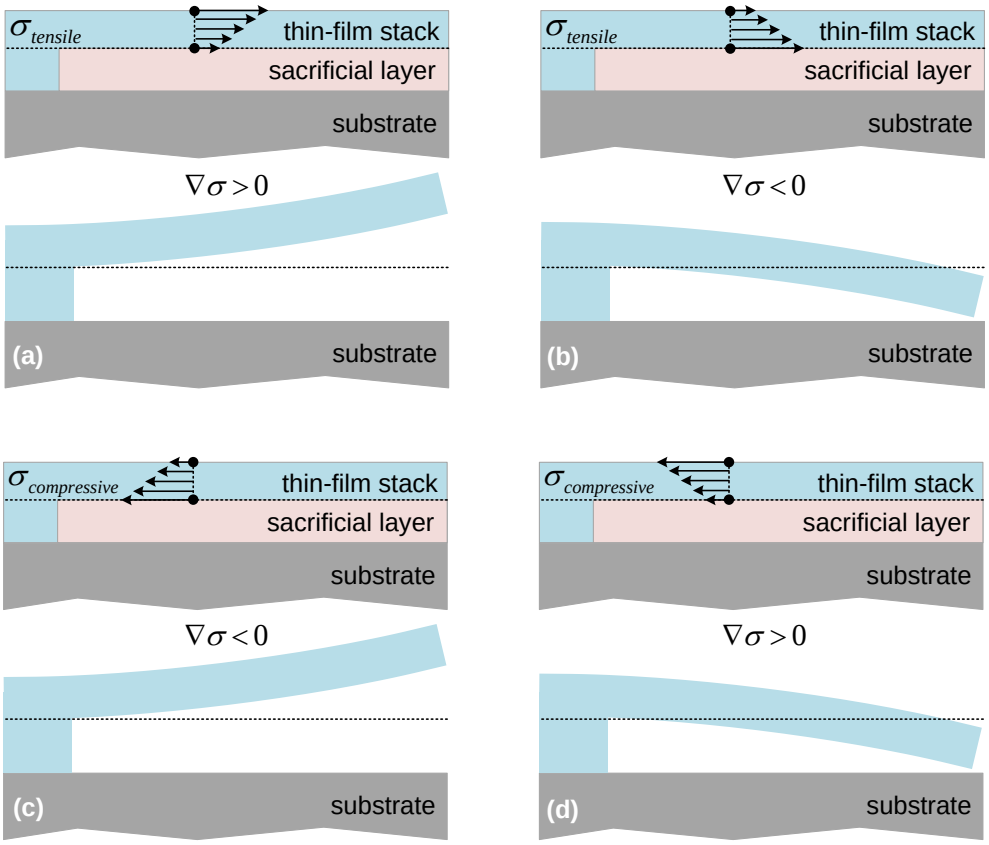

Fig. 21. Intrinsic stress-induced post-release bending in multi-layer thin film stacks due to tensile and compressive stress gradients.

Amount of bending in patterned bi-layer films depends on several factors including thickness of the film, substrate type and deposition temperature, to name a few. Stoney first observed the effect of stressed films on substrate in 1909 [74]. Nickel metal when electro-deposited on silver coated glass substrate resulted in peeling off the Ag-Ni film in the form of curls. The phenomenon happened due to tensile internal stresses of Ni film which caused the bilayer (Ag-Ni) to bend away in the form of curls. Hence, Stoney came up with an equation to measure the amount of internal stresses in thin films deposited on bare substrate using bending information. For measurements, first a target metal layer was deposited on substrate and radius of curvature induced by stresses in thin films was measured. The radius of curvature was further used to derive a simple equation for calculation of internal stress values. The Stoney's equation, which also governs the amount of stresses on metal films deposited on a substrate with respect to given conditions is given as follows:

$$\sigma = \frac{Et_1^2K}{6t_2(1-v_s)} \tag{1}$$

where σ is the amount of stress, K is the radius of curvature, t_1 and t_2 are the thicknesses of substrate and film, E is the elastic modulus of the substrate, and v_s is the Poisson's ratio. Following Stoney's approach, there have been other efforts to model stress in thin-films [75-76].

4.2. Internal Stress Induced Self-Assembled 3D Microstructures

Interestingly, the concept stress induced bending has allowed us to build on-chip self-assembled components for vast number of applications [53, 70]. The idea is to convert convention 2D structure in to vertical direction for applications where sensing in horizontal direction is required e.g. internal stress induced self-assembled airflow sensor [53]. SiO_2/Al cantilevers were built on SOI wafer. Upon release, the cantilever structures were bent away from substrate due to mismatch of internal stresses between silicon oxide and aluminum layer interface (Fig. 22). These bent up cantilevers were used as sensing elements for air flow. As the flow rises, the bending angle of microcantilever changes which can be further translated into flow rate information. These types of internal stress based self-assembled anemometers have edge over conventional hot-wire anemometers because no static current consumption for hot-wire is involved in this case and hence can be considered as energy efficient sensors [53].

Similar approach to fabricate bent up and rolled up cantilevers was proposed [77]. Nitride/aluminum bi-layer was then deposited on patterned top thin silicon layer of SOI wafer. Structures were released by etching of oxide layer of SOI and stress-free microcantilevers were obtained. These cantilevers were then subjected to rapid thermal annealing (RTA) at 600º C inducing stress in top layers and hence bending the cantilever

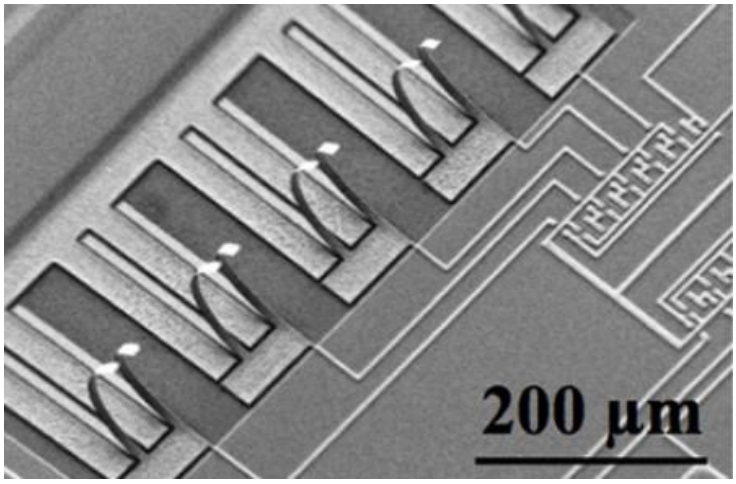

Fig. 22. Stress induced self-assembled cantilever based flow sensor [53].

in upward direction (Fig. 23). The concept was used to fabricate various flow sensing elements as well as passive out-of-plane RF components. Moreover, these cantilevers were also used as thermal sensors, since their bending angles are dependent on thermal conditions hence can be used to translate heat changes in to bending angles.

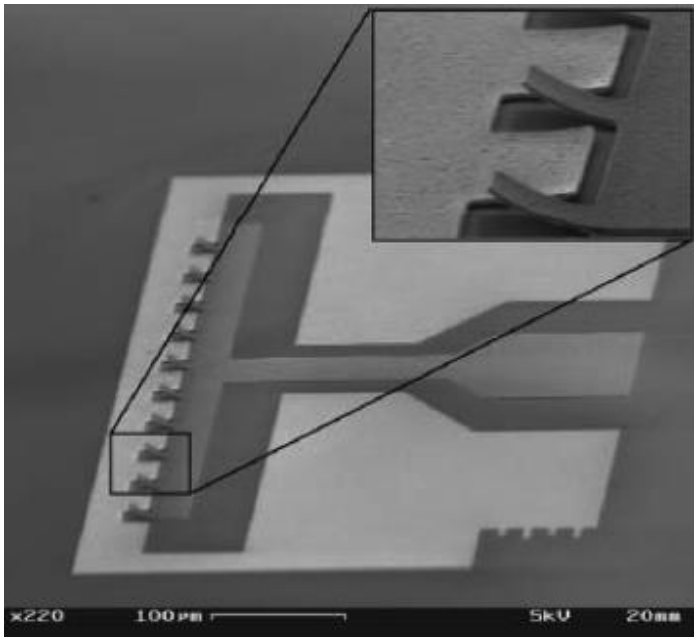

Fig. 23. Cantilever based thermal stress driven temperature sensor [77].

Concept of self-assembly by internal stress was also used to fabricate high-performance on-chip passive components (i.e. inductors and transformers). The idea was first exploited in early 2000s where a direction to fabricate vertical inductors was given using stress induced bending in thin films [78]. However, instead of metal, structural layers of inductors involved the use of polysilicon (semiconductor) as a stressor layer which somehow limited the electrical performance of the inductor. Despite using polysilicon, the *Q*-factor of inductor still assumed the highest value of around 13, hence promising fabrication of high-performance on-chip vertical inductors using stress induced self-assembly (Fig. 24).

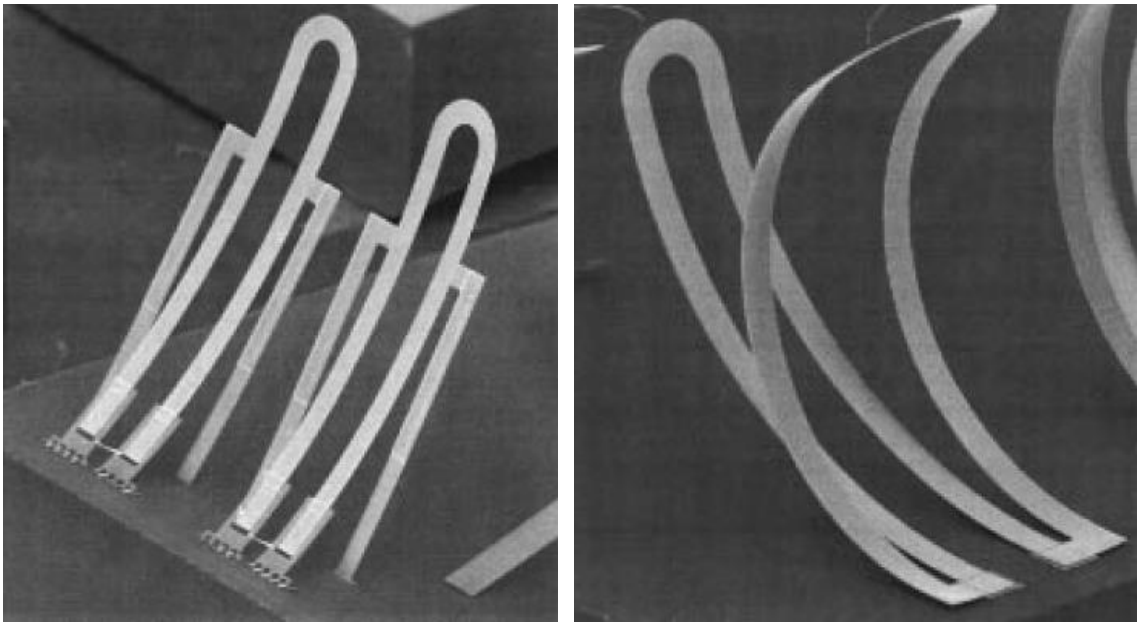

Fig. 24. Earliest attempt to fabricate internal stress induced self-assembled inductors [78].

A later attempt to develop high *Q*-factor inductors using a sputtered thick layer of molybdenum-chromium alloy (MoCr) was put together [79]. Sputtered metal layers tend to develop tensile stress at high pressure values whereas compressive stresses are developed when deposited at low pressure values. Same idea was used here and a single layer of MoCr with a stress gradient (-2 GPa to +2 GPa) along its thickness was sputtered on sacrificial layer coated substrate. MoCr layer was then patterned into a double-sided cantilever and then released using wet etch. The double-sided cantilever curled up and both free ends of double-sided cantilever joined together to make a solenoid shaped structure (Fig. 25). MoCr is a bad conductor of electricity, hence an copper electroplating

step was introduced in last to enhance the electrical performance of inductor. Owing to solenoid shape, the inductor exhibited a maximum *Q*-factor of 70 at 1 GHz.

Progressively, a very recent work reports a unique design of on-chip transformer fabricated using roll-up of released silicon nitride membrane [80]. First, a sacrificial Ge layer was deposited on substrate using electron beam deposition. Next, two silicon nitride

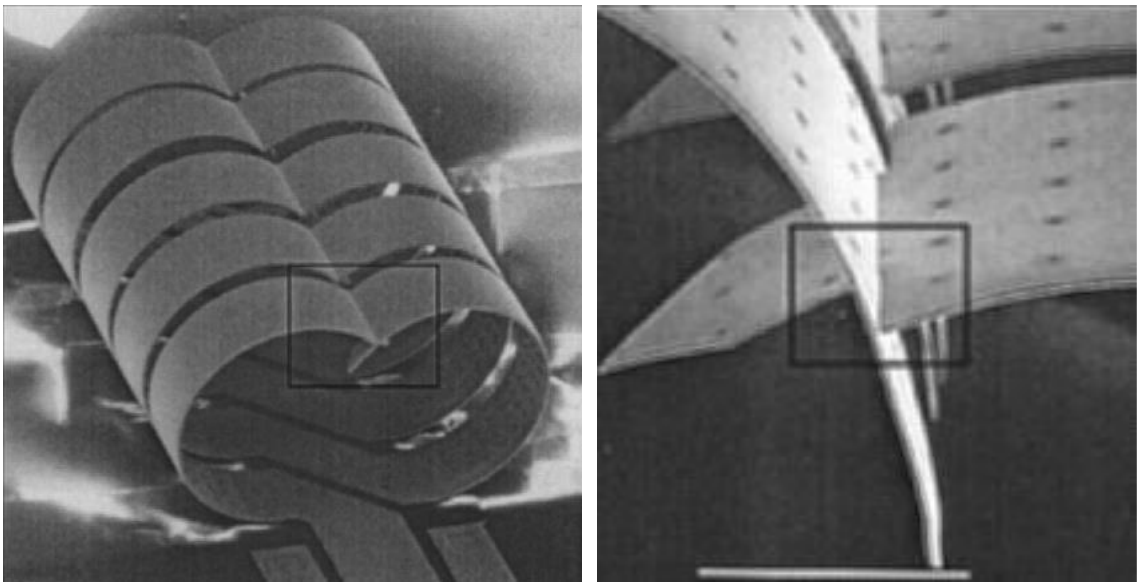

Fig. 25. MoCr alloy based high *Q*-factor solenoid inductor [79].

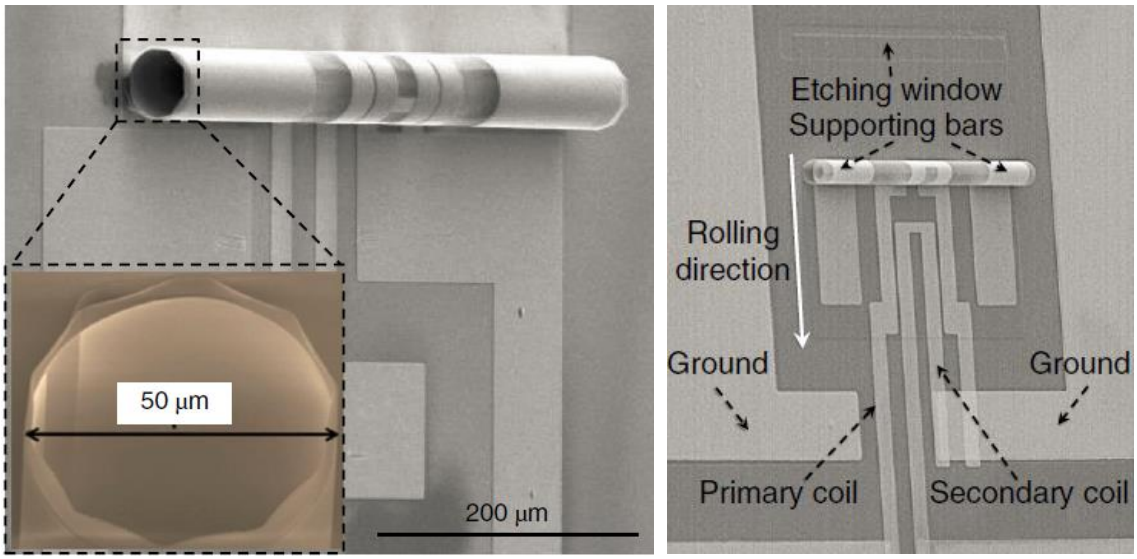

Fig. 26. Self-roll up nitride fim based on-chip transformers [80].

layers with opposite stress condition were deposited on top as a membrane followed by a patterned layer of metal where both primary and secondary coil shapes were defined. Finally, a patterned layer of Al_2O_3 was deposited on stack of these overlying layers to act

as a cover layer as well as to create a etch window for sacrificial layer etch process. Sacrificial etch performed on Ge layer resulted in a self-rolled up transformer (due to rolling of nitride films) with its secondary coil wrapped inside a primary coil hence giving better coupling results (Fig. 26).

CHAPTER 5

Process Technology for Internal Stress Induced Controllable Self-Assembly

In this chapter, a process technology to develop internal stress induced self-assembled bi-metallic thin film microstructures is elaborated. We utilize the inherent mismatch of intrinsic stress conditions between layers of a bi-metallic beam and demonstrate controllable out-of-plane bending of micro cantilever structures. To verify the bending of patterned thin films due to intrinsic stress, we first designed and modelled different bi-metallic cantilever test structures. The effects of dimensional parameters (i.e. length, width and thickness) on the amount of cantilever bending were extensively studied and bending conditions were optimized. Fabrication results of bi-metallic cantilevers showed excellent match with simulation results and bending angles of up to ~ 137° were achieved.

5.1. Internal Stress Modelling for Bi-Layer Cantilevers

To achieve a controllable bending in thin films, effects of different factors on amount of bending should be studied carefully. Hence, it is also critical to quantify the amount of bending when patterned thin-film structures are released from an underlying layer. For this purpose, optical and/or electron microscopy imaging can be used to readily quantify and compare the degree of bending in micro fabricated thin-film structures with varying geometries and/or fabricated using different deposition techniques or conditions. To evaluate bending, in this work, angular displacement was used as a measure of comparison and bending angle θ was estimated both from simulation and fabrication results. Considering a fixed-free, thin-film cantilever (Fig. 27) anchored at point a with its distal end located at position b, and assuming that intrinsic stresses exist in the thin-film cantilever structure, upon release from the substrate the cantilever tip will traverse to position c. The displacement covered by the tip of the cantilever can be used as a parameter to evaluate the amount of bending achieved; however, to normalize the

variation with respect to cantilever length, “angular displacement” was used and bending angle θ was estimated as shown in Fig. 27. This approach provided a sound and practical basis to compare transverse bending of different cantilever geometries.

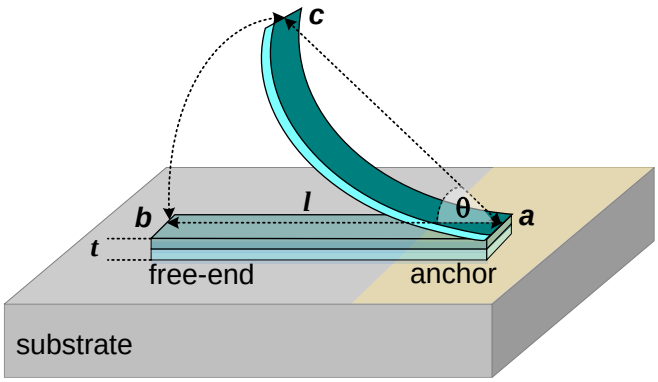

Fig. 27. Concept of bending angle (θ) based on angular displacement.

To characterize the bending angle θ with respect to geometrical specifications of patterned thin films, various sets of bi-layer cantilever structures with different dimensions were designed containing copper (Cu) and chromium (Cr) as stacked metal layers. Evaporated chromium thin films have been reported to possess large tensile stress values of around 1.3 GPa at a thickness of 100nm; whereas, copper films possess smaller tensile stress, usually less than 0.1 GPa, over a large span of thicknesses [76]. Since the actual magnitude of intrinsic stress in metallic thin-films is highly dependent on the film thickness and deposition conditions, by fixing the deposition parameters and varying the thicknesses of Cr and Cu, it is possible to control the stress gradients along the thickness of a metallic multi-layer stack to control their bending. As such, cantilevers made up of stacked layers of Cu/Cr are expected to show upward bending, while reverse stress gradients in Cr/Cu cantilevers are expected to cause downward bending.

Cantilevers assuming different lengths ranging from 90 µm to 290 µm at three different values for the total bi-layer thickness (300 nm, 500 nm and 700 nm) were designed and modelled in CoventorWare®. Thickness of the Cr layer was fixed at 100 nm, and Cu layer was varied at 200 nm, 400 nm and 600 nm; respectively. Following the construction of the model geometry, reference values for intrinsic stresses [76] were assigned between the interfaces of the cantilever structural layers. Automatic meshing was performed and finite element analysis (FEA) results revealed out-of-plane bending of cantilever structures away from the substrate with the bending angle (θ) as a function of cantilever thickness (t) and cantilever length (l). Since cantilever width (w) does not

significantly affect bending in the low width/length (*w/l*) regime of less than 1 [81], *w* was fixed at 50 µm to yield *w/l* ratios of ~ 0.5 or less, and achieve bending primarily as a function of *l* and *t*.

Analysis results display increase in bending angles with increasing cantilever length, and decrease in bending angles for increasing cantilever thickness for thicknesses of 300 nm, 500 nm and 700 nm, respectively (Fig. 28a-28c). To highlight the effect of film thickness, a 280-µm-long cantilever was simulated for various thicknesses and results indicated decreasing bending angles of 128°, 71° and 50° with increasing film thicknesses of 300 nm, 500 nm and 700 nm, respectively (Fig. 28e-28f). The complete trend of bending angles for all simulated cantilever lengths and thicknesses are plotted and compared in Fig. 29.

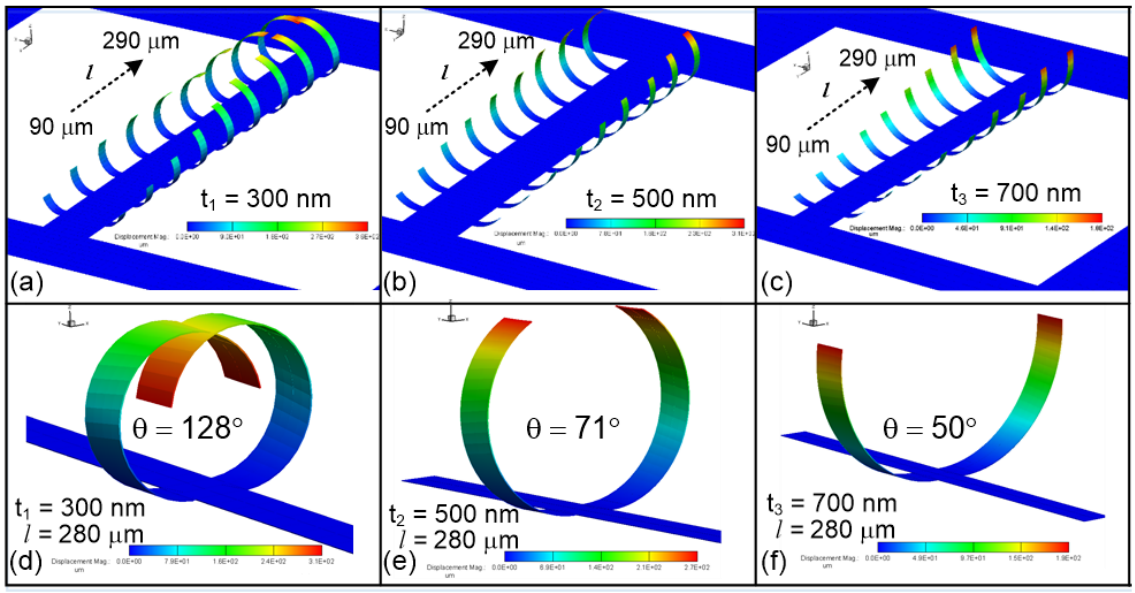

Fig. 28: FEA results indicating intrinsic stress induced bending for a set of cantilevers with lengths "*l*" varying from 90 µm to 290 µm and thickness of: (a) t_1 = 300 nm; (b) t_2 = 500 nm; and (c) t_3 = 700 nm; (d-g) zoom-in views of 280 µm-long, two-sided cantilevers for the same thicknesses t_1, t_2, t_3, respectively.

5.2. Fabrication Results

To verify the bending results obtained from mechanical modelling, identical structures were developed using standard MEMS fabrication processes. First a sacrificial layer of silicon dioxide (SiO_2) was deposited on a silicon substrate using plasma enhanced chemical vapor deposition (PECVD). The sacrificial oxide was lithographically patterned by spin-coating and exposing a layer of AZ 5214E photoresist, and wet etching the oxide

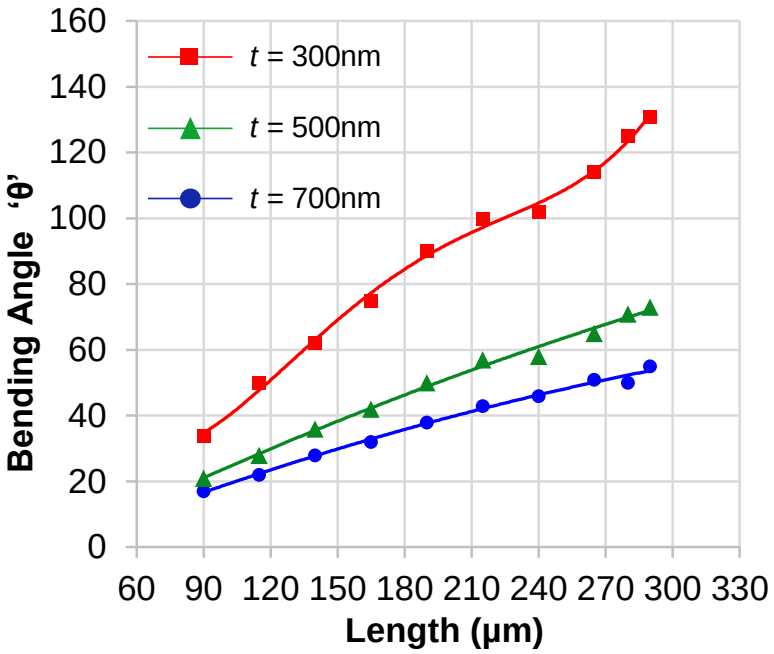

Fig. 29. Trend of simulated bending angles (θ) with respect to the length of cantilevers for varying thicknesses.

with buffered oxide etchant (BOE). As a result, contact holes in the SiO_2 layer were created, through which cantilever structural layers were anchored to silicon and mechanical connection was ensured. To realize multi-layer metallic films, chromium and copper of varying thicknesses were deposited on SiO_2 using e-beam evaporation technique. First, a thin layer (10 nm) of chromium was deposited to serve as an adhesion layer, followed by deposition of a copper layer, and finally by a top chromium layer. The stacked thin-film metallic layers were patterned by photolithography to form cantilever structures, and selectively wet-etched with commercial Cr and Cu etchants. Etching of the sacrificial oxide layer resulted in free standing cantilevers with some finite amount of intrinsic stress.

One of the major concerns during fabrication of self-assembled microcantilevers included non-uniform stress profile of thin films. Since, the deposition rate for e-beam metal evaporation is not uniform due to practical limitations of the equipment, a non-uniform thickness profile is developed in metal thin films which leads to a non-uniform stress distribution over the surface of thin film. To overcome this problem, a substrate rotation was introduced during metal deposition step to increase the uniformity of thin film thickness as well as stress profile over the thin film. Fig. 30 shows bent up released cantilevers with and without substrate rotation.

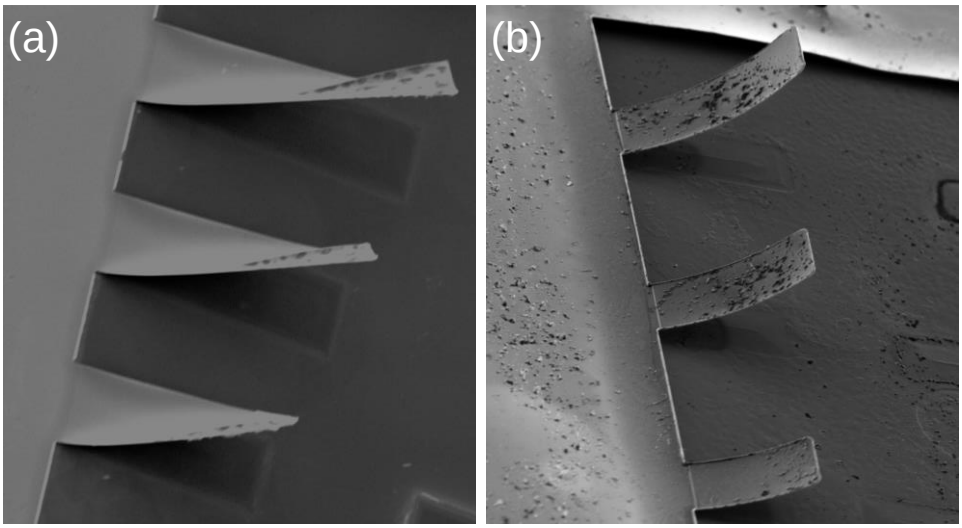

Fig. 30. Effect of substrate rotation during e-beam metal deposition on stress profile of thin film: (a) with no substrate rotation and have non-uniform stresses (b) with substrate rotation hence uniform stress is developed.

Thin-films of chromium have large intrinsic stress and act as the primary stressor layer in the bi-metallic cantilever structure. Additionally, the magnitude of stress in Cr is highly dependent on film thickness. Therefore, to ensure the same magnitude of stress in Cr layers for all fabricated designs, the thickness of Cr was kept constant at 100 nm. Instead, thickness of the Cu layer whose stress is relatively invariant of film thickness was adjusted at 3 different values (200 nm, 400 nm and 600 nm) to achieve of Cr/Cu thickness ratios (t_{CR}/t_{CU}) of 1/2, 1/4, and 1/6, respectively. This approach allowed a more controllable modulation of the total stress gradient in the multi-layer stack and provided tuning of the degree of bending in fabricated micro structures upon sacrificial layer release. Following fabrication, stress-induced bending in cantilevers was observed under a scanning electron microscope (SEM) and bending angles were experimentally quantified. SEM images of cantilevers for three fixed lengths (l) and for three film thicknesses (t) are shown in Fig. 31, which indicate upward bending where θ decreases with t, and increases with l in much similarity to modelling results. Specifically, θ rises from 34° to a maximum of 137° as l increases from 110 μm to 225 μm for t_1 of 300 nm (Fig. 31a-31c), similarly for t_2 of 500 nm θ varies from 25° to 52° (Fig. 31d-31f), and from 15° to a minimum of 38° at t_3 of 700 nm and l of 225 μm (Fig. 31g-31i).

In coherence with the modelling results, 300-nm-thick structures exhibit the highest, whereas 700-nm-thick structures show the lowest bending for all cantilever designs (Fig. 32a-32c). The comparison between simulated and experimental results shows high consistency especially at lower values of length (l), however, at larger lengths the bending

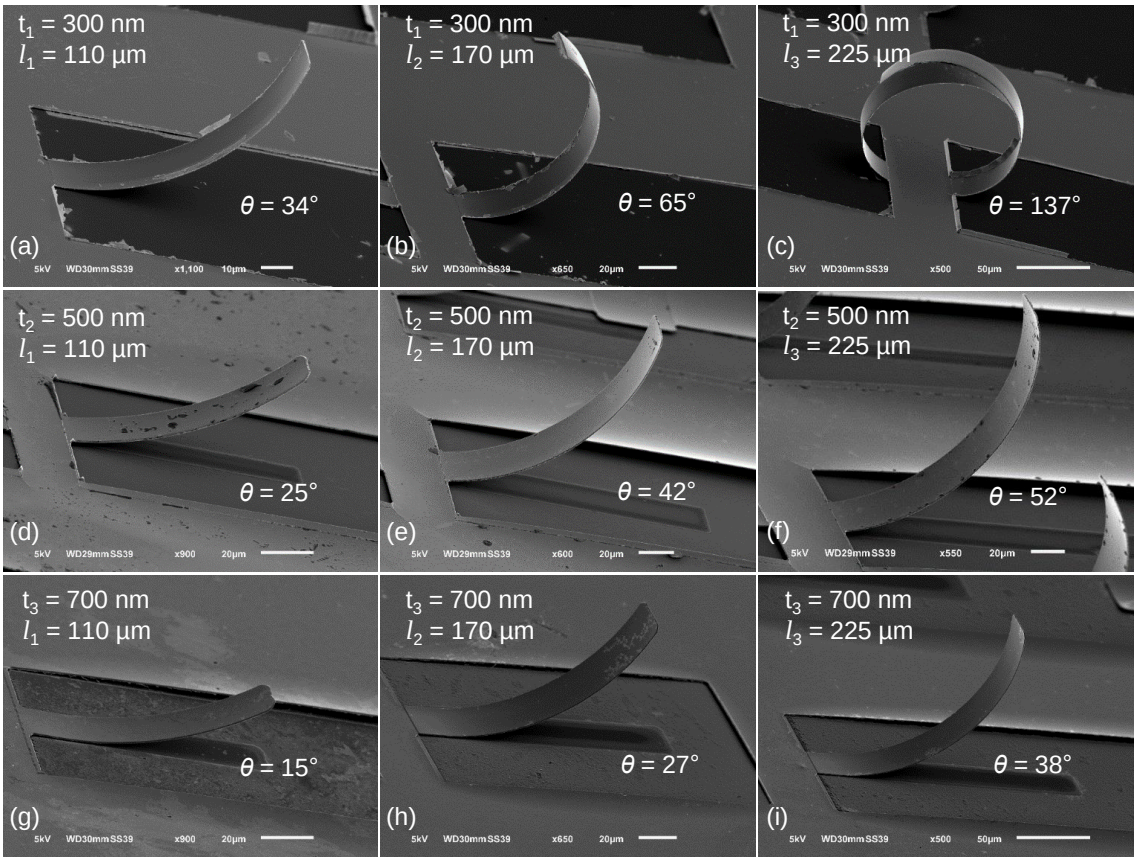

Fig. 31. Side-view SEM images of released cantilevers with corresponding bending angles (θ) for three different lengths (l_1 = 110 µm, l_2 = 170 µm, l_3= 225 µm) and thicknesses t_1 = 300 nm (a-c); t_2 = 500 nm (d-f); t_3 = 700 nm (g-i).

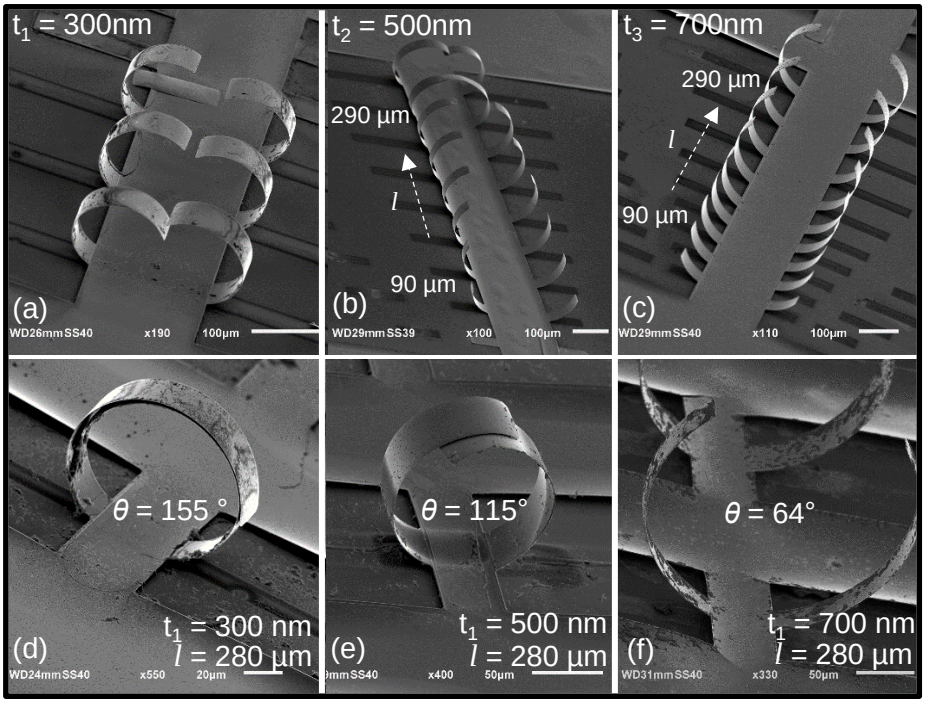

Fig. 32. (a-c) SEM images of two-sided Cu/Cr cantilever arrays consisting of varying cantilever lengths and fabricated at three different film thicknesses; (d-f) SEM images of 280 µm long cantilevers fabricated at thicknesses of 700 nm, 500 nm and 300 nm.

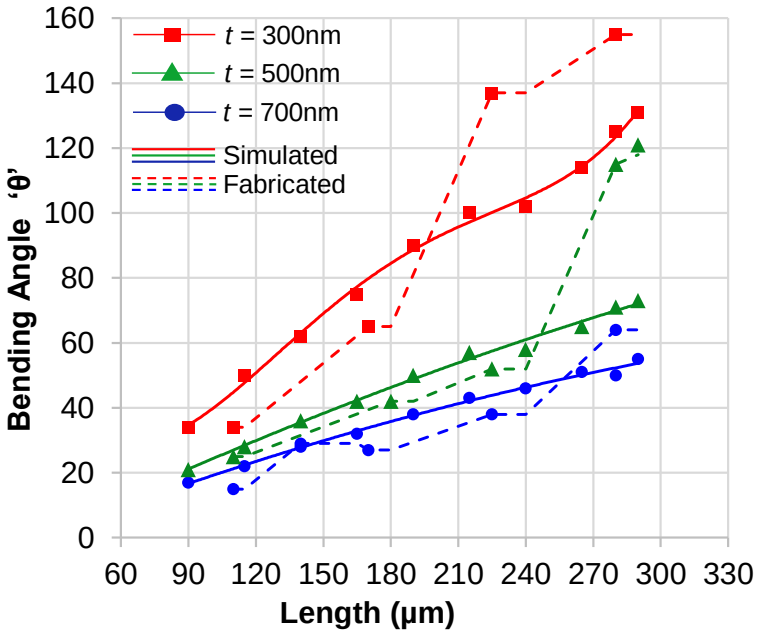

Fig. 33. Comparison of bending data obtained from simulations and fabrication results for cantilevers.

angles of fabricated structures tend to increase more rapidly than simulated bending angles. For instance, bending angles for a cantilever of length 280 μm at film thicknesses of 300 nm, 500 nm and 700 nm were observed to be 155°, 115°, and 64°, respectively (Fig. 32d-32f); whereas, modelled cantilevers with similar l of 300 μm displayed θ of 131°, 77°, and 59°, respectively. Complete bending data from both simulation and fabrication results are plotted and compared in Fig. 33.

5.3. Self-Assembled 3D Wavy Structures

As suggested by the theory, direction of cantilever bending can be adjusted by controlling the sign of the stress gradient or the loading mode. Since stress in evaporated thin-film metals is usually tensile [69]; we have chosen to control the sign of the stress gradient (i.e. considering increase of tensile stress away from the sacrificial layer-thin film interface to yield positive stress gradients ∇_σ and increasing tensile stress gradients towards the sacrificial layer to be negative ∇_σ) rather than the loading mode (tensile vs. compressive). Thus, it can be hypothesized that by modulating the stress gradient along the length of a cantilever, it can be possible to realize complex wavy structures upon post-release self-assembly which are otherwise difficult, if not impossible, to fabricate with conventional microfabrication.

To elaborate on the concept, cantilevers with sections of alternating stress conditions were designed and fabricated. A cantilever with three sections is shown in Fig. 34, where the first and last sections are comprised of Cu/Cr metal layer resulting in upward bending, whereas the middle section is made up of Cr/Cu stack and have opposite stress gradients causing this section to bend downwards. Sacrificial release of such cantilevers resulted in controllable fabrication of wavy shaped structures which also demonstrates the potential of intrinsic-stress induced self-assembly technology in 3D microfabrication.

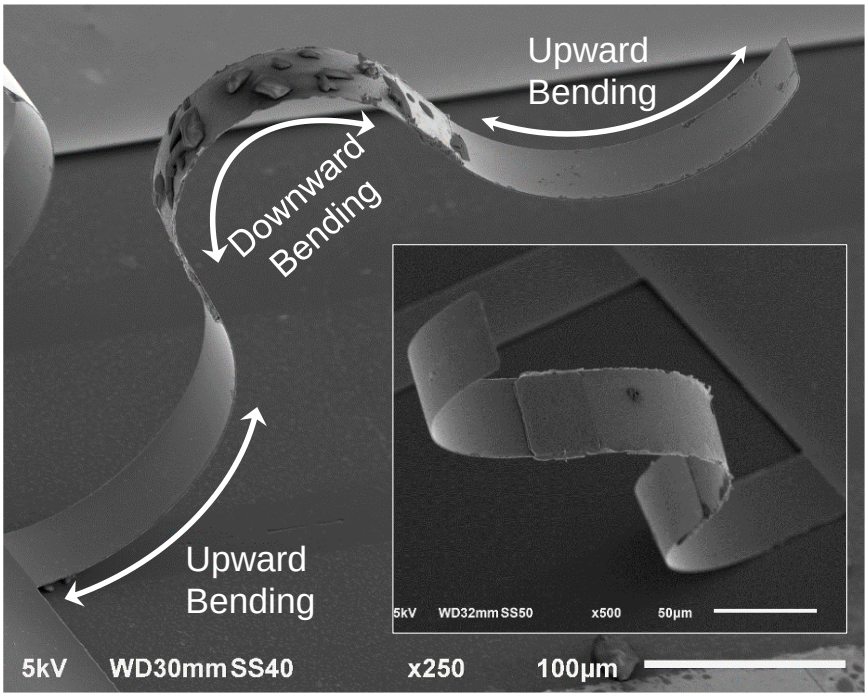

Fig. 34. SEM images of a segmented cantilever showing opposing stress gradients engineered in each segment to controllably realize upward and downward deflections and form a complex wavy-shaped structure.

CHAPTER 6

Internal Stress Induced Self-Assembly Applications to High-*Q* On-chip RF-MEMS Inductors

In this chapter, an RF-MEMS application to controllable self-assembly based on internal stress of thin films (discussed in previous sections) is explored. The concept is applied to conventional on-chip inductors to convert them into vertical inductors due to stress based bending. The performance enhancement is simulated through multi-physics tools and performance parameters before and after the bending are described and compared.

6.1. Introduction to RF-MEMS Inductors

On-chip inductors are important building blocks for many radio-frequency integrated circuits (RFICs) including voltage-controlled oscillators (VCOs), low-noise amplifiers (LNAs), matching circuits, and also needed in power conversion circuitry such as DC-DC convertors [32]. The two major performance parameters of on-chip inductors which directly affect the performance and specifications of the RF circuit are, the *Q*-factor and the self-resonance frequency (f_{SR}).

Q-factor is a measure of the inductor efficiency and describes the inductive quality of an inductor at a given frequency through the ratio of its inductive reactance to its resistance. *Q*-factor of the inductor is directly affected by substrate losses, which could be either due to magnetic losses or ohmic losses. Collectively, substrate losses lead to decreased *Q*-factor and degrade the overall performance of the inductor.

The second important parameter for an inductor is the self-resonance frequency. Due to parasitic capacitances in between the metal conductors of the inductor, and between the metal and the substrate [82], the operating frequency range of an inductor is limited. Inductive reactance of an inductor increases with the increase of operating frequency up

to a certain point referred to as the self-resonance frequency; beyond which, the inductor ceases to display inductive behavior (i.e. capacitive behavior dominates) and the inductance (L) assumes negative values.

To achieve high performance inductors, optimization of the two major figures-of-merit for inductors (*Q*-factor and f_{SR}) is critical. However, this has proven to be a very challenging task due to limitations of standard microelectronic fabrication technologies which primarily rely on planar processing. Owing to this limitation, on-chip inductors have been primarily designed in planar configurations which inevitably cause substrate losses and large parasitic capacitances, thereby lowering the *Q*-factor and f_{SR} of the inductor [83].

Several attempts have been proposed to realize high performance on-chip inductors by improving their *Q*-factor and f_{SR} using different types of techniques including design of new inductor topologies or geometries, and development of novel fabrication processes. The attempts to realize high performance on-chip inductors include fabrication of suspended inductors by removal of the underlying substrate [84], fabrication of thick-metal inductors [85], vertical inductors using plastic deformation magnetic assembly [51], out-of-plane inductors formed by leveraging the intrinsic stress in thin films [79] and surface tension [59]. Among these methods, utilization of intrinsic stress may be a promising approach to fabricate high performance on-chip inductors [57].

6.2. Design and Modelling of Inductors

Different inductor configurations including single-turn ring, 2-turn spiral and 3-turn spiral were modelled. To minimize the resistance and provide structural stability, the inductors were designed for a bi-layer film thickness of 700 nm in total. Inductor structures differing in their metal width (*w*), outer dimension (*D*) and number of turns (*n*) were designed to examine the effect of geometrical parameters (figure 4) on electrical performance. Based on our previous studies [86], inductor geometries were designed to achieve inductance values of >1 nH at frequencies of 1 GHz and above. Accordingly, for ring inductors with circular geometry, width (*w*) of the conductor, inner radius (*r*) and outer dimension (*D*) varies from 60 μm to 150 μm, 150 μm to 500 μm, and 420 μm to 1300 μm, respectively. The single-turn ring inductor is connected with the metal pads by means of straight sections with length (*l*) and typically narrower conductor width. Bending optimization results obtained in previous section provided basic guidelines to specify dimensions of the straight section. Longer length of straight section ensures

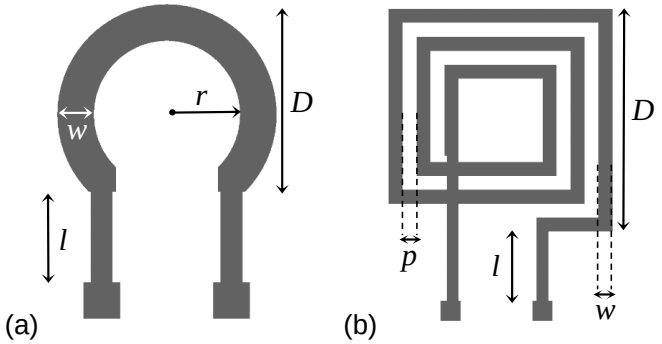

Fig. 35. (a) Geometrical design parameters of single-turn ring inductor; and (b) spiral inductor.

sufficient amount of bending but at the same time increases the overall series resistance of the inductor. Therefore, the length of straight section should be chosen carefully and presumes values of 250 μm and 350 μm for the case of ring inductors.

Similarly, for 2-turn and 3-turn spiral inductors, conductor width (*w*) changes from 80 μm to 140 μm, with pitch values (*p*, distance between two adjacent turns) in the range of 40 μm to 70 μm. The outer dimension (*D*) for 2-turn and 3-turn spirals ranges from 600 μm to 1300 μm, and 840 μm to 1560 μm, respectively. Spiral inductors are also connected to pads with the help of straight sections which have lengths (*l*) of 300 μm for 2-turn spiral, and 500 μm for 3-turn spiral (Fig. 35).

Inductor geometries based on the above parameters were then modelled to determine the level of bending and final three-dimensional device structure upon release and self-assembly. Similar to the case of cantilever bending, appropriate intrinsic stress values were assigned as boundary conditions to the corresponding metal layers. Magnitude of the displacement throughout the inductor surfaces were plotted for all designs (Fig. 36), where maximum displacement occurred typically towards the farther end of the inductor geometry causing significant upward deflections with bending angles ranging from a minimum of ~ 30° up to 80°. Fig. 36a shows a three-dimensional simulation result of a proposed ring inductor experiencing bending in upward direction due to intrinsic stresses with θ of 77°, and similarly, spiral inductors with two and three turns reach 49° and 37° bending, respectively (Fig. 36b and 36c).

6.3. Results and Discussions

On-chip inductors are defined primarily by three parameters; quality factor (*Q*), inductance (*L*) and s elf-resonance frequency (f_{SR}). To study these parameters for the

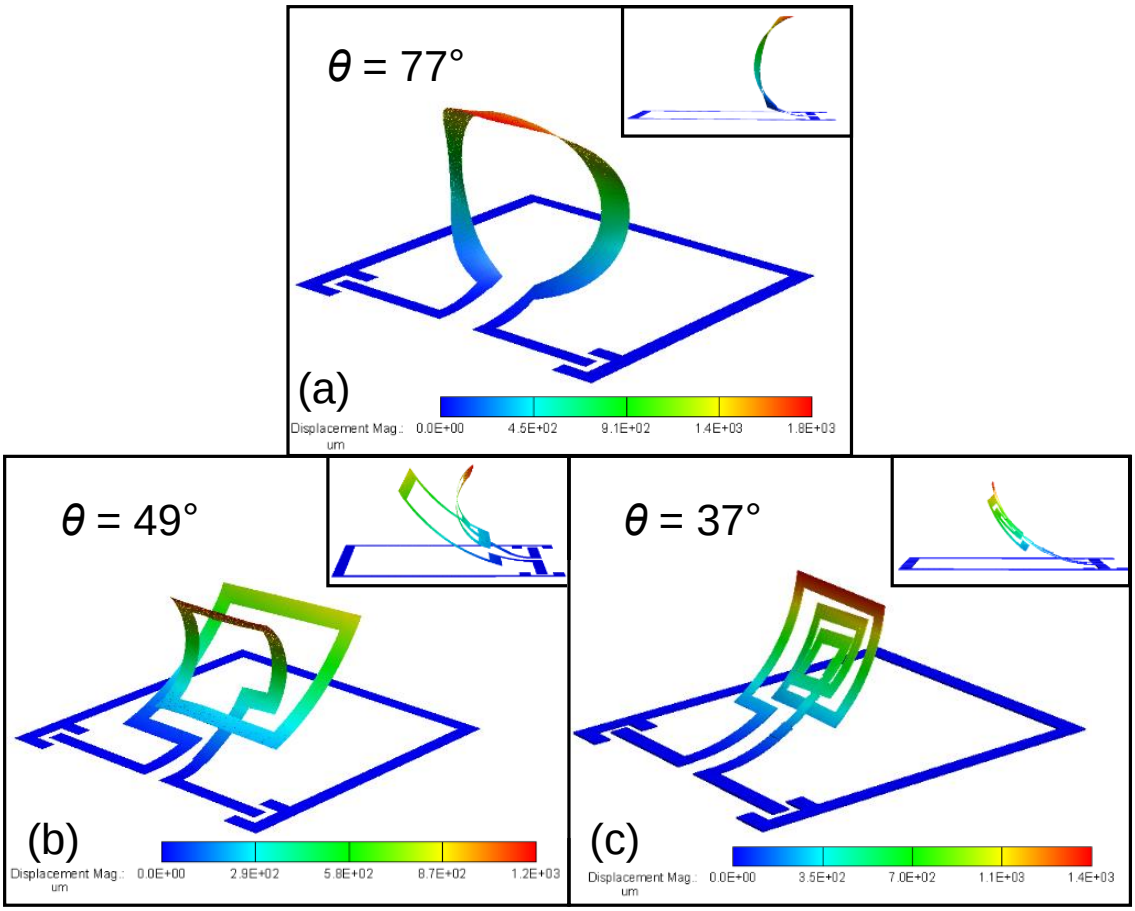

Fig. 36. Three-dimensional modelling of the intrinsic stress-induced post-release bending of: (a) single-turn ring inductor; (b) 2-turn spiral inductor; and (c) 3-turn spiral inductor, with surface plot of the displacement magnitude (μm) and corresponding bending angles (θ); insets show side view images of inductors in raised position away from the substrate surface.

proposed designs, structures before and after bending were simulated in HFSS (ANSYS, Inc., Canonsburg, PA). The relations used in simulations for *Q* and *L* are given as follows:

$$Q = \frac{\mathrm{Im}(Y_{11})^{-1}}{\mathrm{Re}(Y_{11})^{-1}} \tag{2}$$

$$L = \frac{\mathrm{Im}(Y_{11})^{-1}}{\omega} \tag{3}$$

A frequency sweep using two-port analysis was performed in HFSS for both ring and spiral inductors. Results before and after the bending were simulated and compared. Moreover, parametric study on conductor width (*w*), outer dimension (*D*) and number of turns (*n*) was performed to investigate the effects of structural parameters on the electrical response of the inductors.

Q-factors for single-turn ring inductors before and after bending for *w* ranging from 60 μm to 150 μm are shown in Fig. 37a. Since, *Q*-factor of an inductor is the ratio of its inductive reactance to its series resistance, larger conductor cross section hence larger *w* is expected to reduce the series resistance and improve the *Q*-factor. Accordingly, the *Q*-factor for single-turn ring structure improves from 8 to 10.2 as the width increases from 60 μm to 150 μm. The same inductors after bending away from the substrate display *Q*-factors in the range of 18.2 to 21.1, which indicates more than 100% increase in *Q* with intrinsic-stress induced self-assembly. Similar *Q*-factor improvements for spiral inductors are also observed as the structures go through post-release bending where the *Q*-factor increases from 5 to 10.4 for a 2-turn spiral with w of 80 μm (Fig. 37b) and from 3.7 to 5.8 for a 3-turn spiral. However, contrary to ring inductors, the spiral topology shows inverse relation of *Q*-factor with w. The *Q*-factor for 2-turn spiral decreased from 10.4 to 7.9 as the width increased from 80 μm to 140 μm. Additionally, analogous to 2-turn spiral, *Q*-factor for 3-turn spiral also decreased from a value of 5.8 to 4.2 as the width changed from 80 μm to 140 μm.

Although, increasing metal width decreases the series resistance, at the same time the magnetic leakage between metal layer and substrate (with finite resistivity) also increases due to larger overlap area. This effect remains insignificant for the case of ring inductors but becomes dominant for spiral inductors because of their higher turn density. Furthermore, in general, spiral structures show lower *Q*-factor than that of ring structure due to the reason that series resistance in spiral is relatively larger as compared to that of ring inductor (due to longer metallic path), which increases the ohmic losses hence decreasing the overall *Q*-factor.

Using the Y-parameters obtained by a frequency sweep analysis, inductance variations for both ring and spiral structures, before and after bending were obtained. Inductance values before and after bending are similar over a large frequency range; while a positive shift in self-resonance frequencies was observed. This increase in f_{SR} is due to the reduced substrate coupling in vertical structures because of large separation between the metal layers and the substrate. Upon bending, f_{SR} value as high as 24 GHz was achieved for a ring inductor with outer dimension of 500 μm (Fig. 38a).

On the other hand, geometrical parameters, primarily the number of turns (*n*) and outer dimension (*D*), play a fundamental role in defining the inductance value. First, to explore the effect of n, a comparative study between inductance values of vertically bent-up single-turn ring, 2-turn spiral and 3-turn spiral inductor was performed. Inductors with

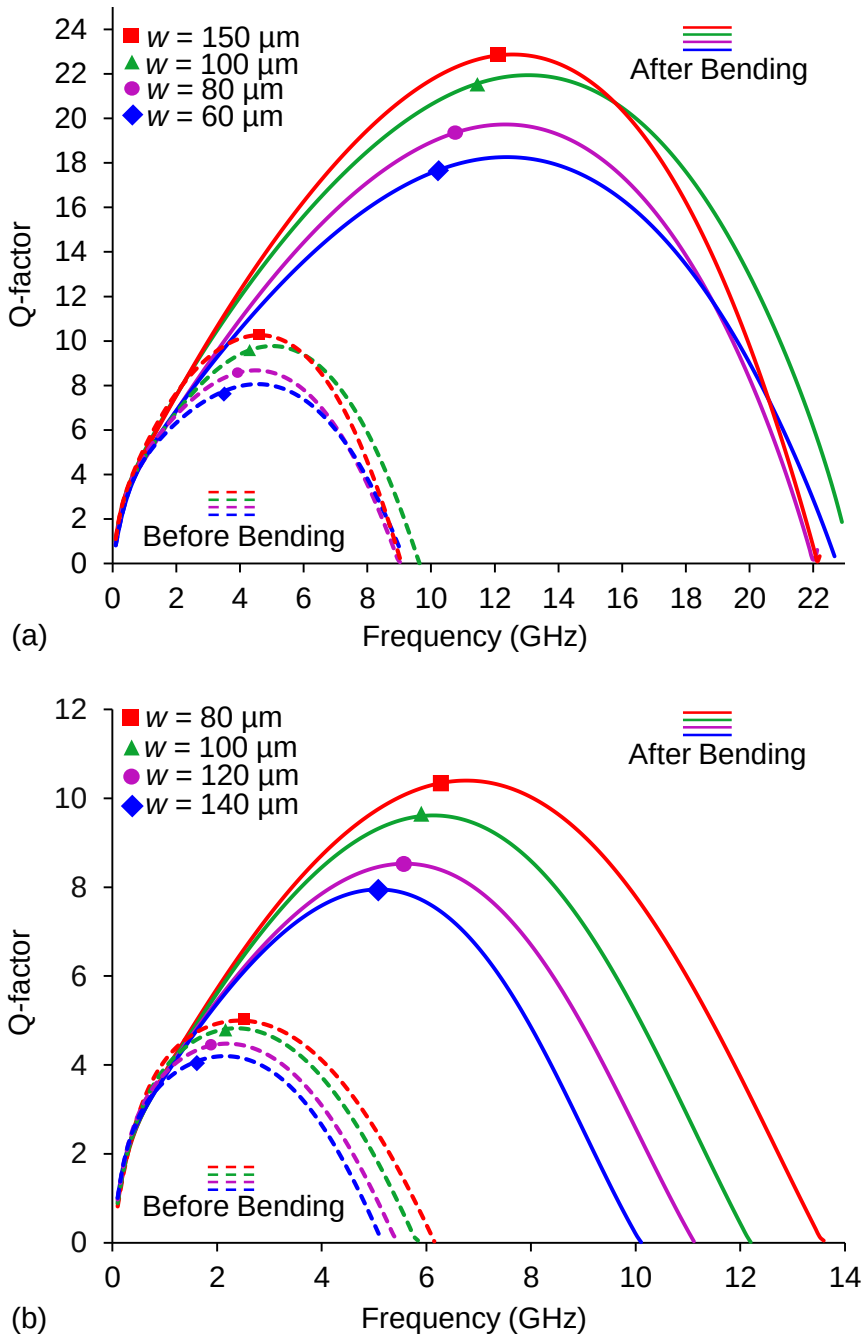

Fig. 37. *Q*-factor variation with frequency for inductor designs with varying conductor widths (w) prior to and post-release bending; plots represent: (a) ring inductors; and (b) 2-turn spiral inductors.

the same outer dimension of 1000 µm were considered and results revealed increase in inductance with increasing number of turns (n). At 1 GHz, a single-turn ring inductor displayed an inductance of 3.49 nH, whereas, 2-turn and 3-turn spiral inductors with the same *D* achieved larger inductance values of 5.13 nH and 6.95 nH, respectively (Fig. 38a inset).

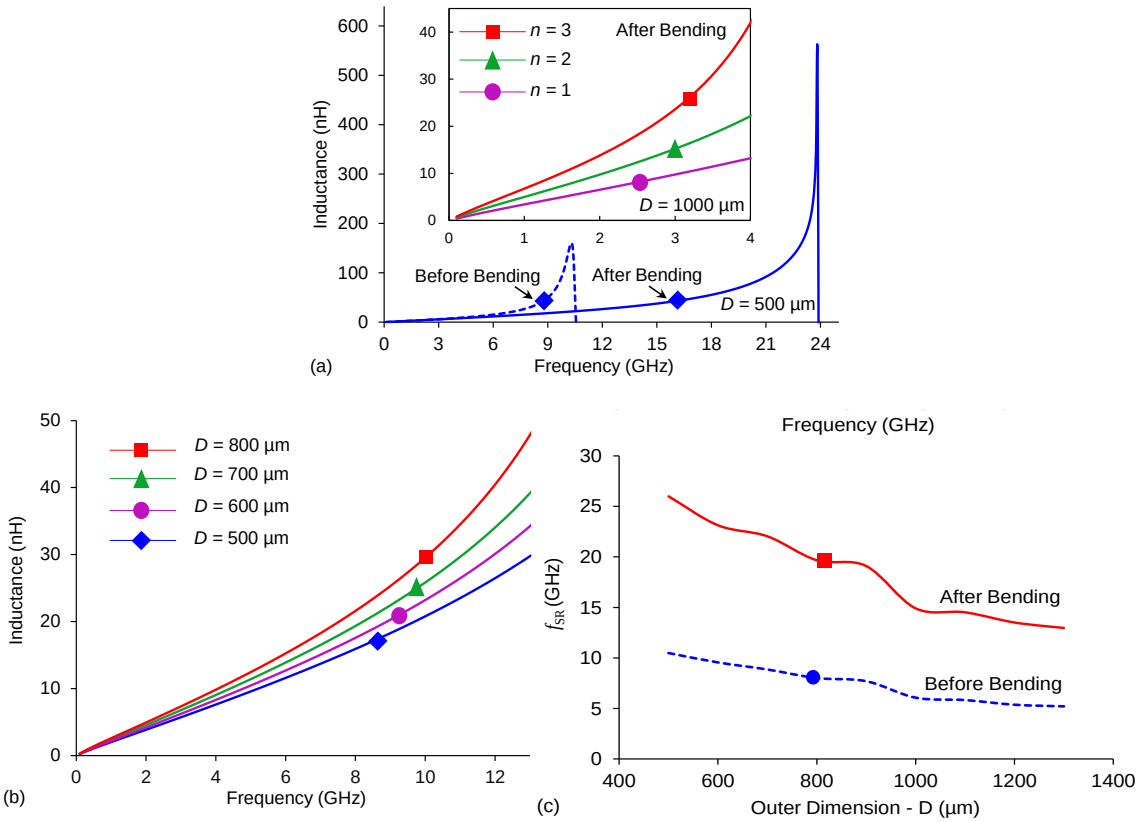

Fig. 38. Plots summarizing the relationships between self-resonance frequency (f_{SR}), inductance (L), and geometrical parameters (n, D) for inductors before and after bending: (a) inductance with respect to frequency for a ring inductor with outer dimension (D) of 500 µm showing f_{SR} up to 24 GHz, inset shows the variation of L with number of turns (n) for vertically bent-up inductors with D of 1000 µm; (b) comparison of L values for vertically bent-up ring inductors with varying D; (c) trend of f_{SR} with D for ring inductors.

Likewise, the effect of D on inductance of vertically bent-up inductors was studied. While the change is smaller at low frequencies, for higher frequencies larger inductance variation is observed with enlargement of the outer dimension (D) of inductors, while the number of turns (n) and conductor width (w) are kept constant. The trend of inductance variation with changing of the outer dimension from 500 µm to 800 µm for single-turn ring inductors show that, at 1 GHz ~ 0.2x fold-change in L is observed and goes up to ~ 0.5x at 10 GHz, which is still well within the range of operational frequencies due to extended f_{SR} of vertically bent-up inductors (Fig. 38b).

Meanwhile, self-resonance frequency of an inductor also depends on its overlap area with the substrate which induces parasitic capacitance and degrades the inductive effect of the inductor, hence causing it to resonate. To explore this concept, trend of f_{SR} with outer dimension (D) of planar and vertically bent-up inductors were studied (Fig. 38c). Results indicate increase in f_{SR} values upon bending, while a decreasing trend from 24 GHz to 12.9 GHz is observed with the increase in inductor's outer dimension (from 500

Table. 1. Comparison of performance metrics for different inductor topologies before and after the bending

Inductor topology	Bending angle 'θ' (degrees)	Outer dimension 'D' (μm)	Metal width 'w' (μm)	Number of turns 'n'	Q-factor before bending	Q-factor after bending	f_{SR} (GHz) before bending	f_{SR} (GHz) after bending	Frequency of max. Q 'f_{max}'	Inductance @ 1 GHz (nH)
Ring	39	500	100	1	10.5	25.8	10.5	24	14.37	2.06
Ring	42	600	100	1	9.7	21.9	9.6	23.1	13.05	2.25
Ring	43	620	60	1	8	18.2	9.1	22.7	12.3	2.57
Ring	51	660	80	1	8.6	19.7	8.9	21.9	12.4	2.54
Ring	67	700	100	1	9.4	20.2	8.8	22.1	12.3	2.46
Ring	71	640	120	1	8.3	20.5	8	18.5	11	2.60
Ring	77	800	150	1	10.2	21.1	8.3	20.5	11.4	2.44
Ring	84	1000	100	1	6.5	14.9	6.1	14.9	8.6	3.40
Ring	88	1300	150	1	6.6	14.1	5.2	12.9	7.1	3.74
Spiral	31	600	80	2	5	10.4	6.1	13.6	6.7	3.61
Spiral	35	700	100	2	4.8	9.6	5.8	12.1	6.1	3.72
Spiral	41	800	120	2	4.5	8.5	5.4	11.1	5.6	3.82
Spiral	49	900	140	2	4.2	7.9	5.1	10.1	4.9	3.86
Spiral	51	1000	120	2	4.1	7.1	3.9	7.7	3.9	5.13
Spiral	37	840	80	3	3.7	5.8	3.3	6.7	3.4	7.57
Spiral	44	1000	100	3	3.5	5.5	3	5.5	2.6	7.86
Spiral	50	1160	120	3	3.3	5.1	2.7	4.4	2.1	8.52
Spiral	59	1320	140	3	3.1	4.2	2.5	3.4	1.7	9.04

μm to 1300 μm) or effective area. Likewise, due to more number of turns, which directly increases substrate coupling (as a result of larger overlap area between metal layer and substrate), spiral geometry showed resonance at relatively lower frequencies than that of ring structures.

The various inductor topologies along with their geometrical parameters (*D*, *w*, *n*) are summarized and compared in table I, to reflect the critical performance metrics including *Q*-factor and self-resonance frequency before and after bending; as well as, the frequency (fmax) at which maximum *Q* is achieved and inductance (*L*) values at 1 GHz.

CHAPTER 7

Conclusion

Intrinsic-stress induced post-release bending of thin films is demonstrated as a technology to realize controllable self-assembly of patterned thin films and as an application the concept is applied to conventional planar inductors converting them into vertical configuration and gaining higher performance. Post-release bending of multi-layer metallic cantilevers was modelled based on residual stress values from the literature, to elucidate cantilever deflection with respect to geometrical design parameters and film thickness. Models of transverse deflection and resulting bending angles were verified against fabrication results which showed very good agreement. Intrinsic-stress induced self-assembly technology was then applied to the design of out-of-plane, three-dimensional inductors which transformed from planar ring and spiral geometries upon release, to achieve a maximum *Q*-factor of more than 25 and high self-resonance frequency of up to 24 GHz. Improvements in *Q*-factor and f_{SR} validate the potential of intrinsic stress-induced self-assembly technology towards the realization of high performance on-chip inductors; as well as, various 3D geometries comprised of curved and wavy structures which are difficult to implement with conventional microfabrication.

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