ON-CHIP ANTENNAS AND PCB PACKAGED PHASED-ARRAY RADAR RECEIVER FRONT-END AT MM-WAVE FREQUENCIES

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ABSTRACT

ON-CHIP ANTENNAS AND PCB PACKAGED PHASED-ARRAY RADAR RECEIVER FRONT-END AT MM-WAVE FREQUENCIES

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Keywords: On-chip antenna, ACP probe, 77 GHz automotive radar, W-band measurement.

In this dissertation, on-chip antennas for integration in a single RFIC radar chip and alternative wire-bonded PCB/chip package for 77 GHz automotive radar front-end are studied and manufactured.

To meet the purpose of dissertation, design and implementation of flat, L-shaped and T-shaped W-band on-chip strip dipole antennas integrated with a LC balun circuit are presented. The on-chip antennas and the balun circuit are realized by using IHP's 0.25 μm SiGe BiCMOS technology with a localized back-side etch (LBE) module to decrease substrate loss.

It has been observed that measurements are highly influenced by the antenna placements and the ACP110-A-GSG-100 probe. Thus, a software calibration is performed similar to a network analyzer calibration to model the effect of ACP probe, and then the antenna reflection coefficient is calculated using the modeled probe-fed antenna.

Finally, a low cost 77 GHz 4-element phased-array radar receiver front-end module is designed and manufactured using PCB patch antennas to get rid of on-chip antennas surface wave and achieve better array gain. The receiver package is implemented by integrating active phase shifter chips on a single layer Rogers 3003 PCB board using ball-to-wedge bonding with insertion loss less than 7.5 dB at 77 GHz; this loss is compensated by the gain of chips' LNA.

A novel method which exploits Klopfenstein tapering is used to connect coplanar waveguide to microstrip line at W-band frequency for chip to PCB board transition. The measured gains of the phased-array receiver and passive 4-element antenna array are compared. The receiver and passive array achieve the maximum gains of 9.7 dBi and 10.4 dBi at 77 GHz. The beam can be steered to ±30°.

ÖZET

MİLİMETRE-DALGA UYGULAMALARI İÇİN YONGA-ÜSTÜ ANTENLER VE PCB PAKETLİ FAZ-DİZİNLİ RADAR ALICI ÖN-UCU

MIRMEHDI SEYYEDESFAHLAN
Doktora Tezi, Aralık 2015
Danışman: Prof. Dr. Ibrahim Tekin

Anahtar Kelimeler: Yonga-üstü anten, ACP prob, 77 GHz otomotiv radar, W-bant ölçüm.

Bu tezde, yonga-üstü antenlerin tek bir RFIC radar yongasına ve alternatif olarak tel-bağlı 77 GHz otomotiv radar PCB/yonga paketi ön ucuna bütünleştirilmesi çalışılmış ve üretilmiştir.

Tezin amacını karşılamak için, düz, L- ve T-tipi, LC balun devresine bütünleşik W-bant yonga-üstü şerit dipol antenlerin tasarımı ve uygulaması sunulmuştur. Yonga-üstü antenler ve balun devreleri, alt tabaka kaybını azaltmak için LBE modülü yardımıyla, IHP'nin 0.25 μm SiGe BiCMOS teknolojisi kullanılarak gerçekleştirilmiştir.

Antenlerin yerleştirilmesi ve ACP110-A-GSG-100 sonda ile ölçümlerin dikkate değer bir ölçüde etkilendiği gözlenmiştir. Bu nedenle, ACP probun etkisini modellemek için ağ çözümleyici kalibrasyonuna benzer bir yazılım kalibrasyonu yapılmış ve ardından modellenen bu prob-beslemeli antenlerin, anten yansıma katsayısı hesaplanmıştır.

Son olarak, yonga-üstü antenlerin yüzey dalgalarından kurtulmak ve daha iyi dizi kazancına erişmek için PCB yama antenleri kullanılarak düşük maliyetli 77 GHz 4-elemanlı faz-dizinli radar alıcı ön-ucu modülü tasarlanmış ve üretilmiştir. Alıcı paketi, aktif faz kaydırıcı yongalarının tek katmanlı Rogers 3003 PCB paneline 77 GHz'te 7.5 dB'den daha az iletim kayıplı tel bağlaması kullanılarak bütünleştirilmesi ile gerçekleştirilmiştir; bu kayıplar LNA yongalarının kazancı ile telafi edilmiştir.

Klopfenstein empedans uyarlamasından yararlanan özgün bir yöntem, yongadan PCB panele geçiş için eş düzlemli dalga kılavuzundan W-bant frekansında mikroşerit hatlara bağlamakta kullanılmıştır. Faz-dizinli alıcı ve pasif 4-elemanlı anten dizilerinin ölçülen kazançları karşılaştırılmıştır. Alıcı ve pasif dizi, 77 GHz'te 9.7 dBi ve 10.4 dBi maksimum kazançlara erişmiştir. Anten ışını ±30° döndürülebilir.

To my beloved wife (Elham) and son (Daniel) for their support

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I enjoyed during my Ph.D. and wish all the best for everybody in their careers.

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LIST OF SYMBOLS AND ABBREVIATIONS

Symbol	Description	Unit
G	Gain	dBi
λ	Wavelength	m
P_r	Received Power	dBm
P_t	Transmitted Power	dBm
kT	Noise power in 1 Hz bandwidth	dBm/Hz

Abbreviation	Description
LRR	Long range radar
SRR	Short range radar
MIM capacitor	Metal insulator metal capacitor
CPW	Coplanar Waveguide
GSG pads	Ground-Signal-Ground pads
ACP	Air Coplanar Probe
TL	Transmission Line
MTL	Microstrip Transmission Line
APS	Active phase shifter
CPW-to-MTL	Coplanar Waveguide to Microstrip Transmission Line transition

CHAPTER 1

INTRODUCTION

1.1 Millimeter Waves Applications and Practical Devices

Investigation on CMOS and chip technology has led to many developments as well as miniaturization of electronic circuits. Demand for integration of different passive and active components inside silicon chips are further increased at mm-wave frequencies [1-8]. Applications of the mm-wave at 60 GHz for wireless communication [9-15], 77 GHz automotive radar [16] and imaging at 94 GHz [17-18] and 140 GHz [19-20] have been increased in recent decades. Radar sensors operating at 77 and 94 GHz can also be used in Helicopters for collision avoidance with an obstacle in difficult weather condition; since it can penetrate through fog and heavy dust and has high resolution [21]. Various practical usage of the mm-wave frequency for communication between game modules, civilian and military applications are shown in Figure 1.1.

The automotive mm-wave radar operating at 77GHz is one of the achievements in CMOS technology, which has been receiving a lot of attention in the last decade; and circuit designers put a lot of energy to bring all components of the system into a single chip to enhance efficiency, performance and specifically decrease the size and cost of the on chip radars [22]. Automotive cruise control systems and especially 77 GHz automotive radar is coming up with new features every day [23-25]. Open literature presents improved low noise amplifiers, phase shifters and also methods which results in better antenna performance, gain and directivity [26-33]. With development of the chip integration technology, radar transceiver modules are being integrated inside a single chip [23-25]. However, when multiple antennas or all components of radar are integrated inside a single chip, the occupied chip size is increased due to large antenna sizes. Each designer proposes new methods to reduce either chip size or cost of his structure. Most of the times, each component is designed individually (lower chip area) and then connected to each other [34] to examine the performance of the targeted system. The other technique is to place some of the components of the radar receiver to the RFIC chip and rest of the components/transitions to the printed

circuit board (PCB) and then use packaging techniques to combine these components which offer superior cost performance compared to RFIC chip only solutions. Thus, radar designers attempt to improve the system-in-package performance by increasing the efficiency of antenna, phase shifter/receiver chip as well as RF transitions that are employed for interfacing between the chip and PCB. Connecting the patterned PCB circuitry to the chips with minimum insertion loss for exploiting probe-measured performance of chip, is demanding innovations and improvements in both the circuits on the board and the connecting techniques.

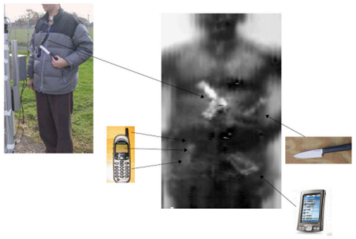
Connecting different modules at lower frequencies may be easier, but as the frequency is increased, the connections are going to be more sensitive and in some cases impossible; at higher frequencies the size and accuracy of the connections have significant effects on transmitted/received signals. Development of technology has been creating different methods of packaging such as embedding the chip in Si substrate [35], embedded wafer level ball grid array (eWLB) package [36-38], flip-chip [39-40] and wire bonding chip to PCB [37], [41-45].

60 GHz WiGig Wireless Gigabit – 802.11ad

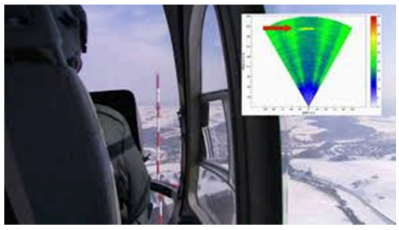
http://www.extremetech.com/computing/191872-samsung-develops-60ghz-wifi-capable-of-4-6gbps-will-be-in-devices-next-year

77 GHz Automotive Radar

http://www.bosch-presse.de/presseforum/details.htm?txtID=7031&locale=en



94 GHz Imaging Radar [17]



77 GHz Radar for Aerospace Applications

http://www.astyx.net/en/radar-assistence-systems/aerospace.html

140 GHz MIMO Baggage Control Radar

https://www.ihp-microelectronics.com/en/research/technology-platform-for-wireless-and-broadband/projects/nanotec.html

95 GHz Active Denial System

https://en.wikipedia.org/wiki/Active_Denial_System

Figure 1.1: Practical applications of the mm-waves radars.

1.2 Automotive Radar Link and Radar Range

Developing the radar technology in the vehicles, The European Telecommunications Standards Institute (ETSI), specified the frequencies 24 GHz and 77 GHz for operating the automotive radar. In the standards of ETSI, 77 GHz is used for automatic cruise control "long range radar", while the anti-collision "short range radar" are operating at 24 GHz and 79 GHz frequencies [46]. Although radars at 24 GHz were marketed for a short term, however, this frequency was temporary due to other radio services in this band and suffering from interference with these services. The 76-77 GHz band is used for long range radar (LRR) and 77 GHz to 81 GHz is allocated for short rang radar (SRR) that has wider bandwidth and higher resolution [47]. Various applications of the LRR and SRR automotive radar are shown in Figure 1.2.

As it shown in Figure 1.2, in addition to the scan the beam and monitor around the vehicle, the range of the radar is also important factor in the design of radar. The Bosch recent third-generation long range radar (LLR3), developed from Infineon chip, can register the ranges up to 250 meters [48]. To improve the maximum range of radar, one can consider to increase gains of both the transmitter and receiver antennas.

The received signal power P_r from the radar that has transmitted the signal with power P_t, is obtained as below [49].

$$P_r = \frac{P_t G}{4\pi R^2} \sigma \frac{1}{4\pi R^2} A_{eff} \tag{1.1}$$

where G is the transmitting antenna gain, R, distance between the target and radar, σ, radar cross section of target and A_{eff} is the effective aperture of the radar receiving antenna. If the

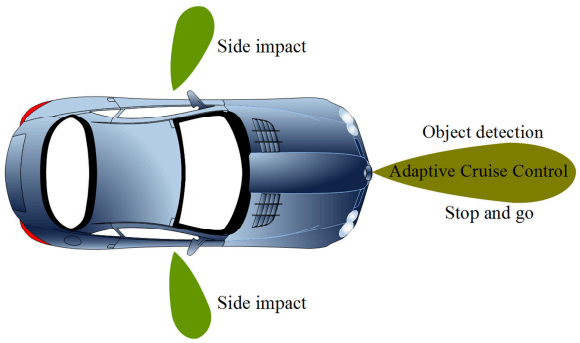


Figure 1.2: Automotive radar applications.

transmitted and received gains of the radar are equal, then received power and radar distance range for specified signal-to-noise ratio (SNR) are obtained as (1.2) and (1.3), respectively.

$$P_r = \frac{P_t G}{4\pi R^2}\sigma\frac{1}{4\pi R^2}\frac{\lambda^2}{4\pi}G = \frac{P_t G^2\lambda^2}{(4\pi)^3 R^4}\sigma \tag{1.2}$$

$$R = \left(\frac{P_t G^2\lambda^2}{(4\pi)^3 N_i\, SNR}\sigma\right)^{1/4} \tag{1.3}$$

where N_i is the input noise and is calculated using kTB (kT_0 = -174 dBm/Hz and B is the radar receiver bandwidth). The radar distance is proportional with the square root of the radar gain. Since the gain of 4-element array is four times of single antenna radar, hence the radar maximum range for a required SNR for two systems with single and 4-element antenna array can be increased by two times. Therefore, using the n-element phased array not only exploits the user to scan the beam, but also increases the radar maximum range.

1.3 Objectives and Major Challenges of This Dissertation

The aim of this dissertation is to make a single integrated chip for 77 GHz automotive radar receiver front-end. The single chip contains antennas, active phase shifter circuits and power dividers/combiners. As a cost effective alternative, it is also aimed to integrate active phase shifter chips on a PCB board that contains antennas and power combining circuits using wire bond technology.

To meet the goal of the dissertation in the field of on-chip W-band strip dipole antennas and automotive radar receiver front-end, integration of the active phase shifts with the PCB package are performed. The different shapes of the on-chip dipole antennas are designed and manufactured. The significant effect of air coplanar probe (ACP) tips on the antenna near field which is used to measure the antennas is demonstrated in both simulation and measurement. The probe de-embedding relation is deduced and used. Furthermore, a 77 GHz patch antenna and transition from coplanar to microstrip transmission lines are designed and manufactured on the PCB board to be integrated with active phase shifter chip and operate as the 77 GHz automotive radar receiver front end. The PCB antenna and phase shifter chip

integration is implemented to avoid the problems that arise during the on-chip antennas usage. The on-chip antennas can have advantages and disadvantages.

The significant effect of the antenna in radar persuades the designer to take more time on the design of the antennas with better gain and directivity. Increasing chip technology and integrating the antennas along with other components inside the chip, size and accordingly the cost of the chip is also employed in the design process.

As the frequency is increased, the size of the antenna becomes comparable to the chip size (less than 1 mm @ W band and on Si substrate) and this creates the opportunity for a highly integrated, single-chip transceiver to be integrated with the antenna or antenna arrays. Also, IHP realize the opportunity to reduce silicon substrate loss by IHP's integrated LBE technology; which offers silicon substrate etch from backside of the substrate, therefore much higher antenna gains and directivity can be obtained. Integrating all components of the system into a single chip will cause to enhance efficiency, performance and specifically decrease the size and cost of the on chip radars. However, when an array of antenna is used, the size of chip is increased to keep the required spacing between the antennas and reduce the coupling between them. The other problem of on-chip antenna is the thick Si substrate with high dielectric constant under the antenna. When the chip is placed on ground plane greater than chip size, the substrate modes are excited and propagated at W band. These surface waves distort the on-chip antenna radiation pattern and side lobes with higher levels are emerged. Thus, the problem is being more complicated as the on-chip antennas are handled in array applications. Therefore, to get away from these problems, the antenna or antennas array can be fabricated on PCB board and integrated with the active phase shifter chips to exploit the beam steering. Consequently, the 77 GHz 4-element phased-array beam steering radar received front end is packaged and the device power gain is measured by controlling the bias voltages of the active phase shifter chips.

This dissertation is organized as follows: in Chapter II, detailed analysis about the balun structure, straight, L-shaped and T-shaped dipole antennas on the chip will be presented. The effect of different parameters on the design of the antennas are simulated and displayed. In Chapter III, the effects of GSG pads in antenna near field and large ground plane on antenna radiation pattern distortion are demonstrated. The influence of the ACP in the measurements

is investigated by modeling and simulating the probe tips. The manufactured on-chip antennas measurements and probe de-embedded post measurement simulations are compared. In Chapter IV, the simulation and measurements of the components that are fabricated the RO3003 board are presented. The components include single, 4-element patch antenna array and coplanar waveguide to microstrip transmission line that are used to integrate with active phase shifter chip for operating a 77 GHz radar receiver front end. Moreover, the insertion loss of the wire-bond for different cases is modeled in simulation. In Chapter V, the procedure for integrating the active phase shifter chip on the PCB will be detailed, 2-element and 4-element beam-steering phased-array are presented. Finally, the dissertation will be concluded with Chapter VI.

CHAPTER 2

ON-CHIP DIPOLE ANTENNAS

2.1 Roadmap to The Chapter

In this chapter, the on-chip microstrip dipole antennas which will be fabricated on Si substrate are introduced. Three straight, L-shaped and T-shaped dipole antennas are designed at 77 GHz and 94 GHz frequencies. The unbalanced microstrip transmission line is connected to balanced dipole antenna using the LC balun circuit. The on-chip balun design process is presented in detail. Different parameters such as antenna arms lengths, widths, Si substrate beneath the antenna and balun capacitor effects on antenna performance are investigated in simulations.

2.2 Designed On-Chip Antennas Different Layers

IHP's 0.25 μm SiGe BiCMOS technology by Localized Backside Etch (LBE) module is used to realize the on-chip microstrip dipole antennas. In this process, the antennas are designed on Si substrate with dielectric constant ε_r = 11.9 and conductivity of σ = 2 S/m. The microstrip transmission line (MTL), balun circuit and antenna are designed on metal layers, called Metal 1 and Metal 2. As shown in Figure 2.1, the metal layers are placed inside the thin (11.4 μm) film of SiO_2 (with permittivity of ε_r = 4.1) on the Si substrate. The thicknesses of Metal 1 and 2 are 1 μm and 3 μm, respectively. The Si substrate thickness for antennas operating at 77 GHz is 670 μm, and for the designed antennas at 94 GHz is considered as 450 μm. To decrease the substrate loss and increase the directivity of the antenna, the Si beneath the antenna is etched using the IHP's LBE module.

2.3 Balun Definition

Generally, the dipole antenna arms are fed using a voltage source that its terminal has 180° phase difference. In order to connect a strip dipole antenna's arm to an unbalanced microstrip transmission line (MTL), a balun circuit is required to divide the input signal of MTL to the antenna arms with equal amplitudes and 180° degree phase difference [50-51]

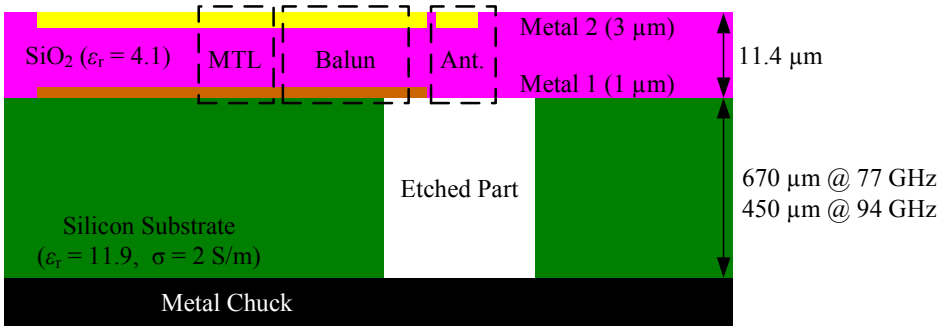


Figure 2.1: Cross sectional view of the designed on-chip dipole antennas

between them. The LC balun type is employed in the designed on-chip dipole antennas in this work. The advantage of the LC balun circuit at mm-wave frequencies is that it occupies a much smaller chip area than the λ/4 long transmission line based approaches. In on-chip LC balun circuits, the metal-insulator-metal (MIM) technology can be used to implement the capacitors. Moreover, the distributed inductors are implemented by thin MTL if their lengths do not exceed 300 μm long at W-band frequency.

2.3.1 LC Balun Circuit

The lattice of lumped component LC balun circuit with input port of P_{in} and output ports of P_{out1} and P_{out2} is shown in Figure 2.2. This balun will divide the input signal P_{in} equally between two output ports, P_{out1} and P_{out2} (opposite sign magnitude voltages). The balun provides 180° phase difference between the signals of P_{out1} and P_{out2} to convert input signal into two balanced signals [50]. The operating frequency of the shown balun circuit (f) is specified by (2.1).

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{2.1}$$

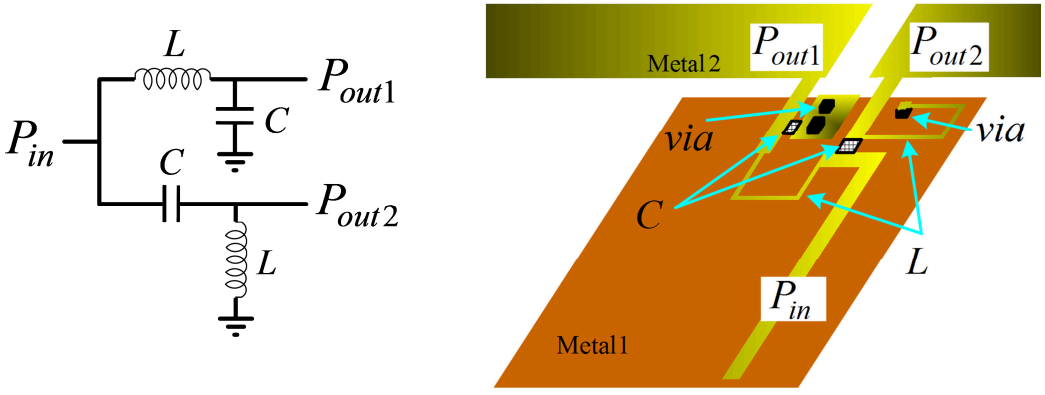


Figure 2.2: Lumped component LC balun circuit and on-chip implementation

2.3.2 Distributed Components LC Balun

The on-chip strip dipole antennas are integrated with the LC balun, as shown in Figure 2.2. The balun circuit with distributed inductors is designed in Metal 1 (as the signal line) and Metal 2 (RF ground plane) layers to feed signal from unbalanced GSG pads to the balanced antenna arms. The circuit is designed on the 11.4 μm thick (including the Metal 1 and 2) SiO_2 layer. The inductors are formed by thin MTLs, while the metal-insulator-metal (MIM), available IHP technology, is used to implement the capacitors. The shown parallel inductor and capacitor in Figures 2.2 are grounded using the vias between Metal 1 and 2 layers, as shown in Figure 2.2.

To realize the balun, the Z_c = 50 Ω MTL signal trace width, W, is calculated [52] using (2.2) for the SiO_2 substrate with ε_r = 4.1 and thickness of h = 8.4 μm between Metal 1 and 2. Therefore, the signal line width equal to 15 μm is obtained for on-chip 50 Ω MTL.

$$\frac{W}{h}=\begin{cases}\dfrac{8\exp(A)}{\exp(2A)-2} & \dfrac{W}{h}<2\\ A=\dfrac{Z_c}{60}\left\{\dfrac{\varepsilon_r+1}{2}\right\}^{0.5}+\dfrac{\varepsilon_r-1}{\varepsilon_r+1}\left\{0.23+\dfrac{0.11}{\varepsilon_r}\right\} & \\ \dfrac{2}{\pi}\left\{(B-1)-\ln(2B-1)+\dfrac{\varepsilon_r-1}{2\varepsilon_r}\left[\ln(B-1)+0.39-\dfrac{0.61}{\varepsilon_r}\right]\right\} & \dfrac{W}{h}\geq 2\\ B=\dfrac{60\pi^2}{Z_c\sqrt{\varepsilon_r}} & \end{cases} \tag{2.2}$$

Since the balun inductors are implemented using the distributed component, the width of the signal line that is used as an inductor is required to be thinner than the one that was calculated for 50 Ω transmission line (inductors need to have characteristic impedance higher than 50 Ω). Consequently, the minimum practical value (by IHP), 5 μm width MTL, is specified as the width of the transmission lines for implementing the distributed inductors. 5 μm MTL has inductive effect when it is connected to 50-Ω 15 μm MTL. Corresponding characteristic impedance and effective dielectric constant for the 5 μm width MTL can be obtained as Z_c = 79 Ω and ε_{re} = 2.61, respectively, using (2.3) and (2.4) [53].

$$\varepsilon_{re} = \begin{cases} \dfrac{\varepsilon_r + 1}{2} + \dfrac{\varepsilon_r - 1}{2}\left\{\left(1 + 12\dfrac{h}{W}\right)^{-0.5} + 0.04\left(1 - \dfrac{W}{h}\right)^2\right\} & \dfrac{W}{h} < 1 \\ \dfrac{\varepsilon_r + 1}{2} + \dfrac{\varepsilon_r - 1}{2}\left(1 + 12\dfrac{h}{W}\right)^{-0.5} & \dfrac{W}{h} \geq 1 \end{cases} \tag{2.3}$$

$$Z_c = \begin{cases} \dfrac{\eta}{2\pi\sqrt{\varepsilon_{re}}} \ln\left(\dfrac{8h}{W} + 0.25\dfrac{W}{h}\right) & \dfrac{W}{h} < 1 \\ \dfrac{\eta}{\sqrt{\varepsilon_{re}}}\left\{\dfrac{W}{h} + 1.393 + 0.677\ln\left(\dfrac{W}{h} + 1.444\right)\right\}^{-1} & \dfrac{W}{h} \geq 1 \end{cases} \tag{2.4}$$

The parallel inductor that is grounded using a via can be realized by a MTL with $W = 5$ μm and length of l_t, as shown in Figure 2.3 [54]. l_t determines the value of the parallel inductor, which is calculated by setting $Z_L = 0$ in (2.5) and replacing $Z_{in}(l_t) = j2\pi f L_t$ in (2.6).

$$Z_{in}(l_t) = Z_c \frac{Z_L + jZ_c \tan(\beta l_t)}{Z_c + jZ_L \tan(\beta l_t)} \tag{2.5}$$

$$Z_{in}(l_t) = jZ_c \tan(\beta l_t) \tag{2.6}$$

β is the propagation constant of transmission line in lossless media and is obtained as $\beta = 2\pi f\sqrt{\varepsilon_0\mu_0}\sqrt{\varepsilon_{re}}$. Therefore, the required length for 79 Ω ($W = 5$ μm) MTL to realize the parallel inductor with value of L_t is concluded as

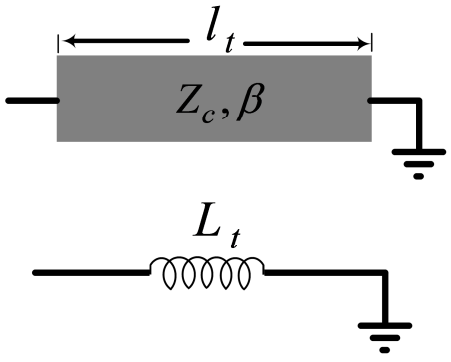


Figure 2.3: Microstrip transmission line model that is shorted at the end.

$$\theta = \beta l_t = \tan^{-1}(\frac{2\pi f L_t}{Z_c}), \qquad \theta < 90^\circ \tag{2.7}$$

where θ is the electrical length of the MTL.

Moreover, the series inductor can be obtained by exploiting the transmission line π model, as shown in Figure 2.4. In this model, the values of shown L_t and C_t can be calculate using the relations in (2.8) [55]

$$j2\pi f L_t = jZ_c \sin(\beta l_t) \tag{2.8 a}$$

$$j2\pi f C_t = j\frac{1}{Z_c}\tan(\beta l_t/2) \tag{2.8 b}$$

relation (2.8 b) presents that the characteristic impedance of MTL, Z_c, and capacitor value, C_t, are inversely related and by increasing Z_c, inductive property of the MTL dominates its capacitive property. Therefore, when a high-impedance MTL is connected to low-impedance transmission lines, its capacitive effect can be neglected versus the thicker lines; and it operate as an inductor with value shown in (2.8 a). Thus, the required 79 Ω-MTL (W = 5 μm) length for realizing the series inductor of the balun circuit is deduced from (2.8 a) as

$$\theta = \beta l_t = \sin^{-1}(\frac{2\pi f L_t}{Z_c}) \tag{2.9}$$

The relation (2.9) is valid for modeling the inductors with short-length high-impedance MTL. As an example, when a high-impedance MTL (Z_c) is terminated by an impedance Z_L, with real value, an inductor L_t can be modeled with that MTL, if $\leq \tan^{-1}(Z_c/Z_L)$ (by setting the imaginary part derivatives of Z_{in} in (2.5) to zero). Therefore, maximum series inductance that can be achieved from the high-impedance MTL is calculated from (2.9), as $2\pi f L_{t\_max} = Z_c^2/(Z_c^2 + Z_L^2)$. Although the length of the high impedance MTL can be extended up to calculated L_{t_max}, however, the parasitic capacitance of high impedance MTL will change the real and imaginary part of the impedance seen at the end of high impedance line.

Relations (2.7) and (2.9) can be employed to find the length of high-impedance MTL for implementing the parallel and series inductors of balun circuit, respectively.

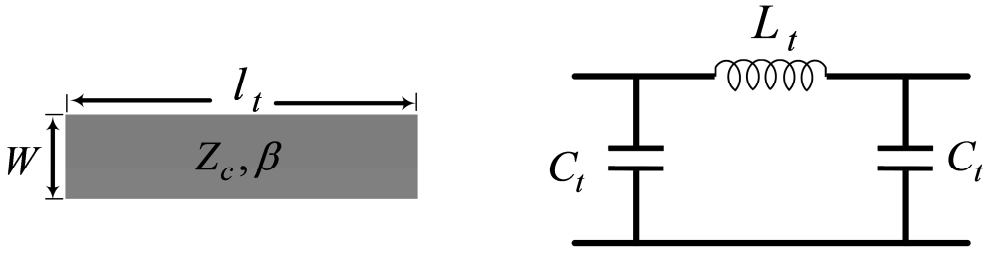


Figure 2.4: Microstrip transmission line LC model

2.4 Design Procedure for 77 GHz On-Chip Strip Dipole Antennas

Three different on-chip straight, L- and T-shaped antennas design for operating at 77 GHz is presented. The MTL length and widths for the introduced distributed/lumped component LC balun circuit is designed for 77 GHz. Different parameters of antennas integrated with balun circuit are swept to show their effect on the antenna performance. The Si substrate below the antenna is etched to reduce the Si loss.

2.4.1 LC Balun Design

The on-chip balun circuit is required to be operated at 77 GHz. This frequency is specified by balun circuit's L and C components as (2.1). Since the operating frequency is 77 GHz and the capacitors are realized by IHP MIM technology, the values of inductors are easily calculated. If a practical value of 37 *f* F ($(C\omega)^{-1}$ = 56 Ω) is determined for capacitors, the indictors will achieve 115 *p*H with respect to (2.1) and *f* = 77 GHz.

As discussed in 2.3.3, the signal trace width of 50 Ω MTL is calculated as 15 μm. If the high-impedance MTL with characteristic impedance of 79 Ω (trace width of 5 μm) is used for implementing the 115 *p*H inductors, relations (2.7) and (2.9) can be employed to obtain the parallel and series inductors values, respectively. Therefore, the calculated high-impedance line length will be 235 μm for parallel inductor and 300 μm for series inductor.

The HFSS model (see Figure 2.2) of the balun circuit is initially started with the calculated values for MTL length and width for inductors, 50 Ω MTL width and inserting lumped 37 *f* F capacitors. Since the series inductor is a high-impedance MTL with parasitic capacitors (is not ideal inductor), and also electromagnetic (EM) coupling between the lines, discontinuities and vias parasitic effect, the lengths of the series and parallel inductors are optimized to operate

the balun at 77 GHz. At the end of optimization, the lengths of the parallel and series inductors are changed to 255 μm and 220 μm, respectively.

The balun structure occupies an area of 200 μm × 210 μm. For measurement purposes, an additional 500 μm long MTL is connected to decrease the effect of the RF measurement probe on the antenna radiation pattern.

In Figure 2.5, the S_{11} at the input port P_{in} and the S_{12} and S_{13} between the input and output ports are plotted. Return loss is around 31 dB and the insertion loss between the ports P_{in}-P_{out1} and P_{in}-P_{out2} are around 3.7 dB at 77 GHz. Additional 0.7 dB is the result of conductor loss of the MTLs at these frequencies. In Figure 2.6, the phases of the ports are plotted with P_{in} port as the reference. One notes that the phase difference between P_{out1} and P_{out2} ports are 180°; which is required to excite both of the dipole antenna arms symmetrically.

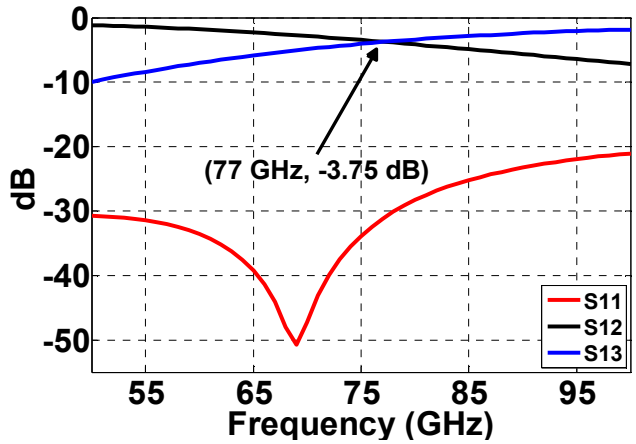


Figure 2.5: Simulated scattering parameters of the balun circuit.

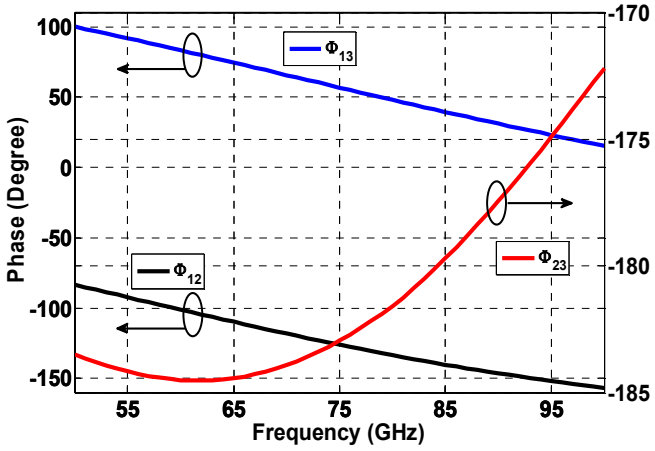


Figure 2.6: Simulated phase difference between different ports.

2.4.2 Straight Dipole Antenna

The on-chip strip dipole antenna fed by the LC balun circuit is shown in Figure 2.7. To design this antenna, the balun circuit is integrated to the strip dipole antenna with etched Si substrate, firstly. As discussed, the etched Si substrate will cause to decrease the Si loss. To increase the stability of the remaining SiO_2 layer, two silicon bars are left between the etching windows (Figure 2.7).

Then, the dimensions of the strip type dipole antennas and the parameters of the balun circuit are optimized for both the impedance matching in a 50 Ω measurement system and the maximum gain of the antennas.

Thus, HFSS simulations are done in terms of dipole length/width, width of the silicon bars ($w1$), etching window size (Δw) and capacitance of the balun circuit. Finally, the antenna optimum performance is obtained by setting the chip parameters with values shown in Table 2. 1. To study the effect of each parameter on antenna performance, the dimensions are swept around their optimum values with respect to the values in Table I. Moreover, the overall size of the chip (the dipole antenna which is surrounded by Si substrate) is 4 mm × 3 mm over the optimization process and the chip is placed on a ground plane with the same size.

The length of the dipole determines the first resonance frequency (°λ/2) and variation of the antenna length versus antenna reflection coefficient is plotted in Figure 2.8. For a dipole length of 1000 μm, the $|S_{11}|$ is obtained as smaller than -20 dB at 75 GHz. There is no silicon

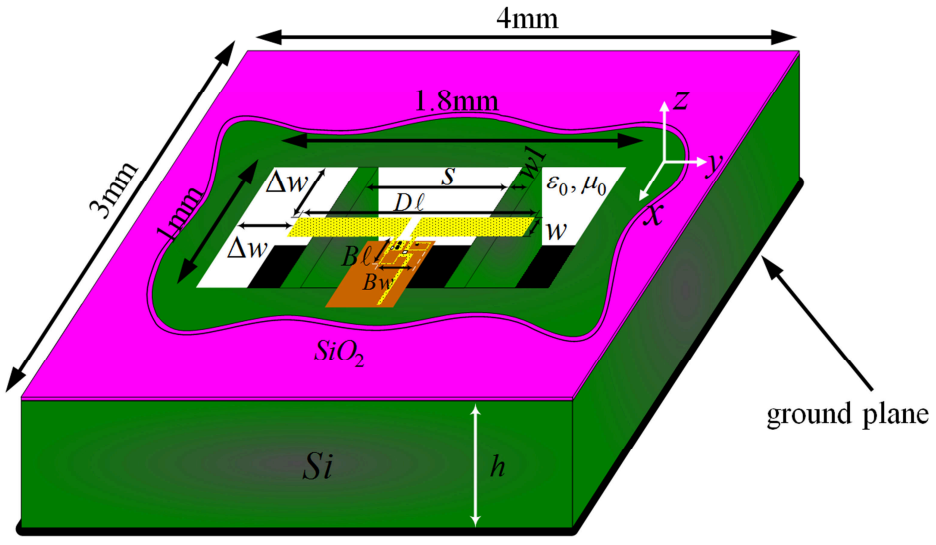


Figure 2.7: Schematic of the straight dipole antenna

Table 2.1: Straight dipole antenna parameters value

Parameter	Value
$D\ell$	1000 μm
w	100 μm
S	700 μm
$w1$	100 μm
Δw	400 μm
feed gap	40 μm
$B\ell$	200 μm
Bw	210 μm
Capacitors	37 fF
Antenna + circuit size	1.8 mm × 1 mm
Chip size	4 mm × 3 mm

substrate under the antenna in the simulated structure and the antenna is placed on a 11.4 μm thick SiO_2 layer. For the stability of the SiO_2 layer, the maximum etch size that is realized by IHP is 700 μm × 700 μm. Therefore, for antennas longer than 700 μm, multiple etch windows can be used, as shown in Figure 2.7, and Si bars are left between these etch windows. Since the bars and antenna arms are very close in some parts, they will affect the impedance and gain of the antenna. The reflection coefficients and gain of the antenna at $\theta = 0°$ for different thicknesses of Si bars are obtained in Figure 2.9. As expected, with thicker silicon bar walls, the effective dielectric constant will increase and resonance frequency, as well as the gain of the antenna, will drop. To minimize the substrate loss, the silicon bars are placed to the most possible distant points (low current distribution) from the terminal of the antenna (each silicon bar is 350 μm away from the dipole terminal point). For this simulation, it is assumed that the Si substrate under the antenna is totally etched away except for the two silicon bars.

While optimizing the impedance of the antenna, one should also look at the antenna gain performance. As the wall width changes, both antenna resonance frequency and the loss introduced by the Si bars are changed. The combined effect can be seen in Figure 2.9, which shows 4 dBi gain for a 100 μm silicon bar width at 77 GHz.

The next step in the simulations is to obtain the antenna reflection coefficient when the size of the etch windows at the right and left sides in Figure 2.7 are changed. The size of windows can be controlled by Δw, which is the distance between any edge of the flat dipole antenna and the start of the unetched part of the silicon substrate. In Figure 2.7, if Δw is set to zero, only the Si below the arms end parts (the parts after Si walls) are etched, whereas all the around etches are filled by setting $\Delta w = -50$ μm. As it is displayed in Figure 2.10, for $\Delta w = -50$ μm, antenna resonance frequency is at 60 GHz. As the etching window size is made larger, the antenna resonance frequency goes up, and after 300 μm, the effect of the etching window size on the antenna input impedance becomes smaller and settles at 77 GHz with $|S_{11}|$ of smaller than -15 dB.

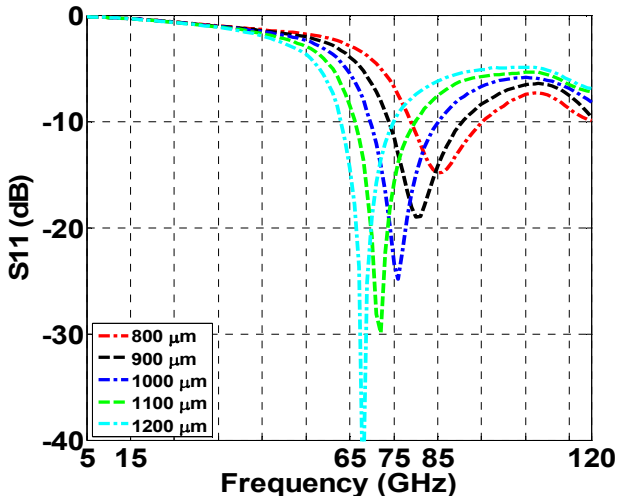
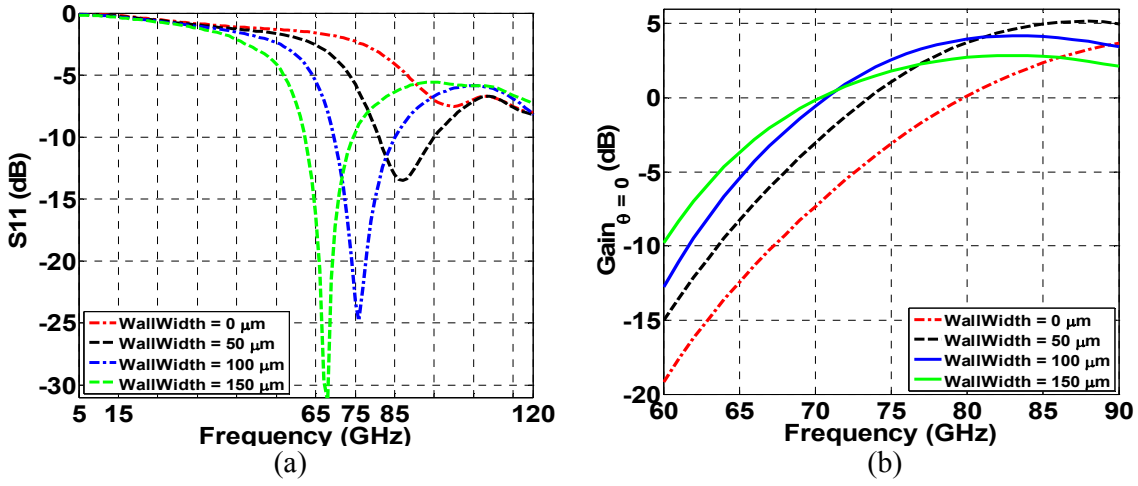
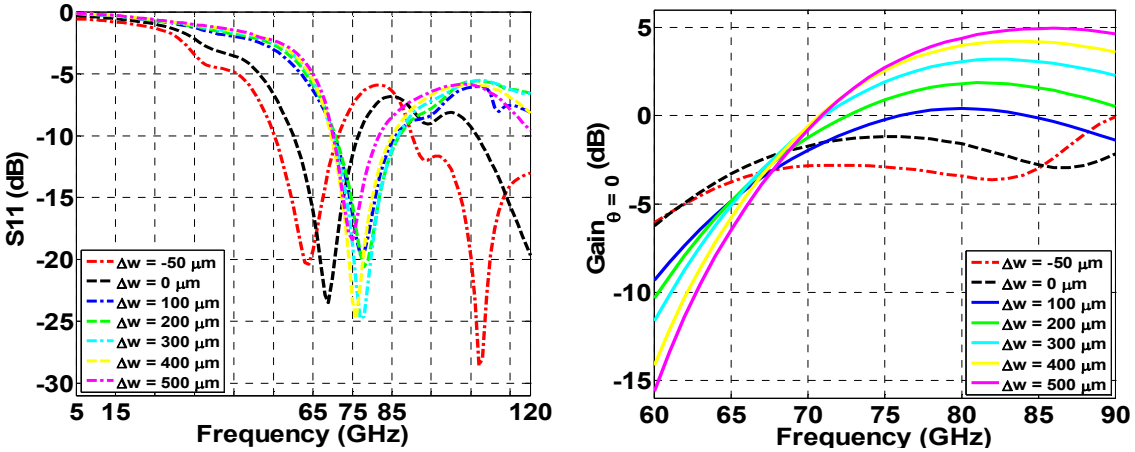


Figure 2.8: Reflection coefficient of the flat dipole antenna for different $D\ell$.



(a) (b)

Figure 2.9: (a) Reflection coefficient and (b) gain of the flat dipole antenna for various $w1$.



(a) (b)

Figure 2.10: (a) Reflection coefficient and (b) antenna gain for different Δ*w*.

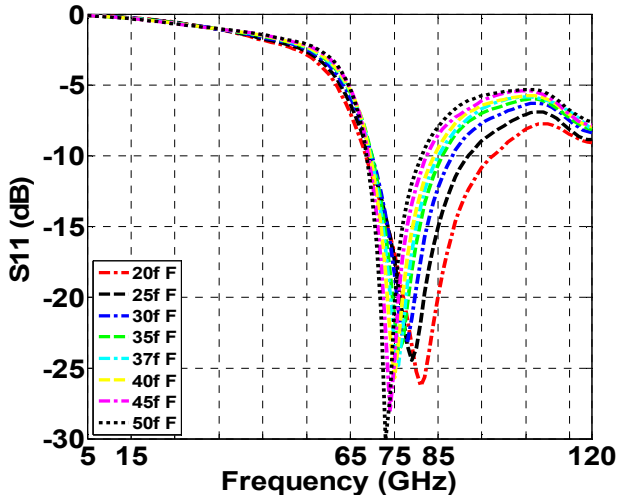


Figure 2.11: Reflection coefficient for various capacitance values in LC balun.

Another parameter which will affect the antenna gain is the substrate loss which is varied by changing the size of the etching window around the antenna. In Figure 2.10, antenna gain is also shown for different etch size windows. As the etch size is changed, antenna gain increases and after a 300 μm distance between the antenna and the silicon substrate, the additional gain of the antenna is incremental.

The last varied parameter is the capacitance of the LC balun circuit feeding the dipole antennas as shown in Figure 2.11. The capacitance is varied between 20 *f* F and 50 *f* F to obtain the best performance in terms of impedance matching at 77 GHz. $|S_{11}|$ of -23 dB is obtained at 77 GHz for a 37 *f* F capacitance value. Note that if a variable capacitance is used, antenna resonance can be easily tuned with a DC bias.

The E (*zy*-plane) and H planes (*zx*-plane) radiation patterns of the final optimized antenna at 77 GHz is shown in Figure 2.12. The maximum gain of around 3 dBi is obtained for dipole antenna with small ground plane under the chip. Generally, the half wave dipole antennas have maximum gain of 2.15 dBi. It was expected that the ground plane, which is placed at the $\lambda_g/4 \approx 670$ μm distance of the dipole antenna, increases the on-chip dipole antenna gain by two (2.15 dB + 3.01 dB = 5.16 dBi). However, the losses that are resulting from the balun circuit and Si substrate decrease the simulated gain maximum value to 3 dBi. Since the ground plane below the chip is small, thus the antenna is also radiating to the bottom with the gain of -1 dBi (see Figure 2.12). 3D plot of the realized antenna gain is with maximum of 3.2 dBi in presented in Figure 2.13.

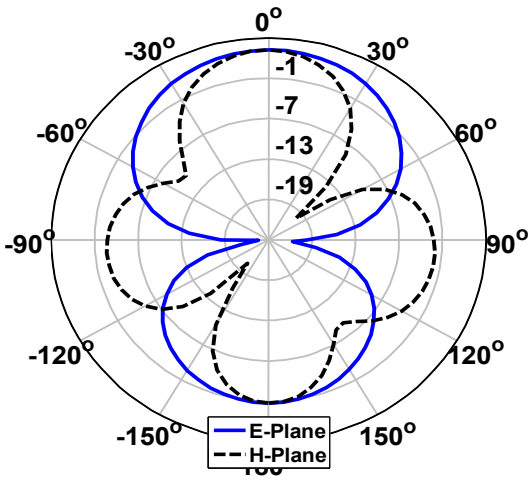


Figure 2.12: E- and H-plane radiation pattern of dipole antenna.

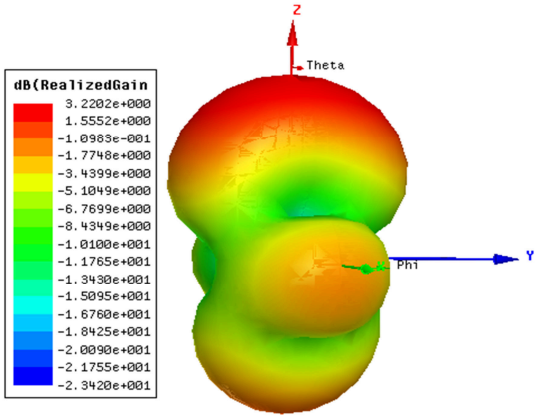


Figure 2.13: 3-D radiation pattern of dipole antenna

2.4.3 L-Shaped Dipole Antenna

The second on-chip antenna that is designed here is the L-type dipole antenna as shown in Figure 2.14. As a trade-off between antenna gain and the chip size, dipole antenna ends are folded. Due to antenna's small size, the etching window can be made much smaller, and hence, the need for the silicon bars is eliminated. This type of dipole design also reduces the substrate loss introduced by the Si bars used in straight dipole antenna. This structure is optimized using geometrical parameters such as length of the dipole arms, the length of the end sections which form then L-structure, the size of the etching window and the distance between the antenna and the ground plane of the LC balun circuit. The same balun circuit as the straight antenna is used in this antenna; the only difference is the length of the feeding MTL, that is smaller in the L-shaped antenna. This type of antenna occupies an area of 690 μm × 500 μm. The optimized antenna dimensions at 77 GHz are shown on the Figure 2.14. The simulated antenna achieves 11 GHz 10-dB bandwidth around 77 GHz band as shown in Figure 2.15. The E- and H-planes radiation patterns of the L-type antenna with maximum value of 0.66 dBi at 77 GHz are given in Figure 2.16. Since the currents' distribution on parallel arms opposes with each other, the antenna total gain is decreased. Therefore, the maximum gain of the L-type antenna is lower compare to the straight antenna.

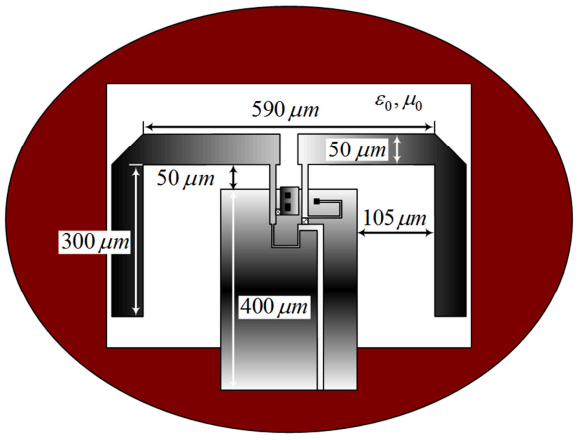


Figure 2.14: Top view for the L-type dipole antenna.

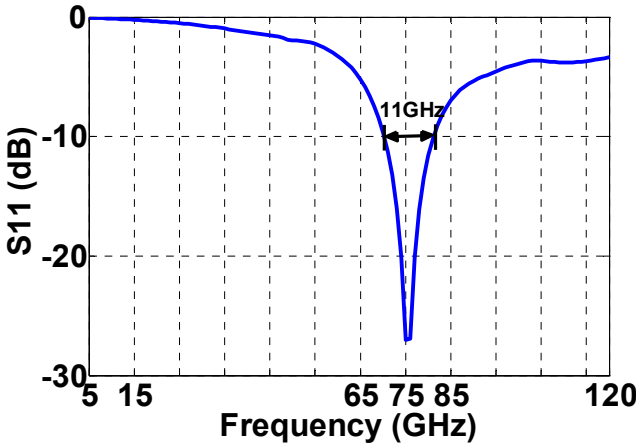


Figure 2.15: Reflection coefficient of the L-type antenna.

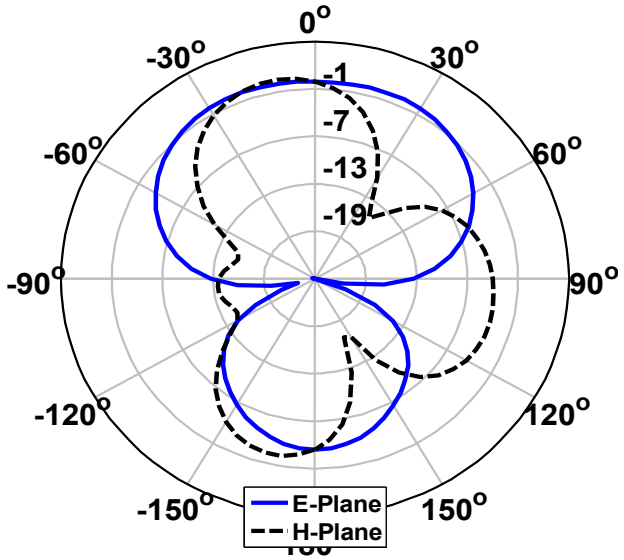


Figure 2.16: E and H-plane radiation pattern of L-type dipole antenna.

2.4.4 T-Shaped Dipole Antenna

One can also fold the dipole arms to form T-type dipole antenna (see Figure 2.17) to gain from the chip area as well as from the reduced loss of Si substrate. The T-type dipole antenna which is optimized with respect to its impedance matching and the gain criteria is shown in Figure 2.17. The antenna occupies an area of 690 μm × 650 μm and achieves 12 GHz 10-dB bandwidth at 77 GHz band as shown in Figure 2.18. The optimized T-type antenna has gain of 1.34 dBi at 77 GHz; radiation patterns in E- and H-planes are given in Figure 2.19.

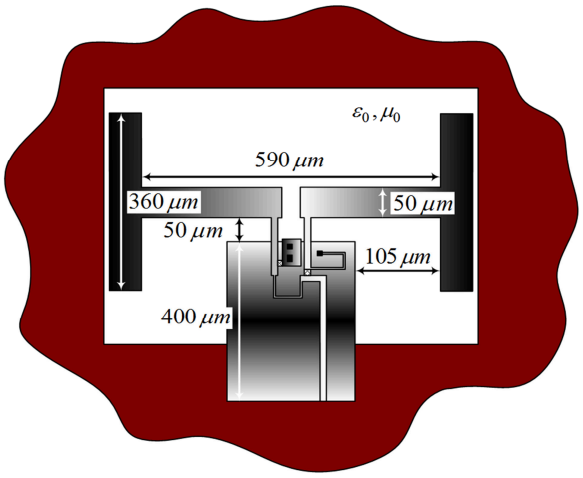


Figure 2.17: Top view for the T-type dipole antenna.

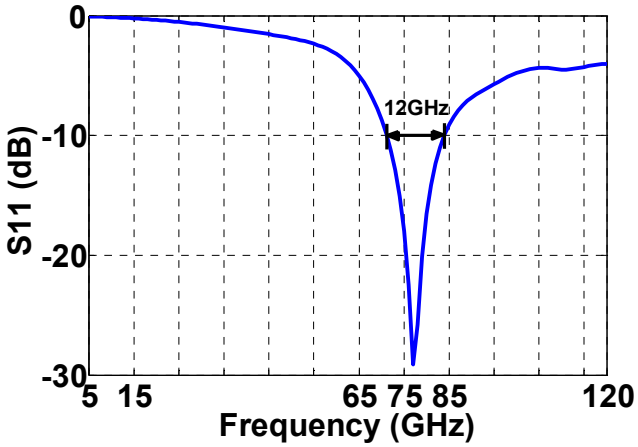


Figure 2.18: Reflection coefficient of the T-type dipole antenna.

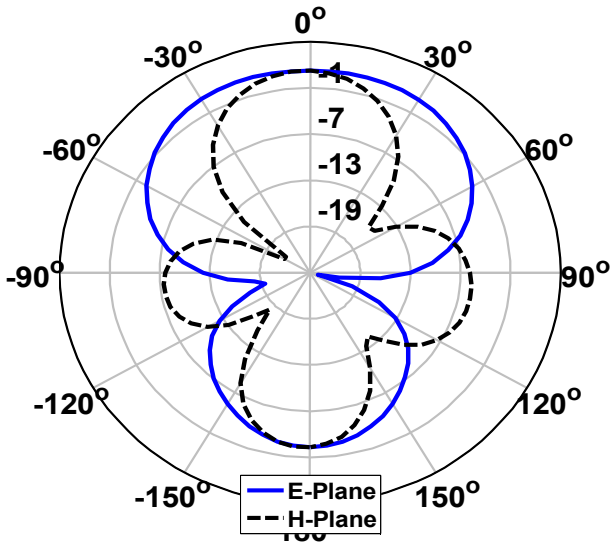


Figure 2.19: E and H-plane radiation pattern of T-type dipole antenna.

2.4.5 L- and T-Shaped Dipole Antennas Applications in an Array

To minimize the dipole antenna size with a resonating length of λ/2, the antenna arms were bent (L- and T- shaped antennas), which reduces the size of the antenna and accordingly the chip size for both single antenna and array applications. By bending each strip's arms in a symmetric shape, the current distributions on the bent sections (shown on each antenna in Figure 20.20) will be in opposite directions. The interaction between two parallel lines carrying currents in opposite directions is additive between the lines and subtractive outside of the lines if the distance between those lines is smaller than λ/2. In addition, simulation results of L- and T-shaped dipole antennas alone for co-/cross-polarization radiation patterns (at 77 GHz) in E-/H-planes, in Figure 20.21, confirms the small value of cross-polarization components versus the co-polarized gains. Therefore, the L- and T-shaped antennas behave very similar to straight dipole antenna and bending the antenna arms just leads to decrease the antenna size. When the antennas are utilized in an antenna array, as it is shown in Figure 2.20, the total coupling between adjacent antennas will be small. Furthermore, the opposite currents' flow on each bent section of the T-type antenna can be canceled by that

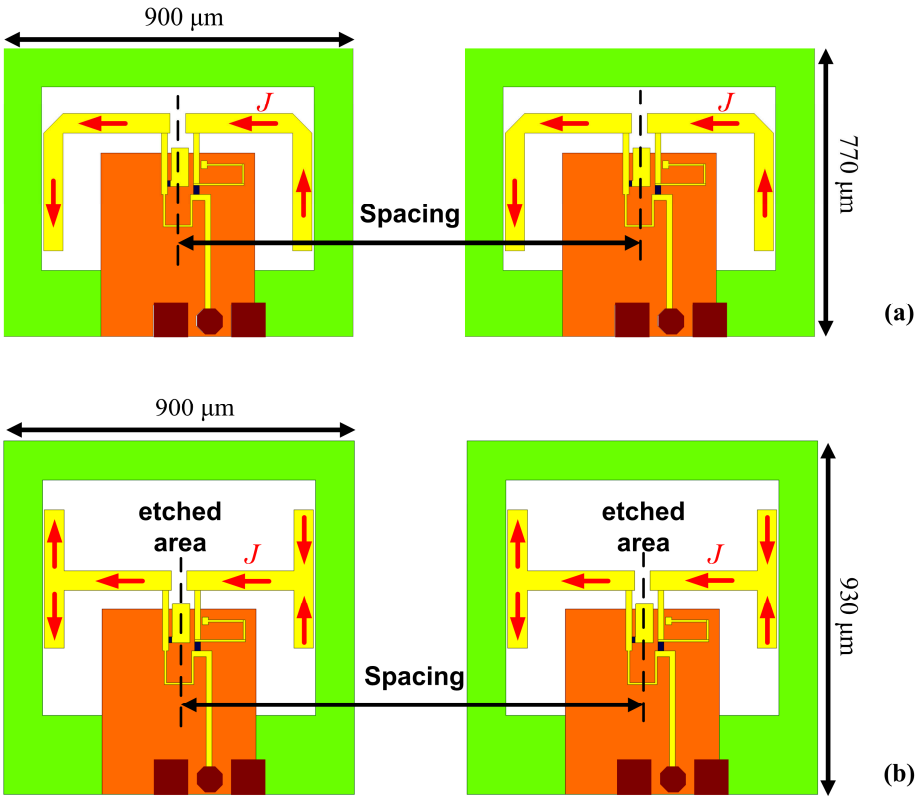


Figure 2.20: Schematics of the two-element 1×2 array using (a) L-shaped and (b) T-shaped on-chip dipole antennas

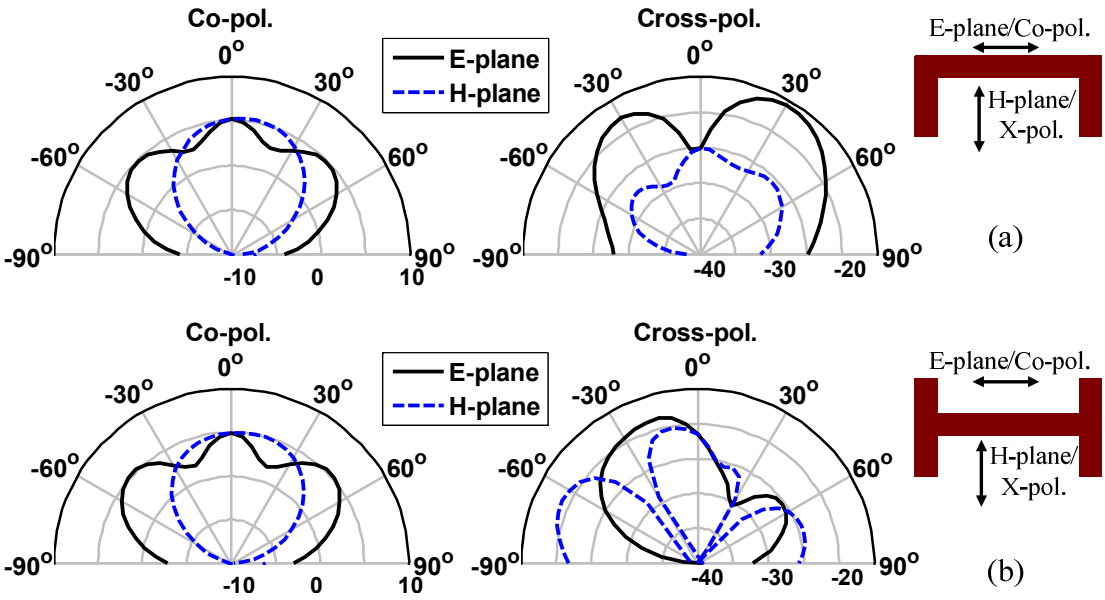
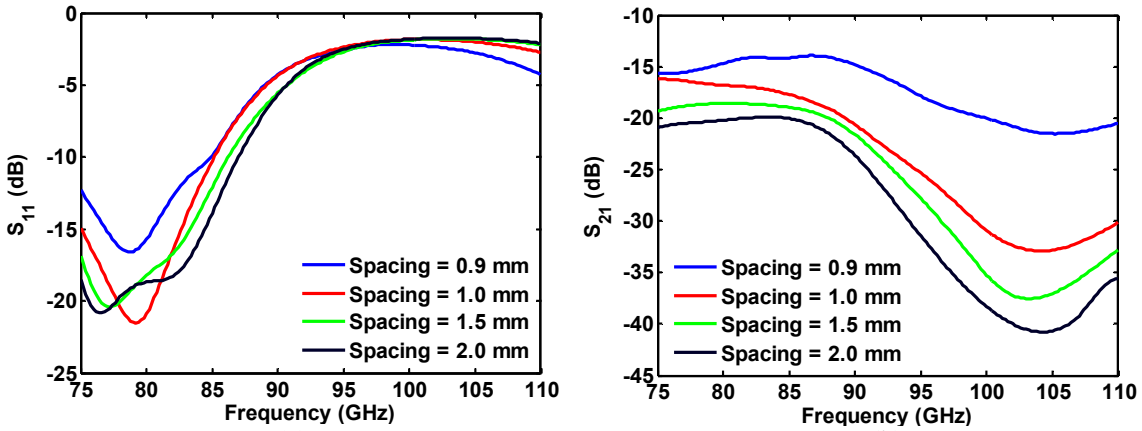


Figure 2.21: Simulated radiation patterns at 77 GHz for (a) L-shaped and (b) T-shaped dipole antennas on large ground plane.

arm alone. However, the effect of bent arms have not to be observed both inside and outside of the bent arms. Therefore, the T-type antenna has to have performance very similar to the short-length straight dipole antenna; and the smaller mutual coupling between the adjacent T-type antennas is expected. This can be the advantage of the T-type antenna over the L-type dipole in the array application.

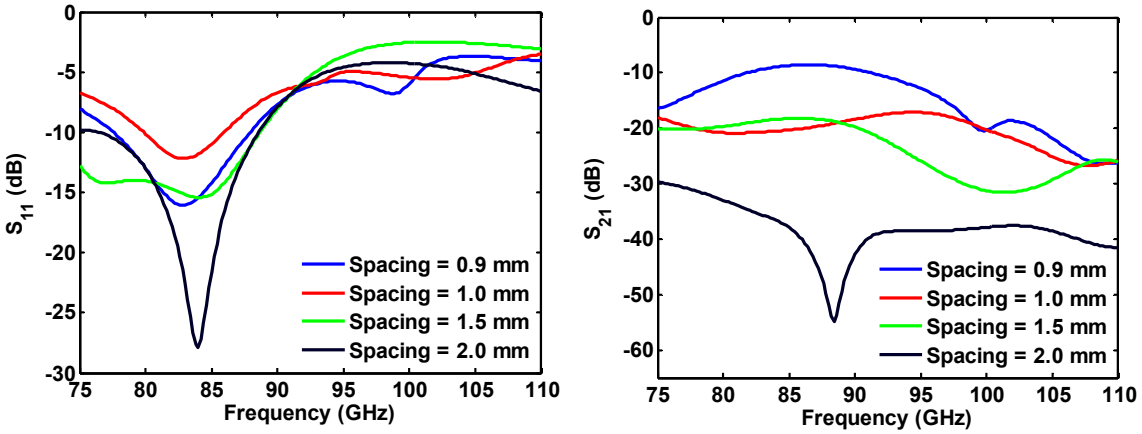
The 2-element antenna array is simulated for each of the L- and T-shaped antenna, as shown in Figure 2.20. The reflection coefficients and isolation between the two antennas for different spacings are shown in Figures 2.22 and 2.23, for L- and T shaped antennas, respectively. Since the elements of each array are same, both S_{11} and S_{22} are similar. As it is seen in Figures 2.22 (a) and 2.23 (a), the antennas resonance are shifted to around 80 GHz (for L antenna) and 85 GHz (for T antenna), while they were designed to be operated at 77 GHz. This frequency shift is coming from the large ground plane below the antennas and inserted GSG pads model in the simulations, which will be discussed in Chapter 3.

The isolation between the antennas is better than 15 dB for L antenna and 10 dB for T antenna which are occurred when the antennas are connected to each other. As it is shown in Figure 2.20, the maximum dimension of the chips is 900 μm at the side that the spacing between the elements is accounted. This means the chips are connected as the spacing approaches to 0.9 mm. 0.9 mm is small value as it is compared with $\lambda/2$ @ 77 GHz $\approx$ 2 mm.



(a) (b)

Figure 2.22: (a) Reflection coefficients and (b) isolation for various spacings between the elements of the 1×2 L-shaped dipole array antenna.



(a) (b)

Figure 2.23: (a) Reflection coefficient and (b) isolation for various spacings between the elements of the 1×2 T-shaped dipole array antenna.

Consequently, the results show that the L- and T-shaped antennas can be employed as the elements of an antenna array with small coupling between the adjacent elements.

2.5 Designed Antennas for 94 GHz application

The performed designs for the 77 GHz are modified to operate the antennas at 94 GHz. The Si substrate thickness that is used for 94 GHz on-chip dipole antennas is 450 μm (it was 670 μm for antennas designed at 77 GHz).

2.5.1 LC Balun Design

The same procedure that was applied to design of 77 GHz balun circuit is implemented to operate the LC balun at 94 GHz frequency. For 94 GHz balun the 20 *f*F capacitors (has an impedance of $((C\omega)^{-1}$ = 84 Ω) at 94 GHz) is selected and hence, 143 *p*H inductors value is then calculated from (2.1). Therefore, the equivalent 258 μm and 494 μm long high-impedance MTL are calculated for shunt and series inductors, using (2.7) and (2.9), respectively.

Full-wave HFSS simulation of the 94 GHz balun with 20 *f*F capacitors, as it is shown in Figure 2.24, shows the required lengths of 105 μm and 150 μm high-impedance MTL for shunt and series inductors, respectively. As shown in Figure 2.24, the high-impedance lines are folded and spacing between the thinner MTL is small. This small distance increases the coupling between the lines and proportionally the inductance of the thinner lines. Consequently, the required length of high-impedance MTL to model the inductors is decreased, significantly. Moreover, the series inductor has two parasitic capacitances (see Figure 2.4) that is paralleled with 20 *f*F balun capacitor. One of these parasitic capacitors is added to the 20 *f*F and increases the balun capacitance value, which results in reducing the required balun's series inductor value (relation (2.1)). Note that, each parasitic capacitance for 494 μm and 150 μm long high-impedance MTL (5 μm width) are calculated as 21.4 *f*F and 5.2 *f*F, respectively. Therefore, the balun's shunt capacitance value will be around 25.2 *f*F (20 + 5.2) which will need series inductance of 113 *p*H (320 μm long high impedance MTL) for operating the balun at 94 GHz. However, HFSS simulation shows 150 μm long high impedance MTL for series inductor which has calculated inductor of 61.5 *p*H for straight line. Due to coupling between the folded inductance MTL, the calculated lengths of 258 μm for

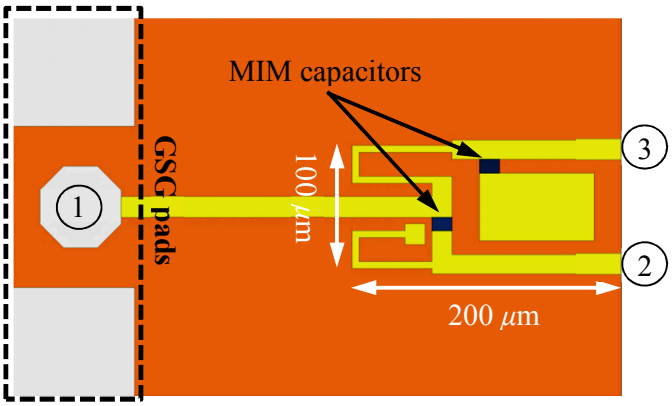


Figure 2.24: HFSS model of the designed on-chip LC balun circuit for 94 GHz operation.

shunt and 320 μm for series inductors are decreased to 105 μm and 150 μm, respectively. Furthermore, the 94 GHz balun circuit is designed with ground-signal-ground (GSG) feeding pads to include the effect of GSG pads in the design. The GSG pads and its effect will be discussed in the next chapter.

The simulated results for 94 GHz balun are shown in Figures 2.25 and 2.26 for S-parameters and phase difference between the output ports, respectively. 3.94 dB insertion loss at 94 GHz between input and each of the output ports is obtained in the simulation, which shows 1 dB loss between input/output signal. S11 is below -20 dB from 50 GHz to 120 GHz. Phase difference between the output ports is 178° at 94 GHz and changes between 157° to 182° from 50 GHz to 120 GHz.

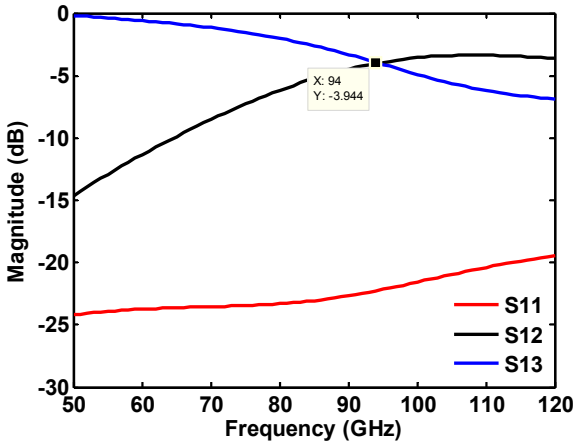


Figure 2.25: Simulated S-parameters for the designed balun at 94 GHz.

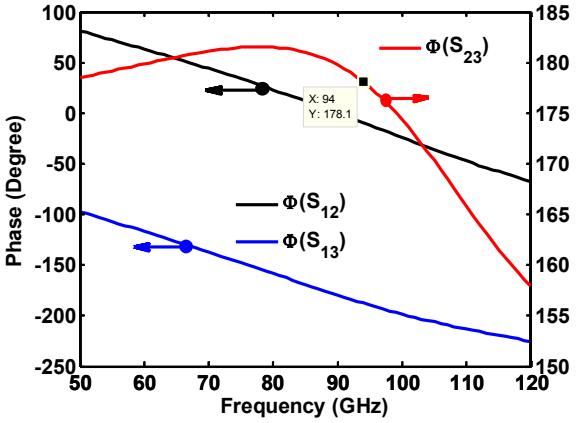
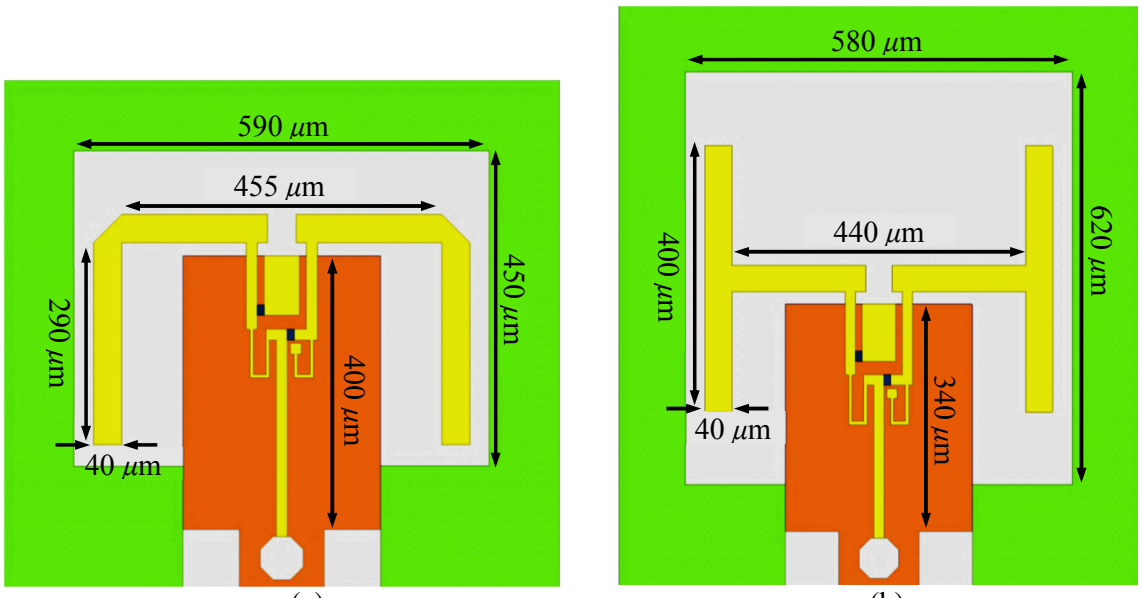


Figure 2.26: Simulated phase at the outputs of the LC balun and their difference.

2.5.2 L- and T-Shaped Antennas

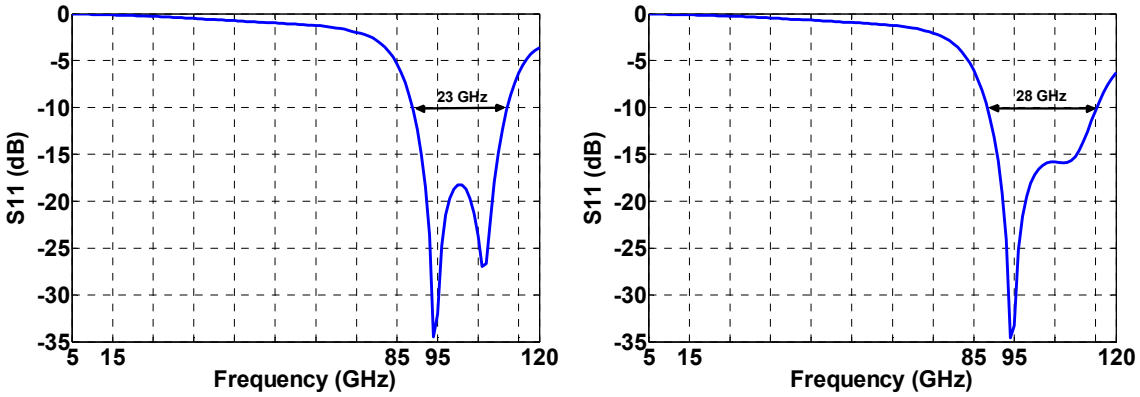
The L- and T-shaped on-chip dipole antennas are designed on 450 μm thick Si substrate for operating at 94 GHz. The other differences between the designed 77 GHz antennas (in former sections) and 94 GHz L and T antennas (here) are the large ground plane (around 20 mm × 20 mm) below the Si substrate and including the GSG pads during the design process. The GSG pads can effect on antenna reflection coefficient, while the size of ground plans cause to changes in radiation pattern of the antennas which are shown in the next chapter.

The designed L and T antennas with the optimum dimensions are shown in Figures 2.27 (a) and (b), respectively. The free space wavelength at 94 GHz is λ_0 = 3.2 mm. However, due to the Si substrate around the antennas, the L antenna is resonating with the total antenna length of 1 mm and T antenna with 1.2 mm. Since the antenna dimensions are small, only single etch (shown white area beneath the antennas) is employed and optimized during the simulation. Thickness of the margin Si walls around the etched areas is 100 μm. The simulated reflection coefficients and gains of the antennas in E- and H-planes for 94 GHz are shown in Figures 2.28 and 2. 30, respectively. L antenna shows 23 GHz 10-dB bandwidth around 94 GHz while it is 28 GHz for T antenna.



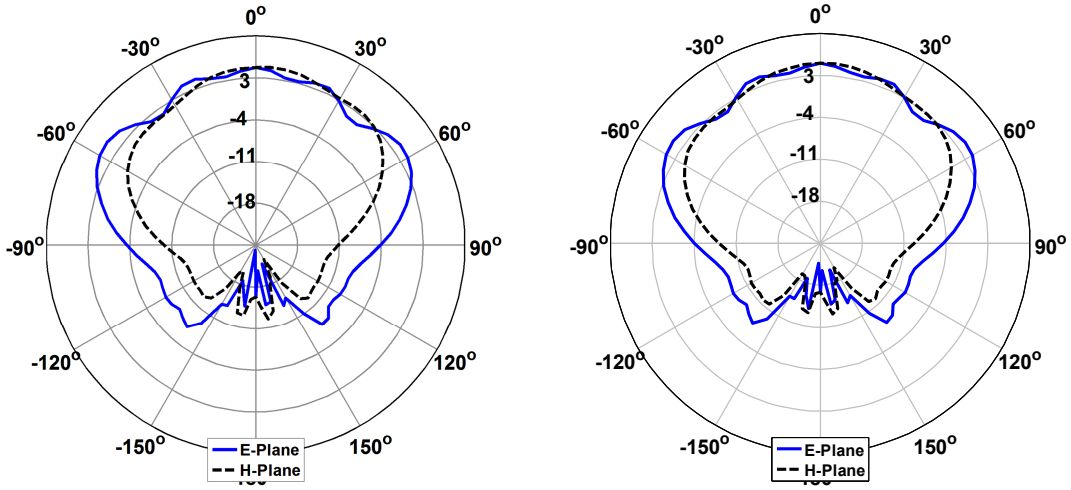
(a) (b)

Figure 2.27: Designed (a) L- and (b) T-shaped on-chip antenna for operating at 94 GHz.



(a) (b)

Figure 2.28: Simulated 94 GHz antenna reflection coefficients for (a) L- and (b) T-antennas.



(a) (b)

Figure 2.29: Simulated gains at 94 GHz and E-/H-planes for (a) L- and (b) T-shaped antennas.

Both of the antennas have gains around 5 dBi at $\theta = 0°$ and have very similar shapes and values. As it is shown in Figure 2.29 (a) and (b), the gain patterns in E-planes are distorted and achieve maximum at $\theta = \pm 60°$ gains. This phenomenon is arisen from thick Si substrate that excites surface waves which are reflected/diffracted from the large ground plane below the Si substrate.

CHAPTER 3

INFLUENCE OF DIFFERENT PARAMETERS ON PRACTICAL PERFORMANCE OF THE ON-CHIP ANTENNAS

Literatures present various types of automotive radar antennas that are designed and characterized at W-band [56-59]. Usually, some frequency shift between the measured and simulated data are observed [60-64] which are attributed to different parameters such as uncertainty in substrate dielectric constant, measuring probe [65], balun circuit [66] and etc.

In this chapter the practical aspects of the designed W-band on-chip strip dipole antennas are investigated. The dimensions and size of the on-chip antennas can be changed within the manufacturing tolerances during the fabrication or dicing the antennas on the wafer. The embedded coplanar ground-signal-ground (GSG) pads for probing purpose, calibration kit, metal chuck size of the measuring set-up and type of the GSG probe can impose significant effect on the measured results of the on-chip antennas at W-band frequency. Therefore, the measurement environments are taken into consideration and new simulated results are compared with the measured results. These investigations can give very valuable information in the designs which can be performed in the future and help to be more familiar with the measurement instruments and their effect on the practical data.

3.1 GSG Pads Effect on Antenna Reflection Coefficient

Since the antennas are intended to be used in the front end of an on-chip automotive radar receiver, they are not designed with GSG pads. They are designed by exciting the MTL with a lumped port in HFSS and the effect of GSG pads are not considered in simulations. However, to probe the manufactured on-chip antenna and measure its performance, the coplanar GSG pads (see Figure 3.1) are essential parts that have to be included in the fabrication of the antennas. The dimensions of these pads that are used in the fabricated chips here are shown in Figure 3.1. These pads are implemented in Metal 2 layer

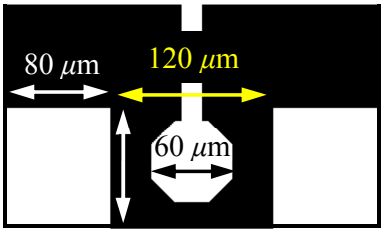
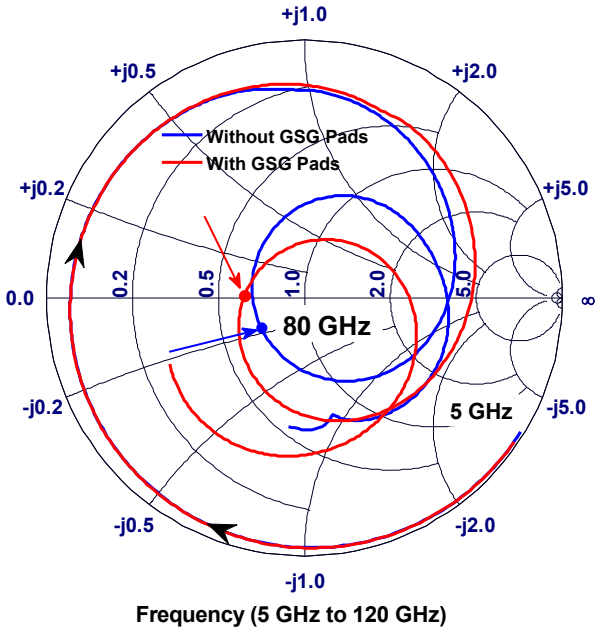
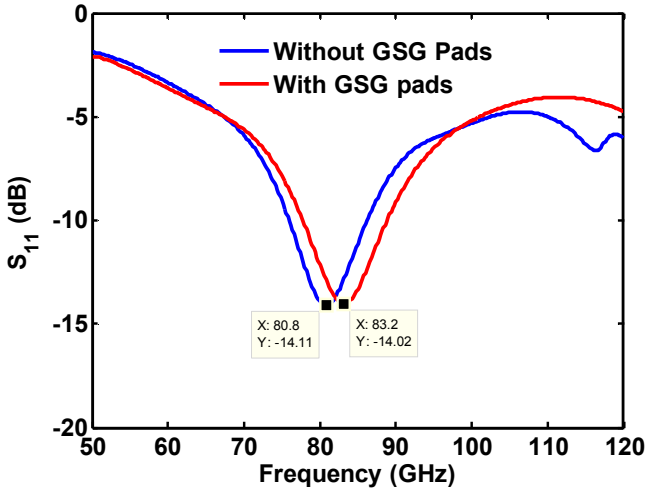


Figure 3.1: GSG pads dimensions



(a)



(b)

Figure 3.2: Effect of the GSG pads on the on-chip straight dipole antenna.

and two lateral ground pads are connected to Metal 1 (see Figure 2.1) as the RF ground plane using the vias. These GSG pads with the shown dimensions operate similar to grounded back

coplanar waveguide (GBCPW) with different characteristic impedance than 50 Ω. The simulation results of the designed 77 GHz straight dipole antenna without and with the GSG pads are shown in Figure 3.2 (a), for frequency range of 5 GHz to 120 GHz. The GSG pads operate as a short length transmission line for frequencies below 50 GHz and hence its effect can be negligible for those frequencies. However, for frequencies higher than 50 GHz it imposes an 80 μm long transmission line effect which causes to shift the resonance frequency of the straight dipole antenna to higher value, as it is shown in Figure 3.2 (b). For this type of antenna, a frequency shift around 2.4 GHz is observed due to the GSG pads. Consequently, the GSG pads effect has to be considered in the proceeding simulations to have a reasonable comparison between the measurement and simulation results.

It was mentioned in the Table 2.1 that the designed straight dipole antenna's chip size is 4 mm × 3 mm while the antenna and RF circuit occupy only an area of 1.8 mm × 1 mm on the center of the chip. The design with massive Si around the antenna was performed to approach a close model of straight dipole antenna when it is integrated in radar chip. However, increasing the chip area is costly and the on-chip antenna is manufactured with total chip size of 2 mm × 1.2 mm (100 μm Si walls are left at the margins of 1.8 mm × 1 mm antenna). Therefore, the designed on-chip antenna frequency resonance at 77 GHz is shifted to 80.8 GHz due to the removed Si around the antenna (reducing the chip size from 4 mm × 3 mm to 2 mm × 1.2 mm).

3.2 Ground Plane Size Effect on Antenna Performance

Although the antennas are designed on the ground planes with the same size of the chip, however they are measured on metal chuck of set-up which is large compare to wavelength over the W-band frequency. The ground plane was used during the design process to increase the antenna directivity. The size of the ground plane causes to minor effect on antenna reflection coefficient and major distortion on antenna radiation pattern.

3.2.1 Effect on Antenna reflection Coefficient

The ground plane size below the antenna can affect on the antenna reflection coefficient by changing the near field around the antenna. Since the antenna near field range is small, inserting a small ground plane can help to model the large ground of chuck in the simulation.

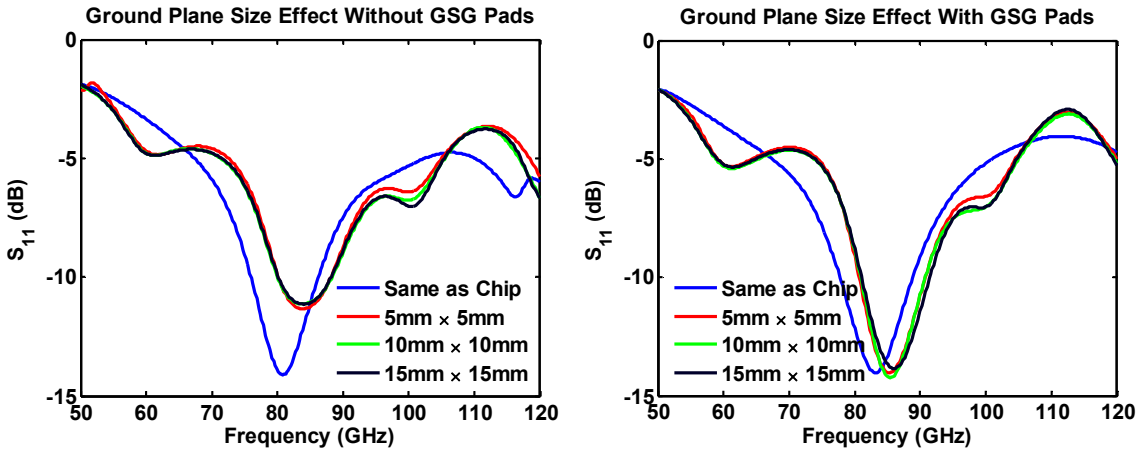


Figure 3.3: Effect of ground plane size on antenna reflection coefficient for exciting (a) without and (b) with GSG pads model.

The effect of ground plane below the simulated 2 mm × 1.2 mm straight dipole antenna is displayed in the Figure 3.3. The simulations are performed for ground planes as the chip size and other square planes with different dimensions with/without the GSG pads. Antenna reflection coefficient is changing as the ground plane size is changed from chip size (2 mm × 1.2 mm) to 5 mm square and remains unchanged for greater ground planes.

3.2.2 Radiation Pattern distortion

Although the chuck effect on antenna reflection coefficient can be considered by a small 5 mm × 5 mm square ground plane in simulation, however, to obtain the far field radiation pattern of the antenna, a large enough ground plane with respect to wavelength at the operating frequency should be placed. The effect of different ground plane size on the antenna E-plane (*yz*-plane in Figure 2.7) radiation pattern is shown in Figure 3.4. The different ground plane sizes are $(1.25\ \lambda_o)^2$, $(3.75\ \lambda_o)^2$,$(6.25\ \lambda_o)^2$ and same as the antenna size (2 mm × 1.2 mm). The plane sizes are in term of wavelength at 75 GHz and radiation patterns are shown in the form of normalized gain. As shown in Figure 3.4, for a small ground plane, the maximum simulated gain is at $\theta = 0^o$ (-3.14 dBi), and for the $(1.25\ \lambda_o)^2$ ground plane, a maximum gain is obtained around $\theta = \pm 40^o$ (-1.16 dBi). As the ground plane size is increased, two additional lobes with values 0 dBi appear around at $\theta = \pm 60^o$. As the ground plane size is increased two side lobes are appeared due to surface waves (TM and TE modes) excited by thick substrate (substrate is thick as it is compared with the operating frequency wavelength) [67-70].

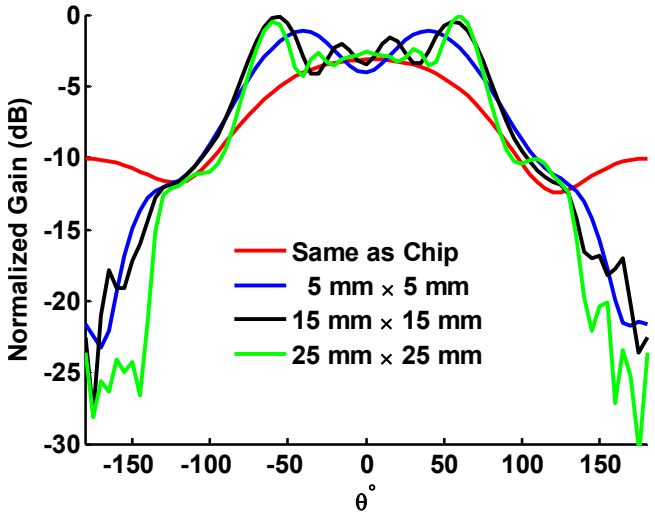


Figure 3.4: Effect of ground plane size on the antenna E-plane radiation pattern distortion

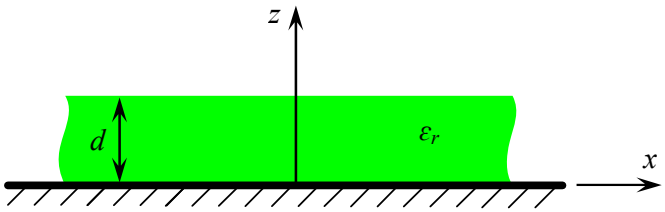


Figure 3.5: Grounded dielectric

Theoretically, TM and TE surface waves [54] can propagate in $+x$ direction if an infinite dielectric slab with thickness of d and permittivity of ε_r is grounded, as shown in Figure 3.5. The cut-off frequency for TM and TE waves can be calculated using (3.1) and (3.2), respectively. TM modes contain electric fields only in x and z directions, while TE modes propagate with single electric field in y direction. For propagation of TM and TE modes in x direction, TM modes can affect on G_θ, while TE modes change G_φ in xz-plane. This is not only valid for propagating TM and TE modes in x direction, but also for any directions parallel to the xy-plane; and if TM and TE modes are propagation in u direction ($\vec{u}$ is perpendicular to the z axis), they will affect, respectively, on G_θ and G_φ in uz-plane. Although the mentioned TM and TE modes are calculated on grounded infinite dielectric sheet, however, very similar phenomenon is occurring when a finite size thick substrate is located on large ground plane. Thus, the quasi TM and TE surface waves which are excited by the finite thick substrate on large ground plane are diffracted/reflected from the large ground plane and distort the antenna radiation pattern [54].

$$f_c\big|_{TM} = \frac{nc}{2d\sqrt{\varepsilon_r - 1}}, \qquad n = 0, 1, 2, \ldots \tag{3.1}$$

$$f_c\big|_{TE} = \frac{(2n-1)c}{4d\sqrt{\varepsilon_r - 1}}, \qquad n = 1, 2, 3, \ldots \tag{3.2}$$

Replacing ε_r = 11.9 and d = 700 μm in (3.1) and (3.2), $f_c|_{TM}$ (GHz) = n × 65 and $f_c|_{TE}$ (GHz) = (2n-1) × 32.5 are obtained. Therefore, for operating frequencies between 65 GHz to 97.5 GHz, the three modes TM_0, TE_1 and TM_1 can be excited by the 700 μm thick Si substrate. If these modes are excited, they can be reflected using the large ground plane and cause to antenna radiation pattern distortion. Although the substrate modes can be excited by thick Si substrate on small ground plane, however, they are not totally reflected by that small ground plane.

Since for the straight dipole antenna, the co-polarized dominant components in E- and H-planes are G_θ and G_ϕ, respectively, it is expected that TM and TE modes are most excited/propagated in antenna E- and H-planes, respectively. Moreover, for an infinite Si substrate (ε_r = 11.9) with thickness of 700 μm, propagation constant (β) for TM_0, TE_1 and TM_1 at 85 GHz (resonance frequency at large ground plane in Figure 3.3) are calculated as β_{TM0} = 5735.2 rad/m, β_{TE1} = 5004.9 rad/m and β_{TM1} = 1905.3 rad/m in the direction of propagation. Therefore, the equivalent ε_r for these βs can be obtained as $\varepsilon_{r|TM0}$ = 10.38, $\varepsilon_{r|TE1}$ = 7.90 and $\varepsilon_{r|TM1}$ = 1.14 using the relation $\beta = k_0\sqrt{\varepsilon_{r|eq}}$ at 85 GHz.

On the other side, the substrate modes may be excited in two ways; a) the reflected EM waves from ground plane below the etched area under the antenna can penetrate to thick Si substrate or, b) thin SiO_2 film and excite substrate modes, or c) due to the EM field below the antenna strip on the Si. If the incident wave angle is θ_i, the propagation constant of the guided wave in directions parallel to ground plane can be $\beta = k_0\sqrt{\varepsilon_r - \sin^2\theta_i}$ inside the Si and $\beta = k_0\sin\theta_i$ inside the SiO_2, which are concluded by exploiting the Snell's law in the air-Si and air-SiO_2 boundaries. Thus, the effective permittivity in the propagation direction can be calculated as $\varepsilon_{reff1} = \varepsilon_r - \sin^2\theta_i$ and $\varepsilon_{reff2} = \sin^2\theta_i$ for propagation inside the Si and SiO_2, respectively. Therefore $10.9 < \varepsilon_{reff1} < 11.9$ and $0 < \varepsilon_{reff2} < 1$ are obtained as the effective permittivity of the penetrated and propagated EM wave in the directions parallel to the ground plane. For the third case, the 100 μm width antenna arm on Si is considered as MTL and corresponding ε_{reff3} = 7.20 is calculated using (2.3).

Comparing the calculated ε_{reff1}, ε_{reff2} and ε_{reff3} with $\varepsilon_{r|TM0}$, $\varepsilon_{r|TE1}$ and $\varepsilon_{r|TM1}$, shows the high probability of all TM0 and TE1 and TM1 modes excitation by the grounded substrate and the

Table 3.1: Maximum gain coordination and values in θ direction.

G_θ	(θ, φ)	Gain (dBi)
Si and SiO_2 are available	(±61°,135°)	7
Si is removed and SiO_2 is available	(±6°,100°)	6.1
Si and SiO_2 are removed	(±13°,94°)	3.2

Table 3.2: Maximum gain coordination and values in φ direction.

G_φ	(θ, φ)	Gain (dBi)
Si and SiO_2 are available	(±33°,0°)	4.6
Si is removed and SiO_2 is available	(±33°,8°)	6.5
Si and SiO_2 are removed	(±33°,12°)	2.7

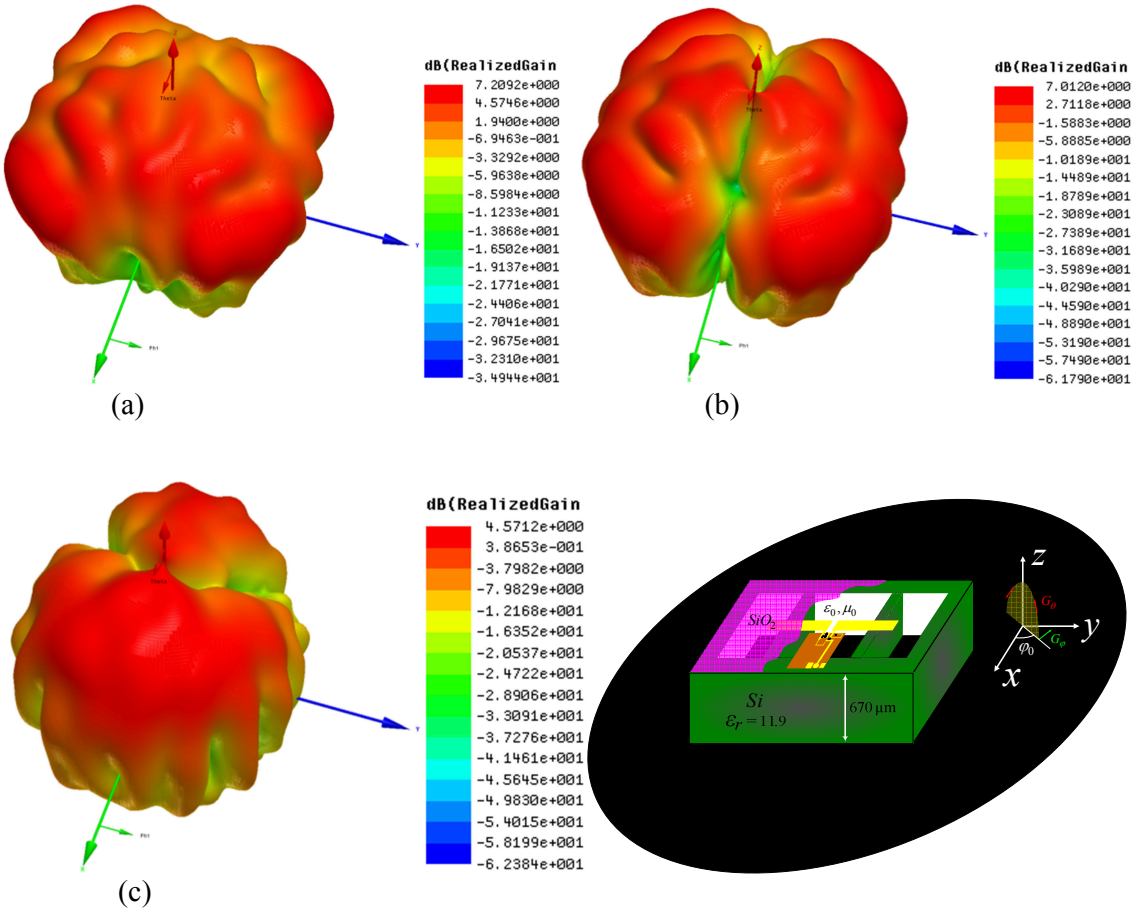


Figure 3.6: 3D realized gain of the straight dipole antenna on 20 mm × 20 mm ground plane for (a) G_{total} (b) G_θ and (c) G_ϕ at 86 GHz.

structure of straight on-chip dipole antenna.

3D simulated realized gain of the straight dipole antenna for total and isolated to θ and φ directions are shown in Figure 3.6. The half-wavelength dipole antenna gain is around 2.15 dBi which can be increased (by two times) up to 5.16 dBi as it is exposed in front of a ground plane at the distance of quarter wavelength. However, the maximum of the shown gains are more than 7 dBi due to the propagated surface waves. In the Figure 3.6 (b), TM modes cause to increase gain in θ direction (G_θ) for all planes in $0° < \varphi < 180°$. In plane $\varphi = 0°$, the co-polarized component of dipole antenna is in φ direction, that excites TE_1 mode. Therefore, the minimum of the G_θ and G_φ is in $\varphi = 0°$ and $\varphi = 90°$, respectively. The maximum and minimum positions and values for different cases are presented in Tables 3.1 and 3.2. Surface waves which are occurring from TM modes cause the maximum in $\theta = 61°$, while the maximum of TE_1 mode is in $\theta = 33°$.

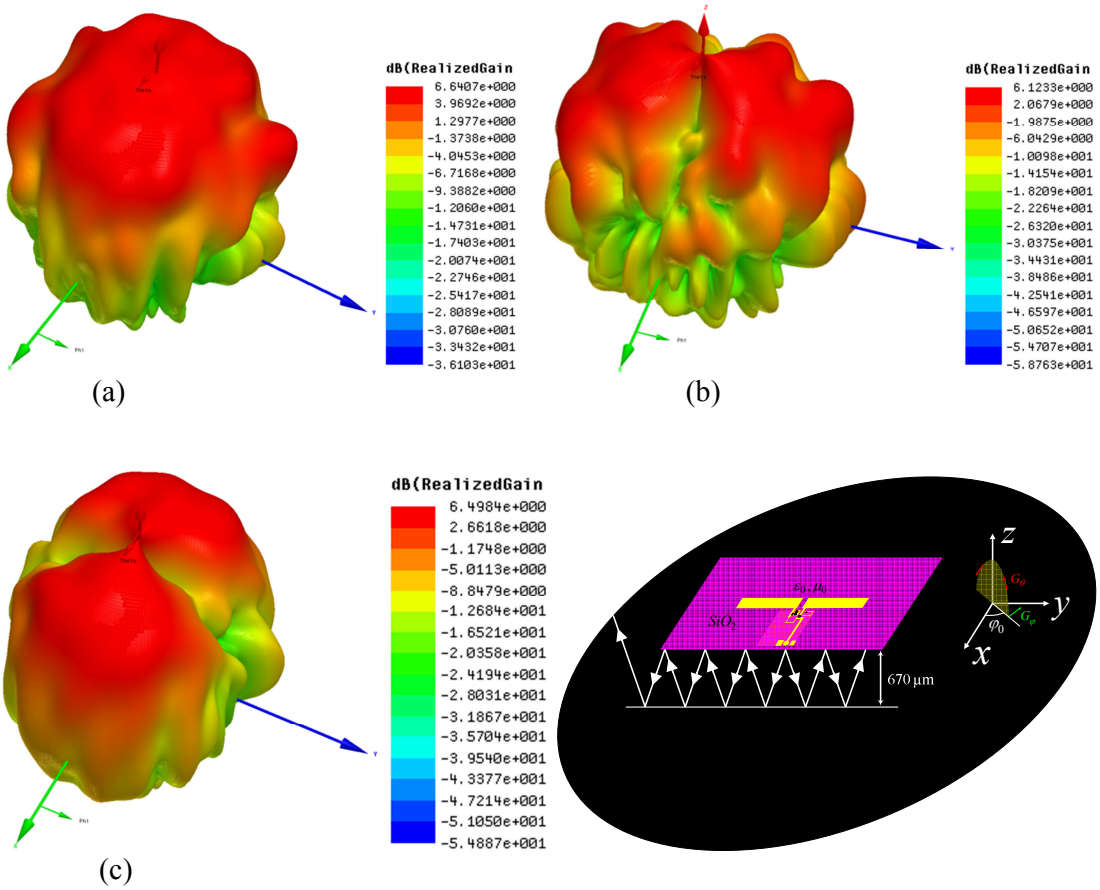


Figure 3.7: 3D realized gain of the straight dipole antenna with removed Si substrate on 20 mm × 20 mm ground plane for (a) G_{total} (b) G_θ and (c) G_ϕ at 86 GHz.

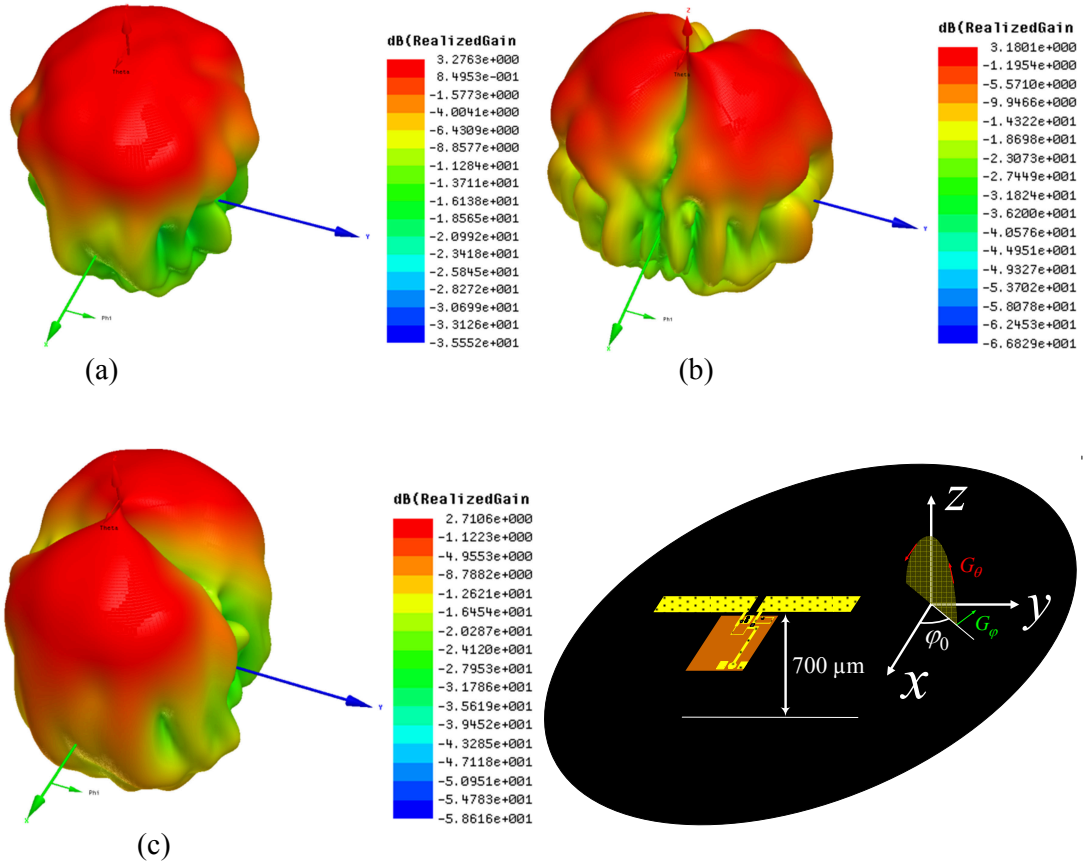


Figure 3.8: 3D realized gain of the straight dipole antenna with removed Si and SiO_2, on 20 mm × 20 mm ground plane for (a) G_{total} (b) G_θ and (c) G_ϕ at 86 GHz.

Figure 3.7 shows the simulated gains at 86 GHz for the antenna after removing the Si substrate. The 3D gain patterns show that the shape of G_θ is more close to the radiation pattern of a dipole antenna; however, the maximum gains are higher and demonstrate the surface wave excitation in absence of the thick Si substrate. Moreover, these gains are obtained while the antenna resonance frequency has shifted to higher frequency due to the removed Si.

The other important element that can have an effective role in excitation of surface waves is SiO_2 below the antenna, whereas the thick Si substrate below antenna is removed in simulations. Although the SiO_2 layer is thin, however, the reflected EM waves from ground plane are also reflected from this layer and are propagated between ground plane and SiO_2 layer. As shown in Figure 3.8, the simulated gain at 86 GHz after removing both Si and SiO_2 confirms the destructive effect of them in exciting and propagating the surface waves. The gain patterns and value show that the patterns are similar to dipole antenna patterns. Due to the suppressed surface waves, the gain of antenna falls down to maximum 3 dBi which is

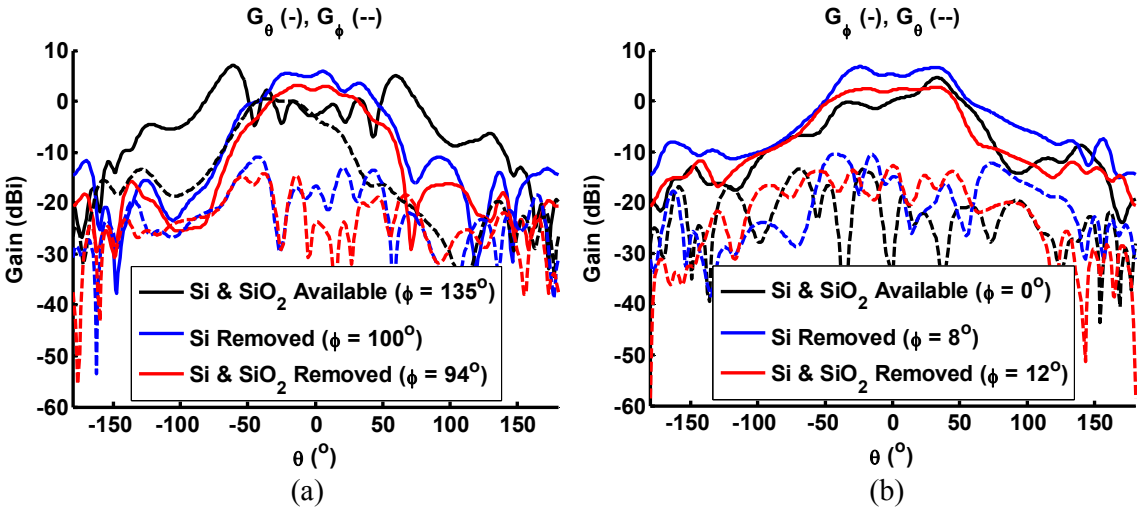


Figure 3.9: Influence of the Si and SiO_2 on (a) E- and (b) H-planes gains of the dipole antenna at 86 GHz.

smaller than 5.16 dBi. Since the antenna is operating at higher frequency than 86 GHz, its gain is lower than the expected value 5.16 dBi.

The 2D G_θ and G_φ gains on the planes that achieve their maximum and for the cases when a) Si and SiO_2 are below antenna, b) Si is removed and, c) both Si and SiO_2 are removed, are shown in Figure 3.9 (a) and (b). The maximums locations and values are also shown in Tables 3.1 and 3.2. It is expected that the G_θ and G_φ gain patterns are affected by substrate TM and TE mode on all of the planes in presence of Si and SiO_2, respectively.

The maximum values on G_θ gains are 7 dBi, 6.1 dBi and 3.2 dBi at 61°, 6° and 13° for black, blue and red curves, respectively. The maximum values of G_φ gains are 4.57 dBi, 6.48 dBi and 2.71 dBi at 33° for black, blue and red curves, respectively. Although an ideal dipole antenna gain in directions θ (G_θ) and φ (G_φ) approaches its higher value on antenna E- (φ = 90°) and H-planes (φ = 0°), respectively, however, the maximum in different cases exist in different planes due to surface waves. The radiation patterns and gains demonstrate the drastic effect of grounded thick Si substrate and also thin SiO_2 layer alone above the ground plane that cause to surface wave excitation and distorting antenna radiation pattern and performance degradation.

Furthermore, the antenna was designed to operate at 77 GHz, but the simulations show it will resonate around 86 GHz (when Si and SiO_2 are below the antenna) due to minimized chip area, embedded GSG pads after fabrication and large ground size during measurement. In the

design circumstance of straight dipole on chip antenna, the 700 μm thick Si+SiO_2 plays the role of λ/4 distance between small ground plane and antenna at 77 GHz. Therefore, the ground plane has an additive role in the antenna gain at antenna main beam direction. When the antenna resonance is changed, the λ/4 distance from ground plane becomes destructive at other frequencies than 77 GHz. In addition, removing Si and SiO_2 impose another condition on antenna performance and shift resonance frequency to higher values; and ground-antenna distance value in term of λ is also changed according to that condition. Therefore, the 3D and 2D gains and radiation patterns can only be used to show the surface wave excitations in different cases and do not contain noticeable data for discussing about the antenna patterns and gains in different cases.

3.3 Radiation Influence of the Air Coplanar Probe

There are different types of GSG probe such as Infinity probe® and Air Coplanar probe (ACP) which are used for coplanar pads measurements. Input of both probes is terminated by coaxial port while their output (tip) is designed to feed coplanar waveguide (CPW) type TL. Thus, the transition from coaxial to CPW is performed near the probe tips.

In Infinity probes, the transition is performed using a MTL. In this probe, the MTL line and ground are connected to inner cylinder and outer body of the coax, respectively. Moreover, the ground tips are connected to microstrip ground using vias to have signal and ground tips at the same plane. Since the microstrip ground on the device under test (DUT) acts as a shielding, hence no EM field is radiated out of the Infinity probe around the transition portion and a 50 Ω TL impedance can be guaranteed right to the probe tips (see Figure 3.10 (a)).

In ACP probes, the air coplanar waveguide is connected to the coax to transit the signal to

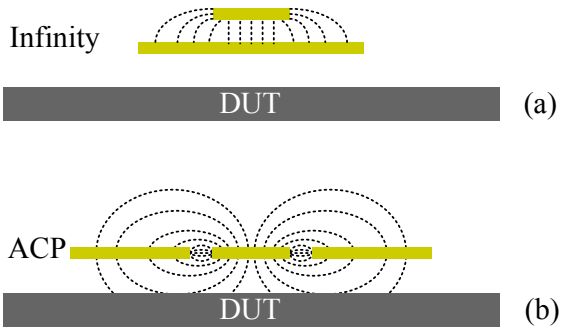
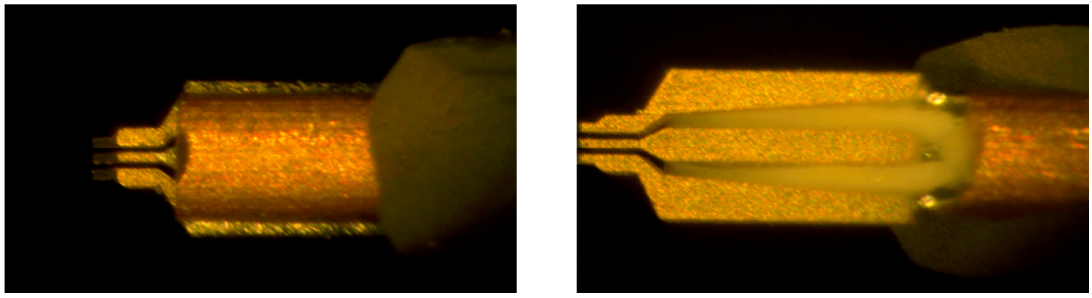


Figure 3.10: (a) Infinity probe versus (b) ACP probe tip



(a) (b)

Figure 3.11: (a) Top and (b) bottom micrographic pictures of the ACP110-A-GSG-100 probe.

the probe tips. In this probe the EM field can radiate and couple with the devices nearby the probe tip (see Figure 3.10 (b)). Top and bottom view of the ACP110-A-GSG-100 probe are shown in Figure 3.11. The radiated EM field can also be reflected back to the probe from the materials and especially metals below the probe tip. Therefore, the EM field distribution inside the ACP probe can be affected (the unwanted transmission modes are excited) not only by terminating the probe tip with an impedance, but also the reflected EM waves from the probe surrounding. Moreover, the material (and different surrounding) around the GSG pads, that the ACP probe lands on, (especially bellow the probe tip) can differ in each DUT, and hence no unique calibration can be meaningful for all measurements. The effect of ACP probe radiation on scattering parameters measurement can be alleviated if same measurement and calibration conditions are created below the probe tip. These conditions, which can reduce the effect of reflected EM waves, can include the use of same board for both measurement and calibration, removing extra metals below the probe tip, increasing the spacing between two DUT on the same board or dicing. In addition, exploiting the ACP probes for no ground plane measurements can increasingly improve scattering parameters measurement.

As mentioned, manufacturing the calibration kit on the material/board that is used for DUT can be considered as a remedy to increase the accuracy of the measured S-parameters that are performed by ACP probes. However, it can be hard or impossible for some cases such as on-chip design. Implementing the 50-ohm load and short on the chip with precise tolerances can be difficult and causes parasitic inductance. In addition, most of the chips are diced near the GSG pads and thus no parts of the chip is left below the probe; consequently, this condition is required to be considered in all standards of calibration on the kit. All the aforementioned problems can cause to exploit impedance standard substrate (ISS) calibration

kit for chip measurement. Consequently, the discrepancy between simulation and measurement can arise in the case of employing the ACP probe in measurement of S-parameters. The effect of ACP probe tip in measurement of antenna reflection coefficient is described here in detail.

Another important part of all types of probes that can have significant effect on the radiation pattern of antennas is the head of probes. Usually, the antenna radiation pattern can be seriously affected on the plane which is perpendicular to the measuring surface and parallel to the probe needle. Moreover, the radiation pattern distortion can increase when the angle of view is increased with respect to the antenna top, as the angle reference. Influence of the probe head on radiation pattern distortion is investigated in [71].

3.3.1 ACP 110-A-GSG-100 Probe Model

A physical examination of the ACP probe shows that the fringing field can couple with the surrounding structures and causes to uncertainty in measurements. To demonstrate the discrepancies between the measurement (performed by ACP probe) and simulation result and show the significant effect of the ACP probe, the coax to air coplanar waveguide transition part (shown part in Figure 3.11) of the ACP110-A-GSG-100 probe is analyzed using the HFSS. All mechanical dimensions of the probe, such as the coax diameter, air coplanar waveguide TL length, and widths and gap spacings at different points of coplanar waveguide, are approximated with good precision using an electron microscope. The 3D schematic of the ACP probe as it feeds the straight dipole antenna and the dimensions of the probe used in simulation to model the ACP probe, are shown in Figure 3.12. Inner and outer diameters of the probe are approximated as 100 μm and 610 μm, respectively. Permittivity of the material that fills the coax can be calculated as [54]

$$\varepsilon_r = \left(\frac{60}{Z_o} \ln(\frac{d_{out}}{d_{in}}) \right)^2 \tag{3.3}$$

where Z_o is the characteristic impedance of the transmission line and d_{out} and d_{in} are the diameters of the outer and inner conductors, respectively. For the approximated diameters and 50 Ω TL, $\varepsilon_r = 4.71$ is obtained.

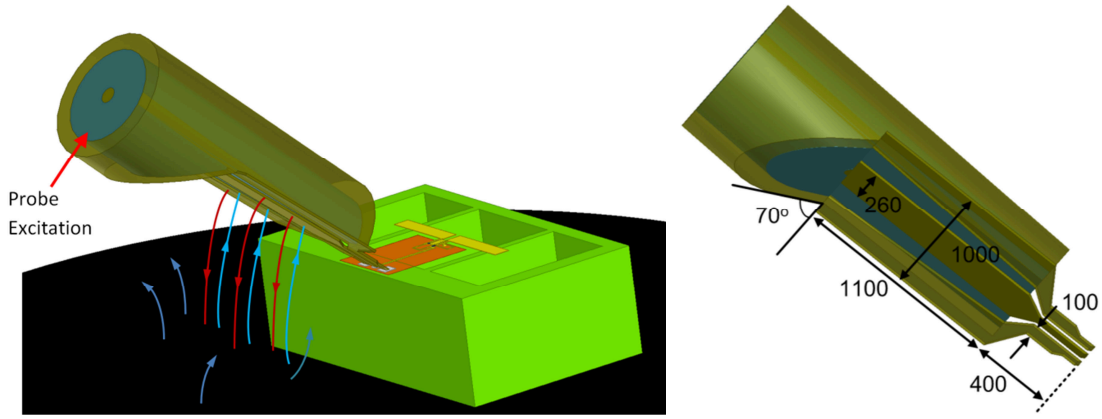


Figure 3.12: the probe-fed model of dipole antenna and its open part geometry with measured dimensions.

The return loss of the ACP probe model is calculated by exciting the probe from the coaxial side in HFSS and terminating its tips with three different loads: 50 Ω load (two 100 Ω loads between S (signal) and G (ground) tips on calibration kit model), short circuit (probe tips are connected with a metal line on calibration kit model) and open circuit (tips of the probe are standing in the air). The calibration kit material is Alumina substrate with a thickness of 254 μm and a dielectric constant of 9.9. Probe insertion loss is calculated between two ports: one port from the coax side, and the other port on the calibration kit. Resulting S parameters from the simulations for different loads at W band frequency are displayed in Figure 3.13. Return loss for 50 Ω termination varies between 6.5 and 8.3 dB from 75 to 110 GHz frequencies, which shows poor matching for the approximated probe model. The simulated realized gain of the ACP probe as it is terminated by 50 Ω at its tip on

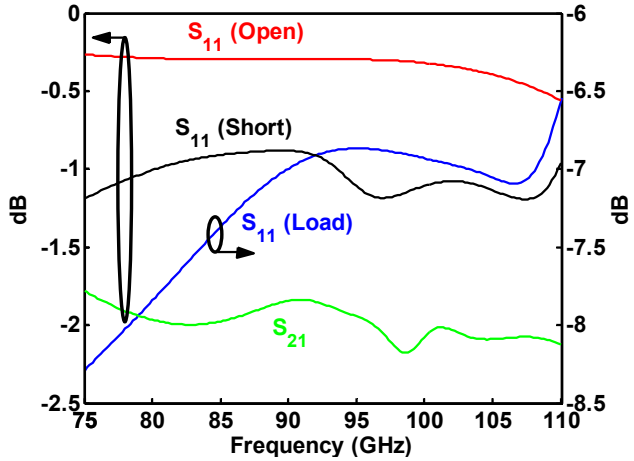


Figure 3.13: S-parameters at the coax side of the modeled ACP probe terminated by open, short and 50 Ω load at its tip.

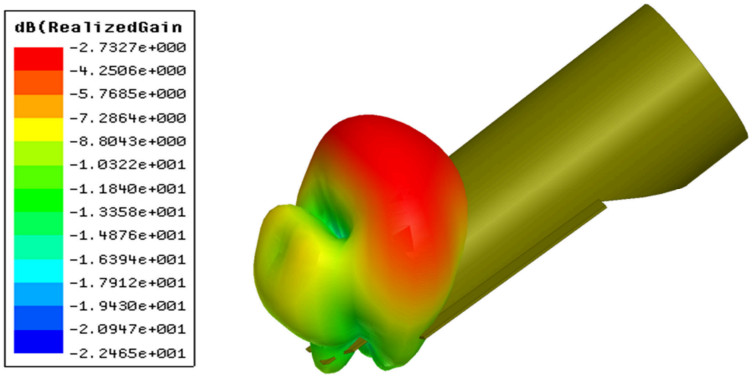


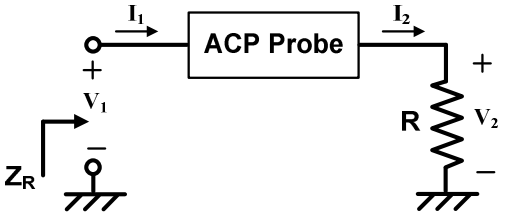
Figure 3.14: 3D realized gain for the modeled probe terminated by 50 Ω load.

the calibration kit is shown in Figure 3.14. The gain pattern in Figure 3.14 shows the reflected power from the ground plane with a minimum power loss of 2.73 dB when the probe is matched at its tips (the probe has 2 dB insertion loss as seen from S_{21} in Figure 3.13). These results hint that the leaked wave from the ACP probe can couple with the devices nearby the probe tip and excite it without any contact, and/or reflect back from ground plane.

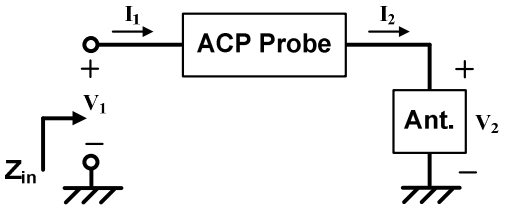
3.3.2 ACP Probe De-embedding

The radiation of ACP probe tip and reflections from its surroundings varies in different DUTs and measurement, and hence this effect cannot be de-embedded from measurements to specify the real performance of DUT. Accordingly, we propose to model the ACP probe tip as it feeds the DUT (as shown in Figure 3.12) and insert the coupling effect of the ACP probe tip in the simulation by putting an excitation port at coax side of the probe model. Then, de-embed the ACP probe circuit with respect to SOL (short, open and load) calibration standard to obtain the antenna reflection coefficient which is equivalent with the measurement result. This method is similar to what is performed in vector network analyzer (VNA) to measure S_{11} after its single port calibration.

Therefore, the *ABCD* matrix of the ACP probe circuit is calculated by putting a port at coax side of probe model (to gain Z_R) and replacing the resistance R, shown in Figure 3.15 (a), by short, open and 50 Ω load. Then, this *ABCD* matrix is used in Figure 3.15 (b) to de-embed the probe circuit from Z_{in} (seen impedance in probe-fed simulation) to obtain the input impedance of the antenna. Figure 3.15 shows the circuit model of the ACP probe excited from coax side and (a) terminated with a load, R, on calibration kit and (b) feeding the antenna for full wave simulations. The ABCD matrix for ACP probe in Figure 3.15 is defined



(a)



(b)

Figure 3.15: Network model of the ACP probe as it is terminated by (a) a load R and (b) feeds an antenna.

as,

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \tag{3.4}$$

Here, three equations that are obtained by replacing R, in Figure 3.15 (a), with zero (short), infinity (open) and 50 Ω (load), are utilized to reduce the four unknowns of the *ABCD* matrix to one, and use it to calculate antenna impedance in Figure 3.15 (b).

As shown in Figure 3.15 (a), the input impedance Z_R, is derived by dividing input voltage V_1 by its current I_1 for a specified load R at the output.

For short circuit ($V_2 = 0$), open circuit ($I_2 = 0$) and 50-ohm load ($V_2/I_2 = 50\ \Omega$) at output in Figure 3.15 (a), the input impedances are calculated in (3.5), (3.6) and (3.7), respectively.

$$Z_{short} = \frac{B}{D} \tag{3.5}$$

$$Z_{open} = \frac{A}{C} \tag{3.6}$$

$$Z_{load} = \frac{50A + B}{50C + D} \tag{3.7}$$

Using (3.5) and (3.6) in (3.7) to cancel out *A* and *B* parameters, (3.7) is modified to (3.8) and subsequently to (3.9) as

$$Z_{load} = \frac{50CZ_{oc} + DZ_{sc}}{50C + D} \tag{3.8}$$

$$\frac{D}{C} = -50\frac{Z_{load} - Z_{open}}{Z_{load} - Z_{short}} \tag{3.9}$$

The goal of these calculations is to de-embed the probe and find the input impedance of the antenna (Z_{ant}) in Figure 3.15 (b). Modifying (3.4) by replacing $Z_{in}=V_1/I_1$ and $Z_{ant}=V_2/I_2$ in the circuit of Figure 3.15 (b)

$$Z_{in} = \frac{AZ_{ant} + B}{CZ_{ant} + D} \tag{3.10}$$

Inserting A and B from (3.5) and (3.6), we conclude Z_{ant} depends on D/C in (3.11).

Note that the A, B, C and D parameters are the same as in the probe network for both circuits in Figure 3.15.

$$Z_{ant} = -\frac{D}{C}\frac{Z_{in} - Z_{short}}{Z_{in} - Z_{open}} \tag{3.11}$$

D/C ratio in (3.11) is replaced by (3.9) and input impedance of the antenna Z_{ant}, which is independent of probe network parameters, is calculated in probe de-embedding relation, (3.12). Z_{ant} in (3.12) is in terms of Z_{in} (simulated input impedance from coax edge of ACP probe feeding the antenna) along with Z_{short} , Z_{open} and Z_{load} (simulated input impedance at coax edge of the ACP probe as it is calibrated on kit model for SOL standard).

$$Z_{ant} = 50\frac{Z_{load} - Z_{open}}{Z_{load} - Z_{short}}\frac{Z_{in} - Z_{short}}{Z_{in} - Z_{open}} \tag{3.12}$$

To compare the simulated results with the measured data, antenna reflection coefficient is derived using the following relation.

$$\left|S_{11}\right|(\text{dB}) = 20\log\left|\frac{Z_{ant} - 50}{Z_{ant} + 50}\right| \tag{3.13}$$

In this technique, the effect of ACP probe is inserted in simulation and its circuit is de-embedded with respect to performed calibration. Note that, we follow the same operation that is performed practically. If the probe circuit is the same at the time of calibration and at the

time of measurement, the de-embedding relation will not be necessary. Furthermore, the reason of discrepancies between the probe-fed and non-probe simulations is the change of ACP probe circuit in different situations which comes from the ACP probe coupling with its surrounding.

3.4 Set-up for On-Chip Measurements

The schematic of W band antenna measurement setup is shown in Figure 3.16. A 25 dBi horn antenna is used as the probe antenna and can rotate between ±60° in *yz*-plane. The horn antenna has a narrow beam width to confine most of the radiated power to the chip structure. As shown in Figure 3.16, the GSG probe is manually rotated by 90° to measure the antenna radiation pattern in E- and H-planes. Frequency of the VNA (working up to 50 GHz) is increased to W band using VDI Harmonic WR10 extenders. As shown in Figure 3.17, the manual (using handle) turning table is used to change the incidence angle of the horn antenna.

3.5 Measurements and Post Measurement Simulations Results for 77 GHz Antennas

The manufactured antennas are measured for reflection coefficient, radiation pattern and gain at W band using the shown measurement setup in Figures 3.16 and 3.17. The antennas are modeled and simulated very similar to the measurement circumstance (GSG pads and large ground plane) and with the manufactured dimensions. The ACP probe effect is inserted

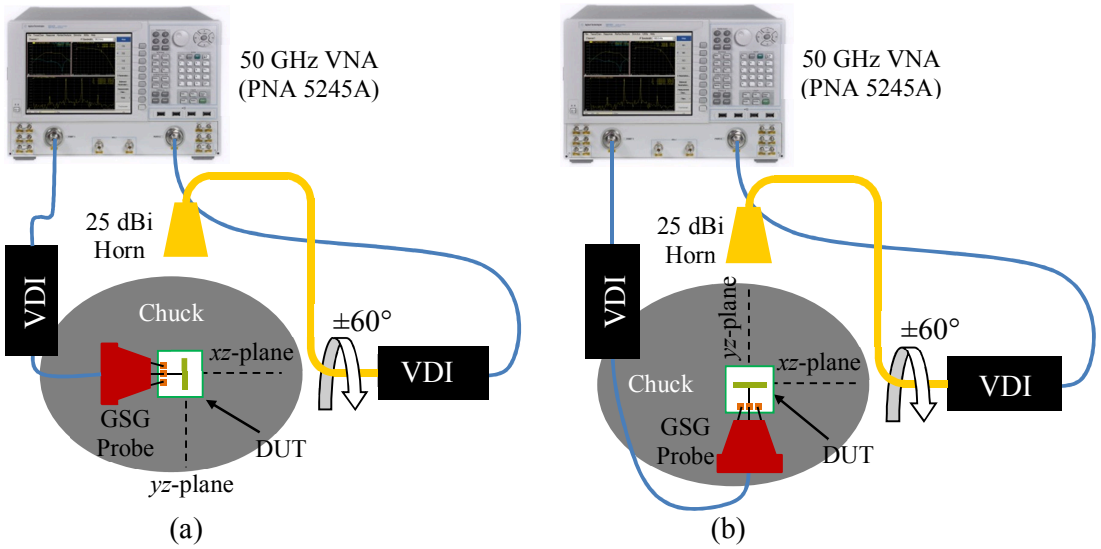


Figure 3.16: Schematic of the antenna radiation pattern measurement in (a) E-plane and (b) H-plane.

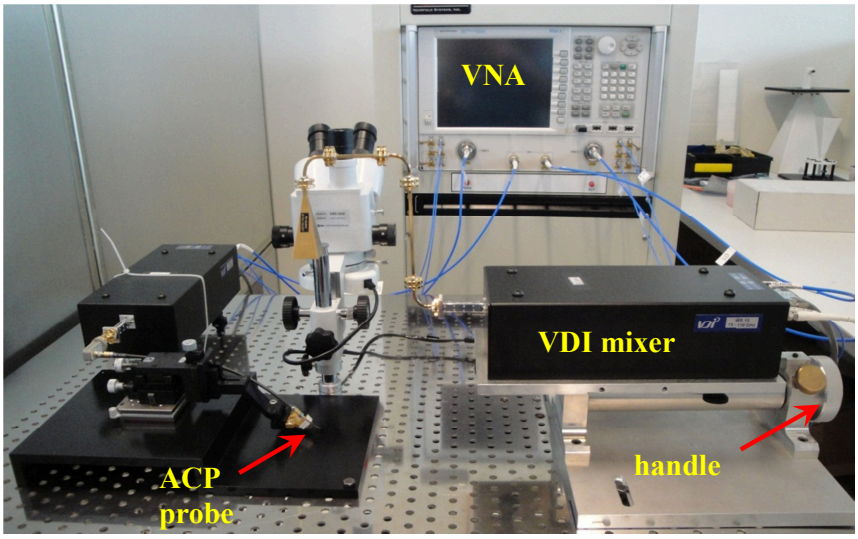


Figure 3.17: Set-up for W band on-chip measurement.

to simulation and its circuit is de-embedding using the obtained de-embedding relation. The measurement and post measurement simulations with and without ACP probe model are compared for fabricated on-chip straight, L-shaped and T-shaped dipole antennas.

3.5.1 Straight Dipole Antenna

The manufactured on-chip microstrip dipole antenna with dimensions 2.2 mm × 1.3 mm is shown in Figure 18. The antenna is manufactured on thick (670 μm) Si substrate and thin (11.4 μm) film of SiO_2. The three etched areas in Si substrate are shown in the chip microphotograph. As shown in Figure 3.18, two walls of Si are left beneath the antenna to prevent the SiO_2 from breakage. The manufactured antenna length is 1040 μm. And the LC balun dimensions are measured as 210 μm × 200 μm.

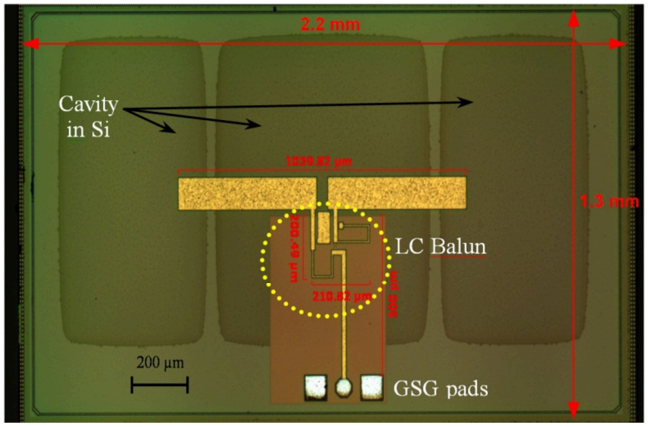


Figure 3.18: Micrographic picture of the manufactured on-chip straight dipole antenna.

3.5.1.1 Straight Dipole Antenna Reflection Coefficient

To show the effect of Infinity and ACP probes on the antenna reflection coefficient and compare with the simulated results, corresponding curves are displayed in Figure 3.19. As shown in Figure 3.19, the antenna was measured for S_{11} when it was on wafer and after dicing by using the Infinity probes®. When these curves with colors blue and brown are compared with the simulated antenna S_{11} (the dashed black curve without probe model), show the antenna resonance at frequencies which are very close in those curves (around 84 GHz). Also, these curves are in good agreement for frequencies below 100 GHz. On-wafer measurement has acceptable performance since it has been done with Infinity probe. However, it is expected that during on-wafer measurement, there are other devices around the measured antenna, and these devices interfere in antenna's near field, and consequently change the measured S_{11}.

The third measurement is performed using ACP probe, shown with green curve, which is different than previous measurements and antenna simulation (dashed black curve). Although the measurement is realized on single antenna (after dicing from wafer), however, the radiation of ACP probe and its coupling with its surround cause to uncertainty on the measured S_{11}. To show the ACP probe effect, its model is used in the simulation, as it was displayed in Figure 3.12, and obtained Z_{in} is inserted into probe de-embedding relation, (3.12), to de-embed the probe circuit and calculate the input impedance of the antenna as, Z_{ant}. The calculated S_{11} magnitude using (3.13), is shown with purple curve in Figure 3.19. This curve and the ACP measured one present very similar performance, and demonstrate the ACP probe effect.

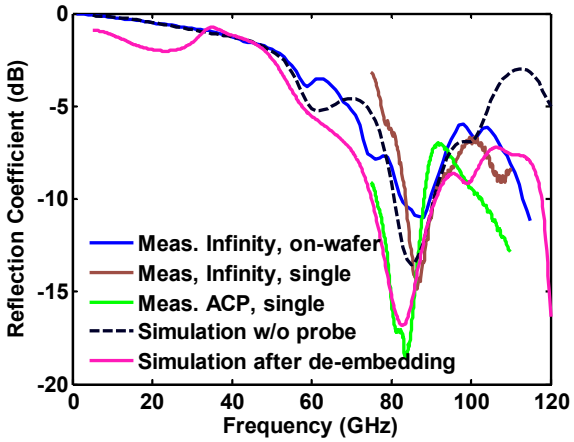


Figure 3.19: Antenna reflection coefficient for different on-wafer and single measurements using Infinity and ACP probes and simulations without probe and with ACP probe effect.

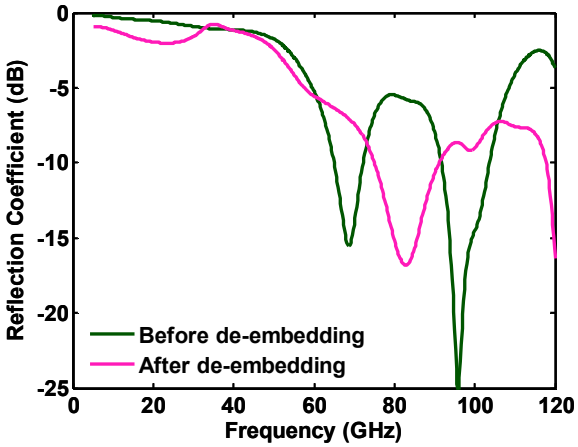


Figure 3.20: Antenna reflection coefficient results for probe-fed simulation (before and after ACP probe circuit de-embedding).

The reflection coefficient of the probe-fed model simulation before (can be calculated by replacing Z_{in} by Z_{ant} in (2)) and after probe circuit de-embedding are shown in Figure 3.20. This figure shows that de-embedding can completely change the shape of the simulated S_{11} which is seen from the coax edge.

Although the antenna was designed to be operated at 77 GHz, the simulations and measurements show resonances around 84 GHz. This frequency shift is attributed to the removed Si around the antenna in fabrication (4 mm × 3 mm designed dimensions are reduced to 2 mm × 1mm) and the GSG pads. Since the antenna will be used at the front end of automotive radar and is connected directly to other components, the GSG pads model was not considered in the design process. However, the pads are inserted to feed and measure the antenna.

3.5.1.2 Straight Dipole Antenna Radiation Pattern and Gain

In Figure 3.21, measured and simulated E- and H-plane (*xz*-plane in Figure 2.7) radiation patterns which are normalized to their maximum values are shown for 85 GHz. The antenna is fed using Infinity probe. E-plane radiation patterns (red and black curves) are wider than the H-plane radiation patterns (green and blue curves). For the E-plane, there are two side lobes due to the effect of the surface wave at 60°. Gain at these side lobes is 3 dB larger than the gain at $\theta = 0^{\circ}$. The H-plane radiation pattern is more directive than the E-plane pattern. For wide angle range around 0º, the measured E-plane radiation pattern is well matched with the simulated result. Measured and simulated gain at $\theta = 0^{\circ}$ versus frequency is depicted for the

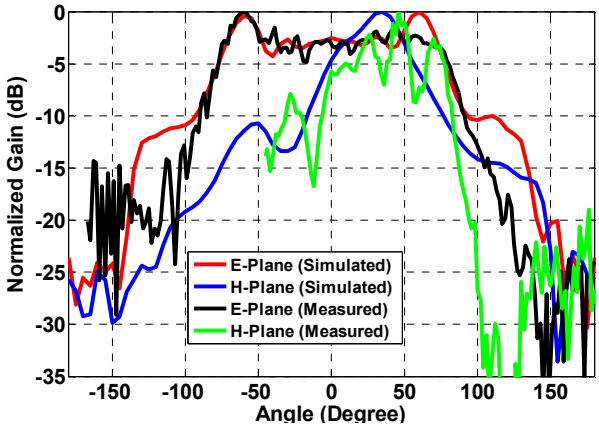


Figure 3.21: Simulated and measured radiation pattern for E and H-plane at 77 GHz.

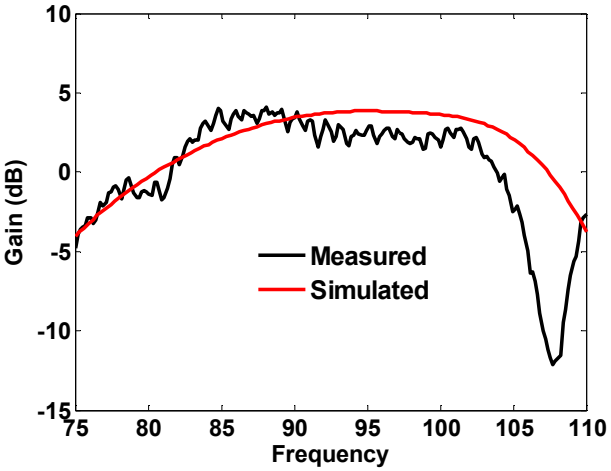


Figure 3.22: Measured and simulated antenna maximum gain in E-plane.

W band in Figure 3.22. Around the operation frequency, the measured and simulated results are in good agreement. Since the antenna is matched better in the band 85 GHz to 90 GHz higher gain is obtained at θ = 0º in this band (85-90 GHz). Maximum gain of 4.1 dBi at frequencies 84.8 GHz and 88 GHz is achieved. Measured antenna maximum gain (around θ = 57º) for 77 GHz and 85 GHz are -1.9 dBi and 4 dBi, respectively. Note that a free space dipole has 2.15 dBi gain, which can increase to 5.16 dBi as it is placed above a ground plane.

3.5.2 L- and T-Shaped Dipole Antennas

Although the L and T antennas are designed separately, however, they are located next to each other in a single chip in the manufactured versions (see Figure 3.23). As shown in Figure 3.23, some parameters such as the width of the chip and cavity size and shape (super ellipses instead of rectangles) are changed during the fabrication process. Micrographic length

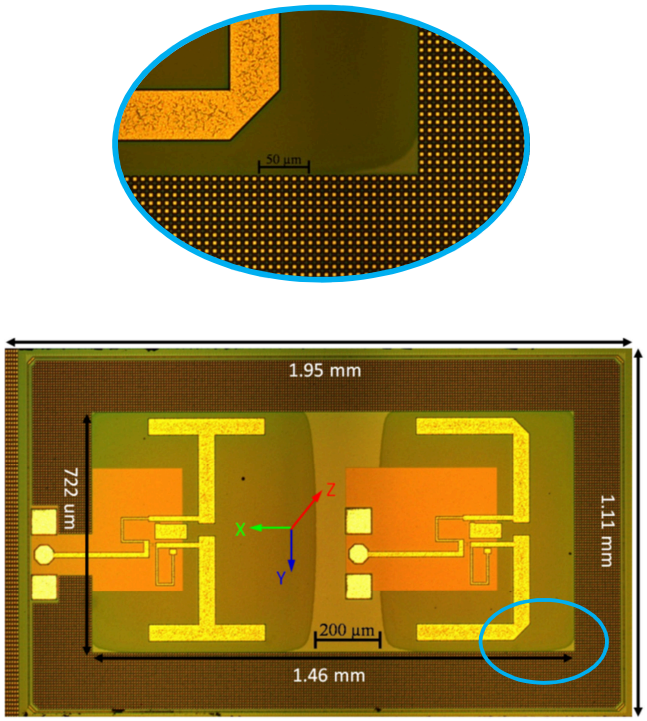


Figure 3.23: Micrographic picture of the manufactured L and T antennas inside a chip monolithically with magnified small metal cells at chip margins.

measurement of the manufactured chip demonstrates the chip width increases to 1.11 mm (was 900 μm) and center-to-center cavity size of the L and T antennas are changed to 650 μm × 820 μm (designed 470 μm × 700 μm) and 630 μm × 820 μm (designed 600 μm × 700 μm), respectively, after fabrication. However, other dimensions have very small tolerance of about 2-3 μm. Another interesting aspect of the fabricated chip is the metal particles surrounding the antennas, which are used for increasing the mechanical strength and the metal density of the BEOL (Back end of line) process. Magnified micrographic picture of these metal particles around the antenna as clear small rectangular pieces is displayed in Figure 3.23. These small metal cells around the antennas in are separated by 4 μm thick slits.

3.5.2.1 L- and T-Shaped Antennas Reflection Coefficients

As shown in Figure 3.24, when the L antenna next to the T antenna is fed by ACP probe, the EM field leakages from the bottom part of the ACP probe excite the T antenna and are also reflected back from the conductor platform and metal cells around the probe. This coupling cause to modify the EM fields inside the probe. Thus, the measured S_{11} in VNA, for L antenna, will be the received power resulting from both L and T antennas plus metallic

reflections. Moreover, the distance between the probe radiating part and the T antenna is smaller than 400 μm (< λ/10 @ 75 GHz).

Depending on probe position, the chip shape or location of the GSG pads on the chip, the probe can cause errors in the calibration of VNA because of the mentioned reflections and changing field distribution on the ACP probe.

Figure 3.25 shows reflection coefficients of L and T antennas for measured (black graph), simulated with lumped port (red graphs), and ACP probe model with (solid blue graph) and without (dashed blue graph) de-embedding. The simulation results with ACP probe (after de-embedding) are very interesting and reasonably close to the measured results, which clear the drastic effect of the ACP probe in the simulations data. The small metal pieces around antennas (Figure 3.23) are modeled as single metal in simulations whereas they are not physically connected in manufactured antennas. Other conditions, such as the exact permittivity of silicon substrate, capacitors' value after fabrication and approximate ACP probe geometry model can make some difference between simulation and measurement.

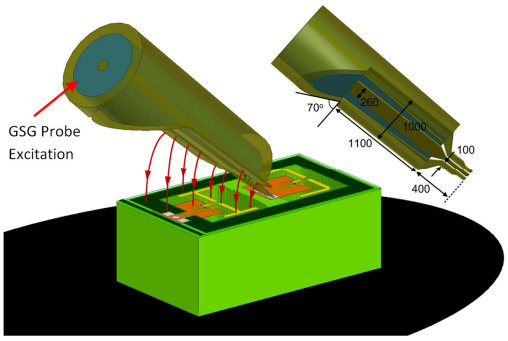


Figure 3.24: 3D schematic of the probe-fed L antenna next to the T antenna.

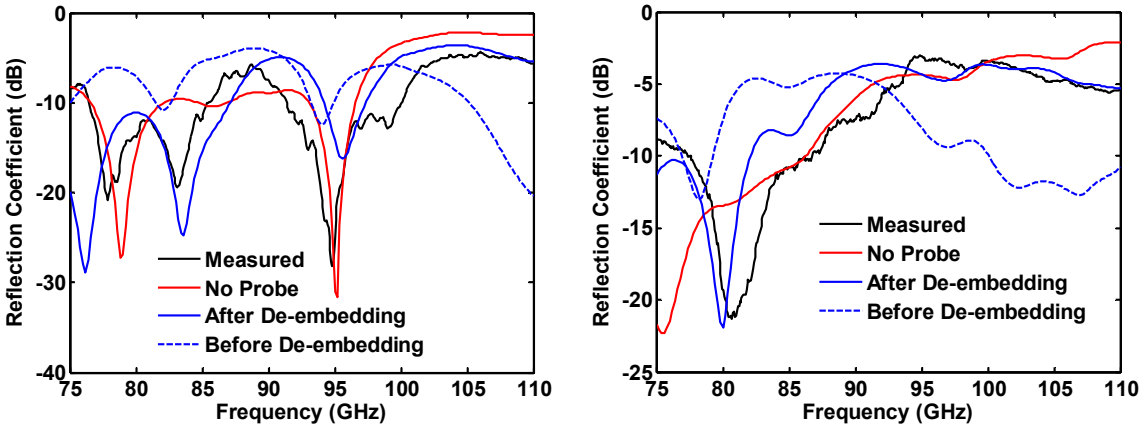


Figure 3.25: Reflection coefficient for (a) L and (b) T antennas before dicing.

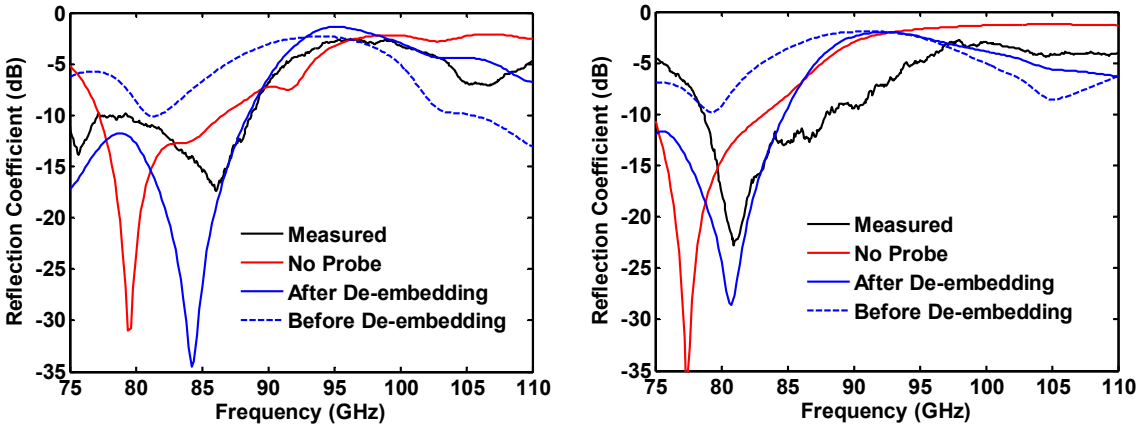


Figure 3.26: Reflection coefficient for (a) L and (b) T antennas after dicing.

The L antenna result with label After De-embedding in Figure 3.25 is complicated and has many nulls, while T antenna is much simpler since there is no additional antenna below the probe. Differences between measurements and simulations confirm the effect of probe on antenna performance when there is different substrate/environment under the probe.

Measurements and simulations for isolated L and T antennas (after dicing) are displayed in Figure 3.26 (a) and (b), respectively. The implemented antennas are simulated with the real dimensions of the structures, which are measured after the dicing of the chip. The measured performance of the antennas is very close to the simulations when the ACP probe model is taken into account and de-embedded in simulations (blue solid curves). These results for diced chip show that the ACP probe shifts the resonance frequency around 5 GHz to higher frequencies (in comparison with lumped port excitation). Since probe-fed measurement and simulation data (After De-embedding labels in Figure 3.26) present similar performances, it can be deduced that this is the effect of the probe and the manufactured antennas will show their real performance similar to lumped port (red) plots if the probe were to be ideal or shielded up to its tips. In fact, with no obstacle around the antennas, the L and T antennas will operate at 80 GHz and 77 GHz, respectively, as they are fed right from the edge of the GSG pads. However, the L antenna resonance shifts by 3 GHz because of the increased length of the etched area in fabrication (650 μm instead of 470 μm).

The measurement and the calibration will be more consistent when the height and properties of the calibration kit and chip are the same. Also, avoiding conductor platforms can improve the measurement results.

The L antenna measurement next to T antenna presents three nulls at 78, 83 and 95 GHz frequencies (Figure 3.25 (a)) that are disappeared after dicing. These results reveal the role of the ACP probe as it is utilized in complicated environment.

3.5.2.2 L- and T-Shaped Antennas Radiation Patterns and Gains

The radiation patterns for isolated L and T antennas are measured on E-plane (*yz*-plane in Figure 3.23) and H-plane (*xz*-plane in Figure 3.23) for co- (y direction) and cross- (x direction) polarization at 77 GHz frequency as shown in Figures 3.27 and 3.28, respectively. Measured and simulated radiation patterns are compared with and without the ACP probe in simulations and it is seen that probe-fed measurements and simulations for radiation patterns are very similar. Furthermore, the effect of the ACP probe in distorting the radiation patterns is illustrated in simulation. The nulls around $\theta = 0°$ in co-polarization pattern of L antenna, in Figure 3.27, are the result of ACP probe and margin metal cells in front of the L antenna. When the chip in Figure 3.23 is diced into L and T antennas, the margin metal cells in front of L antenna are left, which are not there in front of the isolated T antenna. These small metal cells are modeled as connected metal bars (colorful green metals in Figure 3.24) around the antenna in simulations. This metal bar in front of the L antenna is parallel to co-polarized E-field and causes a null around $\theta = 0°$ in presence of the ACP probe (co-polarized E-field can be reflected from probe), which is not seen in Figure 3.28 for T antenna.

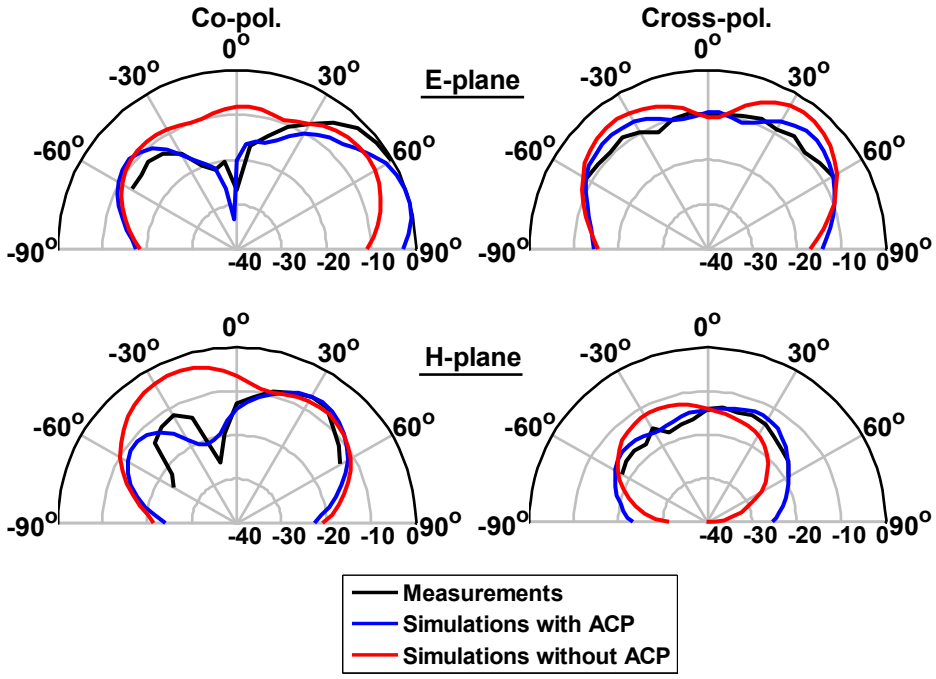


Figure 3.27: Co- and cross-pol. radiation patterns for L antenna on E/H-plane at 77 GHz.

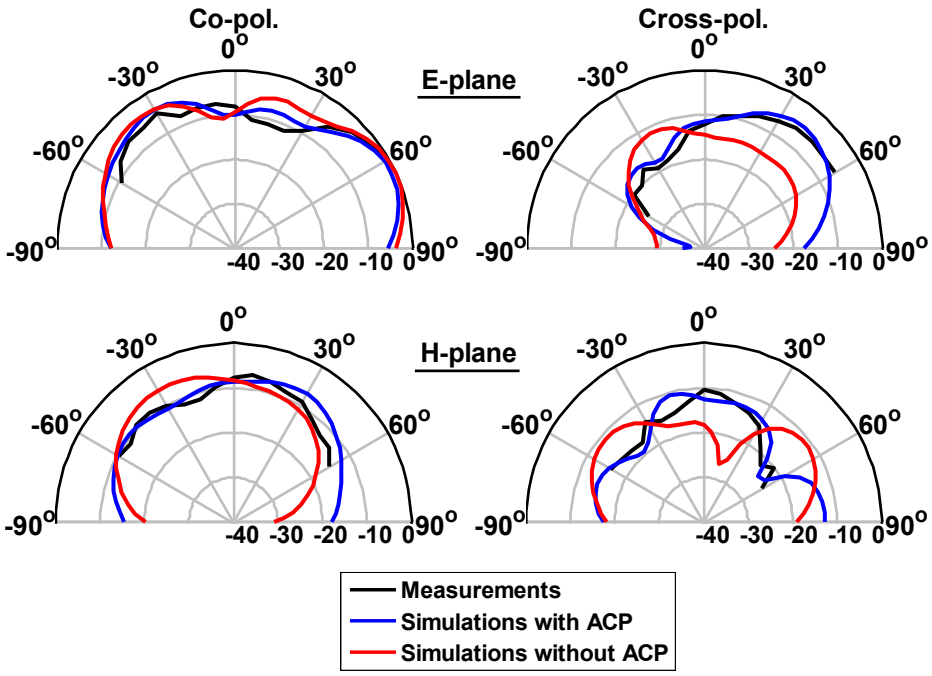


Figure 3.28: Co- and cross-pol. radiation patterns for T antenna on E/H-plane at 77 GHz.

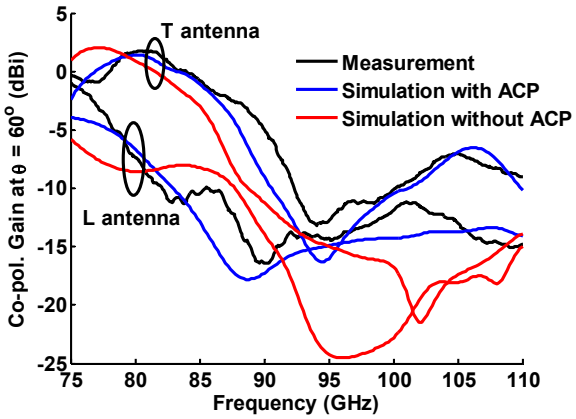


Figure 3.29: Measured and simulated co-pol. gains on E-plane at $\theta = 60^{o}$.

The simulations show that antenna (with chip dimensions 1 × 1.1 mm^2 and 1.1 × 1.1 mm^2 for L and T antennas, respectively) and radiated field from the bottom of the probe excite the surface waves in thick substrate (700 μm) and cause the side lobes level to increase around θ = ±30° and 60° on E- and H-planes. All the simulations are performed in a confined 16 mm × 16 mm (> 4 λ × 4 λ @ 75-110 GHz) PEC plane to model a large ground plane.

Regarding our design (Figure 2.21), simulations and logic about two parallel and opposite directed current distributions would lead us to expect higher gain in co-polarization on E- and H-planes for both the L and T antennas, but this is not evident in Figures 3.27 and 3.28. The

antenna radiated power is totally distorted by varying the ground plane size, dimension/location of the etched area, margin metal cells around the diced chip and ACP probe leakage and its metal body.

The co-polarized gains of the antennas are measured at $\theta = 60^o$ (maximum gain on E-plane) versus frequency as shown in Figure 3.29. The gains are calculated using gain comparison technique with respect to a 10 dBi standard gain horn antenna. Maximum values of the measured and simulated gains on E-plane are below 2 dBi and agree well for the probe-fed case. However, simulated realized gain and efficiency at 77 GHz for probe-fed, without probe, without probe and margin metal bars are given in Tables I and II for L and T antennas, respectively.

The effect of the probe on the gain and efficiency of the L antenna is more significant due to presence of metal bar in front of the antenna. Radiation efficiency can be calculated using average gain method for measurements that are performed for limited number of angles on E- and H-planes; these calculations will result in lower/inaccurate values, because of lower gain at the measured planes.

3.6 Measurements and Post Measurement Simulations Results for 94 GHz Antennas

The L and T antennas for 94 GHz are measured and simulated as they are next to each other. The influence of the ACP probe is considered and de-embedded in these antennas, too.

Table 3.3: Simulated Realized Gain and Efficiency for L Antenna

Simulations	Peak Realized Gain (θ, φ)	Peak Realized Gain (dBi)	Eff. %
Probe-fed, Margin Metals	($\pm 55^o$, 130^o)	4.60	59
No Probe, Margin Metals	($\pm 45^o$, 110^o)	2.44	31
No Probe, No Margin Metals	($\pm 45^o$, 90^o)	5.33	73

Table 3.4: Simulated Realized Gain and Efficiency for T Antenna

Simulations	Peak Realized Gain (θ, φ)	Peak Realized Gain (dBi)	Eff. %
Probe-fed, Margin Metals	($\pm 45^o$, 60^o)	3.70	53
No Probe, Margin Metals	($\pm 45^o$, 40^o)	3.99	49
No Probe, No Margin Metals	($\pm 50^o$, 90^o)	5.21	72

3.6.1 Manufactured L- and T-Shaped Antennas

The fabricated L and T antennas for 94 GHz are located next to each other, as shown in Figure 3.30. The chip dimensions are 1.9 mm × 780 μm. These antennas are located back to back, unlike the L and T chip for 77 GHz. Back to back position of the antenna can have an advantage in measurements performed using ACP probe. When one of the antennas is probed, the other one is far from the ACP open part that causes to alleviate the effect of ACP probe. The other important part is the unavailability of small metal particle around the antennas. Therefore, it is expected to have better reflection coefficient measurement by ACP probe in this chip versus the fabricated L and T chip for 77 GHz.

3.6.1.1 L- and T-Shaped Antennas Reflection Coefficients

The antennas are simulated and measured for reflection coefficient as they are located next to each other (Figure 3.30). The reflection coefficients for antennas are shown in Figure 3.31. The results of probe de-embedding are closer to the measurements results. The nulls at 80 GHz for the simulated results with ACP model are arising from the complicated surrounding around the probe and modeling only its tip which cause to poor performance. Since the back to back antennas position and no extra metal particles around the antennas in the probe-fed simulation for 94 GHz, they are better than the obtained results for 77 GHz antennas.

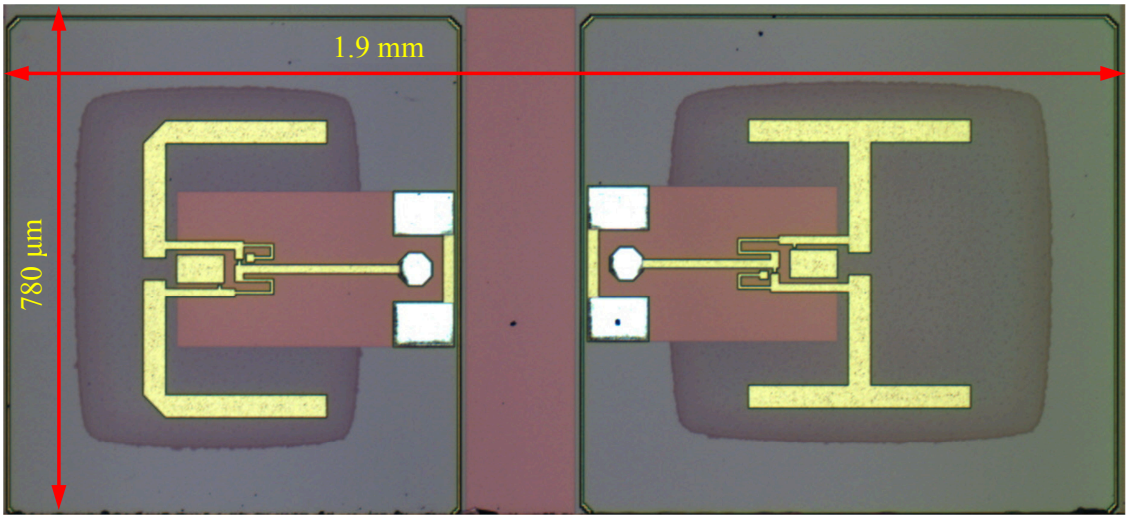


Figure 3.30: Fabricated 94 GHz on-chip L and T antennas.

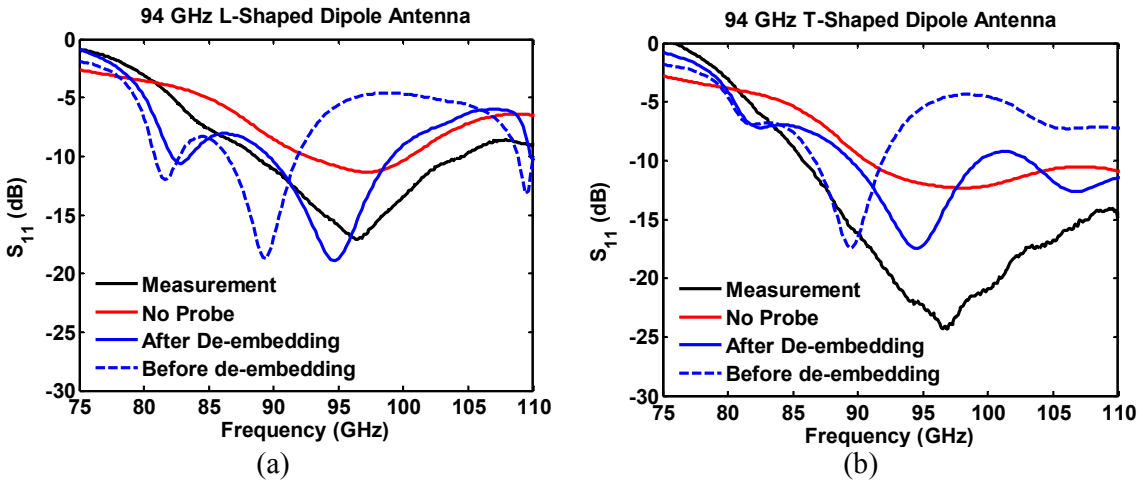


Figure 3.31: Reflection coefficient for 94 GHz (a) L and (b) T antennas before dicing.

3.6.1.2 L- and T-Shaped Antennas Radiation Patterns

The L and T antenna radiation patterns are shown in Figures 3.32 and 3.33. The antennas radiation patterns are simulated with and without ACP probe model as they are next to each other similar to measurements. There are nulls at $\theta = 0°$ in cross-polarization of H-plane patterns. These nulls can be the effect of probe which causes to decrease in cross-polarization components and increase in co-polarization components at $\theta = 0°$ in H-planes. Although the ACP probe model is used during the simulation, however, its head and reflected EM waves

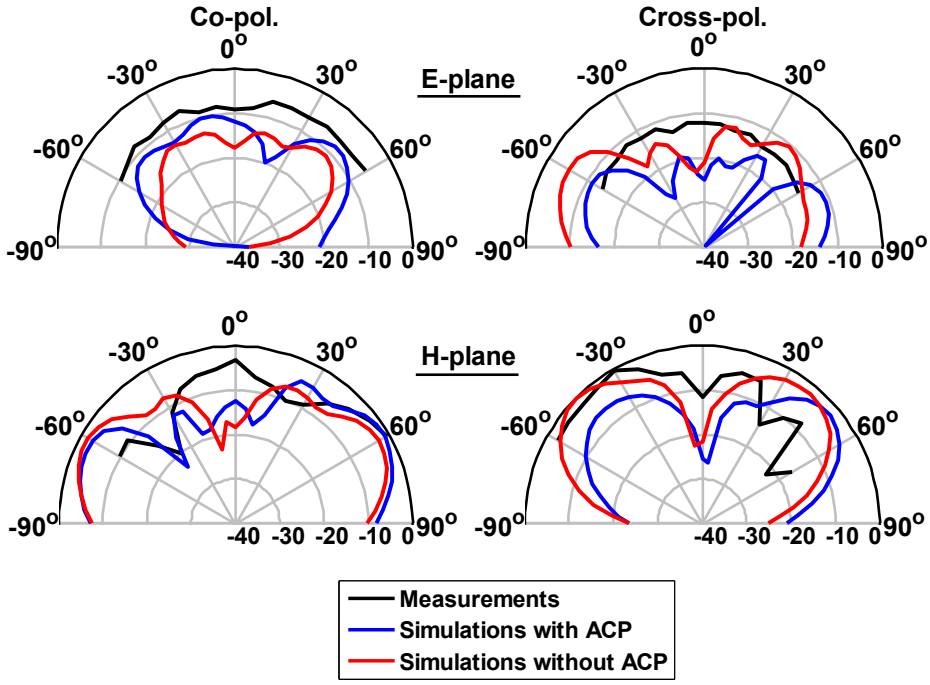


Figure 3.32: Co- and cross-pol. radiation patterns for L antenna on E/H-plane at 94 GHz.

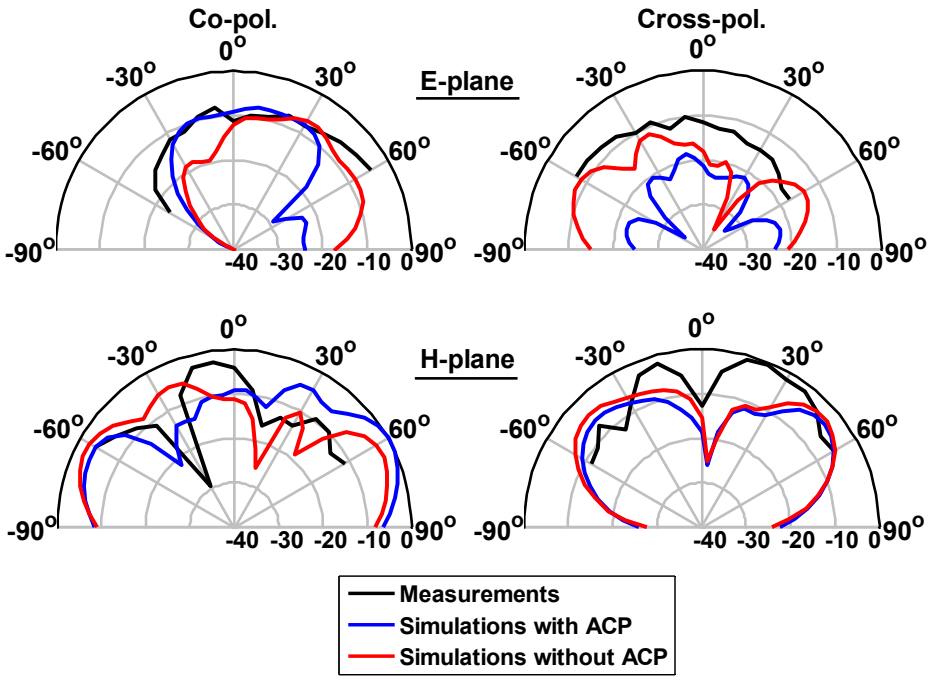


Figure 3.33: Co- and cross-pol. radiation patterns for T antenna on E/H-plane at 94 GHz.

from the measurement setup environment can cause the differences between the simulated and measured radiation patterns at 94 GHz.

3.7 Dielectric Constant Measurement of Si Slab

Variation in Si dielectric constant, as the substrate below the antenna, can cause shift in antenna resonance frequency. A phase based experiment [72-74] is performed to specify the Si dielectric constant range which is placed by 11.9 in the simulations. In this experiment a slab of silicon wafer with dielectric constant of ε_1 is placed in the far fields of the two horn antennas as shown in Figure 3.34. Thickness of the DUT is supposed to be d_1, while d_0+d_1 is the total distance between the two antennas. Impedance variation in the direction of wave propagation will cause multi-reflections inside the silicon sheet and infinite series of rays with different phase difference will be picked up by the receiver antenna (RX in Figure 3.34).

S_{21} between two antennas can be calculated for the configuration of the Figure 3.34 which is confined to the air (ε_o) at both sides of the DUT. Analytical relation for S_{21} is obtained as follow,

$$\begin{aligned} S_{21} &= e^{-jk_0d_0}T_{21}e^{-jk_1d_1}T_{12} + e^{-jk_0d_0}T_{21}e^{-j3k_1d_1}\Gamma_{12}\Gamma_{12}T_{12} + \cdots \\ &= e^{-j(k_0d_0+k_1d_1)}T_{21}T_{12}(1+\Gamma^2e^{-j2k_1d_1} + \Gamma^4e^{-j4k_1d_1} + \ldots) \\ &= e^{-j(k_0d_0+k_1d_1)}T_{21}T_{12}\big/(1-\Gamma^2e^{-j2k_1d_1}), \qquad |\Gamma| < 1 \end{aligned} \tag{3.14}$$

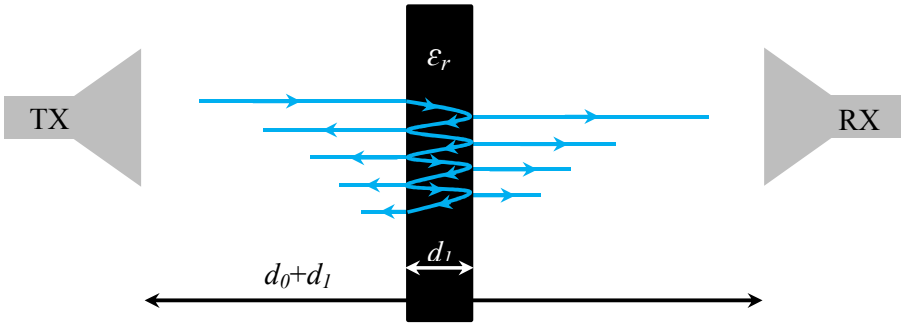


Figure 3.34: Schematic of the measurement setup.

where T_{21} and T_{12} are transmission coefficients from air to dielectric and vice versa, respectively. Γ_{12} is reflection coefficient from dielectric to air and is defined as:

$$\Gamma = \Gamma_{12} = \frac{1-\sqrt{\varepsilon_r}}{1+\sqrt{\varepsilon_r}} \tag{3.15}$$

and

$$k_i = \omega\sqrt{\mu_0\varepsilon_i}, \quad i = 0,1 \tag{3.16}$$

which is wave-number in each of the media.

Accurate measured phase between transceiver antennas will be

$$\varphi_{S_{21}} = -(k_0 d_0 + k_1 d_1) - \tan^{-1}(\sin(2k_1 d_1)/(\Gamma^{-2} - \cos(2k_1 d_1))) \tag{3.17}$$

which is deduced from relation (3.14). We can use phase of the measured S_{21} and (3.17) with determined d_0+d_1 and d_1 to calculate the permittivity of silicon at the measured frequency. In this case, accurate values of measured phase, transceiver antennas spacing and dielectric thickness is needed to achieve accuracy in the calculated ε_r.

Two increase the accuracy of measurement, phase of S_{21} is measured in two cases; 1) Silicon sheet is placed between the antennas. 2) Silicon is absent between the antennas.

Phase difference between two cases can be calculated by subtracting two transmitting phase in (3.17), when the silicon is between the antennas and silicon is replaced by air (by setting $\varepsilon_r = 1$ or $\Gamma = 0$ in (3.17)).

$$\Delta\varphi = \varphi_{S_{21}}\Big|_{air} - \varphi_{S_{21}}\Big|_{sub.} = (k_1 - k_0)d_1 + \tan^{-1}(\sin(2k_1 d_1)/(\Gamma^{-2} - \cos(2k_1 d_1))) \tag{3.18}$$

The calibrated formula is independent of the spacing between the antennas. If multiple reflections are neglected, one can obtain a closed form expression for the solution which is given by

$$\Delta\varphi = (k_1 - k_0)d_1 = 2\pi f d_1(\sqrt{\varepsilon_r} - 1)/c \tag{3.19}$$

by replacing $\Gamma = 0$ in (3.18). Although evaluated ε_r in (3.19) cannot achieve a good approximation due to neglected multiple reflections, however, relation (3.19) can easily be solved for relative dielectric constant as given in (3.20).

$$\varepsilon_r = (1 + c\Delta\varphi/(2\pi f d_1))^2 \tag{3.20}$$

The setup for transmitting power phase measurement is shown in Figure 3.35. Two 25 dBi and 15 dBi horn antennas are used as the transmitting and receiving antennas. Around the antennas and ground plane are covered by absorbers, due to the destructive effect of reflections on measured phase. To investigate the effect of polarization in measurements, the vertical and horizontal polarizations are examined by rotating the antennas by 90°. The measurements are done at W band frequency. Simulated phase difference for various dielectric constants in Figure 3.36 (a) and measured phase difference $\Delta\varphi$ for 500 μm thick silicon wafer in Figure 3.36 (b) are shown. Figure 3.36 (b) demonstrates that the dielectric constant of measured 500 μm thick silicon wafer varies between 10.5 to 12.5 in W band frequency. ε_r for the measured $\Delta\varphi$ with accurate relation (3.18) and closed form formula (3.19)

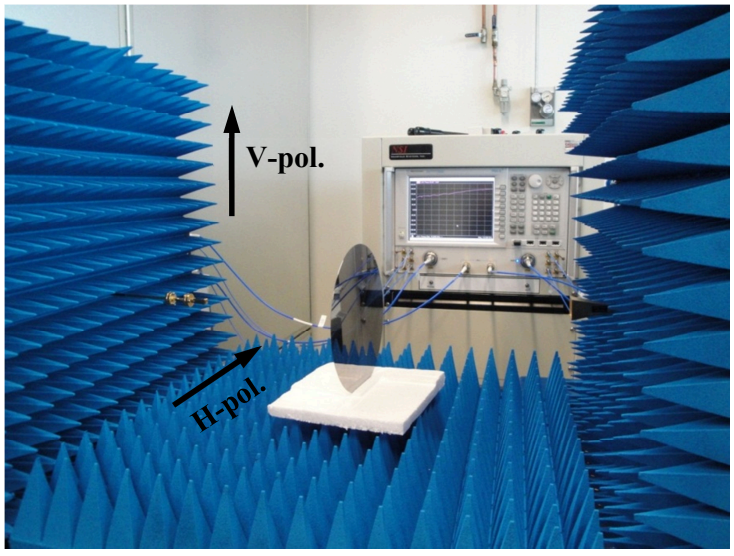


Figure 3.35: Measurement setup to specify Si sheet dielectric constant.

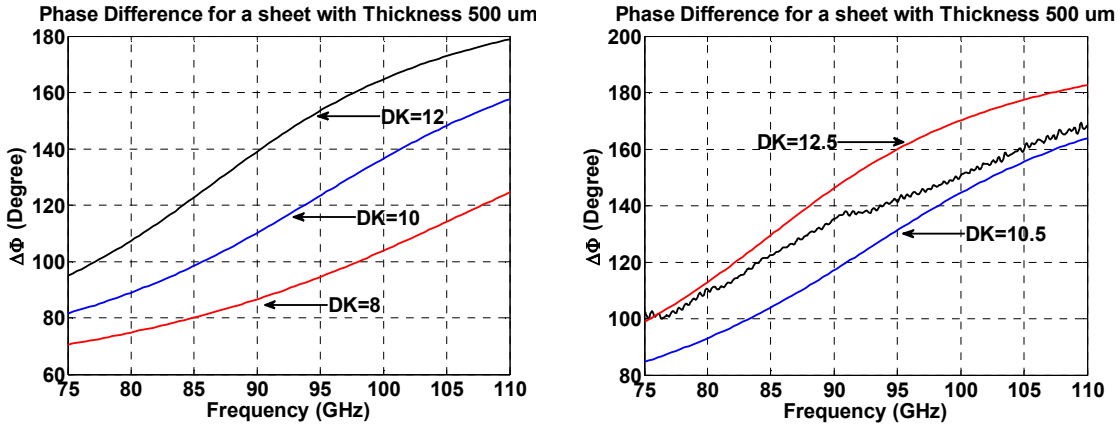


Figure 3.36: (a) Simulated phase differences for various dielectric constants and (b) H-pol. measured ΔΦ with simulated values for 500 μm thick Si sheet.

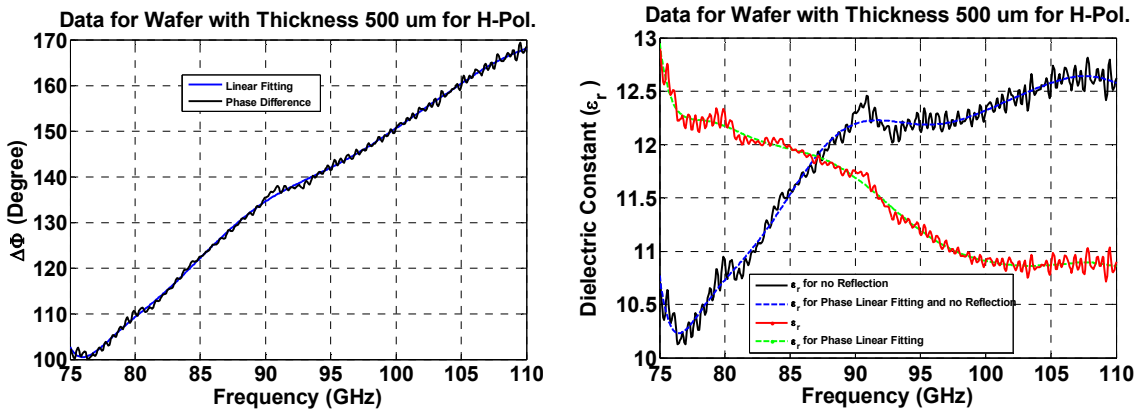
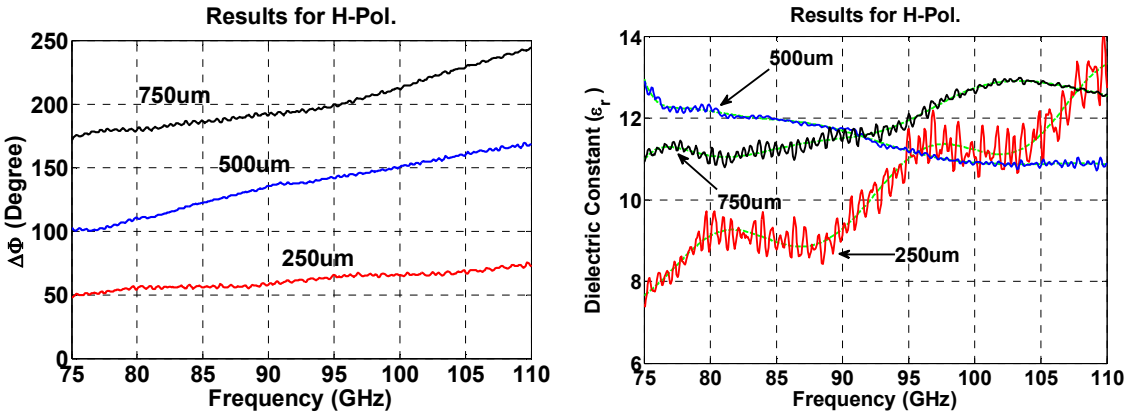


Figure 3.37: (a) H-pol. measured ΔΦ and (b) calculated ε_r with accurate (red) and closed form relations (black) for 500 μm thick Si sheet.

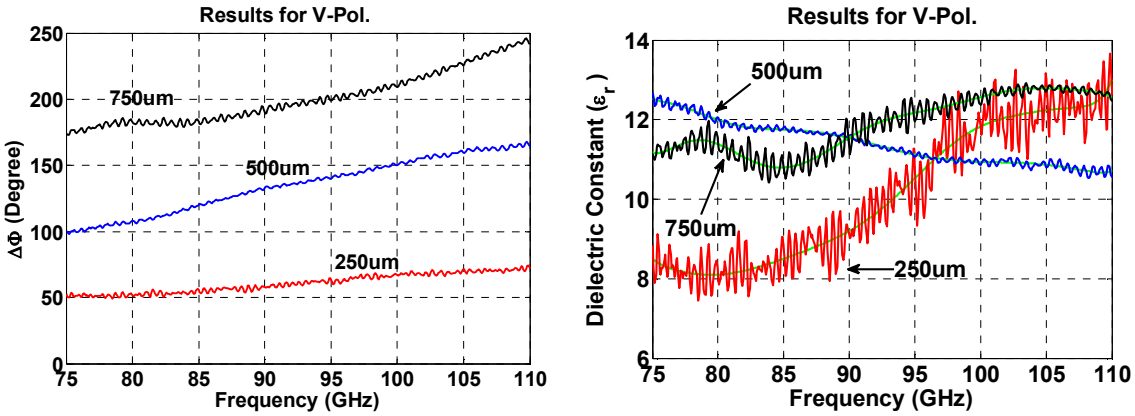
and (3.20) are calculated in Figure 3.37. Because of the fluctuation in the curves, ΔΦ is also fitted with a line for minimum error and then ε_r is calculated and shown in Figure 3.37 with green and blue colors. The fluctuations in the measured ΔΦ are coming from multiple reflections of the surrounding environment and cause to instability in the calculated dielectric constant accordingly. Calculated accurate ε_r curve is descending versus frequency, while ascending for when the reflection is neglected in (3.19).

The measured ΔΦ for Si sheets with various thicknesses and calculated corresponding ε_r are shown in Figures 3.38 and 3.39 with horizontal and vertical polarized (Figure 3.35) horn antennas, respectively. The fluctuations for vertical polarization are more than the



(a) (b)

Figure 3.38: (a) H-pol. measured ΔΦ and (b) calculated ε_r with accurate relations for Si sheets with different thicknesses.



(a) (b)

Figure 3.39: (a) V-pol. measured ΔΦ and (b) calculated ε_r with accurate relations for Si sheets with different thicknesses.

horizontally polarized measurement due to reduced reflections. In horizontal polarization the magnitude of the incident E-fields to the bottom absorber are highly attenuated versus the vertical polarized E-field. As shown in the results, small fluctuation in the measured ΔΦ, causes to instability in the calculated ε_r. Moreover, the measured/calculated ε_r for thicker Si sheets is very close to its typical value 11.9.

3.8 Summary to On-Chip Antennas and RFIC Monolithic Chip

The influence of different parameters that affect on the practical results of the designed on-chip dipole antennas in Chapter 2, was discussed and demonstrated by comparing the measurement and modeled ACP probe tips, ground size effect and GSG pads in the simulations. The ACP probe deteriorates both antenna reflection coefficient and radiation

pattern. The embedded GSG pads as the probing pads cause to frequency shift in antenna resonance. The ground plane causes to propagation of excited surface wave by grounded thick substrate. Due to the cost of BiCMOS process, the used area on the chips is decreased, as possible as it can, during the samples fabrication, while they are aimed to be utilized on the RFIC with greater dimensions.

When an on-chip antenna is integrated with other components such as low noise amplifier, phase shifter, up/down convertor, inside a single chip, the chip size and Si area surrounding the antenna is changed. Therefore, the antenna performance including near and far fields are completely affected by that circumstance when it is integrated inside a single chip. Moreover, the used GSG pads for measuring on-chip antenna alone are not required after integration and antenna resonance frequency is changed. This means the manufactured/measured antenna results for alone on-chip antenna and integrated features can be significantly different. In addition, the antennas performance will deteriorate by employing multiple of antennas as an array in monolithic manner inside a single chip, because of the lossy Si substrate, coupling between the antennas and complexity of the structure. The grounded thick Si substrate with high permittivity excites substrate modes at W-band frequency that distort the antenna radiation pattern. Although the ground plane can be removed, however, the antenna gain will drop drastically, and practically the RFIC chip needs to be mounted on a plate that is mechanically strict and may have high conductivity. The other remedy to prevent the substrate wave excitation may be polishing the bottom of the chip to reduce the thickness of Si, that changes the quarter wavelength height and decrease the antenna gain.

All the mentioned problems compel us to change the way of thinking for integrating on-chip antenna in mm-wave radar and investigate the other solutions. One of the solutions is to suppress the substrate modes using the Electromagnetic Band Gap (EBG) structures around the antenna that increase the chip area and cost. The other solution can be manufacturing the antennas on the PCB board and integrate with the on-chip active components. The advantage of this method is its lower cost, unlimited area for antenna on the PCB, lower occupied chip area. Integration of active on-chip components to the components on the PCB board can be highlighted as the challenging part of the method. In the following chapters, a 77 GHz phased array radar receiver front end that employs the active phase shifter chips on the passive components and antenna array on the PCB are discussed in detail.

CHAPTER 4

INVESTIGATION ON DIFFERENT COMPONENTS FOR ITEDRATING 77 GHZ RADAR RECEIVER ON PCB BOARD

Radar designers attempt to improve the system-in-package performance by increasing the efficiency of antenna, phase shifter/receiver chip as well as RF transitions that are employed for interfacing between the chip and printed circuit board (PCB). Connecting the patterned PCB circuitry to the chips with minimum insertion loss for exploiting probe-measured performance of chip, is demanding innovations and improvements in both the circuits on the board and the connecting techniques. One of these techniques is to place some of the components of the radar receiver to the RFIC chip and rest of the components/transitions to the PCB board and then use packaging techniques to combine these components [75] which offer superior cost performance compared to RFIC chip only solutions [76]. A 77 GHz phased-array radar receiver is shown in Figure 4.1 with on-chip active phase shifter and other components: patch antennas, microstip lines (MS), coplanar waveguide (CPW) lines, and power dividers that reside on the PCB board. Connection of the chip and the PCB board are implemented using wire bonds and the measurements are performed from the PCB board via coaxial probe. Figure 4.1 presents a 77 GHz phased-array radar receiver with active phase shifter chip and PCB circuits. The chip is built using a low-cost SiGe HBT process providing a high-level of integration. The chip is integrated with the PCB circuit using wire-bonding.

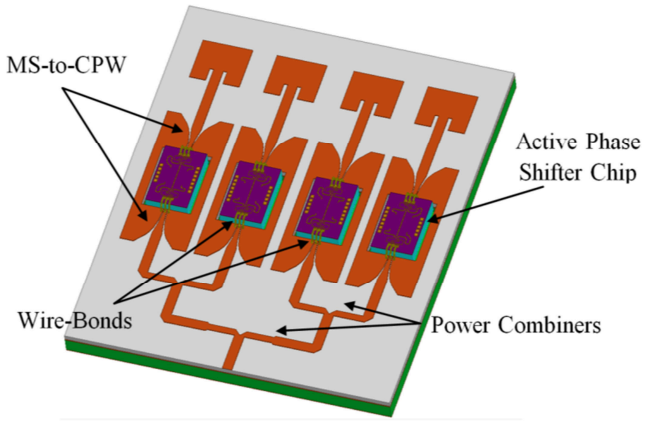


Figure 4.1: Schematic of four-element 77 GHz radar receiver front-end

The effect of wire-bonds is investigated in simulations and in order to decrease bonding loss, short length and tight bonds are realized for chip-PCB board interface. A new procedure based on Klopfenstein impedance matching method [26] is employed in the MS-to-CPW transition section to realize proper matching and less insertion loss at the desired frequency band.

4.1 Four-Element Passive Antenna Array

To evaluate the performance of beam-steering patch antenna array with integrated active phase shifter chips, a passive 1 × 4 patch antenna array was also designed and manufactured on RO3003 board. The passive array was implemented to give the overall performance including power dividers, antennas and transmission lines which were used similarly in receiver circuit at 77 GHz. The only difference between passive array and the integrated array package is the CPW structure which is placed in the middle of MS line between patch antenna and power dividers, as shown in Figures 4.1 and 4.2. Also, the chips are placed in the wells which are etched in the center of CPW, and their ground-signal-ground (GSG) pads are wire bonded to the CPW (Figure 4.1).

The simulated and measured results of 4-element passive array for reflection coefficient and gain will be presented at the operating frequency of antennas. Further power dividers performance and losses resulting from transmission lines and mismatches will also be reported in the next sections.

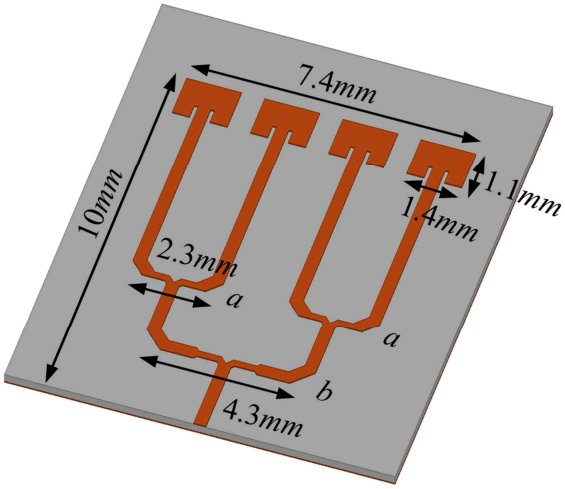


Figure 4.2: Schematic of passive 4-element patch antenna array

4.1.1 Single Patch Antenna

An inset-fed patch antenna operating at 77 GHz was designed and manufactured on RO3003 board. The PCB board has substrate thickness of 130 μm and 17 μm copper cladding. The resonance length of the rectangular microstrip patch antenna is calculated using the relations [77]

$$\lambda_g / 2 - 2\Delta L \tag{4.1}$$

and

$$W = \frac{c}{2 f_r} \sqrt{\frac{2}{\varepsilon_r + 1}} \tag{4.2}$$

where λ_g and ΔL are, respectively, the guided wavelength inside the dielectric and extension length to bring the fringing fields into the calculation.

As the antenna is going to be matched to 50-ohm TL using inset feed, the feed point needs to be calculated. Distance between edge of the patch and feed point, y_0, is obtained by []

$$R_{in} = \frac{1}{2G} cos^2(\pi \frac{y_0}{L}) \tag{4.3}$$

where G is the conductance from each side of the patch and is equal to

$$\begin{aligned} G &= \frac{I_1}{120\pi^2}, \\ I_1 &= -2 + cos(X) + XSi(X) + \frac{sin(X)}{X}, \\ X &= k_0 W \end{aligned} \tag{4.4}$$

Initial values of L = 903 μm, W = 974 μm and y_0 = 376 μm for the antenna length, width and feed distance from the edge of patch, respectively, are obtained to operate the antenna at 77 GHz. The width of 50 Ω MTL is 318 μm.

The antenna is simulated and optimized for S_{11} and radiation pattern at 77 GHz using electromagnetic simulator software HFSS. Simulations accomplished by setting L = 1049 μm, W = 1412 μm, y_0 = 343 μm and g = 100 μm to approach the required return loss and gain at the desired frequency.

The experimental results in data sheet shows the substrate dielectric constant of 3 for

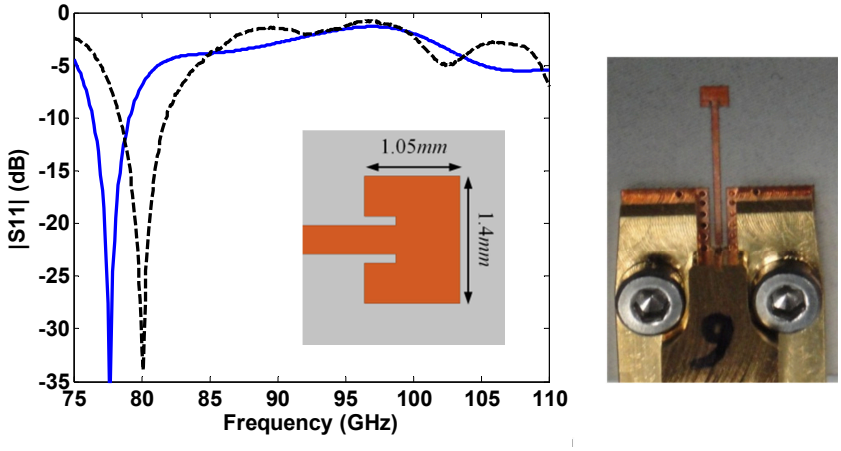


Figure 4.3: Measured (--) and simulated S_{11} for single patch antenna.

frequency range of 8 to 40 GHz and dissipation factor of 0.001 at 10 GHz. As it is shown in Figure 4.3, 3 GHz frequency shift of resonance frequency of the microstrip patch antenna is due to ε_r uncertainty at the W-band frequency. The value of ε_r was changed in simulations to tune the resonating frequency to the measured value (80 GHz) and, $\varepsilon_r = 2.8$ was achieved at 77 GHz. The patch antenna dimensions for $\varepsilon_r = 2.8$ are modified as 1.1 mm × 1.4 mm.

4.1.2 Power Dividers

The input signal is divided to feed four antennas using three one-to-two power dividers with different dimensions, as shown in Figures 4.2 and 4.4.

Constructing a 100-ohm resistor between two output ports of Wilkinson power divider is very hard/impossible at 77 GHz; consequently, causes less isolation between those output ports. Spacing between the outputs of each power divider is different from the other and the impacts of 90° bends are significant. Therefore, the optimization of the overall circuit is performed by considering the bends and length of the high impedance (70.71 ohm) transmission lines with fixed spacing between two outputs for each power divider. As shown in Figure 4.4, widths of two different power dividers *a* and *b* are 2.3 mm and 4.3 mm, respectively. Center-to center spacing between the outputs of power divider *a* is around 2 mm to keep the antennas spacings at $\lambda_0/2$. Simulated S-parameters of the power dividers with letter *a*, *b* and their combination, with the dimensions shown in Figure 4.4, are presented in Figure 4.5 (a) and (b) and (c) respectively. Since the simulated results for the 5-port one-to-four power divider show $S_{22} = S_{33}$, $S_{24} = S_{25} = S_{34}$ and $S_{13} = S_{12}$, only 5 results of the S-parameters are depicted in Figure 4.5 (c). The return loss for input ports of all structures in Figure 4.4 are properly matched, while the power dividers suffer from output ports matching

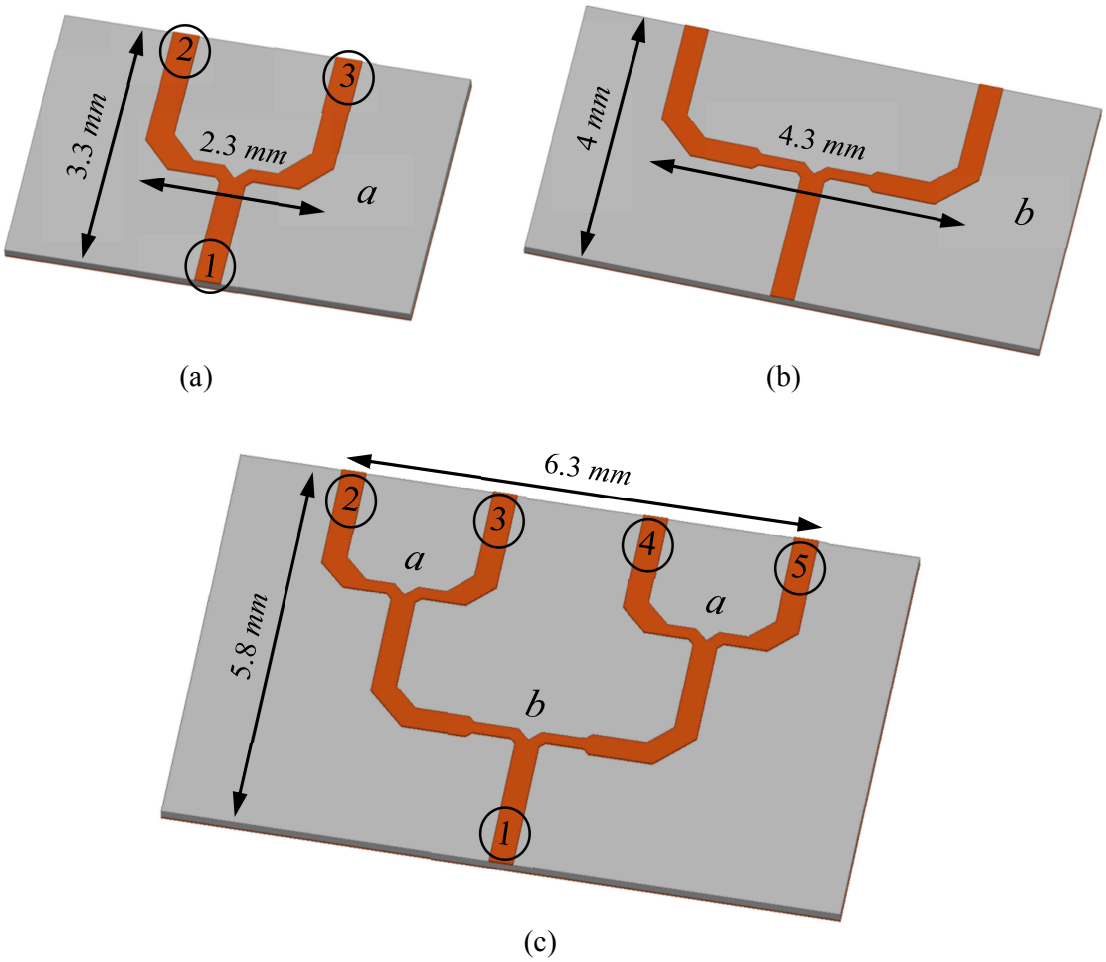
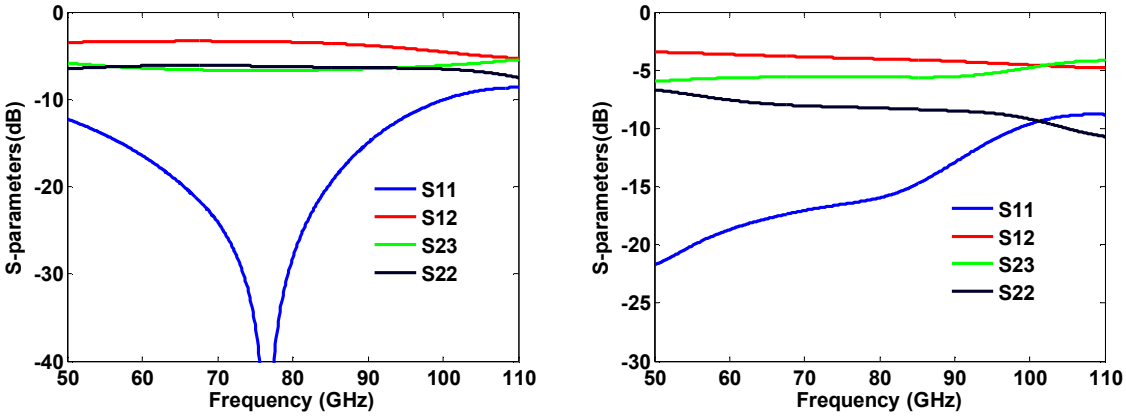


Figure 4.4: The Wilkinson power dividers (a) after patch antennas, (b) after *a* power dividers and (c) the structure after their connections.

and isolation between them due to the removed 100 Ω resistor between the output ports. Simulated results for the 1 to 4 power divider show that the input port is well matched; the insertion loss between input port and each of the output port is 7.2 dB at 77 GHz that demonstrate the 1.2 dB attenuation and radiation loss for the structure. Isolation between ports 34, 24 and 25 is better than 10 dB due to the long paths between them. Isolation between ports 23 is 5.6 dB at 77 GHz. Return loss of the output ports are 6.14 dB at 77 GHz.

4.1.3 Modified Patch Antennas and Overall Structure

The structure of the 4-element antenna array in Figure 4.2 was simulated and measured for reflection coefficient and gain. The spacing between the antennas is $\lambda_o/2$ = 2 mm. As the antennas are designed separately, they are also resonating at 77 GHz in the array (Figure 4.6). Furthermore, as a small object is brought close to the antennas, the null at 77 GHz is highly



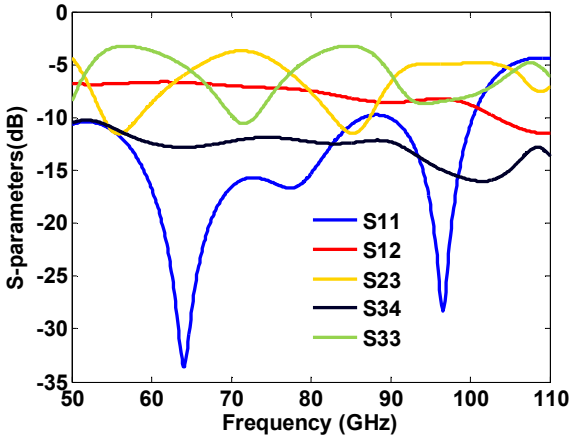


Figure 4.5: Scattering parameters for Wilkinson power dividers with different dimensions (a) with name *a*, (b) with name *b*, and (c) combined 1 to 4 structure.

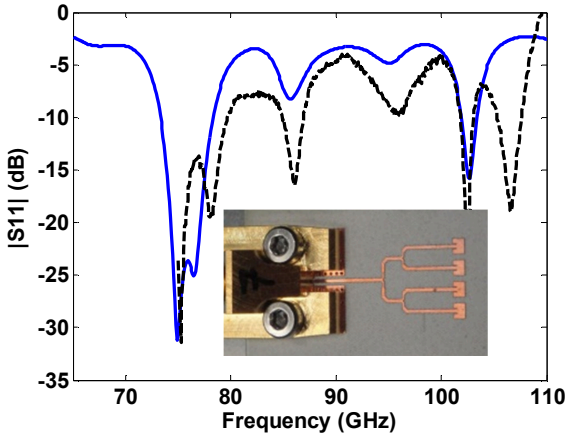


Figure 4.6: Measured (--) and simulated S_{11} for passive 4-element patch antenna array.

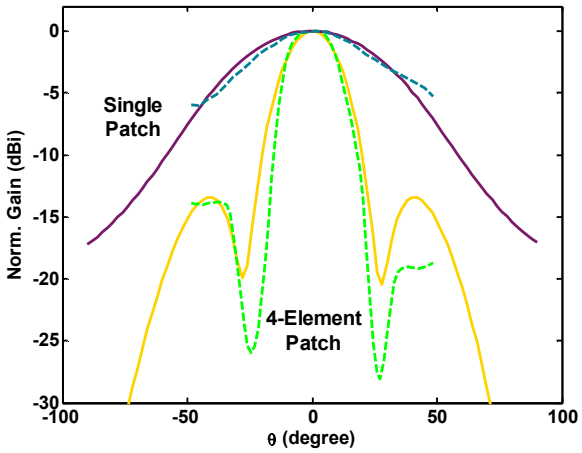


Figure 4.7: Measured (--) and simulated radiation patterns for single and 4-element patch antennas at 77 GHz.

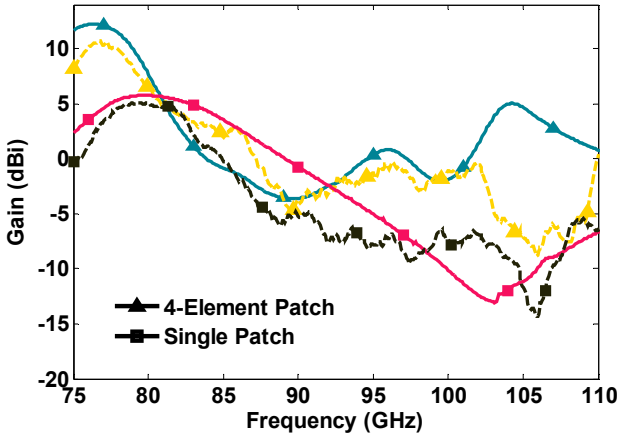


Figure 4.8: Measured (--) and simulated gains for single and 4-element patch antennas at W-band frequency.

affected, which confirms its dependency to the antennas and the radiation from the antennas. Multiple nulls at other frequencies over the W-band in the Figure 4.6 are due to the length of MS lines and power dividers' mismatches and parasitic radiation at W-band. Normalized H-plane radiation pattern for both single and 4-element patch antennas at 77 GHz are shown in Figure 4.7. Simulated and measured H-plane gain over W-band in Figure 4.8, agree well up to 103 GHz. The difference between theoretical and experimental values at the end of W-band can arise from the calibration uncertainty, which is also evident in Figures 4.3 and 4.6. Measurement results in Figure 4.8, show the gains around 10.4 dBi and 5 dBi for 4-element array and single patch antenna at 77 GHz, respectively.

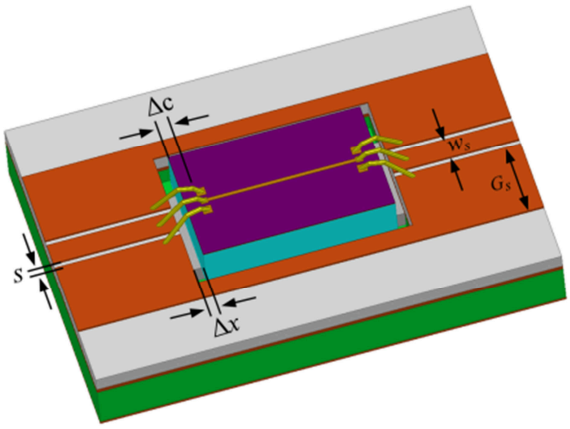
4.2 Integration of the Chip on PCB

In order to embed the active phase shifter chips into the RF circuitry on the PCB board to apply the phase difference between the antennas for steering the beam in the H plane of the patch array, first, a rectangular cavity, which its dimensions are greater than the chip dimension is carved out from the CPW line. Practically, this cavity also helps for easier mounting of the chip on the PCB board. Then the GSG pads on the chip are wire-bonded to the corresponding signal and ground metals lines on the PCB board. The position/location of the embedded chip into the PCB board and wire-bonds are shown in Figure 4.9.

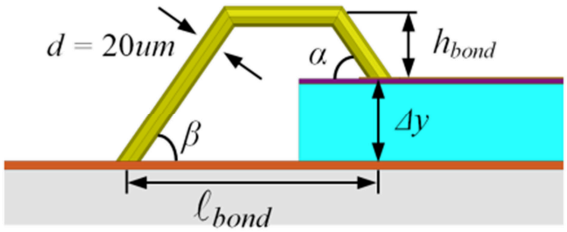
The top and cross sectional schemes in Figure 4.9 presents the lamination of 130 μm RO3003 on the thicker (500 μm) FR4 PCB which increases the mechanical strength of the board and is placed as a basement to hold and fix the chip using silver filled epoxy adhesive film. Since Si substrate thickness of the chip is around 350 μm, a rectangular well with the same height of Si is etched on the board. However, the epoxy thickness can cause the chip surface be located at higher level with respect to the board surface. As it is shown in Figure 4.9 (a), each via connects top/bottom copper layers of RO3003 and FR4 to each other.

4.2.1 Wire Bond Interconnections

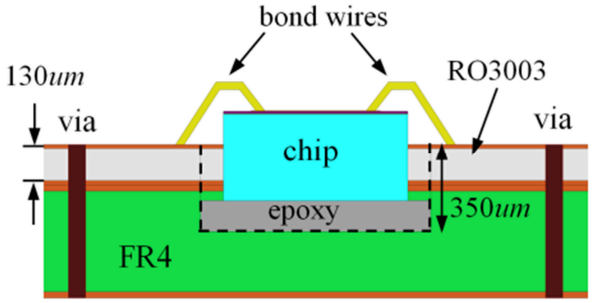
Generally, the wire bond interconnections impose significant insertion loss on the received RF signal. This loss is the result of inductive characteristic of the bonding wires which cause to mismatch in the transition part. Consequently, long and loose bonding can cause very high insertion loss and hence, short-length wire and ball-type bonding is recommended [78-80]. As the frequency is increased, the bond also starts to radiate which increases the inductance of bond wires and insertion loss, accordingly. Using the methods such as multiple bonds, thicker or ribbon type bond, decreasing the height of bond and bending it toward the underneath metal can increase the parallel capacitance of the bond. This capacitance can decrease the high impedance of bond and increase the matching factor [79]. We tried to consider most of the mentioned points by implementing low-height and short-length bonding. To investigate the effect of different parameters on the value of insertion loss by wire-bond interconnections, simulations are performed. These simulation results can give an idea about the insertion loss which can be practically realized in the receiver front-end-circuit.



(a)



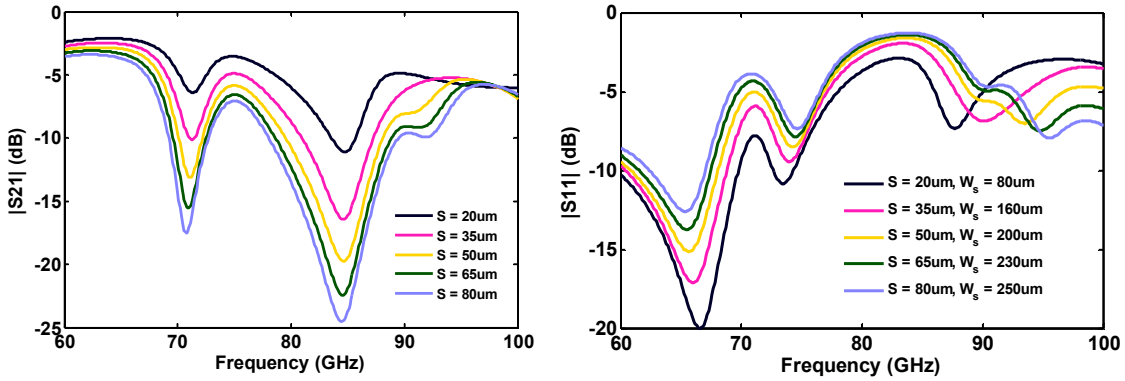
(b)



(c)

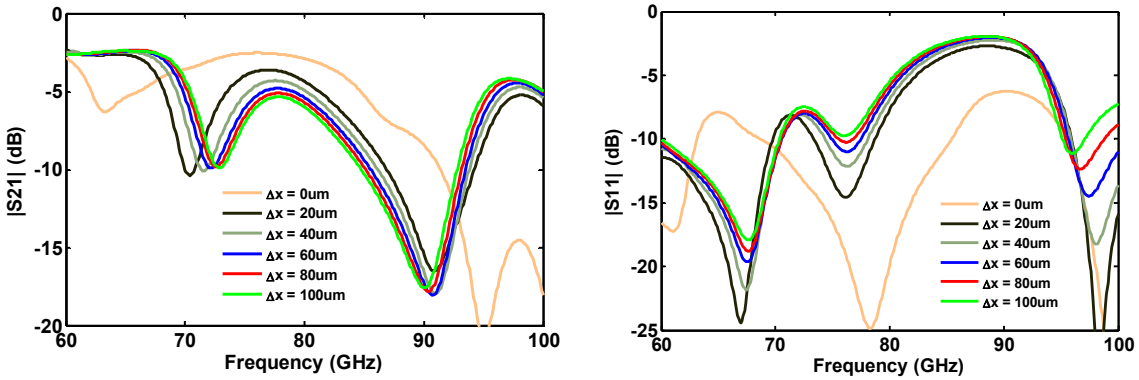
Figure 4.9: Schematic for (a) cross sectional view of the overall receiver circuit, (b) wire-bond different parameter show, and (c) top view of the integrated chip on PCB using wire-bonds interconnections.

The simulations are done for the parameters which are introduced in Figures 4.9 (b) and (c). In Figure 4.9 (c), Δc and Δx are extended part of chip at the back of the GSG pads and the gap spacing due to larger dimension of the etched cavity. Δc is equal to 30 μm at one side and 100 μm in the other side. The bond height (h_{bond}), distance (ℓ_{bond}), chip height from the PCB level (Δy) and rising (α), falling (β) angles of the bond wire are displayed in Figure 4.9 (b).



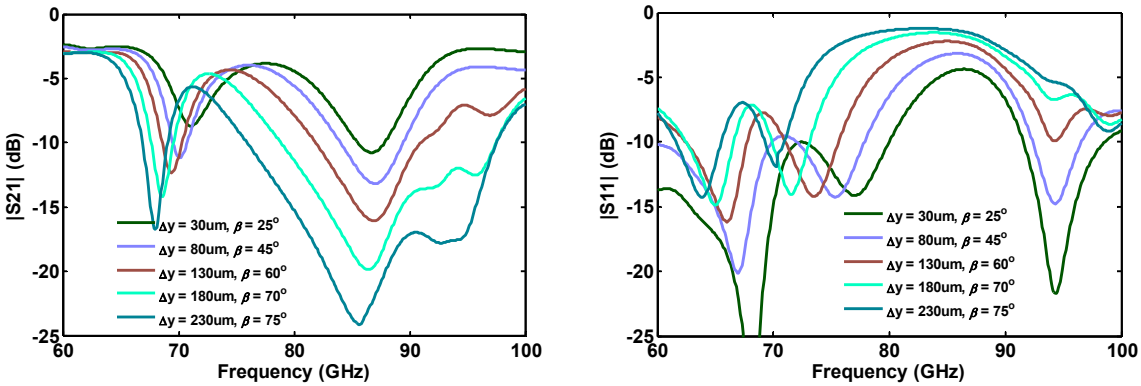
(a) (b)

Figure 4.10: Simulated S_{11}/S_{21} for displaying the effect of different signal trace width (50 Ω CPW) in wire-bonding.



(a) (b)

Figure 4.11: Simulated S_{11}/S_{21} for displaying the effect of gap between chip and CPW edge in wire-bonding. $S = 50\ \mu$m, $\Delta c = 30\ \mu$m, $\alpha = 40°$, $\beta = 45°$, $h_{bond} = 40\ \mu$m, $\Delta y = 80\ \mu$m, $\ell_{bond} = 200\ \mu$m.



(a) (b)

Figure 4.12: Simulated S_{11}/S_{21} to show the effect of chip/CPW level difference in wire-bonding. $S = 50\ \mu$m, $\Delta c = 30\ \mu$m, $\Delta x = 30\ \mu$m, $\alpha = 40°$, $h_{bond} = 40\ \mu$m, $\ell_{bond} = 200\ \mu$m.

The diameter of the gold wire is 20 μm. Since the symmetry is kept for both of the transition parts, only half of the calculated loss can be accounted for each transition in all of the simulations. The chip has active circuit, thus the chip is modeled with its actual size (1.1×1.5 mm^2), and a 50-ohm MS line on the SiO_2 is used to connect GSG pads of chip to each other. The chip model and via-less CPW line are initially simulated only for S_{11} and S_{21} to check them for 50-ohm matching and low insertion loss at 77 GHz.

To see the effect of signal trace width of CPW in the wire-bond, several 50-ohm CPW lines were designed and simulated. As it is shown in Figure 4.10, the simulations are done for various widths of signal line, w_s = 80 to 250 μm, and corresponding gap spacing of S = 20 to 80 μm, by adjusting CPWs characteristic impedance to 50 ohm, and setting the parameters $\Delta c = 100$ μm, $\Delta x = 50$ μm, $\alpha = 40°$, $\beta = 57°$, $h_{bond} = 40$ μm, $\Delta y = 130$ μm and $\ell_{bond} = 250$ μm.

The simulation results show that increasing the width of signal line increases wire-bond insertion loss. For 50-ohm CPW line, w_s and S are changing proportionally and reducing w_s can cause the signal and ground bonds keep their smaller spacings along the bonding wires from chip pads to CPW conductors. These three gold wires are operating as a transmission line with impedance that depends on the distance between the signal and ground wires. When the distance between them is increased the characteristic impedance of this transmission line is increased similar to what is happening for the simulation by increasing w_s and S.

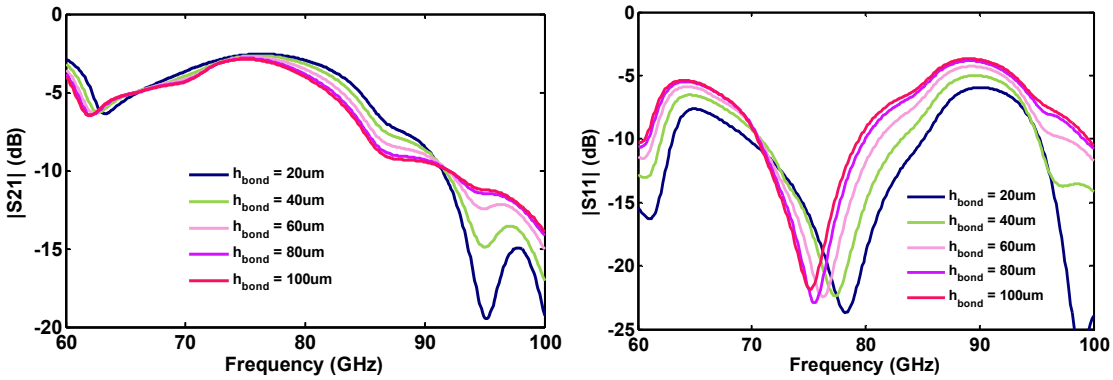
Although the low gap spacing (S = 20 μm) will give us better results, the smallest etching resolution that the PCB prototyping machine (LPKF laser) could etch was S = 50 μm. Thus the remaining simulations are followed by setting S = 50 μm.

The gap between chip and edges of CPW line (Δx), as shown in Figure 4.11, and chip level difference from PCB surface (Δy), in Figure 4.12, have considerable effects on the insertion loss of the bonds. Increasing either Δx or Δy will result in increasing the bond length and degrading the performance. Moreover, by increasing Δy, the falling angle (β) needs to be increased to prevent the contact of the bond with the chip edge.

Changing h_{bond} from 20 μm to 100 μm does not present significant variation on the insertion loss of bond wires (Figure 4.13). Over this simulation, the other parameters are as

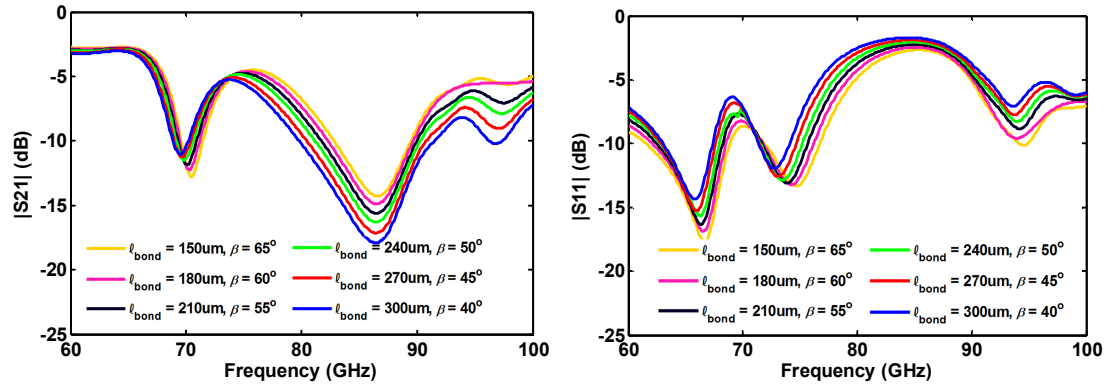
S = 50 μm, Δc = 30 μm, Δx = 0 μm, α = 40°, β = 65°, Δy = 80um, ℓ_{bond} = 200 μm. Since the α and β angles are fixed during the process, variation of the bonds total length does not cause significant changes. Apparently, increasing the bond distance (ℓ_{bond}), increases the bond length and hence insertion loss. The simulations in Figure 4.14, for the swept ℓ_{bond}, are to specify the range of the insertion loss which is imposed by performing different distance bonding in practice.

The measurement of various implemented wire-bonds show that the different parameters are in the range of Δx = 40 to 90 μm (for Δc = 30 μm) and 30 to 50 μm (for Δc = 100 μm),



(a) (b)

Figure 4.13: Simulated S_{11}/S_{21} to show the effect of wire-bonding height. S = 50 μm, Δc = 30 μm, Δx = 0 μm, α = 40°, β = 65°, Δy = 80 μm, ℓ_{bond} = 200 μm.



(a) (b)

Figure 4.14: Simulated S_{11}/S_{21} to show the effect of wire lenght. S = 50 μm, Δc = 30 μm, Δx = 50 μm, α = 40°, h_{bond} = 40 μm, Δy = 130 μm.

h_{bond} = 30 to 50 μm, Δy = 50 to 150 μm, and ℓ_{bond} = 180 to 250 μm. For these parameters, simulated results show that the insertion loss will be lower than 7.5 dB (5-7.5 dB) at 77 GHz.

4.2.2 MS-to-CPW Transitions

The CPW lines need to be connected to the microstrip patch antenna from one side and MS line from the other side. To connect a 50-ohm MS line with trace width of W_0 to the signal line of the 50-ohm CPW line with narrow width (w_s), Klopfenstein impedance matching method [81] is applied for tapering W_0 to w_s ($W_0 > w_s$). In this procedure, the gap spacing (S) and ground plates of CPW line are neglected in first step and it is supposed that the 50-ohm MS line (trace width of W_0) will be connected to another high-impedance MS line with trace width of w_s and impedance of Z_N. (Z_N is calculated for a MS line with trace width of w_s). The geometry of the MS-to-CPW transition which is divided to N equal points is depicted in Figure 4.15. At point $i = N$, W_i approaches to $W_N = w_s$. Afterward, the impedance of N points (Z_i, i = 1, ... , N) are calculated using Klopfenstein method to taper 50-ohm to

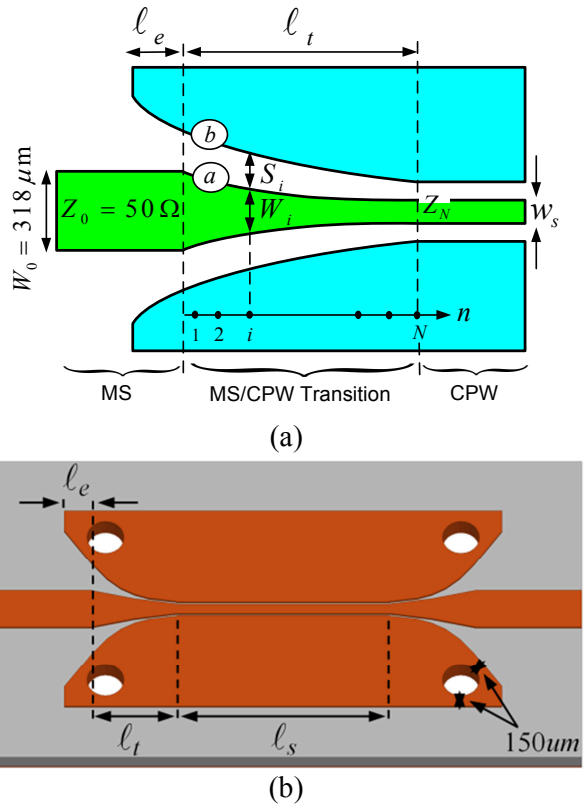


Figure 4.15: Schematic of MS-to-CPW structure for transmitting MS mode to CPW mode and vice versa.

Z_N. In the second step, the MS trace widths W_i are calculated for a MS line with respect to the specified impedance distributions, Z_i. Finally, it is assumed that W_i is the signal trace width of a 50-ohm CPW line and then S_i is determined, accordingly. Therefore, the transition is obtained by connecting W_i points to each other (curve *a* in Figure 4.15) as the signal line, and S_i as the edge of ground plate (curve *b* in Figure 4.15). Here, the 5th order polynomial is used (curves *a* and *b*) to interpolate the middle point for CPW signal trace width and gap spacing. To improve the matching, the ground plates are extended by the length of ℓ_e to the MS part (Figure 4.15). The curves *a* and *b* are functions of ℓ_t and in the case of interpolation with a good approximation (*N* be large enough), ℓ_t can be easily optimized to improve the return loss at the operating frequency.

This method for tapering MS-to-CPW transition helps better matching. Some different methods which use a via-less MS-to-CPW or vice versa have been implemented for probing purposes [82]-[89]. However, these transitions are performed on a Si substrate with high dielectric constant of 11.7. As the dielectric constant of substrate increases, a high percentage of electromagnetic (EM) field is propagating inside the substrate and in-substrate EM wave coupling can be realized simply. Therefore, the CPW mode is easily exchanged to MS line mode due to high dielectric constant.

Here, the MS-to-CPW transitions are designed on RO3003 board with dielectric constant of 2.8 at 77 GHz. This low value of dielectric constant makes the design of transition part challenging. Different methods such as gradually increasing signal line of CPW [86], use matching network [83] were used to have optimum MS-to-CPW transition, however, none of them were good as much as the introduced Klopfenstein taper for our case. Some via-less back to back connected MS-to-CPW line simulation were performed to connect 50-ohm MS to 50-ohm CPW with different gap spacing (*S*). Magnitude of S_{11} and S_{21} are presented in Figure 4.16. Each case is optimized for maximum return loss at 77 GHz, with respect to the transition length ℓ_t and extended ground plates length ℓ_e. Quantities ℓ_t and ℓ_e are shown in Figure 4.15.

Note that, the vias on Figure 4.15 (b) are not valid for the simulation shown in Figure 4.16.

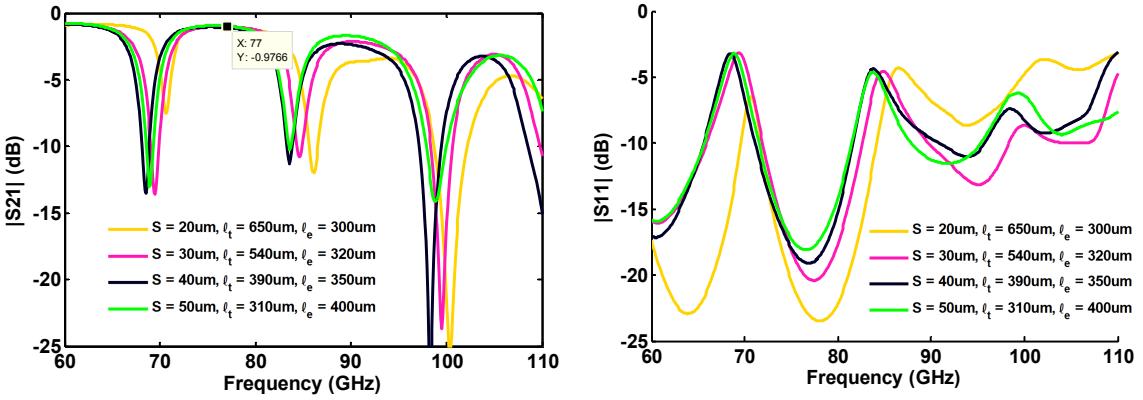
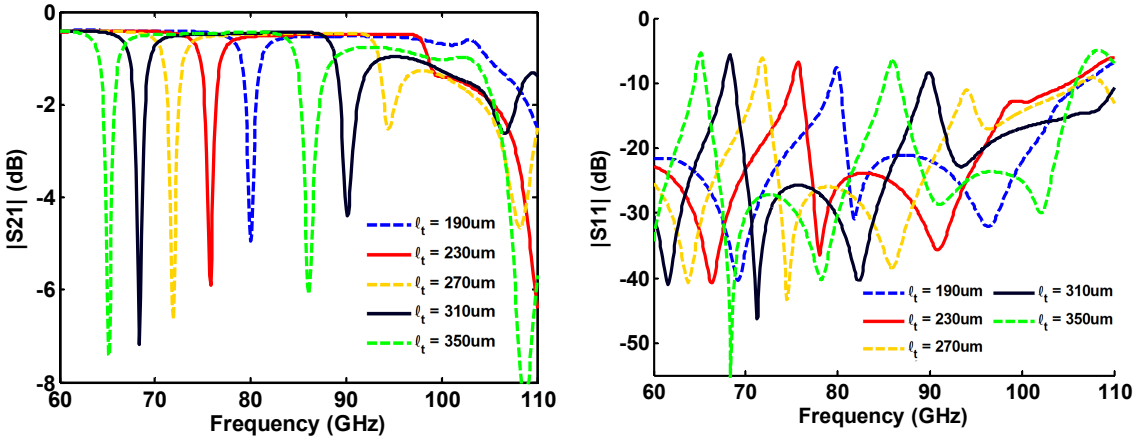


Figure 4.16: Simulated S-parameters for different 50 Ω CPWs in via-less MS-to-CPW structure.

The simulations in Figure 4.16 are done for two similar back to back connected MS-to-CPW transition with ℓ_s = 3 mm. The 10 dB return loss bandwidth is more than 10 GHz and going to be well as the gap spacing (S) is reduced. The simulations show insertion losses better than 1.5 dB in the bandwidth and 1 dB at 77 GHz, as shown in Figure 4.16. As the S is increased, the transition length is reduced and extended length is also increased. In 50-ohm CPW line, by reducing S, value of signal trace width (w_s) is also decreased and hence connecting lower w_s to 318 μm (trace width) 50-ohm MS line needs more transition length. In the other hand, the lower transition lengths are compensated with longer ℓ_e to make the matching well around the operating frequency.

Overall width of CPW line including signal trace width, two gap spacings and two ground plate width (w_s+2S+2G) is fixed to 1.7 mm.

Since only the top layer of the PCB is used for both RF and DC bias lines, the board can suffer from low space to accommodate all DC bias lines. This problem can be solved to some extent by using the ground plates of the CPW, where the chip is placed on, as the DC ground reference. In this way, at least one DC pad per each chip is reduced which is considerable, according to six DC pads of the chip in addition to the DC ground pads. Accordingly, the CPW ground plates are connected to ground plane using vias for DC ground although we try to avoid the vias for its fabrication difficulties and realization with small size and good accuracy. The vias and metal layers which are connected to ground plane are shown in Figure 4.9 (c). The other important point is the location of vias. A single via can be placed just in the middle of CPW ground plate which is irrational since etching the chip cavity will



(a) (b)

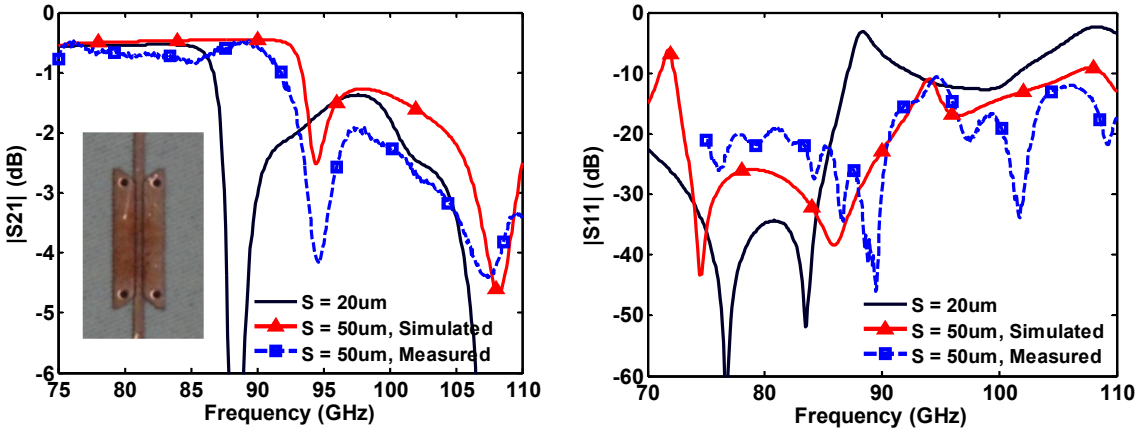
Figure 4.17: Simulated S-parameters for different transition lengths in MS-to-CPW with via.

leave only narrow metal at both sides (Figure 4.9 (a)). The structure in Figure 4.15 (b) is symmetric and it is preferred to keep this symmetry using two vias. The best place for vias can be the end of MS-to-CPW transitions part (Figure 4.15 (b)) which is not only effective for CPW/MS mode exchange but also far away from the chip to use the remaining wide area of CPW ground plates for bonding ground pads of chip. There is manufacturer limitation for the location of vias that they have to be at least 150 μm far away from the edges, as shown in Figure 4.15 (b).

Consequently, the via-less designs are modified with inserting vias at the shown locations in Figure 4.15 (b) and reducing the values of ℓ_t and ℓ_e. The effect of transition length (ℓ_t) in tuning the frequency is shown in Figure 4.17 for S = 50 μm. In the simulations of the Figure 4.17, ℓ_t is changed between 190 to 350 μm, by setting ℓ_s = 4 mm, ℓ_e = 200 μm and total width of CPW (w_s+2S+2G) equal to 1.7 mm. The results show the vias make the bandwidth widen (15 GHz 10 dB bandwidth) and reduce the insertion loss. As it is expected, increasing the ℓ_t causes to shift to lower frequencies.

Between the simulated results, return loss associated with ℓ_t = 270 μm shows compatible bandwidth around the desired frequency and is selected for implementation.

In Figure 4.18, the simulated structures for S = 20 μm, 50 μm and measurement results of



(a) (b)

Figure 4.18: Measured and simulated S-parameters for MS-to-CPWs with 50 μm gap spacing CPW, and simulated for S = 20 μm with vias.

the fabricated sample with S = 50 μm are compared. All parameters for the simulated samples are similar, but ℓ_t = 550 μm for S = 20 μm. These samples show that the matching is going to be well as the gap spacing is reduced, similar to what is occurring in via-less structures in Figure 4.16. The W-band measurements and simulation for S_{11} and S_{21}, show good agreement between them for S = 50 μm. Measurement shows 15 GHz 10 dB bandwidth and insertion loss better than 0.8 dB below 80 GHz.

4.3 Calibration Kit

The Measurements are performed with solderless surface mount RPC-1.00 (up to 110 GHz) Rosenberger probe. For calibration of the probe, transmission lines, open and short circuits are fabricated on RO3003 board.

To calibrate the system till tip of probes, the two ports TRL (also called LRL) calibration method which includes highest accuracy and minimal standard definition [90] is implemented. This method requires very good transmission lines with high accuracy in trace width and length.

In this method, two different length transmission lines are designed as the line of the calibration standard. The electrical length difference between those lines are not allowed to exceed 180° and are designed with electrical length between 10° to 170° to guarantee the difference phase of two different long lines falling into the confined range. Since the

frequency changes will change the phase difference between two lines with fixed length, the design is valid only for limited band of frequency. Difference between electrical length ($\Delta\theta$) of two transmission lines and the corresponding physical length (Δl) are related by [90]

$$\Delta\theta = \frac{360 f \Delta l}{v_{ph}}, \qquad 0 < \Delta\theta < 180 \tag{4.1}$$

where, v_{ph} is the phase velocity on transmission line with $v_{ph} = C/\sqrt{\varepsilon_{r,eff}}$.

To realize $\Delta\theta$ condition two 9.3 mm and 10 mm long transmission lines are designed. Calculated $\Delta\theta$ for the two lines with length difference of Δl = 0.7 mm lies between 100° to 150° along the W-band frequency. As shown in Figure 4.19, two 9.3 mm and 10 mm long transmission lines, zero-length line and open circuit structure are used as the line, thru, and reflect standards in the calibration process, respectively.

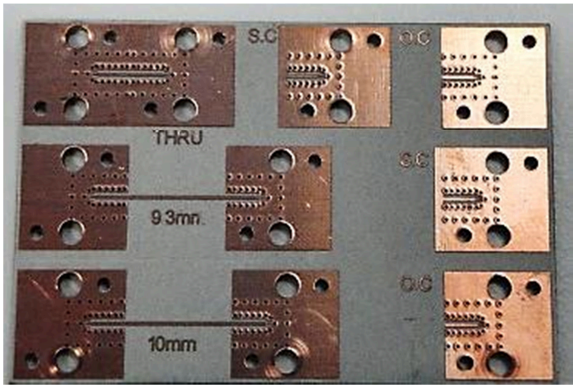


Figure 4.19: Fabricated TRL calibration kit for W-band frequency.

CHAPTER 5

INTEGRATING 77 GHZ PHASED-ARRAY RADAR RECEIVER FRONT-END

In this chapter, the wire bonded active phase shifter to the CPW metals on PCB board is measured for S_{21} phase and amplitude by changing the bias voltages of active phase shifter chip. The measured results can help to see the chip performance as it is integrated on the PCB board. Afterward, the chip is integrated on the PCB with two-element and four-element patch antenna array. The circuit can operates as a beam steering array by controlling the bias voltages of the chips. Measured gain patterns for various bias voltages are shown for the manufactured circuits.

5.1 Active Phase Shifter Chip and Integration on the PCB Board

The active phase shifter structure and its operation are shown. The on chip and integrated forms are characterized to investigate the chip performance in the beam steering array.

5.1.1 Active Phase Shifter and On-Chip Measurement

The used active phase shifter (see Figure 5.1 (a)) utilizes three-vector-sum method based on vector-modulator topology which does not require any additional circuitry other than LNAs to cover full 360^o as compared to traditional designs [91]-[94].

As shown in Figure 5.2 (b), the structure cuts the phase diagram into three regions: I (0^o-120^o), II (120^o-240^o) and III (240^o-360^o). After 3-way Wilkinson power divider, signal splits into three magnitude-even vectors and is separated by 60^o with the help of additional phase shifting lines. The same structure is also used in power combining scheme so that the symmetry results in 120^o phase separation between vectors with a little difference in amplitudes due to lossy lines, which forms these three phase regions. As a final step, 360^o phase coverage can be obtained by changing the LNA gains.

To operate in region I, II and III, the gains achieved from LNA 3, LNA 2 and LNA 1 should be turned-off, respectively. Therefore, each time, one of the LNAs are turned off and, from the summation of the remaining two vectors, one can achieve desired phase in desired

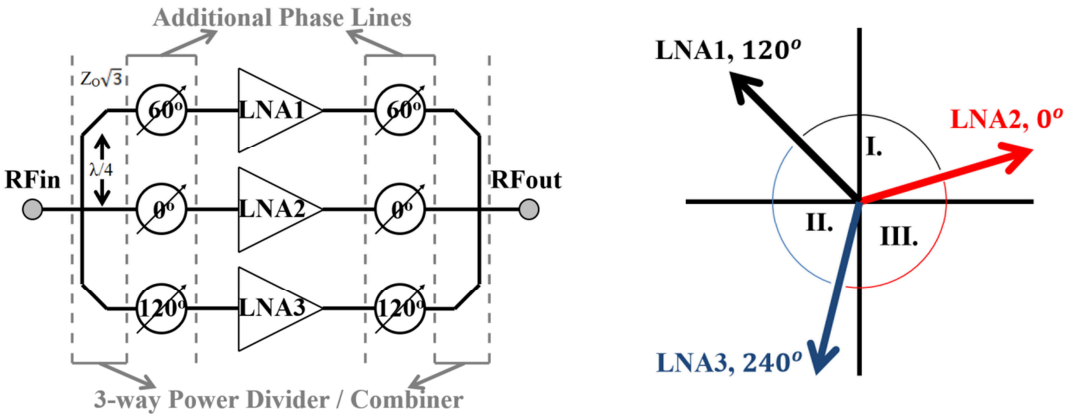


Figure 5.1: (a) Schematic, (b) working principle and (c) fabricated 1.65 mm^2 active phase shifter chip.

region at the output.

Having completed LNA and power divider/combiner, they are combined on a 1.5 mm × 1.1 mm single chip to compose the active phase shifter shown in Figure 5.1 (c) [95].

The on-chip measurement of the active phase shifter is displayed in Figure 5.2 that highlights input and output return losses, gain (or insertion loss) and phase information for different phase states obtained by tuning the LNA biases. The voltage sweep range is taken as 0.8 V to 1.5 V and maximum 100 mW is consumed.

According to results in Figure 5.2 (a), input and output return losses are above 10 dB level in 76 to 105 GHz band and are quite independent of the LNA matchings due to isolation resistors at the outputs of Wilkinson power dividers. Moreover, variable 0 to 12 dB and 0 to 9 dB gains are achieved at 75 GHz and 77 GHz for different phase states, respectively. As it is seen in Figure 5.2 (c), the phase shifter can sweep all through 360^o continuously.

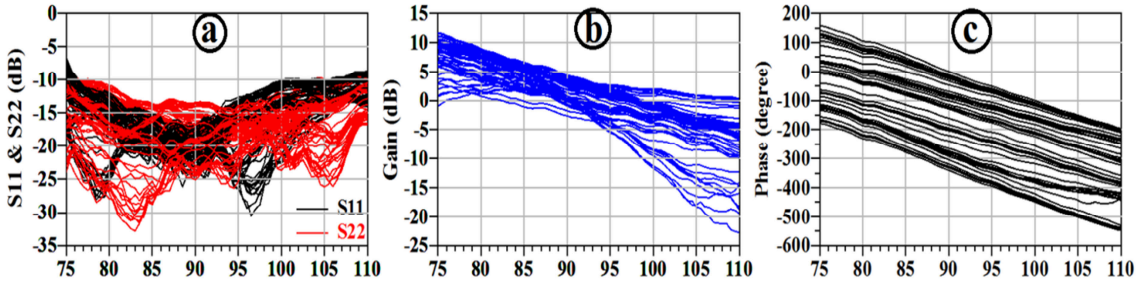


Figure 5.2: Phase shifter performance parameters: (a) measured S_{11} & S_{22}, (b) measured gain, and (c) measured phase states.

5.1.2 Phase/Amplitude Measurement of the Integrated Chip on PCB

The chips are further integrated using CPW line (as shown in Figure 4.9 (c)) and measured on the PCB at W-band frequency. CPW line is connected to the MS lines at both ends to be able to make coaxial cable measurements, as shown in Figure 5.3. The integrated chip is then measured to investigate the performance of chip and wire-bonds at 77 GHz. Consequently, the measurement is done for phase and amplitude by biasing only two of three amplifiers in each step, to sweep the phase difference which falls into one of the three 120° sections, as shown in Figure 5.1 (b). It is expected, by biasing amplifiers 1 and 2, 1 and 3, or 2 and 3 the phase shifts between 0°~120°, 120°~240° or 240°~360° are obtained, respectively. For each combination, the desired two amplifiers are turned on by setting their base voltage to 1.5 V. Then, the drain of one amplifier is fixed to a voltage between 1 to 2 V and the voltage of the other one was changed in the range 1 to 2 V for changing the phase and amplitude of S_{21}. The

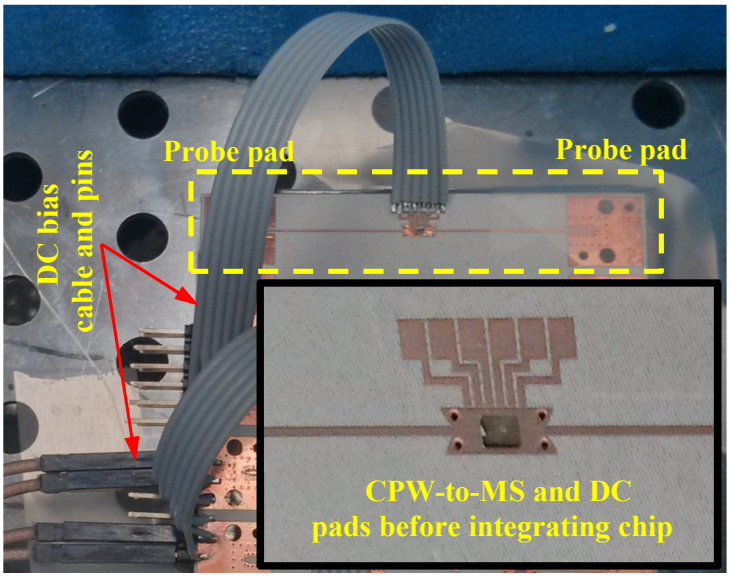


Figure 5.3: Characterization of the integrated active phase shifter chip on the PCB board.

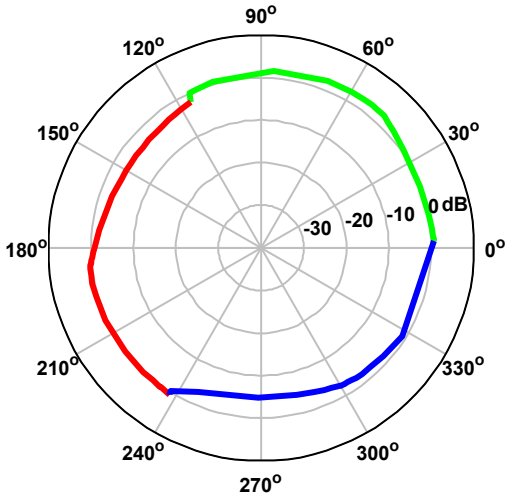


Figure 5.4: Integrated Chip measurement for S_{21} amplitude/phase for different bias voltages.

measurement results for S_{21} phase and amplitude which are obtained for different bias voltage are displayed in Figure 5.4. In this figure, all of the phases are normalized with respect to the phase of middle branch (containing LNA 2 and 0° phase shift in Figure 5.1 (a)).

When the chip is integrated with the PCB board, the measurement shows the gain around 0 dB for the phase differences 0° to 360°, which means the gain of chip in different settings (different amplifier combinations) is canceled by the losses that are arising from wire-bonds (simulated 5 to 7.5 dB insertion loss) and MS-to-CPW transitions (measured 0.8 dB loss), Figure 5.4. Originally, the gain of the on-chip measured active phase shifter was 9 dB.

Furthermore, the wire bonds were utilized by ball-wedge wire bonder machine. The experiments showed the ball-type bond on the 80 μm × 80 μm GSG pads of chip is suitable to place the bump ball on the pad.

5.2 Two-Element Beam-Steering Phased Array

The active phase shifter chip are integrated with the 2-element array on the PCB board to form the 2-element phased array receiver front end at 77 GHz, as shown in Figure 5.5. The spacing between patch antennas is 2 mm. Since the width of the CPW structures is 1.7 mm (as mentioned in 4.2.2), the CPWs of chip A and B are separated by 300 μm gap. The circuit is a receiver circuit and the input of chip is connected to antenna at lower position in Figure 5.5 which causes to locate the DC bias lines at the right of the chips (Figure 5.1). However, the

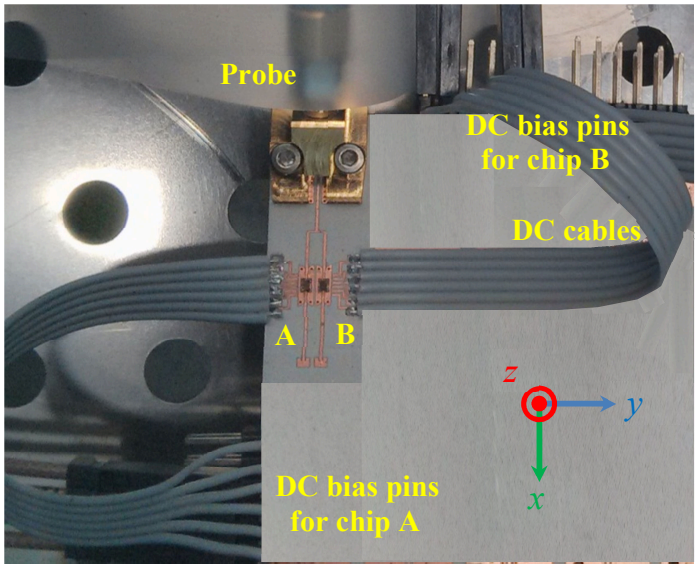
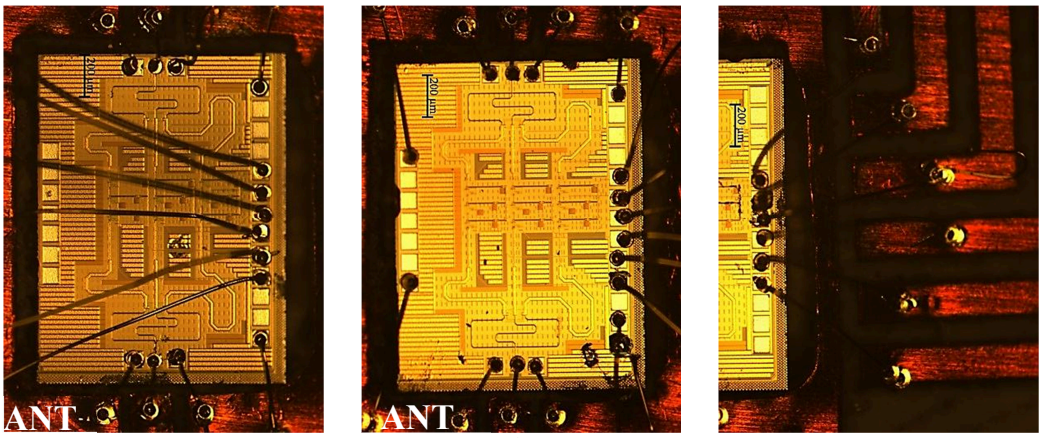


Figure 5.5: Two-element phased array radar receiver.



(a) (b) (c)

Figure 5.6: Wire bonded chips when DC pads are located at (a) left side of chip A and (b) right side of chip B and (c) connections on the PCB pads.

DC traces for chip A are located at its left side (Figure 5.5) and the DC bond cross over the chip to be connected to corresponding pads on the chip. Wire bond interconnections for chips A and B with the specified antenna position are shown in Figure 5.6. As it was measured for integrated chip phase and amplitude, the integrated chip insertion loss is fluctuating around 0 dB (see Figure 5.4). Since the measured gain of single patch antenna is 5 dBi at 77 GHz (see section 4.1.3), the maximum gain of 8 dBi is expected from the 2-element array.

The measured array gains on H-plane of patch antenna (*yz*-plane) for different bias voltages are shown in Figure 5.7. The beam steering is performed for confined number of angles. Since the array is composed of only two antennas, the array factor beam width is wide

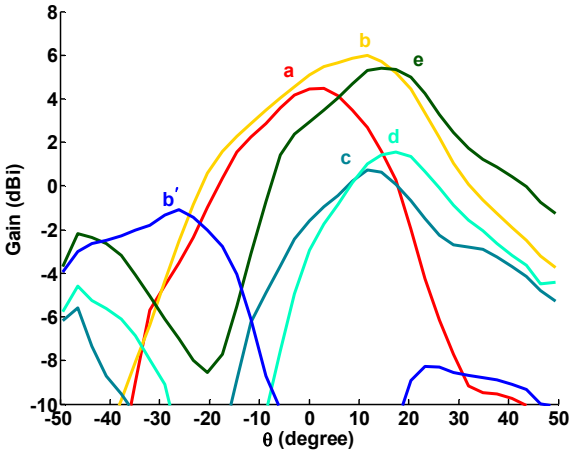


Figure 5.7: Beam-steering measured gain at 77 GHz for the 2-element radar receiver.

and in the case of changed phase, the array factor maximum is dominated by patch antenna beam maximum. Therefore, changing the phase difference between the antennas imposes only some difference in the gain pattern shape, and the maximum position does not change, significantly. The measured beam patterns gain is below 6.5 dBi which is 1.5 dB lower than the expected value. This difference can be duo to the long transmission lines which increase the line loss and radiation and also more loss of wire bonds. During the measurements, the DC base voltages of the used LNAs are set to 1.5 V and drain voltages are changed from 1 to 2 V with the step of 0.2 V. The beams in Figure 5.7 are obtained using the bias voltages displayed in Table 5.1. Because of high DC current flow in LNA 3 of Chip B, only two LNAs of this chip are biased. Due to lower resolution of array beam which is dominated by single patch radiation pattern, the other combinations/drain voltages have very similar beams to those in Figure 5.7 and are avoided.

Table 5.1: DC bias voltages of Chips A, and B for steering the beam to different positions.

Beam Position	Drain DC Bias Voltages of Chip A and B				
	Chip A			Chip B	
	LNA 1 (V)	LNA 2 (V)	LNA 3 (V)	LNA 1 (V)	LNA 2 (V)
a	2.00	2.00	—	1.60	2.00
b	2.00	—	2.00	2.00	1.00
c	1.00	—	2.00	2.00	2.00
d	1.20	—	2.00	2.00	2.00
e	1.60	—	2.00	2.00	2.00
b′	1.00	—	2.00	1.00	2.00

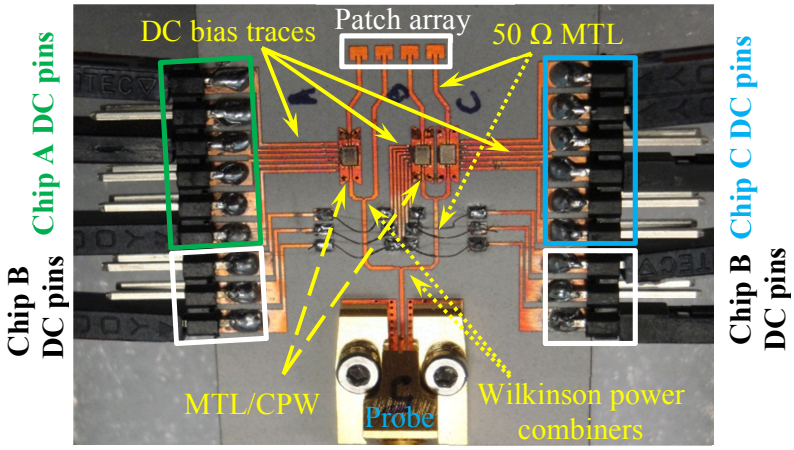


Figure 5.8: Fabricated four-element receiver with DC bias lines and enlarged wire-bonded chip.

5.3 Four-Element Beam-Steering Phased Array

Integrating active phase shifter chips after four antenna input can allow beam steering with good resolution along the direction on which the antennas are aligned (H-plane of the patch antennas). In the 77 GHz 4-element phased array receiver in the Figure 5.8, the spacing between patch antennas is 2 mm. Since the width of the CPW structures is 1.7 mm, the CPWs of chip B and C are separated by 300 μm gap, however, to embed the DC pads of chip B, the arms of large size power combiner are extended by 5.8 mm. After the chips, the MTL get closer to each other to supply the 2 mm spacing.

As it is shown in Figure 5.8, only three antennas are accompanied with chips, one antenna used as reference phase element of the array. Noteworthy, each chip has six DC bias pads (excluding ground pads), which needs six DC-carrying lines on the PCB; including all four chips needed accommodating 24 traces can cause to crossover between DC and RF lines.

Although, all the DC pads of the chips are located on their left sides (when they are aligned similar to Figure 5.8), the DC traces on of the board were located on both left and right sides of the board. Chip A has the DC pads on the left side, and corresponding DC pins on the board are on the left side of the board. Therefore, DC wire-bonds did not cross over the chip A. Chip B has the DC pads on the left side, and corresponding DC pins on the board are both on the left and right side of the board. DC wire-bonds did not cross over the chip B, however, DC lines has to cross over the RF lines over the board. Chip C has the DC pads on the left

side; corresponding DC pins on the board are on the right side of the board. Consequently, DC wire-bonds crossed over the chip C to be able to connect from the right side of the board.

One of the antennas was connected to power divider directly, using the MS line. The received signals by the remaining three antennas pass through the integrated chips. As discussed, with respect to Figure 5.4, the measured amplitude for the integrated chip in different positions is varying around 0 dB. This value is important since the directly connected antenna can also have zero dB (may be 1-2 dB) insertion loss and is not dominated by the others.

Using three active phase shifters for a 1 × 4 array will be possible since one of the antennas will be the reference one. However, if this array is used as a sub-array, then we would need a phase shifter at the fourth antenna or this additional phase shifter can be placed after the summation of four antenna signals. The dimensions of the structure, including the feeding probe and DC bias lines (shown PCB overall area in Figure 5.8) are 3 cm × 3.5 cm.

To receive signals from various angles (steering the beam to a desired angle) the following consideration has to be accounted for this package. Firstly, only the phases of received signals from three antennas are affected by chips. Secondly, estimating DC bias voltage for each chip to supply the required phase is hard. Although the integrated chip was measured by changing bias voltage, as shown in Figure 5.4, however, the same bias voltage in two similar chips can cause to different phase and amplitude. In addition, bonding parameters such as the length of bond and level of chip from PCB (Δy) can differ from one chip to other and different phase/amplitude are achieved for same biasing voltage. Consequently, a new method is required to be employed for measuring the package.

In this method, the probe antenna is fixed to specific angle and all of the DC bias voltages of the chips are adjusted sequentially to maximize the received power value, monitored in Vector Network Analyzer (VNA). After approaching the maximum power level, the bias voltages are left and the received power is measured for the specified angles (-50° to 50°) to form the gain pattern at H-plane. The measured gain pattern at 77 GHz frequency using the proposed method is shown in Figure 5.9. The maximum gain is around 9.7 dBi at 5° for curve b, which is reasonable when it is compared with 4-element passive array (see Figure 4.8).

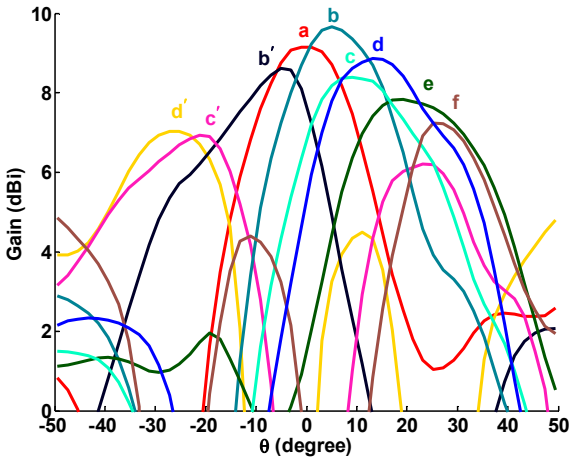


Figure 5.9: Beam-steering measured gain at 77 GHz for the 4-element radar receiver.

As a rule of thumb, the measured integrated chip shows the gain around 0 dB for phase difference between 0 to 360° and hence the phased array can have a performance similar to 4-element passive array which has the gain of 10 dBi at 77 GHz. The transmitting antenna of our set-up can turn up to ±50°. The measurement results show that the array pattern can be steered between ±30°. In the measurements, the LNAs are biased by setting the base voltages to 1.5 V. The LNAs combinations and their drains voltage values for realizing the beams in Figure 5.9, are presented in Table 5.2 for different positions. Four out of nine LNAs of three chips are not used due to high DC current flow or possible damage during the wire-bonding process. The obtained beams in Figure 5.9 confirm that the null angles such as at -15° can be covered if all of the nine LNAs work properly and are exploited during the beam steering.

The measurement setup for biasing the active phase shifter chips and measuring received power at W-band frequency is shown in Figure 5.10.

Table 5.2: DC bias voltages of Chips A, B and C for steering the beam to different positions.

Beam Position	Drain DC Bias Voltages of Different Chips				
	Chip A		Chip B		Chip C
	LNA 1 (V)	LNA 3 (V)	LNA 2 (V)	LNA 3 (V)	LNA 1 (V)
a	2.00	2.00	0.70	2.10	1.50
b	1.90	2.00	0.70	2.10	1.40
c	2.00	1.00	0.90	2.00	1.10
d	2.10	0.70	0.70	2.00	1.40
e	2.00	0.80	1.50	2.00	1.30
f	2.00	1.30	2.00	1.30	1.90
b′	1.80	1.90	0.80	2.00	1.50
c′	1.90	1.80	2.10	0.80	1.30
d′	1.80	1.20	2.00	1.40	2.10

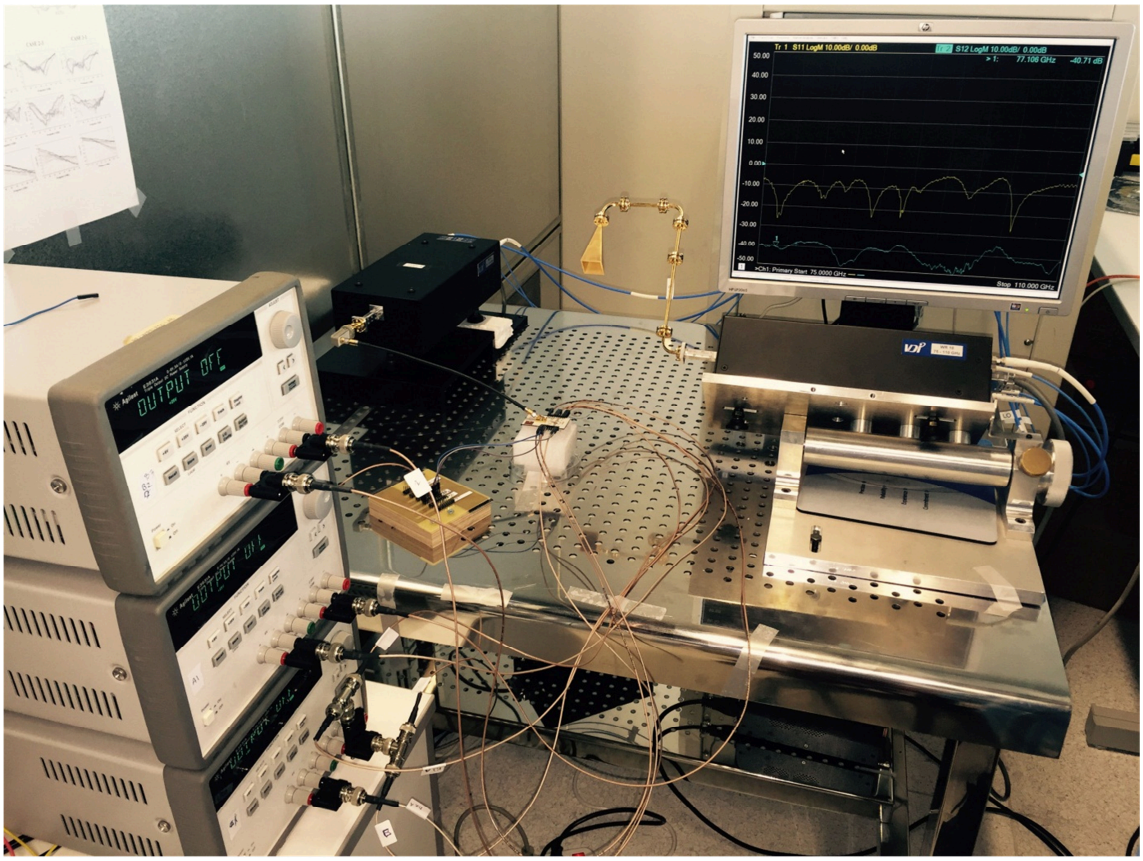


Figure 5.10: W-band measurement setup for integrated phased-array radar receiver.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

The different shapes of on-chip dipole antennas are designed and manufactured at W-band frequency. The on-chip antennas were measured and compared with simulated results. Measured and simulated results confirm that the on-chip antennas suffer from surface waves when they are placed on large size ground plane and a thick Si substrate with high dielectric constant. Surface wave excitation of the grounded chip antennas deteriorate the performance of the antennas and hence decreases its potential to be integrated with other components to realize a single RFIC chip solution. In the case of using multiple antennas as an array inside the RFIC chip, firstly, the distorted radiation pattern of the on-chip antenna cannot steer properly due to excited surface waves, and secondly, and the size of array is increased which causes higher cost of fabrication. However, the on-chip antennas alone can be utilized for other applications with very small ground plane or without ground plane.

Meanwhile, influence of ACP probe tips in presence of ground plane below the chip samples and complexity around probe tips, was demonstrated during the measurement and its effect was modeled in the simulations.

As an alternative, the on-chip antennas are replaced by PCB antennas. In this method, the array of patch antennas, microstrip transmission lines with ground backed coplanar waveguide transitions and power combiners were designed and fabricated on the PCB board. The available active phase shifter chips are embedded to the PCB circuit by wire-bonding their GSG pads to the ground-signal-ground traces of CPW. The two- and four-element phased array radar receiver front-end are measured at 77 GHz for automotive radar application. Although the packaging process can be difficult and cause higher power loss due to the wire-bonds, the beam can be steered to angles between ±30° at 77 GHz for 4-element array. Much lower cost of fabrication with good beam steeing resolution are obtained due to good radiation patterns of the PCB patch antennas.

A more detailed conclusion for each chapter are as follows:

For 77 GHz automotive radar and 94 GHz imaging radars applications, on-chip LC balun circuit with three different straight, L-shaped and T-shaped dipole antennas on the small ground plane were designed and presented in Chapter 2. To increase the gain of the antenna while matching the impedance to 50 Ω, substrate is etched using IHP LBE module except for silicon bars. Antennas are well matched at the design frequency and gains ranging from 0 dBi to 4 dBi are simulated. Antennas can also be arrayed, on small ground, especially for L- and T-type dipoles for higher gain and steering the beam by changing the phase difference between them.

In Chapter 3, GSG pads structure behaves similar to grounded coplanar waveguide (GCPW) and shifts the resonance frequency of manufactured antennas by 3 GHz. If the antennas are designed with the GSG pads for measurement purposes, then manufactured antennas can be measured with the GSG pads. However, if the antenna is integrated to the RFIC chip without the GSG pads, the antenna resonance will be different. To calculate reflection coefficient of the antennas accurately, a $(1.25\ \lambda_o)^2$ large ground plane is enough. However, to calculate far fields of the antennas, larger ground plane simulations are necessary. The destructive effect of surface waves on on-chip antennas that are excited and propagated due to the grounded thick Si substrate and thin SiO_2 layer on it was demonstrated.

The effect of the ACP probe was shown by measuring and simulating the reflection coefficient/radiation pattern of the straight, L and T strip dipole antennas on a large ground plane and when they were manufactured next to each other and diced from each other. The antennas displayed different performances when they were simulated using lumped port excitation. However, the effect of the ACP probe in this abnormality was studied and demonstrated by modeling the probe in simulations. The modeled probe was calibrated in simulation and de-embedded to resemble what was done in VNA for S_{11} measurement. It is deduced that, most of the parameters such as distance of probe from ground plane, material beneath the ACP probe and calibration kit could increase/decrease the error from the coupling between the ACP probe and the material around it. These parameters changed the power of the reflected wave (from those reflector surfaces) at the unshielded part of the probe and affected the recorded data at VNA. Moreover, as the complexity around the ACP probe tips is

increased, the uncertainty of the measured data is also increased, proportionally. The results confirm that the ACP probe is not suitable for on wafer measurements, at all.

A dielectric constant of silicon slab was measured at W-band using free space method to obtain the range that its permittivity is located and compare with the typical value that is used in the simulations. The fluctuation of the measured ε_r values for Si sheets with different thicknesses is due to multiple reflections and diffraction from environment. The measured results can be improved if the measurements are done on perfectly absorbent chamber.

In Chapters 4 and 5, the three-way Active Phase Shifter chips were integrated with 4-element phased array radar receiver and measured for beam steering at 77 GHz using wire-bonding. The beam was steered between ±30° with maximum realized gain of 9.7 dBi using microstrip patch antennas built on RO3003 board. The gain and pattern of 4-element phased array structure and measured passive array are similar, around 77 GHz. To have well matching in CPW-to-MTL transitions on low dielectric constant substrate, a tapering based on Klopfenstein relation was used. The measured two back-to-back connected MS-to-CPW shows a bandwidth of greater than 15 GHz around operating frequency, with the insertion loss that is lower than 0.9 dB. The active phase shifter circuit and the 1 × 4 patch array can be used for 77 GHz automotive radar application.

The advantage of this design is that the chip area is only 1.65 mm^2 and PCB board with antennas and DC bias lines can be manufactured with very low cost. However, when RFIC only solution which has all the antennas and all the active phase shifters and transmission lines is desired, the die area and cost of the receiver will increase.

The PCB-chip package can be optimized by reducing the loss which is coming from the RF carrying wire-bonds interconnections between chip and PCB pads using packaging technologies such as flip-chip bonding or embedded wafer level ball grid array (eWLB).

In flip-chip method, the chip is flipped (front to back) and the pads of the chip are connected to the corresponding pads on the PCB board, as it is shown in Figure 6.1. In this method, the pads on the PCB board are required to be located exactly below the pads on the chip and are connected using the left bumps between two pads and heating the bumps.

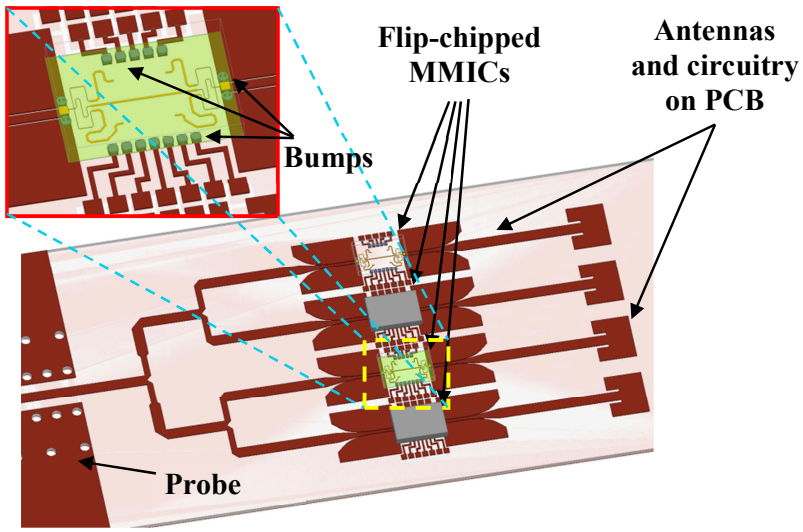


Figure 6.1: Schematic of 4-element phased array packaging using the flip-chip interconnection.

To integrate the chips, high accuracy is needed to locate the pads on the chip are placed exactly on the corresponding bumps on the pads of the PCB, while some of the pads may not be connected during the process. However, the value of transmitting signal loss can be decreased significantly, due to the small height of the bump. Moreover, the location of connections and dimensions of the bumps can be brought into simulations and a suitable matching circuit is designed on the PCB prior to the RF interconnections, which cause to increase the efficiency of the flip-chip interconnection.

In eWLB method, all of the chips are placed in a mold material and then the antennas and the RF/DC circuitry are implemented on the redistributed layers (RDL) which are placed on the mold, as it is shown in Figure 6.2. Therefore, the package is completed using the bumps between the pads on eWLB part and the PCB. The chips pads can be connected to the pads with greater size on the RDL layer that makes the eWLB/PCB interconnection easier and privilege eWLB method over the flip-chip method. Moreover, the sensitive passive circuit that their implementation on the PCB is hard or impossible can be done on RDL of eWLB. However, this method is costly (not as the chip area), and changes with respect to its size.

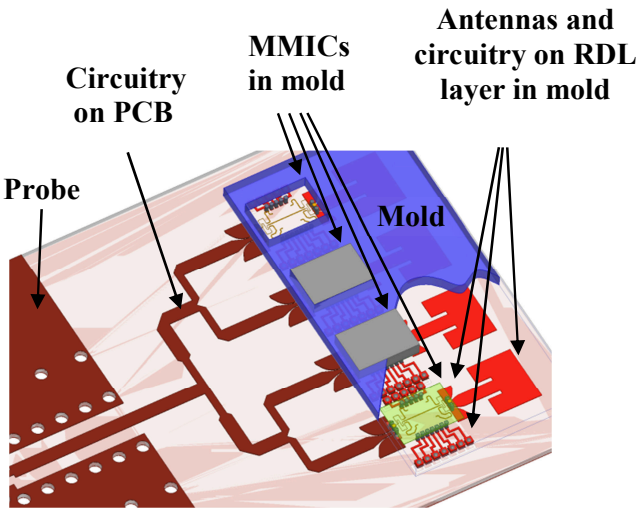


Figure 6.2: Schematic of 4-element phased array packaging using the eWLB method.

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