A Wideband Low Noise SiGe Medium Power Amplifier for X-Band Phased Array Applications

Can Çalışkan[1], İlker Kalyoncu[1], Emre Ozeren[1], Mehmet Kaynak[2], Yasar Gurbuz[1]
[1]Faculty of Engineering and Natural Sciences, Sabanci University, Orhanli, Tuzla, 34956, Istanbul, Turkey
[2]IHP Microelectronics, Im Technologiepark, 25, 15236, Frankfurt (Oder), Germany
email: yasar@sabanciuniv.edu

***Abstract*—This paper presents a Medium Power Amplifier (MPA) for X-Band Phased Array RADAR applications in 0.25µm SiGe technology. The MPA is designed such that it achieves high output power and low noise simultaneously that enables its use in Transmitter/Receiver (T/R) core module as a Low Noise Amplifier (LNA). The MPA achieves 23.6dB peak gain and 17.3dB maximum output power at 10GHz with a power consumption of 190mW. Its input and output is matched in a 7 GHz of bandwidth, while its mean Noise Figure (NF) is about 3dB throughout the defined bandwidth. According to authors' knowledge, this work presents state-of-the-art wideband MPA performances in literature, with 7GHz of operational bandwidth and 17.3dBm output power.**

Keywords— power amplifiers; linearity; silicon germanium; heterojunction bipolar transistors; transformer; low-noise amplifiers;

I. INTRODUCTION

In modern phased array systems, T/R Module gives the opportunity of varying the direction of the multiple antenna elements electronically that enables fast beam scanning [1]. T/R Module is one of the most essential blocks of phased array systems because of its strong influence on system level performance i.e gain, output power, NF, and beam shifting [2]. It consists of major blocks, such as Power Amplifier (PA), Low Noise Amplifier (LNA), Phase Shifter (PS), Single-Pole-Double-Throw (SPDT) switch and Attenuator (Att.) or Variable Gain Amplifier (VGA). PA is one of the most significant blocks of T/R module as it affects transmitting power of the system.

In recent years, Si-based devices reached performance level of III-V devices with the addition of linearly-graded SiGe/Si region in base terminal of HBT [3]. SiGe HBT BiCMOS technology gives opportunity of integration with digital circuits that are Silicon-based technology [2]. However, output power level of HBT devices are limited in compared to its III-V counterparts, due to being restricted by the breakdown voltage limitations. Therefore, SiGe based T/R core module can be preferred as a transition block between III-V and Si-based blocks. In these systems, main high frequency amplifications are achieved with LNA and (High Power Amplifier) HPA in III-V blocks, while SiGe T/R core module exists for reducing expectations from HPA, and inhibiting additional noise sources [4,5,6].

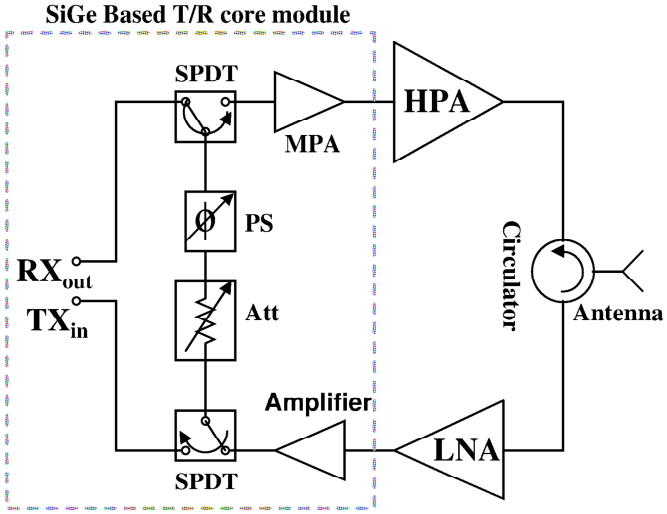

Figure.1. View of SiGe based T/R core module together with III-V blocks

This paper presents a wideband Medium Power Amplifier (MPA) that achieves 17.3dBm of maximum output power with 23.6dB of peak gain. Its NF is about 3 dB at 10GHz, which allows MPA to be utilized as a LNA in T/R core module. For this design, IHP's 0.25µm SiGe BiCMOS technology is used, because of its high gain and high breakdown voltage features. Technology provides High Performance (HP) and Medium Voltage (MV) npn-HBTs having 110 GHz and 45 GHz of f_t, respectively. MV HBTs have 5V of collector-emitter breakdown voltage.

II. DESIGN PROCEDURE OF MPA

The presented amplifier is designed as a block for a SiGe based T/R core module, which can be utilized as a transition block between III-V based RF blocks and Si-based IF blocks, therefore its specifications are not as strict as an ordinary PA. However, targeting high output power with a flat response throughout the defined bandwidth is a major concern. The aim of this block is to be able to achieve more than 15dBm output power with acceptable level of NF and power consumption, which gives chance of utilizing designed amplifier not only as a MPA, but also as a LNA.

The specifications can be prioritized as output power, high and flat gain, wide bandwidth, and low NF. Regarding these expectations, a cascode based topology is preferred, due to

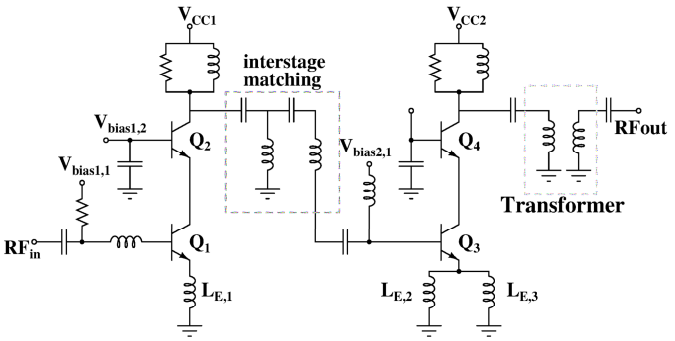

Figure.2. Schematic view of the MPA

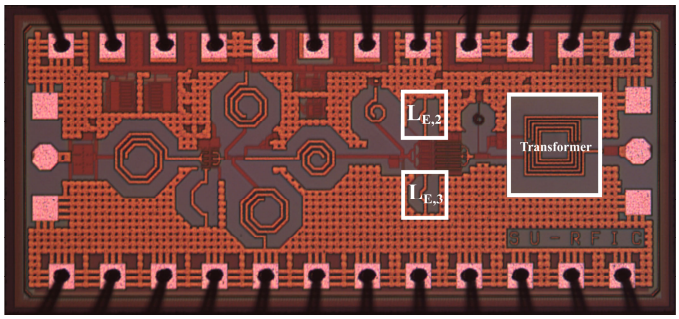

Figure.3. Top view die photo of measured design

required high voltage swing. Moreover, cascode designs are more stable in compared to Common-Emitter (CE) amplifiers, due to the cancellation of Miller effect and high output impedance, which are significant parameters for the stability of PA. Achieving high output power and high gain from a single stage architecture can limit the total performance of the design, such as limited bandwidth, high power consumption. Therefore, two-stage cascode topology is preferred as demonstrated in Figure. 2; first stage is targeted for high gain, while second stage is aiming high output power. HP HBTs are utilized in the first stage and as the driver transistor of the second stage (Q_1, Q_2, Q_3), while Middle Voltage (MV) HBTs are preferred as the load transistor (Q_4), to achieve high gain performance. MV HBTs give chance to increase voltage swing at the output node of the cascode, due to having higher breakdown level, with the cost of reduced gain.

After selecting transistors, bias points are chosen to obtain as high f_T as possible, to conclude with a high gain from first stage. Moreover, f_T has direct influence on NF performance of the amplifier [7], therefore selecting the bias point affects not only gain but also NF performance. On the other hand, the noise of the second stage can be suppressed, by achieving high gain from the first stage while total NF performance is mainly determined by the first stage. Therefore, the gain of first stage is selected as higher than 15 dB, with a NF close to 2 dB.

The DC operating points, especially for the load transistors, are selected regarding the voltage swing range, which is limited by the breakdown voltage of the transistor; the second stage is mainly responsible for maximizing output power, but its input compression can be high due to having relatively low gain. Therefore, the output power of the first stage has to be high to satisfy input power level of the second stage. For that purpose, 15 dBm of output power is aimed for the first stage, which results in about 25 mA of collector current, with 2.5 V of voltage swing. After selecting appropriate voltage biases, current level is decided with regarding the expected power level from the first stage, which is varied by changing the number of transistors.

Different than the first stage, HP and HB transistors are utilized for the second stage. As mentioned before, the purpose of the second stage is to maximize the output power with boosting total gain. For that purpose, voltage and current bias of the cascode topology is calculated with regarding the expected power level; the voltage swing is limited with the breakdown voltage of the HBTs, while current level is selected according to desired output power level. One of the major restriction of mentioned design procedure is low impedance at the output node; requiring high voltage swing and current level conclude with low impedance, which limits the frequency range that desired block is still functional. Actually, there exist a trade-off between operational bandwidth and maximum output power; calculated output impedance value means that the maximum output power can be achieved with that specific impedance. Therefore, as it is matched to load impedance, the output power that amplifier can deliver is reduced. On the other hand, the output impedance is highly varying with frequency, because of the size of the transistors for the second stage is large. Moreover, a mismatch at the output node can cause high reflected power, which can cause oscillation due to increased base-to-collector capacitance and reduced resistance.

One of the main criteria of the presented amplifier is being operational in defined bandwidth, which is limited by the output impedance. To overcome this problem, a transformer is designed; as a first step the output node is transformed to higher impedance with matching components. Then, a transformer is designed such that one of its port is matched to output node, while other end is matched to 50Ω. With mentioned designing technique, the output is properly matched to load throughout the bandwidth, reducing the risk of oscillation. The intermediate node between the stages also has to be concerned, because a mismatch at that node can cause oscillation; to prevent that, the input of the second stage is matched to output of the first stage throughout the bandwidth. Additionally, the parasitic capacitances at intermediate nodes are reduced in layout, by connecting cascode pairs to each other, instead of connecting CE and CB pairs directly.

Figure. 3 presents top view image of the amplifier; total area of the die is 1.42 mm^2. Emitter connections are another problem in amplifier designs that include high number of transistors, because there will be significant amount of inductance variation from top-to-bottom HBTs, which can cause different RF responses from each device. To solve that problem, driver transistor is divided into two groups as $L_{E,2}$ and $L_{E,3}$, in a way that they have separate emitter connections, as demonstrated in Figure. 2 and 3. The inductance variation throughout the transistors is decreased by applying described methodology in the layout.

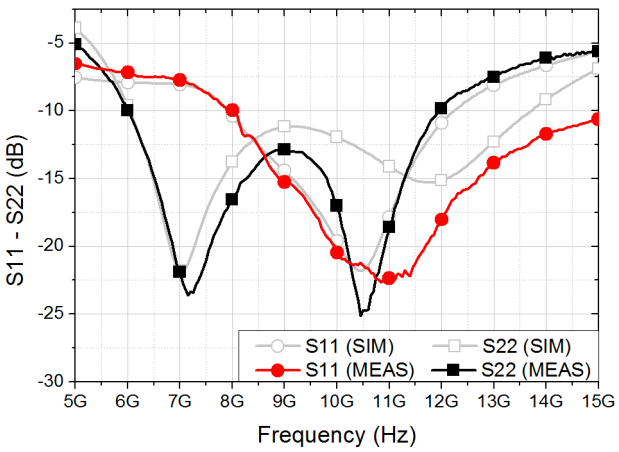

Figure.4. Measured versus schematic matching performance of MPA

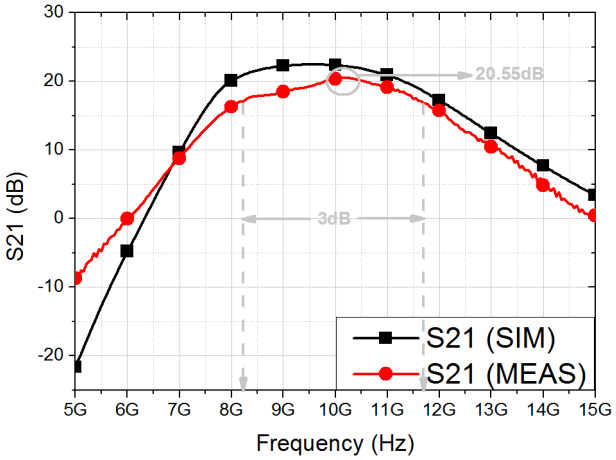

Figure.5. Measured versus schematic gain performance of MPA

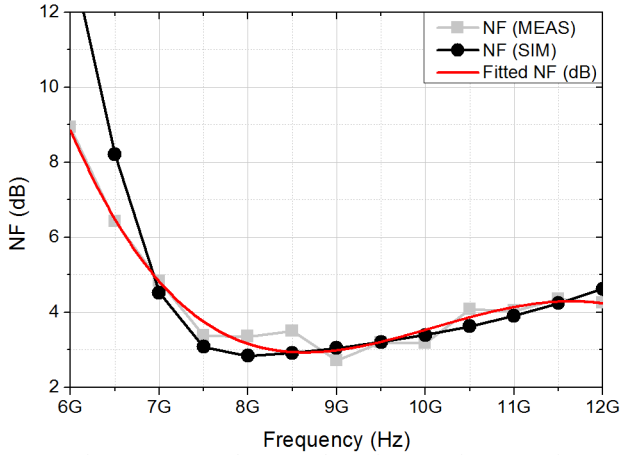

Figure.8. Measured versus schematic NF performance of MPA

III. Measurement Results of MPA

Measurement of S-parameters are done both with R&S ZVL and Agilent 8720ES Network Analyzer. S-parameters are measured with introducing different power levels, which are -30dBm, -10dBm, and 0dBm, to observe the response of the MPA at different input RF powers. Measurements for

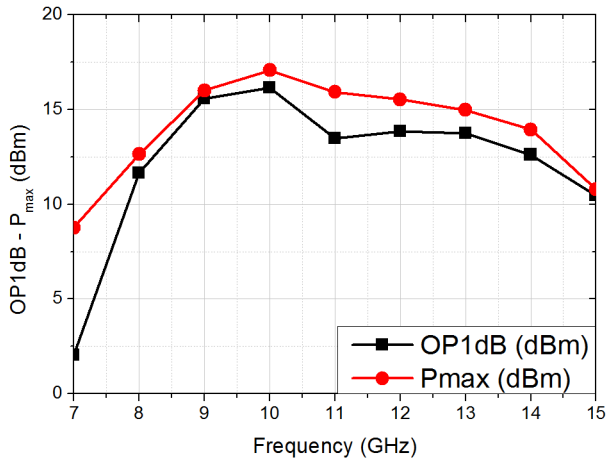

Figure.6. Measured Pmax and OP1dB performance with varied frequency

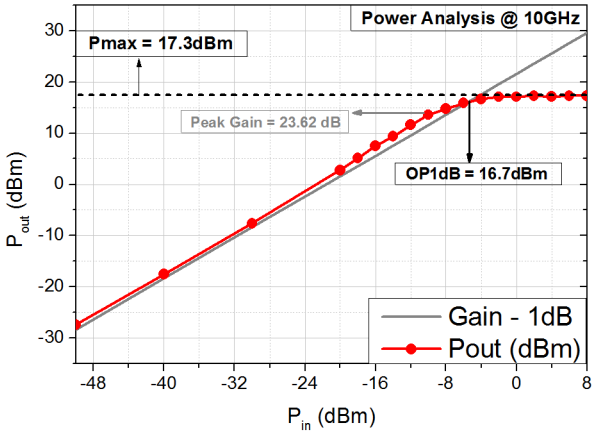

Figure.7. Measured Pmax and OP1dB performance of MPA at 10GHz

output power is done with Agilent 8267D Vector Signal Generator and ESA-E E4407B Spectrum Analyzer. For measuring NF performance of MPA, Agilent ESA-E E4407B Spectrum Analyzer is utilized together with, Agilent 346A Noise Source and Agilent 87405C Pre-amplifier.

Figure. 4 and 5 demonstrate return loss and gain performance of the designed MPA respectively, together with simulation results. One of the major criteria of the design is to being able to operate throughout the bandwidth. As can be seen, presented work has about 7 GHz of return loss bandwidth, while its 3dB gain bandwidth is defined with about 4GHz. MPA has more than 20dB gain, while its peak gain is about 23.6dB. Figure.6 represents output-referred compression point (OP1dB) of MPA as the frequency varies, while Figure.7 demonstrates its OP1dB and maximum output power (Pmax) behavior at 10GHz. Obtaining flat output power is significant, because otherwise the behavior of the whole T/R core module will vary with the frequency, which is not expected; measured MPA achieves approximately 16.7dBm output power throughout the bandwidth, while its peak power is 17.3dBm at 10GHz. In simulations, OP1dB is observed as 20.3dBm and Pmax is founded as 21dBm. At 10GHz, Power Added Efficiency (PAE) is measured as about 10%, with 190mW of DC power consumption.

TABLE.I. COMPARISON TABLE

	Technology	Frequency (GHz)	Gain (dB)	Max. Output Power (dBm)	Power Cons. (mW)
This work	0.25µm SiGe	8 - 13	23.6	17.3	190
[6]	0.18µm SiGe	7.25 - 10.25	21	27	577.5
[8]	0.25µm SiGe	8.5 - 10.5	12.2	21	214.5
[9]	0.35µm SiGe	7 - 18	15	17.5	56
[10]	0.25µm SiGe	8.5 - 10.5	40	21	~300

As mentioned before, the presented work targets an MPA that can also be utilized as an LNA of a SiGe T/R core module. Figure.8 demonstrates the NF performance of the design; when it is considered that the presented work is not the first LNA block in the receiver chain, measured MPA can also be utilized in the receiver path, due to having adequate level of gain and NF performance with adequate bandwidth.

Table.I demonstrates the comparison of MPA with similar works in literature. Primary concern of the presented work is to achieve high output power, high gain, and low NF in defined bandwidth. Therefore, this work is compared not only in terms of output power, but also in terms of bandwidth, and NF performance, which gives a chance to MPA to be used as an LNA. When presented MPA is compared with given references, measured MPA achieves best bandwidth - gain performance with high and flat output power response, and acceptable NF performance.

REFERENCES

[1] Dinc, T.; Zihir, S.; Kalyoncu, I.; Gurbuz, Y., "X-band, high performance, SiGe-heterojunction bipolar transistors-low noise amplifier for phased array radar applications," Microwaves, Antennas & Propagation, IET , vol.6, no.7, pp.768,772, May 16 2012.

[2] Kane, B.C.; Geis, L.A.; Wyatt, M.A.; Copeland, D.G.; Mogensen, J.A., "Smart Phased Array SoCs: A Novel Application for Advanced SiGe HBT BiCMOS Technology," Proceedings of the IEEE , vol.93, no.9, pp.1656,1668, Sept. 2005

[3] Freeman, G.; Jae-Sung Rieh; Jagannathan, B.; Zhijian Yang; Guarin, F.; Joseph, A.; Ahlgren, D., "SiGe HBT performance and reliability trends through fT of 350 GHz," Reliability Physics Symposium Proceedings, 2003. 41st Annual. 2003 IEEE International , vol., no., pp.332,338, 30 March-4 April 2003

[4] van Vliet, F.E.; de Boer, A., "Fully-integrated core chip for X-band phased array T/R modules," in Microwave Symposium Digest, 2004 IEEE MTT-S International , vol.3, no., pp.1753-1756 Vol.3, 6-11 June 2004

[5] Bentini, A.; Ciccognani, W.; Palomba, M.; Palombini, D.; Limiti, E., "High-density mixed signal RF front-end electronics for T-R modules," in Satellite Telecommunications (ESTEL), 2012 IEEE First AESS European Conference on , vol., no., pp.1-6, 2-5 Oct. 2012

[6] Harir, E.; Socher, E., "0.5W X-band SiGe PA with integrated double-tuned transformers," in Microwave Symposium Digest (IMS), 2013 IEEE MTT-S International , vol., no., pp.1-3, 2-7 June 2013

[7] Kalyoncu, I.; Dinc, T.; Gurbuz, Y., "A high-dynamic range SiGe low-noise amplifier for X-band radar applications," in Microwave Integrated Circuits Conference (EuMIC), 2012 7th European , vol., no., pp.385-388, 29-30 Oct. 2012

[8] Kim, H.S.; Kim, K.Y.; Kim, W.Y.; Noh, Y.S.; Yom, I.B.; Oh, I.Y.; Park, C.S., "SiGe MMIC power amplifier with on-chip lineariser for X-band applications," in Electronics Letters , vol.45, no.20, pp.1036-1037, September 24 2009

[9] Bakalski, W.; Vasylyev, A.; Simburger, W.; Thuringer, R.; Wohlmuth, H.-D.; Scholtz, A.L.; Weger, P., "A fully integrated 7-18 GHz power amplifier with on-chip output balun in 75 GHz-fT SiGe-bipolar," in Bipolar/BiCMOS Circuits and Technology Meeting, 2003. Proceedings of the , vol., no., pp.61-64, 28-30 Sept. 2003

[10] Andrews, J.; Cressler, J.D.; Mitchell, M., "A High-Gain, Two-Stage, X-Band SiGe Power Amplifier," in Microwave Symposium, 2007. IEEE/MTT-S International , vol., no., pp.817-820, 3-8 June 2007