# A PFM-Based MWIR DROIC Employing Off-Pixel Fine Conversion of Photocharge to Digital using Integrated Column ADCs

S. Abbasi, A. Galioglu, A. Shafique, O. Ceylan, M. Yazici, Y. Gurbuz
Microsystems Group, Sabanci University, 34956 Tuzla, Istanbul, Turkey; Dept. of Electronics

## ABSTRACT

A 32x32 prototype of a digital readout IC (DROIC) for medium-wave infrared focal plane arrays (MWIR IR-FPAs) is presented. The DROIC employs in-pixel photocurrent to digital conversion based on a pulse frequency modulation (PFM) loop and boasts a novel feature of off-pixel residue conversion using 10-bit column SAR ADCs. The remaining charge at the end of integration in typical PFM based digital pixel sensors is usually wasted. Previous works employing in-pixel extended counting methods make use of extra memory and counters to convert this left-over charge to digital, thereby performing fine conversion of the incident photocurrent. This results in a low quantization noise and hence keeps the readout noise low. However, focal plane arrays (FPAs) with small pixel pitch are constrained in pixel area, which makes it difficult to benefit from in-pixel extended counting circuitry. Thus, in this work, a novel approach to measure the residue outside the pixel using column -parallel SAR ADCs has been proposed. Moreover, a modified version of the conventional PFM based pixel has been designed to help hold the residue charge and buffer it to the column ADC. In addition to the 2D array of pixels, the prototype consists of 32 SAR ADCs, a timing controller block and a memory block to buffer the residue data coming out of the ADCs. The prototype has been designed and fabricated in 90nm CMOS.

**Keywords:** Pulse Modulation Frequency (PFM), Digital Read-out IC (DROIC), Successive Approximation Register (SAR) ADC, Infrared Focal Plane Array (IR-FPA), Direct Injection (DI)

## INTRODUCTION

Successful implementations of digital readout integrated circuits (DROICs) for infrared focal plane arrays (IR-FPAs) have been demonstrated many times in the literature [1-4]. DROICs employing both analog and digital versions of pixel sensors can be found. While analog sensors offer a larger fill factor, digital pixels provide a direct digital output and can significantly improve the charge handling capability [5]. Generally, a DPS either consists of an in-pixel analog-to-digital converter to perform the signal conversion or it is based on a pulse frequency modulation (PFM) loop. While the former applies direct analog-to digital conversion to the pixel, the latter incorporates multiple-self-reset operation using a comparator. PFM-based designs have shown better signal-to-noise ratio (SNR) and dynamic range performance [6]. Recently, several applications for FPAs requiring small pixel pitches in the medium-wave infrared (MWIR) regime have emerged [6-7]. Smaller pixel pitch means that the pixel real estate is constrained in terms of area. In this case, analog pixels are usually preferred due to their superior fill factor. Analog pixels however, have shown poor SNR performance. Traditional DPSs on the other hand can provide significant improvement in the SNR at the cost of increased area, though not at low illumination levels. A need therefore arises to develop DROIC architectures that can achieve acceptable SNR performance at low illumination levels.

Traditional PFM based implementations of DPSs store charge in the digital domain resulting in the charge handling capacity increasing exponentially with respect to pixel area contrary to the linear scaling of conventional analog pixels. These pixels typically consist of a front-end based on a PFM loop, counters and memory.

Such PFM implementations can be found in [8-10] where excellent imaging results are obtained but only at higher illumination levels when the detector current is large. An extended counting technique has been proposed in [5] where the left-over charge on the integration capacitor is computed (converted to digital) in-pixel and then stored in-pixel as

Infrared Technology and Applications XLIII, edited by Bjørn F. Andresen, Gabor F. Fulop, Charles M. Hanson, John L. Miller, Paul R. Norton, Proc. of SPIE Vol. 10177, 101771Z · © 2017 SPIE
CCC code: 0277-786X/17/$18 · doi: 10.1117/12.2262451

well. This computation is carried out by counting the number of clocks from the time when integration is stopped till the next auto-reset. The additional bits obtained from this computation are added to the pixel count. The drawback of this technique is the increase in pixel area. The design in [5] was for a 30um pixel pitch. With smaller pixel sizes, such as 15um pitch the required additional circuitry for extended counting cannot fit within the pixel area.

In this brief, the idea of residue measurement to improve SNR has been exploited and a DROIC employing off-pixel residue measurement has been designed and fabricated. A digital pixel which is a modified version of the conventional PFM architecture has been proposed along with a method to measure residue outside the pixel. A prototype has been developed as a proof of concept. The idea is to exploit the superior SNR performance of digital pixels and at the same time keep the pixel size small by delegating the residue measurement job to an off-pixel ADC. SNR has been measured and reported.

The paper is organized as follows: Section 2 describes a conventional PFM based pixel and provides background on the extended counting technique reported in [5], Section 3 describes the architecture of the proposed DROIC. Measurement results are shown in Section 4 and finally the concluding remarks are provided in Section 5.

## DROIC IMPLEMENTATION

### Conventional PFM based Pixel

Schematic of the pixel front-end is shown in Figure 1. This is a conventional pixel architecture based on a PFM loop. Detector current (or photocurrent) is imitated by the current supplied by current source device M1 and direct injection (DI) device M2. This current fills up the capacitor C at a speed determined by magnitude of the current. Once the voltage at node A exceeds Vref, the comparator switches to high and M3 turns on. This resets the capacitor to 0V and the integration operation repeats. The 4 inverters in the loop create delay to ensure that the capacitor gets enough time to discharge completely.

Every time the comparator switches, a short pulse is generated at node P. This is what we call the PFM signal. This signal is fed to a counter as its clock. The integration operation continues till a manual reset signal turns M4 on. When this happens, the capacitor is discharged to 0V and at this point the counter holds the digital value corresponding to the integration time and eventually the number of charges collected. This count value is transferred to a memory in the form of a register. Period of this reset signal defines the duration of integration phase.

Figure 2 illustrates the operation of the pixel front-end. As shown, the residue, which corresponds to the remaining charge on the capacitor at the end of the integration period, is essentially wasted. The method proposed in [2] makes use of this left-over charge to improve the overall SNR of such a DPS for scenarios where detector illumination is low and hence the current is low. Next section briefs the extended counting technique.

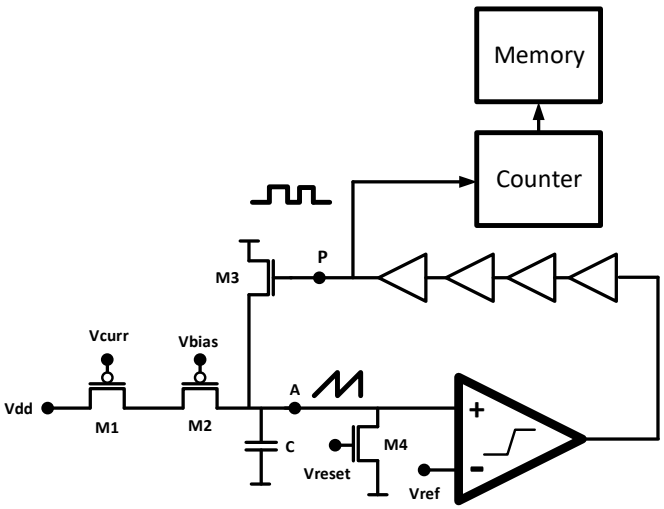


Figure 1. Schematic of a conventional PFM-based digital pixel

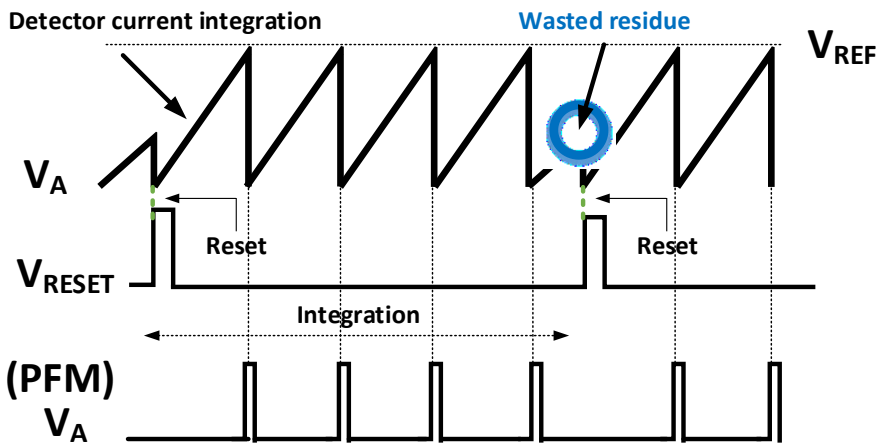


Figure 2. Timing and operation of a conventional digital pixel

**Pixel based on Extended Counting**

In extended counting, the integration phase is the same as in a conventional PFM-based DPS as explained in the previous section. However, another phase is added to the pixel's operation where value of the left-over charge on the integration capacitor is calculated using the same counter but with a different clock which is much faster than the PFM signal [5]. This phase is termed as the fine quantization phase which makes integration the coarse quantization phase. This phenomenon is same as seen in a sub-ranging ADC where the signal range is reduced after a coarse quantization step and then further conversion is performed on the remaining signal. Therefore, during fine quantization, conversion of this left-over charge (or voltage) is carried out by using the same counter which basically computes the time that is required to trigger the comparator one more time. The residue enable signal shown in Fig. 3 is responsible for switching between integration and residue phases.

Integration of the photocurrent onto the integration capacitor can continue at this phase even though integration has logically ended. This counting is done till the next auto-reset event occurs at which point the residue data is transferred to a register. An ALU then performs the computation described in [2] on the residue value obtained to get the final output.

This technique produces excellent results, especially at low illumination levels where the improvement in SNR is significant. However, the additional logic required to perform residue computation and the extra storage registers increase the area requirement of the pixel. As mentioned before, FPAs having pixel pitches down to 15um won't allow adding this much real estate to the pixel electronics.

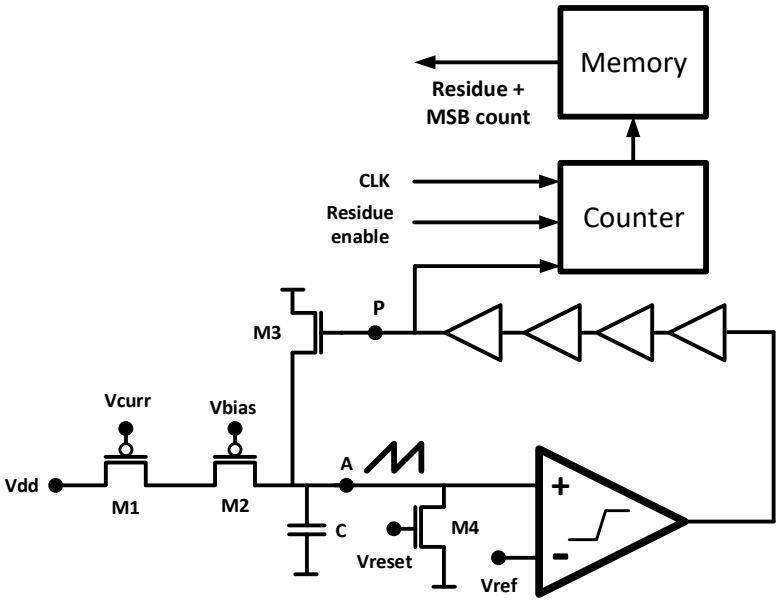


Figure 3. . Pixel architecture incorporating extended counting as proposed in [5]

## PROPOSED ARCHITECTURE

Given the area constraints of a 15umx15um size pixel, using the extended counting technique for measuring residue does not seem feasible. To this end, a method is proposed where a modified PFM-based pixel architecture is used for the front-end whereas residue measurement is performed off-pixel using a column ADC. MSB counting is carried out the same way as in a conventional architectural. From the experience of a previous design, a 5-bit MSB counter seems appropriate given the area constraints.

The ADC performs a direct conversion on the residue voltage and the digital value obtained is simply appended to the MSB count value. From computational point of view, this method has a certain degree of simplicity compared to the extended counting method because residue bits don't have to go through any computations before being combined with the final output. Moreover, an ALU is also not needed. However, accuracy of the measured residue in the proposed method is dependent on the performance of the ADC. Moreover, with several ADCs now being used, power consumption of each ADC will need to be below a tight specification.

Major modifications to the pixel include the addition of a source follower and the use of a power efficient self-biased differential amplifier in place of the comparator. In Figure 4 part of the full pixel front-end has been shown with the proposed modifications highlighted.

Before discussing the proposed architectural modifications of the DPS let's look at the operation of the pixel in this case. As shown in Figure 5, the instant at which integration is stopped the residue charge (or voltage) is sampled by the ADC. In a design with a full 2D array, the residue must be held on the integration capacitor before reset is issued. This will require minor changes in the design of the pixel front-end.

A block diagram of the proposed DROIC is depicted in Fig. 6. The core of the DROIC consists of a 32 × 32 array of digital pixel sensors (DPSs), single-ended to differential converters (SDCs) and column SAR ADCs. Buffered analog residue outputs from the pixels in a column are connected to a common signal line feeding the SDC, which produces a differential output with appropriate common-mode to drive the SAR ADC. The 10-bit digital output from the ADC forms the LSB part of the final output. As far as the MSB bits are concerned, they are read out on 5-bit wide row-common buses. This 5-bit data, from the counter registers, is read and fed to the row mux. Row and column selection

signals, row_sel and col_sel, from the control unit determine which pixel has been selected for data read. In addition to the control signals for readout, timing signals for pixel and SAR ADC operation are also generated by the control unit.

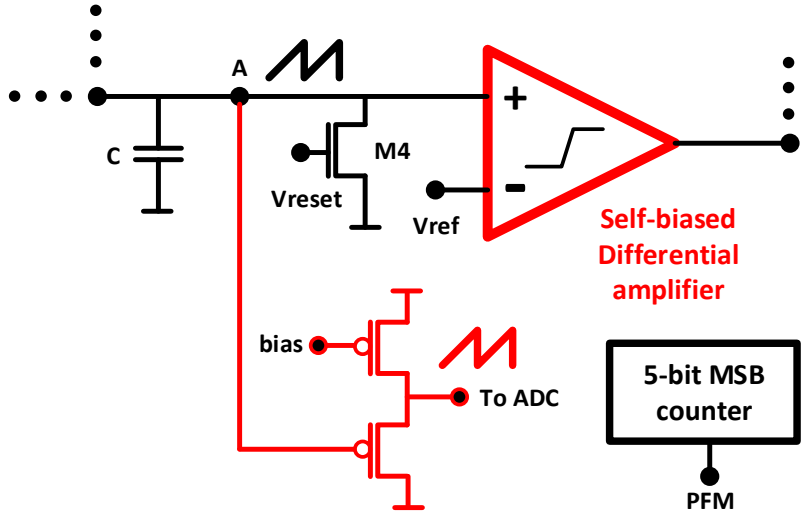


Figure 4. Proposed modification to a conventional PFM-based digital pixel

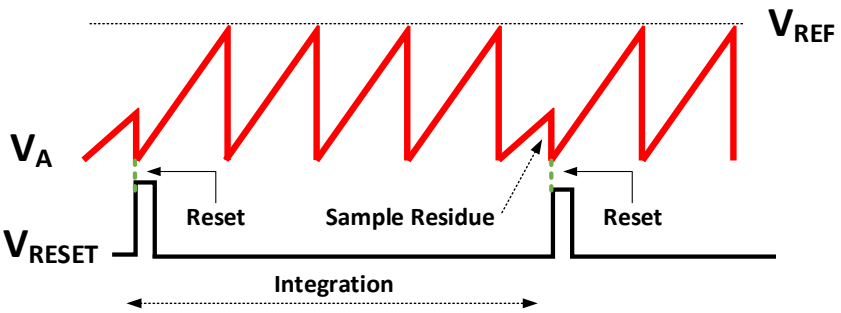


Figure 5. Timing operation of propsed pixel

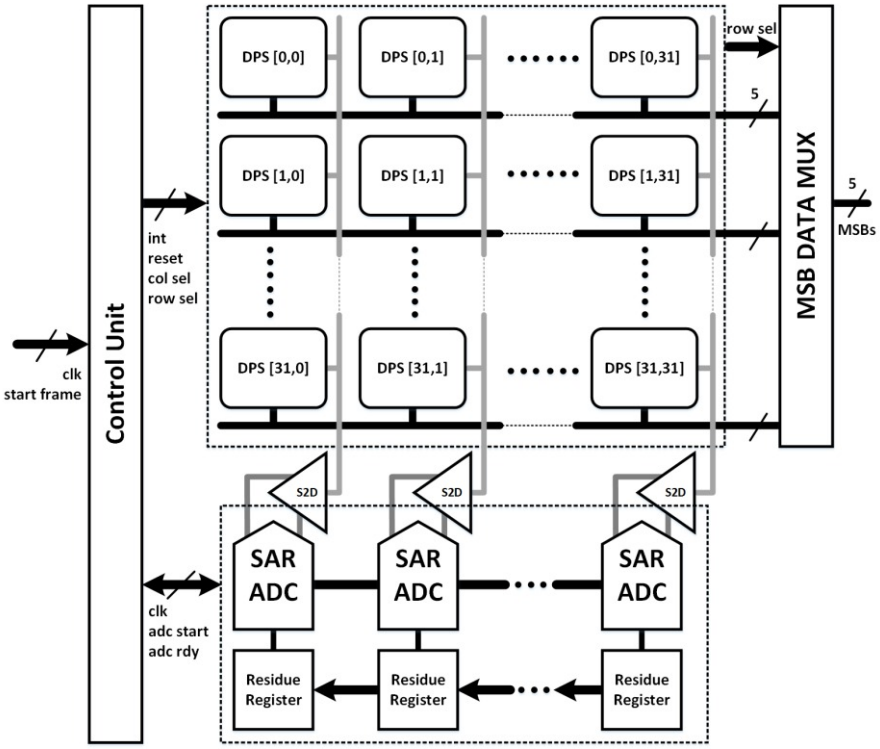


Fig. 6 Array Architecture

**Buffer**

Delegating the pixel measurement job to an off-pixel circuit requires proper buffering at node A because this node is very sensitive and can be easily loaded by the ADC. This is done by adding a source follower inside the pixel as shown in Figure 4. Source follower is a very simple and concise circuit that can provide decent buffering performance and doesn't add too much area. Adding the source follower does result in a level-shift of the integration (saw-tooth) waveform though, but this is something that can be accounted for by adjusting ADC's reference voltage.

**Comparator**

Comparator design doesn't have a direct impact on the performance of a given residue measurement method but if off-pixel ADCs will add to the overall power consumption, a power efficient pixel design is needed. Furthermore, it is shown in [5] that power consumption of a PFM-based pixel is dominated by the dynamic elements in the PFM loop which include the inverters and comparator. Therefore, besides the addition of a source follower in the modified pixel, a new comparator in the form of a power efficient self-biased differential amplifier has been added. It is shown in Fig. 7. The amplifier works as a pseudo comparator. It magnifies the difference between the voltage on the integration node and reference voltage Vref. This difference voltage then drives the feedback inverters to generate the PFM signal. Figure 6 shows the schematic of the designed amplifier. The self-biased topology also helps reduce a bias voltage from the pixel circuit.

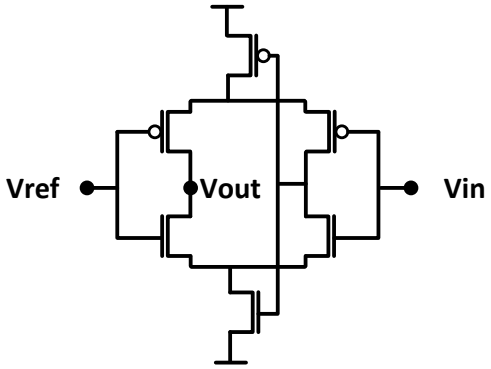


Figure 7. Self-biased power efficient differential amplifier as Pseudo Comparator

## MEASUREMENT RESULTS

As discussed earlier, the overall noise reduces because of the reduced quantization noise owing to the residue conversion. To demonstrate this, SNR measurements have been carried out. The MSB and residue bits are read out at a fixed current for various integration times. 128 samples (15-bit output) of all pixels are taken for each integration time. Average of these samples forms the signal part of the SNR expression, whereas the noise is found by calculating the variance. The expression below has been used

The SNR has been plotted against collected charge in Fig. 8. Once again the integration time has been varied keeping the current constant. At the full-well capacity of 2.4Me-, the SNR is 64 dB. The SNR would have been much worse without the residue information being appended to the final output.

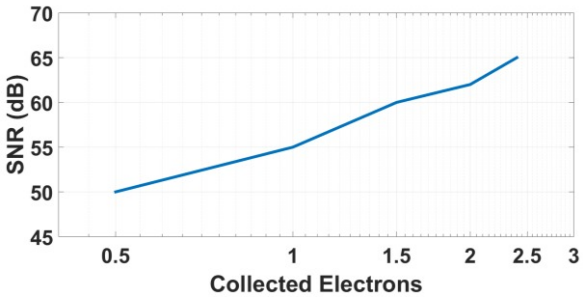


Figure 8. Measured SNR

## CONCLUSION

A prototype of a DROIC, intended for small pixel pitch MWIR FPAs, employing off-pixel residue measurement has been demonstrated. The developed chip, comprising a 32x32 array of pixels and column ADCs, has been used to measure SNR. And as reported, SNR numbers breaking through the usual limitation at low illumination levels have been observed. Hence the proposed approach achieves the intended improvement in SNR performance by combining residue charge with the MSB count and at the same time allows concise pixel size by allowing off-pixel residue measurement.

## ACKNOWLEDGEMENT

The authors would like to thank TUBITAK, The Scientific and Technological Research Council of Turkey, for funding this project. The work was carried out under grant 113E598.

## REFERENCES


[1] S. D. Gunapala et al., "Demonstration of Megapixel Dual-Band QWIP Focal Plane Array," in IEEE Journal of Quantum Electronics, vol. 46, no. 2, pp. 285-293, Feb. 2010.

[2] L. E. Marchese et al., "A 0.1 Megapixel THz camera with 17 degree field of view for large area single shot imaging," 2014 39th International Conference on Infrared, Millimeter, and Terahertz waves (IRMMW-THz), Tucson, AZ, 2014, pp. 1-2.

[3] L. c. Hao, R. j. Ding, J. l. Zhang, A. b. Huang and H. l. Chen, "A high-performance readout circuit (ROIC) for VLWIR FPAs with novel current mode background suppression," Proceedings of 2012 International Conference on Measurement, Information and Control, Harbin, 2012, pp. 869-873.

[4] H. S. Gupta, A. S. K. Kumar, M. S. Baghini, S. Chakrabarti and D. K. Sharma, "Design of High-Precision ROIC for Quantum Dot Infrared Photodetector," in IEEE Photonics Technology Letters, vol. 28, no. 15, pp. 1673-1676, Aug.1, 1 2016.

[5] Kayahan, H., Yazici, M., Ceylan, O., Gurbuz Y., "A new digital readout integrated circuit (DROIC) with pixel parallel A/D conversion and reduced quantization noise," Infrared Physics and Technology Journal, pp. 125-132 (2013).

[6] L. Cheng and G. Y. Tian, "Surface crack detection for carbon fiber reinforced plastic (CFRP) materials using pulsed eddy current thermography," IEEE Sensors J., vol. 11, no. 12, pp. 3261–3268, Dec. 2011.

[7] S. Yin, H. Gao and O. Kaynak, "Data-Driven Control and Process Monitoring for Industrial Applications—Part I," in IEEE Transactions on Industrial Electronics, vol. 61, no. 11, pp. 6356-6359, Nov. 2014.

[8] Bisotto, S., de Borniol, E., Mollard, L., Guellec, F., Peizerat, A., Tchagaspanian, M., et al "A 25 lm pitch LWIR staring focal plane array with pixel-level 15-bit ADC ROIC achieving 2 mK NETD," Electro-Optical Infrared Syst.: Technol. Appl. VII 7834. Proc. SPIE (2010).

[9] Guellec, F., Peizerat, A., Tchagaspanian, M., de Borniol, E., Bisotto, S., Mollard, L., et al "A 25 lm pitch LWIR focal plane array with pixel-level 15-bit ADC providing high well capacity and targeting 2 mK NETD," Infrared Technol. Appl. XXXVI, Pts 1 and 2 7660. Proc. SPIE (2010).

[10] Tyrrell, G., Anderson, K., Baker, J., Berger, R., Brown, M., Colonero, C.,et al "Time delay integration and in-pixel spatiotemporal filtering using a nanoscale digital CMOS focal plane readout," IEEE Trans. Electron Devices 56 2516–2523 (2009).