SiGe BiCMOS 4-bit Phase Shifter and T/R Module for X-band Phased Arrays

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SiGe BiCMOS 4-bit Phase Shifter and
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SiGe BiCMOS 4-bit Phase Shifter and T/R Module for X-band Phased Arrays

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Abstract

Current phased array RADAR (RAdio Detection And Ranging) systems conventionally employ transmit/receive (T/R) modules implemented in III-V technologies (such as GaAs and InP) and their usage is mainly restricted to military applications. The next generation phased array systems require thousands of T/R modules with lower cost, size and power consumption. Advances in SiGe BiCMOS process technologies make it a viable option for next generation phased array systems, especially for commercial applications. In the light of these trends, this thesis presents the design of a 4-bit SiGe X-band (8-12 GHz) passive phase shifter and the complete SiGe X-band T/R module, realized in IHP 0.25-μm SiGe BiCMOS process.

The phase shifter is based on switched filter topology, utilizing a low-pass Π network for phase shift state and isolated NMOS transistors are used for bypass state. It is composed of 22°, 45° and 90° bits and the 180° bit is realized by cascading two 90° bits. The return loss of each bit is better than 10 dB, the overall phase shifter has an average of 14 dB insertion loss. Minimum RMS phase error of 3° is obtained at 10.1 GHz. RMS phase error is better than 11° at 9.2-10.8 GHz band. The overall phase shifter occupies 0.9 mm^2 area, has no DC power consumption and achieves input-referred 1-dB compression point of 15 dBm.

The integration of a compact T/R module using the 4-bit phase shifter and the previously developed building blocks such as low-noise amplifier (LNA), power amplifier (PA) and single-pole double-throw (SPDT) switches is presented. The developed SiGe X-band T/R module occupies only 4.9 mm^2 chip area. In 9-10 GHz band T/R module achieves a measured gain of 10-11.5 dB in receiver mode and 10.7-12 dB gain in transmitter mode. A minimum RMS phase error of 5° is achieved at 9 GHz. Noise figure in receiver mode is measured between 4-6 dB while the IIP_3 is receive mode is measured as -10.5 dB. Output power at 1-dB compression in transmit mode is 16 dBm. These parameters are achieved with a power consumption of 285 mW.

X-band Faz Dizinleri için SiGe BiCMOS 4-bit Faz Kaydırıcı ve Alıcı/Verici Modülü

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Özet

Günümüzün faz dizinli radyo algılama ve menzil tayini (RADAR) sistemleri, geleneksel olarak GaAs ve InP gibi III-V teknolojileriyle geliştirilen alıcı/verici (T/R) modülleriyle gerçeklenir. Bu nedenle uygulama alanları daha çok askeri uygulamalarla sınırlıdır. Yeni nesil faz dizinli sistemler düşük maliyetli, küçük alanlı ve az güç harcayan binlerce alıcı/verici modülüne gereksinim duymaktadır. SiGe BiCMOS teknolojisindeki ilerlemeler sayesinde bu teknoloji yeni nesil faz dizinli sistemler için, özellikle de ticari uygulamalar için geçerli bir opsiyon olarak ortaya çıkmıştır. Bu trendlerin ışığında, bu tezde, IHP'nin 0.25 μm SiGe BiCMOS teknolojisi ile gerçeklenen ve X-bandında (8-12 GHz) çalışan 4-bit pasif faz kaydırıcı ve komple tamamlanmış alıcı/verici modülünün tasarımı ve gerçeklenmesi sunulmuştur.

Faz kaydırıcı, anahtarlamalı filtre topolojisine dayanmaktadır; alçak bant geçiren Π tipi süzgeç faz kaydırmak için kullanılırken izole edilmiş NMOS tranzistörler bu süzgeçi baypas etmek için kullanılmıştır. Faz kaydırıcının 22°, 45° ve 90° blokları bu topolojiyle tasarlanmış ve 180° bloğu iki kademli 90° bloğu olarak gerçeklenmiştir. Tüm blokların geri dönüş kaybı 10 dB'den iyidir ve tüm faz kaydırıcının ortalama ekleme kaybı 14 dB'dir. 3°'lik en düşük RMS (etkin değer) faz hatası 10.1 GHz'de elde edilmiştir. RMS faz hatası 9.2-10.8 GHz bandında 11°'nin altındadır. Faz kaydırıcı toplam 0.9 mm^2 kırmık alanı kullanır, DC güç tüketimi yoktur ve giriş 1-dB sıkışma gücü 15 dBm'dir.

4-bit faz kaydıcırı ve daha önce tasarlanan düşük gürültülü kuvvetlendirici (LNA), yüksek güç kuvvetlendiricisi (PA) ve tek giriş çift çıkışlı (SPDT) anahtar bloklarını kullanarak tüm alıcı/verici modülünün entegrasyonunun gerçekleştirilmsi sunulmuştur. Geliştirilen SiGe X-band alıcı/verici modülü sadece 4.9 mm^2 kırmık alanı kullanır. 9-10 GHz bandında, modülün alıcı modundaki kazancı 10-11.5 dB ve verici modundaki kazancı 10.7-12 dB arasında ölçülmüştür. 9 GHz frekansında 5°'lik bir en düşük RMS faz hatası ölçülmüştür. Alıcı modundaki gürültü sayısı 4-6 dB arasındadır. Yine alıcı modunda, girişe endeksli üçüncü derece harmoniğin kesişim noktası -10.5 dBm'dir. Verici modunda 1-dB sıkışmış çıkış gücü 16 dBm olarak ölçülmüştür. Bu parametrelere 285 mW DC güç tüketimi ile ulaşılmıştır.

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List of Abbreviations

AF	Array Factor
AM	Amplitude Modulation
BV_{CEO}	Collector-Emitter Breakdown Voltage
BV_{CBO}	Collector-Base Breakdown Voltage
CB	Common-Base
CCB	Constant Current Biasing
CE	Common-Emitter
CVB	Constant Voltage Biasing
DBF	Digital Beam Forming
DE	Drain Efficiency
DF	Direction Finding
EIRP	Equivalent Isotropically Radiated Power
FM	Frequency Modulation
FOM	Figure-of-Merit
GaAs	Gallium-Arsenide
HP	High Pass
IC	Integrated Circuit
IF	Intermediate Frequency
IL	Insertion Loss
InP	Indium phosphide
iNMOS	Isolated NMOS
LNA	Low Noise Amplifier
LO	Local Oscillator
LP	Low Pass
MEMS	Microelectromechanical System
MIM	Metal-Insulator-Metal
MMIC	Monolithic Microwave Integrated Circuits
mm-Wave	Millimeter-wave
MOS	Metal-Oxide-Semiconductor
MtM	More than Moore
OAE	Overall Efficiency
PA	Power Amplifier
PAE	Power-Added-Efficiency
PAWS	Phased Array Warning System
PS	Phase Shifter
QAM	Quadrature Amplitude Modulation
RADAR	Radio Detecting And Ranging
RF	Radio Frequency
RMS	Root Mean Square
RX	Receiver
SiGe	Silicon-Germanium
SPDT	Single-Pole Double-Throw
T/R	Transmit/Receive
TX	Transmitter
VGA	Variable Gain Amplifier

1 Introduction

1.1 A Brief History of Radar

Radar (RAdio Detection And Ranging) is one of rare technologies, the invention of which cannot be easily attributed to a single scientist. Maxwell's establishment of electromagnetic theory, Hertz's discovery of electromagnetic waves, Tesla's ideas and experiments on wireless communication and Marconi's first long distance transmission of radio frequency signals were the main significant steps toward the radar technology. But, it was Christian Hulsmeyer's development of the "telemobiloscope" in 1904, that set the mark as the first practical radar in history, which was intended to be used for maritime traffic monitoring on poor weather conditions [6].

Due to its military applications, radars become popular during and after World War II. Development of klystrons, magnetrons, horn antennas and parabolic reflectors are followed by first mechanically steerable radar systems. Mechanical steering helps to increase the visible area of the radar, achieving hundred scans per minute. With advances in every field of electronics engineering, mechanical steering is replaced with electronically scanned arrays, more commonly known as "phased arrays", achieving hundred scans per second [7].

1.2 Phased Array Radars

Even today, phased array radar technology is mainly driven by military applications such as missile guidance and defense, surface radars and satellite-based radars. However, there are emerging civilian applications such as automotive radars, weather monitoring and radio astronomy. Fig. 1 shows various phased array radar examples: (a) AN/TPS-59 is a transportable air search radar and it does electronic steering in altitude and mechanical steering in azimuth [8]. (b) AN/FPS-123 is a solid-state phased array radar system (SSPARS) used for ballistic missile warning [9] (c) Active phased array multifunction radar (APAR) has the capability of search-and-track of low altitude and air targets as well as multiple missile guidance at the same time [10]. (d) SKA (square kilometer array) used for radio astronomy [11]. (e) WSR-88D Doppler weather radar [12]. (f) LRR3 automotive radar for driver assistance systems [13].

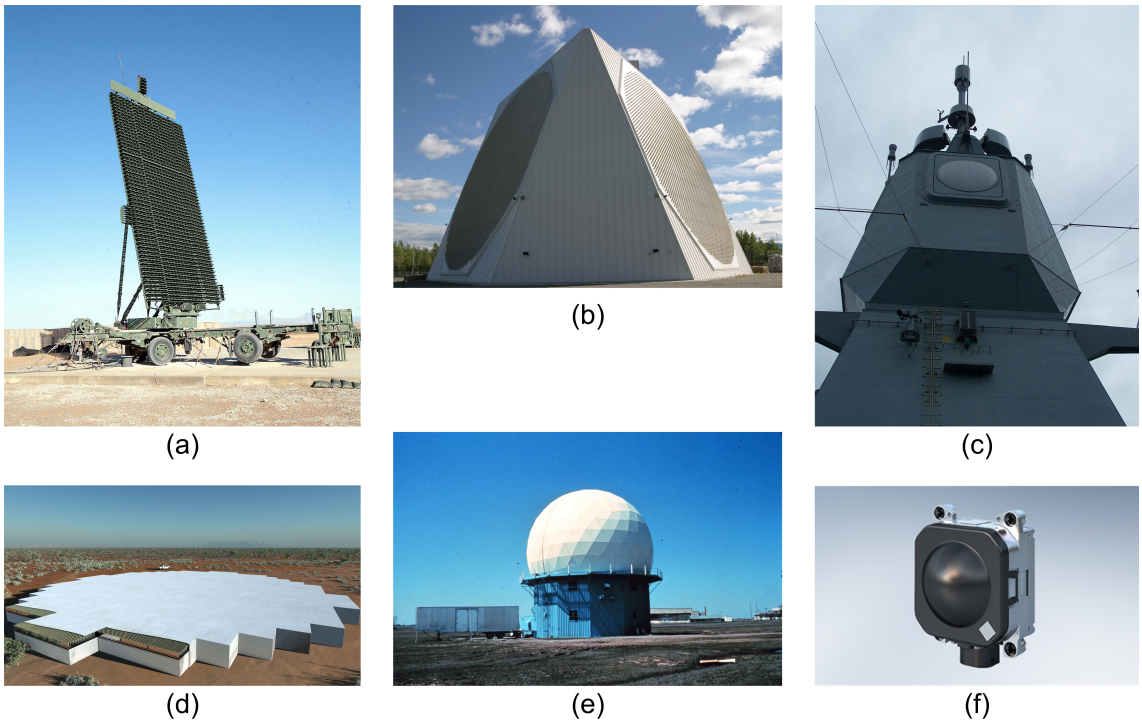

Figure 1: Various military (a-c) and commercial (d-f) phased array radars

The advantage of a phased array over a conventional radar is its ability to steer the beam without any mechanical systems. In this way, radar systems becomes more reliable (mechanical errors are eliminated) and beam positioning becomes faster, so higher scan rates are achieved. Phased arrays also provide multi-mode and multi-target operation as well as increased data rates if they are used in a communication application.

In phased arrays, spacial resolution depends on the number of radiating elements, unlike conventional radars. These radiating elements are generally followed by transmit/receive (T/R) modules to control amplitude and phase of signal at each radiating element. These modules are generally realized using separate GaAs or InP monolithic microwave integrated circuits (MMIC) and they are widely used in military applications. Their size and cost can pose a challenging problem for commercial applications of phased arrays [14]. The future in phased array technology is to integrate as much RF front-end blocks as possible into a single solid-state chip, with the ultimate goal of wafer scale phased arrays [15].

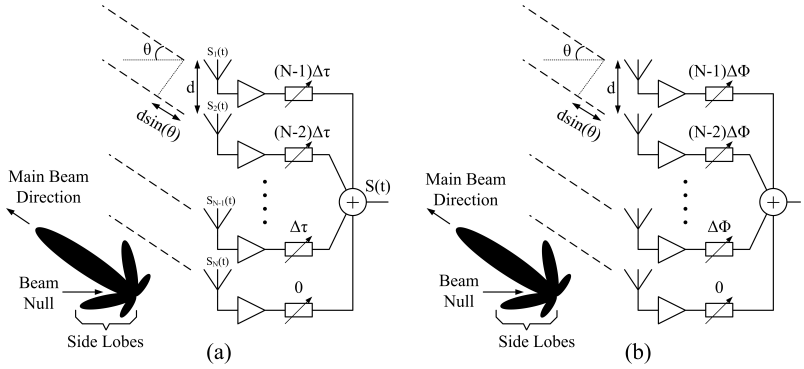

Figure 2: Basic timed-array receiver blcok diagram.

1.3 Phased Array Operating Principles

1.3.1 Time Delay vs Phase Shift

Depending on the control mechanism, arrays can be split into two: Timed-arrays (Fig. 2) and phased arrays (Fig.3). Now, let's have a closer look at the operation principles of these two systems.

Let's assume a sinusoidal electromagnetic plane wave at frequency ω and amplitude A is incident on the antenna array at an angle of θ to the normal direction. The beam will experience a time delay of $\frac{d\sin\theta}{c}$ between adjacent antennas, where d is the spacing between antennas and c is the speed of light in free space. Then the signal received by the i^{th} antenna can be written as,

$$S_i(t) = A\cos\left(\omega t - \omega(i-1)\frac{d\sin\theta}{c}\right) \tag{1}$$

These signals received by the antenna can be added up coherently by adjusting the time delay elements in each receiver channel properly. In this case, the time delay of the i^{th} receiver channel is set to $(N-i)\Delta\tau$. So, the signal after the combiner becomes,

$$S(t) = \sum_{i=1}^{N} GA\cos\left(\omega t - \omega(i-1)\frac{d\sin\theta}{c} - \omega(N-i)\Delta\tau\right) \tag{2}$$

where G is the receiver gain of a single channel. If the incremental time delay in each channel is chosen as,

$$\Delta\tau = \frac{d\sin\theta}{c} \tag{3}$$

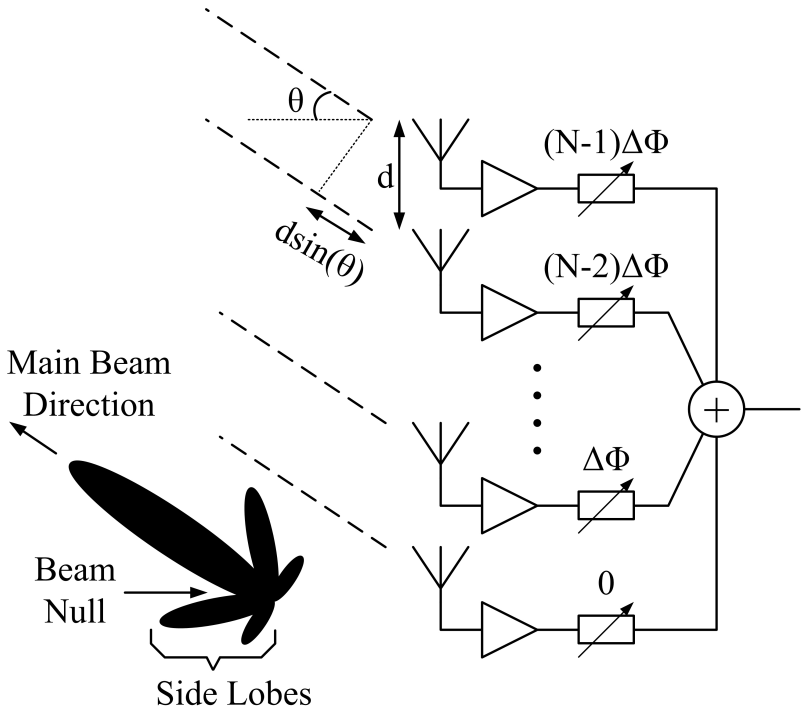

Figure 3: Basic phased-array receiver blcok diagram.

then the combined signal becomes,

$$S(t) = \sum_{i=1}^{N} GA \cos\left(\omega t + \omega \frac{d \sin\theta}{c}(1-N)\right) \tag{4}$$

where the terms with dummy random variable i cancel each other out, which implies that with the value of $\Delta\tau = \frac{d\sin\theta}{c}$ the received signals are coherently added in θ direction while incoherently added in other directions, resulting in a beam shape shown in Fig. 2. So, by controlling the time delay in each receiver channel using variable delay elements, the main beam direction can be controlled.

Actually, for a timed array, the incident signal does not have to be at a single frequency, it may consists of many sinusoids at different frequencies. The time delay experienced by the beam between antenna elements, given in (3) is independent of signal frequency. This means that, if each receiver has time delay elements, then all frequency components of the incident signal from θ direction can be coherently added. Therefore, timed array systems enables wideband operation.

However, time delay elements are hard to implement as integrated circuits, especially for silicon MMICs. Therefore, for narrowband systems, variable time delay is approximated by variable phase shift. This is called the delay-phase approxima-

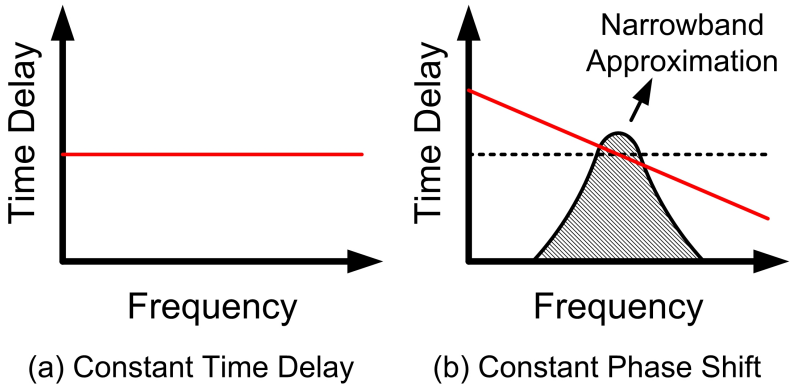

Figure 4: Narrowband phase shift approximation for time delay

tion. In a phased array system, as shown in Fig. 3, the required phase shift in each channel becomes (5), where λ is the wavelength.

$$\Delta\phi = \omega\Delta\tau = \omega\frac{d\sin\theta}{c} = 2\pi\frac{d\sin\theta}{\lambda} \tag{5}$$

In a phased array system, where each receiver channel includes variable phase shifters instead of variable time delay elements, the instantaneous bandwidth of the signal is limited. Theoretically, as shown in Fig. 4, a constant phase shift vs. frequency means larger time delay at lower frequencies and smaller time delay at higher frequencies. Therefore, phased array systems does not provide wideband operation and can only be used in narrawband systems. Yet, phased arrays are nowadays dominant over timed arrays and the reason is that integrated true time delay elements are challenging and area consuming. For the rest of the thesis, phased arrays will be focused.

1.3.2 Beam Steering and Array Factor

As stated in previous section, in a phased array, by adjusting the phase shift (and amplitude if desired) in each receiver/transmitter channel, the main beam direction can be steered. Eq. (5) can be rearranged as

$$\theta = \sin^{-1}\left(\frac{\lambda}{2\pi d}\Delta\phi\right) \tag{6}$$

where θ is the angle between main beam direction and the array normal (same as in Fig. 2 and Fig. 3) and $\Delta\phi$ is the incremental phase shift between each channel. So, at a given wavelength, the beam direction is only a function of spacing between

antenna elements and incremental phase shift in each channel. As the antenna spacing gets larger, the beam width gets smaller, which increases the directivity of the array. However increasing antenna spacing too much brings grating lobes which makes the array more susceptible to interferer signals. Therefore, it is generally chosen close to $\lambda/2$ to achieve highest directivity without any grating lobes.

The radiation pattern of an array is the multiplication of antenna element factor and array factor (AF) [16]. Normalized array factor of a N-element array is given as

$$AF = \frac{\sin\left(N\frac{\psi}{2}\right)}{N\sin\left(\frac{\psi}{2}\right)} \tag{7}$$

where $\psi = \frac{2\pi}{\lambda}d\sin(\theta) + \phi$. Fig. 5 shows the normalized array factor of a phased arary with $\lambda/2$ spacing between antennas for various number of elements. The main beam is steered from 30° to 150° (or from $\theta = -60°$ to $\theta = +60°$) with 15° steps. It is seen that beamwidth is not only a function of antenna spacing but also number of antennas and the beamwidth decreases as the number of elements are increased. Also, the beamwidth is smallest for broadside (90° radiation angle or $\theta = 0°$) and increases as the beam is steered to the sides. So, in order to obtain a narrower beam and therefore get a better spacial resolution, array size must be chosen as large as possible. This aspect is one of the motivations for silicon based, small foot-print, fully-integrated transmit/receive blocks that enables thousands of antenna elements feasible.

1.3.3 Phased Array as a Receiver

A phased array does not only steer the beam by electronically controlling the phase shift in each receiver/transmitter channel, it does more than that. Going back to Eq. (4), it is seen that the *voltages* at the output of each receiver channel is coherently added and the combined signal voltage is n times increased with respect to a single channel, therefore the combined received signal *power* is increased n^2 times. This observation can be rewritten as

$$S_{out} = n^2 G S_{in} \tag{8}$$

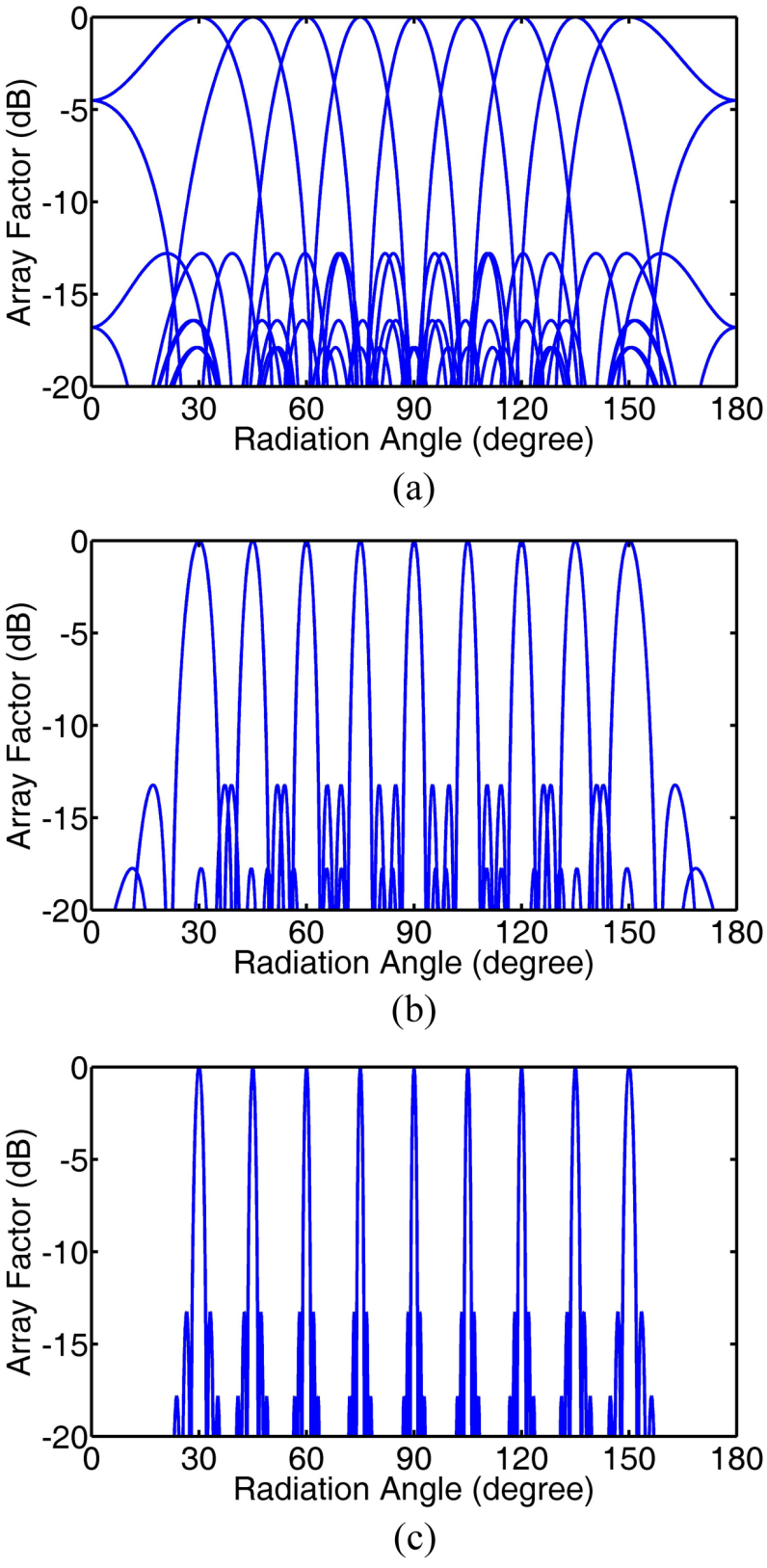

Figure 5: Normalized array pattern of a linear array with $\lambda/2$ spacing for (a) N=8 (b) N=32 (c) N=100 antenna elements

where S_{in} is the input power in each receiver channel, S_{out} is the combined signal power at receiver output, G is the power gain of each receiver channel and n is the number of channels or antenna elements.

Assuming noise contributions of different receiver channels are uncorrelated, their signal powers (not voltages) are added at the receiver output, which can be written as

$$N_{out} = nG\,(N_{ant} + N_{rec}) \tag{9}$$

where N_{out} is the combined noise power at the receiver output, N_{ant} is the noise power feeding from antenna and N_{rec} is the noise power added by each receiver channel. Comparing (8) and (9) shows that, output SNR of a phased array linearly scales with number of antenna elements, n. For a thousand element phased array, an SNR improvement of $10\log(1000) = 30$ dB can be achieved with respect to a single receiver channel.

Furthermore, a phased array receiver can be used for nulling out interferences in the environment by adjusting phase and especially weighting amplitudes of signals received from each receiver channel so that beam nulls point at the direction of interference [17]. With these advantages, phased arrays provide improved sensitivity in receiver end.

1.3.4 Phased Array as a Transmitter

The coherent addition of signals in phased arrays not only directs the beam in a desired direction but also increases the radiated power in the main beam direction [18]. Assuming each antenna radiates P watt power in all directions (antenna element pattern is omitted), the effective isotropic radiated power (EIRP) of an N-element phased array in the main beam direction becomes N^2P watt. So, there is a $20\log(N)$ dB improvement in radiated power for a phased array transmitter with respect to a single transmitter channel. Hence, in order to achieve high radiated powers, a large number of moderate power transmitters can be used instead of a single, large power amplifier. This property of phased array transmitters are especially useful in silicon based phased arrays where the available output power from power amplifiers are limited with low breakdown voltage devices.

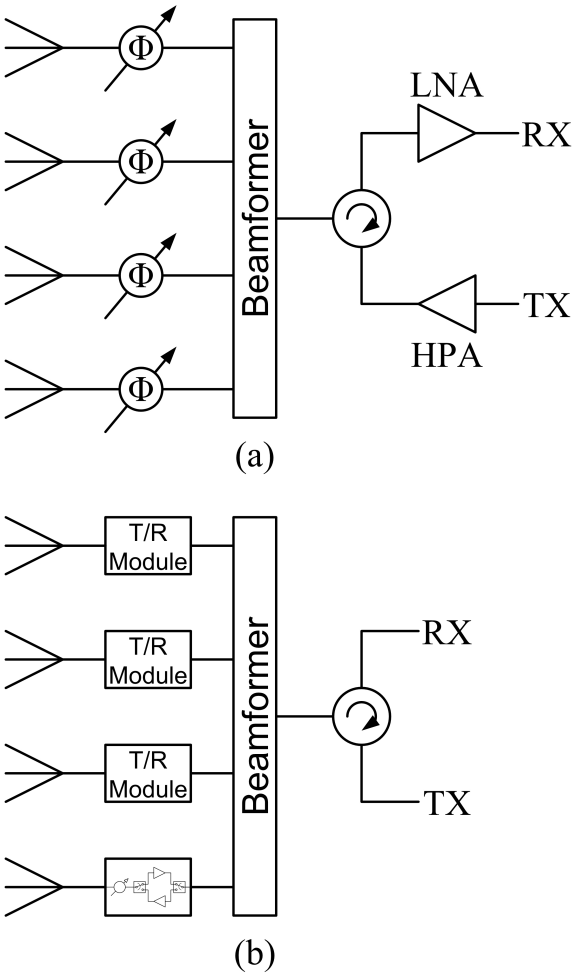

Figure 6: Block diagram of (a) passive phased arrays and (b) active phased arrays

1.4 Phased Array Architectures

1.4.1 Passive vs. Active Arrays

Phased array systems can be split into to two categories depending on the feeding of antenna elements: Passive and active.

Passive phased arrays (Fig. 6.a) consist of a very high power PA (power amplifier) in transmit mode and very high performance LNA (low noise amplifier) in receive mode, connected to multiple phase shifting and radiating elements through a circulator. In this architecture, phase shifting and radiating elements are all passive. Very high power requirements of such systems are met with klystrons, magnetrons, traveling wave tube devices etc. In such passive arrays, a single PA can be connected either to whole array or some sub-array of the whole array [19].

Active phased array approach is shown in Fig. 6.b. In this case, each antenna

element is followed by an active transmit/receive (T/R) module. Each T/R module internally contains its own PA, LNA, phase shifter and switches. Active array approach offers some advantages over its passive counterpart. First, passive arrays are more prone to device failures. Since a single PA (or LNA) is connected to multiple radiators, any possible failure of a single device during operation may cause significant number of radiators to become useless, which degrades the phased array performance significantly. In active array approach, a failure in one of the T/R module causes only single radiator element to become non-functional and its effect on the whole array performance may be negligible if the number of antenna elements are large enough. Second, in passive array approach, antenna elements are preceded by phase shifters, beamformer and switching networks, before the LNA. These blocks introduce unavoidable losses before LNA in receive mode and after PA in transmit mode, which eventually degrades noise figure and sensitivity of the array in the receive mode and total radiated power in transmit mode. Additionally, active phased arrays do not require very high power vacuum tube devices. These devices can be replaced with moderate power solid state electronic circuits in active phased arrays.

1.4.2 Phase Shifting Methods

Phased array systems can also be categorizes according to how the phase shifting functionality is realized. In this respect, there are four main phased array architectures: RF phase shifting, IF phase shifting, LO phase shifting and digital beam forming.

Fig. 7.a show RF phase shifting approach (or All-RF phased array architecture) which has been the most dominant approach since it is the most compact architecture. It employs a single mixer after the RF combiner, therefore does not require an LO distribution network. Also, the combining point is in RF domain in this architecture and the combined signal before the downconversion mixer has a high pattern directivity. Therefore, strong inband interferences at the direction of beam nulls are easily canceled/rejected in RF phase shifting approach. This feature helps to alleviate dynamic range requirements of mixer and following blocks. A challenge in all-RF architecture is the RF phase shifters. Passive phase shifter MMICs are

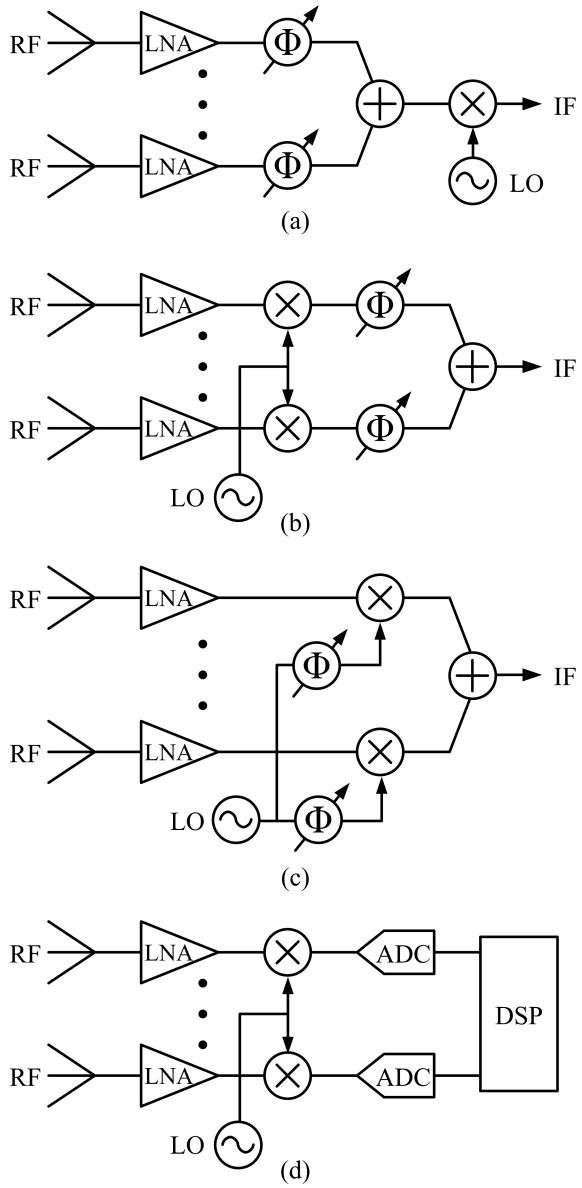

Figure 7: Phased array architectures: (a) RF phase shifting (b) IF phase shifting (c) LO phase shifting (d) Digital beam forming

generally lossy and active phase shifters must be designed with sufficient linearity, otherwise interference rejection advantage of all-RF architecture will be lost [20].

Although phase shifters can be realized in IF stage (Fig. 7.b), it has no practical advantage over all-RF architecture. Passive component values are inversely proportional with frequency, so IF phase shifters require larger area. This architecture also employs individual mixers for each antenna element, therefore has significantly larger power consumption.

LO phase shifting approach (Fig. 7.c) also requires separate mixers for each channel, but its advantage is that phase shifters are removed from RF signal path.

Phase shifters that are used in all-RF architectures can be directly used in LO paths, plus the parameters such as loss, linearity and noise figure of phase shifters are no longer any concern. Yet, there are some challenges in LO phase shifting approach. Inband interference cancellation occurs only after signal combining, which in this case happens to be after downconversion mixers. Therefore, mixers must provide sufficient dynamic range, which means a higher power consumption. Another challenge of both IF and LO phase shifting architectures is that they both require LO distribution networks, which means a more complex system and layout, especially for large arrays [21].

Finally, in digital beam forming approach (Fig. 7.d), phase shifters are totally removed from analog signal chain and phase shifting is performed in digital domain. This method also suffers from interference rejection same as IF and LO phase shifting architectures and requires high dynamic range mixers and ADCs. Due to the usage of separate ADCs for each antenna element, it has the highest power consumption. Yet, despite all these disadvantages, digital beam forming enables a variety of complex signal processing using a digital signal processor (DSPs). In this way, large number of beams can be simultaneously synthesized [22].

1.5 All RF Transmit/Receive Module

The performance of active electronically scanned phased arrays (AESA) strongly depends on the performance of transmit/receive (T/R) modules. Typical building blocks of an all-RF T/R module are low noise amplifier (LNA), power amplifier (PA), single-pole double-throw switches (SPDT), phase shifters (PS), variable gain amplifiers (VGA) and attenuators.

Fig. 8 shows different system level architectures for all-RF T/R modules. Fig. 8.a shows the most trivial architecture where transmit and receive paths are totally isolated and these paths are routed to antenna by ay a T/R switch (could be a circulator as well but they are hard to implement on-chip). In this architecture, phase shifters can be active or passive, and VGAs can be employed if necessary. The use of multiple PS and VGA in this T/R module architecture can be overcome by sharing PS and VGA in transmit and receive modes, as shown in Fig. 8.b. In this architecture PS and VGA must be bidirectional, which necessitates the use

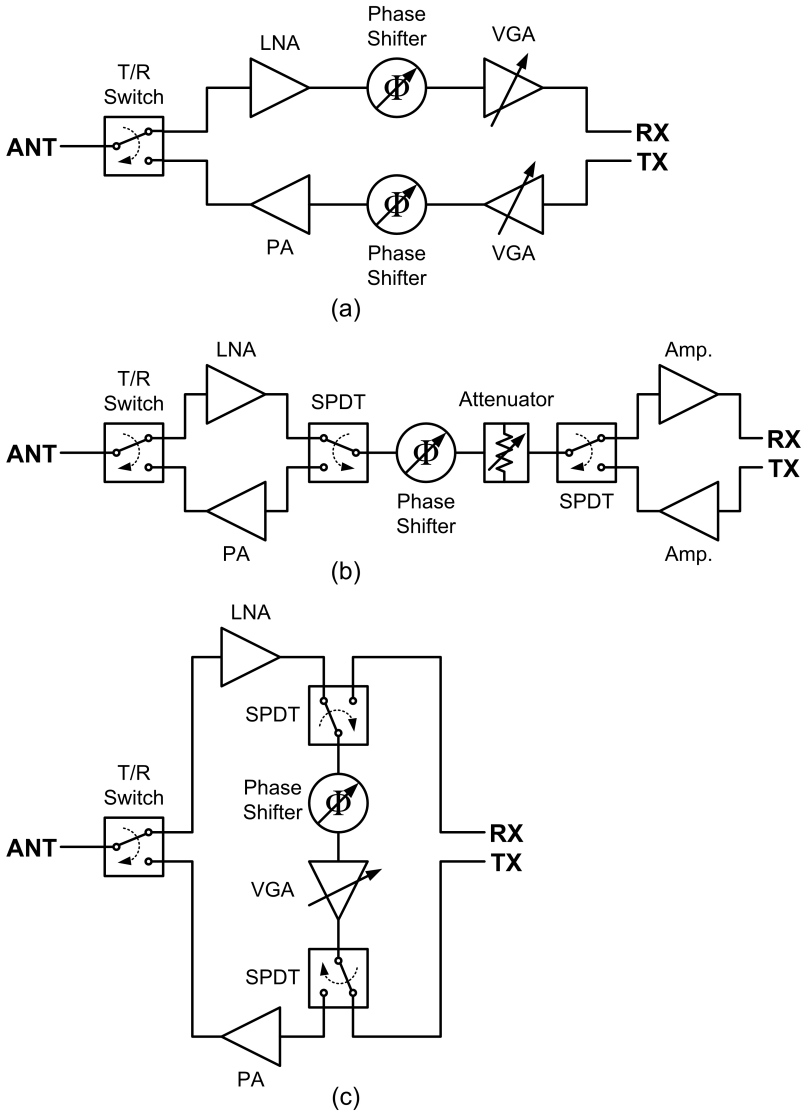

Figure 8: Several system level architectures for RF transmit/receive modules

of a passive phase shifter and an attenuator instead of a VGA. However, in this architecture LNA and PA gain requirements are more strict, since they have to compensate for losses introduces by PS, attenuator and additional SPDT switches.

The loop constructed by T/R switch, LNA, SPDT and PA in Fig. 8.b can pose oscillation problems if T/R switch and SPDT switch isolation is not enough. This problem can be solved by the T/R module architecture shown in Fig. 8.c. Also an active PS and VGA (instead of an attenuator) can be used in this architecture, since they no longer have to be bidirectional.

Performance of a radar system can be compared by maximum radar range R_{MAX} which is the longest distance the radar can successfully perform search and track functionality. Well known radar equation is given in [16] as

$$P_r = P_t \frac{G_t A_r \sigma}{(4\pi)^2 R^4} \tag{10}$$

where P_r is the received signal power, P_t is the transmitted power, G_t is the transmitter antenna gain, A_r is the effective aperture of receiving antenna, σ is the radar cross-section of the target and R is the distance between the target and the array. In a phased array, transmitted power linearly scales with number of antenna elements N. In other words, $P_{t,array} = NP_t$, where P_t is the power transmitted from a single element. The same is true for antenna gain and antenna aperture (i.e. $G_{t,array} = NG_t$ and $A_{t,array} = NA_t$) and the relation between antenna gain and antenna aperture is given as

$$G = \frac{4\pi A}{\lambda^2} \tag{11}$$

Assuming transmitting and receiving arrays are the same, maximum radar range R_{MAX} can be found from (10), by substituting P_r with P_{min} (minimum detectable signal) and R with R_{MAX}, and it is found as

$$R_{MAX} = \sqrt[4]{\frac{NP_t \left(NA_t\right)^2 \sigma}{\lambda^2 P_{min}}} = \sqrt[4]{\frac{N^3 P_t A_t^2 \sigma}{\lambda^2 P_{min}}} \tag{12}$$

From (12) it can be seen that the largest improvement in maximum radar range is not due to transmit power of a single element P_t or antenna aperture A_t, but the number of antenna elements N. A direct corollary of this is that a given maximum radar range can be achieved by a lower P_t by slightly increasing the number of radiating elements. This nuance is the motivation for active electronically scanned phased array radars consisting of thousands of fully integrated, single chip T/R modules, which will dramatically reduce the overall cost.

1.6 SiGe BiCMOS Technology

T/R modules for phased array applications have been usually implemented in III-V technologies, such as GaAs and InP. With the recent advances in SiGe bipolar complementary metal oxide semiconductor (SiGe BiCMOS) technologies, today it is possible to develop single chip T/R modules for microwave and millimeter wave

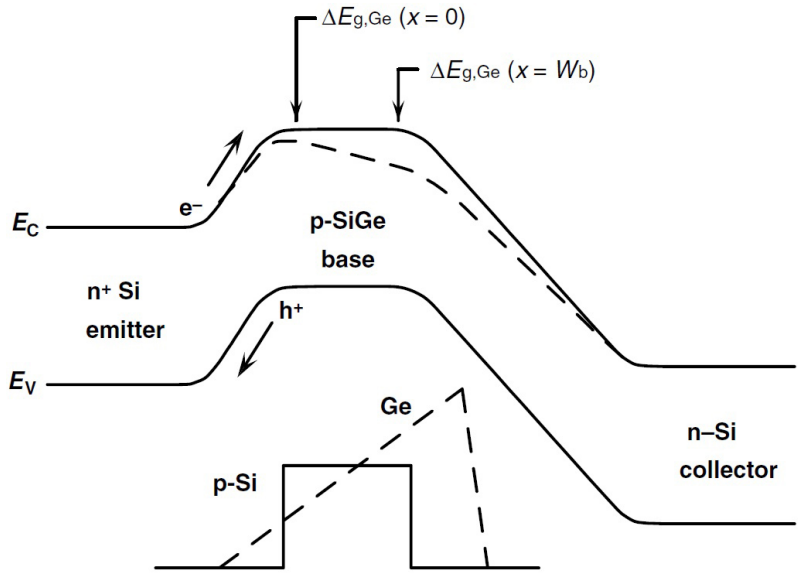

Figure 9: Energy band diagram of a Si BJT vs. SiGe HBT [1]

applications. Heterojunction bipolar transistors (HBT) in state-of-the-art SiGe processes have matched their III-V counterparts in terms of speed and performance.

SiGe HBT technology utilizes bandgap engineering in the base of bipolar transistors. In this technology, base of bipolar transistors are epitaxially grown SiGe alloys. Ge has a bandgap of 0.66 eV compared to 1.12 eV bandgap of silicon. In this way, electron injection is increased and this produces a higher current gain, β. Also, the Ge content at the base is graded, as shown in Fig. 9, which generates a built-in electric field, accelerating minority carriers in the base region, therefore reducing base transit time, τ_b. Addition of graded Ge doping in base significantly improves high frequency performance of HBTs. This improvement can be seen in

$$f_T = \frac{1}{2\pi}\left(\tau_b + \tau_c + \frac{1}{g_m}\left(C_\pi + C_\mu\right) + \left(r_e + r_c\right)C_\mu\right)^{-1} \tag{13}$$

where f_T is the cutoff frequency (frequency at whcih current gain β becomes unity), τ_c is the transit time in collector region, g_m is the transconductance, C_π and C_μ are BE and BC junction capacitances, r_e and r_c are emitter and collector resistances [5]. f_T is increased via τ_b and g_m. Maximum oscillation frequency, f_{MAX}, (frequency at which power gain becomes unity), is another important performance metric which is given as

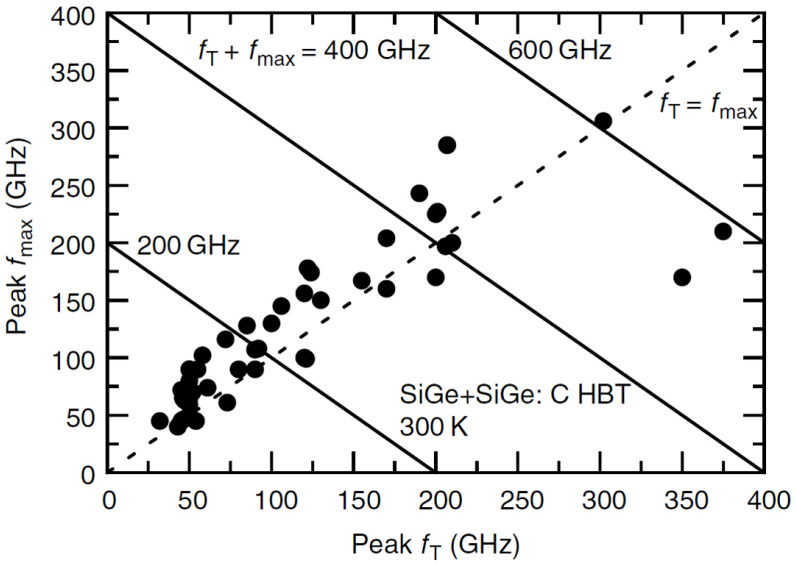

Figure 10: Cutoff frequency (f_T) and maximum oscillation frequency (f_{MAX}) for different SiGe HBT technologies. [2]

$$f_{MAX} = \sqrt{\frac{f_T}{8\pi C_\mu r_b}} \tag{14}$$

where r_b is intrinsic base resistance. In a normal Si BJT, increasing base doping reduces r_b, but it reduces current gain as well. However, by adjusting Ge grading at the base, higher base doping can be achieved in SiGe HBT, without worsening the current gain. So, r_b is effectively reduced in SiGe HBTs, resulting in improved noise performance. By introducing graded Ge doping in base region, all important high frequency performance parameters such as β, τ_b, f_T, f_{MAX} and r_b is improved. Fig. 10 shows reported f_T and f_{MAX} values for different SiGe HBT technologies.

Improved RF performance of SiGe HBT is crucial for T/R module performance, but its real advantage over its III-V counterparts is the integration potential with CMOS. SiGe BiCMOS offers competitive RF performance with III-V technologies, and at the same time, benefits from yield, cost and manufacturing advantage of silicon CMOS fabrication. Digital baseband and RF front-end blocks can be easily integrated in SiGe BiCMOS. A comparison between SiGe HBTs with alternative technologies are presented in Table 2. The device performance parameters for IHP SiGe BiCMOS technology that is used in this work is presented in Table 2.

Extreme performance phased arrays required by military applications will be still realized in III-V. Although SiGe can be used for some military applications

Table 1: Relative performance comparison of different IC technologies (Excellent: ++; Very Good: +; Good: 0; Fain: –; Poor: – –) [5]

Performance Metric	SiGe HBT	SiGe BJT	Si CMOS	III-V MESFET	III-V HBT	III-V HEMT
Frequency Response	+	0	0	+	++	++
1/f and Phase Noise	++	+	–	– –	0	– –
Broadband Noise	+	0	0	+	+	++
Linearity	+	+	+	++	+	++
Output Conductance	++	+	–	–	++	–
Transconductance	++	++	– –	–	++	–
Power Dissipation	++	+	–	–	+	0
CMOS Integration	++	++	N/A	– –	– –	– –
IC cost	0	0	+	–	–	– –

Table 2: SiGe HBT performance parameters for IHP 0.25-μm HBTs (SG25H3)

peak f_T	110 GHz
peak f_{MAX}	180 GHz
peak β	150
J_C @ peak f_T	6.5 mA/μm^2
BV_{CEO}	2.2 V

as well, its main dominance is the commercial applications such as short range vehicular radars, weather radars, RFIDs, satellite communications, short range indoor communications, radio astronomy and even biomedical applications. In short, SiGe BiCMOS technology is a good candidate for low-cost, light-weight, fully integrated T/R modules and system-on-chip solutions for microwave and millimeter wave pahsed array applications.

1.7 Motivation

As stated in previous sections, there are many military and civilian applications of fully integrated T/R modules at different frequency bands. Low frequencies (below 5 GHz) are not well suited for integrated T/R module solutions, since the area dominated by passive components (especially inductors) is inversely proportional with frequency. Current phased array T/R modules in III-V technologies at X-band (8-12 GHz) and beyond has relatively high cost, size, weight and power consump-

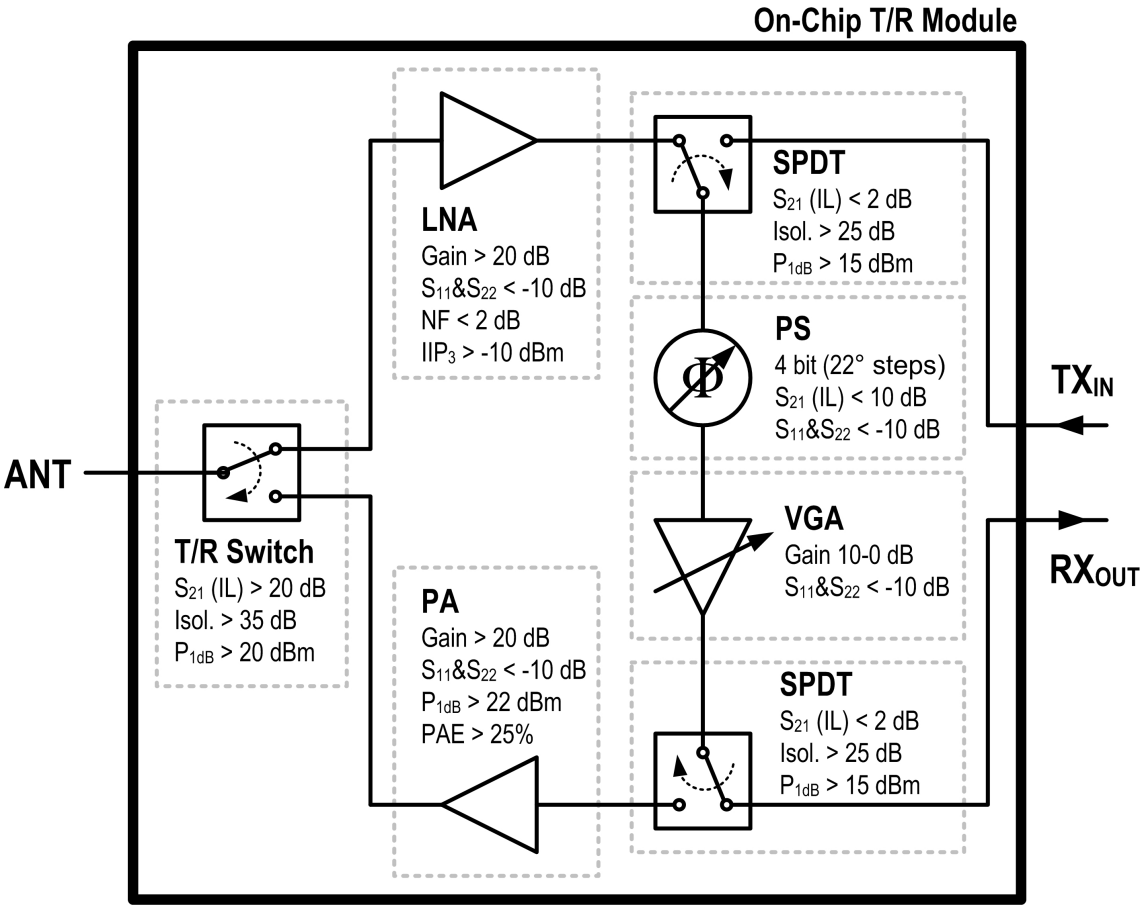

Figure 11: SiGe X-band all-RF T/R module block diagram and component specifications

tion. These are the limitations for next generation phased array T/R modules to be used in military and commercial applications.

The objective of this thesis is to develop an X-band (8-12 GHz) fully integrated all-RF T/R module, as shown in Fig. 11, using SiGe BiCMOS technology that will overcome the limitations mentioned above. On top of the previously developed building blocks, this thesis aims to present the design and measurements of a 4-bit X-band passive phase shifter and realization of the complete T/R module chip in IHP 0.25-μm SiGe BiCMOS process. Further discussion about T/R module specifications are given in Chapter 4.

1.8 Organization

The thesis is organized as follows.

Chapter 2 introduces phase shifter fundamentals ans different approaches for RF phase shifting. A comparative analysis between different phase shifter topologies are

presented. It is shown that switched filter topology offers the best trade-off between, insertion loss, area and RMS phase error.

Chapter 3 includes investigation of quantization loss of passive phase shifters on the array performance. Later on, the design approach and implementation of 4-bit switched filter passive phase shifter is presented. Simulation and measurement results are also presented in this chapter.

Chapter 4 starts with system level discussion of X-band T/R module and component specifications. The measured results of the previously developed blocks, namely SPDT switch, LNA and PA are presented. Later on, the integration and measurement of complete SiGe X-band T/R module is presented and compared with similar works in literature.

Chapter 5 concludes the thesis with some additional discussion on the problems encountered throughout the thesis and provides information on possible future studies.

2 Phase Shifter Fundamentals

In this section, fundamentals of phase shifters will be covered with an emphasis on their integrated circuit implementations. The section starts with categorizing phase shifters in terms of different perspectives, then continues with the performance metrics of phase shifters and concluded with a comparison of different phase shifter topologies.

Phase shifter is simply a circuit block that changes the transmission phase, $\angle S_{21}$, of a signal in a controlled way. A phase shifter has a 360° control over the phase of the signal. To shift the phase more than 360°, time delay elements are used.

2.1 Analog vs. Digital Phase Shifter

Analog phase shifter provide continuous phase shift from 0° to 360°. They are mostly controlled by a voltage and, for example, can be realized by varactor diodes. On the other hand, digital phase shifters cover the same range in discrete steps. A digital phase shifter is composed of several "bits". Each bit provides a desired phase shift between its "ON" and "OFF" state. The bit that provides the largest phase shift is called MSB (most significant bit) and the lowest bit is called LSB (least significant bit). An N bit phse shifter covers the 0° to 360° range in $360°/2^N$ steps. So, a 3-bit phase shifter has an LSB of 45°, 4-bit phase shifter has an LSB of 22.5°, 5-bit phase shifter has an LSB of 11.25° and so on. Digital phase shifters are more common since they are immune to noise from control voltage lines, unlike analog phase shifters [23].

2.2 Active vs. Passive Phase Shifter

Simply, an active phase shifter provides gain while a passive phase shifter introduces attenuation. Both has advantages and disadvantages. Passive phase shifters are lossy. So, the loss of passive phase shifters are almost always compensated by amplifiers in the next stage, which brings additional power consumption. Active phase shifter merges amplification and phase shifting together, to end up at a lower power consumption overall. However, they generally suffer from low linearity. Passive phase shifters have higher linearity due to their intrinsic losses, however they

suffer from higher noise figure. Yet, passive phase shifters are more common, mainly because they are "reciprocal", unlike active phase shifters. This comes in handy for system level integrations.

2.3 Performance Metrics

All common RF performance parameters such as insertion loss, return loss, noise figure, linearity and general IC performance metrics such as power consumption, chip area etc. are same for phase shifters as well. Here, we are going to focus on performance metrics specific to phase shifters.

2.3.1 RMS Phase Error

For a phase shifter, there is always some error between the desired phase shift and the obtained phase shift. These errors are different for each phase state and vary with frequency. A method to describe these errors is to calculate their root-mean-square as,

$$\text{RMS Phase Error } (\omega) = \sqrt{\frac{\sum_{n=1}^{N} \left(\Delta\phi_n(\omega)\right)^2}{N}} \tag{15}$$

where $\Delta\phi_n$ denotes the error between the desired and obtained phase shifts for the n^{th} phase state. RMS phase error is minimum at center frequency and increases for for higher and lower frequencies.

2.3.2 RMS Gain Error

An ideal phase shifter only changes $\angle S_{21}$ and does not affect $|S_{21}|$. However, this is not so in practice. There is a deviation in phase shifters' gain (or loss) for different phase states. RMS gain error (or RMS amplitude error) describes the deviation of gain of different phase states from the average gain, which is given as,

$$\text{RMS Gain Error } (\omega) = \sqrt{\frac{\sum_{n=1}^{N} \left(\Delta A_n(\omega)\right)^2}{N}} \tag{16}$$

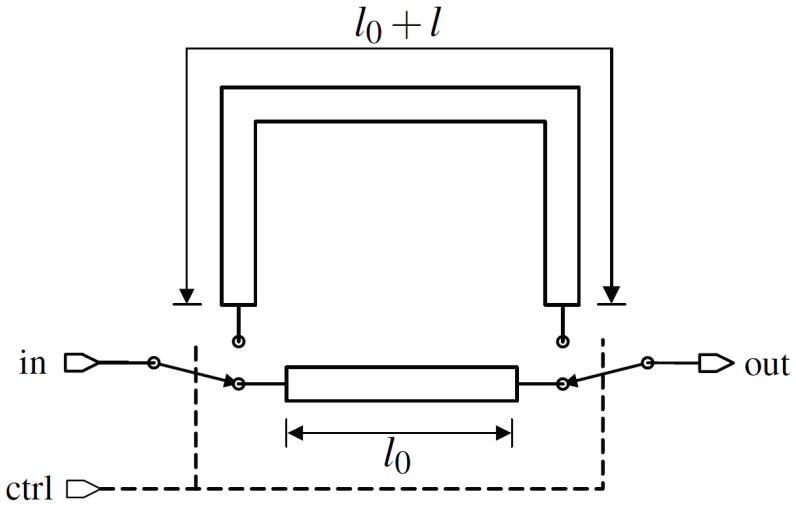

Figure 12: Switched-line phase shifter [3]

In this case, ΔA_n denotes the error between the amplitude of the n^{th} state and the average amplitude.

2.3.3 Effective Number of Bits

An N bit phase shifter may physically consist of N bits. However, its effective number of bits is defined in regard to its RMS phase error. To have N bit operation, in other words, to have N effective number of bits, the RMS phase error must be lower than LSB/2 for that specific N. For example, to achieve a 4-bit operation (22.5° step size), RMS phase error must be lower than 11.25.

This definition of effective number of bits is actually used for determining the useful bandwidth of the phase shifter. In other words, a phase shifter achieves N bit operation in the frequency band where its RMS phase error is less than its LSB/2.

2.4 Phase Shifter Topologies

There can be more deeper categorization of phase shifter topologies, most common RF-path phase shifters can be grouped into five main categories: Switched line, loaded line, reflection type, switched filter and vector modulator.

2.4.1 Switched-Line

Switched-line phase shifter is the most natural approach for phase shifting (Fig. 12). Actually it operates as a true time delay element and the delay is determined

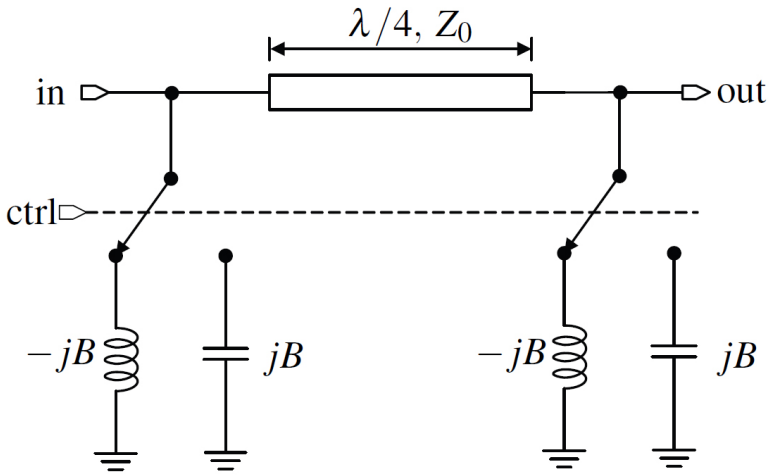

Figure 13: Loaded-line phase shifter [3]

by the difference of the two path lengths. Theoretically this would be the best option since it would allow wideband operation. However, there are practical limits. The use of two SPDT switches per bit increases insertion loss. Paths with different lengths has different attenuations, causing amplitude errors. The requirement of using long transmission lines and coupling between them are disadvantage as well.

2.4.2 Loaded-Line Phase Shifter

In this approach, instead of changing transmission line lengths, the line characteristics are changed by loading the line appropriately (Fig. 13). It features smaller area than switched line approach, but its main disadvantage is that the return loss strongly depends on phase shift, allowing only small phase shifts to be realized. Also dependence of $\lambda/4$ lines makes it a narrowband solution.

2.4.3 Reflection Type Phase Shifter

The common element of reflective type phase shifter (RTPS), as shown in Fig. 14, is coupler. It can be a 90° hybrid or a 180◦ rat-race coupler or even a circulator. Two ports of the coupler is used as RF input and output, while the other port(s) are terminated with variable loads.They can be tunable passives or diodes. Phase shift is obtained by tuning the loads. In this sense, RTPS is an analog type phase shifter, but it can be used as a digital phase shifter as well, if the load network consists of digitally controlled FETs instead of varactors. For on-chip applications, the coupler part can be implemented using lumped LC networks to obtain smaller chip area at

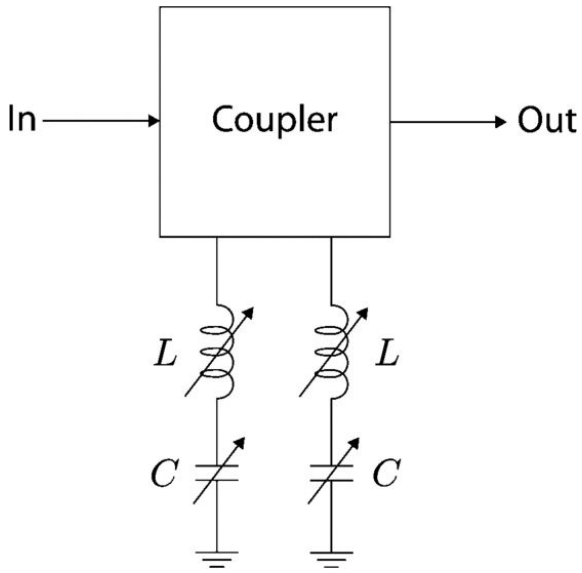

Figure 14: Reflection type phase shifter [4]

lower frequencies, making it a more suitable solution for on-chip applications than previous two phase shifters. Yet, transmission lines are preferred for mm-waves. The lossy couplers are a disadvantage for this topology but input/output ports are better matched than its alternatives due to the high isolation between the coupler ports.

2.4.4 Switched Filter

Switched filter phase shifter can be considered as a subset of switched line appraoch, where LC filters are used instead of transmission lines. Fig. 15 shows high-pass/low-pass phase shifter, in which the signal path is switched between high-pass and low-pass Π-networks. A high-pass or low-pass, Π- or T-network can provide up to 90° phase shift at a center frequency ω_0 while being matched to Z_0 [ref. ver]. (Analysis for low-pass Π-network is provided in the next section). In this way, high-pass/low-pass topology can provide up to 180° phase shift. Also, it provides near an octave bandwidth, much more than its previous alternatives. This is due to that the phase vs. frequency slopes of two filters are almost parallel around the center frequency.

This topology requires two SPDTs. For discrete phase shifters or for the application where MEMS switches are feasible, this topology would be no brainer. However, for CMOS and BiCMOS technologies, due to the lack of very low insertion loss RF

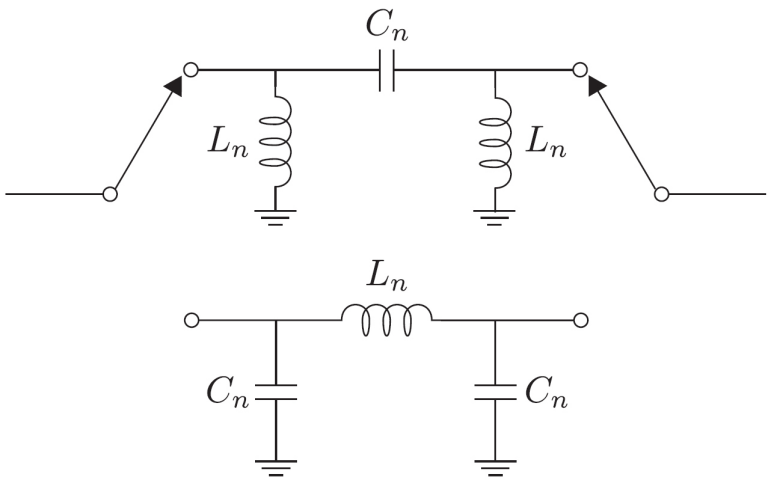

Figure 15: High-pass/Low-pass phase shifter [4]

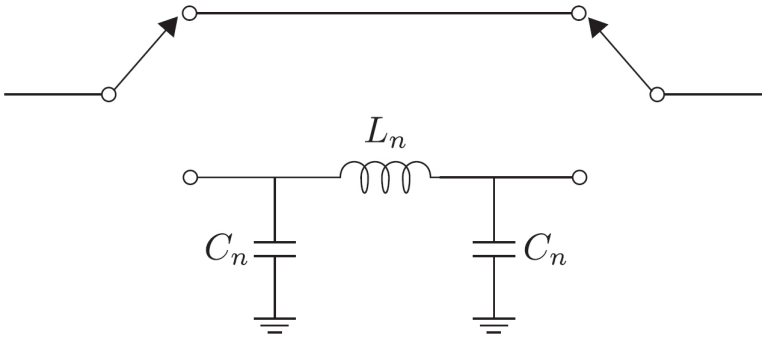

Figure 16: By-pass/Low-pass phase shifter [4]

switches, high-pass/low-pass topology must be modified to achieve lower insertion loss. In this context, Fig. 16 shows an alternative topology, where high-pass filter section is replaced with a by-pass section, making it a by-pass/low-pass topology. Although this topology can generate only up to 90° phase shift and can provide only narrowband operation, the realization of each bit with only a single series switch is an advantage. Also, this topology requires less chip area due to reduced number of inductors.

2.4.5 Vector Modulator

The previous topologies were all passive, reciprocal and they control only the phase of the signal. They also tend to be lossy and require large chip area in general due to use of many passive devices (especially inductors). Vector modulation scheme

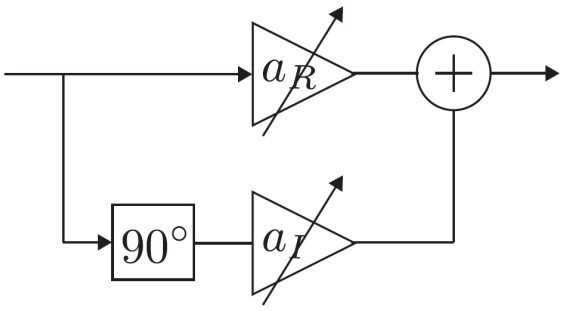

Figure 17: Vector modulator phase shifter [4]

has a very different operating principle, as shwon in Fig. 17. First, the input signal is decomposed into its in-phase (I) and quadrature-phase (Q) parts such that there is 90° phase difference between them. This part can be realized by hybrid couplers or all-pass RLC filters etc. Then by properly setting the gain of each VGA and adding the output signals, one can generate all the phases in between I and Q signals. This provides 90° phase control. By changing the sign of the gain of VGAs (can be easily done in a differential system) whole 360° phase control is achieved. RMS phase error of this topology mainly depends on the calibration of DACs that are used to supply required control votlages to VGAs, as well as generation of I and Q signals.

2.5 Quantization Loss and Number of Bits

As emphasized in the previous pages, digital phase shifters are generally preferred over analog phase shifters due to their immunity to noise coming from control voltages and due to much simpler control mechanism and lower power consumption in general. However, the digital phase shifters can affect the performance of the array they are used in. In an ideal phased array, all radiating elements are excited

Table 3: Phase Quantization Example

Antenna Number	Desired Phase (deg)	4-Bit Quantized Phase (deg)
1	0.0	0
2	61.6	67.5
3	123.1	112.5
4	184.7	180
5	246.3	247.5
6	307.8	315
7	369.4 (=9.4)	0
8	431.0 (=70.9)	67.5

with a linear incremental phase taper of ϕ if the desired beam direction is θ as given in (5). For instance in an 8-element, d=$\lambda/2$ spacing array, to steer the beam in θ=20° direction, a phase taper of ϕ=61.6° must be applied to the array. These phases are quantized according to a 4-bit digital phase shifter as seen in Table. 3, i.e. phases are rounded to nearest phases state of a 4-bit representation. Those inaccurate phases introduced to the radiating elements cause some degradation in directivity of the beam and its direction. This degradation is called quantization loss. Fig. 18 shows a detailed simulation result analyzing the quantization loss. A 100-element array with $\lambda/2$ spacing is compared under continuous (ideal) phase shift and 1-bit to 5-bit digital phase shift, while beam is scanned with 1° steps. Results show that quantization loss is negligible after 4-bits.

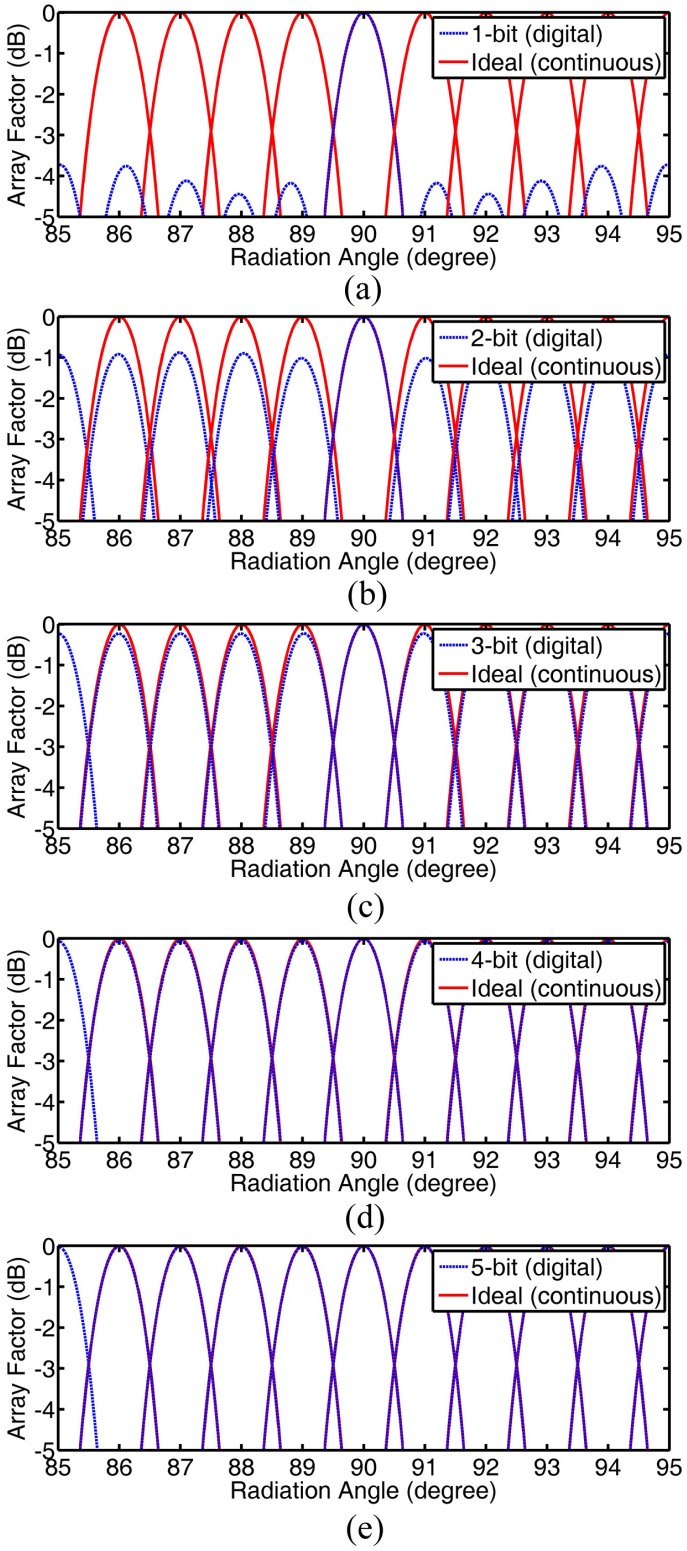

Figure 18: Comparison between continuous phase shift and discrete phase shift, displaying quantization loss. Figures show normalized array factors of a linear array with N=100 elements and $\lambda/2$ spacing, using (a) 1-bit (b) 2-bit (c) 3-bit (d) 4-bit (e) 5-bit digital phase shifting. Quantization loss is negligible after 4-bits.

3 A 4-bit X-band Switched Filter Phase Shifter in SiGe BiCMOS

Up to now, phased arrays and T/R modules are introduced in Chapter 1 and phase shifters are briefly discussed in Chapter 2. This chapter will focus on the design, analysis and results of a 4-bit X-band switched filter phase shifter.

3.1 Phase Shifter Requirements

Phase shifter is probably the most important building block of the T/R module (Fig. 41). The capability to correctly adjust the phases are crucial for beam scanning performance of the array, so minimum RMS phase error is required. On top that, in order not to degrade receiver sensitivity or transmitter output power, phase shifter must be low loss. In order to realize an X-band T/R module with a very small chip area (< 5 mm^2), a phase shifter topology with small chip area must be chosen. Also, non-ideal RF switches at BiCMOS technologies must be taken into account while choosing the optimum topology. In this sense, and in the light of the discussion in Chapter 2, switched-filter (bypass-lowpass) topology is chosen to realize the phase shifter. It is shown in the previous chapter that less than 4 bit operation for a phase shifter causes quantization loss. Although using higher number of bits improves spacial resolution, it also increases the phase shifter loss and T/R module noise

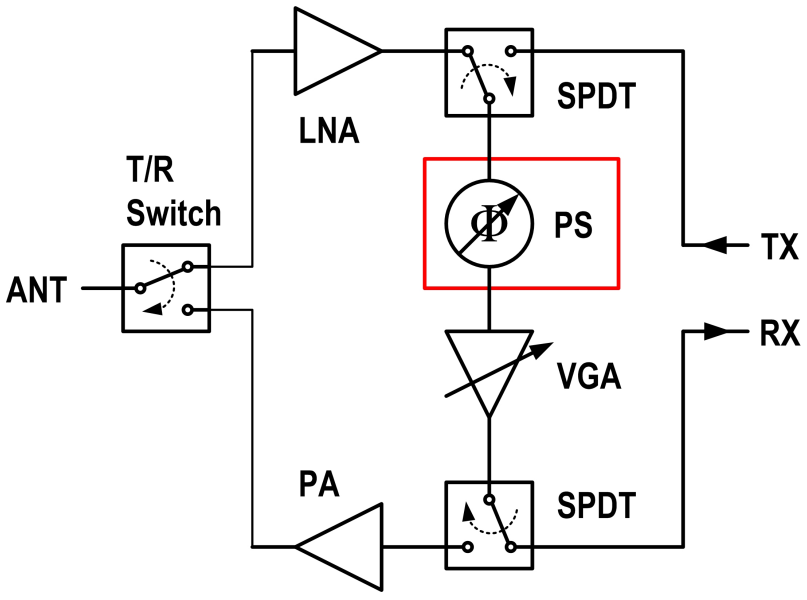

Figure 19: System diagram of a T/R module

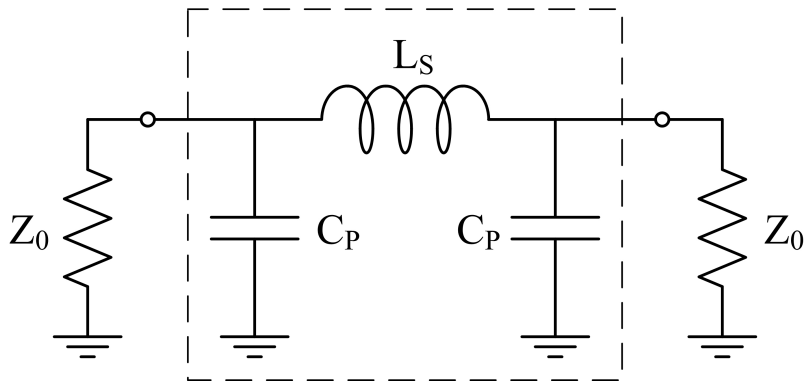

Figure 20: Schematic view of Π-type low pass filter

figure. So, 4-bit is chosen as the optimum number.

3.2 Low-Pass Π Network

Before going any further, let's analyze the low-pass Π network shown in Fig. 20. Since this is a symmetric structure, it can be separated it into two, as shown in Fig. 21. The impedance seen looking into each symmetric side, Z_A is given as,

$$Z_A = \frac{j\omega L}{2} + \left(Z_0 \parallel \frac{1}{j\omega C}\right) = \frac{j\omega L}{2} + \frac{Z_0\left(1 - j\omega Z_0 C\right)}{1 + \omega^2 Z_0^2 C^2} \tag{17}$$

This network will be used as a phase shifter, which implies that its input and output must be matched to 50 Ω. This further implies that imaginary part of Z_A must be zero, otherwise the two sides will not be matched to each other.

$$\mathrm{Im}\{Z_A\} = \frac{\omega L}{2} - \frac{\omega Z_0^2 C}{1 + \omega^2 Z_0^2 C^2} = 0 \tag{18}$$

$$\frac{L}{2} = \frac{Z_0^2 C}{1 + \omega^2 Z_0^2 C^2} \tag{19}$$

The transfer function $H(\omega)$ of the half network in Fig. 21 can be written as,

$$H(\omega) = \frac{\left(Z_0 \parallel \frac{1}{j\omega C}\right)}{\left(Z_0 \parallel \frac{1}{j\omega C}\right) + \frac{j\omega L}{2}} \tag{20}$$

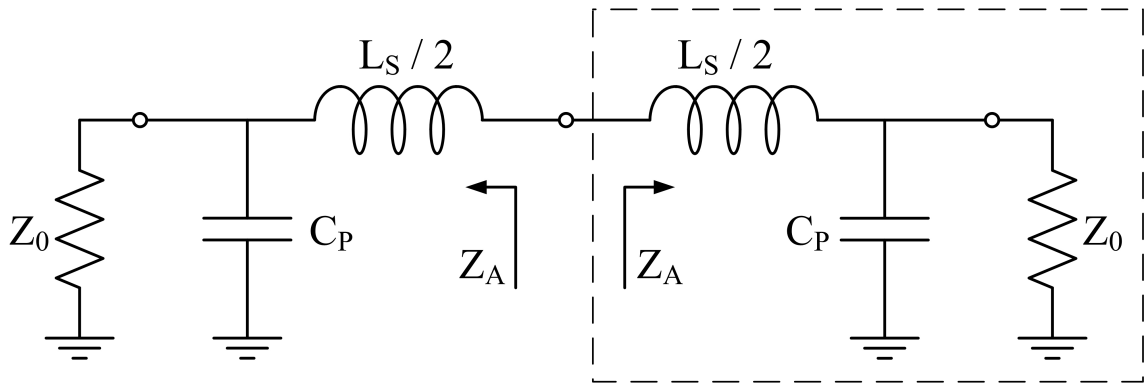

Figure 21: Decomposition of Π-type low-pass filter into two symmetric circuits

Combining (19) and (20) gives,

$$H(\omega) = \frac{\dfrac{Z_0\,(1 - j\omega Z_0 C)}{1 + \omega^2 Z_0^2 C^2}}{\dfrac{Z_0\,(1 - j\omega Z_0 C)}{1 + \omega^2 Z_0^2 C^2} + \dfrac{j\omega Z_0^2 C}{1 + \omega^2 Z_0^2 C^2}} \tag{21}$$

which is simplified to,

$$H(\omega) = 1 - j\omega Z_0 C \tag{22}$$

Since this is the transfer function of the half circuit and assuming the overall low-pass Π network provides a phase shift of ϕ, we can find the required value of C as,

$$\angle H(\omega) = \frac{\phi}{2} = \tan^{-1}(\omega Z_0 C) \tag{23}$$

$$C = \frac{\tan(\phi/2)}{\omega Z_0} \tag{24}$$

Inserting (24) into (19) and with some little trigonometry, the value of L can be found as,

$$\frac{L}{2} = \frac{Z_0^2 \dfrac{\tan(\phi/2)}{\omega Z_0}}{1 + \omega^2 Z_0^2 \dfrac{\tan^2(\phi/2)}{\omega^2 Z_0^2}} \tag{25}$$

$$\frac{\omega L}{Z_0} = \frac{2\tan(\phi/2)}{1 + \tan^2(\phi/2)} = \sin(\phi) \tag{26}$$

$$L = \frac{Z_0 \sin(\phi)}{\omega} \tag{27}$$

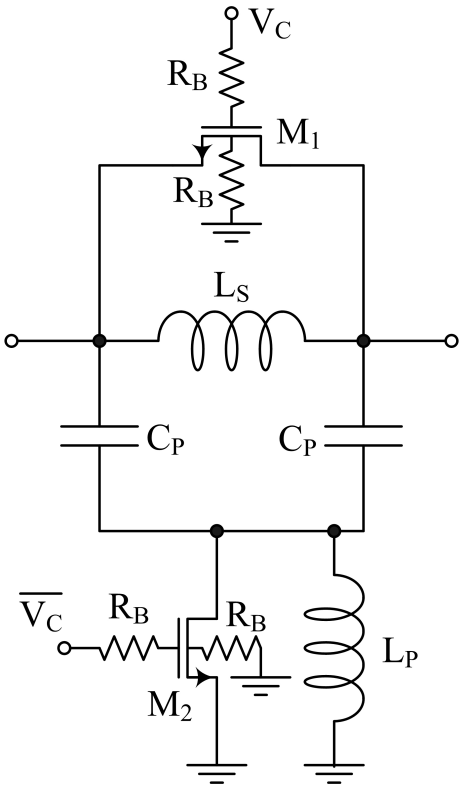

Figure 22: Switched filter phase shifter topology

Using (24) and (27), capacitance and inductance values can be obtained for any given phase shift of $0° < \phi < 90°$ and vice versa.

3.3 Circuit Design

Circuit schematic of the switched filter phase shifter topology is presented in Fig. 22. It is based on a low-pass Π network and isolated NMOS transistors are used for switching purposes. The circuit operates as follows: When M_1 transistor is OFF and M_2 is ON, the inductor L_S and the capacitors C_p construct the low-pass filter and the circuit operates in "phase shift" mode. When M_1 transistor is ON and M_2 transistor is OFF, the low-pass network is bypassed by M_1, so the circuit operates in "bypass" mode. In order to remove any signal coupling to ground in bypass mode via the OFF-capacitance of M_2, a shunt inductor L_P is introduced such that it resonates out the OFF-capacitance of M_2. 22.5°, 45° and 90° bits are implemented with this topology. For 180° bit, two 90° bits are cascaded, since this topology cam provide up to 90° phase shift only. In this way, RF signal path includes only 5 series NMOS transistors, when compared to 8 MOSFETs in a 4-bit high-pass/low-pass

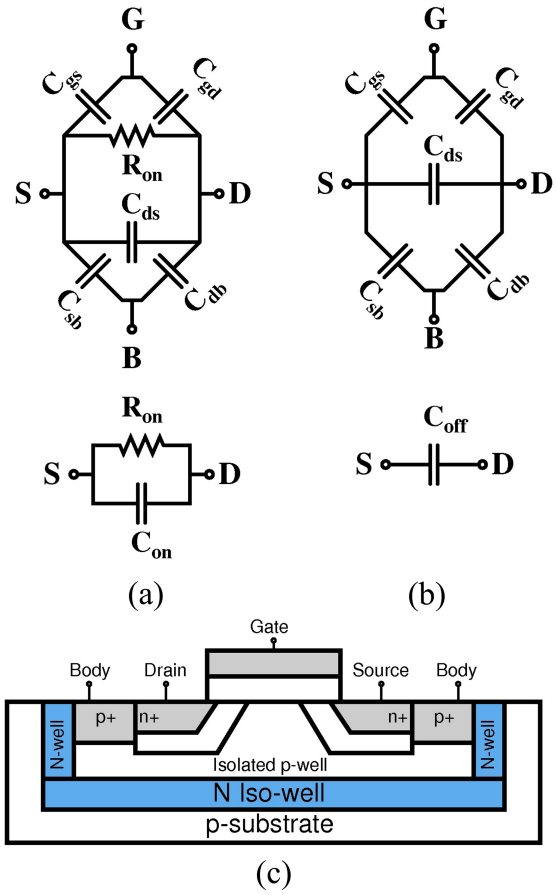

Figure 23: (a) ON-state (b) OFF-state equivalent circuit models of an NMOS transistor and (c) crossection of a typical isolated NMOS transistor.

topology, which would exhibit a better insertion loss.

$$L_P = \frac{1}{\omega^2 C_{off}} \tag{28}$$

For switching purposes, the isolated NMOS transistors offerd by IHP 0.25-μm BiCMOS technology is used. Fig. 23 shows crossection of a typical isolated NMOS device. Using these devices, body terminals are connected to ground via large resistances (20 kΩ). In this way, insertion loss due to capacitive coupling to substrate is reduced.

Fig. 23 also shows the electrical equivalent circuits for an isolated NMOS device with gate and body floating. Inserting these models into Fig. **??** and also including the parasitic resistances of inductors, the equivalent circuits for the switched filter phase shifter in "phase shift mode" and "bypass mode" is shown in Fig. 24. Table. 4 shows the electrical model parameters for NMOS switches.

A typical design starts with determining ideal component values for a desired

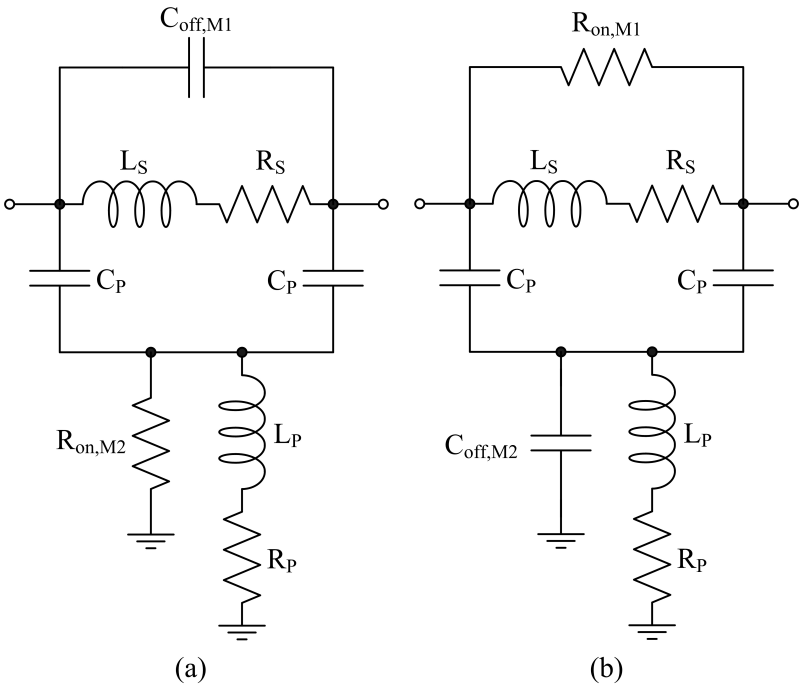

Figure 24: Equivalent circuit schematics for the phase shifter in (a) phase shift mode and (b) bypass mode, including inductor parasitics

Table 4: Simplified electrical switch models derived from simulations

Transistor Width	40-μm	100-μm	200-μm
R_{on}	23.5 Ω	9.5 Ω	4.9 Ω
R_{off}	60 kΩ	200 kΩ	400 kΩ
$C_{on} = C_{off}$	35 fF	85 fF	170 fF

Table 5: Calculated component values vs. Component values used in the design

	L_S	C_P	L_P	M_1	M_2
22°-bit (Calc.)	300 pH	63 fF	–	–	–
45°-bit (Calc.)	560 pH	132 fF	–	–	–
90°-bit (Calc.)	795 pH	320 fF	–	–	–
22°-bit (Design)	280 pH	75 fF	2.5 nH	100 μm	100 μm
45°-bit (Design)	420 pH	145 fF	2.2 nH	100 μm	100 μm
90°-bit (Design)	700 pH	335 fF	1.1 nH	40 μm	200 μm

phase shift using (24) and (27). After that, switches are introduced and component values of the low-pass network are *readjusted to achieve the best trade-off between phase error, insertion loss and return loss*, as shown in Table 5.

Normally, increasing the transistor width of M_1 reduces the insertion loss, but only to some extent. The reason is that, the increased capacitance of the MOS transistor becomes no longer negligible with respect to the low pass filter response. In this case, value of L_S and C_P can be readjusted but with this method, either

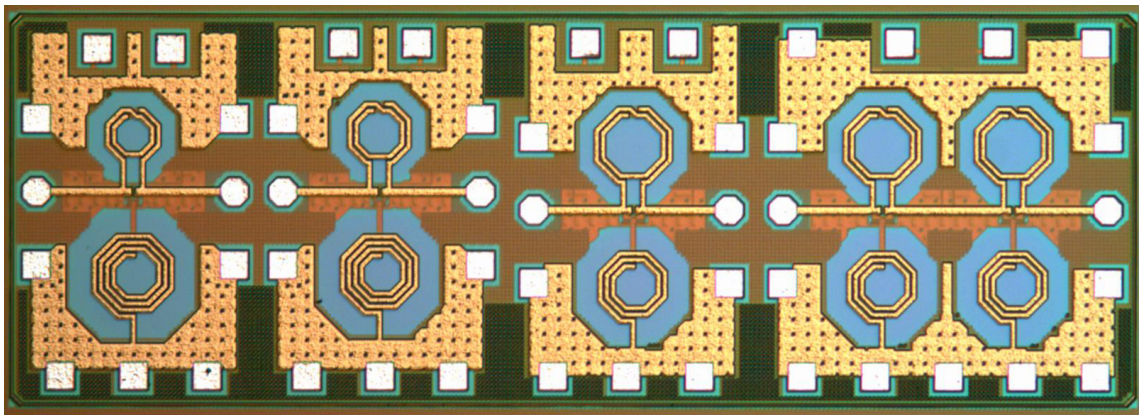

Figure 25: Chip photo of the fabricated 4-bit SiGe X-band passive phase shifter.

correct phase shift or 50 Ω matching can be achieved, not both.

Few remarks about the design: The amount of phase shift in "phase shift mode" does not change with R_{on}. It is only a function of L_S, C_P and C_{off}. Also due to the high quality factor of inductors, their series resistances does not affect the phase response in either mode of operation. They only slightly affect the insertion losses.

3.4 Measurements

The designed X-band phase shifter is fabricated using a high performance 0.25-μm SiGe BiCMOS process (SG25H3), offered by IHP Microelectronics. The fabricated chip is shown in Fig. 25. Total chip area is 0.8 x 2.3 μm^2. In this version, each bit is fabricated in a standalone manner, to see the performance of each block separately, while a complete phase shifter is integrated into the T/R module (see next chapter for details). The blocks in the figure from left to right are 22°, 45°, 90° and 180° bits. The 180° block is cascaded by slightly modified two 90°-bits. Phase shifter bits are connected to RF pads via custom designed 50 Ω microstrip transmission lines. Pad-to-pad S-parameter measurements are performed using Agilent 8720ES network analyzer.

3.4.1 Return Loss

Since the phase shifters are reciprocal, their S_{11} is equal to S_{22}. So, only one of them is given. Return loss of 22°-bit (Fig. 26) shows good agreement between simulation and measurement for phase shift mode while not that good agreement for bypass mode. Still, they are better than 15 dB at X-band (8-12 GHz). Measured

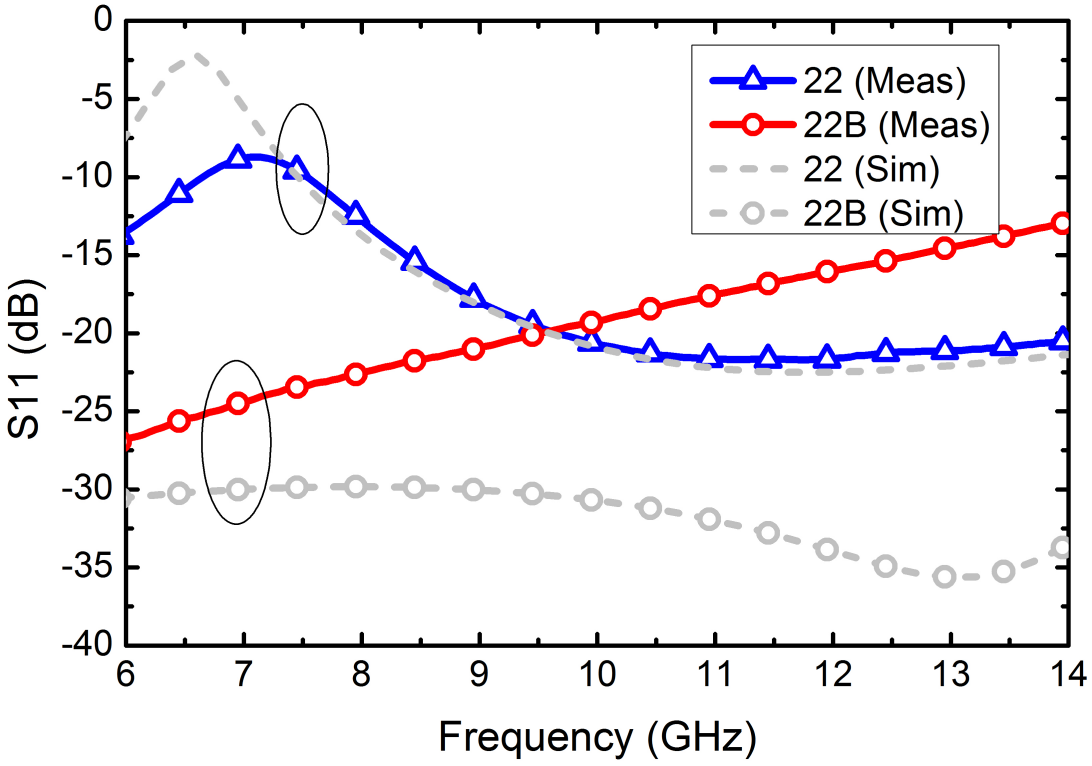

Figure 26: Simulated and measured return losses of 22.5° bit in both phase shift and bypass modes.

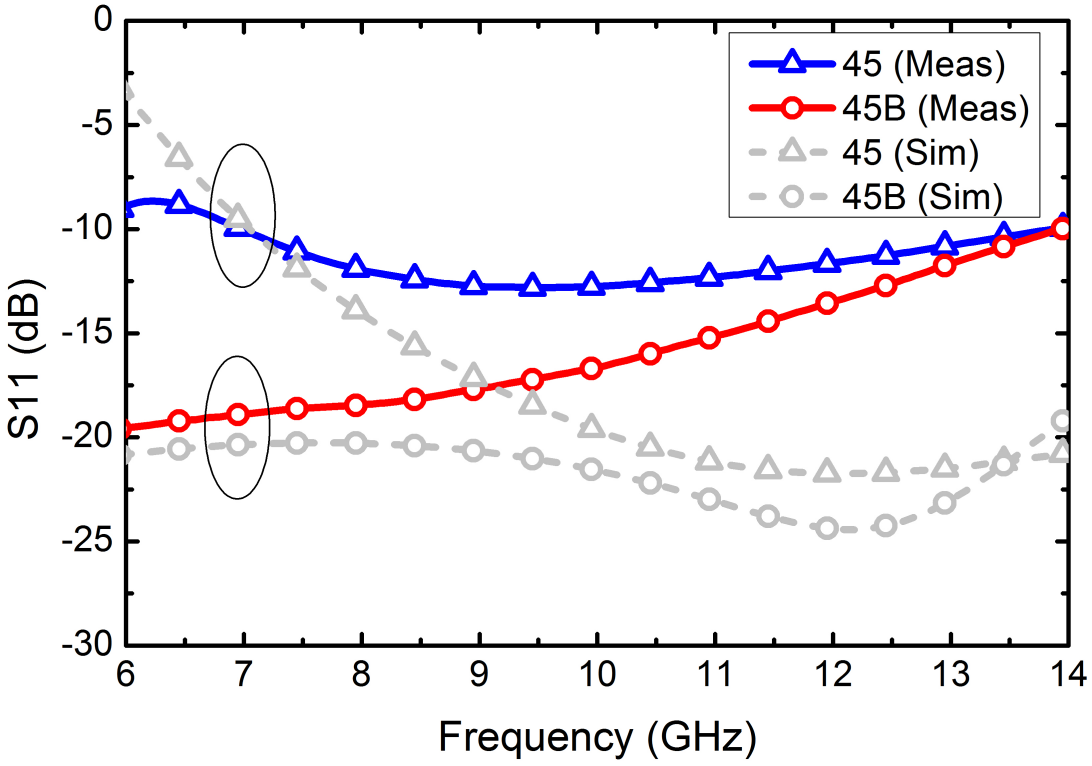

Figure 27: Simulated and measured return losses of 45° bit in both phase shift and bypass modes.

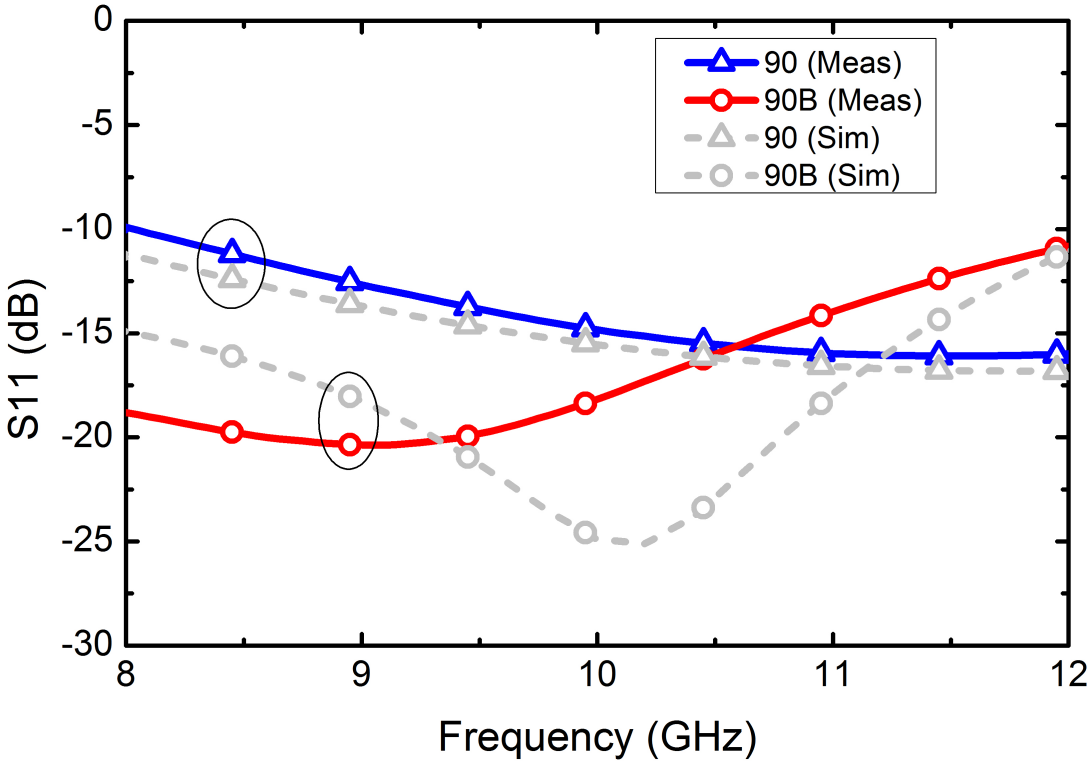

Figure 28: Simulated and measured return losses of 90° bit in both phase shift and bypass modes.

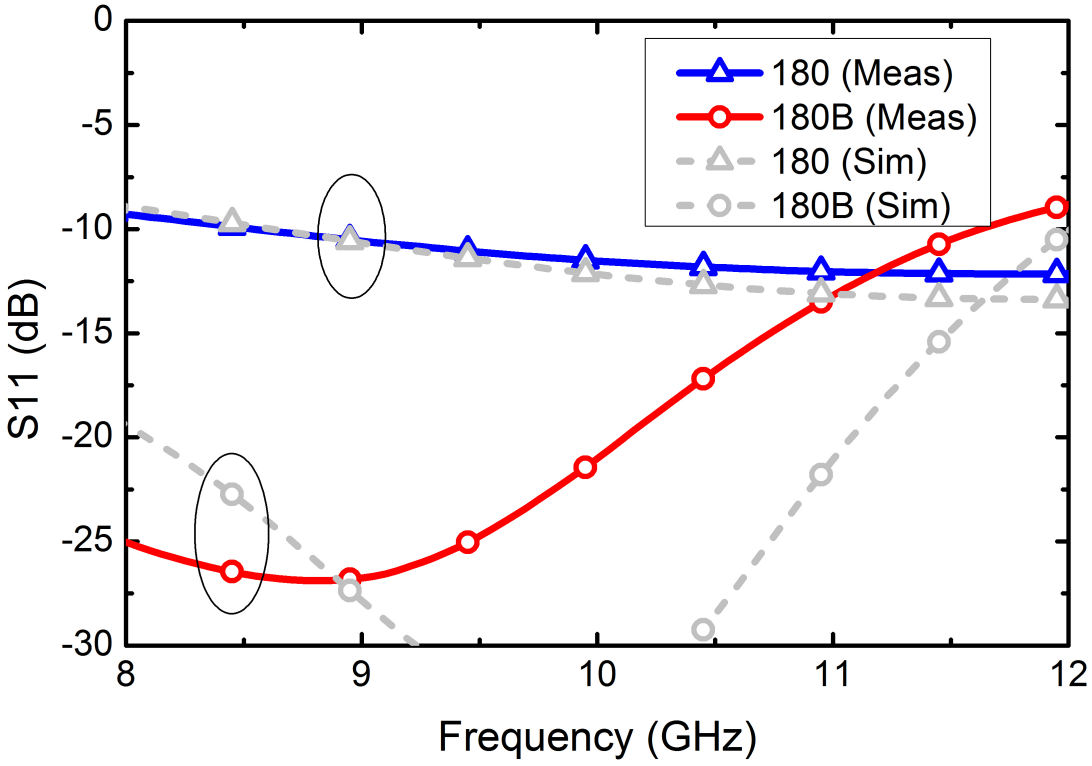

Figure 29: Simulated and measured return losses of 180° bit in both phase shift and bypass modes.

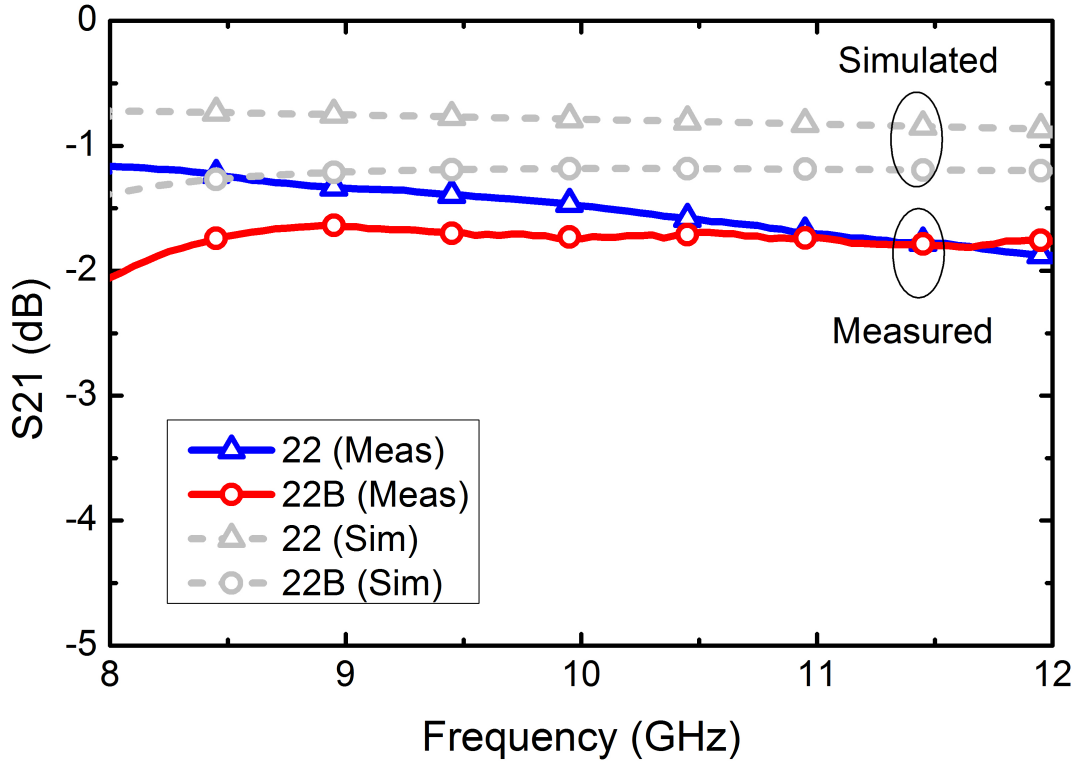

Figure 30: Simulated and measured insertion losses of 22.5° bit in both phase shift and bypass modes.

return losses of the 45°-bit is better than 10 dB almost in 7-14 GHz range as shown in Fig. 27. Fig. 28 shows that the 90°-bit has good agreement between simulation and measurements and they are just better 10 dB at X-band. The 180°-bit has a similar result to the 90°, and its return losses are better than 10 dB for most of X-band frequencies as shown in Fig. 29. In short, return losses of all bits are better than either 10 or 15 dB across X-band.

3.4.2 Insertion Loss

There is a constant offset between insertion loss simulation and measurements. For the 22°-bit, measured insertion loss is in 1-2 dB range at X-band as shown in Fig. 30, while Fig. 31 shows that the 45°-bit has a 2-3 dB insertion loss across X-band frequencies. Although measured results are nearly double of the simulated values, up to 3 dB insertion loss is acceptable. The 90°-bit, as shown in Fig. 32, has a measured insertion loss of 2.2-4.2 dB at X-band for phase shift mode. In b bypass mode, however, it is around 4 dB only between 9-10.5 GHz range. A similar picture is shown in Fig. 33. The 180°-bit has an insertion loss of 3.7-7.0 dB in phase shift

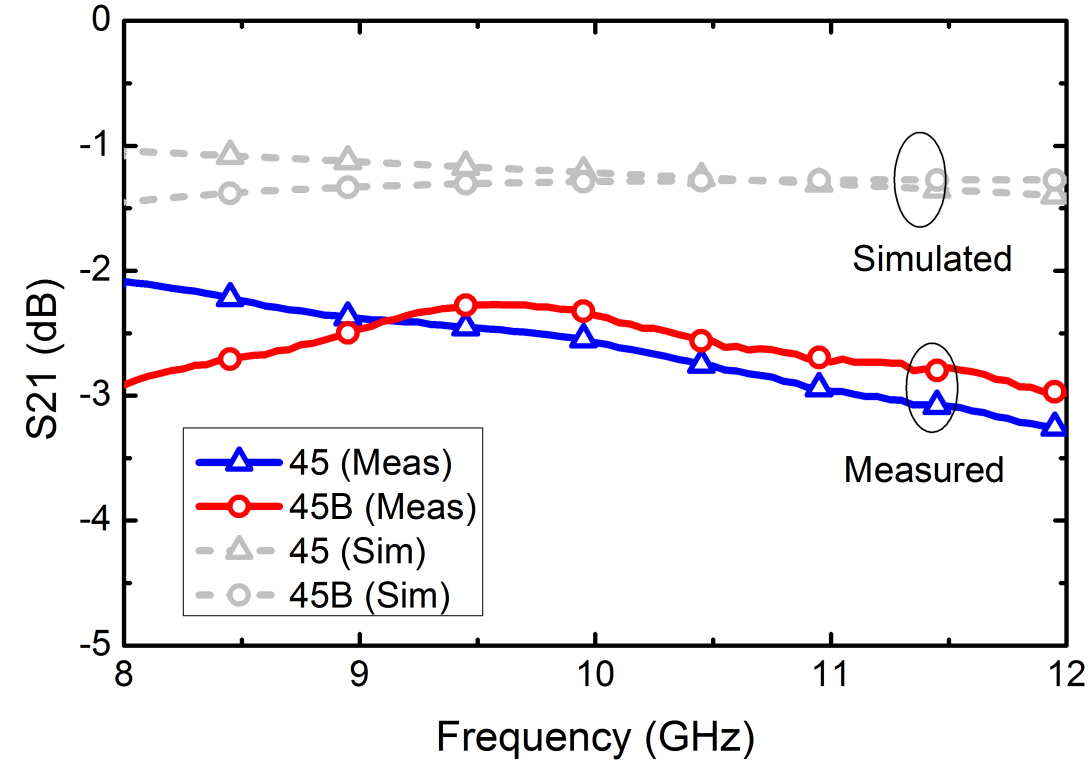

Figure 31: Simulated and measured insertion losses of 45° bit in both phase shift and bypass modes.

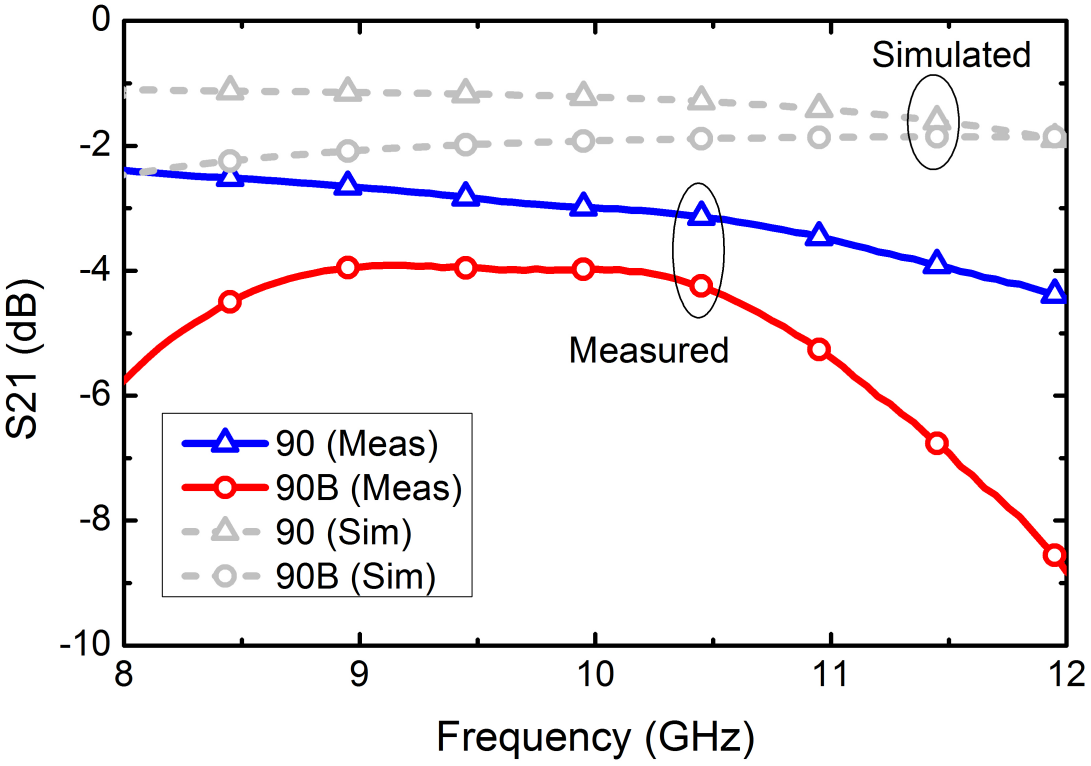

Figure 32: Simulated and measured insertion losses of 90° bit in both phase shift and bypass modes.

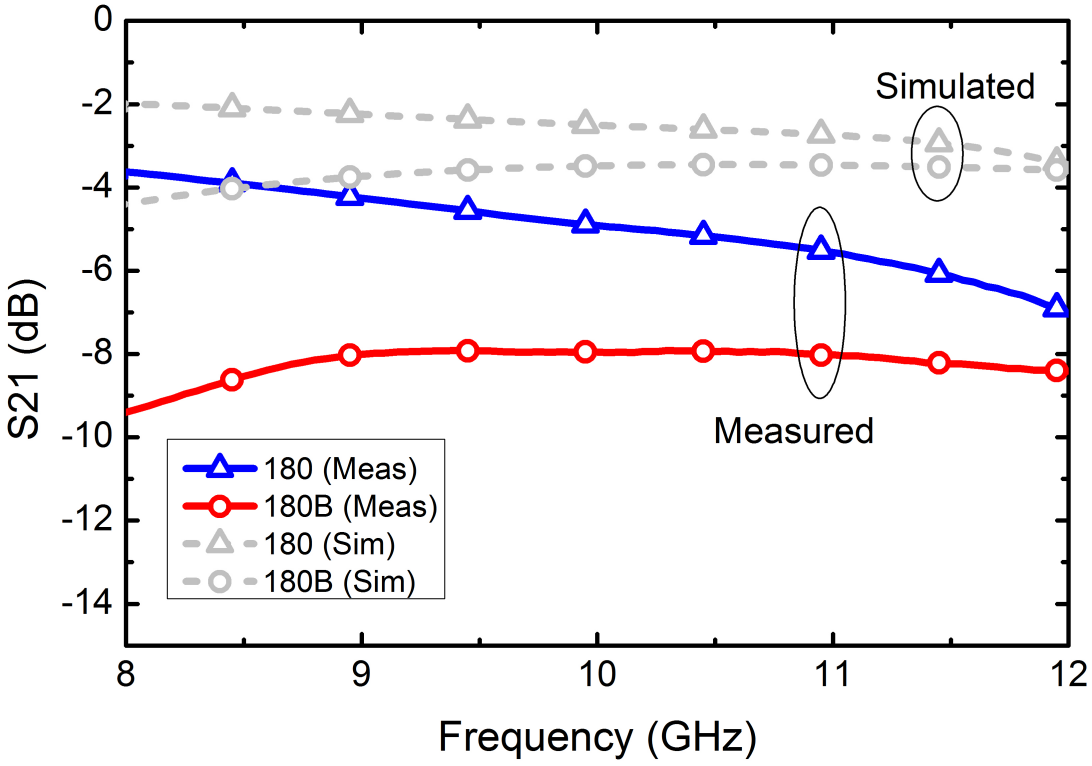

Figure 33: Simulated and measured insertion losses of 180° bit in both phase shift and bypass modes.

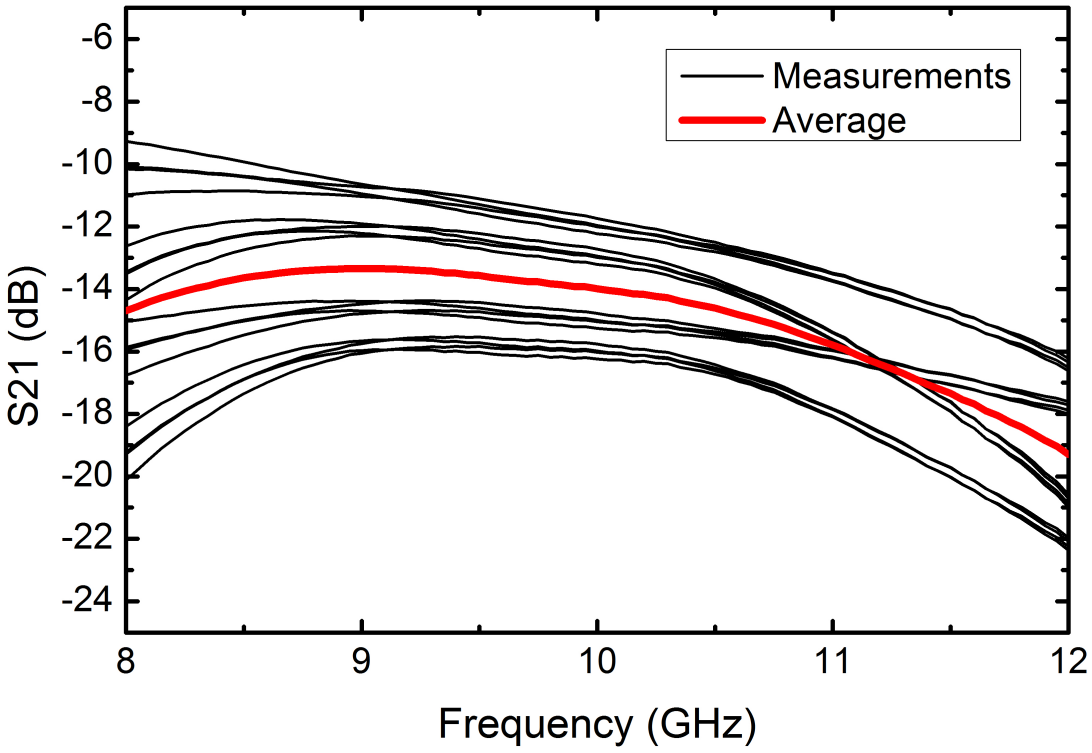

Figure 34: Extrapolated insertion losses of the 4-bit phase shifter from the measurements of standalone phase shifter bits.

mode and 7.5-9.5 dB in bypass mode.

Fig. 34 shows the overall insertion losses of all the bits combined, extrapolated from the measured results of standalone bits. The average insertion loss is 14 dB at 10 GHz. The biggest variation occurs at 8 GHz. The figure also shows that there are four clusters with similar return losses to each other. So, the variations in insertion losses are mainly generated by the 90° and 180°-bits.

3.4.3 Phase Shift

Despite the poor insertion loss performance of the phase shifter block, the phase shift performance is acceptable, at least in the vicinity of the center frequency of 10 GHz, as shown from Fig. 35-38. 22° and 45°-bits have a maximum error around 5° across X-band frequencies while having a phase shift of 21.5° and 45.5° phase shift at 10 GHz. These two bits' performance is very good. The 90° and 180° bits matches well with the simulations but only around 10 GHz, with a phase shift of 92° and 181° respectively. Their phase shift vs. frequency slopes are increased too much with respect to simulations, suppressing the useful bandwidth of the overall phase shifter.

Using the individual blocks' measured S-parameters, the insertion phase of the overall phase shifter is extrapolated as shown in Fig. 39. The solid lines are the measured phase shifts of standalone blocks, while the dotted lines are extrapolation results. The linear phase shift is observable around 10 GHz.

Finally, Fig. 40 shows the RMS phase and gain error for the overall 4-bit phase shifter. As low as 3° RMS phase error is achieved at 10.1 GHz, while it is better than 11° at 9.2-10.8 GHz band. Lowest RMS gain error of 1.5 dB is achieved at 10.6 GHz and it is better than 3.3 dB across X-band frequencies.

In summary, the presented 4-bit by-pass/lo-pass SiGe X-band phase shifter achieves better than 11° RMS phase error in 9.2-10.8 GHz range, allowing 4-bit operation, while achieving as low as 3° RMS phase error at 10.1 GHz. Average insertion loss is 14 dB at 10 GHz and the phase shifter has an input 1-dB compression point of 15 dBm. The power consumption is negligible ($< 1\ \mu$W).

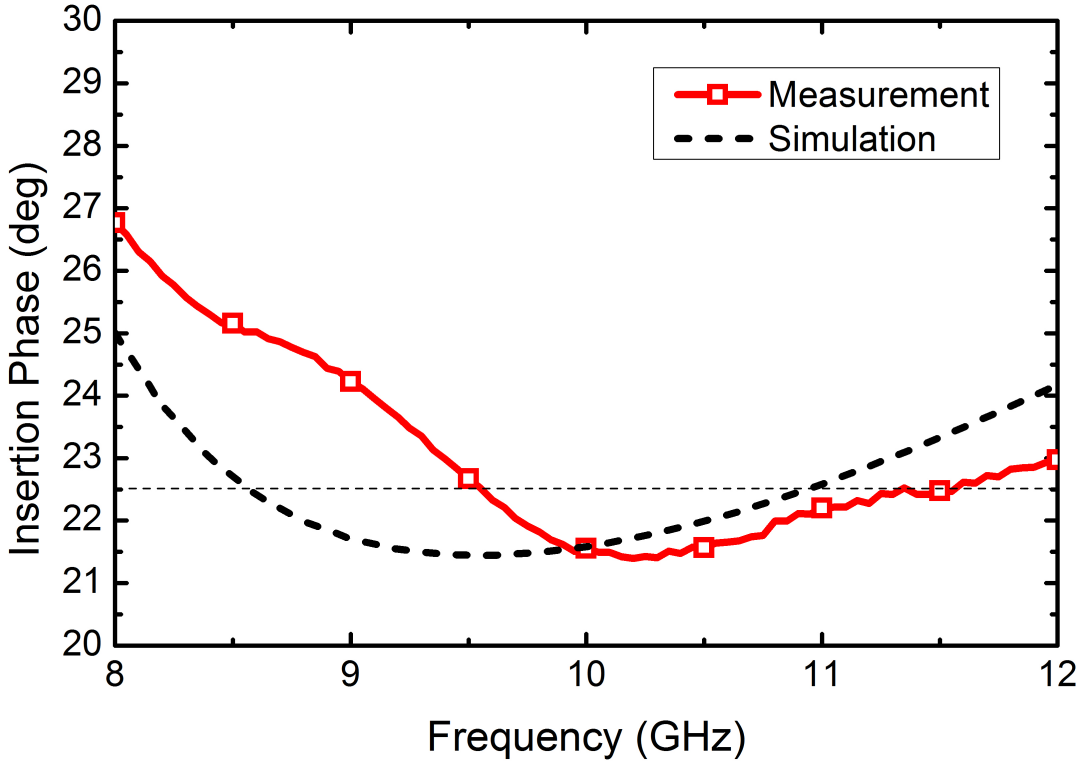

Figure 35: Simulated and measured phase shift of 22.5° bit.

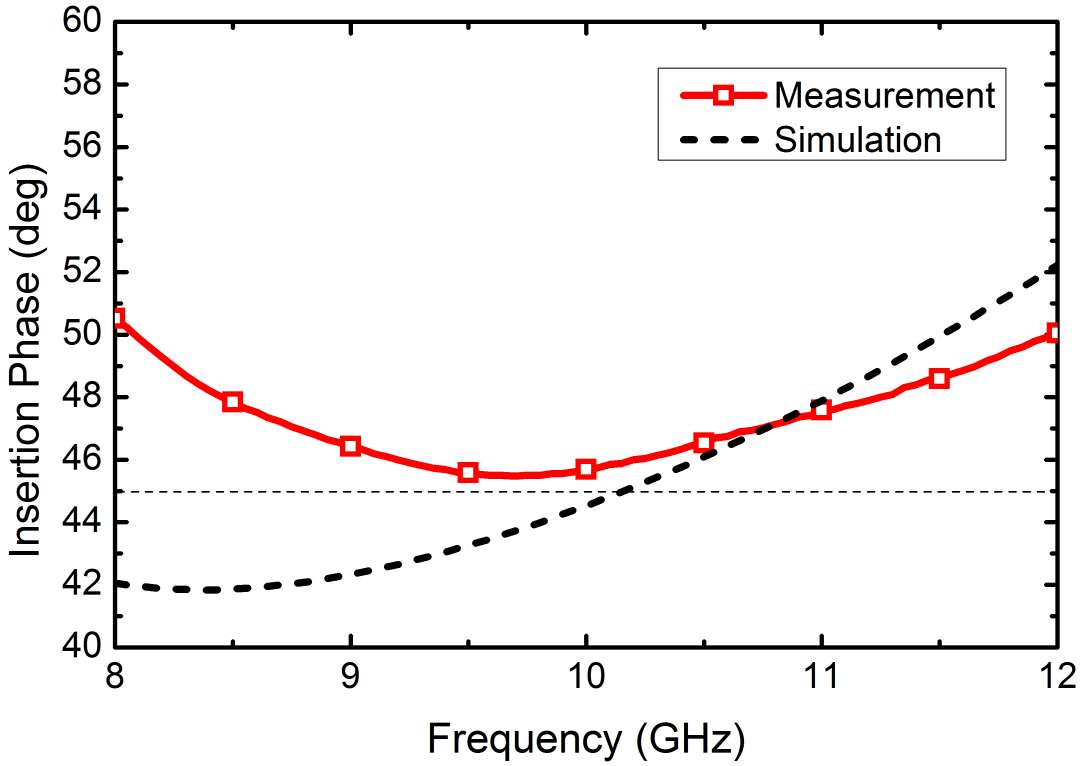

Figure 36: Simulated and measured phase shift of 45° bit.

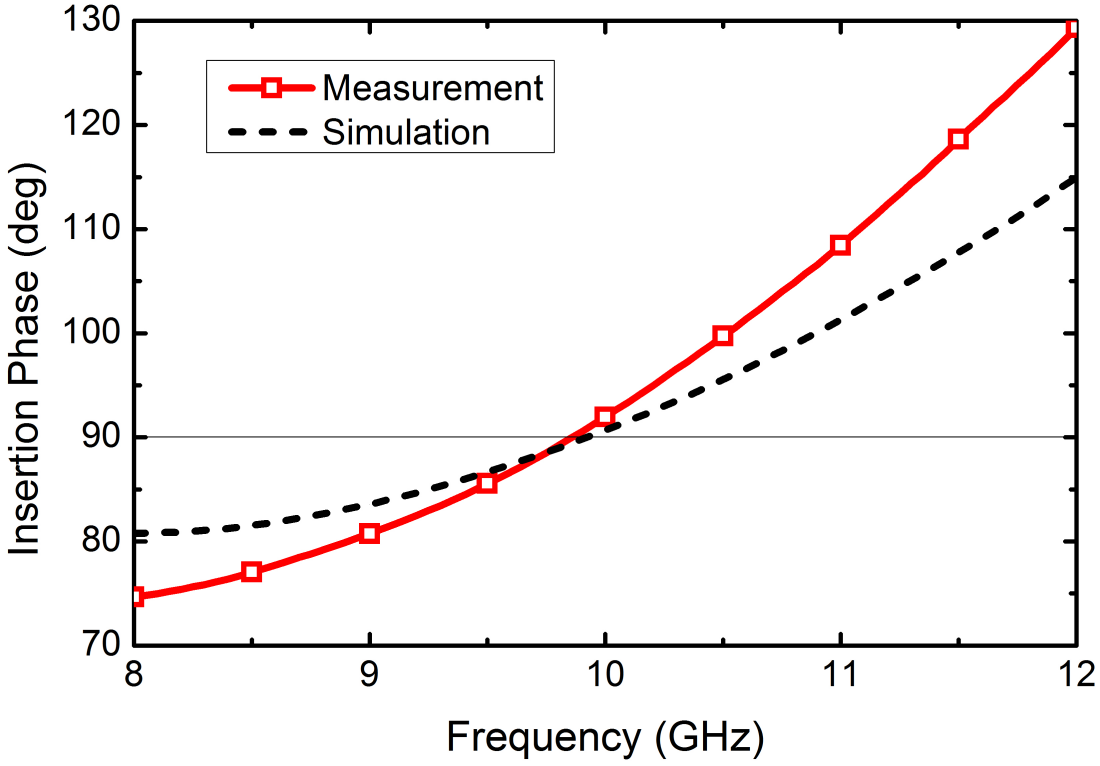

Figure 37: Simulated and measured phase shift of 90° bit.

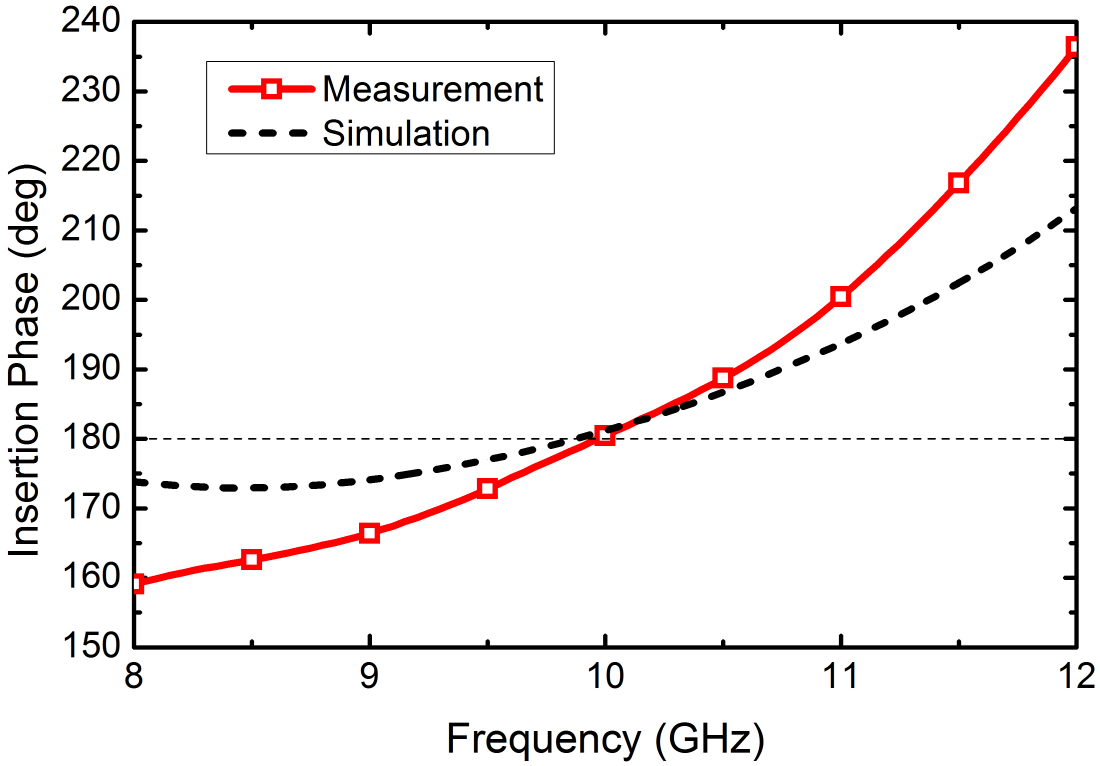

Figure 38: Simulated and measured phase shift of 180° bit.

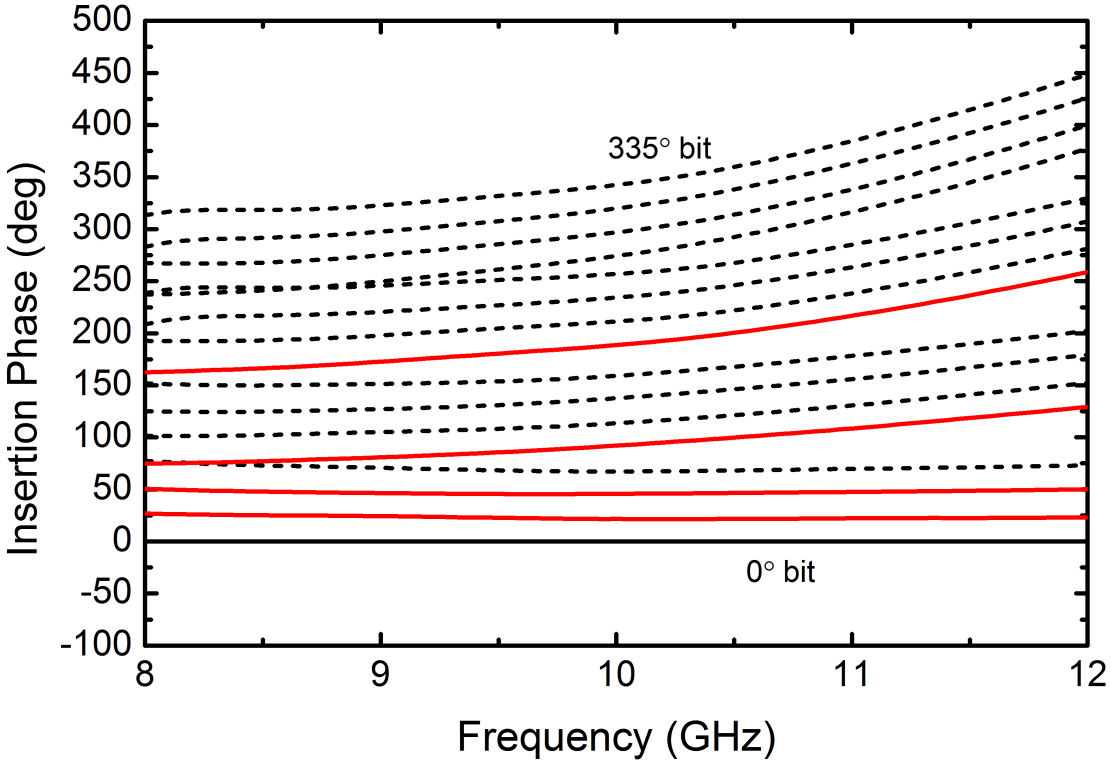

Figure 39: Extrapolated 16 phase states from the measurements of 4 standalone phase shifter bits.

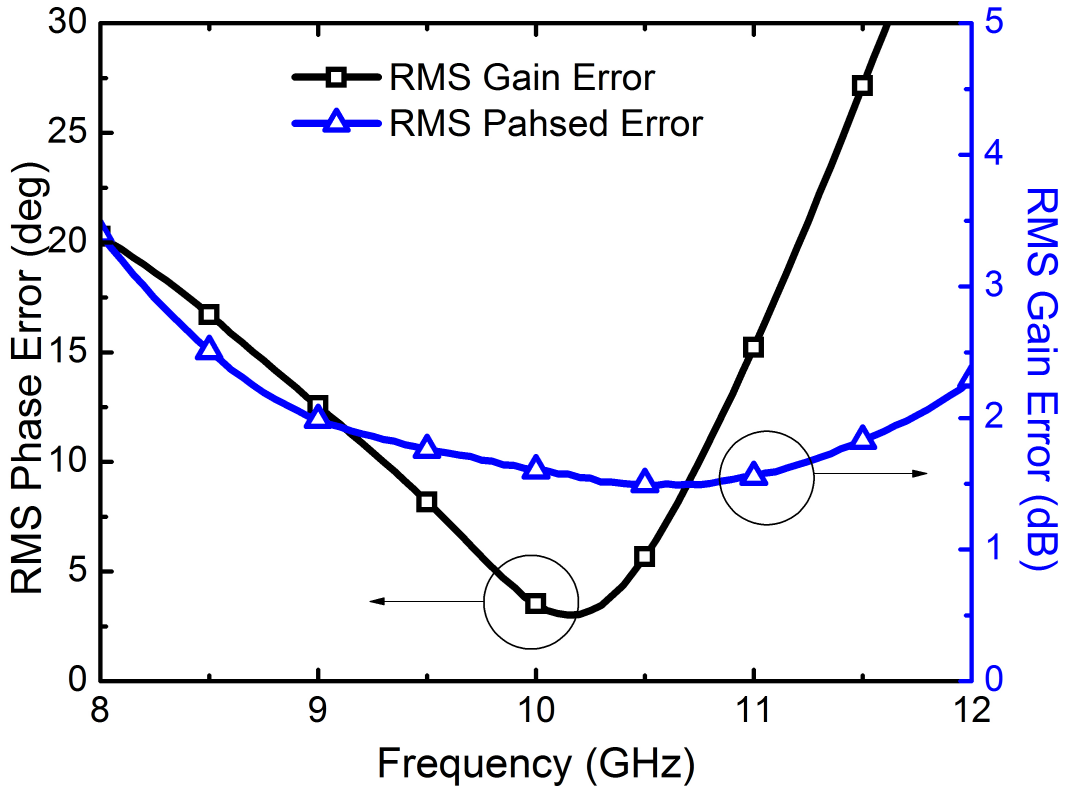

Figure 40: Measured RMS phase and gain error of 4-bit phase shifter.

3.5 Comparison

Table 6 shows the comparison between the presented 4-bit SiGe X-band phase shifter with the similar works in the literature. The presented work shows significant reduction in chip size with respect to hi-pass/lo-pass topologies at the expense of reduced bandwidth, while achieving the highest 1-dB compression point. The presented phase shifter also achieves wider bandwidth than [24] where by-pass/lo-pass topology is used as well. The best phase error performance is achieved by [25].

Table 6: Comparison of 4-bit SiGe X-band phase shifters with reported works

Frequency (GHz)	Num. of bit	RMS Phase Error (deg)	Ins. Loss (dB)	RMS Gain Error (dB)	Input P_{1dB} (dBm)	Power Diss. (mW)	Chip Size (mm^2)	Topology	Process	Ref.
9.2 – 10.8	4	3 – 11	10 – 20	2	15	0	0.9	Bypass/Lopass	0.25-μm SiGe (CMOS)	This work
9.1 – 10.3	4	< 11	8.7	1	N/A	0	0.9	Bypass/Lopass	0.25-μm SiGe (CMOS)	[24]
8 – 12	5	<8	14 – 18	N/A	4.4	248	9.8	Hipass/Lopass	0.13-μm SiGe (HBT)	[26]
8.5 – 10.5	5	<9	<21	N/A	7	<1	4.8	Hipass/Lopass	0.13-μm SiGe (CMOS)	[27]
8 – 12	4	2.7 – 5	2.1	1	-5.4	8.7	0.2	Vector Mod.	0.13-μm Si (CMOS)	[25]
11 – 13	Cont.	N/A	5 – 8	0.8	N/A	0	1.68	RTPS	0.15-μm pHEMT	[28]

4 SiGe X-band T/R Module

4.1 Proposed T/R Module Architecture

This chapter presents the design and measured results of a single-chip transmit/receive (T/R) module at X-band in SiGe BiCMOS technology. The all-RF T/R module shown in Fig. 41 includes an LNA, a PA, two SPDT switches, a phase shifter and a VGA. The 4-bit by-pass/lo-pass phase shifter presented in Chapter 4 is integrated into the complete T/R module. There are a couple of T/R switches developed to be integrated into the module, as presented in [29]. However, their lowest achieved insertion loss is 2.3 dB, which would degrade the T/R module noise figure in receive mode. Also, including the T/R switch in the module would break the compact layout of the module and increase the chip area by 20%. For those reasons, the T/R module is not included in the developed T/R module and it is assumed that output of the module can be connected to the antenna by MMIC switches (with as low insertion loss as 0.5 dB) or circulators.

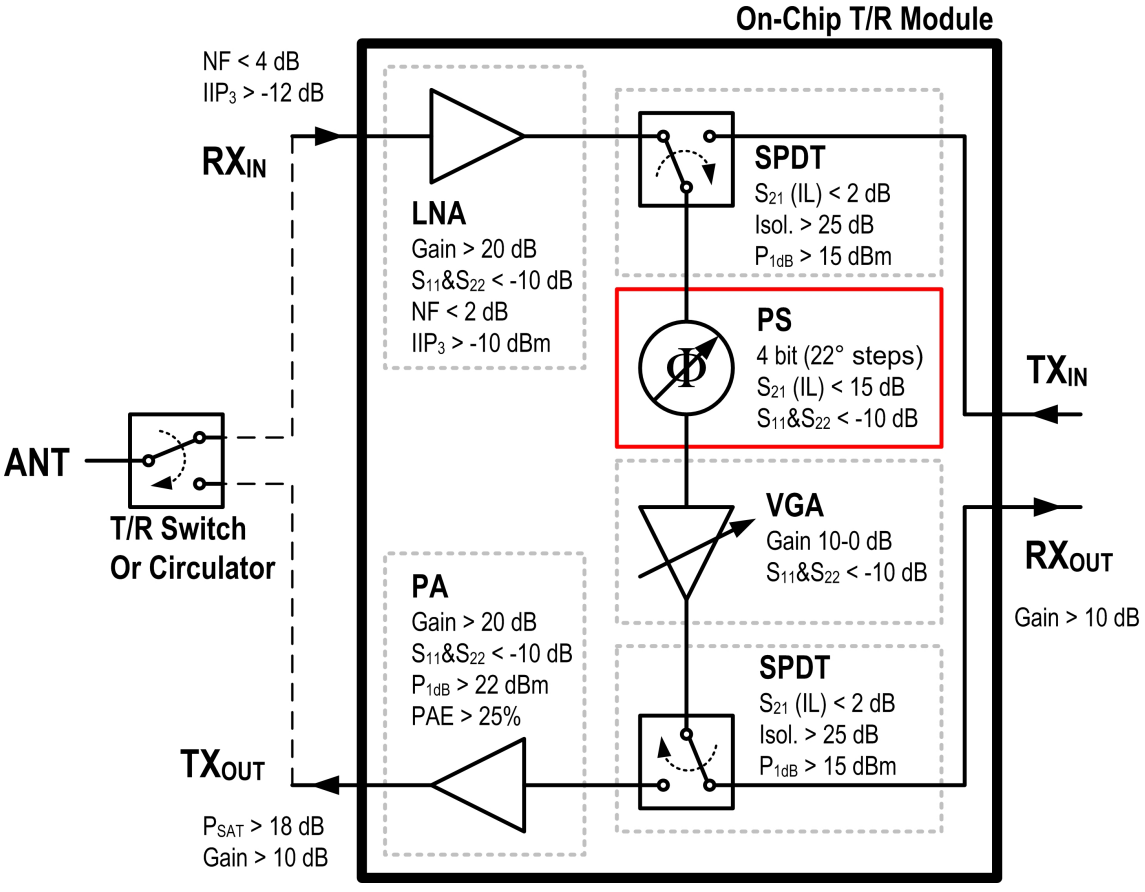

Figure 41: Proposed SiGe X-Band T/R Module Architecture

Initially, the module is planned to achieve a transmit/receive gain of 20 dB with a noise figure of 2.5 dB in RX mode and an output power of 22 dBm at TX mode.Also, it is aimed to achieve the smallest chip area for X-band T/R modules with low power consumption. In the light of these values, the specifications of each block is determined. Input and output of all blocks will be matched to 50 Ω.

Single-pole double-throw (SPDT) switches are required to have an insertion loss less than 2 dB in order to route the signal from TX_{IN} to TX_{OUT} and from RX_{IN} to RX_{OUT}. They require at least 25 dB of isolation to reduce the coupling between TX and RX paths. Since the output of the LNA will not carry a high-power signal, a very high P_{1dB} is not required for SPDTs, 15 dBm is suitable.

Low noise amplifier (LNA) is required to have sufficient gain (>20 dB) and minimum noise figure (<2 dB) in order to suppress the noise contributions of the following blocks, as can be seen in Friis equation [30]

$$F_{Total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + ... \tag{29}$$

where F_n is the noise factor and G_n is the power gain of each block in linear scale. Also LNA is required to an IIP_3 higher than -10 dBm to achieve a high dynamic range.

Power amplifier (PA) is required to have higher than 20 dB linear gain and an output power of at least 22 dBm. In this way, assuming a typical X-band antenna gain of 6 dB and subtracting possible losses due to T/R switch and interconnection, 26-27 dBm (400-500 mW) radiated output power per element can be realizable which would satisfy the requirements for commercial phased array applications. Target power-added-efficiency is 20%.

Phase shifter (PS) is the critical block of the T/R module. Low insertion loss, low phase and gain variation are required. Lower than 8 dB insertion loss is needed to achieve the complete T/R module target specifications given above. Higher insertion loss would degrade all three performance parameters. Due to the use of digital phase shifting, a variable gain amplifier (VGA) is required right after the PS in order to compensate the loss and loss variation in the PS.

4.2 SiGe BiCMOS Technology

SiGe BiCMOS technology is a very promising candidate for commercial phased array applications at X-band and beyond due to its lower cost, higher integration potential of RF front-end circuits with baseband blocks, higher yield and manufacturing capabilities. In this work, a 0.25-μm SiGe BiCMOS process (SG25H3), offered by IHP Microelectronics, is used to realize the X-band T/R module. This technology offers three different kinds of heterojunction bipolar transistors (HBTs) with high speed (110/180 GHz f_T/f_{MAX} and 2.3 V BV_{CE0}), high voltage (7 V BV_{CE0}) and medium voltage (7 V BV_{CE0}) options available, as well as NMOS transistors for switching and digital applications. This technology also provides passives such as high-Q metal-insulator-metal (MIM) capactiros, two thick top metal layers with 2 and 3-μm thickness for high-Q realizations and various kinds of poly and diffusion resistances. All of the building blocks and the complete T/R module is realized in this technology.

4.3 Previously Designed Blocks

4.3.1 SPDT Switch

Fig. 42 shows the schematic of the SPDT switch design [31]. It is based on series-shunt topology. When control voltage is high, M_1 and M_3 operates in deep-

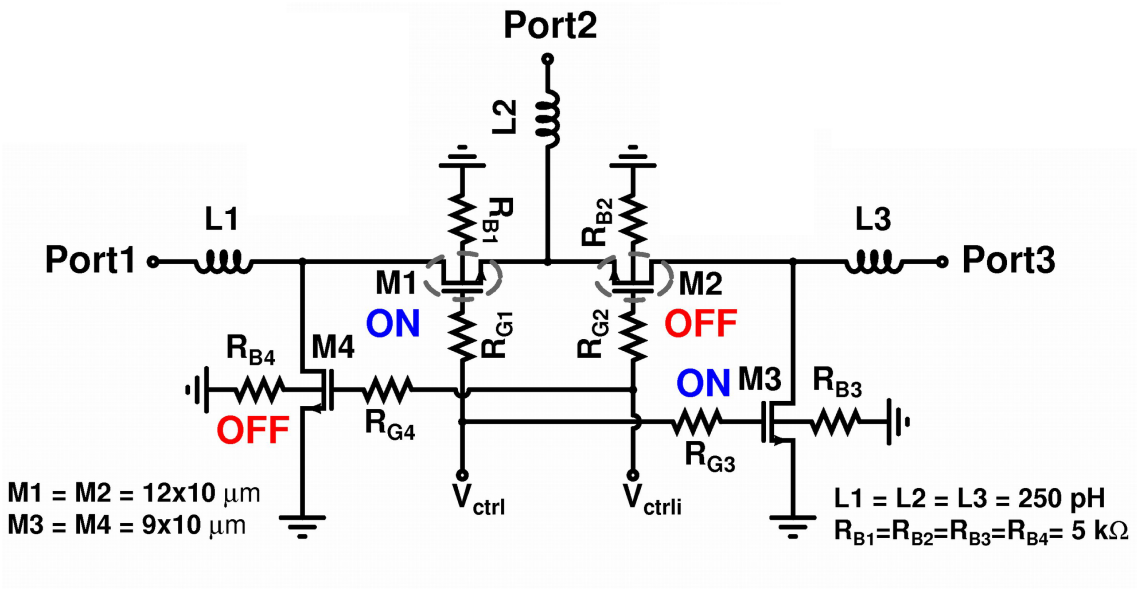

Figure 42: Schematic view of the SPDT switch

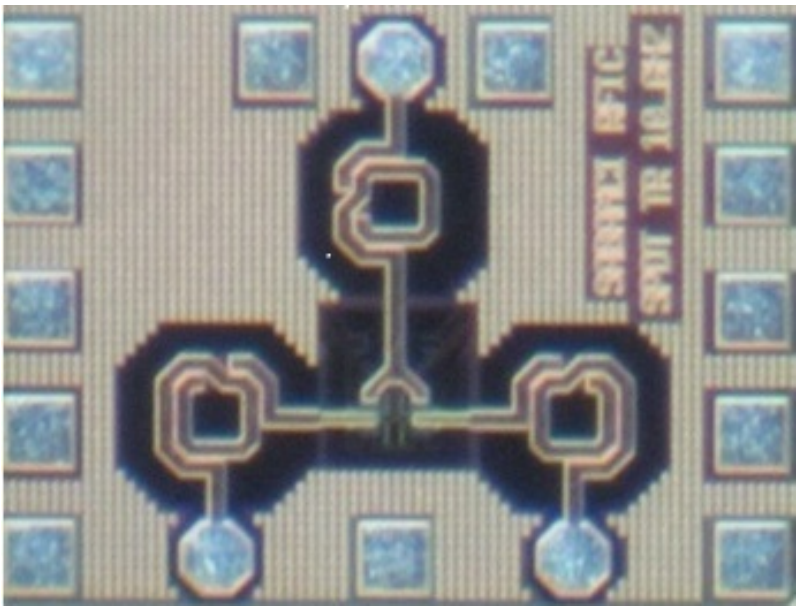

Figure 43: Chip photo of the SPDT switch. Chip area is 0.48x0.36 mm^2

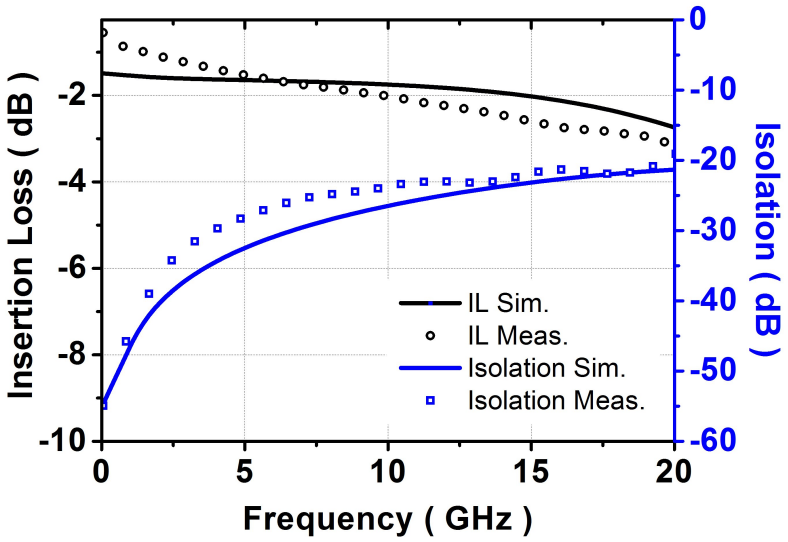

Figure 44: Simulated and measured insertion loss and isolation of the SPDT switch

triode region while M_2 and M_4 operate in cut-off region. In this mode, there is a low impedance path between port 2 and port 1 while port 3 is isolated. M_1 and M_2 transistors perform the switching function while M_3-M_4 transistors are used to improve the isolation by grounding any RF leakage to the isolated port. The insertion loss mainly depends on the channel resistance, which depends on the transistor width in deep-triode region for a given V_{Gs} voltage and mobility. Therefore larger-width transistors are required to lower the insertion loss. However, capacitive coupling to substrate increases by increase transistor dimensions, increasing the insertion loss.

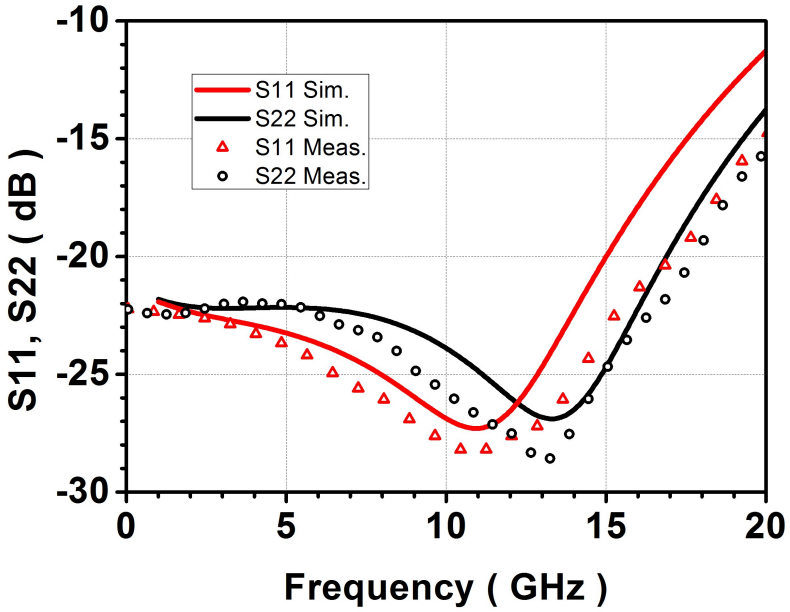

Figure 45: Simulated and measured input/output return losses of the SPDT switch

So, transistor widths are optimized for lowest insertion loss. Additional techniques such as S/D biasing, gate/body floating and parallel resonance are used to improve the isolation and power handling of the switch.

Fig. 43 shows the fabricated SPDT switch. It has a small chip size of 0.48x0.36 mm^2 without pads. Measurements show that the switch has insertion loss of 2 dB at X-band and lower than 3.2 dB from 0-20 GHz (Fig. 44) and the input/output matching is better than -20 dB at X-band (Fig. 45). The isolation of the switch is better than 23 dB and the input P_{1dB} is 17 dBm at X-band.

4.3.2 Low Noise Amplifier

Fig. 46 shows the designed low noise amplifier circuit schematic [32]. It is a two-stage amplifier where each stage is using cascode topology, to achieve 20 dB gain requirement. Cascode topology is chosen for its better stability then CE topology at high frequencies at the expense of slightly increased noise figure. First stage is designed using simultaneous input noise and power matching technique. First, an optimum base-emitter voltage is selected for a unit-sized device to achieve the best trade-off between NF_{min} and IIP_3. Second, transistor sizes are increased and capacitors C_ext are inserted between base and emitter of the driver transistors, to achieve an optimum source resistance of 50 Ω. Third, an inductor degeneration is

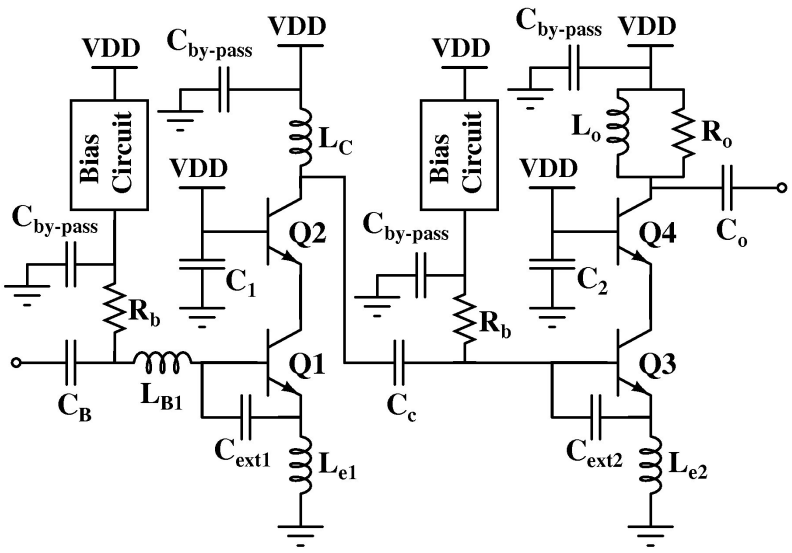

Figure 46: Schematic view of the two stage LNA.

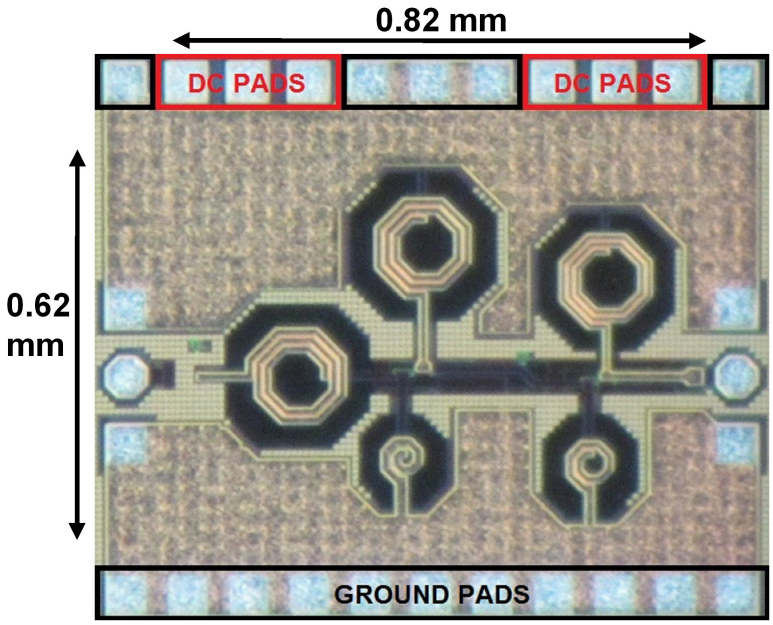

Figure 47: Chip photo of the fabricated LNA.

introduces, which sets the real part of input impedance to 50 Ω and also improves the linearity. Finally, another base inductor is used to achieve the rest of the matching. Output of each stage is loaded with inductors to achieve highest voltage swings and minimal noise contribution. The second stage design is similar but it operates at a higher current in order not to degrade the overall IIP_3 of the LNA. Bias circuits are connected to the base of HBTs via 5 kΩ resistors and output of bias circuits are terminated with bypass capacitors, to reduce their effect on the noise figure of the LNA.

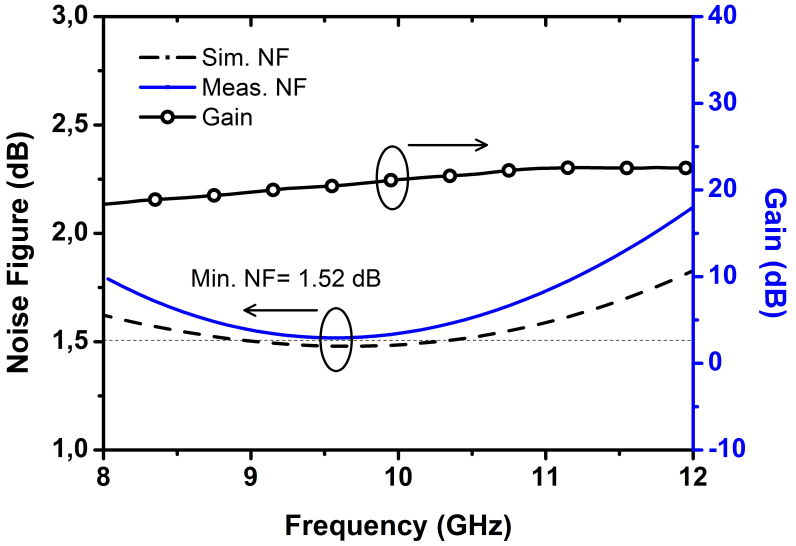

Figure 48: Gain and noise figure of the LNA.

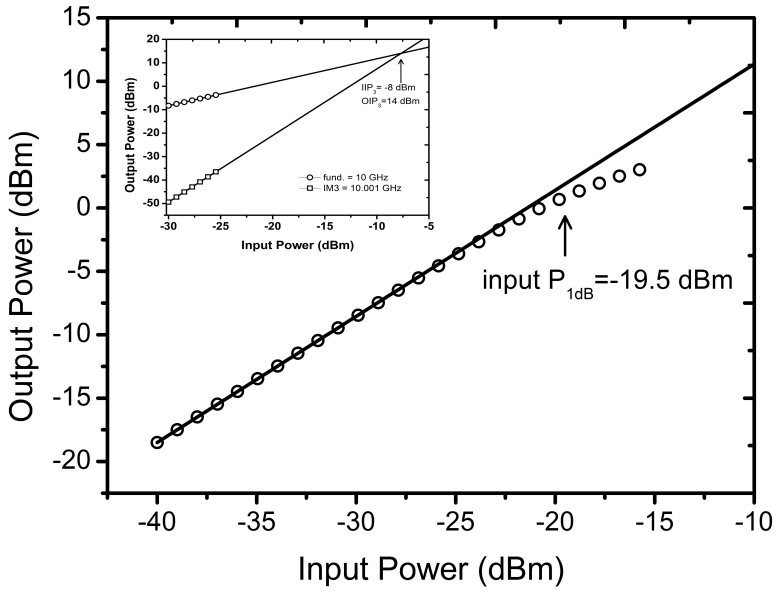

Figure 49: Single-tone and two-tone linearity measurement results of the LNA.

The fabricated LNA chip is shown in Fig. 47. It employs five spiral inductors and the chip area excluding measurement pads is 0.5 mm^2. First and second stage draw 2.5 mA and 7.5 mA, respectively, from a 2.2 V supply, for o total power consumption of 22 mW. The measured results are shown in Fig. 48-49. The LNA has a small signal gain of 22 dB and a reverse isolation of -47 dB across X-band frequencies. Input and output ports are well matched, S_{11} is varying between -11 and -22 dB while S_{22} is between -12 and -20.5 dB at X-band.

LNA achieves 1.52-2.1 dB noise figure across X-band frequencies, with a mean noise figure of 1.65 dB, very competitive pr better than other reported SiGe X-band

LNAs. The linearity measurements show that LNA achieves input 1-dB compression point of -19.5 dBm and input referred third order intercept point of -8 dBm.

4.3.3 Power Amplifier

A linear two-stage power amplifier is designed for the T/R module as shown in Fig. 50 [33]. Each stage is composed of cascode topology. The high speed transistors are used as driver transistor of the cascode pair, while medium votlage transistors (with higher breakdown voltages) are used as the common base transistor in the cascode pair to overcome the low breakdown voltage of silicon technologies. Active bias networks are used to improve the linearity. C_3 capacitor is shunted with an RC

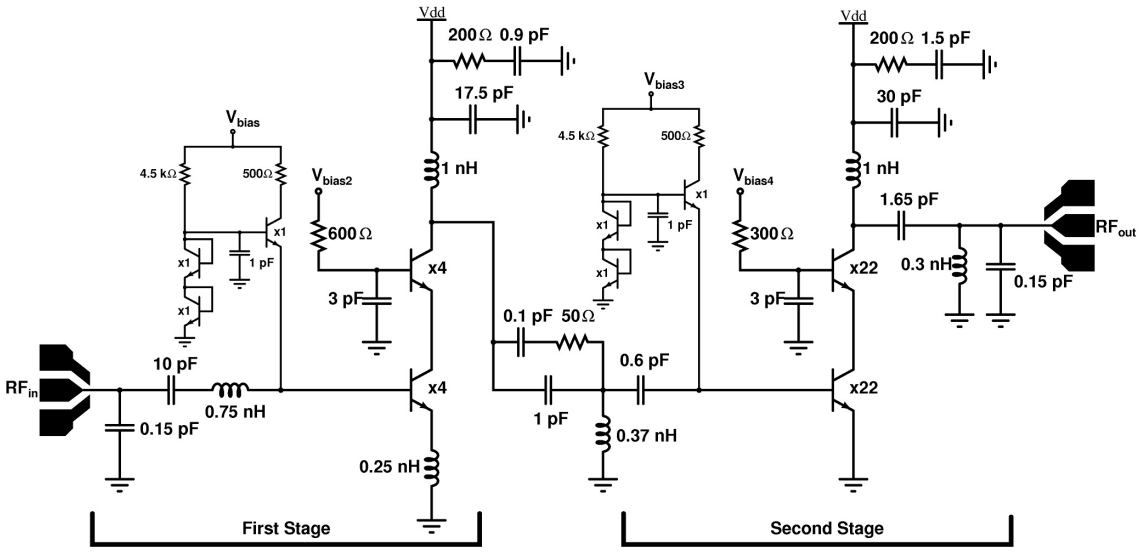

Figure 50: Schematic view of the two stage power amplifier.

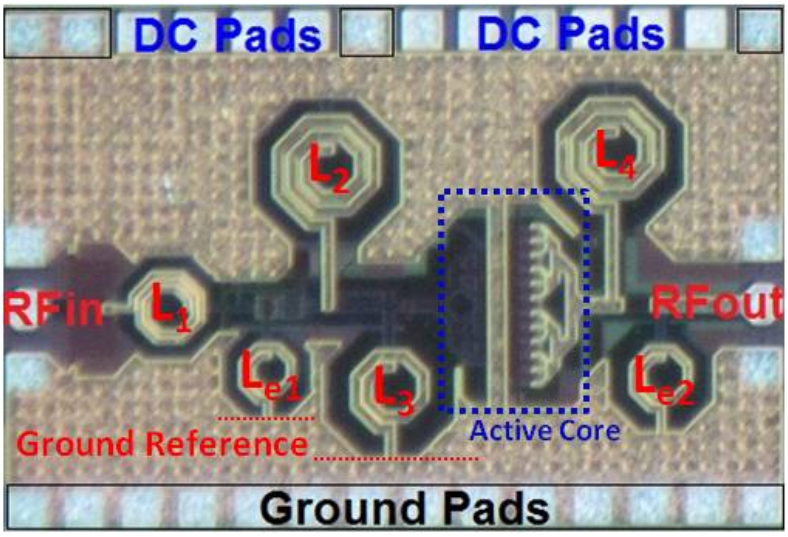

Figure 51: Chip photo of the fabricated PA.

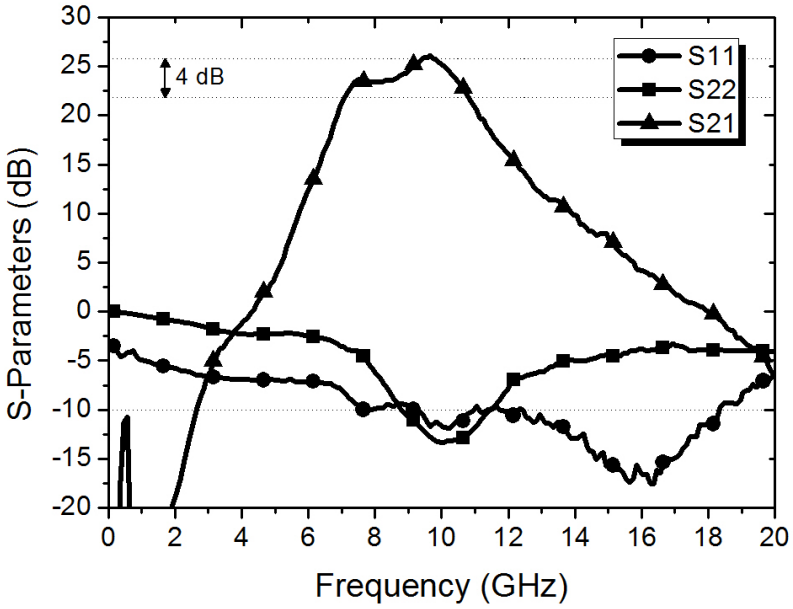

Figure 52: Measured gain and return losses of the PA.

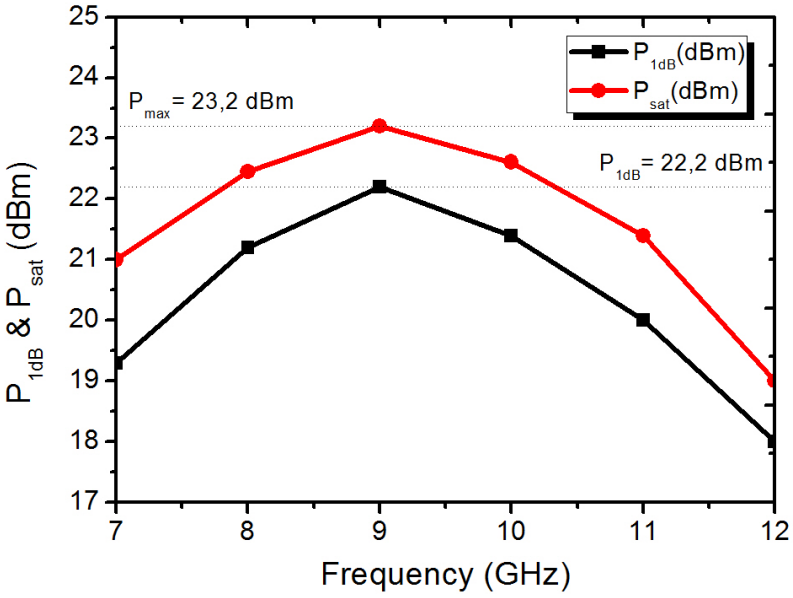

Figure 53: Measured 1-dB compression point and saturated output power of the PA.

network to improve the stability.

Fabricated PA chip photo is shown in Fig. 51 and it occupies 0.6 mm^2 chip area. It has a small signal gain of 25 at X-band as shown in Fig. 52. Input return loss is better than 10 dB at X-band, while output return loss is better than 10 dB only in a 2 GHz bandwidth, since the output of the PA is optimized for maximum output power by load-pull simulations. Large signal measurement results are shown in Fig. 53. PA achieves an output-referred 1-dB compression point of 22 dBm and

saturated output power of 23 dBm. Operating at 1-dB compression point, PA draws 100 mA from a 4 V supply. The resulting PAE is 28%.

4.4 Implementation

The T/R module architecture shown in Fig. 54 is integrated using the previously designed blocks. In the phase shifter presented in Chapter 3, the 4 bits were separate. Those separate bits were merged and integrated into the T/R module. During this process, the layout of the phase shifter is slightly modified due to the system level layout of the complete T/R module. The bit ordering is optimized for minimum RMS phase error under some layout constraints. Also, in order to compensate the losses introduced by the phase shifter, a VGA is used right after the PS. VGA is based on variable transconductance topology. It is based on [34], where the MOSFET is replaced by a resistor and the variable gain is obtained by controlling the bias of the common base transistor.

The fabricated SiGe X-band T/R module is shown in Fig. 54. The T/R module

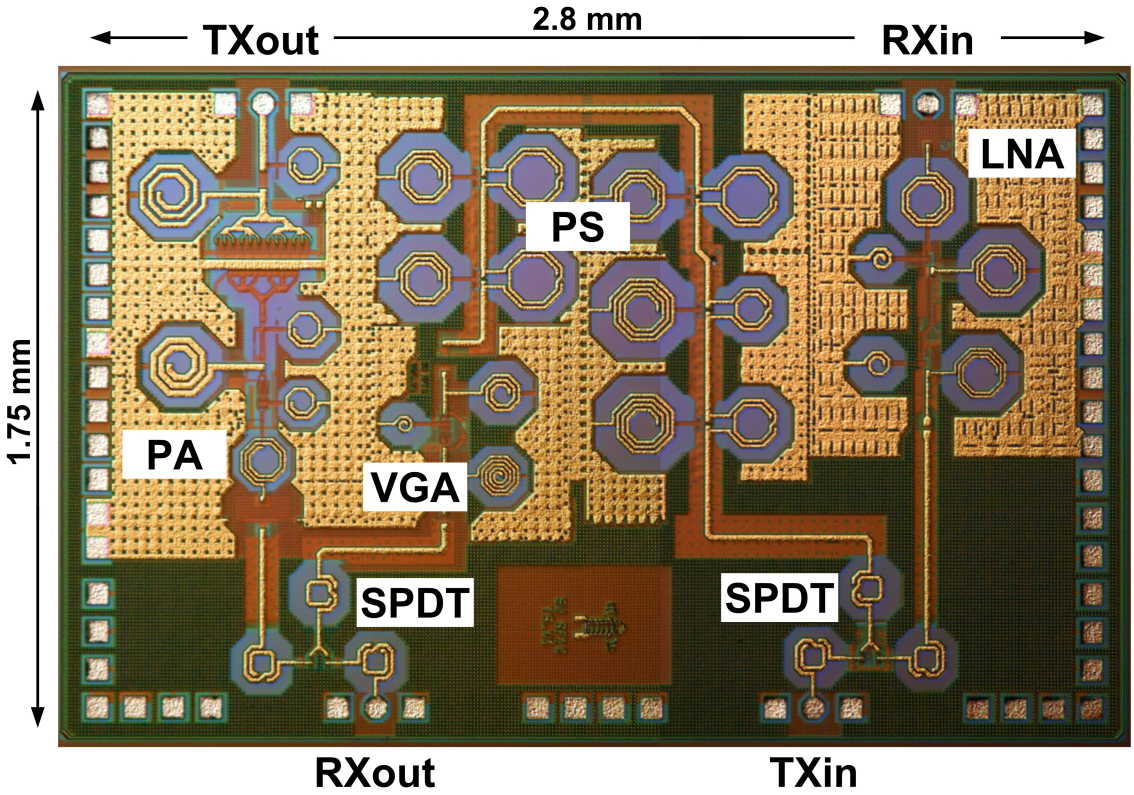

Figure 54: Chip photo of the fabricated SiGe X-Band T/R module. Chip size is 4.9 mm^2.

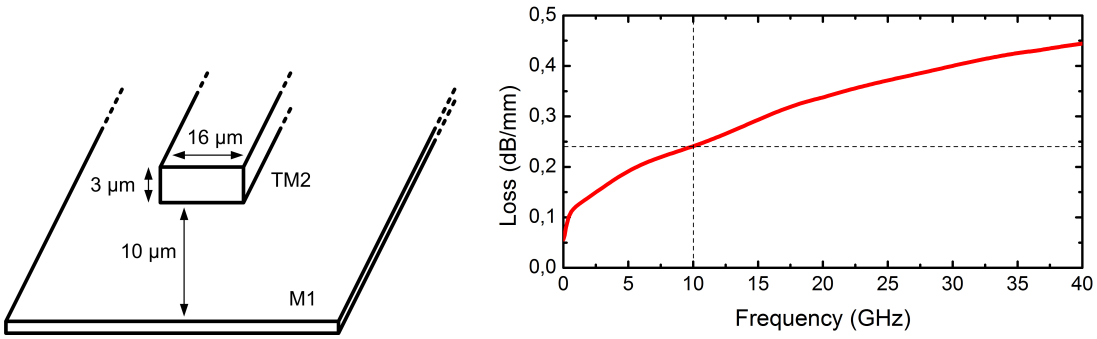

Figure 55: (a) Designed microstrip transmission line in SiGe BiCMOS process (b) Simulated line loss at Sonnet

occupies 4.9 mm^2 chip area. The chip includes large number of DC pads as shown in the figure. The reason is that the DC supplies of different blocks are not merged, in order to track the power consumption of each block separately to see if they match their own performance. Another reason is that a large number of ground pads are included, distributed throughout the chip and supported by very large number of substrate contacts to ground the substrate as much as possible.

For the interconnections between the building blocks, microstrip transmission lines are custom designed and used. The microstrip line is realized using the thickest top metal in the process as the signal line and the bottom metal line as the ground plane. The geometry can be seen in Fig. 55. Electromagnetic simulations result in a line impedance of 49.6 Ω and a line loss of 0.24 dB/mm^2. All of the inductors used in the T/R module is also custom designed and most of them has a quality factor higher than 20.

4.5 Measurement Results

To test the performance of the SiGe X-band T/R module, a printed circuit board is designed and the chip is stick to the PCB with conductive epoxy. Then the DC pads are wire-bonded to the PCB. During this process, large number of DC pads with 30-μm spacing caused some problems within the capabilities in our lab. The main problem is the lack of ESD protection at the pads. There are large number of control pads in the T/R module that is connected to the gates of NMOS transistors (8 for the phase shifter and 2 for each SPDT switch). Any potential ESD problem at one of those control pads, malfunctions the overall T/R module chip. Because

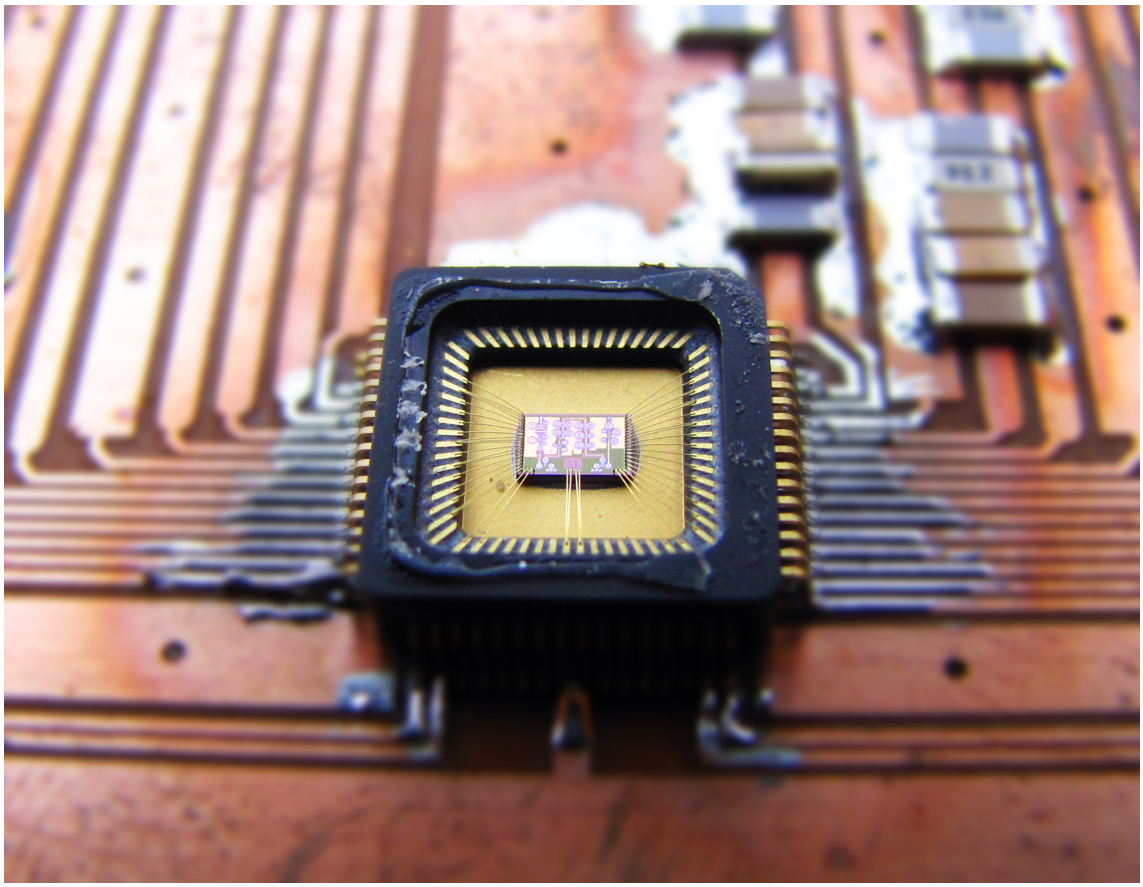

Figure 56: Simulated and measured gain of T/R module in receiver mode for all phase states

of this reason, the chips measured in this way is not functional in terms of RF performance, although LNA and PA are properly drawing desired currents from DC supplies.

In order to get ride of that problem, the T/R modules are sent to a professional bonding facility and the DC bads are wire bonded to a QFN-64 package and this package is soldered to a PCB test board, as shown in Fig. 56, including additional SMD bypass capacitors. In this way, potential ESD problems during the bonding process are alleviated. RF pads are not bonded and measurements are performed using a prob station after the metallic covers of the QFN package is removed.

For the performance evaluation of the SiGe X-band T/R module, S-parameter, noise figure, single-tone and two-tone linearity measurements are performed. For these measurements, Agilent 8720ES network analyzer, E4407B spectrum analyzer, E8267D vector signal generator, E4417A power meter and E3631A DC power supplies are used. Measurement results is presented in two sections:

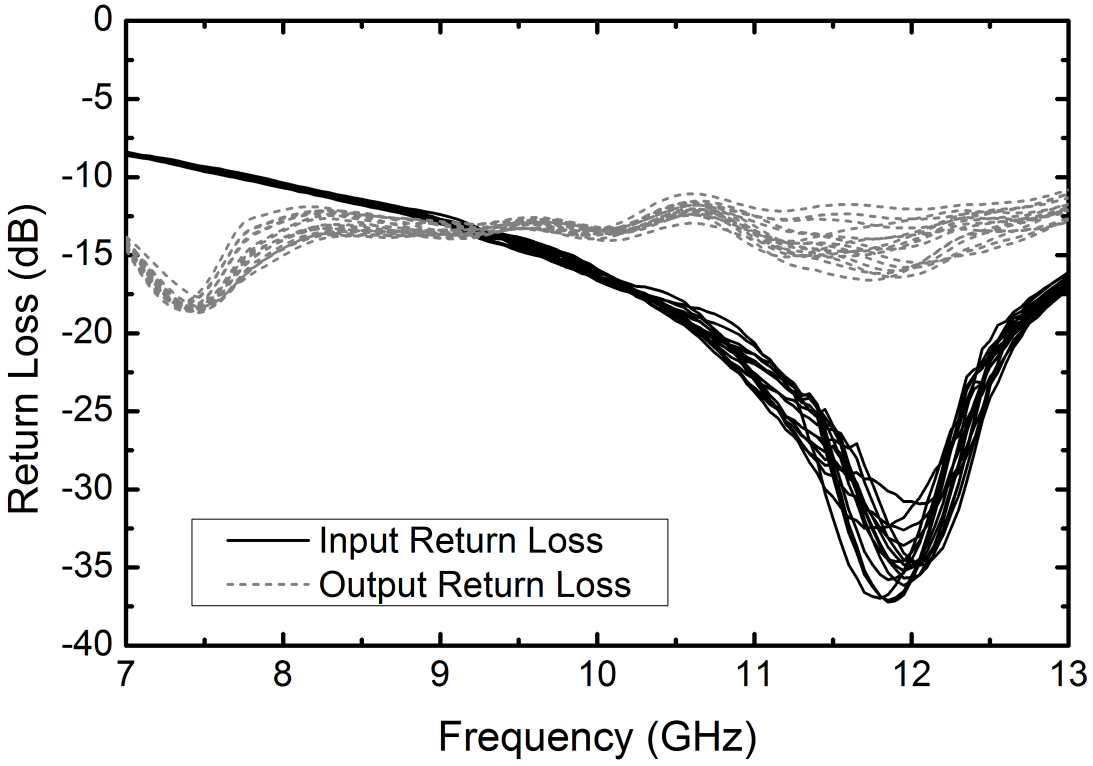

Figure 57: Measured input and output return losses of T/R module in receiver mode for all phase states

4.5.1 Receiver Mode

The measured S_{11} and S_{22} of the T/R module in RX mode is shown in Fig. 57. They are both better than 10 dB for at X-band for all phase states. The simulated and measured gains are shwon in Fig. 58. The average measured gain of the T/R module in RX mode is 11.5 dB at 10 GHz and it is better than 10 dB between 8.9 and 10.9 GHz. There is a 8-9 dB discrepancy between the simulated and measured data. This is mainly attributed to the excessive insertion loss of the phase shifter, that is presented in Chapter 3. The simulation results data for all the figures include the phase shifter simulations, therefore the deviations are consistent throughout all the measurement results.

Fig. 59 shows an illustration of the setup for measuring the noise figure of the module in RX mode, including Agilent 346A noise source and 87405C preamplifier that are used to increase the sensitivity of the spectrum analyzer. The simulated and measured noise figure of the T/R module in RX mode is shown in Fig. 60. The minimum measured NF is 4 dB and it varies with frequency and with different phase states. NF is between 4-6 dB in 9-12 GHz band, and below 10 dB at X-band.

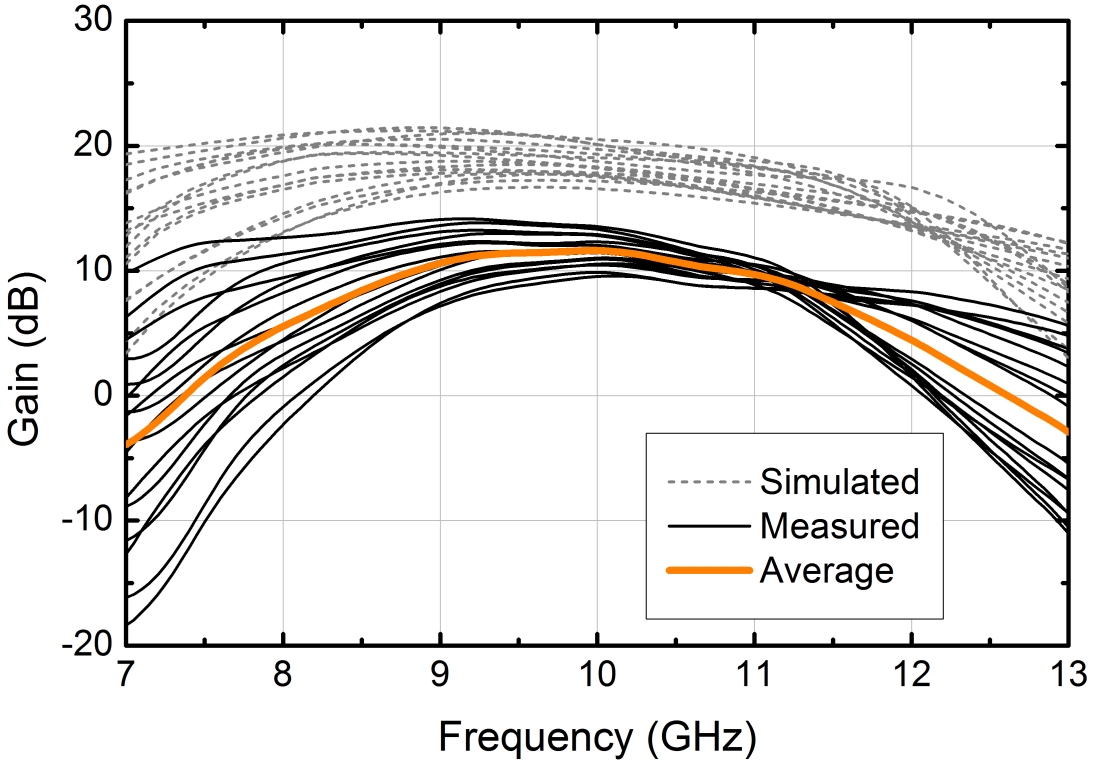

Figure 58: Simulated and measured gain of T/R module in receiver mode for all phase states

The discrepancy between the simulated and measured data is expected due to the phase shifter performance.

The phase shift performance of T/R module in RX mode is shown in Fig. 61, displaying the insertion phase for all 16 phase states. The figure demonstrates a linear phase shift around 9 GHz. Also, it is clear from the figure that the performance is degraded mainly because of 90° and 180° bits. The simulated and measured RMS phase errors can be seen in Fig. 62. A minimum RMS phase error of 5° is achieved at 9 GHz, while RMS pahse error is better than 11° in 7.5-10 GHz band. The measured center frequency is shifted towards lower frequencies. This means that phase shifter is performing slightly higher than the desired phase shift. One possible explanation is that due to the aggressively compact layout of the T/R module, the inductors in the adjacent bits has mutual coupling, therefore each bit performs slightly higher phase shift, since the phase shift and inductance values are proportional as given in (27). The mutual coupling is not observed in the standalone phase shifter measurements in Chapter 3 since each bit is far away from each other due to the inclusion of RF pads. Another explanation would be the loading effect of each phase shifter

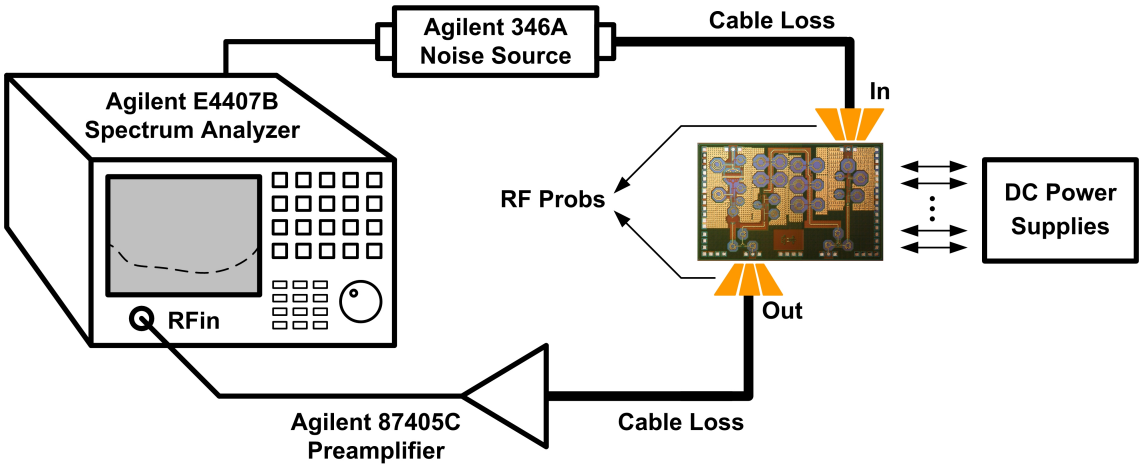

Figure 59: Noise figure measurement setup

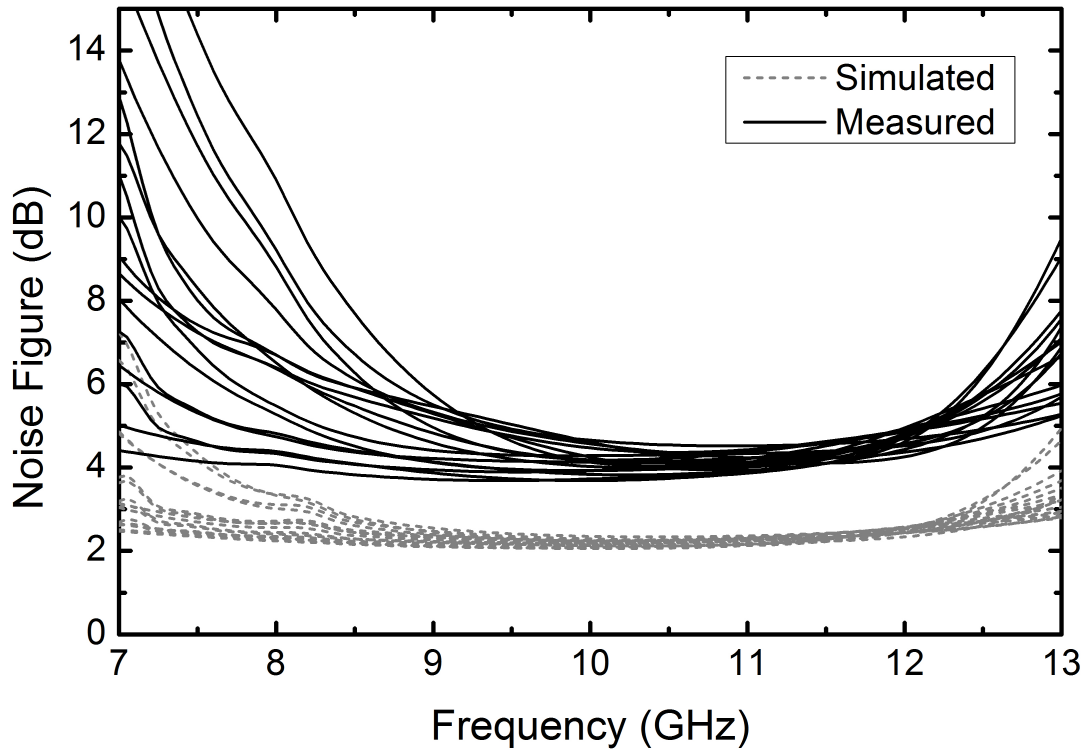

Figure 60: Simulated and measured noise figure of T/R module in receiver mode

bit on the adjacent bit. Each phase shifter bit is designed assuming a 50 Ω port termination. Due to the non-perfect 50Ω termination of the input and output of phase shifter to the SPDT switch and the VGA respectively may cause some phase shift performance degradation. But these effects should be minimal since the return loss for each phase shifter bit is better than 10 dB as presented in Chapter 3.

Finally, single-tone and two-tone tests are performed to measure the linearity of the T/R module as shown in Fig. 63. In receiver mode, the T/R module exhibits an

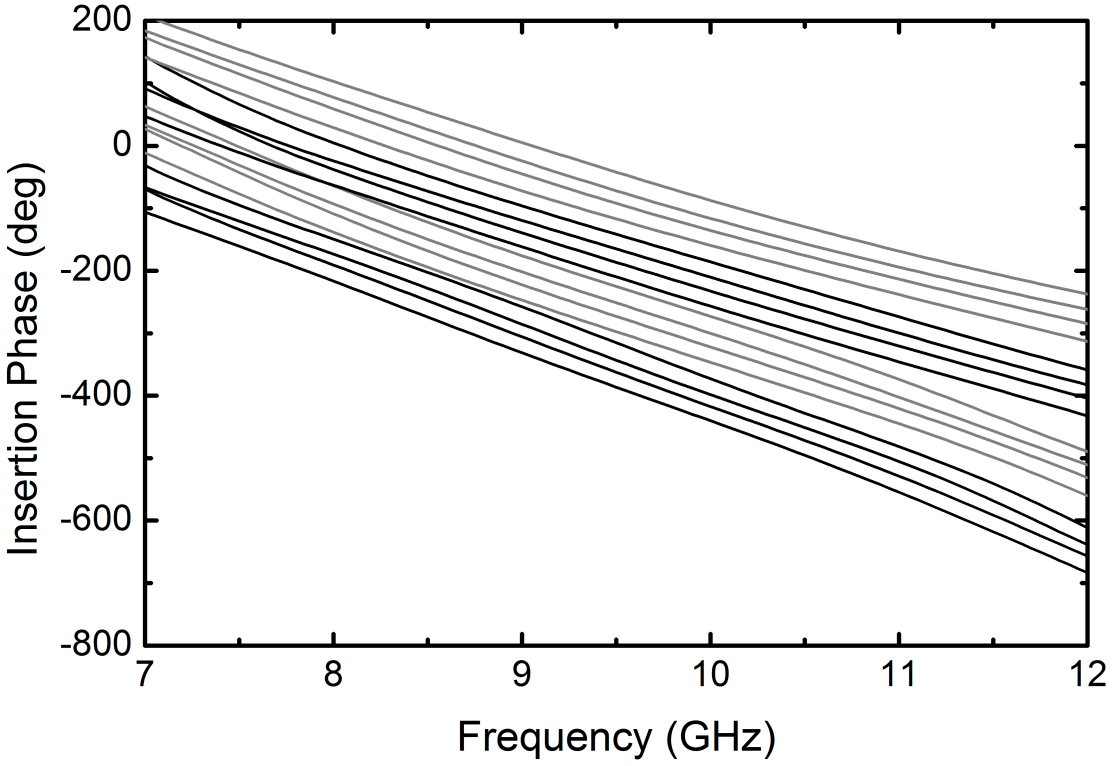

Figure 61: Measured insertion phase of T/R module in receiver mode for all phase states

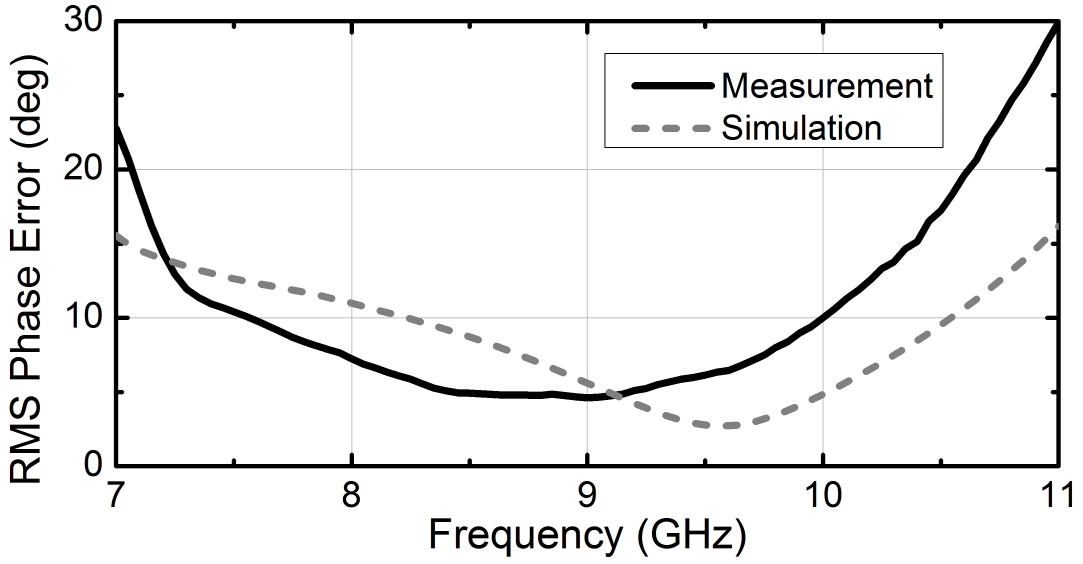

Figure 62: Simulated and measured RMS phase error T/R module in receiver mode

input-referred 1-dB compression point of -22 dBm for a single tone 10 GHz, while the input-referred third-order intercept point is -10.5 dBm for two input tones at 10 and 10.01 GHz. Considering the measured IIP_3 of the LNA is -8 dBm, this result

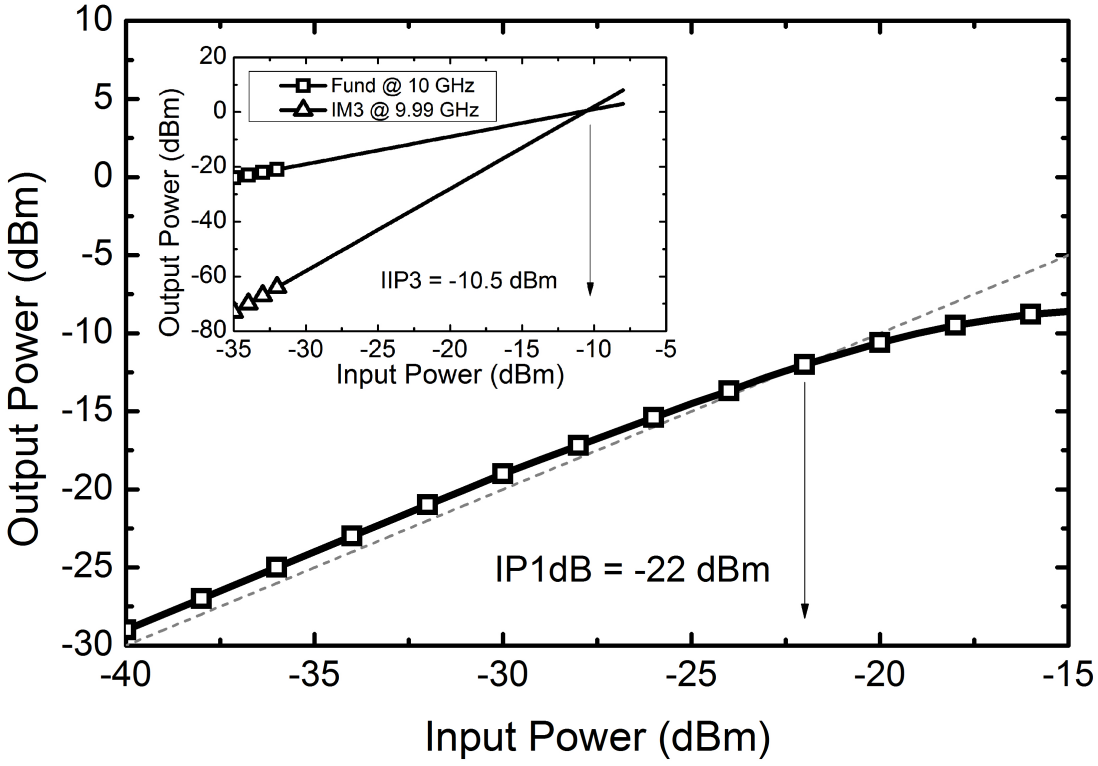

Figure 63: Measured 1-dB compression point and third order intercept point of T/R module in receiver mode

is acceptable.

4.5.2 Transmitter Mode

Same measurements are performed for the TX mode operation of the T/R module. Measured return losses of the T/R modules are shown in Fig. 64. The output matching performance of the PA is observed with a shift to lower frequencies, being better than 10 dB in 7.5-9.5 GHz. The output matching is narrow because it is matched using load-pull techniques to reach high output powers. The input return losses on the other hand considerably varies vs. different phase states. This is due to that there is only a passive SPDT in this case between the TX_{in} port and the phase shifter input, unlike the receiver mode of operation, where there is an active LNA in the front, preventing the return loss variation of the PS reflect to the RX_{in} port. Still the input return loss of the T/R module is better than 10 dB at X-band for most of the phase states and better than 8 dB for all phase states across X-band frequencies.

The simulated and measured gains of the T/R module for TX mode of operation

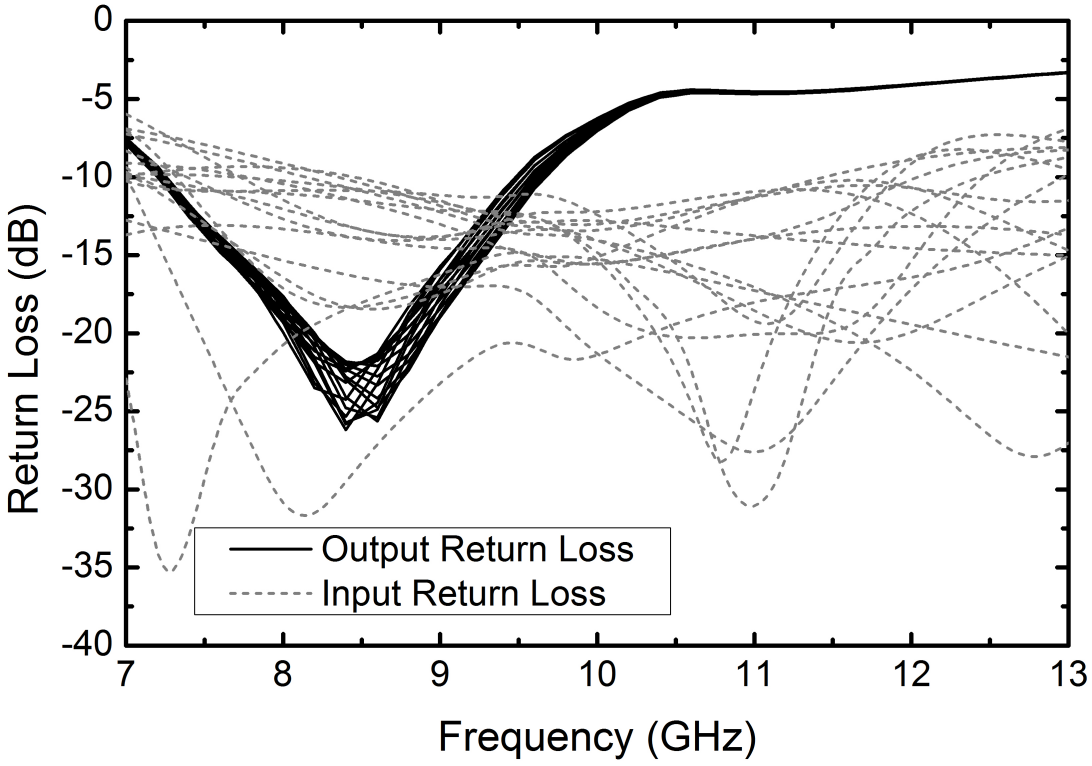

Figure 64: Measured input and output return losses of T/R module in transmitter mode for all phase states

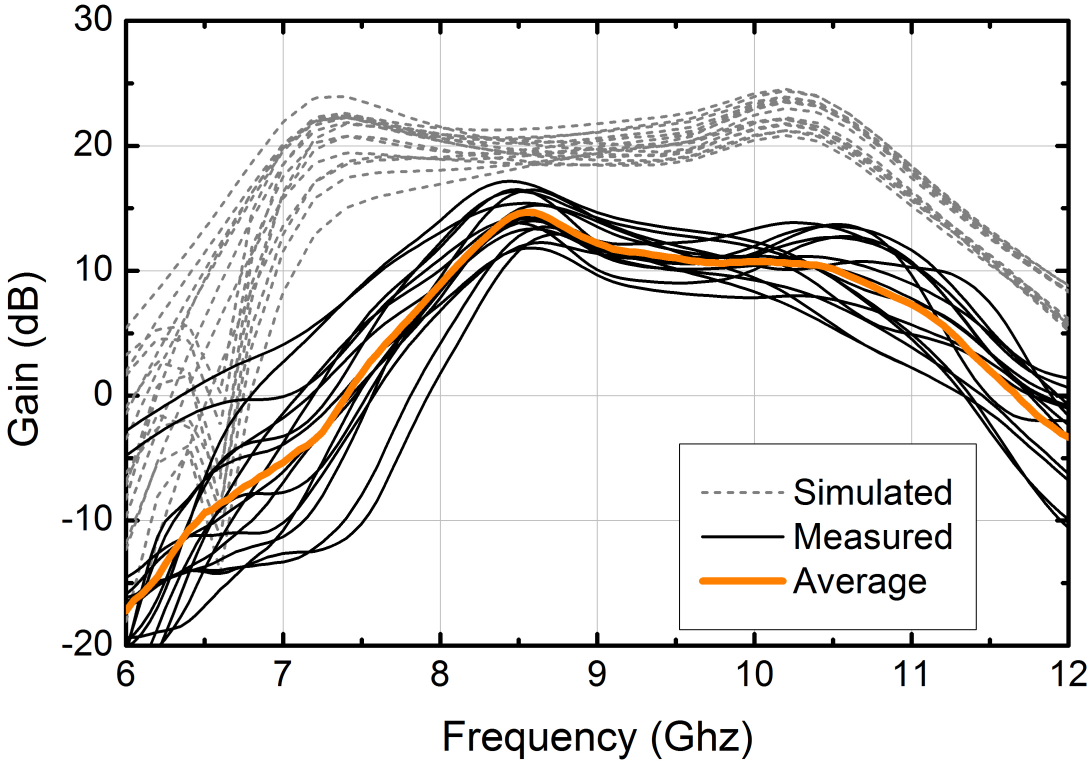

Figure 65: Simulated and measured gain T/R module in transmitter mode for all phase states

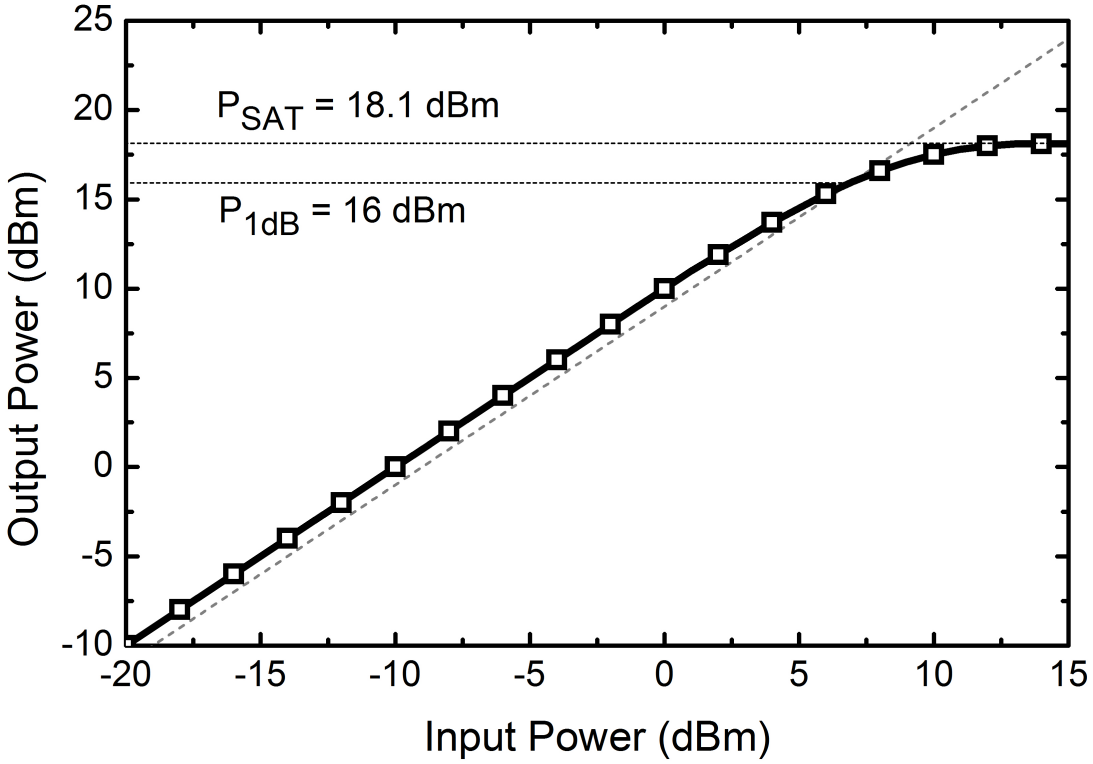

Figure 66: Measured 1-dB compression point and saturated output power of T/R module in transmitter mode

is shown in Fig. 58. There is a slight deviation in the frequency on top of the usual 8-9 dB deviation caused by the phase shifter losses. The average measured gain is drawn in bold; it is 10.7 dB at 10 GHz. A peak gain of 14.5 dB is achieve in 8.5 GHz and it is higher than 10 dB in 8.1-10.5 GHz band.

The phase shift performance and RMS phase error of the T/R module in TX mode (not shown here) is nearly the same as RX mode performance shown in Fig. 61 and 62.

The output power of the T/R module is shown in Fig. 66. The measured output-referred 1-dB compression point is 16 dBm for a single tone at 10 GHz. The saturated output power is measured as 18.1 dBm. These are lower than expected, which would normally be set by the PA performance of 21 dBm output 1-dB compressed power. This may be due to an unexpected saturation of the VGA.

The gain of the T/R module for both RX and TX mode of operation shown in Fig. 58 and Fig. 65 does not incorporate the variable gain functionality of the VGA and it is operated in the highest gain mode which is around 10 dB. Fig. 67 shows the RMS gain error of S_{21} in both TX and RX mode of operation. They are quite

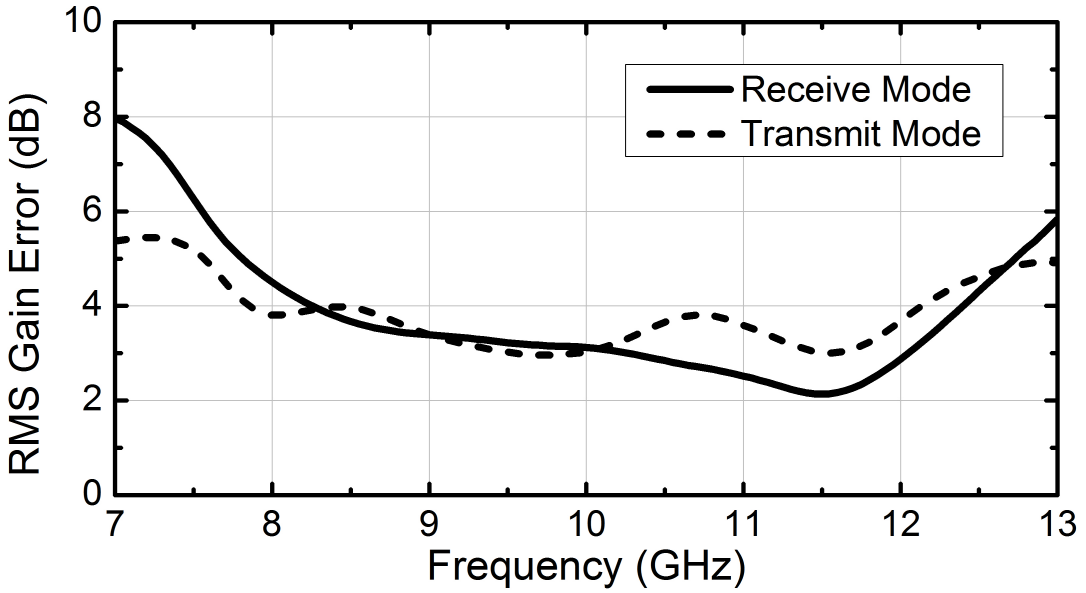

Figure 67: Measured RMS gain error of T/R module in receiver and transmitter modes

similar to each other, which means that the dominant source of gain error is only the phase shifter. Normally if an RX/TX gain of 20 dB were achieves, the VGA could be used to control the gain of the T/R module as well, without degrading the overall noise figure. However, due to the unexpectedly high insertion loss of the PS, using VGA for amplitude control would be meaningless, since it would degrade the NF too much. However, VGA can be used to compensate for the PS loss variations, forcing the RMS gain error to be as low as 0 dB at a desired center frequency of operation.

Finally, the power consumption of the T/R module is 35 mW in receive mode, assuming LNA is operating in its linear region; and the power consumption in transmitter mode is 250 mW assuming PA is operating around its 1-dB compression point.

4.5.3 Discussion and Comparison

In short, designed SiGe X-band T/R module has a measured RMS phase error of 5°-10° in 7.5-10 GHz band wiith a 4-bit phase control for both TX and RX mdoes. The module achieves a measured RX/TX gain of 11.5/10.7 dB at 10 GHz with a minimum NF of 4 dB and an IIP_3 of -10.5 dBm in RX mode; while achieving an output-referred P_{1dB} of 16 dBm in TX mode. These results are obtained in 4.9 mm^2

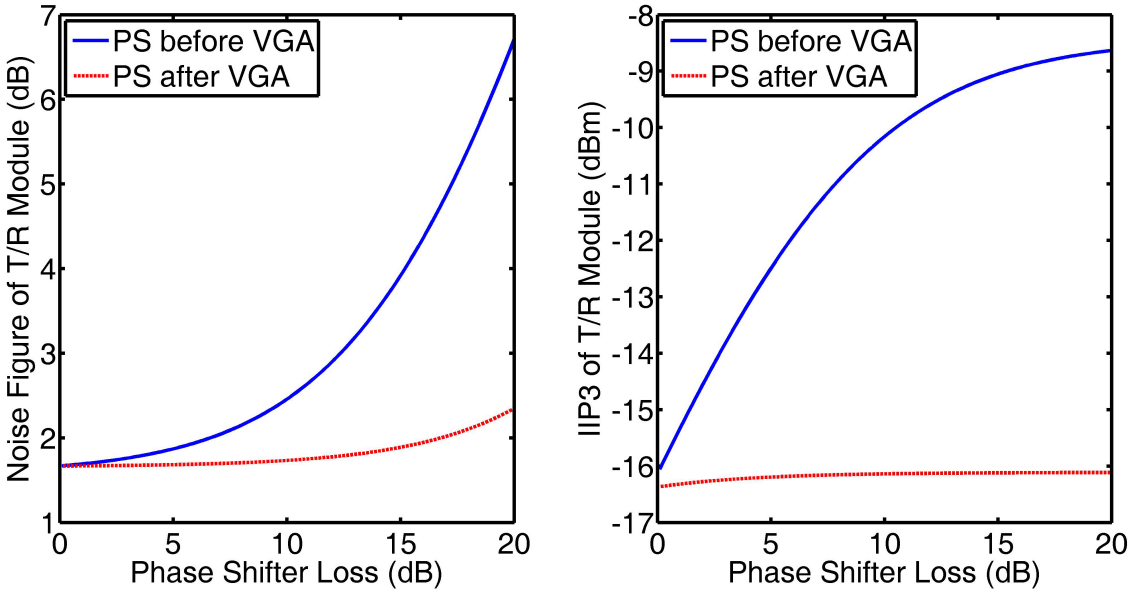

Figure 68: Simulated noise figure and third order intercept point of T/R module vs. phase shifter loss, using measured results of other building blocks.

chip area and 285 mW total power consumption of RX and TX modes.

The minimum noise figure of the module is increased from 2 dB in simulation to 4 dB in measurements due to the extra losses caused by the phase shifter. This degradation could be overcome if the PS is used in front of the VGA, which however would degrade the linearity performance in RX mode. This is showed in Fig. 68, where the measured performance data of the other building blocks is used to evaluate the effect of phase shifter loss using (29) and (30).

$$\frac{1}{IIP3_{Total}} = \frac{1}{IIP3_1} + \frac{G_1}{IIP3_1 IIP3_2} + \frac{G_1 G_2}{IIP3_1 IIP3_2 IIP3_3} + ... \qquad (30)$$

where $IIP3_n$ is the input-referred third-order intercept point of the n^{th} stage and G_n is the power gain of the n^{th} stage, both in linear scales. Currently achieved NF and IIP3 values are in good agreement with these simulation results. Increased noise figure of reduced gain problems could be overcome by introducing a second VGA in the middle of the phase shifter bits.

Finally, Table 7 provides a comparison between current SiGe X-band T/R modules. Since the designed SiGe X-band T/R module offers the best performance in 9-10 GHz band, these values are used in the table. It achieves comparable performance to other demonstrations at X-band in the smallest chip area except [**?**]

Table 7: Comparison of SiGe X-band T/R Module with reported works

Reference	Frequency (GHz)	Num. of bit	RX Gain (dB)	TX Gain (dB)	RMS Ph. Err. (deg)	RX NF (dB)	RX IIP_3 (dBm)	TX OP_{1dB} (dBm)	Power Cons. (mW)	Chip Area (mm^2)	Technology
This work	9 – 10	4	10 – 11.5	10.7 – 12	5 – 10	4 – 6	-10.5	16	285	4.9	0.25-μm SiGe
[35]	8 – 10.7	5	11 – 12	11 – 12	5 – 8	3.5 – 4.5	-13	N/A	33	13.3	0.13-μm SiGe
[36]	8 – 11	5	20	30	6	7 – 8	N/A	18	1500	8.4	0.25-μm SiGe
[37]	8 – 11	5	10 – 18	10 – 18	6	11 – 15	N/A	12	800	16	0.25-μm SiGe
[38]	8.5 – 10	6	12	11	2	8.5	8	11.5	650	12.8	0.18-μm CMOS
[39]	8.5 – 10.5	6	3.5	3.5	4.3	8	0.3	0.3	150	1.2	0.13-μm CMOS

5 Conclusion & Future Work

5.1 Summary of Work

Next generation phased array radars requires thousands of transmit/receive modules to be able to scan the beam electronically. These modules require low cost, high performance and high integrated IC solutions. With the recent advances in silicon based technologies, SiGe BiCMOS has a great potential to be used in the next generation phased arrays, especially for commercial applications. For military applications, SiGe BiCMOS can provide hybrid solutions with III-V technologies for optimum balance between performance, cost and operation expenses.

In this thesis a 4-bit passive X-band (8-12 GHz) phase shifter and a fully-integrated transmit/receive (T/R) module is presented, realized in IHP Microelectronics 0.25-μm SiGe BiCMOS technology. Initially phase shifter fundamentals are covered. A comparative analysis of different phase shifter topologies such as switched line, loaded line, reflective type, switched filter and vector modulator phase shifters are investigated. By-pass/lo-pass topology is chosen due to its smaller required chip area and reduced number of series switches. Also, the effect of phase shifter number of bit on the array performance is discussed and an analysis of the low-pass Π network that is used in the phase shifter is provided.

SiGe 4-bit X-band phase shifter is implemented using switched filter topology. Low-pass Π networks are used as phase shifting elements (phase shift state). Isolated NMOs transistors are used for switching purposes (bypass state). Phase shifter is composed of 22°, 45° and 90° bits, while the 180° bit is realized by cascading two 90° bits. Each bit is fabricated and measured as a standalone component. The return losses of each bit is better than 10 dB, the overall phase shifter has an average of 14 dB insertion loss. Minimum RMS phase error of 3° is obtained at 10.1 GHz. RMS phase error is better than 11° at 9.2-10.8 GHz band. The overall phase shifter occupies 0.9 mm^2 area, has no DC power consumption and achieves input-referred 1-dB compression point of 15 dBm.

The design and measurement of previously developed building blocks such as SPDT switch, LNA and PA is presented. Using these blocks and the presented 4-bit phase shifter, a SiGe X-band T/R module with a small chip area (4.9 mm^2)

is developed. The building blocks of the T/R module is interconnected by on-chip microstrip transmission lines. In 9-10 GHz band T/R module achieves a gain of 10-11.5 dB in receiver mode and 10.7-12 dB gain in transmitter mode. RMS phase error is between 5° and 10°. Noise figure in receiver mode is between 4-6 dB, IIP_3 is receive mode is -10.5 dB and 1-dB compressed transmit power is 16 dBm. Total power consumption is 285 mW.

5.2 Future Work

One of the main problems that is faced throughout the thesis is the excessive insertion loss of the phase shifter, which is mainly attributed to the lossy MOS switches in the technology. As a short-term future work, there are two ways for solving this problem. Frist, additional amplifier stages can be inserted between the bits of the phase shifter, which will increase the power consumption by only tens of mW and the chip area less than 15%. Another and much fancier solution would be to implement the phase shifter using vector modulation scheme. Actually, foreseeing the excessive insertion loss of the phase shifter in this work, a vector modulator phase shifter has been designed by one the senior students under my supervision. An RC filter is used to generate two orthogonal vectors which are then fed into four VGAs, two using the CB and two using the CE topology. This generates 4 vectors of 0°, 90°, 180° and 270° which are scaled and added by varying the gains of the VGAs to generate any phase between 0-360°. It has a simulated RMS phase error of 0.6° at 10 GHz and lower than 5.6° RMS phase error at X-band.

As a long-term future work, integrating low-power, low-cost and low-chip area SiGe phase and amplitude control chips with very high power and extremely low noise GaN amplifiers as a hybrid solution for phase arrays seems as a promising candidate for military applications with extreme specifications.

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