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An Ultra-Wideband SiGe BiCMOS LNA for W-band Applications

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Abstract **–**This paper presents the design steps and implementation of a W-band ultra-wideband LNA for both automotive and imaging applications. Three amplifiers based on common-emitter topology with different configurations are manufactured using IHP 0.13µm SiGe BiCMOS 300/500 GHz (f_t/f_{max}) SG13G2 technology. A three-stage, single-ended structure is proposed for ultra-wideband imaging purposes. As the results are analyzed, this 0.2mm^2 LNA can operate in a 25GHz of measured 3dB-bandwidth in W-band with 21dB peak gain and 4.9dB average noise figure using 1.5V supply voltage. It consumes 50mW of power in the edge operation conditions and the output 1dB compression point is found as -4dBm. To the authors' knowledge, this chip achieves one of the best overall performances compared to other W-band LNAs.

Keywords**:** Automotive radar, Imaging applications, SiGe BiCMOS 0.13µm, W-band Low Noise Amplifier

1. Introduction

The advancements in SiGe technology has paved the way to high level of integration with high speed, low-cost and high temperature resolution for mm-wave ICs [1, 2]. However, this technology still suffers from increased noise and higher power consumption compared with GaAs, InGaAs and InP [3-6] (see Table I). In recent years, there has been significant efforts on designing integrated on-chip W-band active phased array systems and TR (transmit / receive) modules for commercial, military, space and medical purposes requiring high speed data communication. One such area is the use of these radars in automotive applications [7-9]; such as blind side detection and cruise control mechanisms, collision avoidance/mitigation systems and automated driving units. In addition to automotive applications, other safety / security related field exist in imaging applications [10, 11]; such as concealed weapon-detection, security screening and video enhancement of low-visibility scenes. Considering the wide range and importance of application fields, high quality and low cost transceiver units are required. Therefore LNAs are one of the quality determining components in this case due to their gain, ability of operation in multiple frequencies and noise figure performances in these units.

In this work, measurement results of the fabricated LNA structures to be used in W-band automotive and imaging applications are presented. The chips are built using a low-cost SiGe BiCMOS process providing a high-level of integration. The steps until designing a wideband amplifier are clearly explained by comparing fabricated chips. Finally a three-stage single-ended ultra-wideband W-band HBT-based LNA is proposed and measurement results are discussed.

2. Design Procedure

There are various topologies with related trade-offs that can be used in LNA design; such as common base/gate, common emitter/source, shunt-series, cascode structures, and so on. Working in the mm-wave frequencies does not allow designs to have high gain and also causes an increase in the NF_{min} (minimum noise figure) because of operation close to f_t. The gain-noise figure trade-off is basically what determines the topology, as well as the design complexity and supply voltage. Taking these into account, common-emitter topology, which is the most used driving circuit, is utilized in presented designs. While providing comparable gain and very low noise, its low output impedance can overcome matching networks with low quality factor [1]. Another advantage is that supply voltages will be much lower since a single transistor is fed. In order to increase the gain further, cascode and cascade architectures are selected and discussion of the results of different configurations is shared. Although the cascaded structure has more insertion loss due to increased number of inductors at each stage, the configuration allows a simple design with relatively high gain and low noise if the first stage has enough gain to reduce the noise of latter stages. Cascode structure, on the other hand, allows increased isolation and removes Miller parasitic, however supply voltages and noise figure will be much higher. The simplified schematics of the designed amplifiers are shown in Fig. 1.

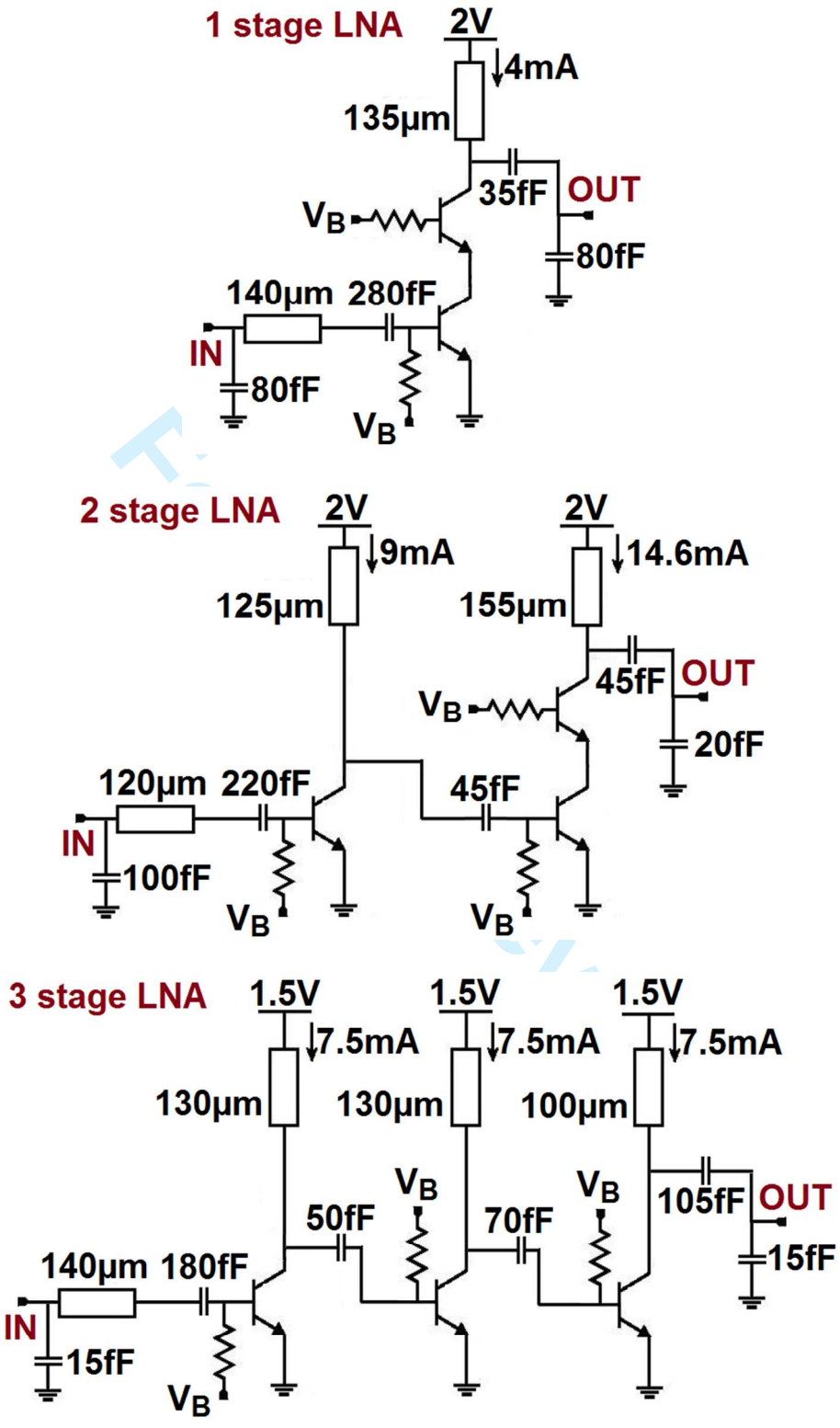

Fig.1. Schematic designs of 1 stage cascade structure (LNA1), 2 stage cascade structure (LNA2), 3 stage single ended structure (LNA3)

It is explicit that a single stage, single-ended amplifier (the core, single BJT) will have the lowest noise figure, but gain will not be enough for most applications. Therefore, cascode architecture (LNA1) should be manipulated to increase the overall gain while compromising on overall noise performance. For wideband applications, the number of stages should be increased therefore increasing the complexity and noise figure of design. In this configuration (LNA2), a single-ended stage is followed by a second cascode. However, it is expected to have much higher noise figure since the gain of first stage is not high enough to lower the noise contribution of the second cascode stage. As a result, a three stage single-ended structure (LNA3) will resolve the noise figure issue, providing relatively high gain and having a wideband performance. Noise contribution of the latter stages are negligible compared to LNA2, which yields a careful optimization on the first stage according to the lowest possible noise figure and, on the latter stages, optimization to highest gain. Moreover, owing to having no cascode parts, supply owing to having no cascode parts, supply voltages will be much lower. Adding another stage provides a wider bandwidth with a higher gain, but contradicts with the amplifier stability. In order to make the circuit unconditionally stable for the band of interest again, gain should be reduced. However, instead of using a 4 stage amplifier, a less-complex 3 stage design achieves almost the same specifications. Note that using an ultra-wideband LNA will decrease the noise equivalent temperature difference, NETD, given by

$$NETD = \frac{T_{sys}}{\sqrt{B\tau}} \quad (1)$$

where T_{sys} is the noise temperature of the system, B is the bandwidth and τ is the integration time [1]. As the bandwidth is increased by using a wide band LNA, more sensitive temperatures can be measured in imaging applications. Moreover, in order to enable all automotive radar functions, systems should have the ability of clear separation amongst the objects which requires higher

resolution and the low noise using SiGe technology will reduce NETD further. Therefore LNA design with increased bandwidth and low noise figure is necessary for both applications that attracts IC researchers.

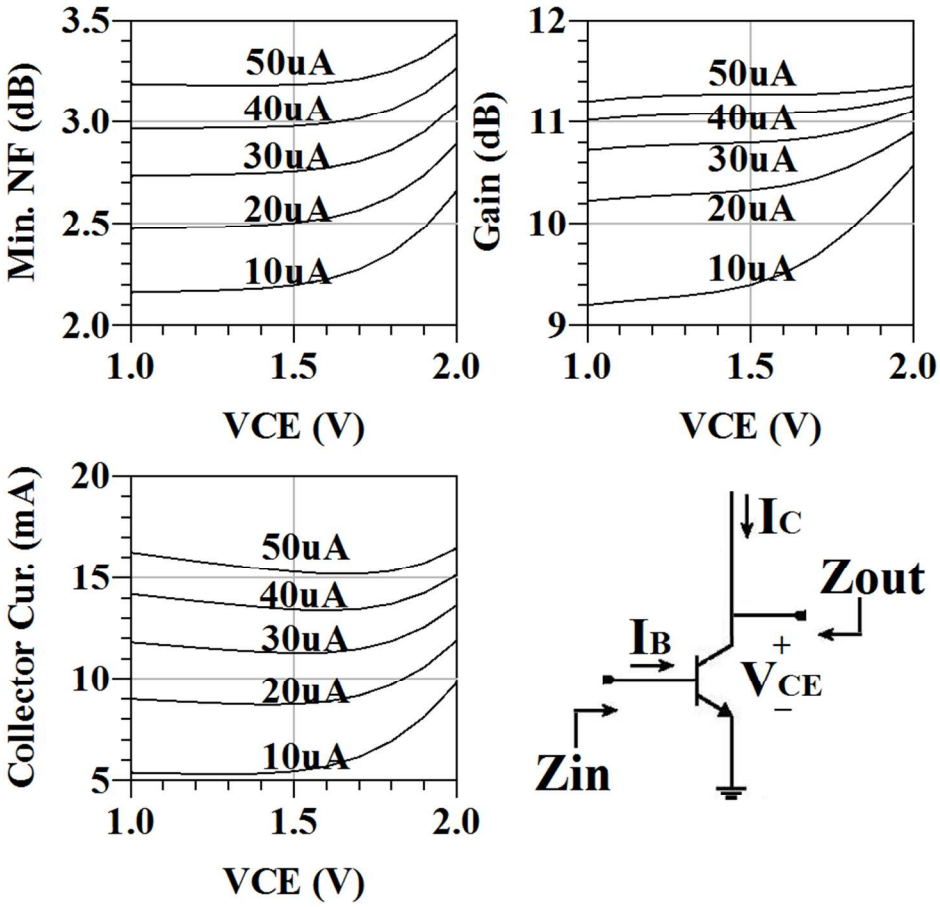

Fig. 2. BJT performance graphics to find the optimum bias point of transistor. Noise Figure, Gain & Collector Current with respect to changing Collector-Emitter Voltage (V_{CE}: 1V-2V) and Base Current (I_B: 10µA-50µA) at 77 GHz of operation frequency

To find the optimum bias point of a common-emitter stage, Fig. 2 is drawn. In this figure, the changes in noise figure and associated power gain (input matched to optimum noise figure and then output conjugately matched for minimum reflection) are highlighted with changing collector-emitter voltage (V_{CE}) for some different base currents (I_B). By using this data for LNA3,

where the same design procedure applies to LNA1 and LNA2, an optimum point of 17μA of I_B at 1.5 V of V_{CE} is found which corresponds to 2.4dB of NF, 10dB of gain and 7.5mA of collector current approximately. This optimum point is also utilized for latter stages since the gain and noise figure performances are satisfying.

After finding the optimum bias points and placing the bias circuits, input and output matching networks are designed accordingly to extract the expected noise figure and gain. L-type and Π-type matching networks, including the pad capacitances, are used in input, output and inter-stage matching as shown in Fig. 1. For the inductors, simple microstrip transmission lines are designed whose lengths are altering between 100μm and 155μm with fixed 3μm width for all LNA designs. As a result, the microstrip lines correspond to inductor values ranging from 55pH to 95pH with quality factor of 20 and parasitic resistances of 1.4Ω to 2.3Ω. The transmission lines are drawn in the upper most metal layer in a 7-layer technology [12] to lower the insertion loss and to be able to derive the maximum current without damaging the lines (3μm-thick TopMetal2). Additionally, ground shields are used below the inductors to enhance the quality factor performance by removing the substrate parasitic. Also, MIM (metal-insulator-metal) capacitors are placed for RF ground, DC blocks and in matching circuits. These foundry provided capacitors have high quality factors and are placed between TopMetal1 and Metal5 with a dielectric thickness of 40nm and relative permittivity of 6.75. For the upper and lower plates, 150nm thick special MIM layers and Metal5 layer are used. GSG pad capacitances of about 15fF are also included in the schematic level designs.

Considering all these design procedures, full EM simulations are performed in Agilent ADS software and the designed LNAs were manufactured at IHP-Microelectronics by using SiGe

BiCMOS 0.13µm SG13G2 technology. The fabricated LNA chips can be seen in Fig. 3. They occupy approximately 400µm X 500µm of area (0.18mm^2, 0.21mm^2 and 0.2mm^2 from LNA1 to LNA3).

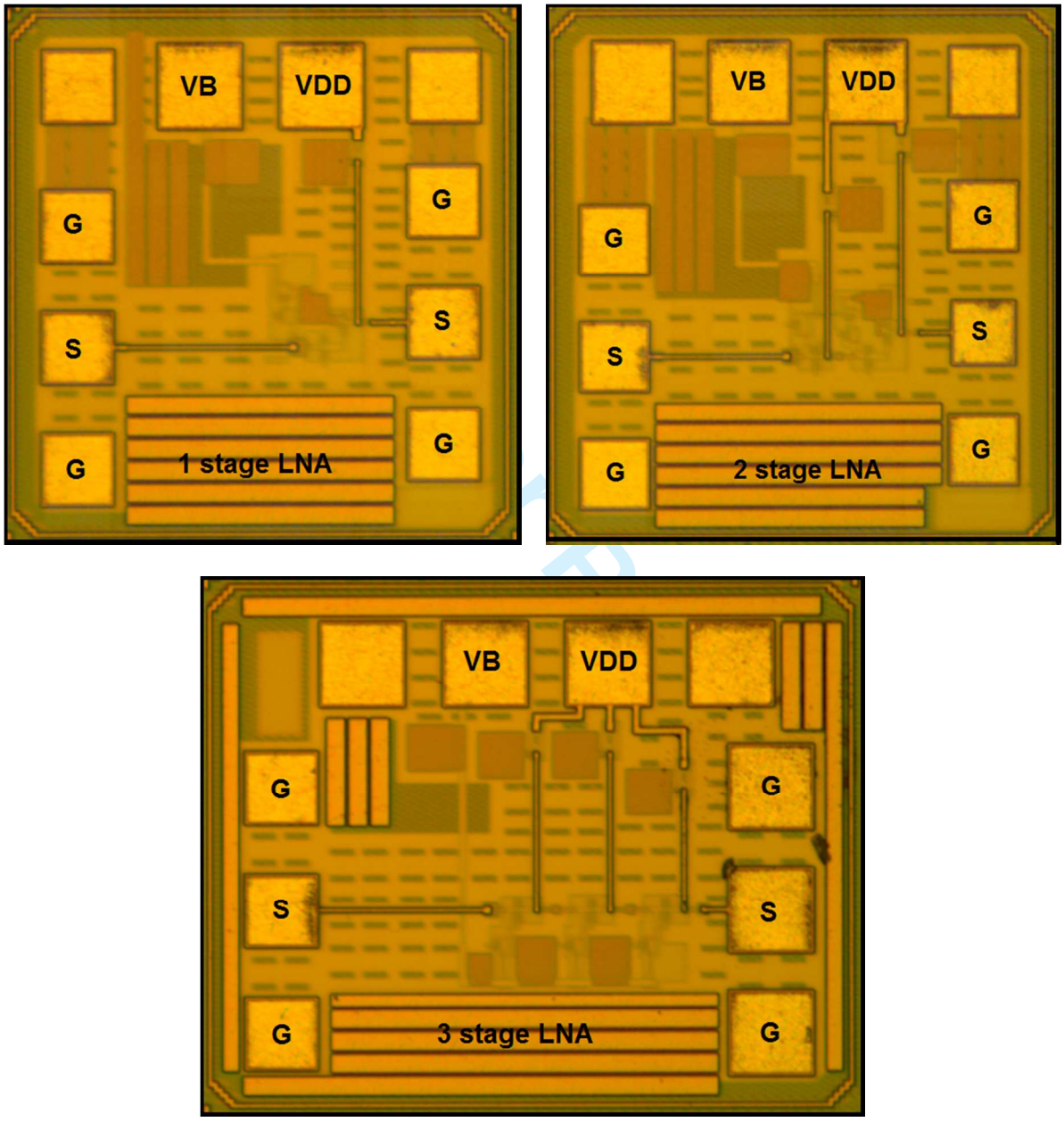

Fig. 3. Fabricated chip photos. *TopLeft*: 1 stage cascade structure (LNA1), *TopRight*: 2 stage cascade structure (LNA2), *Bottom*: 3 stage single-ended structure (LNA3)

3. Measurement Results

Measurements are conducted in the SUNUM labs (Sabanci University Nanotechnology Research and Application Center) using a PNA 5245A Network Analyzer.

The edge operation conditions are as follows. LNA1 which is composed of a single cascode stage derives 5.2mA of current in total and consumes 10.64mW of power. On the other hand, LNA2 which has a cascode structure only on the second stage, consumes 60mW by drawing 28.6mA. Finally, LNA3 is formed by cascading three single-ended parts and absorbs 50.55mW with 33mA. In Figs. 4-5-6, measured (straight lines) and simulated (dashed lines) S-parameter performances of the LNAs are highlighted. LNA1 has 17dB peak gain at 80GHz from a single stage (see Fig. 4).

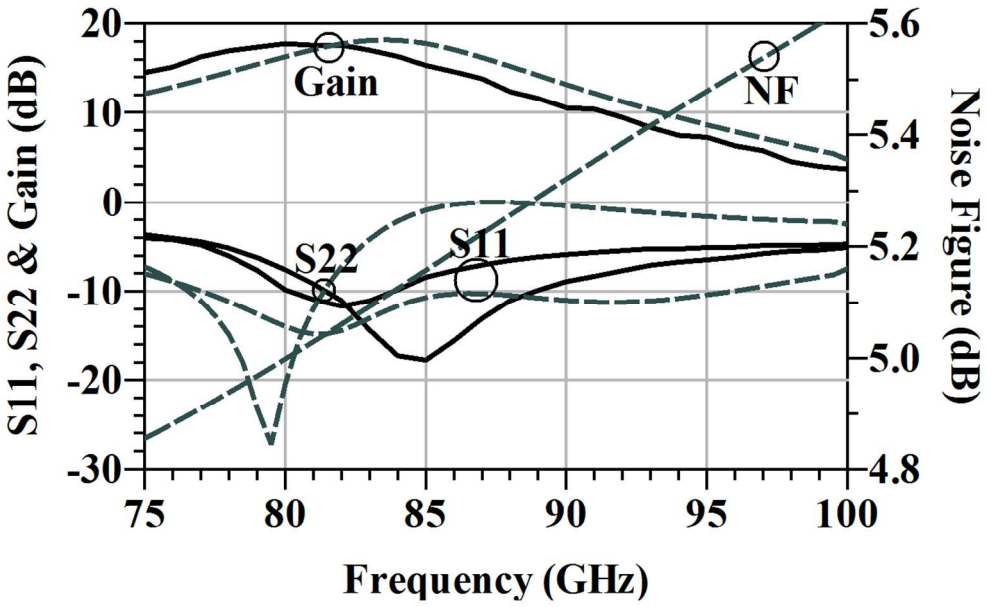

Fig. 4. Measured & Simulated (dashed) performance parameters of LNA1

In the 82-85GHz band, input and output return losses are both below 10dB with 16.5dB gain and 30dB isolation. The measured 3dB-bandwidth is 11GHz. From the simulations, average

noise figure in this band is found to be 5.1dB and gain performance is parallel to measurement results. However a 3GHz of frequency shift is observed at both input and output ports.

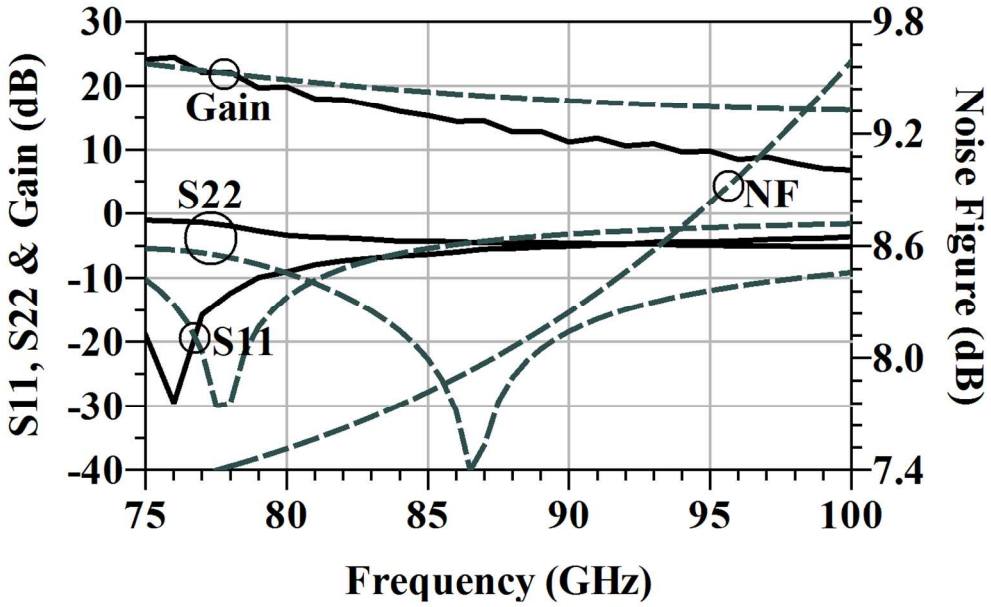

Fig. 5. Measured & Simulated (dashed) performance parameters of LNA2

On the other hand, at 76GHz, 25dB of gain can be extracted from LNA2 with well-matched input below 20dB and simulated noise figure of about 7.5dB (Fig. 5). The noise figure can be decreased with the lowered bias voltage as these figures represent the performances in the edge operating conditions.

As stated in the previous sections, the ultra-wide band performance is attained from LNA3 with a flat over 15dB gain throughout the entire W-band, with 21dB peak, as shown in Fig. 6. Input and output are well matched below 10dB in a minimum-25GHz bandwidth between 75-110GHz. The available setup allows measurements between 75-110GHz, however in the simulations, 3dB bandwidth is found as 35GHz, covering the entire V-band & W-band. Noise figure is also very low for such high frequencies, which is 4.9dB on average in simulations,

where isolation is more than 40dB. For the schematic design in which only lumped components are used for an overall look at the very first design steps, noise figure is tried to be matched in first stage without much compromise in gain, return loss and bandwidth. Considering the selected bias points and these constraints, minimum noise figure is found near 70 GHz. However in full layout simulations, this frequency shifted to 60 GHz being 4dB and, at 77 GHz, noise figure is simulated as 4.45dB. From the simulations it is seen that the measured results almost overlaps the simulation results in gain and return loss performances.

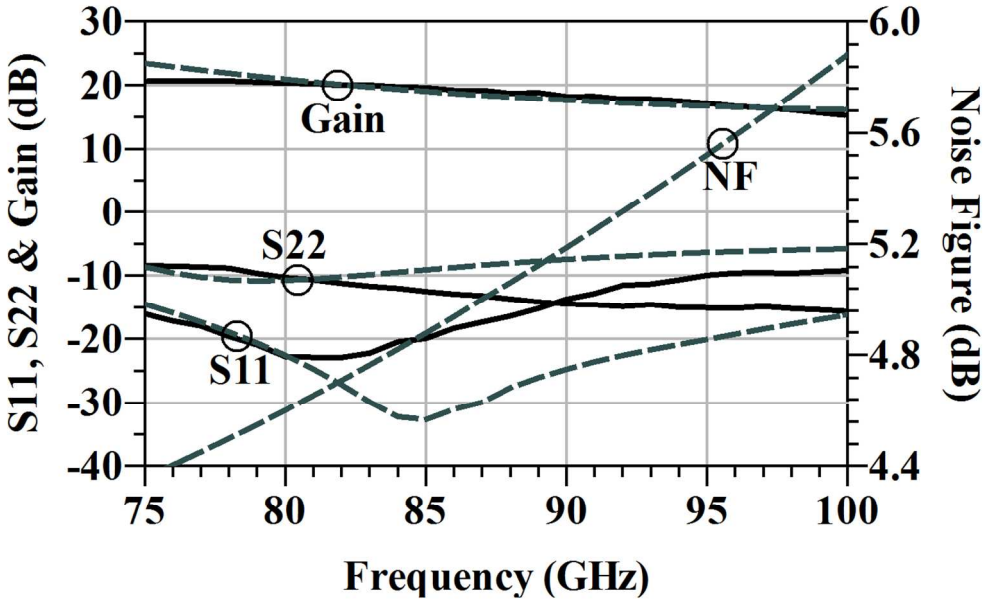

Fig. 6. Measured & Simulated (dashed) performance parameters of LNA3

In Fig. 7, input and output power handling performances extracted from the simulations of each are presented. From the results, it is seen that LNA1, LNA2 and LNA3 have output 1dB compression points of -6dBm, -10dBm and -4dBm. Furthermore LNA3 has a 5.5dBm of OIP3 (output third order intercept point) from two-tone intermodulation simulations.

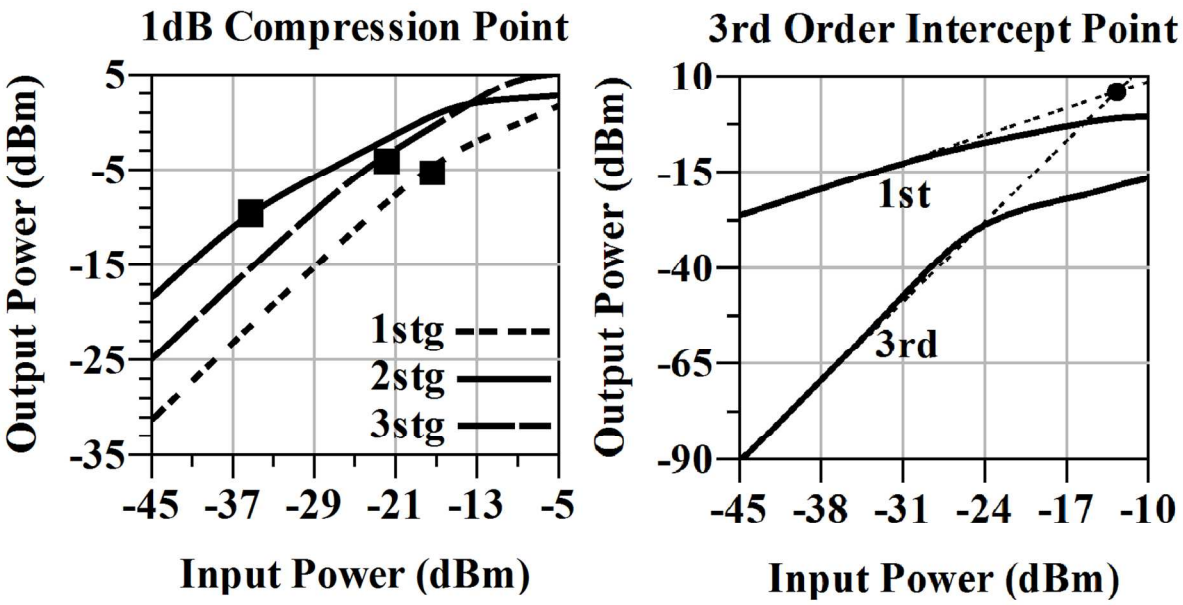

Fig. 7. Simulated Input/Output 1dB compression point of LNAs and IIP3 / OIP3 point of LNA3

In Table I, some of the state-of-the-art LNAs (mostly SiGe technology for a proper comparison including some other technologies) operating in W-band are shown. According to the results of proposed LNA3, highest bandwidth and gain with low noise figure are extracted while input and output return losses are better than 10dB for the whole frequency band which implies that LNA3 could be used as a complete amplifier, not requiring any off-chip matching networks.

TABLE I
COMPARISON OF STATE-OF-THE-ART W-BAND LOW NOISE AMPLIFIERS

Ref	Technology	Used Arch.	f_o (GHz)	Gain (dB)	NF (dB)	RL (dB) < 10dB	3dB BW (GHz)	Power (mW)	OP1dB (dBm)
[1]	0.13µm SiGe BiCMOS	4stage SE-CE	85-89	19	8	94-98 GHz	17 (80-97)	25	-3
[2]	0.13µm SiGe BiCMOS	2stage C-CE	110	20	4	100-115 GHz	20 (100-120)	17	-4 **
[3]	90nm SiGe BiCMOS	4stage SE-CE	90	19	5.1	S11 not well	30 (75-105)	43	-3
[4]	70nm GaAs mHEMT	4stage SE-CS	80-95	25	2.7 **	S11 not well	35 (70-105)	35	2 **
[5]	50nm InGaAs mHEMT	3stage SE-CS	57-110	16.4-23.2	2.1-2.8	75-90 GHz	NG	0.9	-1.4
[6]	0.1µm InP HEMT	3stage	94	19.4	2.5	S11 not well	35 (67-102)	18	NG
[10]	0.18µm SiGe BiCMOS	2stage C-CE	77	14.5	6.9	76-85 GHz	14.5 (69-83.5)	37	3.1
[11]	65nm CMOS	5stage SE-CS	90	27	6.8	S22 NG	10	36	NG
This Work	0.13µm SiGe BiCMOS	3stage SE-CE	77	21	4.5 **	75-100 GHz	> 25 (75-100)	50	-4 **

*C: cascode, SE: single-ended, CE: common-emitter, CS: common-source, NG: Not Given, **: simulated.*
For the return loss, a common frequency band is extracted where both input and output return losses are better than 10dB.

4. Conclusion

This paper presents the results of fabricated W-band LNA chips that were built using the SiGe BiCMOS 0.13µm SG13G2 technology of IHP Microelectronics. The chips are designed based on common-emitter topology with cascode, single-ended and multi-stage configurations. Among these chips, the three stage, single-ended HBT-based amplifier offers an ultra-wideband operation to be utilized in W-band automotive and imaging applications. To the best of the

authors' knowledge, this design achieves one of the best overall performances compared to other W-band LNAs (see Table I).

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References

[1] J. W. May and G. M. Rebeiz, "A W-Band SiGe 1.5V LNA for Imaging Applications," Radio Frequency Integrated Circuits Symposium, pp. 241-244, Apr. 2008.

[2] A. Ç. Ulusoy, M. Kaynak, V, Valenta, B. Tillack and H. Schumacher, "A 110GHz LNA with 20dB Gain and 4dB Noise Figure in an 0.13µm SiGe BiCMOS Technology," International Microwave Symposium (IMS) proceedings, Seattle, USA, 2013.

[3] Y. Yang, S. Cacina and G. M. Rebeiz, "A SiGe BiCMOS W-Band LNA with 5.1dB NF at 90 GHz," Compound Semiconductor Integrated Circuit Symposium, pp. 1-4, Oct. 2013.

[4] X. Ciccognani, F. Giannini, E. Limiti and P. E. Longhi, "Full W-band High-Gain LNA in mHEMT MMIC Technology," Microwave Integrated Circuit Conference (EuMIC). pp. 314-317, Oct. 2008.

[5] F. Thome, H. Massler, S. Wagner, A. Leuther, I. Kallfass, M. Schlechtweg and O. Ambacher, "Comparison of two W-band low-noise-amplifier MMICs with ultra low power consumption based on 50nm InGaAs mHEMT technology," International Microwave Symposium Digest (IMS)., pp. 1-4, Oct. 2013.

[6] X. Mei, C. Lin, L. Lee, Y. Kim, P. Liu, M. Lange, A. Cavus, R. To, M. Nishimoto and R. Lai, "A W-band InGaAs/InAlAs/InP HEMT low-noise-amplifier MMIC with 2.5dB noise figure

and 19.4dB gain at 94GHz," Indium Phosphide and Related Materials, 2008, IPRM 2008. 20th International Conference on, pp. 1-3, May. 2008.

[7] J. Hasch, E. Toprak, R. Schnabel, T. Zwick, R. Weigel and C. Waldschmidt, "Millimeter-Wave technology for automotive radar sensors in the 77 GHz frequency band," IEEE Transactions on Microwave Theory Techniques, vol. 60, no. 3, pp. 845-860, Mar. 2012.

[8] ECC decision of 19 March 2004 on the frequency band 77-81 GHz to be designated for the use of automotive short range radars (ECC/DEC 04) Eur. Radiocommun Office. Copenhagen, Denmark, 2004, Online, http://www.ero.dk

[9] J. Metz, and T. Baras, "High speed data communications based on W-band automotive radar MMIC," in Proc. IEEE Wireless Commun. Appl. Computat. Electromagnetics, pp. 438-442, Apr. 2005.

[10] A. Y. K. Chen, Y. Baeyens, Y. K. Chen, and J. Lin, "A Low-Power Linear SiGe BiCMOS Low-Noise Amplifier for Millimeter-Wave Active Imaging," IEEE Microwave and Wireless Component Letters, vol. 20, no. 2, pp. 103-105, Feb. 2010.

[11] A. Tomkins, P. Garcia, and S. P. Voinigescu, "A passive W-band Imaging Receiver in 65-nm Bulk CMOS," IEEE J. Solid-State Circuits., Vol. 45, No. 10, pp. 1981-1991, Oct. 2010.

[12] H. Rucker, B. Heinemann and A. Fox, "Half-terahertz SiGe BiCMOS technology," IEEE 12th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, Jan 2012, Santa Clara, CA, pp. 133-136.