Modeling and Optimization of BiCMOS Embedded Through-Silicon Vias for RF-Grounding

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***Abstract* —In this paper we demonstrate the modeling and optimization of BiCMOS embedded high aspect ratio through-silicon vias (TSV) for RF-grounding applications. The inductance and the resistance of the TSV are analyzed with respect to TSV design parameters and process effects such as sidewall-tilting and void formation. RF measurement results with extracted inductance and resistance of 24 pH and 86 mΩ for a single TSV are in very good agreement with the simulation results. Based on the simulated and measured results, RLC-lumped-element models are developed considering the aforementioned process characteristics to provide realistic models for Process-Design-Kit (PDK) implementation.**

I. Introduction

There is a growing interest on the integration of through-silicon vias (TSV) in CMOS and BiCMOS technologies [1]. Recently, the potential of TSV has been successfully demonstrated for different applications e. g. grounding of mm-wave power amplifiers and 3D chip stacking [2,3], as shown in Fig. 1.

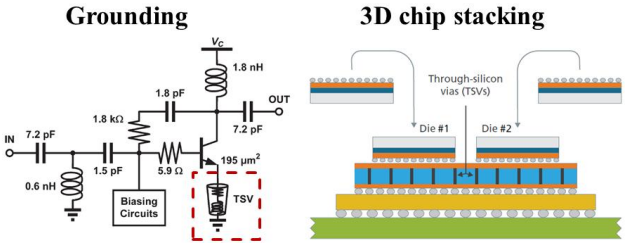

Fig. 1 Main application areas using TSV; power amplifier grounding [2] and 3D chip- stacking [3].

In many cases, the ground connections of silicon chips are realized by bond wires, which add additional inductances. For grounding applications, using TSV instead of wire bonding is a promising solution to prevent from these high inductances. Wire bonding requires large and costly interconnection area and introduces parasitics which might strongly degrade the circuit performance [4]. The typical way to decrease the inductance of bond wires is to parallel arrange many of them which increase the required pad area; thus the chip size. The main interconnection parasitics, namely the inductance and resistance can be significantly minimized using TSVs which helps to improve the electrical performance, reduce power consumption and shrink the chip size [5]. Since the inductance and resistance of TSVs are sensitive to fabrication process a deep understanding of the TSV fabrication flow is essential. Lastly, to be able to use TSVs in circuit design, lumped-element based models are necessary to implement into PDK of the technology.

In this work, we demonstrate the modeling and optimization of BiCMOS embedded TSVs for RF-grounding applications. High aspect ratio (1:25) TSVs are realized in IHP's SG25H1/H3 technologies. The TSV inductance and resistance are analyzed with respect to TSV design parameters and process effects such as sidewall-tilting and void formation. RF measurement results with extracted inductance and resistance of 24 pH and 86 mΩ for a single TSV provide a good agreement with the simulation results. Based on the simulated and measured results, a lumped-element based model is developed for PDK implementation.

II. Through-Silicon Via Fabrication

A. *Process Integration of TSVs*

BiCMOS embedded annular-type TSVs are integrated into IHP's high performance SG25H1/H3 BiCMOS technologies [6] using a via-middle approach. After finalizing the Front-End-of-Line, deep annular trenches with a depth of 75 µm are etched into silicon substrate using the Bosch process. A SiO_2 layer is deposited at the trench sidewalls to isolate the TSVs from the silicon substrate. To achieve an electrical connection from wafer front- to backside, trenches are filled with tungsten using CVD process. Then, TSVs are connected to the Back-End-of-Line (BEOL) via the first metallization layer and BEOL fabrication is finalized (Fig. 2).

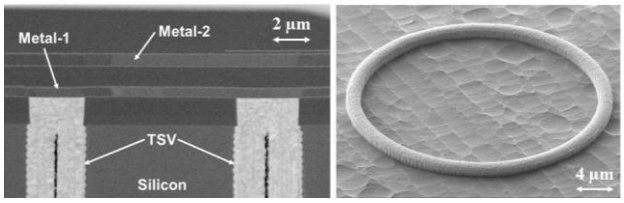

Fig. 2 BiCMOS embedded TSVs with first two metallization layers (left). TSV released from wafer-backside (right).

During TSV fabrication, two main fabrication steps have been intensively optimized, namely the sidewall tilting which leads to a narrowing of ring-width (Fig. 3) and void formation during W-filling due to the high aspect-ratio trenches.

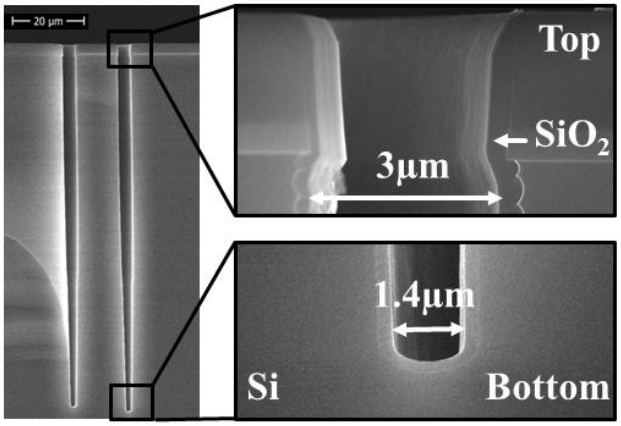

Fig. 3 SEM pictures of TSV showing the trench tilting with the final trench width at top and bottom.

After finalizing the BiCMOS fabrication including the TSV-module, a carrier-wafer is applied from the frontside. The wafer is then thinned down to 75 µm using a grinding process followed by a dry etch release. Finally, 1 µm of aluminum is deposited as backside metallization (BSM) layer which provides a chip to package interface (Fig. 4).

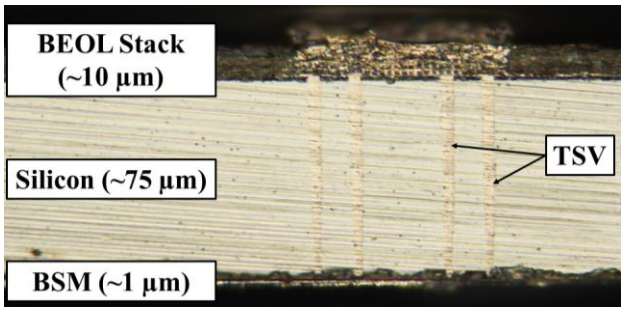

Fig. 4 Cross-section of BiCMOS chip with TSV.

B. *EM Modeling and Optimization of TSV*

For accurate TSV inductance and resistance extraction, ANSYS Q3D Extractor, which is a 3D electromagnetic field simulator and parasitic extraction tool, is used. The cross-section of a single TSV is shown in Fig. 5.

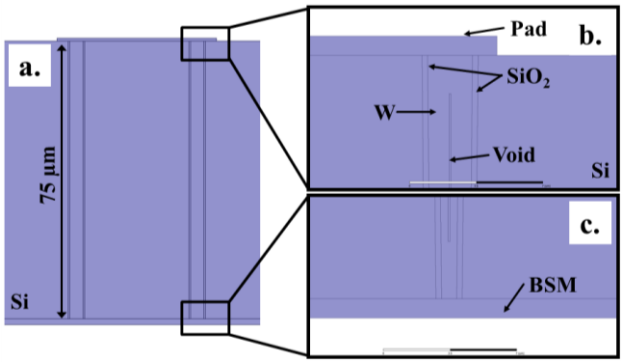

Fig. 5 Cross-section of full TSV (a.) and detailed view of TSV with probing pad (b.) and BSM (c.) in ANSYS Q3D.

From EM simulation of a TSV with a depth of 75 µm and a diameter of 25 µm, the extracted inductance and resistance with respect to both sidewall-tilting and void formation is shown in Fig. 6.

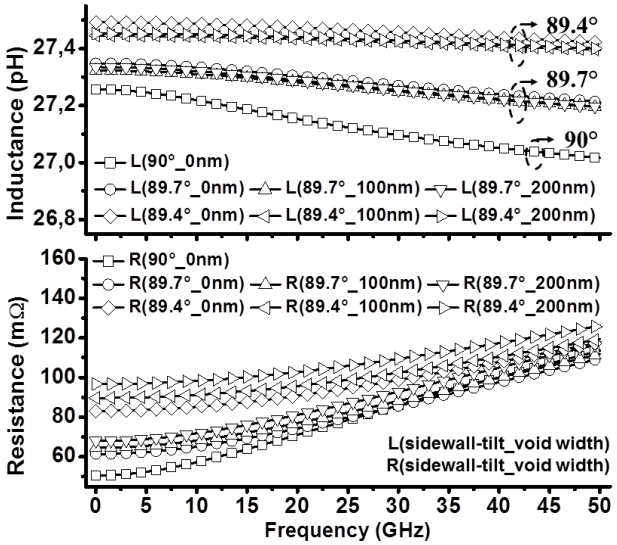

Fig. 6 Inductance and resistance vs. frequency with respect to different sidewall-tilts and void width.

The inductance is slightly affected by the sidewall-tilt with increased inductance for lower sidewall-tilting, however different void width do not show an influence on the inductance. In comparison the resistance is strongly affected by both sidewall-tilting and void formation. Smaller sidewall-tilts and higher void widths significantly increase the resistance of the TSV.

For fabricated TSVs, a tilt of 89.4°, a maximum void width of 100 nm and length of 65 µm is measured from SEM characterization and is used in the final optimization. As the final optimization parameter, the influence of TSV diameter is analyzed in Fig. 7. With larger TSV diameter, the inductance and resistance can be decreased but as a result the size per TSV increases. With a final diameter of 25 µm, an inductance of 27 pH and a resistance of 90 mΩ at 1 GHz are simulated.

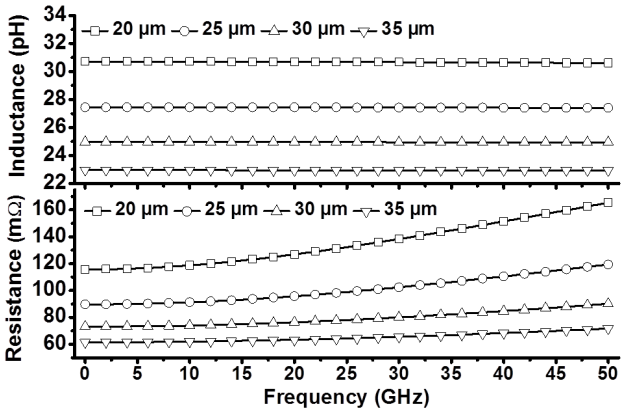

Fig. 7 Inductance and resistance vs. frequency with respect to different TSV diameter.

III. Experimental Results

For electrical characterization, one-port test structures with a TSV diameter of 25 µm have been fabricated. The S-parameter measurements are done up to 50 GHz and open/short de-embedding is performed to remove the effect of the measurement pads. Inductance and resistance values are extracted in Fig. 8.

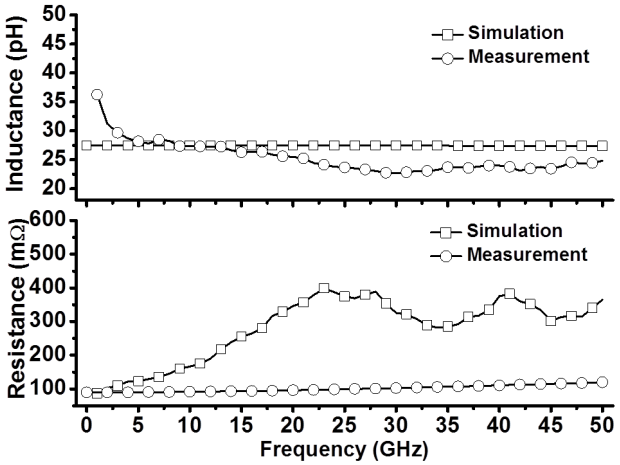

Fig. 8 TSV inductance and resistance vs. frequency with measured and simulated parameters

The measured inductance of 24-28 pH above 5 GHz and resistance of 86 mΩ shows a very good agreement with simulated values with 27 pH and 90 mΩ at 1 GHz. The measured resistance at higher frequency is slightly different from the simulated one. This can be correlated with contact resistance between the TSV and BSM.

IV. Process Design Kit - Implementation

Lumped-element based model of TSVs are realized for implementation into the PDK. The used model of a grounding TSV is shown in Fig. 9. The Cox, Csub and Rsub parameters are extracted from the simulation results and given in Fig. 10.

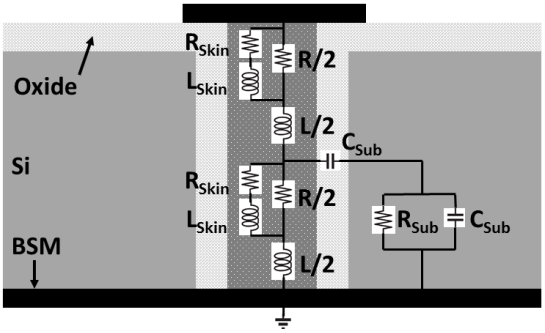

Fig. 9 Lumped-element based model of grounding TSV with additional components for frequency dependency.

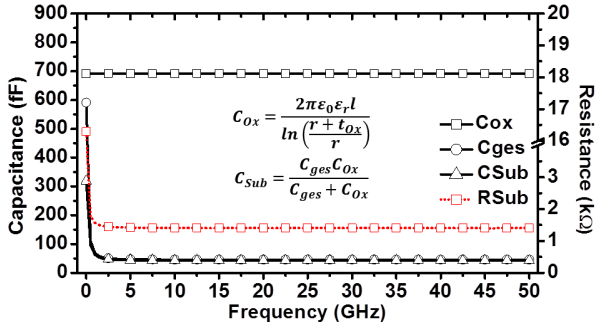

Fig. 10 Simulation of SiO_2 capacitance, substrate capacitance and substrate resistance. The SiO_2 capacitance of ~690fF is similar to analytical equation for cylindrical capacitors.

Due to the ideal dielectric behavior, the capacitance C_{ox} is constant whereas substrate capacitance and resistance decrease with increased frequency due to the Si-SiO_2 dielectric and the higher dielectric loss coming from low-resistive silicon substrate (50 Ω-cm).

The real and imaginary part of Z11 from measurement and RLC-model are shown in Fig. 11. Due to the aforementioned difference of resistance, the real-part extracted from measurement shows a difference at higher frequencies whereas the imaginary part is in very good agreement to the RLC-model.

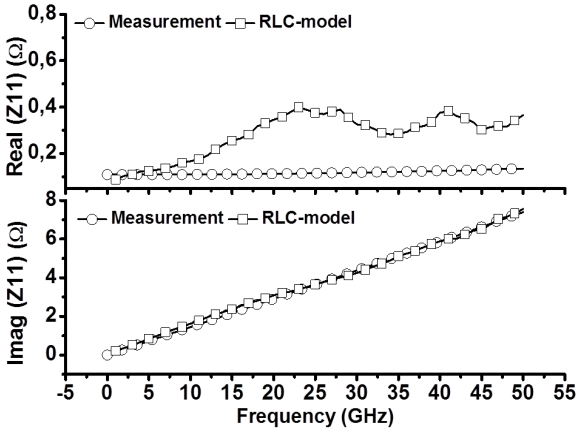

Fig. 11 Comparison of simulated and measured real and imaginary part of Z11.

IV. Conclusion

In this work, we demonstrate the modeling and optimization of BiCMOS embedded TSVs for RF-grounding applications. High aspect ratio TSVs are realized in IHP's SG25H1/H3 process flow. The TSV inductance and resistance are analyzed with respect to TSV design parameters and process effects such as sidewall-tilting and void formation. RF measurement results with extracted inductance and resistance of 27 pH and 86 mΩ for a single TSV provide a good agreement with the simulation results. Based on the simulated and measured results, lumped-element based models are developed for PDK implementation.

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