A77 GHz On-Chip Dipole Antenna with Etched Silicon Substrate

Mehdi Seyyed-Esfahlan[1], Mehmet Kaynak[2], and Ibrahim Tekin[1]

[1]Sabanci University, Electronics Engineering, 34956 IST, TURKEY
[2]Technology/Process Integration IHP GmbH, 15236 Frankfurt, Germany

***Abstract* — In this paper, a 77 GHz microstrip dipole antenna is integrated on a layered 11.4 μm SiO_2 and a silicon substrate with thickness of 670 μm. The unbalanced microstrip line is balanced by using a lumped LC circuit balun to feed both of the dipole arms. To decrease the substrate loss and hence increase the antenna gain, Localized Backside Etch (LBE) module offered by IHP is utilized to etch the area under the dipole antenna. For mechanical robustness, two walls of silicon substrate are left at the end of the dipole arms inside the etched area. The simulation results show a 3.2 dBi gain and 15 GHz bandwidth at 77 GHz.**

I. Introduction

As the frequency reaches mm-wave region, silicon substrate becomes more lossy and circuits suffer from the substrate loss. However, using silicon technology at high frequencies brings some benefits such as, well matching, miniaturization, and integration on a single chip.

The mm-wave radars are being used on vehicles at 24, 60 and 77 GHz frequencies, especially for safe drive, collision avoidance and to reduce accidents. To monitor the area ahead of the vehicle for different scan angles with different beamwidth and steering capability, one needs small, directive and efficient antenna that can be used as an element inside an array [1]. As the frequency is increased, the size of the antenna is decreased and this makes chip area small enough for integrating antenna arrays on a single chip.

There is extensive research for improving and optimizing on-chip antennas at 77 GHz band for various types of antennas such as slot, microstrip patch, and Yagi-Uda and dipole antenna. Research, however, is not only confined to antenna design, but also includes the balun circuit to feed the balanced antenna from the unbalance feed. Single ended circuit in [2], and balun structure in small area in [3] to feed the antennas at 77 GHz are shown. The effect of dimension and the geometrical shape of the antenna on antenna gain are studied at 66 GHz [4], over different types of antennas such as dipole, 2-elements Yagi, rhombic and loop antennas. In [5], both dipole and loop antennas are integrated in the 8 × 8 mm^2 package of Infineon's embedded wafer level ball grid array (eWLB) with WR12 rectangular waveguide and GSG feeding and achieved gains of 7.5 dBi and 7.7 dBi at 76.5 GHz with 8 GHz bandwidth for dipole and loop antennas, respectively. A wide band balun with high return loss (–6.5 dB return loss between input and each of the output ports/Yagi arms) on 74-82 GHz band, in which phase alternates up to 5º over 180º between two input ports of the Yagi antenna arms, is presented in [6], which radiate up to 0.5 dBi at 77 GHz. To reduce the size of the dipole antenna, a meander-line is used to match the planar inverted-F antenna with bandwidth of 7 GHz at 60 GHz, where a size 0.815 × 0.707 mm^2 with maximum gain equal to –13.82 dB is achieved [7]. The explorations and publications on various types of on-chip antennas on upper 60 GHz band, however, show very low or negative gain without incorporating them with another method such as using reflectors [5]. Small size of the manufactured device and the substrate loss are basic challenges and derives the interest in the methods of feeding, measuring, design and fabrication of these types of antennas [8]. In this paper, we design and optimize all parameters of dipole antenna and its feeding LC balun circuit, while by etching silicon under the dipole antenna and placing the ground plane below the etched silicon substrate, decrease the loss of silicon and increase the directivity of the antenna.

When antenna and feeding balun structures are integrated on the same chip are in the vicinity of each other on the same chip, the radiation properties of the antenna are highly affected by the metallic structures of the balun circuit. Hence, this requires the co-design of both the wire/strip antenna and the balun structure. For full integration of mm-wave circuits with the properly designed antenna, the overall chip size is still a challenge and has to be small. In this paper, strip flat dipole on-chip antennas are designed with an integrated lumped balun structure to obtain a small-sized chip.

The structure of the paper is organized as follows: In section II, detailed analysis about the balun structure and dipoles will be presented. In section III, simulation and measurement results will be presented for the antennas, and finally the paper will be concluded in section IV.

II. Balun and Antenna Design

Both balun circuit and dipole antenna design which are integrated on etched silicon substrate with ε_r = 11.9 and thickness of 670 μm. A top view sketch of the on-chip dipole antenna integrated with the LC balun circuit is shown in Fig. 1; which is optimized for 77 GHz operation. Both antenna, and the feeding balun circuit are embedded in a thin layer of SiO_2 with ε_r = 4.1 and

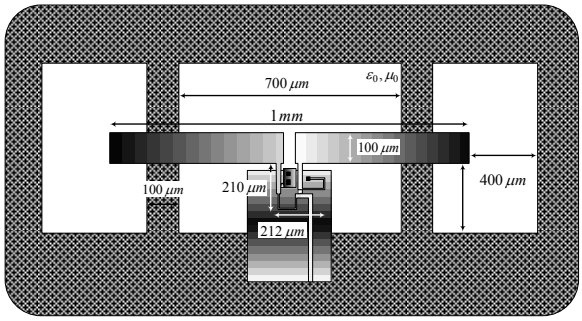

Fig. 1. Top view of the designed dipole antenna with its feeding balun circuit at 77 GHz.

thickness of 11.4 μm. Although below the antenna is etched (Fig. 1, white areas), two bars of silicon (Fig. 1, dotted area) are left inside the etched area to increase mechanical robustness of the antenna. The electrical conductivity of the substrate silicon is 2 Siemens per meter. The side view of the antenna and the balun circuit is shown in Fig. 2. Balun circuit and antenna are embedded inside the silicon dioxide, and Metal 5 layer is used for the signal and the antenna and Metal 1 layer is used as the ground plane for the balun.

A. Balun Circuit

There are filters which can be used as the balun to convert unbalanced signal coming from the source circuit to a balanced signal which feed two arms of the dipole antenna with 180º phase difference. In order to confine the balun circuit to the possible small area on the chip, LC balun circuit is selected in which the capacitors are metal-insulator-metal (MIM) type capacitors and inductors are formed by thin microstrip lines. The balun structure which occupies an area of 210 μm × 212 μm is shown in the Fig. 1. All parameters of LC balun are optimized and S-parameters for input port and two output ports are performed at 77 GHz. Simulations are performed by the 3-D finite element method EM simulator, HFSS version 12. The simulation results for inductor and capacitor at 77 GHz demonstrate the values of 140 *p*H and 37 *f* F, respectively. The width/impedance of unbalanced input line and two balanced output lines which feed the antenna, are optimized to 50 Ω to match the input port to the source at the desired frequency. To reduce the effect of measurement probe on the antenna radiation and for further mechanical stability, the length of the unbalanced input microstrip line is increased up to 500 μm long.

B. Antenna Design

After designing the balun circuit two output balanced ports are connected to antenna arms and antenna parameters are optimized in terms of the S-parameter of antenna input port, antenna radiation pattern and gain. Connection between LC balun circuit and dipole antenna is shown in Fig. 1.

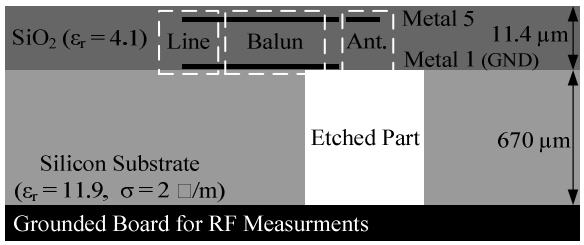

Fig. 2. Side view of the designed chip.

All dimensions of the dipole antenna such as antenna width, length, and dimension of etched part, thickness of the silicon bars and their location are optimized at 77 GHz. The goal of the optimization is to achieve minimum S11 and maximum gain in the desired direction. The results of simulations show optimum for antenna length equal to 1mm, width 100 μm, thickness of the silicon bars 100 μm, spacing between the bars 700 μm, and distance of antenna edge from the silicon substrate is 400 μm. The thickness of the silicon substrate is optimized to 700 μm to achieve the desired gain.

III. Simulation Results

In this section, detailed simulation results will be given for the both balun circuit and the dipole antenna obtained from HFSS.

A. Balun Circuit Simulation Results

A balun circuit with optimum dimension 210 μm × 212 μm is obtained which divides the input signal with 180º phase difference between two output ports at the 77 GHz. A 37 *f* F MIM capacitor and the microstrip line length of 200 μm which has an inductor of 140 *p*H are used. Return loss of input port and insertion loss between input and each of the output ports are shown in Fig. 3. This figure demonstrates well matching and 3 dB power divider which shows 180º phase difference at 77 GHz. Phase of S21, S31 and their difference are also presented in Fig. 4.

B. Antenna Simulation Results

By connecting balun circuit to the dipole antenna, dimensions of the dipole antenna, thickness of silicon bars and their spacing are optimized at 77 GHz. The optimum values are shown in Fig. 1. To analyze the antenna performance in terms of varying design parameters, simulations have been performed by changing values of antenna length and, thickness of silicon bars

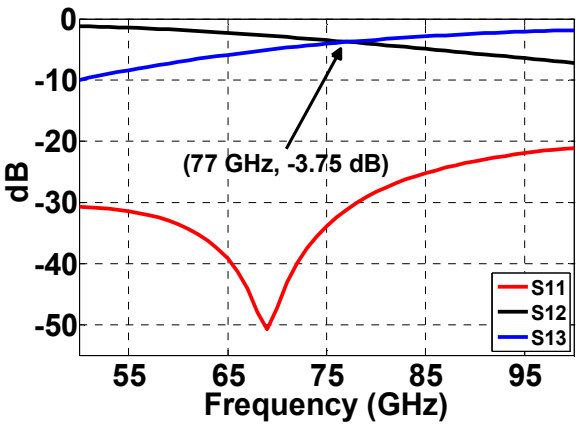

Fig. 3. Return loss of input port and insertion loss between the input and each of the output ports.

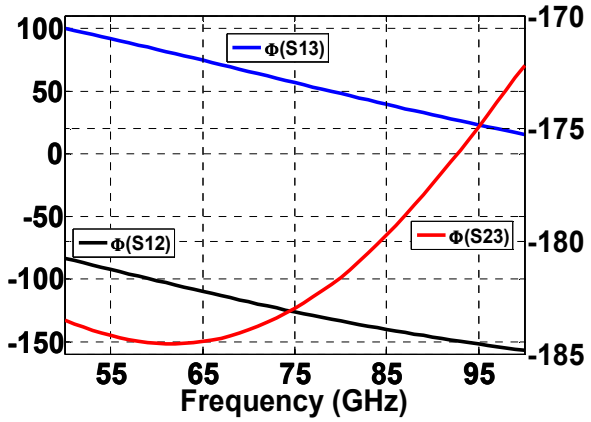

Fig. 4. Phase of the different S-parameters.

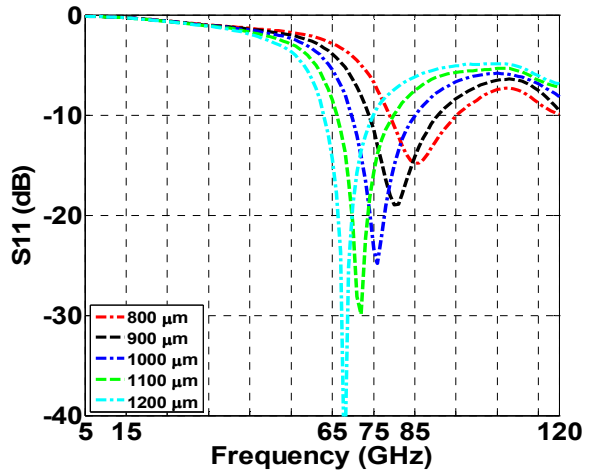

Fig. 5. Return loss from the unbalanced input port for different length of dipole antenna.

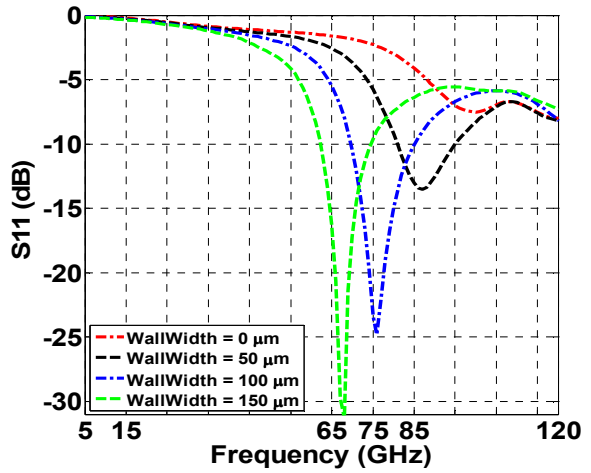

Fig. 6. Return loss from the unbalanced input port for different thickness of silicon bars.

over the specified value for which the antenna operates with gain.

Fig. 5 and 6 show antenna performance for different values of antenna length and silicon bars thickness, respectively. As expected, the frequency of the antenna is shifted to lower frequencies by increasing length of the antenna in Fig. 5 and is working at 77 GHz for 1mm length Fig. 6. shows better matching for thicker values of

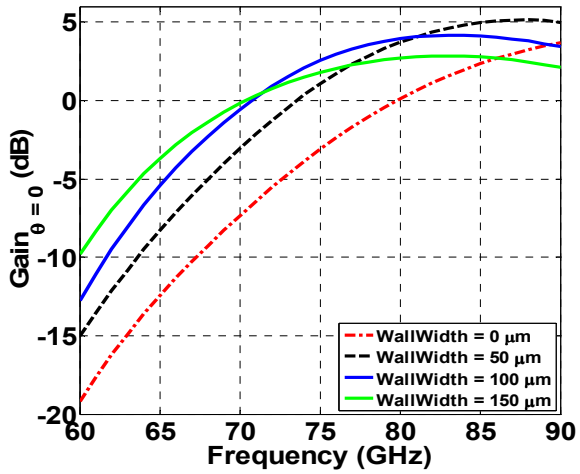

Fig. 7. Maximum gain of antenna versus frequency for different silicon bars thickness.

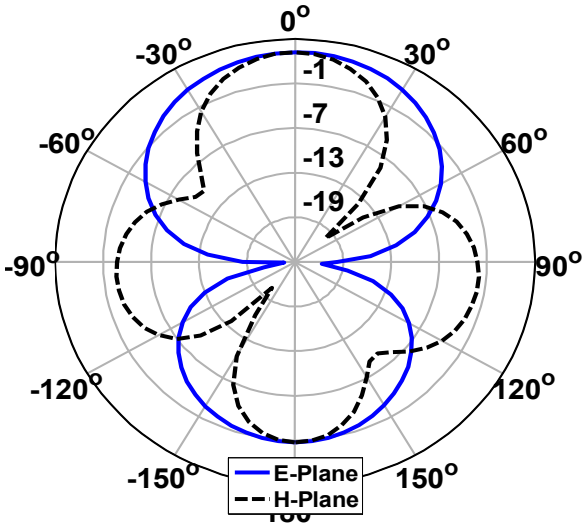

Fig. 8. Radiation pattern for both E and H planes of the designed dipole antenna.

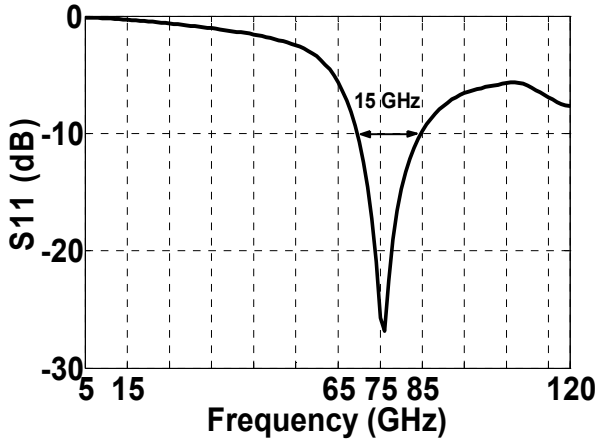

Fig. 9. Simulation result for return loss of the dipole antenna with optimum parameters value.

silicon bars, while the antenna frequency is shifted to lower frequencies. This sketch presents 100 μm for silicon Wall thickness at the desired frequency. Zero wall width stands for no wall inside the etched part (dimension of etched part without Si bars 1.8 × 0.9 mm^2).

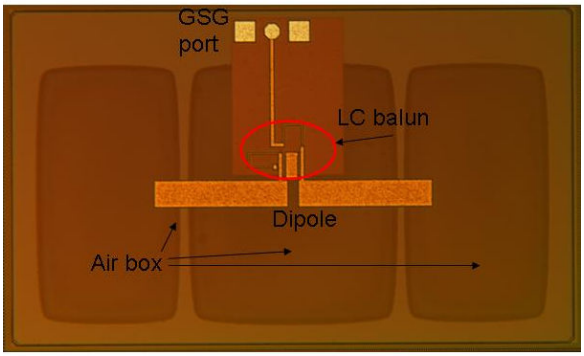

Fig. 10. 77 GHz designed dipole antenna layout.

Maximum antenna gain versus frequency for different silicon bars is also depicted in Fig. 7. This result shows 100 μm for silicon wall has the best gain at the desired frequency. This figure also demonstrates the effect of wall thickness in increasing the antenna gain for different frequencies.

Radiation pattern for the total realized antenna gain in the Fig. 8 shows its symmetry in the E-plane and reaches its maximum value of 3.2 dBi directly above the antenna at $\theta = 0$, which is reasonable compared to aforementioned references.

In Fig. 9, simulation results for return loss which is seen from the unbalanced input feeding port of the balun has 15 GHz 10 dB bandwidth and is below 20 dB at the desired frequency.

Prototype of the antenna which is manufactured by IHP LBE technology is shown in Fig. 10. Etched area and balun circuit is also shown in this figure.

IV. Conclusion

An LC balun circuit, which converts unbalanced input signal to two balanced signals to feed the dipole antenna arms, is designed at 77 GHz. To increase directivity and decrease loss of silicon substrate, Si substrate under the antenna is etched, while a ground plane is used under the silicon substrate. The antenna is tuned at the desired frequency by adjusting antenna length, thickness of the silicon bars and their spacing, etched window size and LC values of the balun. The results of simulations for the embedded LC balun and dipole antenna in SiO_2 on silicon substrate show that the input is properly matched to the antenna. Realized antenna gain of 3.2 dBi is obtained with maximum gain at 77 GHz.

Acknowledgement

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