DESIGN AND REALIZATION OF FULLY INTEGRATED MULTIBAND AND MULTISTANDARD Bi-CMOS SIGMA DELTA FREQUENCY SYNTHESIZER

by

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Abstract

Wireless communication has grown, exponentially, with wide range of applications offered for the customers. Among these, WLAN (2.4-2.5GHz, 3.6-3.7GHzand 4.915-5.825GHz GHz), Bluetooth (2.4 GHz), and WiMAX (2.500-2.696 GHz, 3.4-3.8 GHz and 5.725-5.850 GHz) communication standard/technologies have found largest use local area, indoor – outdoor communication and entertainment system applications. One of the recent trends in this area of technology is to utilize compatible standards on a single chip solutions, while meeting the requirements of each, to provide customers systems with smaller size, lower power consumption and cheaper in cost.

In this thesis, RF – Analog, and – Digital Integrated Circuit design methodologies and techniques are applied to realize a multiband / standart (WLAN and WiMAX) operation capable Voltage- Controlled-Oscillator (VCO) and Frequency Synthesizer. Two of the major building blocks of wireless communication systems are designed using 0.35 µm, AMS-Bipolar (HBT)-CMOS process technology. A new inductor switching concept is implemented for providing the multiband operation capability. Performance parameters such as operating frequencies, phase noise, power consumption, and tuning range are modeled and simulated using analytical approaches, ADS® and Cadence® design and simulation environments. Measurement and/or Figure-of-Merit (FOM) values of our

circuits have revealed results that are comparable with already published data, using the similar technology, in the literature, indicating the strength of the design methodologies implemented in this study.

TAMAMEN TÜMLEŞİK ÇOK BANTLI VE ÇOK STANDARTLI Bİ-CMOS SİGMA DELTA FREKANS SENTEZLEYİCİSİ TASARIMI VE GERÇEKLEMESİ

Emre ÖZEREN

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Anahtar Kelimeler: Faz Kilitlemeli Çevrim, Sigma Delta Modülasyonu, Kesirli N Frekans Sentezleyici, Gerilim Kontrollü Osilatör, WLAN, WiMAX, SiGe, BiCMOS, 0.35µ

Özet

Kablosuz haberleşme sistemleri tüketicilere sunulan geniş bantlı uygulamalarıyla beraber eksponansiyel olarak büyümüştür. Bu dâhili ve harici haberleşme standartlarından, WLAN (2,4-2,5GHz, 3,6-3,7GHz ve 4,915-5,825GHz), Bluetooth (2,4 GHz), ve WiMAX (2,500-2,696 GHz, 3,4-3,8 GHz ve 5,725-5,850 GHz) en geniş kullanım alanlarına sahiptirler. Teknolojinin bu alanındaki son eğilimlerden birisi de kullanıcıya daha düşük alan ve güç tüketimli ve düşük maliyetli sistemler sunarken, birbiriyle uyumlu birden fazla standardı, her birisi için gerekli şartların sağlanması koşuluyla, tek bir yongaya sığdıran çözümler bulmaktır.

Bu tezde çok bantlı/standartlı Gerilim kontrollü osilatör ve Frekans Sentezleyici, RF, Analog ve Sayısal tümleşik devre tasarım metotları ve teknikleri kullanılarak tasarlanmıştır. Kablosuz haberleşme sistemlerinin bu temel iki bloğunun tasarımında da 0,35 µm AMS-Bipolar (HBT)-CMOS teknolojileri kullanılmıştır. Bunun yanında çok standartlı tasarımın sağlanmasında yeni bir endüktans anahtarlama sistemi önerilmiştir.

Çalışma frekansı, faz gürültüsü, güç tüketimi ve ayar menzili gibi performans parametrelerinin modellenerek elde edilmesinde analitik yaklaşımın yanında, Cadence® ve ADS® gibi tasarım ve benzetim araçları kullanılmıştır. Tasarlanan devrelerin ölçüm sonuçları ve liyakat hesabı (FOM), bu çalışmada kullanılan tasarım metotlarının gücünü işaret ederek, aynı teknolojiyle tasarlanmış yayınlarla karşılaştırılabilir seviyede olduğunu göstermiştir.

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To my Family

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LIST OF SYMBOLS / ABBREVIATIONS

A	Ampere
f	femto
DLL	Delay-Locked Loop
F	farad
G	Giga
gm	Transconductance
Hz	Hertz
K	Kilo
KVCO	VCO gain
KPD-CP	Phase detector & charge pump gain
L	Length of transistor
m	mili
M	Mega
n	nano
NRZ	Non-return-to-zero
p	pico
r_o	Output resistance
s	second
μ	Micro
μ_o	Mobility
PLL	Phase-Locked Loop
V	Volt
W	Width of transistor
mW	mili-Watt
ζ	Damping factor
ω_n	Natural frequency
λ	Channel length modulation
Ω	Ohm

PFD	Phase-Frequency Detector
PD	Phase Detector
CP	Charge Pump
LF	Loop Filter
CMRR	Common Mode Rejection Ratio
PM	Phase Margin
ECL	Emitter Coupled Logic
FOM	Figure of Merit
ESD	Electrostatic Discharge
Gbps	Giga bits per second
IEEE	The Institute of Electrical and Electronics Engineers, Inc.
I/O	Input/ output
LPF	Loop filter
LVDS	Low Voltage Differential Signalling
MLF	Multi Lead Frame
OPAMP	Operation Amplifier
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PSRR	Power Supply Rejection Ratio
SDM	Sigma Delta modulator
VC	Control Voltage of Voltage controlled oscillator
VCO	Voltage controlled Oscillator
VPP	Volts peak-to-peak

1. INTRODUCTION

1.1 Motivation

Wireless communication has grown, exponentially, with wide range of applications offered for the customers. Among these, WLAN (2.4-2.5GHz, 3.6-3.7GHzand 4.915-5.825GHz GHz), Bluetooth (2.4 GHz), and WiMAX (2.500-2.696 GHz, 3.4-3.8 GHz and 5.725-5.850 GHz) communication standard/technologies have found largest use local area, indoor – outdoor communication and entertainment system applications. One of the recent trends in this area of technology is to utilize compatible standards on single chip solutions, while meeting the requirements of each, to provide customers systems with smaller size, lower power consumption and cheaper in cost.

The main purpose of this thesis is to implement high resolution, low phase noise, low power consumption and spur free frequency synthesizer in small area which meets WLAN and WiMax specifications.

In this design, AMS® 0.35µ BiCMOS technology is selected, because of its high performance HBT's and low cost integration.

1.2 Thesis Organization

The goal of this thesis is designing multiband and multi-standard (WLAN and WiMAX) BiCMOS PLL frequency synthesizer with sigma delta modulator.

Chapter 2 gives a brief review of fundamentals of PLLs, loop transfer functions, stability analysis, and performance parameters.

Chapter 3 introduces Matlab® and Simulink® modeling of the architecture. Loop dynamics of both coarse and fine loop components are determined and s-domain model of the circuit is generated according to determined loop dynamics. Simulink® model of the loop is formed for the transient analyzes and corresponding simulation results are discussed.

Chapter 4 explains circuit design of all sub-blocks of the loop. Circuit and layout design techniques are given. Transistor level circuit design is discussed in detailed with Cadence® Virtuoso® Spectre® simulation results.

Chapter 5 covers top-level construction of the system, as well as the top-level simulation results.

Chapter 6 discusses measurement results of the system. Post measurement analyzes are also taken place in this chapter.

Chapter 7 is a review of the thesis, future works are also mentioned in this chapter.

2. PHASE LOCKED LOOP BASICS

2.1 Basic Topology and Transfer Functions

A phase-locked loop is a feedback system that produces a periodic signal at the same phase of an input reference signal. As represented at Figure 2.1, it consists of three basic components; phase-detector (PD), loop-filter (LPF) and voltage-controlled oscillator (VCO).

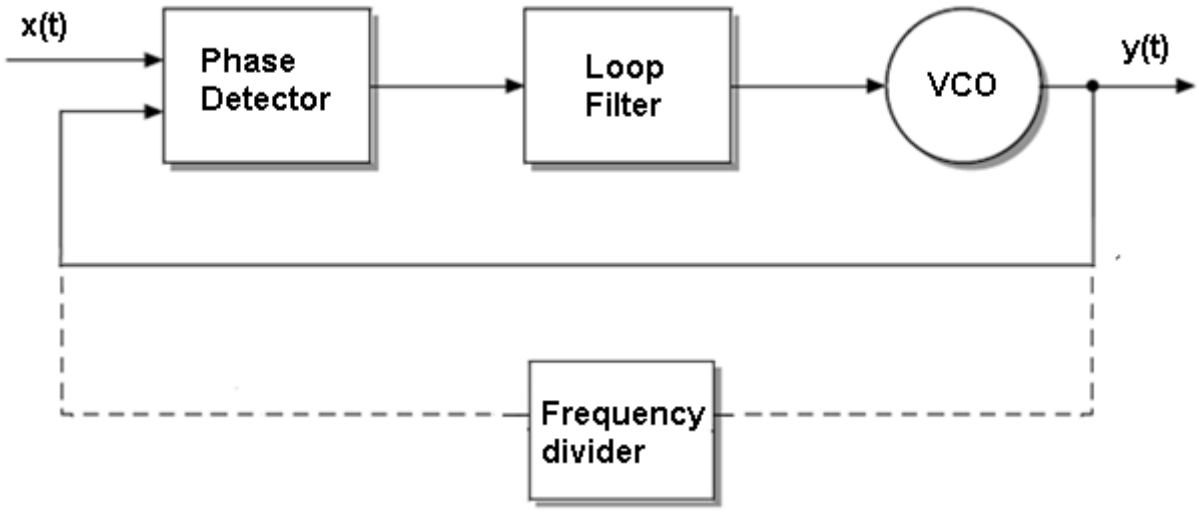


Figure 2.1: Basic phase-locked loop block diagram. Frequency divider can also be added to the system, for frequency generation.

Phase of the input signal x(t), and phase of VCO output signal y(t) are compared by the phase-detector. Phase-detector generates an output voltage according to the phase difference of two inputs. If the phase difference does not change with time, the loop is locked. Output voltage of

phase-detector is integrated by a low pass loop-filter. This Loop filter suppresses the high frequency signal components and noise. Output of the loop-filter is applied to the VCO as the control voltage. The frequency generated by VCO is changed by this voltage in a way that to decrease the phase difference. The frequency of the VCO is equal to average frequency of the input, when the loop is locked. As seen at Figure 2.1, frequency divider can be added to the loop. In this condition output of VCO will be divided before compared by phase detector. When phase of divided VCO output signal is equal to phase of input, output frequency of the loop will be equal to multiplication of input frequency and division value. Thus, PLL's are used as frequency synthesizers.

In time domain, response of PLL is nonlinear and hard to formulate. On the other hand, general approach of feedback control systems is using s domain transform. Thus, in this chapter PLL is analyzed in s domain to understand system behavior and tradeoffs.

According to the linear model, which is shown at Figure 2.2, the open loop transfer function of the system is

$$G(s) = \frac{K_{VCO} K_{PD} F(s)}{s} \tag{2.1}$$

And close loop transfer function is:

$$\frac{\theta_o}{\theta_i} = \frac{G(s)}{1+G(s)} = \frac{K_{VCO} K_{PD} F(s)}{K_{VCO} K_{PD} F(s) + s} \tag{2.2}$$

In charge pump based PLL's, current of the charge pump, I_{CP}, flows during the phase error. For whole 2π phase, K_{PD} constant is linerized as $I_{CP}/2\pi$.

Ideally, VCO generates an output frequency at $\Delta\omega$ offset from its free running frequency (ω_{FR}), while $\Delta\omega$ is proportional to the control voltage with a K_{VCO} constant. If we consider frequency is derivative of phase, VCO is linearized as K_{VCO}/s as represented at Figure 2.2.

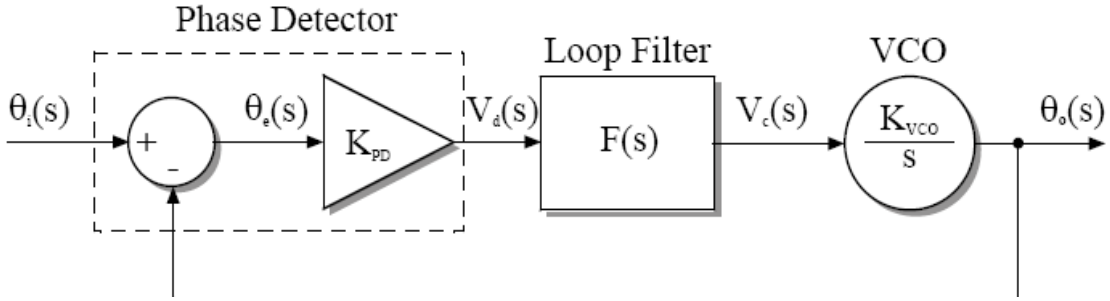


Figure 2.2: Simplified linear model of PLL

2.2 Performance Parameters of PLL

In this section, main parameters of PLL, which are important for performance measures, are shortly explained. These parameters are also important for analyses and design of the system. In most of these analyses, PD is taken as analogue multiplier, because of its linearity.

2.2.1 Loop bandwidth and Damping Factor

In order to benefit from control systems literature, where second order systems are analyzed in detail, loop filter is assumed as first order RC low pass filter and PLL becomes second order. Thus, denominator of closed loop transfer function can be modified to the well-known form used in control theory, $s^2 + 2\omega_n\zeta s + \omega_n^2$, where ζ is the damping factor and ω_n is the natural frequency of the system which is also referred as loop bandwidth [1], [3], [4].

$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\omega_n\zeta s + \omega_n^2} \tag{2.3}$$

$$\omega_n = \sqrt{K\omega_{LF}} = \sqrt{\frac{K_{VCO}I_{CP}}{NC_1 * 2\pi}} \tag{2.4}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LF}}{K}} = \frac{\omega_n}{2}RC_1 \tag{2.5}$$

According to the above equations, (2.3), (2.4) and (2.5), required three loop parameters ζ, K and ω_n, which are related to each other, must be met. Transient settling behavior of the system is determined by damping factor as seen from Figure 2.3. Loop bandwidth and damping factor are important parameters in analyze of PLL as it can be seen from following sections.

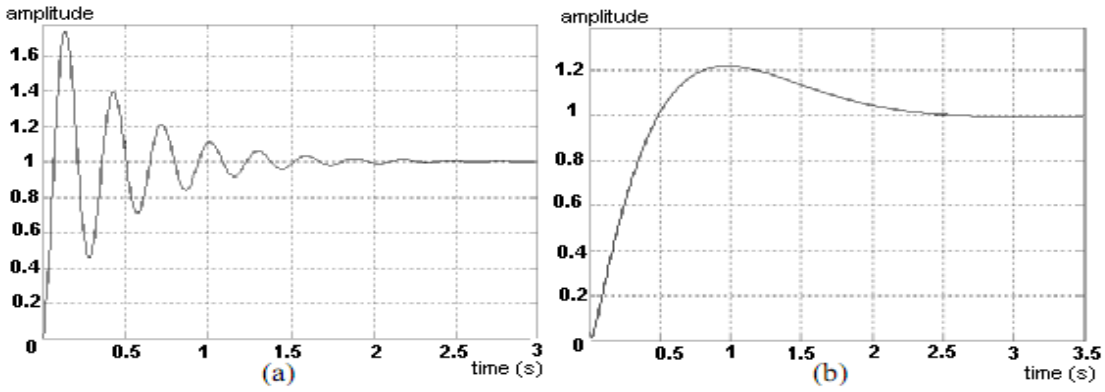


Figure 2.3: Under-damped response of PLL to a frequency step (a) ζ = 0.25, (b) ζ = 0.707[2]

2.2.2 Lock Time and Pull in Time

The amount of time needed to accomplish lock without cycle-slipping (cycle-slipping occurs if no edges are detected at one input of pfd during both up and down edges detected at the other input) is the definition of Lock time [4].

To analyze lock time in time domain, closed loop poles can be derived from (2.3) that,

$$s_{1,2} = -\zeta\omega_n \pm \sqrt{(\zeta^2 - 1)\omega_n^2} = \omega_n(-\zeta \pm \sqrt{\zeta^2 - 1}) \tag{2.6}$$

Poles are real for the condition ζ > 1 and inverse Laplace of this function will have exponential components (e^{s1t}, e^{s2t}) while the system is over-damped. For the condition, ζ < 1, the poles are complex and if we apply an input frequency step, $\omega_{in} = \Delta\omega.u(t)$ the response will be

$$\begin{aligned}\omega_{out}(t) &= \left\{1 - e^{-\zeta\omega_n t}\left[\cos\left(\omega_n\sqrt{1-\zeta^2}\,t\right) + \frac{\zeta}{\sqrt{1-\zeta^2}}\sin\left(\omega_n\sqrt{1-\zeta^2}\,t\right)\right]\right\}\Delta\omega.u(t) \\ &= \left[1 - \frac{1}{\sqrt{1-\zeta^2}}e^{-\zeta\omega_n t}\sin\left(\omega_n\sqrt{1-\zeta^2}\,t + \theta\right)\right]\Delta\omega.u(t)\end{aligned} \tag{2.7}$$

Where ω_{OUT} is the change at output frequency and $\theta = \sin^{-1}\left(\sqrt{1-\zeta^2}\right)$. Eq. (2.7) shows us that sinusoidal component decays with a time constant $\left(\zeta\omega_n\right)^{-1}$, which is also shown at Figure 2.3(a). The response of the system will not change for a phase step input. In addition, this exponential decay at Eq. (2.7) is important to define settling speed (or settling time), indicating that $\zeta\omega_n$ must be maximized. Eq's (2.4) and (2.5) yield, [3]

$$\zeta\omega_n = \frac{1}{2}\omega_{LF} \tag{2.8}$$

Thus, settling speed is inversely proportional with 3dB bandwidth of loop filter.

In practice formula of lock time can be taken as [5],

$$T_L = \frac{2\pi}{\omega_n} \tag{2.9}$$

After a frequency step input is given, in an amount of time, which is called pull in time, aimed output frequency is achieved initially. Formula of pull in time is [4],

$$T_P = \frac{\Delta\omega - \omega_L}{\pi N \omega_n^2} \tag{2.10}$$

Tradeoff between settling speed and ripple on VCO control line has become obvious after these derivations. If a small ω_{LF} is selected to increase the attenuation of high frequency components at phase detector output, settling time will increase.

Choice of ζ, which affects stability, causes other tradeoffs. First of all, reduction of ω_{LF}, degrades stability. Secondly reduction of phase error with increase of K also makes the system less stable. To conclude, tradeoffs between stability, settling speed, the ripple on the control voltage (or high frequency components on the control voltage) and the phase error are the challenges of the design of second or higher order PLLs.

2.2.3 Tracking Range (Lock Range)

PLL can track reference frequency in an amount of range. This range is defined as lock range of a PLL system. Limits of the range are determined by non-linear components of the system such as VCO and PD.

For a slow input frequency variation, $|\omega_{in}-\omega_{out}|<<\omega_{LF,}$ the magnitude of control voltage of VCO increases due to the increase of static phase error as represented at Figure 2.4. If routine change of the parameters, which are plotted in Figure 2.4, is obtained, tracking of PLL occurs.

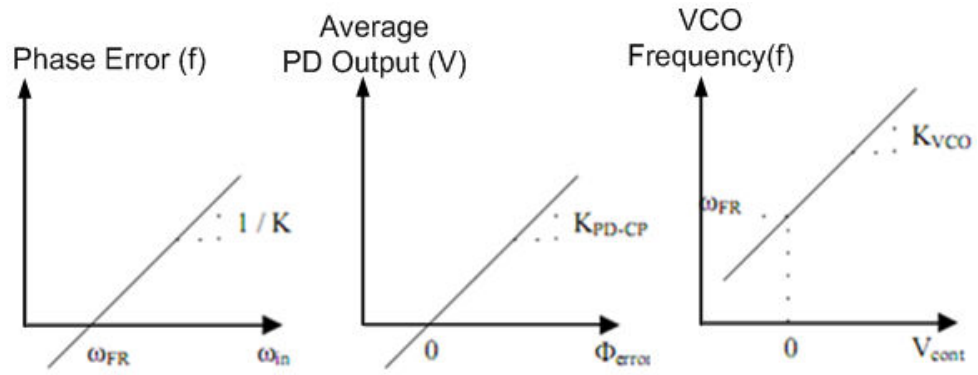


Figure 2.4: Variation of ideal parameters during tracking [2]

For a large frequency variation PD (for analogue multiplier type) behaves as non linear and average phase difference behaves as Figure 2.5(b). In addition, as seen at Figure 2.5, gain of VCO is non-linear. In some cases, the VCO gain is negative. Lock range is between the points where the slops of VCO and PD are positive.

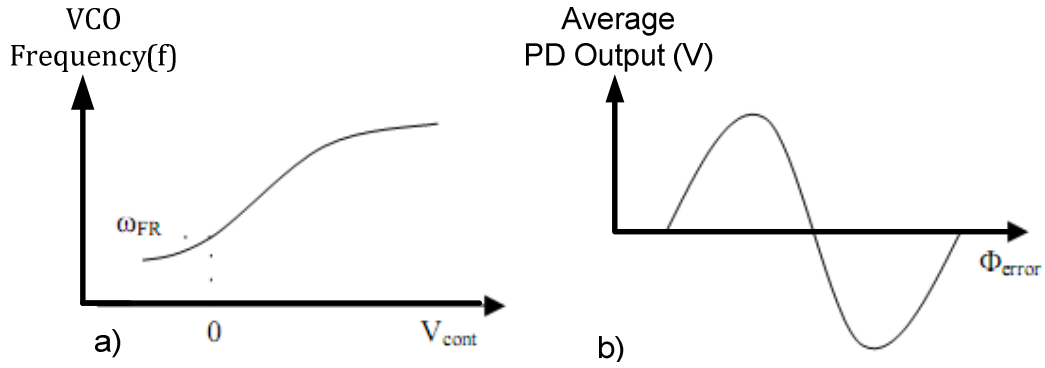


Figure 2.5: Plot of Gain values of a) VCO and b) PD in practice [2]

For analogue multiplier type PD (mixer) tracking range can be calculated as, [3],

$$\Delta\omega_{tr} = K_{PD-CP}\left(\sin\frac{\pi}{2}\right)K_{VCO} \qquad (2.11)$$

Every change at input frequency makes PLL to fail at locking. For stabilizing, a number of cycles, which is proportional to the magnitude of change, are needed. If the size of change is small, lock time is small, and transient view is tracking. Both of the two circumstances are congruent in the case of acquire lock: locked loop which detects a large input frequency change, and unlocked loop which has to lock to a frequency which is Δω away from operating frequency, [3]. Acquisition of lock concept which has mentioned above is explained in the next section.

2.2.4 Acquisition Range and Acquisition of Lock

PLL is initially oscillating at ω_{FR}, then PLL is adjusted to oscillate at ω_{FR} + Δω. In the mean time the loop try to lock new oscillation frequency, this behave of the loop is defined as acquisition of lock. Highest angular frequency step (Δω), gives acquisition range.

Phase detector is assumed as analogue multiplier type, loop filter is initially at 0, Δω cannot be attenuated by LPF, and $K_{vco}A_m$ / Δω << 1. For these assumptions variation frequency at control voltage is equal to Δω. In the first cycle of loop, output of VCO can be derived as [3]:

$$V_{out}(t) = A\cos\left(\omega_{FR}t + K_{VCO}\int A_m \cos(\Delta\omega t)\,dt\right)$$
$$= A\cos\left[\omega_{FR}t + \frac{K_{VCO}}{\Delta\omega}A_m \sin(\Delta\omega t)\right] \quad (2.12)$$
$$= A\cos(\omega_{FR}t) - \frac{K_{VCO}}{\Delta\omega}A_m \sin(\omega_{FR}t)A_m \sin(\Delta\omega t)$$

As a result of (2,12), VCO output consists of three main frequencies: $\omega_{FR} + \Delta\omega$, $\omega_{FR} - \Delta\omega$ and, ω_{FR}. In next cycle, multiplication of this output with the input signal at $\omega_{FR} + \Delta\omega$ at PD produces three components. One of these components is at DC which adjusts VCO in the direction of locking. Acquisition of lock is achieved in couple of cycles. Suppression of other components and power of DC component determines acquisition range. Loop gain decreases with respect to $\Delta\omega$, which limits acquisition range [3].

For the phase frequency detector used in this design, acquisition range of the system can be found as [7];

$$\Delta\omega_{acq} = 4\pi\zeta\omega_n = 2\pi RC_1\omega_n^2 \quad (2.13)$$

To sum up, acquisition range is proportional with loop bandwidth. Thus, acquisition range is short for the applications which need small loop bandwidth. In addition, maximum operation frequency step at input or VCO is determined by acquisition range.

2.2.5 Settling Time and Total Acquisition Time

The amount of time needed to settle in the acquisition range is the definition of settling time. For the assumption that lock range is 0.5 % of frequency range, settling time can be calculated with, [4]

$$T_S = \frac{5.29}{\zeta\omega_n} \quad (2.14)$$

The amount of time for acquisition of lock defines total acquisition time which can be calculated as [4],

$$T_{acq} = T_S + T_L \quad (2.15)$$

2.2.6 Jitter

According to ITU-T G.810 standard [6], definition of jitter is “the short-term variations of the significant instants of a timing signal from their ideal positions in time (where "short-term" implies that these variations are of frequency greater than or equal to 10 Hz).” In other words, jitter is time domain response of phase noise.

Two noise sources can be modeled as [1],

$$v(t) = A(1 + a(t))\sin(2\pi f_0 t + \theta(t)) + harmonics \tag{2.16}$$

Amplitude modulation noise is represented as a(t) and phase modulation noise is represented as θ(t). For remaining analyses, amplitude modulation noise is avoided because it does not create jitter.

To find timing jitter, Eq.(2.16) can be re arranged as [1],

$$v(t) = A\sin\left[2\pi f_0\left(t + \frac{\theta(t)}{2\pi f_0}\right)\right] = A\sin\left[2\pi f_0(t + \Delta T(t))\right] \tag{2.17}$$

And timing jitter, ΔT, is, [1],

$$\Delta T(t) = \frac{\theta(t)}{2\pi f_0} \tag{2.18}$$

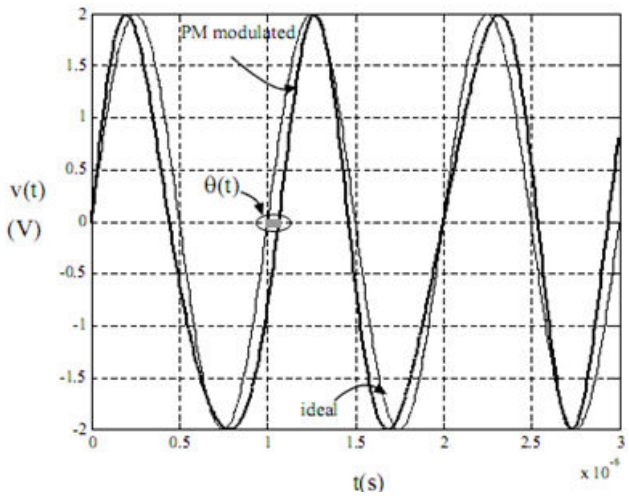


Figure 2.6: Phase modulated signal and Jitter [1]

2.2.6.1 Specific Jitter definitions

If the standard deviation of the timing jitter is taken, RMS timing jitter is defined as

$$\Delta T_{rms} = \sigma_{\Delta T} \tag{2.19}$$

Cycle-to-Cycle Jitter: Period difference of sequential cycles is Cycle-to-Cycle jitter, [14].

Period Jitter: Period jitter is comparison of the length of each period with average period, T_0, of an ideal signal. For each measured period, T_n, difference, T_n-T_0, is period jitter.

Long-Term Jitter: The rising or falling edge variation after "n" cycles defines long term jitter (Figure 2.7). Number of cycles, n, is selected according to application or frequency, [15].

For a free-running oscillator, long-term jitter increases proportional to the measurement time. All the following transitions are affected by any wavering in earlier transitions, and effect stays infinitely. This is also called jitter accumulation.

If we assume Gaussian distribution is valid for long term jitter, the peak to peak jitter is defined between (-3 σ, 3σ). Thus, the peak-to-peak jitter is [15]:

$$\Delta T_{pp} = 6\sigma_{\Delta T} \tag{2.20}$$

That is defined in terms of seconds.

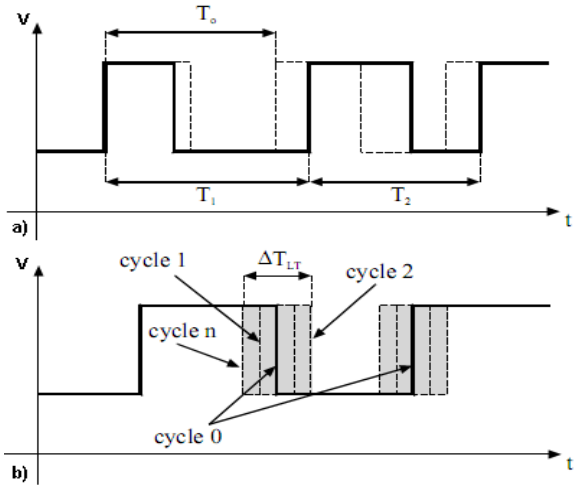


Figure 2.7: a) Cycle to cycle jitter (T_2-T_1) and Period jitter (T_1-T_0) b) Peak to peak jitter in long term [1]

Eye Diagram

In eye diagram, which is best view for jitter, edge placements of generated signals are plotted cumulatively. Due to jitter, edges of signal are located at different coordinates for sequential periods of signal. Figure 2.8 (a) represents basics of eye diagram. To analyze a signal with period T, the time axis is divided into pieces of length T/2. Each piece is folded up on the following one. Folding is started, t=0, with a zero crossing of the signal, then for an ideal sinusoidal signal, the gap at the center of the diagram looks like an eye, thus, it is called an eye diagram. If zero crossing (edge) jitter increases, the apparent eye begins to close Figure 2.8 (b). Figure 2.8 (c) shows peak to peak calculation.

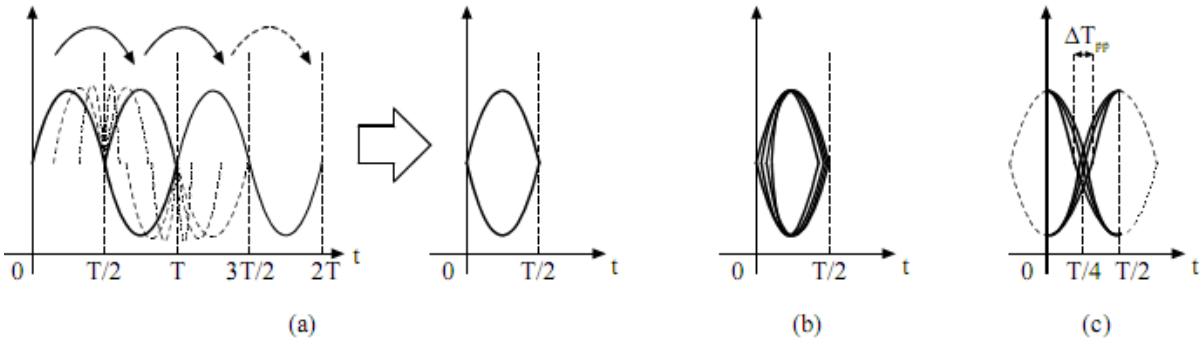


Figure 2.8: (a) Eye-diagram operation, (b) Eye-diagram of a jittered sine wave, (c) Eye-diagram for peak-to-peak jitter calculation. [1]

2.2.7 Phase Noise

Main purpose of frequency synthesizers, in ideal, is to generate a Dirac delta function in an aimed frequency as shown at Figure 2.9 (a). In practice, output spectrum of frequency synthesizer consists of two types of phase terms as shown at Figure 2.9(b). First type is random phase fluctuations caused by internal noise sources, such as flicker noise, shot noise, thermal noise etc., and external noise sources, such as power supply fluctuations. Second type is spurs, caused by internal imperfections of frequency synthesizers such as quantization noise, current mismatches etc [16].

As can be seen from Figure 2.9, phase noise distribution is symmetric around the oscillation frequency [17], therefore, phase noise single-sideband is defined as the ratio between noise power in a 1 Hz bandwidth with an offset, $\Delta\omega$, and the signal power which is specified in dBc/Hz as [17],

$$PN_{SSB}(\Delta\omega) = 10\log\left[\frac{(1/2)(V_0\theta_p/2)^2}{(1/2)V_0^2}\right] = 10\log\left[\frac{\theta_p^2}{4}\right] = 10\log\left[\frac{\theta_{rms}^2}{2}\right] \quad (2.21)$$

Where θ_{rms}^2 is the rms phase noise power density in units of [rad^2/Hz].

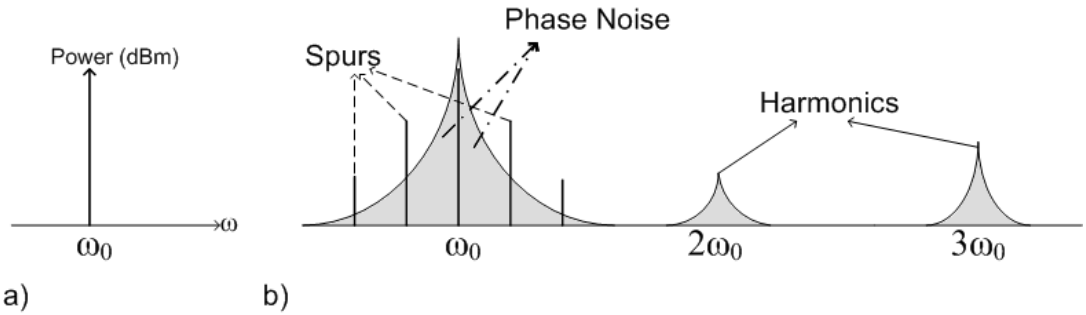


Figure 2.9: output of oscillators in frequency domain a)ideal b)practical

Alternatively double sideband noise can be written as, [17]

$$PN_{DSB}(\Delta\omega) = 10\log\left[\frac{P_{Noise}(\omega_0+\Delta\omega)+P_{Noise}(\omega_0-\Delta\omega)}{P_{carrier}(\omega_0)}\right] = 10\log\left[\theta_{rms}^2\right] \quad (2.22)$$

The rms phase noise can be obtained in the linear domain as, [17]

$$\theta_{rms}(\Delta\omega) = \frac{180}{\pi}\sqrt{10^{PN_{DSB}(\Delta\omega)/10}} = \frac{180\sqrt{2}}{\pi}\sqrt{10^{PN_{DSB}(\Delta\omega)/10}}\left[\text{deg}/\sqrt{Hz}\right] \quad (2.23)$$

It is also important to mention rms integrated phase noise over a certain bandwidth. The limits of integration are usually offsets which correspond to the lower and upper frequencies of the bandwidth of the information being transmitted, [17].

$$IntPN_{rms} = \sqrt{\int_{\Delta\omega_1}^{\Delta\omega_2}\theta_{rms}^2(\omega)d\omega} \quad (2.24)$$

In addition, it should be noted that dividing or multiplying a signal in the time domain also divides or multiplies the phase noise. Similarly, if a signal is prescaled to a frequency by a factor of N, the phase noise power is increased by a factor of N^2 as [17]:

$$\theta_{rms}^2(N\omega_0+\Delta\omega) = N^2\theta_{rms}^2(\omega_{LO}+\Delta\omega),$$

$$\theta_{rms}^2\left(\frac{\omega_{LO}}{N}+\Delta\omega\right) = \frac{\theta_{rms}^2(\omega_{LO}+\Delta\omega)}{N^2} \quad (2.25)$$

2.2.7.1 Noise Analysis of the loop

Each component of the loop adds phase noise to the system and noise is shaped by the transfer functions of the components. Total phase noise of complete PLL is the combination phase noises generated by all blocks. Figure 2.10 shows linear model of PLL with noise sources.

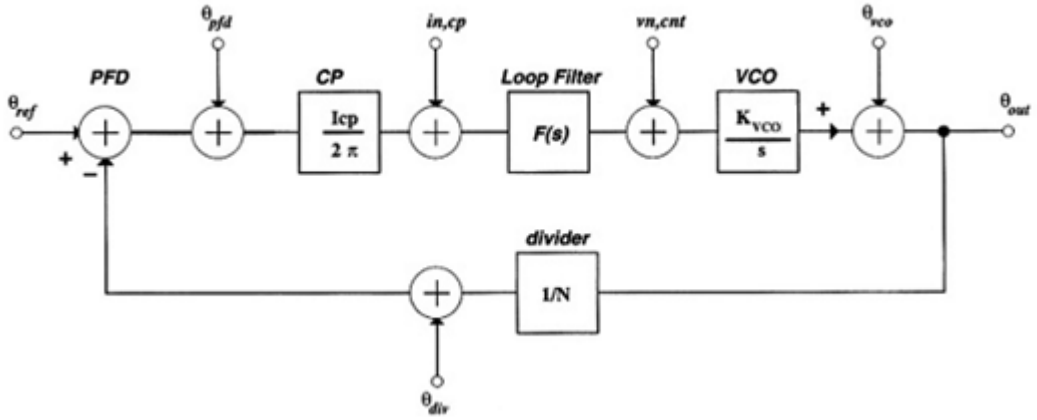


Figure 2.10: Linear model of PLL with noise sources[**16**]

θ_{VCO} is the phase noise of the VCO in *rad/*$\sqrt{Hz}$ which can be described as [19, 20]

$$\theta_{VCO}^2(\Delta\omega) = \left(\frac{\omega_0}{(2Q\Delta\omega)}\right)^2 \left(\frac{GkT}{2P_S}\right)\left(1+\frac{\omega_C}{\Delta\omega}\right) \tag{2.26}$$

Where, flicker noise corner frequency is represented as ω_c , G is proportionality constant to model transistor noise and nonlinearity and power of fundamental frequency (ω_0) is P_S.

θ_{ref} represents the phase noise of crystal resonator that can be used as reference frequency is another important parameter, which can be found from Leeson's formula [21]:

$$\theta_{ref}^2(\Delta\omega) = 10^{-16\pm1}\left[1+\left(\frac{\omega_0}{2\Delta\omega Q_L}\right)^2\right]\left[1+\frac{\omega_C}{\Delta\omega}\right] \tag{2.27}$$

Loaded quality factor of Crystal is represented as Q_L which is in the order of 10^4 to 10^6. The noise converges to thermal noise floor at offset frequency around ω_c.

Frequency divider noise is represented as θ_{div}. Rather than phase noise, spurious noise is generated by frequency dividers. Empirical phase noise formula of frequency dividers is provided by Kroupa, where ω_{do} is output frequency of divider, [22,23]:

$$\theta_{div}^2(\Delta\omega) \approx \frac{10^{-14\pm1} + 10^{-27\pm1}\omega_{do}^2}{2\pi\Delta\omega} + 10^{-16\pm1} + \frac{10^{-22\pm1}\omega_{do}}{2\pi} \tag{2.28}$$

Phase noise of phase frequency detector is represented as θ_{PFD} which is estimated empirically by [23]:

$$\theta_{PFD}^2(\Delta\omega) \approx \frac{2\pi 10^{-14\pm1}}{\Delta\omega} + 10^{-16\pm1} \tag{2.29}$$

$i_{n,cp}$ is the noise of the CP current which can be characterized as an output noise current and is usually given in pA/√Hz. The results depend on the design in question so no simple general analytical formula will be given here.

In this design second order loop filter is selected, the reasons of this selection is explained at chapter 3. The loop filter with its associated noise source is shown at Figure 2.11.

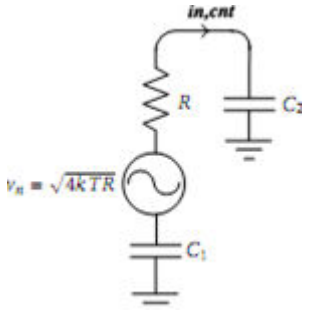


Figure 2.11: loop filter with thermal noise added [**16**]

Noise voltage provided by the resistor, generates a noise current which is given by

$$i_{n\_cnt} = \frac{1}{R}\frac{v_n s}{s + (C_1 + C_2)/(C_1 C_2 R)} \approx \frac{1}{R}\frac{v_n s}{s + 1/(C_2 R)} \tag{2.30}$$

No DC component occurs as can be seen from (2.31), and noise will be flat after cut off frequency [17]. Charge pump noise can be added to this noise.

Final output noise can be derived as

$$\theta_{out}^2 = \left(\frac{G(s)}{1+\frac{G(s)}{N}}\right)^2 \left[\theta_{ref}^2 + \theta_{div}^2 + \theta_{pfd}^2 + \left(i_{n,cp}\frac{2\pi}{I_{CP}}\right)^2\right] + \left(\frac{1}{1+\frac{G(s)}{N}}\right)^2 \left[\theta_{vco}^2 + \left(v_{n,c}\frac{2\pi K_{VCO}}{s}\right)^2\right] \tag{2.31}$$

Noise shaping effect can be observed by the noise transfer function [16]. Phase noise of VCO and its control voltage noise are multiplied by $1/(1+\frac{G(s)}{N})$, which is a high pass filter. These

noises are attenuated inside the loop bandwidth while they are effective above the loop bandwidth. On the other hand noises of other components are multiplied by $G(s)/(1+(G(s)/N))$ which behaves as low pass filter. Thus, PFD, CP, frequency divider and reference signal are primary noise sources at low frequencies. In addition, noises from these components are proportional with division ratio of frequency divider (N). Noise shape behavior of PLL is decided by loop bandwidth. For minimum integral noise at PLL output, optimum loop bandwidth must be selected.

From fundamental frequency to 100Hz-1KHz offset frequencies (first region), reference oscillator noise is dominant. From this corner to the loop bandwidth corner of PLL (second region), phase frequency detector charge pump and frequency divider noises are dominant. Above the loop bandwidth (third region), VCO noise is dominant. The performance of PLL can be observed at second region, [16].

Noise floor of PLL can be defined as, [16]

$$L_{pll,nf} = L_0 - 20\log(N) - 10\log(f_{ref}) \quad (2.32)$$

Phase noise inside loop bandwidth is represented as L_0 in terms of *dBc*. Total noise caused by loop components are represented at $L_{pll,nf}$. Noise due to reference frequency is 10 log(f_{ref}). Because of frequency multiplication, phase noise is increased as 20 log(N). Performance of a given PLL can be observed by noise floor in consideration of N and reference frequency, [17].

3. MODELING AND SIMULATING FREQUENCY SYNTHESIZER AT MATLAB®

Before start of physical circuit design, understanding the influence of circuit defects to complete operating characteristics is must. Modeling whole system is also needed for an adjustable and durable circuit. In consideration of design specifications, a combined simulation environment that allows the modeling of all important circuit deteriorations is essential. To expedite observing either tradeoffs between performance and complexity of system or tradeoffs between circuit blocks, overall simulations are needed. Use of wide-range modeling tools such as; Matlab® Simulink® 1) reduces the design time, in pursuance of acquiring essential design and model parameters, 2) examining signal flow and 3) ascertainment of system characteristics.

Important circuit parameters such as damping factor, settling time, phase margin, -3dB bandwidth etc. have been examined and optimized by usage of MATLAB®. Modeling of the circuit and the system by this program has continued at the higher steps of the physical circuit design.

To model the Frequency Synthesizer, Simulink® from The Mathworks and techniques at [34] have been used. "Simulink® is an environment for multidomain simulation and Model-Based Design for dynamic and embedded systems. It provides an interactive graphical environment and a customizable set of block libraries that let you design, simulate, implement, and test a variety of time-varying systems" [24]. The challenges for simulating analogue non-ideal effects with Matlab® and Simulink®, and solutions are described at this chapter.

3.1 Selection of Order and Type of Loop filter

Before performing simulations at Matlab® , type, order and transfer function of loop filter must be selected.

Fluctuations at control voltage of VCO are needed to be suppressed by loop filter which is also used to integrate the charge pump current. PLL is at least second order without a loop filter, because the input capacitance of VCO and output capacitance of charge pump produces a pole. For a first order low pass filter which can be implemented as Figure 3.1, loop filter transfer function, $F(s)$, will be :

$$F(s) = \frac{1}{1 + \frac{s}{\omega_{LF}}} \tag{3.1}$$

Where, $\omega_{LF} = \frac{1}{RC} = \frac{1}{\tau}$. Thus, equation (2.1) can be reordered as

$$G(s) = \frac{K/\tau}{s^2 + s/\tau} \tag{3.2}$$

and, equation (2.2) can be reordered as:

$$\frac{\theta_o}{\theta_i} = \frac{G(s)}{1+G(s)} = \frac{K_{VCO}K_{PD}\omega_{LF}}{K_{VCO}K_{PD}\omega_{LF} + s(\omega_{LF}+s)} = \frac{K_{VCO}K_{PD}\omega_{LF}}{s^2 + s\omega_{LF} + K_{VCO}K_{PD}\omega_{LF}} \tag{3.3}$$

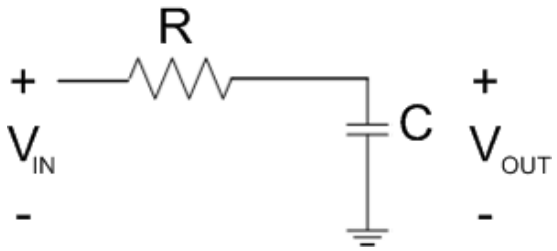


Figure 3.1: First order Low pass filter

In order to analyze the open loop transfer function, the root-locus of equation (3.3) is plotted at Figure 3.2. At start, K=0, poles of transfer function are located at s=0 and s= -1/τ. As the increase of loop gain, K, the poles come closer and meet at halfway and become a complex conjugate pair, then these poles move to infinity along a vertical line at s=-1/2τ. The gain is inversely proportional to damping. In addition, the system is unconditionally stable, [1].

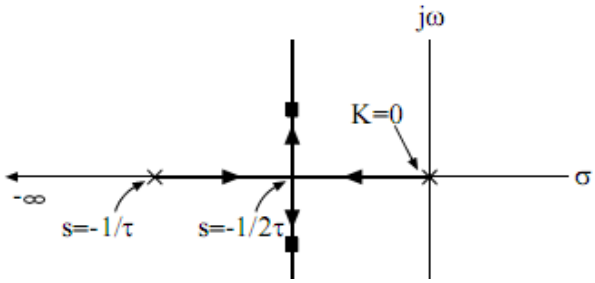


Figure 3.2: Root-locus plot of a PLL with a first order low pass filter, the system is unconditionally stable [1]

For a better suppression of high frequency components at the phase detector output, without having essential effect on the loop bandwidth and damping factor, another is added as Figure 3.3. Then, this loop filter will have a transfer function as:

$$F(s)=\frac{s\tau_2+1}{s\tau_1(s\tau_3+1)}=\frac{sC1R+1}{s^2C_1C_2R+s(C_1+C_2)} \tag{3.4}$$

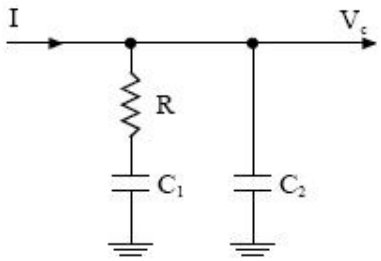


Figure 3.3: Second order low pass filter, this filter has been used at design of the system

One of the poles of the loop filter is located at ω=0 and another one is at ω=-1/τ3, and zero of the filter is at ω=-1/τ2. As mentioned above, not to change second order characteristics, the pole at ω=-1/τ3 should be placed far from the crossover frequency. After using this filter, open-loop transfer function becomes:

$$G(s)=\frac{K(s\tau_2+1)}{s^2\tau_1(s\tau_3+1)} \tag{3.5}$$

Figure 3.4 represents the root-locus plot. Two of the open loop poles are located at zero and open-loop pole is at ω=1/τ3 while the system is having a zero at ω=1/τ2. As shown in the figure, according to the increase of the gain to infinity, the third pole converges to the zero and the other poles become complex conjugate chasing a curve while making the system unconditionally stable [1].

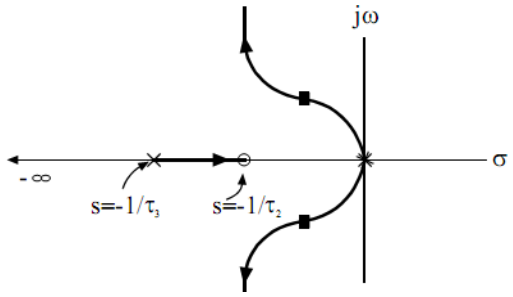


Figure 3.4: Root locus of the third order PLL, with second order low pass filter represented at Figure 3.3. The system is unconditionally stable, [1]

Using higher order loop filters will have better performance on attenuating fluctuations at control voltage of VCO, which cause phase noise and jitter. Because of the need for high C_1 capacitance at control voltage of VCO, which will be explained at chapter 5, loop filter must be second order. Additionally, in practice VCO gain is highly non-linear (which is explained at chapter 4) and brings additional poles to system which degrades stability. Behavior of VCO also changes at different bands. Moreover, to operate at different bands, division ratio of loop must be changed. Furthermore, after insertion of additional blocks which controls division ratio such as accumulators or sigma delta modulators, stability will also be degraded. Because of unconditionally stabile behavior of the system (at least in linear approach), second order loop filter is selected.

3.2 Determining loop Parameters

In order to make loop stable, loop parameters such as loop bandwidth and damping factor have to be determined. These parameters must supply all performance parameters for all bands. At this stage, both Simulink® models and .m files are used. After iterations Table 3-1 has been generated. These parameters have been used for following MATLAB® models and calculations.

Table 3-1: Loop parameters and values

Parameter	Value	Unit	Expression
$K_{VCO\ Band1}$	0.8	GHz/V	Gain of The VCO for band 1 (5G)
$K_{VCO\ Band1}$	0.36	GHz/V	Gain of The VCO for band 2 (3.6G)
$K_{VCO\ Band3}$	0.3	GHz/V	Gain of The VCO for band 3 (2.4G)
C1	384	pF	Loop filter Capacitor
C2	48	pF	Loop filter capacitor
R	7.5K	Ohm	Loop filter resistor
I_{cp1}	104	µA	Charge pump current for band1
I_{cp2}	270	µA	Charge Pump current for band2 and 3
N	64-124	N/A	Final Ratio of the divider Circuit

After applying the values for band 1 to the transfer functions at (3.4) and (3.5) final closed loop is represented at Figure 3.5.

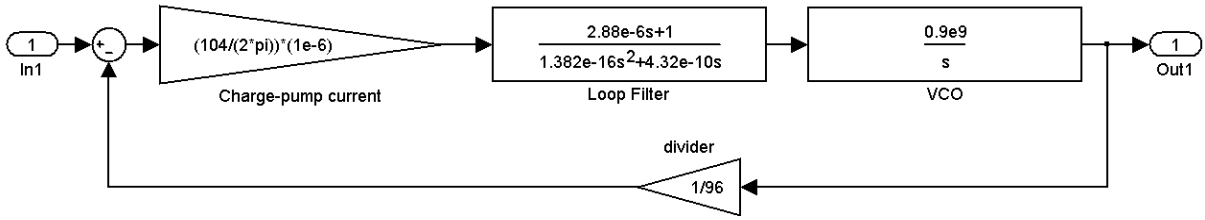


Figure 3.5: Closed loop block diagram for the values at Table 3-1.

With these values, final open and close loop transfer function of the loop will be:

$$G(s)=\frac{K_{VCO}K_{PD}F(s)}{Ns}=\frac{K_{PD}K_{VCO}(sC1R+1)}{Ns(s^2C_1C_2R+s(C_1+C_2))}=\frac{3.234\bullet10^{12}s+1.123\bullet10^{18}}{s^3+3.125\bullet10^6s^2} \quad (3.6)$$

$$H(s)=\frac{\theta_o}{\theta_i}=\frac{K_{PD}K_{VCO}(sC1R+1)}{Ns(s^2C_1C_2R+s(C_1+C_2))+K_{PD}K_{VCO}(sC1R+1)}$$
$$=\frac{3.104\bullet10^{14}s+1.078\bullet10^{20}}{s^3+3.126\bullet10^6s^2+3.234\bullet10^{12}s+1.123\bullet10^{18}} \quad (3.7)$$

Generally, for stabile systems desired phase margin is 65^0. Because of selected VCO topology, C2 capacitance must be selected maximum (which is explained at chapter 5). C1/C2 ratio is one of the most important criteria which determines phase margin. For 62^0 open loop phase margin C1 must be 16 times larger than C2. 53.1^0 phase margin is enough for stability, thus, to save area, C1/C2 is taken around 8.

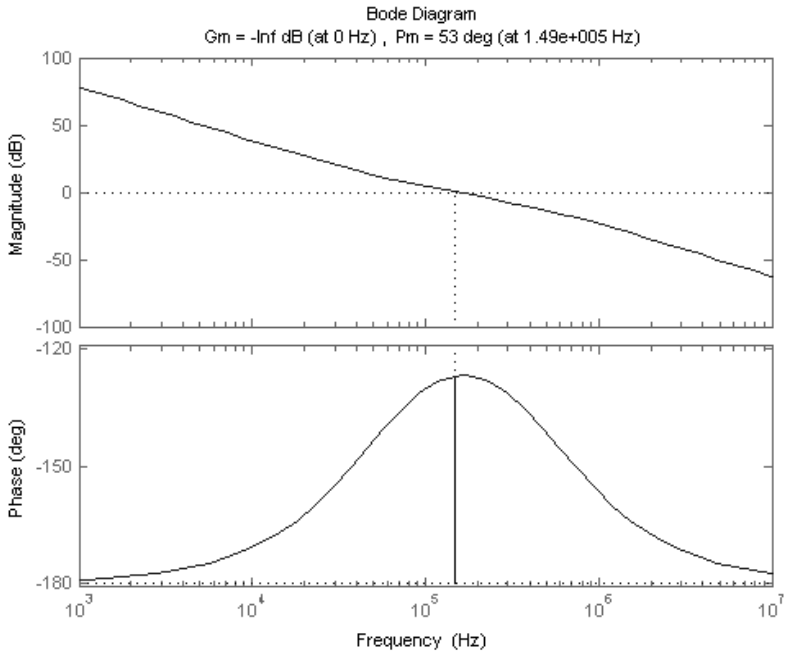


Figure 3.6: Open loop Bode plot of the system. Phase margin of the loop is 53^0

3dB bandwidth (loop bandwidth) of the closed loop, which is shown at Figure 3.7, defines lower limit of synthesizer step size [25]. This parameter must be small enough. As it is shown at eq. (2.14), loop bandwidth must also be large enough to decrease settling time. Figure 3.7 shows that, loop bandwidth of the system is 267 kHz which is selected in consideration of the tradeoffs mentioned above, and, acquisition range and acquisition time are also concerned. If loop parameters are applied to the eq. (2.14),

$$T_S = \frac{5.29}{\frac{K_{VCO} I_{CP}}{NC_2 * 2\pi} \frac{RC1}{2}} = 10.227\mu s \tag{3.8}$$

Figure 3.8 shows step response of the loop. Step response is used for observation of the settling and settling time is around 10µs.

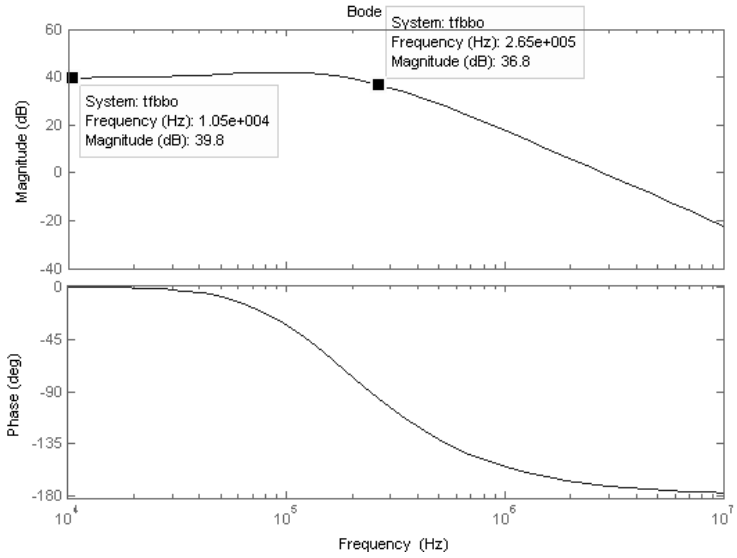


Figure 3.7: Bode plot of the closed loop transfer function. Loop bandwidth is 267kHz

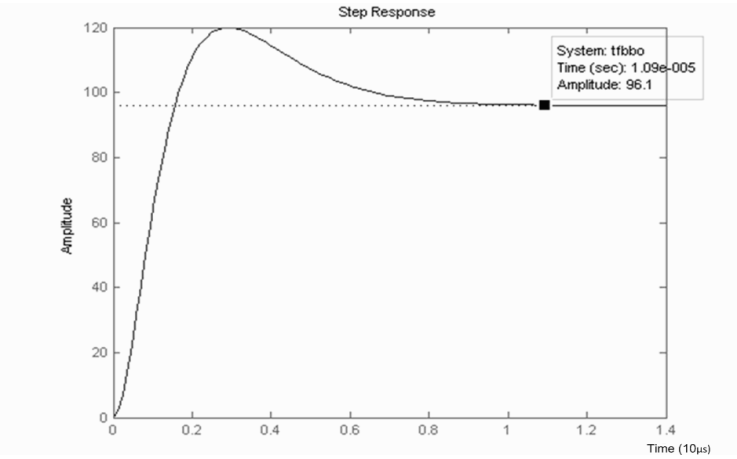


Figure 3.8: Step response of Closed loop transfer function.,

The stability behavior of the loop can also be analyzed by the root locus plots of open and closed loop transfer functions. These figures can be found at Appendix B1. From these figures it is obvious that no pole leaves left hand plane, thus, open and closed loop stabilities are obtained, [26].

3.3 SİMULİNK® MODELS of PLL BLOCKS

3.3.1 Phase Detectors

Xor gates, SR flip-flops, analog multipliers and switching phase detectors can be used for detection of phase. The one used is phase frequency detector, which is represented at Figure 3.9.

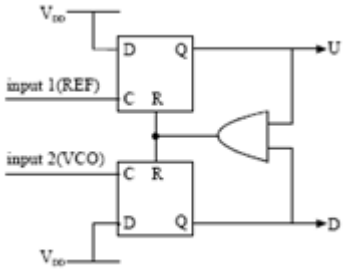


Figure 3.9: Gate level representation of Phase Frequency Detector [1]

Figure 3.10 represents progress of the phase-frequency detector. To analyze this block, initial condition is set such that, input frequencies are evenly matched and VCO output follows reference input with a phase error θ_e. For arriving of each rising edge of the reference, the U output will have logic high value. Subsequent arrive of rising edge of the VCO output, either U or D outputs are set to logic high for a short while, thus, a pulse at reset input of the flip flops which is connected to the output of AND gate is generated. This reset pulse pulls U and D down to logic low. AND gate is assumed as ideal, which does not have a gate delay. If output of VCO is behind of the reference input, the phase difference is signified by the mean value of the U. On the contrary, if output of VCO is followed by the reference input, phase difference is signified by D output, while mean value of the U is practically zero. In ideal U and D cannot be active at the same time.

First Simulink® model is represented at Figure 3.11. For instance, reference frequency is 1MHz and the feedback is 0.5 MHz, the up and down signals generated by PFD can be seen at Figure 3.12. As a second example, reference frequency = 0.5MHz, feedback = 1MHz, the output can be

seen at Figure 3.13. It is obvious that, the expected waveforms are achieved except non zero outputs at Figure 3.12 (b) and Figure 3.13(a), which is caused by non zero delay of AND gates.

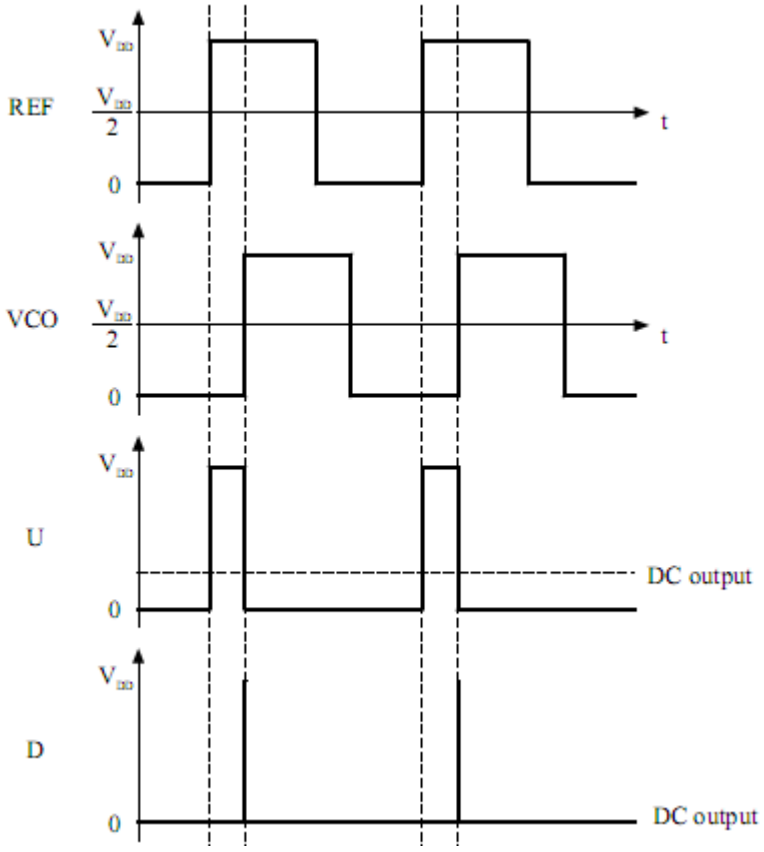


Figure 3.10: Progress of Phase and frequency detector [1]

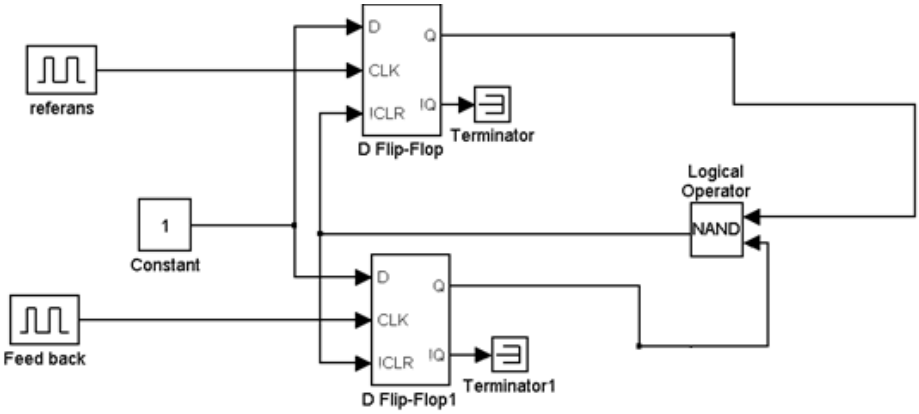


Figure 3.11: Phase frequency detector block

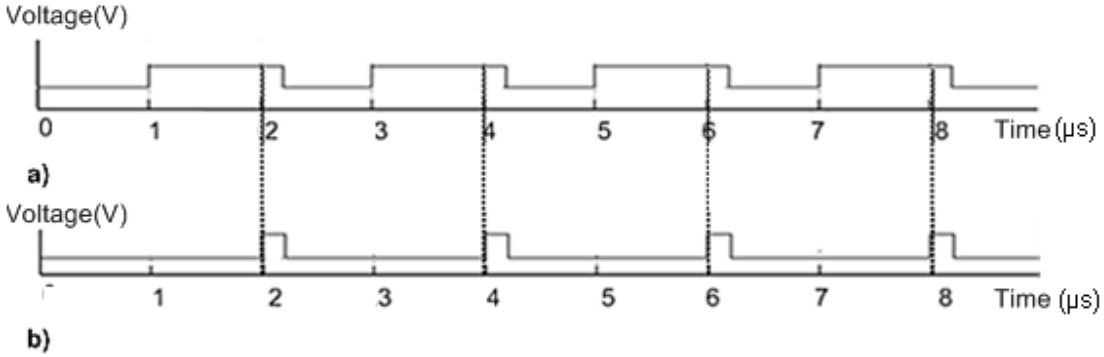


Figure 3.12: Simulink® result of PFD. The output signals for high frequency reference low frequency feedback signal: a) is up signal b)is down signal. Time of up signal is larger to reduce frequency difference between two inputs of Phase frequency detector.

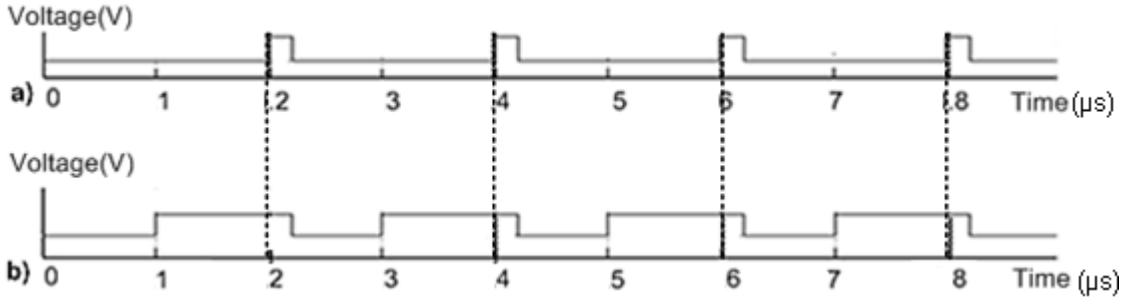


Figure 3.13: Simulink® results of PFD. The output signals for high frequency reference low frequency feedback signal: a) is up signal b)is down signal. Contrast of the situation at Figure 3.12

3.3.2. Charge Pump

Charge pump is a circuit that supplies + I_1 current when up signal comes and supplies $-I_2$ current when down signal comes. This circuit is explained at chapter 4. Simplified charge pump circuit is represented at Figure 3.14 (a) and simple Simulink® model is shown at Figure 3.14 (b).

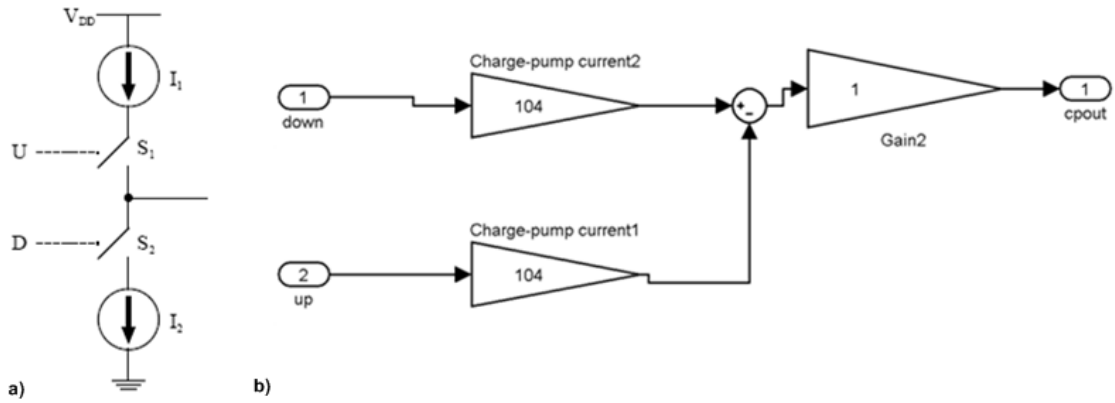


Figure 3.14: a) Simplified charge pump circuit b) Charge pump model for Simulink®

3.3.3 Loop Filter

Loop filter is represented as a transfer function at Simulink® which can be seen at Figure 3.15.

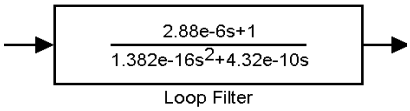


Figure 3.15: Loop filter model for Simulink®

3.3.4 VCO

VCO is modeled by a single block at Simulink® where free running frequency, VCO gain and initial phase are defined.

3.3.5 Frequency Dividers

Two types of dividers have been used in this thesis; single mode frequency divider and multi mode frequency divider. Although both synchronous and asynchronous counters can be used as single mode frequency divider, asynchronous frequency dividers have been used because of their low power consumption and low area.

An asynchronous divide-by-two circuit is shown at Figure 3.16. Logic high is assumed as initial value of Q. After arriving of rising edge of clock signal, Q will be set to high which will be inverted after subsequent rising edge of clock. Thus, Q and Q' generate a square signal which has half frequency of clock signal.

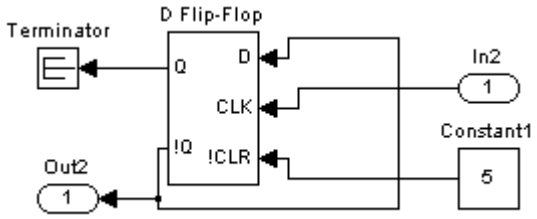


Figure 3.16: Divide-by-two circuit

In fractional N PLL systems, at least two different division ratios are needed to make fractional division. For this purpose dual modulus dividers are being used. 2/3 dual modulus divider is represented at Figure 3.17. According to the Figure 3.17, if control value is set to zero, first flip-flop (FF1) is eliminated and second flip-flop (FF2) acts like asynchronous divide-by-two circuit. For the contrary, if control signal is high, assuming that initial value of Q output of FF2,

which is also D value of FF1, is as set logic high. After arriving rising edge of CLK, Q' value will be set to 0, D input of FF2 will be set to 0, Q output of FF2 remains high because signal comes to D two gates delay later than the rising edge. After arriving of subsequent rising edge of CLK, Q value of FF2 will be set to low, and D input will be set to high, while Q' of FF1 remains zero. After arriving of next rising edge of CLK, Q value of the FF2 will be set to high while Q' of FF1 is set to high which will make D value high. After arriving of subsequent rising edge of CLK, Q of FF2 remains high while making a series of low–high–high–low–high–high, which has a period three times of CLK. Thus, frequency is divided by 3. Output of dual modulus divider is shown at Figure 3.18. According to this figure after 30s the control signal changes 1 to zero; the change at division ratio can be seen from Figure 3.18 (a), while clock frequency is represented at Figure 3.18 (b).

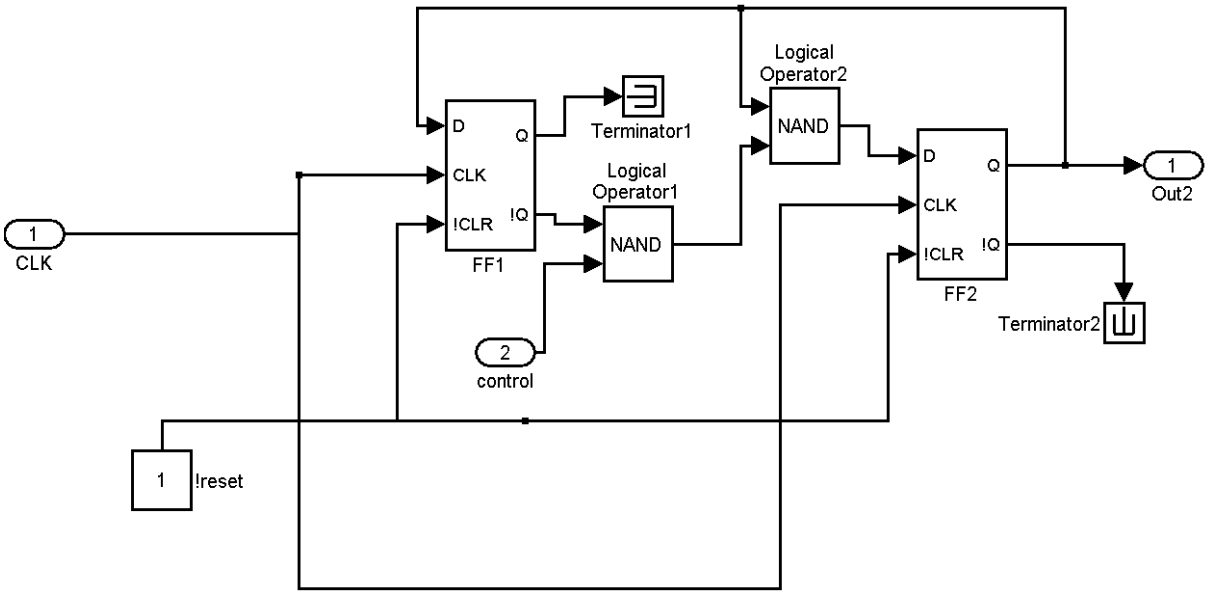


Figure 3.17: Dual modulus Divider

For either, multiband PLLs or PLLs which have second or higher order ΣΔ modulators, frequency dividers which have more than two division ratios are needed. These frequency dividers are also called as multi-modulus frequency dividers. A two bit divider which has divider value range starts from 4 to 7 is represented at Figure 3.19. According to this figure,

- If C0 and C1 are zero, dual-modulus dividers will act like cascade asynchronous divide-by-two circuits where frequency is divided by four.
- Assuming C0 is high and C1 is low, if Q output of dual modulus2 is high, dual modulus1 divides frequency by three, else dual modulus1 divides frequency by two. Output of circuit will have three periods high and two periods low, thus input frequency is divided by five.

- Assuming C0 is low and C1 is high, dual modulus1 always divides frequency by two, while dual modulus2 divides frequency by three, thus frequency is divided by six.
- Assuming C0 and C1 are one, if Q output of dual modulus2 is one, dual modulus1 divides frequency by three(with 66% duty cycle, with a sequence 1-1-0) , else dual modulus1 divides frequency two while dual modulus always divides frequency by three. If the inverse output of the frequency divider is zero which will be zero for two times, dual modulus divider1 divides frequency by two. Else dual modulus divides frequency by three so seven cycles pass for all division period, while the frequency is divided by seven. Outputs of divider and clocks of dual modulus dividers are represented at Figure 3.20.

Four bits multi-modulus frequency divider is used at Designed PLL, which is shown at Figure 3.21. The division mentality is the same as two bits 4-7 multi-modulus frequency divider which has been explained above.

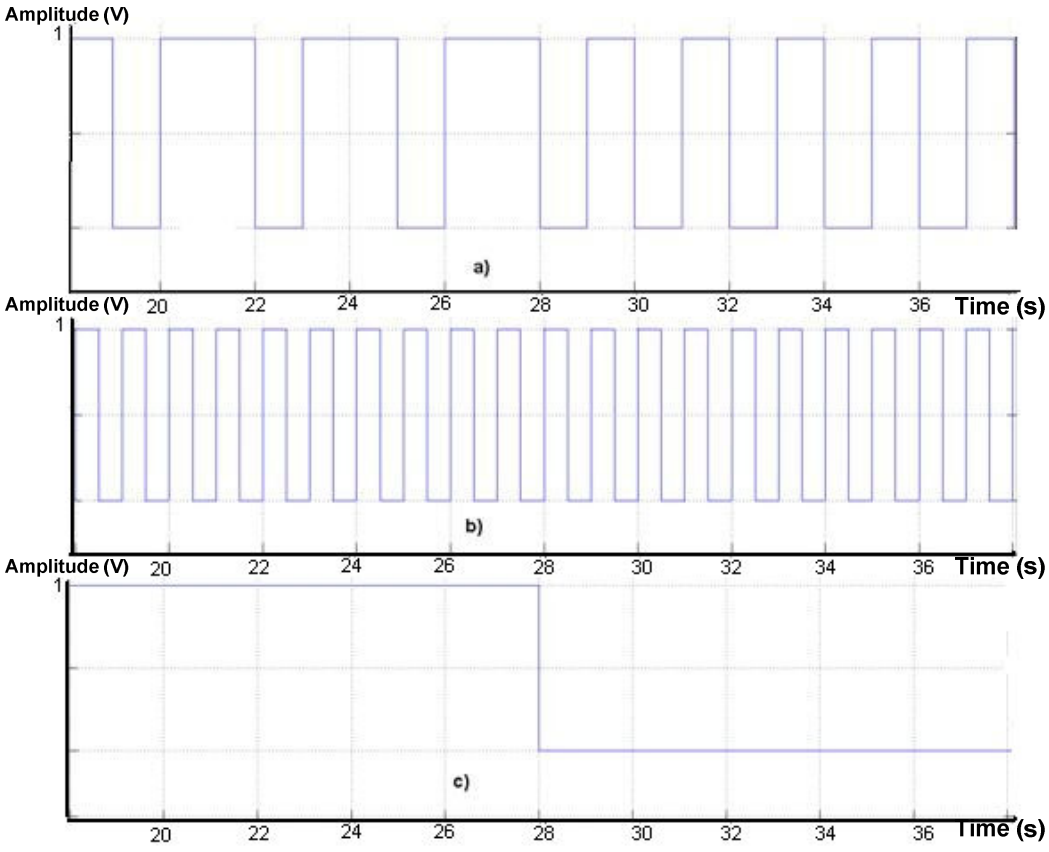


Figure 3.18: Output of dual modulus divider. a) Divided output, b) Clock signal, c)control signal, when the control signal is high, period of output signal is one and half square length. In contrast situation, period is one square length

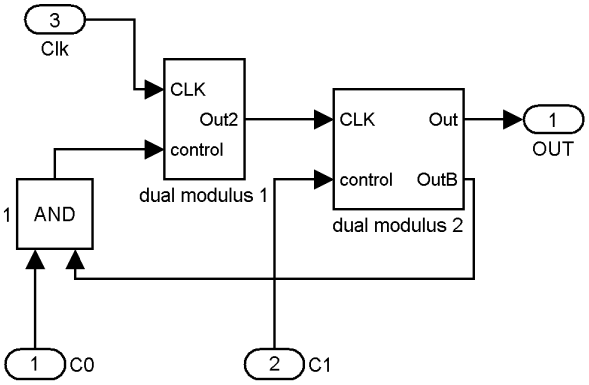


Figure 3.19: Two bits Multi modulus divider (4-7 multimodulus)

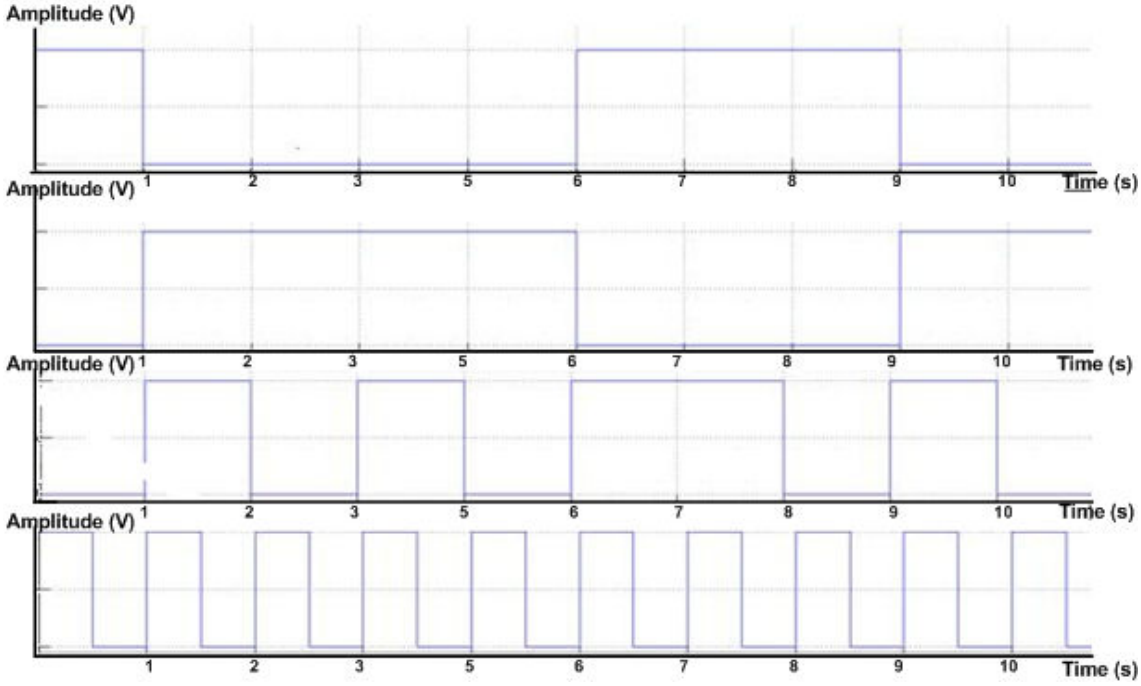


Figure 3.20: a) inverse output of 4-7 multimodulus divider, b) output of 4-7 multimodulus divider c)clock of second dual modulus divider d)clock of 4-7 multimodulus divider

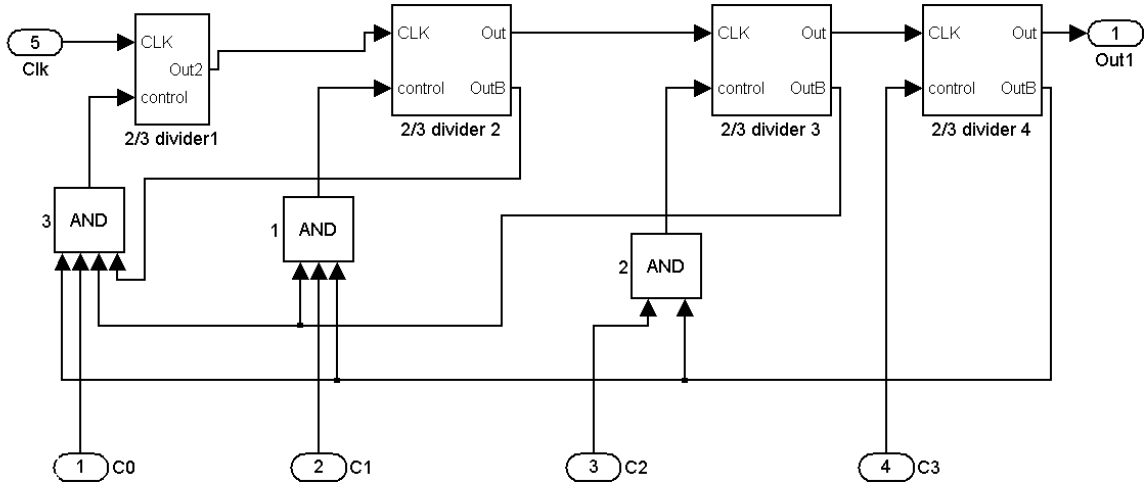


Figure 3.21: Four bit programmable frequency divider

3.3.6 Frequency Division Control Circuits Sigma Delta Modulators

Sigma delta modulators are being used to generate the control bits which determine the division ratio of dual modulus dividers, in frequency synthesis. To understand the effect of modulator, a system without a sigma delta modulator is examined. The division ratio, N+(1/64) can be obtained by dividing N+1 for 1 clock cycles and N for 63 clock cycles. For this division, spurious noise spectral characteristic is represented at Figure 3.22. Two peaks at Figure 3.22 are caused by the error which occurs when the frequency is divided by both N and N+1. This error is also known as quantization error.

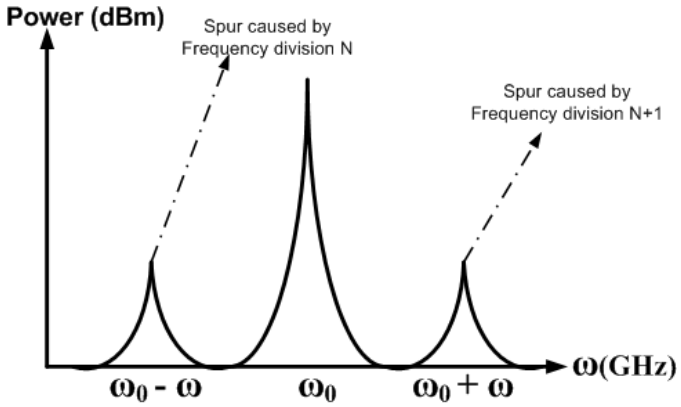


Figure 3.22: Noise spectral characteristic of a system without sigma-delta modulator as seen the peaks are sharp

On the other hand, if a sigma-delta modulator with 3 loops is used which will be examined later and for 128 cycles which we expect to see 2 cycles for N+1 divisor value, the division ratios will be like at Figure 3.23, total of the division ratios is represented at Figure 3.24. Final spurious noise spectral characteristic of the system after reshaping of the noise is represented at Figure 3.25.

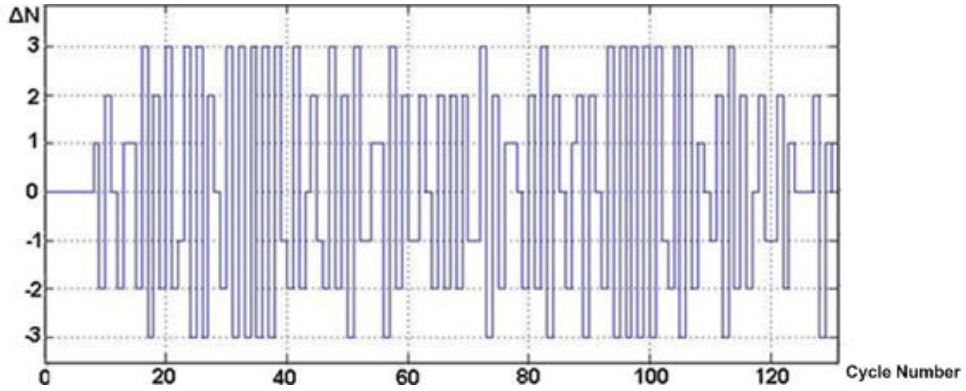


Figure 3.23: Instantaneous divisor ratio for sigma-delta modulator (Mash 1-1-1). Frequency division varies between +3 and -3. Frequency division is randomized and with this quantization noise is shifted to higher frequencies

From Figure 3.24, it can be seen that the total change at division ratio is 2 which can also be get by an accumulator. The main idea is using more than two division ratios to randomize the quantization which make the peaks at noise spectrum smaller and shift the quantization error to high frequencies by the loop filter of PLL.

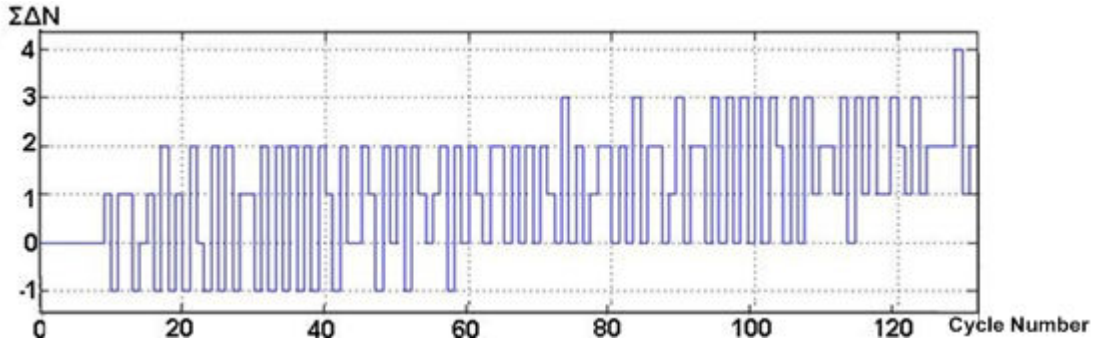


Figure 3.24: Total change in division ratio for second order sigma delta modulator. Frequency division changes but in long range period like 120 clock cycles, total division is the same as the system with first order SDM.

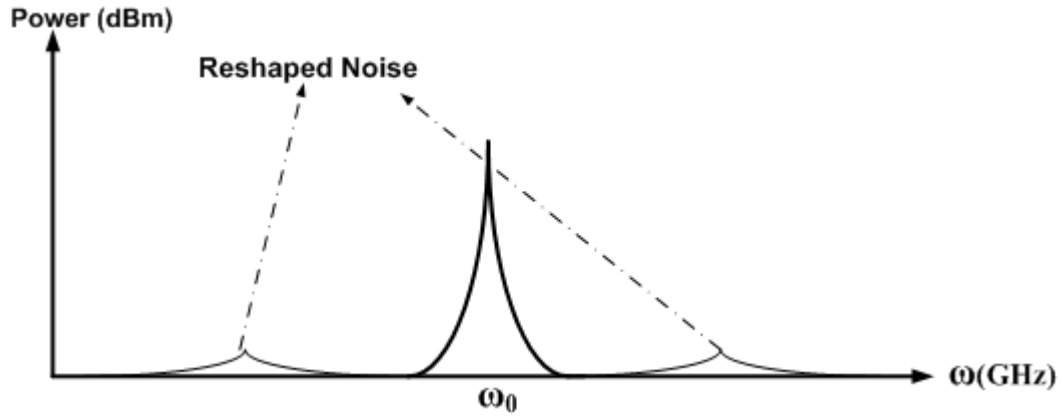


Figure 3.25: Spurious noise spectral characteristic of a system with sigma-delta modulator. As increase of change at division value, spurs in a wider frequency range frequencies are generated, but the magnitude of spurs are decreased, thus spurs are randomized.

3.3.6.1 First, Second and Higher Order Sigma-Delta Modulators

In first order ΣΔ-modulator, the input number is added to the number at register for every clock. If the adder and register have k bits (for example 5 bits), the accumulator gives a carry output for K times in 2^k cycle (for the example above K=1, so the accumulator gives carry for one times in thirty two cycles), the circuit model is shown at Figure 3.26, the Simulink® model is shown at Figure 3.27 with z domain representation.

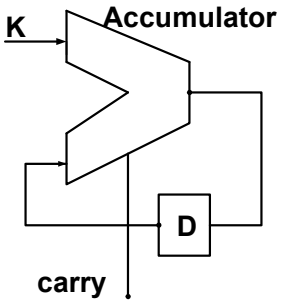


Figure 3.26: first order sigma-delta modulator

According to the z domain model at Figure 3.27, [28],

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z) \quad (3.9)$$

It is obvious that quantization error (E(z)) is suppressed at low frequencies with $(1 - z^{-1})$ and shifted to high frequencies that can be filtered by the Loop filter of PLL. The noise spectral density, $N_1(f)$, [28]

$$N_1(f) = E(z)(1 - z^{-1}) = E(f)\,|1 - e^{-j2\pi fT}| = 2e_{rms}\sqrt{2T}\sin(\pi fT) \quad (3.10)$$

Noise power in the signal and Noise magnitudes are, [28]

$$n_0^2 = \int_0^{f_0} |N_1(f)|^2\, df \approx e_{rms}^2 \frac{\pi^2}{3}(2fT)^3 \quad (3.11)$$

$$n_0 = e_{rms}\frac{\pi}{\sqrt{3}}(2fT)^{3/2} = e_{rms}\frac{\pi}{\sqrt{3}}(OSR)^{-3/2} \quad (3.12)$$

This means each doubling the oversampling ratio the quantization noise decreases by 9dB, [28].

In Figure 3.28, the second order $\Sigma\Delta$ modulator is shown. For this model transfer function is generated as [28],

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})^2 E(z) \quad (3.13)$$

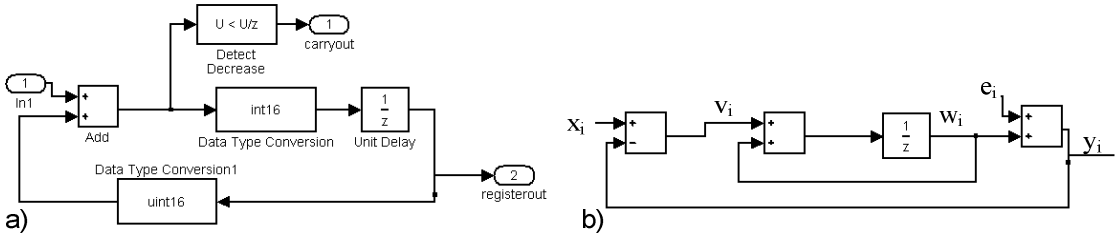


Figure 3.27: a) Simulink® model of first order sigma-delta modulator b) z domain representation

Where, $(1-z^{-1})^2$ component makes transfer function sharper high pass filter than first order SDM. Noise spectral density and noise powers are, [28]

$$N_2(f) = E(z)(1-z^{-1})^2 = E(f)\,|1-e^{-j2\pi fT}\,|^2 = 4e_{rms}\sqrt{2T}\sin^2(\pi fT) \quad (3.14)$$

$$n_0 = e_{rms}\frac{\pi}{\sqrt{5}}(2fT)^{5/2} = e_{rms}\frac{\pi^2}{\sqrt{5}}(OSR)^{-5/2} \quad (3.15)$$

For this topology if we double oversampling ratio, noise is lowered by 15dB, [28].

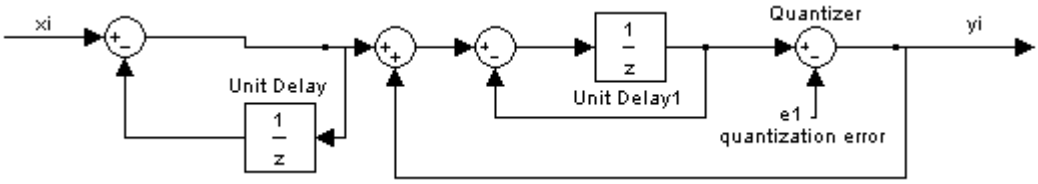


Figure 3.28: second order sigma-delta modulator

For n'th order ΣΔ modulators, which is at represented at Figure 3.29, the output at z domain, noise spectral density and noise magnitude are, [28]

$$Y(z) = z^{-1}X(z) + (1-z^{-1})^n E(z) \quad (3.16)$$

$$N_n(f) = E(z)(1-z^{-1})^n = E(f)\,|1-e^{-j2\pi fT}\,|^n = e_{rms}\sqrt{2T}\,|\,2\sin(\pi fT)\,|^n \quad (3.17)$$

$$n_0 = e_{rms}\frac{\pi^n}{\sqrt{2n+1}}(2fT)^{(n+1/2)} = e_{rms}\frac{\pi^n}{\sqrt{2n+1}}(OSR)^{-1*(n+1/2)} \quad (3.18)$$

If noise spectral densities and noise magnitudes of first second and third order sigma delta modulators are compared, it can be said that higher order ΣΔ modulators are more successful at shifting quantization noise to high frequencies and decreasing phase noise, [28].

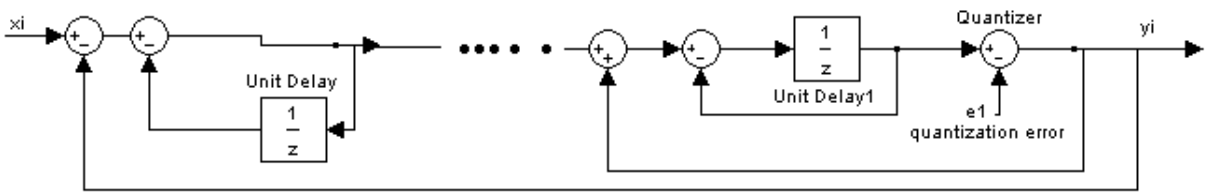


Figure 3.29: high order sigma delta modulator

3.3.6.2 ΣΔ Modulator Topologies

3.3.6.2.1 Mash 1-1-1 Modulator

One of the most popular ΣΔ modulator topology is Mash 1-1-1. In this topology three first order modulators are cascade connected as can be seen from Figure 3.30. ".F(z)" is the control of ΣΔ modulator, which comes as input of n bit adder which gives out an n+1 bit output. According to the Figure 3.30, the most significant bit of the output can be counted as an carry out (C_1), rest of the bits are counted as quantization error and these are two outputs of quantizer. Quantization error of first block is input of the register which produces the second input of the first adder that we discussed above. Second block takes the quantization error as its input. This block accumulates quantization error of first block while generating second carry out (C_2). Quantization error of second block is accumulated and third carry out (C_3) is generated at last block. While C_3 is saved, the difference between present C_3 and old value of C_3 is added to C_2, which can be assigned as $C_{Sub\text{-}total}$. While $C_{Sub\text{-}total}$ is saved, the difference between present $C_{Sub\text{-}total}$ and previous $C_{Sub\text{-}total}$ is added to C_1, which will be the output of ΣΔ modulator. To summarize z domain transfer function is, [28]

$$C_1(z) = .F(z) + (1 - z^{-1})^3 E_{q3}(z) \tag{3.19}$$

1 bit quantization error power is $1/\Delta^2$ for quantization step size $\Delta=1$. Frequency noise is, [28]

$$S_{\Omega}(z) = \frac{|(1 - z^{-1})^3 f_r|^2}{12 f_r} = \frac{1}{12}(1 - z^{-1})^6 f_r \tag{3.20}$$

Where f_r is sampling frequency which corresponds reference frequency of PLL, for third order Mash ΣΔ modulator. The phase noise can be found in some arrangements as, [28]

$$\frac{\varphi^2_{\Sigma\Delta}(f)}{2} = \frac{(2\pi)^2}{24 f_r}[2\sin(\frac{2\pi f}{f_r})]^4 \ \& \ PN(f) = 10\log\{\frac{(2\pi)^2}{24 f_r}[2\sin(\frac{\pi f}{f_r})]^4\} \tag{3.21}$$

Where, f is offset frequency and f_r is sampling frequency.

On the other hand for third order Mash ΣΔ modulator, the loop bandwidth is upper limited as, [28]

$$f_c < \frac{f_r}{2\pi}[\frac{f_r}{8\pi^2} A_n (2n+1)]^{\frac{1}{4}} \tag{3.22}$$

Where f_r is sampling frequency of ΣΔ modulator, A_n is in-band phase noise. In practice maximal loop bandwidth for a single-loop, multibit ΣΔ modulator should be smaller than 25% of the value calculated above [28].

For instance, if the in-band phase noise A_n is -100dBc/Hz, the above equation estimates the maximal loop bandwidth as 1.3217 MHz for a third order ΣΔ modulator with f_r = 50MHz. In practice maximal loop bandwidth of f_r <330 kHz should be chosen. As stated before, loop bandwidth is set to 267 kHz for this design.

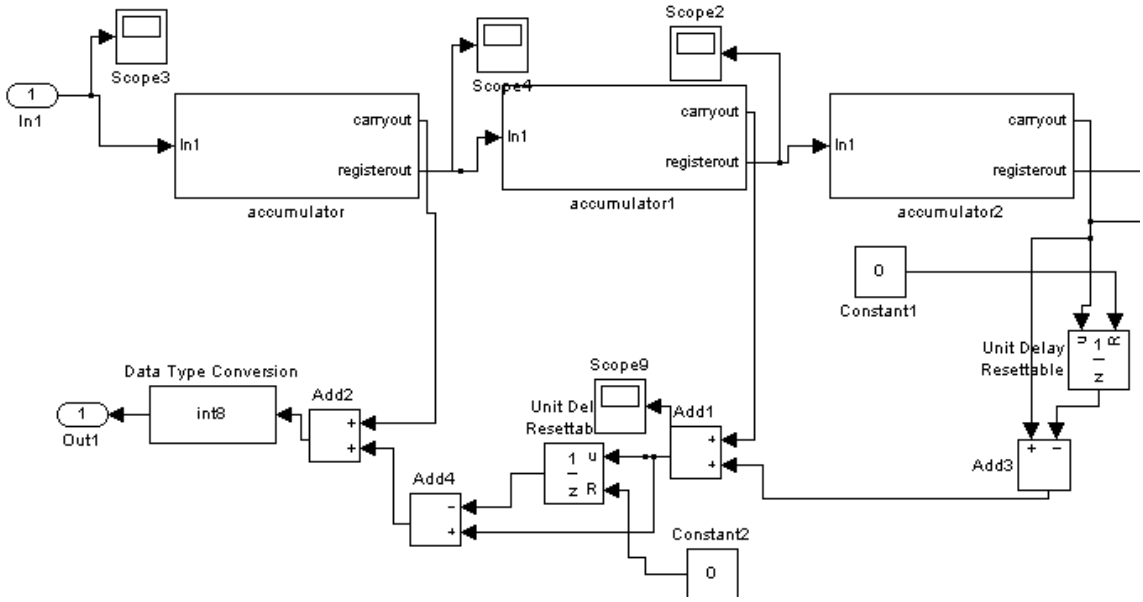


Figure 3.30: Mash 1-1-1 Simulink® Model

However, the Mash 1-1-1 modulator has three bit ΔN output (which varies from -4 to +3). If we use fixed dividers and programmable dividers, the divisor ratio will have big variations. For instance: if the PLL system which has 50MHz reference clock, and programmable divider with a fixed divider which divides frequency by 4, proposes to 5GHz, the difference between division values from -4 to +3 corresponds to frequency range from -800MHz to 600MHz. This trend of PLL causes large frequency step at feedback input of phase detector which is much higher than acquisition range. Thus, stabilization cannot be achieved.

3.3.6.2.2 Mash 1-1 Modulator:

In this topology two first order modulators are cascade connected as can be seen at Figure 3.31 . This type of modulator has a quantization error shape as, [28]

$$Y(z) = z^{-1}X(z) + (1-z^{-1})^2 E(z) \qquad (3.23)$$

Both quantization error and noise behaviors are worse than Mash 1-1-1 structure. However, it is easier to implement in Simulink® and does not degrade stability as Mash 1-1-1 because the output of Mash1-1 varies from -1 to +2. The outputs of Mash1-1 are at Figure 3.32 and Figure 3.33.

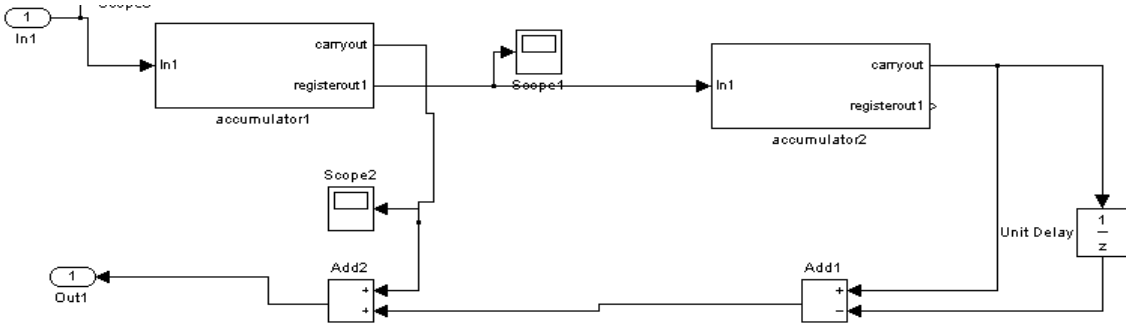


Figure 3.31: Mash 1-1 Simulink® model

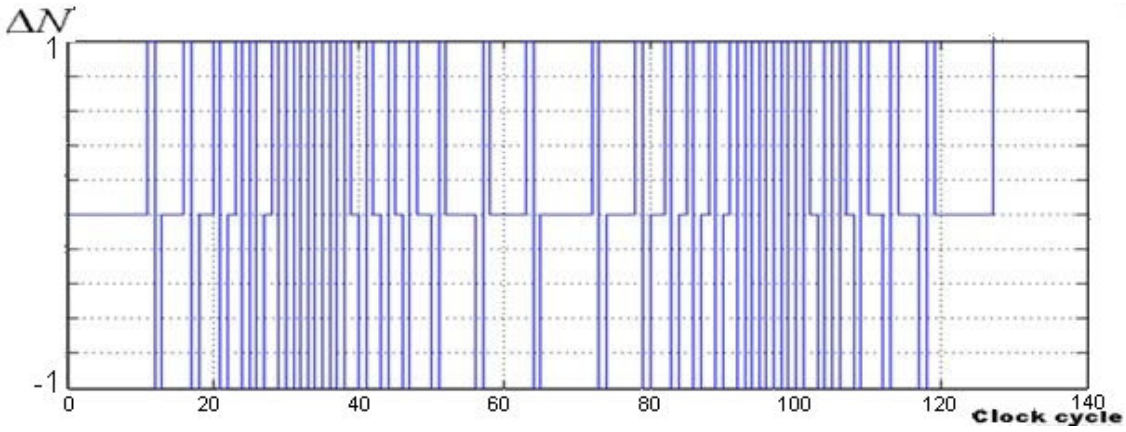


Figure 3.32: Instantaneous divisor ratio for sigma-delta modulator(Mash 1-1)

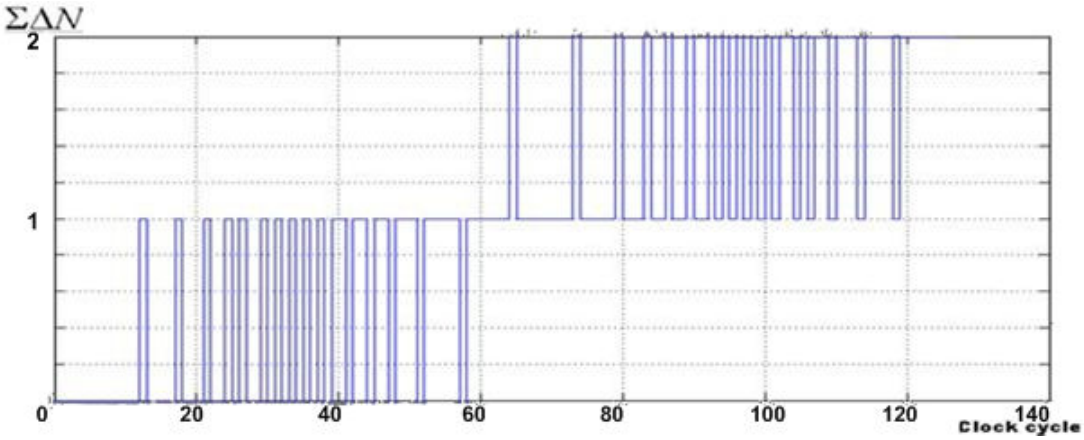


Figure 3.33: Total change in division ratio

3.3.7 Accumulator & Dual Modulus Divider

Before start of complete system simulations, simulations of small combinations are done. In Figure 3.34 the combination of dualmodulus divider and accumulator is represented. The output of combination in time domain is represented in Figure 3.35, in frequency domain is represented in Figure 3.36. The divider and accumulator are built in 8bits for this topology. From this combination, the divide value, N, is expected to be, [28]:

$$N = 8 + \frac{constant}{256} \qquad (3.24)$$

It is possible to calculate average divisor value at MATLAB, by using command lines at Appendix A2:

Output of this code is : F_{out} = 8.4447e+006 Hz.

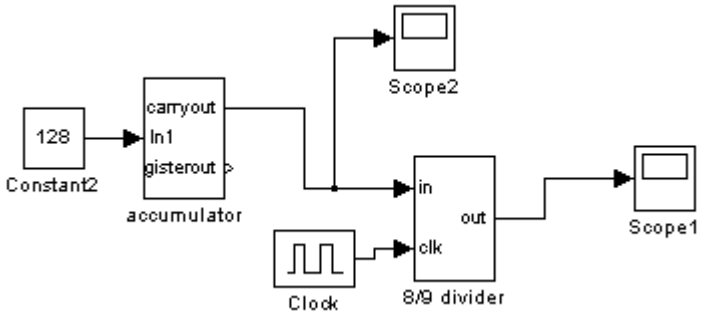


Figure 3.34: combination of dualmodulus divider and accumulator

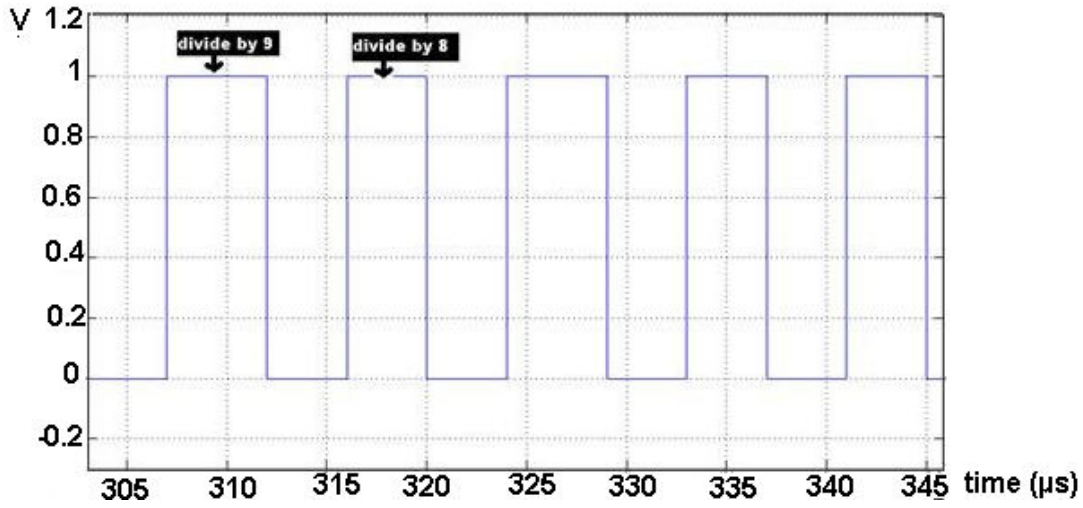


Figure 3.35: Output of combination in time domain, division value changes from 8 to 9 consecutively

The constant value at Figure 3.34 is 128, so the expected divisor value is 8.5. This error comes because the simulation time is not common power of divider values. In general PLL settling period it is impossible to have enough time to divide perfect 8's and perfect 9's.

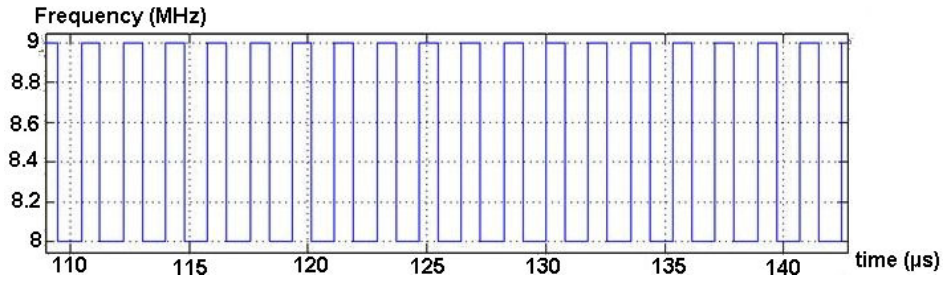


Figure 3.36: Output of combination in frequency domain a 72MHz clock is divided by 8 and 9 consecutively

3.3.8 System level simulation of PLL at Matlab

Simulink® block diagram is represented at Figure 3.37. At this figure, two divide-by-two circuits are used as divide-by-four circuit and 4 bit (16 to 31) programmable divider is attached to this block. Division ratio of the programmable divider is controlled by ΣΔ modulator (SDM), while using a data conversion system to convert integer output data of the SDM to binary input data of the programmable divider. Single tone frequency estimator block of Simulink® is used to examine the output of the system at frequency domain.

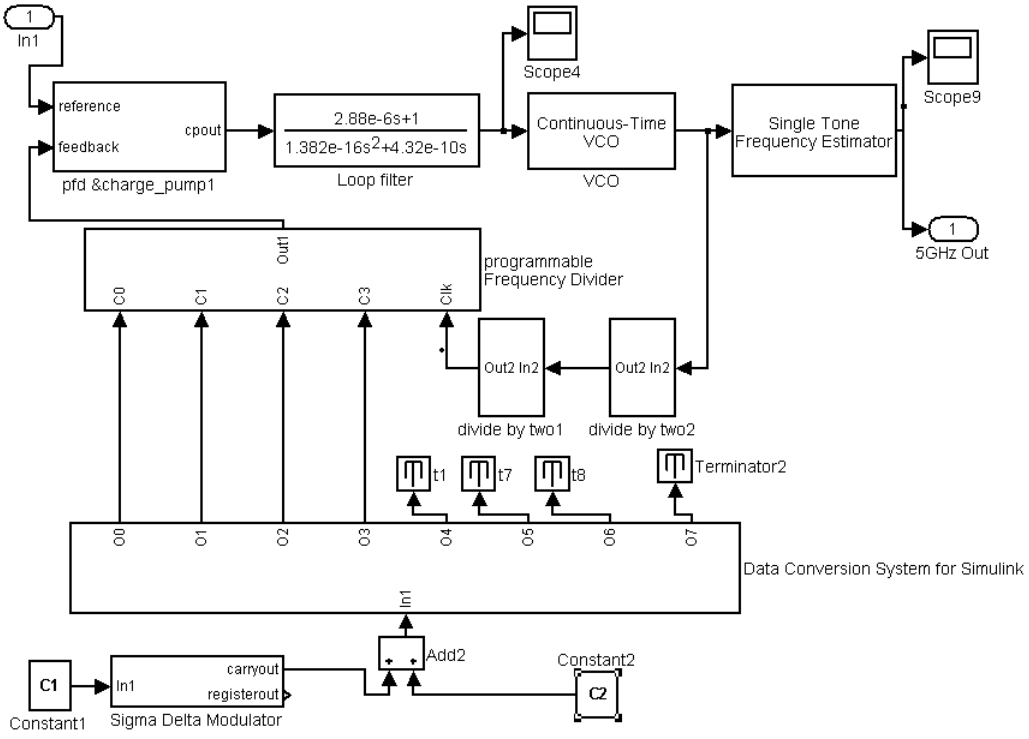


Figure 3.37: Simulink® model of ΣΔ-Fractional N PLL

Final division ratio can be calculated as:

$$N = \left((C2 + 16) + \frac{C1}{256} \right) * 4 \tag{3.25}$$

where constant C1 determines fractional division ratio, C2 corresponds division control input four bits frequency divider.

From (3.26) output frequency can be calculated as:

$$F_{out} = \left(\left((C2 + 16) + \frac{C1}{256} \right) * 4 \right) * F_{reference} \tag{3.26}$$

If C1 is set to zero, the system acts like integer N PLL. Reference clock frequency is set to 50 MHz, and if we set C2 to 8, output frequency of PLL is expected to be 4.8GHz. Output of PLL at frequency domain is represented at Figure 3.38. According to this figure, the settling time of the system is 10μs, as expected from the step response of the system shown at Figure 3.8 and hand calculations. This figure is important because of showing stability of the system and settling behavior. If we zoom to output frequency after settling achieved is also can be seen from this figure, we can see that final frequency error magnitude is 1 kHz, which is sufficiently small.

For another instance if C1 is set to 115, the system acts like fractional N PLL and the output frequency of PLL is expected to be 5.0898GHz. If first order sigma delta modulator is used, which is made up of a single accumulator, the output of the system is represented at Figure 3.39. In this figure, output frequency is settled to 5.09GHz with a frequency error which has around 14 MHz magnitudes. On the other hand, 50MHz magnitude peaks are located. Settling time is around 10μS.

For the same conditions if second order ΣΔ modulator is used, the output of the system is represented at Figure 3.40. According to Figure 3.40, output frequency of the system is settled to around 5.09GHz with a frequency error which has 25MHz magnitude. This value is 1.8 times of the system with first order sigma delta modulator. On the other hand settling time did not change.

If third order sigma delta modulator is used, the output of the system is represented at Figure 3.41. According to Figure 3.41 output frequency of the system is settled around 5.1GHz with a frequency error which has an error magnitude more than 100MHz. Thus, settling is not achieved properly. To conclude despite decrease of quantization error and randomization of division ratios, the total phase error (frequency error) is increased.

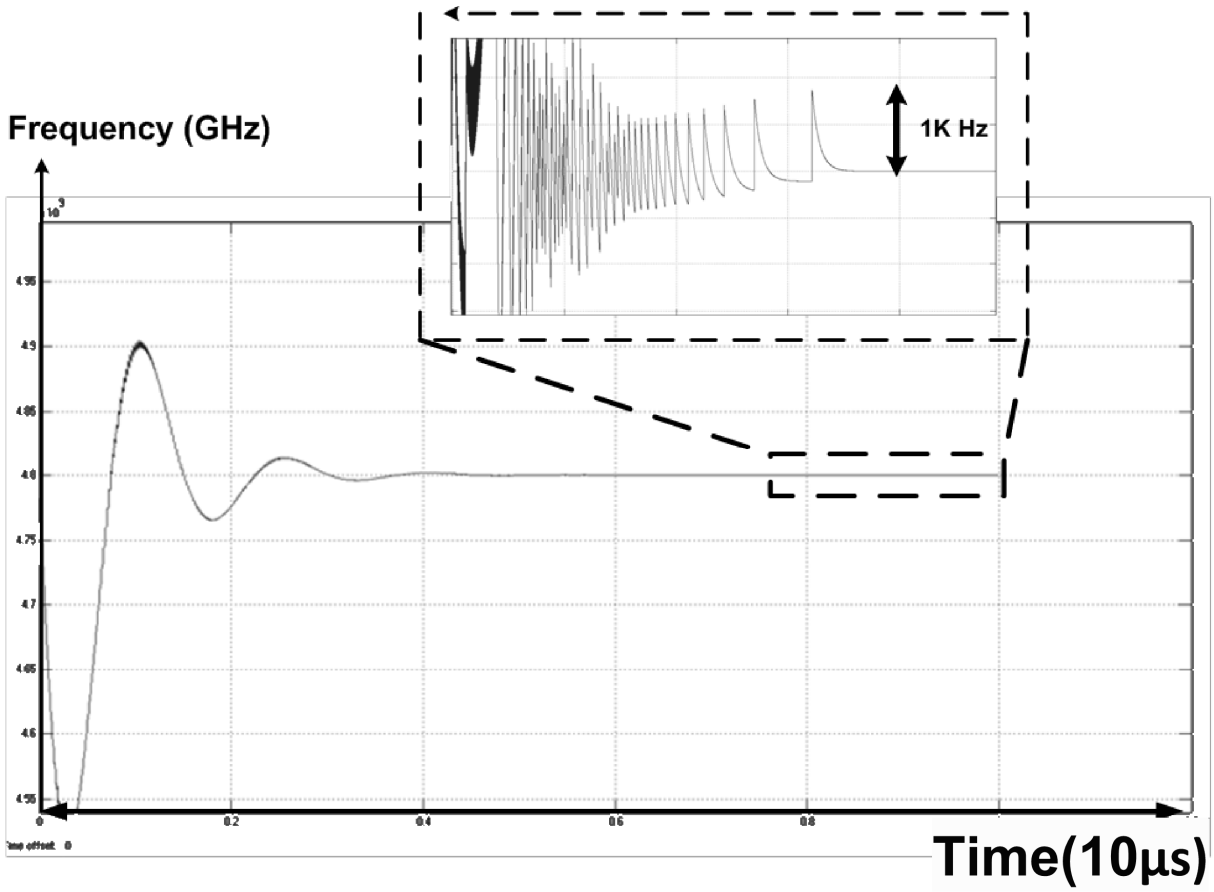


Figure 3.38: Output of System at frequency domain for integer N mode. Frequency error magnitude is less than 1KHz after 10µs.

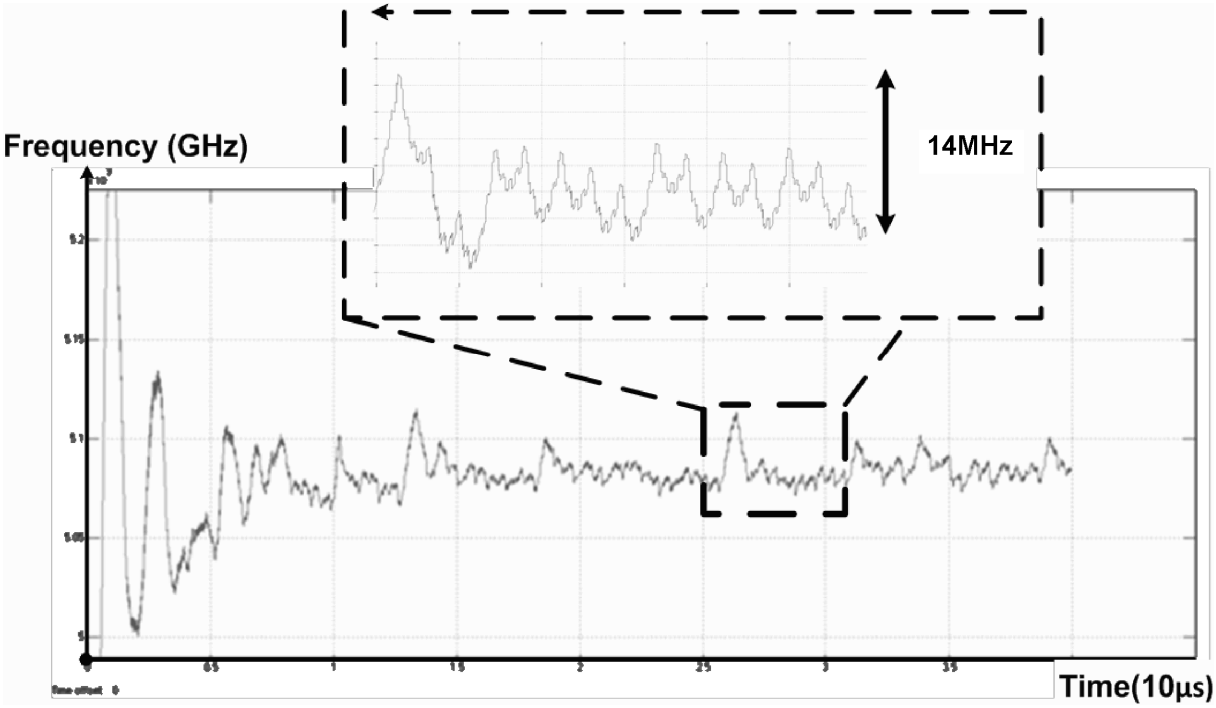


Figure 3.39: Output of the system with first order sigma delta modulator. Settling time is around 10µs, Frequency error magnitude is 14MHz.

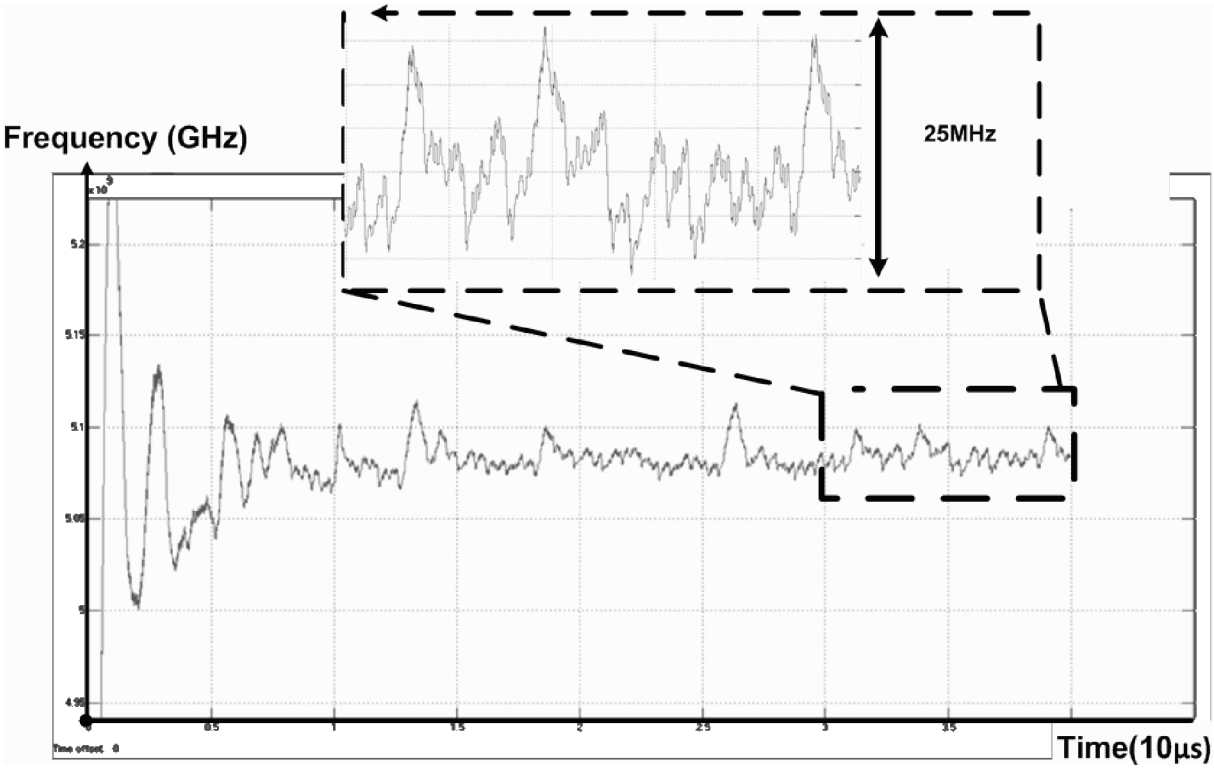


Figure 3.40: Output of the system with Second order sigma delta modulator. Settling time is around 10µs, Frequency error magnitude is 14MHz

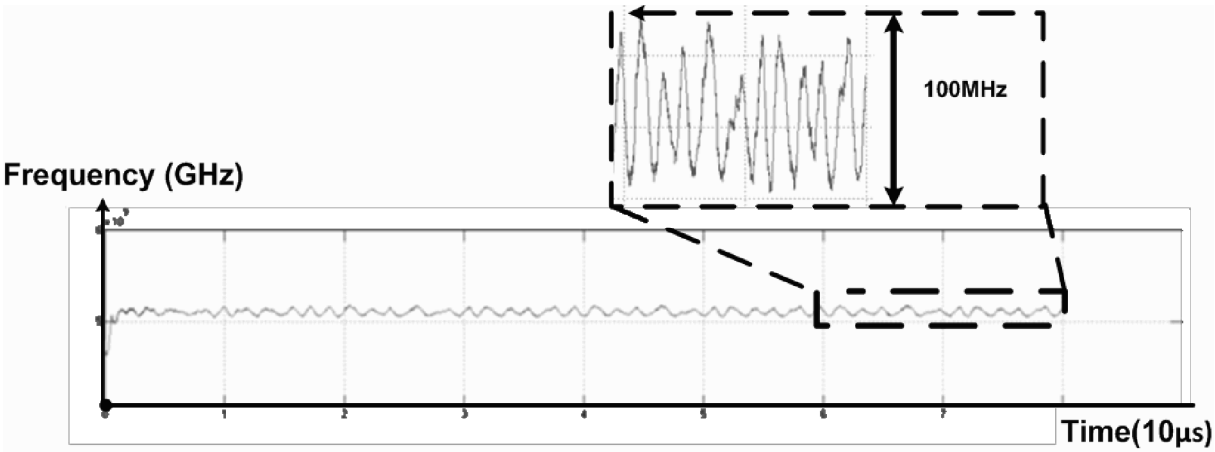


Figure 3.41: Output of the system with Third order order sigma delta modulator. Error magnitude is around 100MHz, settling is not achieved

Finally, if it was possible to design programmable divider which can work at 6GHz, frequency variations of output of the first order system after settling time would be at Figure 3.42. According to this figure, magnitude of these variations reduced to 0.8MHz. Operating frequency of programmable divider has highest significance because of its effect over frequency variations, accuracy and spectral purity.

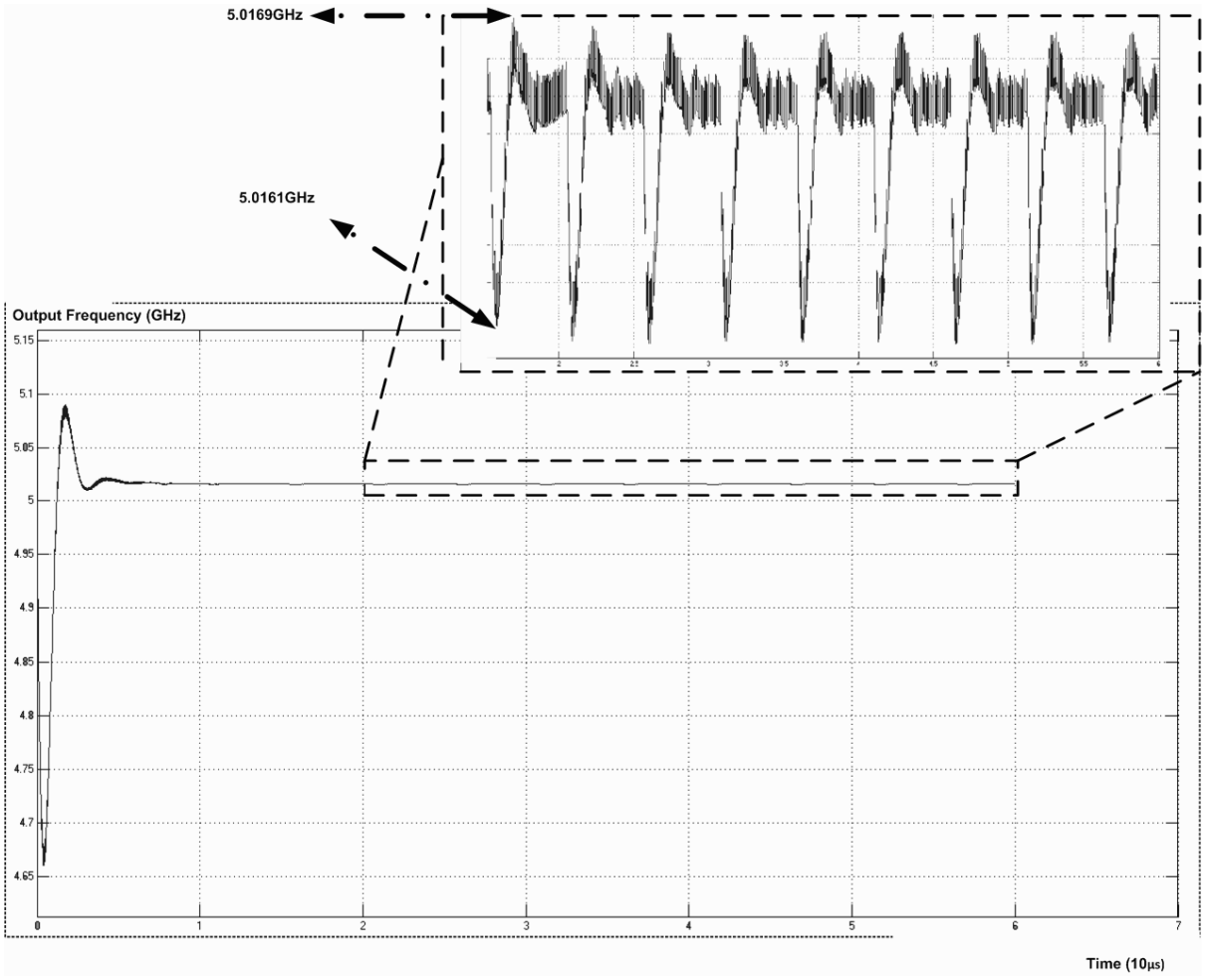


Figure 3.42: Fully programmable Frequency divider output for first order sigma delta modulator

4. DESIGN OF LOOP COMPONENTS

4.1 Charge Pump Circuit

Ideal operating principle of the circuit is explained at section 3.3.2 via the simplified circuit which is given at Figure 3.14. The current sources at this figure is can be designed by MOS current mirrors. Using cascode technique at design increases output resistance which will be important to have stabile current despite varying control voltage of VCO. MOSFETs can also be used for the “U” and “D” switches which can be added to gates or sources or drains of current mirrors.

The switch at source side would make VDS voltage varying which changes VGS of the current mirror. Varying VGS voltage makes current unstable. Thus, this option is not useful.

On the other hand, the switches at gate side, which can be seen at, Figure 4.1, increases the settling time of current charge pump dramatically because of the delay which comes from the product of R_{on} resistance of the switch and C_{GS} capacitance. The output of gate switched charge pump is shown at Figure 4.2. This figure shows that, settling time of up circuit is more than 5ns to generate 6μA charge pump current. Because of its large settling time, despite small output current, this topology is not also useful.

The most popular circuits are drain switched circuits that have the least settling time and stabile output current. Basic drain switched charge pump circuit can be seen at Figure 4.3. According to this topology, when one of the switches is at cut off region, the drain of the transistor of current mirror at this switch’s side goes VDD or GND. After the switch is turned on, the drain voltage must rise or fall to the control voltage of VCO. That increases settling time and charge injection of charge pump. To solve this problem, a buffer can be added as Figure 4.4.

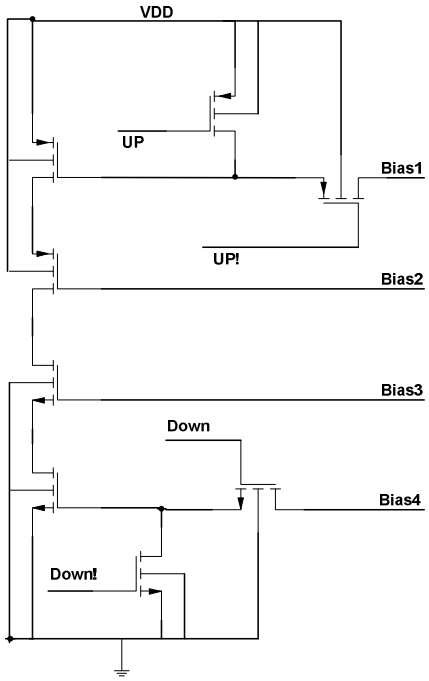


Figure 4.1: Gate switch based charge pump circuit

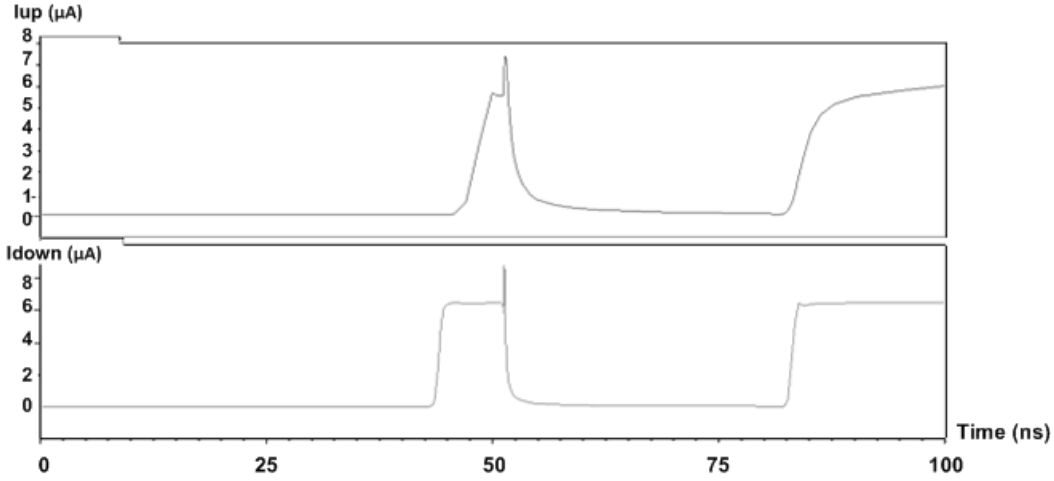


Figure 4.2: Output of gate switched charge pump, Up current needs more than 5ns to settle to 6 µA Charge pump current

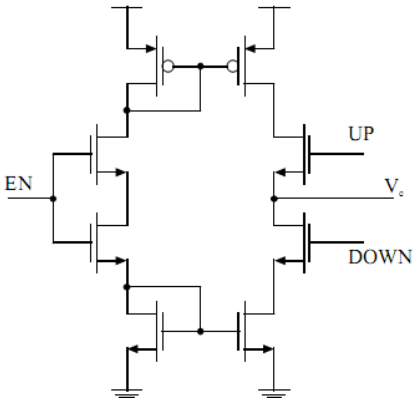


Figure 4.3:Basic Drain swiched charge pump topology [1]

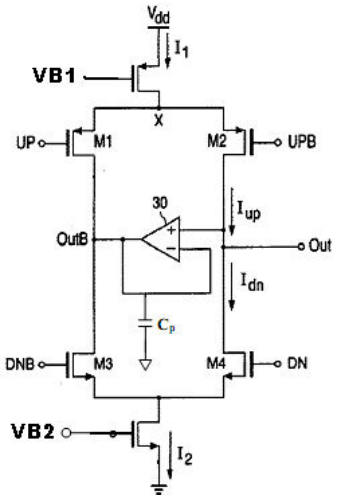


Figure 4.4: Basic current mirror circuit with buffer.[1]

First improvement is increasing output resistances. To have high output resistances, the current mirrors can be cascoded. To have high output swing, the bias circuits at [29] and [30] are used.

Secondly, to have fastest settling behavior with low glitches, the switch transistors must be at the smallest size. After comparing the performance of three switches, (NMOS switch, PMOS switch and transmission gate) the best performance is PMOS switches for up currents and NMOS switches for down currents. The simulation result window is at appendix B2.

Thirdly, the reference current is highly dependent on power supply and temperature, which is shown at Figure 4.5 and Figure 4.6. To solve this problem, band gap reference circuit, which can be found at [31], is used for reference currents and these are copied as up and down currents. The band gap reference circuit is shown at Figure 4.7.

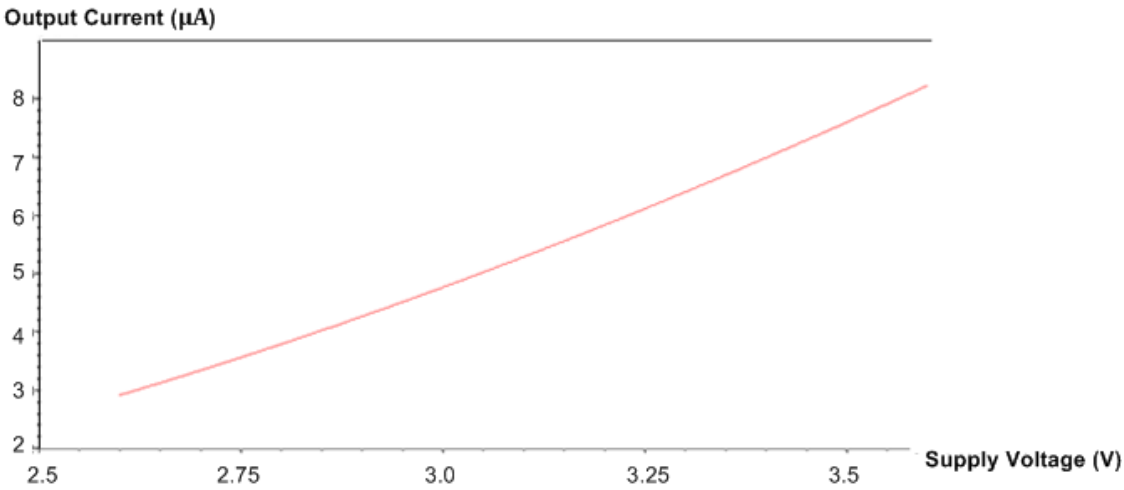


Figure 4.5: Output current vs power supply (without band gap reference circuit), Output current is dependent from power supply.

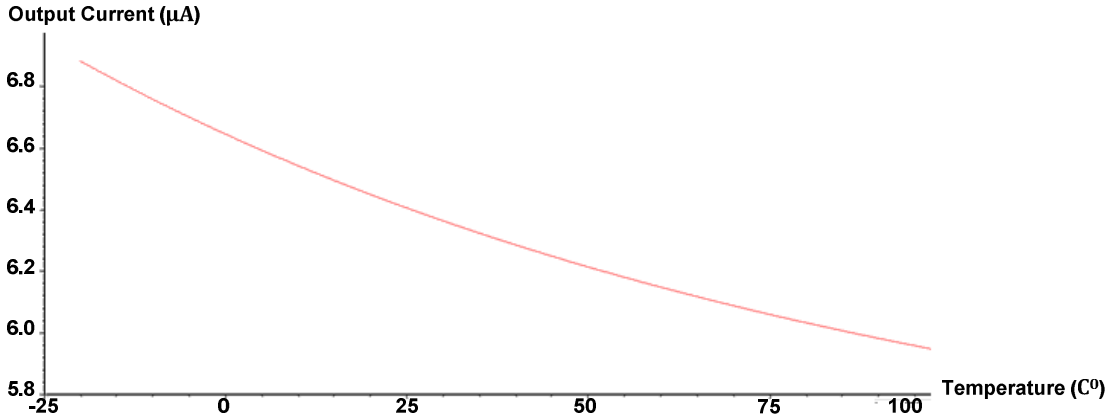


Figure 4.6: Output current vs temperature(without band gap reference circuit), Output current is inversely proportional to temperature

To obtain a faster charge pump, the capacitance at dummy node OutB (Figure 4.4) can be increased. Cp at this figure provides the charge that is needed to decrease the charge injection caused by parasitic capacitances at OutB node. The glitch on the output node of buffer is reduced by increasing this capacitance. If we add the effect of this capacitance, charge pump gain is derived as [32];

$$\frac{dQ}{dt_e}\Big|_{t_e \approx 0} = Ip\left(1 - \frac{C_{parasitics}}{C_P}\right) \qquad (4.1)$$

Output current with respect to temperature is at Figure 4.8, output current with respect to power supply is at Figure 4.9. Without band gap reference circuit, the change of supply voltage from 3Vto 3.6V results change in output current from 4.8uA to 8uA as can be seen from Figure 4.5.

According to Table 3-1, two different charge-pump values are needed. These values are achieved by switching two resistors at band gap reference circuit. On the other hand, because of the increase of current from 6uA to 104uA and 270uA, the width of the transistors which are used for switching are increased, thus, glitches at output current are also increased as it can be seen from Figure 4.15. After these changes, final version of band gap reference circuit is shown at Figure 4.10.

As shown at Figure 4.12 high output swing CMOS cascode current mirrors are used to decrease voltage headroom at output. Control voltage of VCO is connected to charge pump output, thus, this voltage is limited by output swing of the charge pump. According to Figure 4.12 and Figure 4.13, output swing of the charge pump is between 0.3V to 3V. This swing is achieved by using techniques described at [29] and [30]. The effect of band gap reference circuit can be seen from Figure 4.8 and Figure 4.9. Output current changes less than 0.25% with respect to change of power supply from 3V to 3.6V with charge pump circuit (without charge pump circuit this ratio

was more than 67%). In addition, output current change with respect to the change at temperature is much more linear, and proportional to temperature.

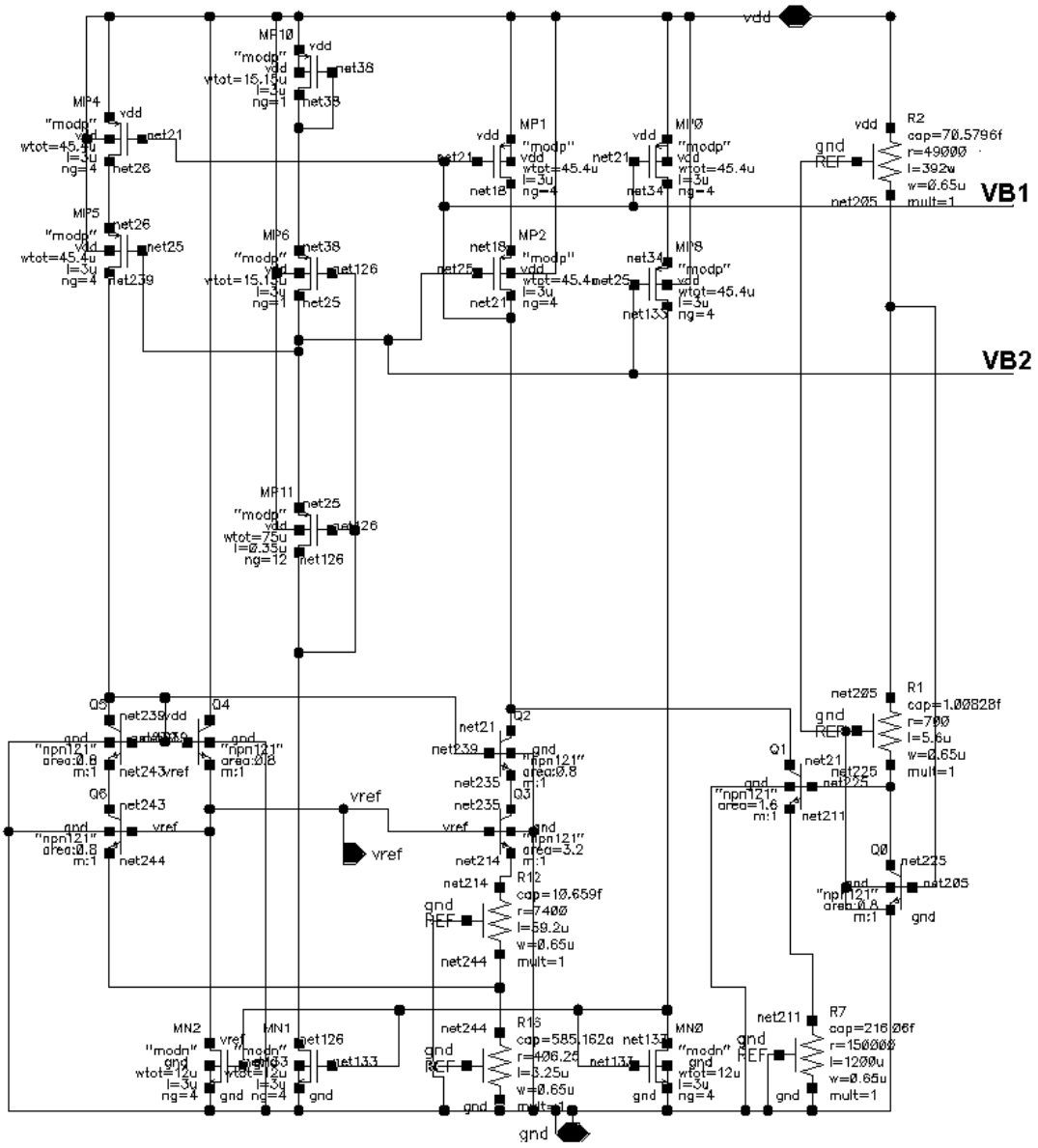


Figure 4.7: Band Gap reference Circuit

The schematic of the operation amplifier, which can be seen at Figure 4.11, is shown at Figure 4.14. At Design of this OPAMP (basically it is a miller OTA which is being used as OPAMP), rather than having high gain, low phase margin and low output resistance with high output swing is aimed. Although using buffer stages, such as common collector and common source topologies, at output of OPAMP can reduce output resistance, they are not used because of their limitation at output swing while relatively low supply voltage (3.3V) is being used. To decrease output resistance of this circuit, the current at output stage is selected sufficiently high and lengths of transistors are chosen at minimum to decrease r_o of transistors. At layout of input transistors, which is shown at Figure 4.16, common centroid technique is used to compensate

the effects of random defects at fabrication and achieve symmetry. Final area of the layout of OPAMP which is shown at is 36x44μm^2. Finally transient currents of the charge pump (for I_{cp1}) are shown at Figure 4.15. According to this figure, "up" and "down" currents match with an error less than 0.1 %. The transient currents for I_{CP2} are at appendix B2.

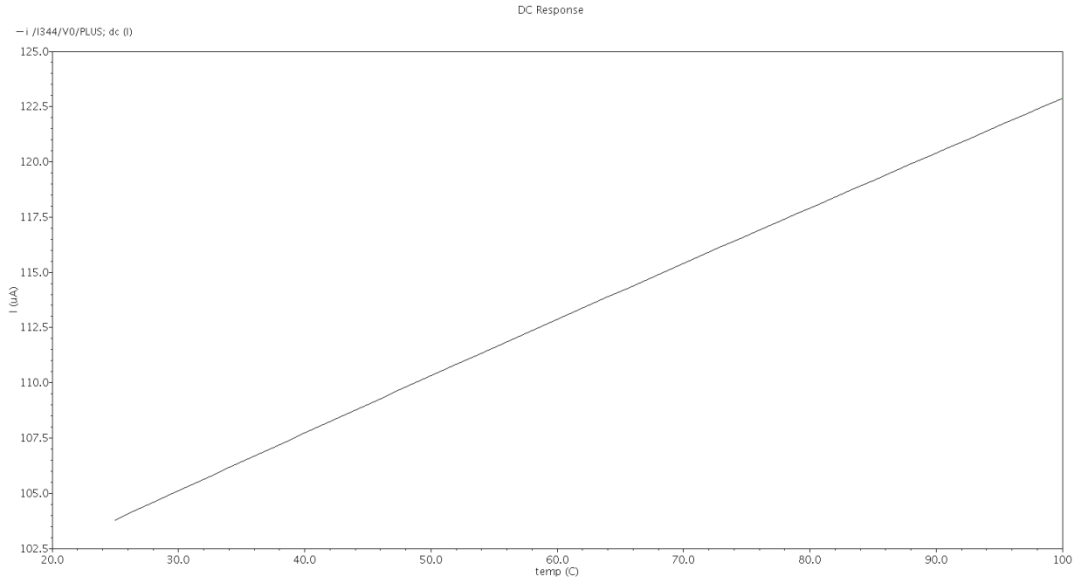


Figure 4.8: Output current of Final circuit vs temperature

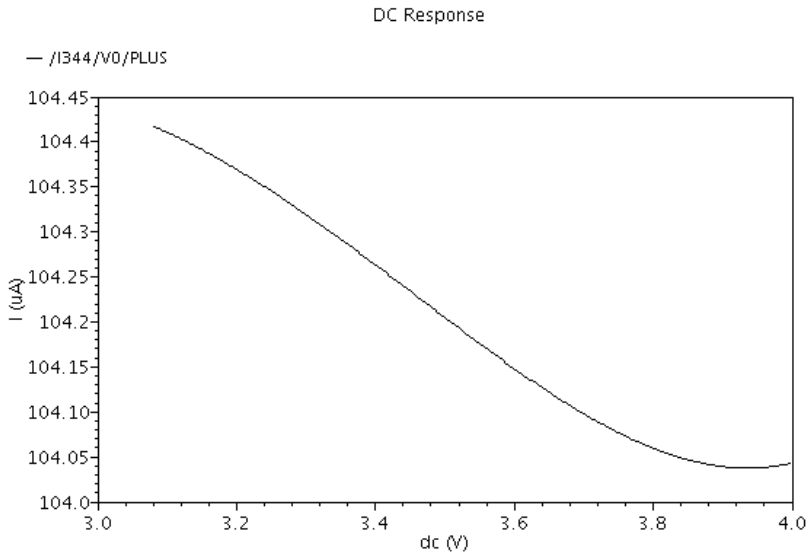
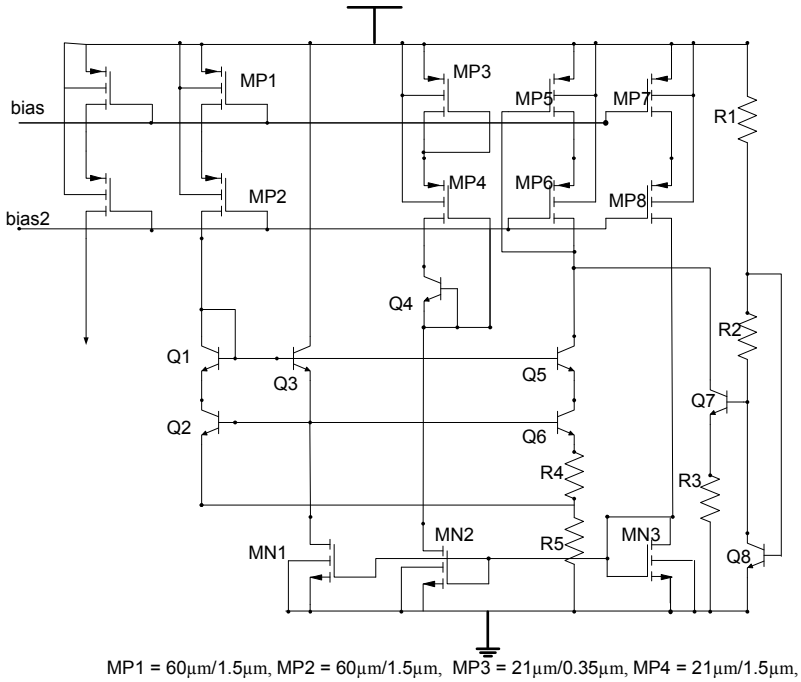


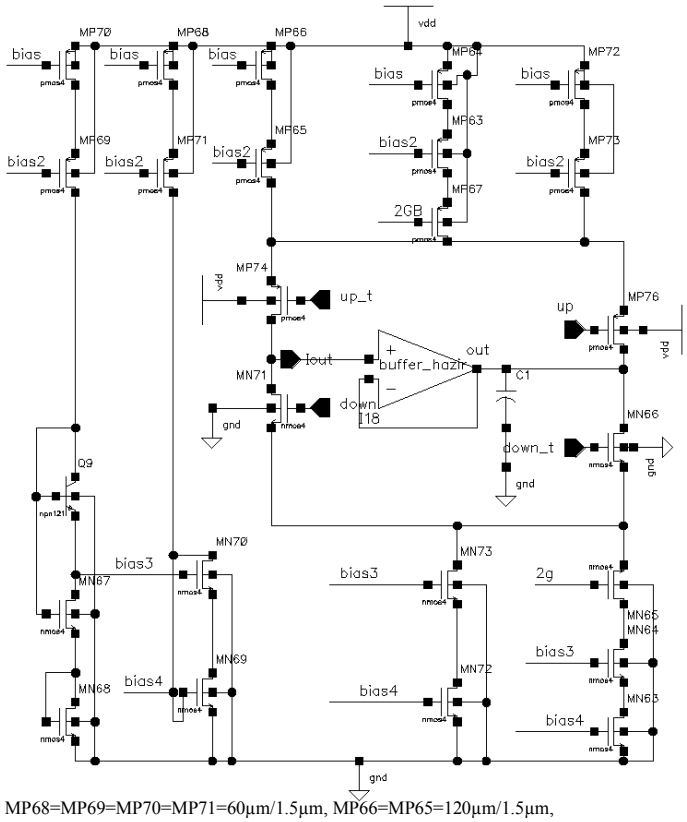
Figure 4.9: Output Current of Final circuit vs Power supply

The glitches at Figure 4.15 have both positive and negative values, to see the effect of these currents over control voltage of VCO, integration can be used. On the other hand, integration of the charge-pump currents, for the case that PLL is locked, is also important because it can cause long term jitter. These currents and integration is shown at Figure 4.18. According to this figure, this integration has values in the order of 10^{-21}, thus, current mismatch for this charge pump is sufficiently small.



MP1 = 60µm/1.5µm, MP2 = 60µm/1.5µm, MP3 = 21µm/0.35µm, MP4 = 21µm/1.5µm,
MP5 = 60µm/1.5µm, MP6 = 60µm/1.5µm, MP7 = 60µm/1.5µm, MP8 = 60µm/1.5µm,
MN1 = 18µm/1.5µm, MN2 = 18µm/1.5µm, MN3 = 18µm/1.5µm
R1 = 49k Ω, R2 = 700 Ω, R3 = 5kΩ, R4 = 931.25 Ω, R5 = 406.25 Ω,
Q1 = 0.8, Q2 = 0.8, Q3 = 0.8, Q4 = 1, Q5 = 0.8, Q6 = 3.2, Q7 = 1.6, Q8 = 0.8,

Figure 4.10: Final Band gap reference Circuit and PTAT current source



MP68=MP69=MP70=MP71=60µm/1.5µm, MP66=MP65=120µm/1.5µm,
MP72=MP73=60µm/1.5µm, MP67=80µm/0.35µm, MP76=MP74=80µm/0.35µm
MN67=MN68=10µm/1.5µm, MN63=MN64=MN72=MN73=36µm/1.5µm,
MN65=30µm/0.35, MN71=MN66=15µm/0.35µm

Figure 4.11: Final Charge Pump Circuit, this circuit is connected with Figure 4.10, via bias and bias2 nodes

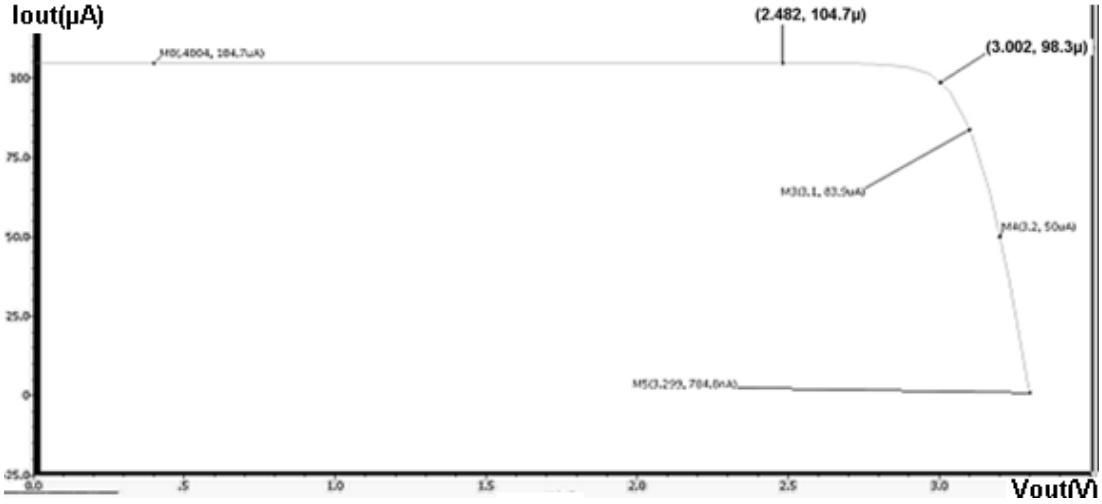


Figure 4.12: Charge pump up current vs output voltage. Output Current reduces form 104.7µA to 98.3 at 3V output Voltage

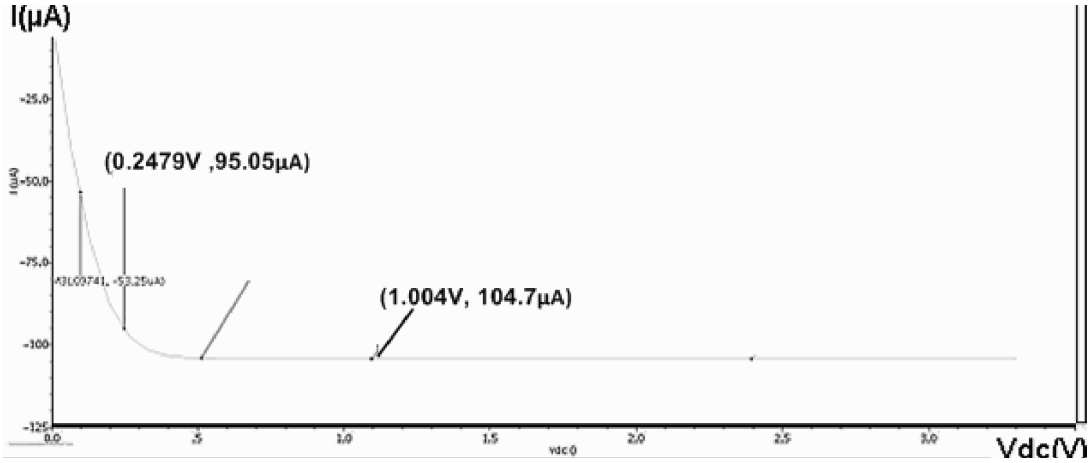


Figure 4.13: Charge pump down current vs output voltage

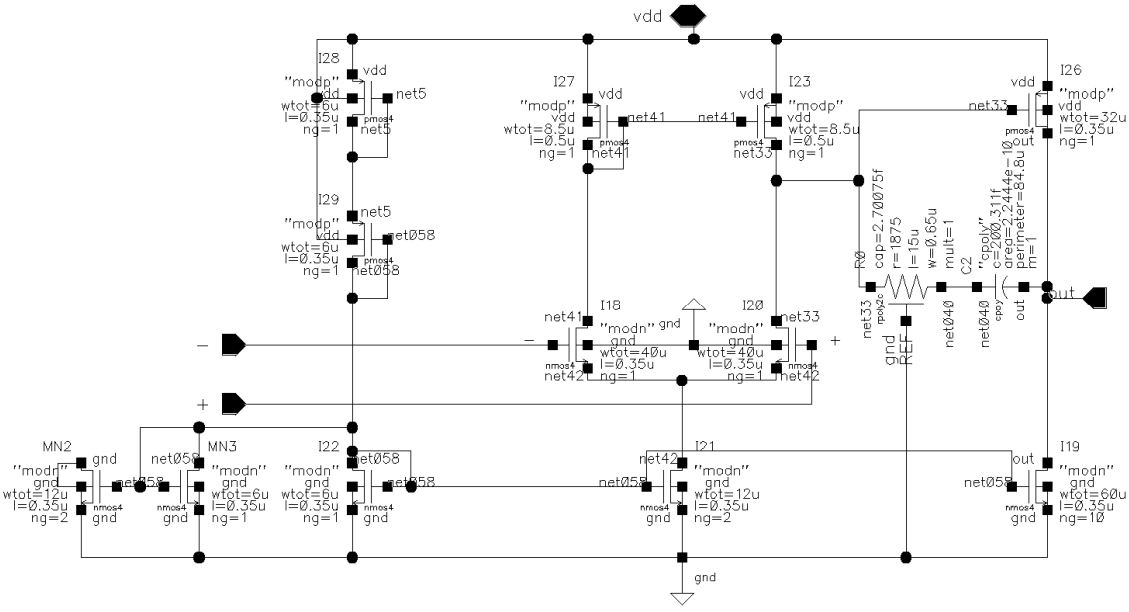


Figure 4.14: Schematic of Opamp, which is used at Charge pump

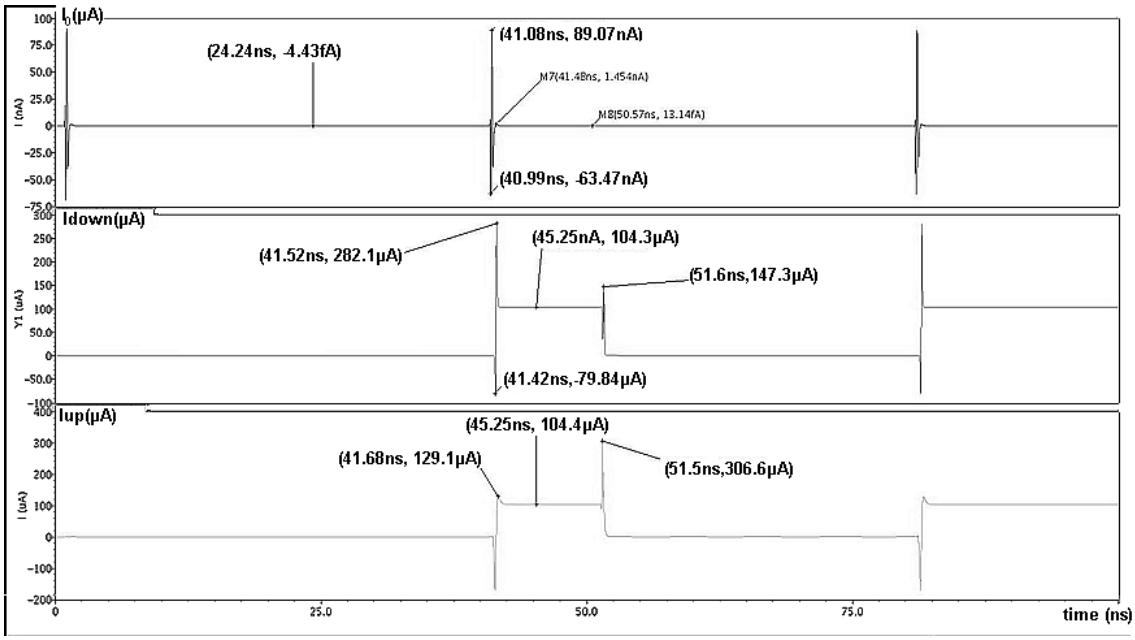


Figure 4.15: Transient charge pump currents: Up current is shown at south of the figure, Down current is shown at center of the figure and if the PLL locks, the noise current is shown at north of the figure.

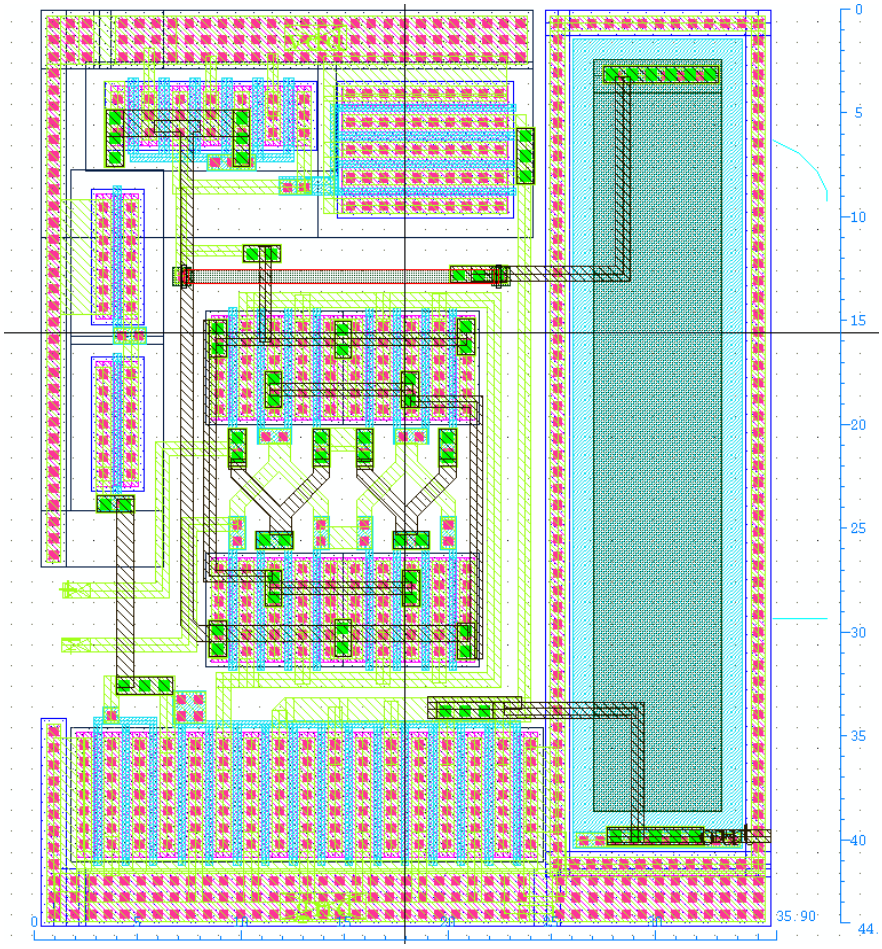


Figure 4.16: layout of the opamp used at chargepump

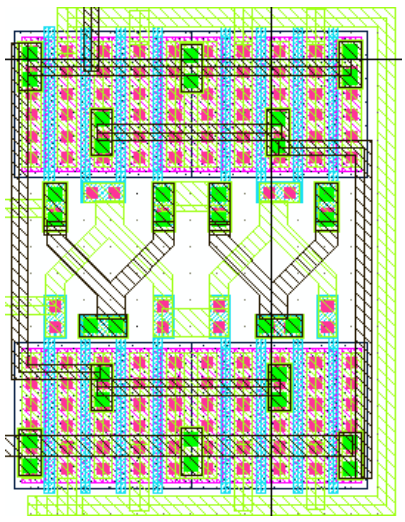


Figure 4.17: Layout of input transistors of Opamp

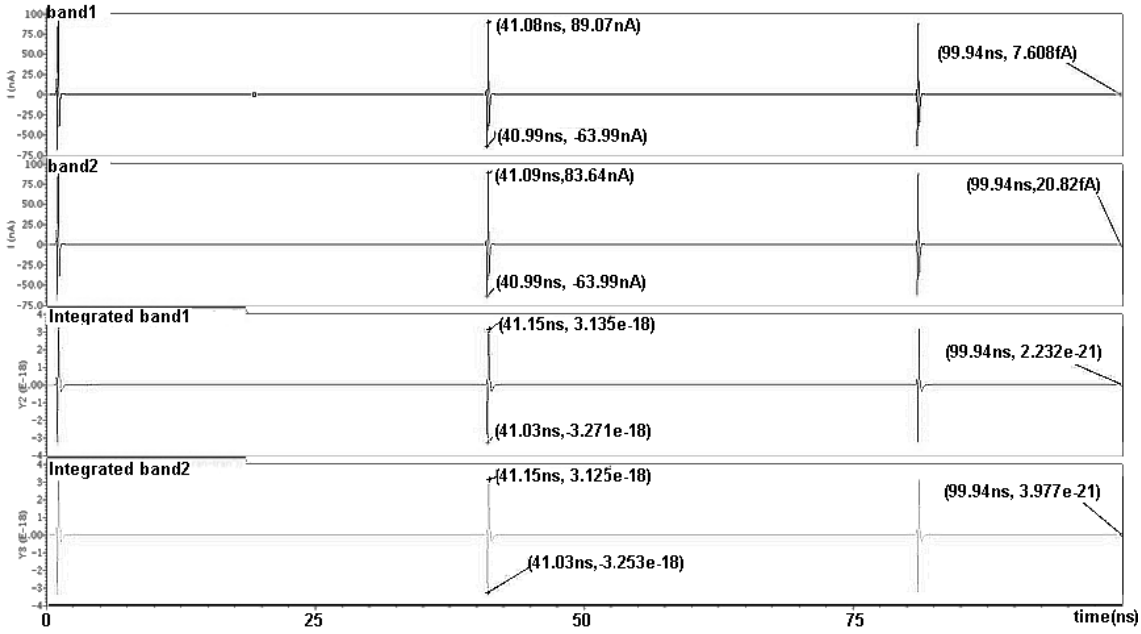


Figure 4.18: Charge pump currents for the case both up and down signals are applied and The definite integrals of these currents for the simulation range

Current Mismatch at Charge Pumps

Usually there is a minor difference (around 0.1%) between I1 and I2 of the circuit at Figure 2.2, which causes fluctuations at output voltage although two input frequencies of PFD are same. A finite phase error occurs at lock condition because PLL reacts to compensate this charge difference. Thus, spurs at output frequency spectrum (at $f_{out} \pm f_{ref}$) are generated as represented at Figure 4.19. $\pm f_{ref}$ comes, because the fluctuations at control voltage are at reference frequency.

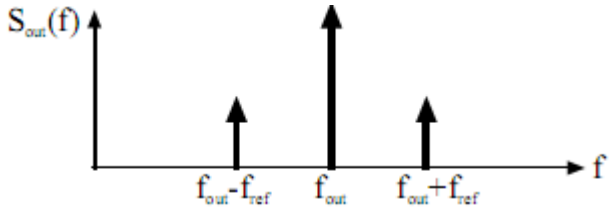


Figure 4.19: Spurs Caused by current mismatch

To calculate the phase error, the ratio of currents can be taken as

$$K = \frac{I_2}{I_1} \tag{4.2}$$

(Assuming I2>I1). If the phase detector represented at Figure 3.9 is used, during the T_e period total charge at loop filter increases proportional to I1 and decreases proportional I2-I1, during reset delay. For the lock condition total charge difference must be zero as represented at Figure 4.20. Thus, T_e (in seconds) can be calculated as [1]:

$$T_e = (K-1)t_R \tag{4.3}$$

Where t_R is the reset path delay. If symmetrical AND gate is used to have equal path delay, the amount of voltage ripple is given as [1]:

$$\Delta V_C = \frac{I_1}{C_p}(K-1)t_r \tag{4.4}$$

Control voltage variation and phase error caused by this variation are directly related with K. This phase error can be reduced by using an advanced phase detector topology which is explained at 4.2.

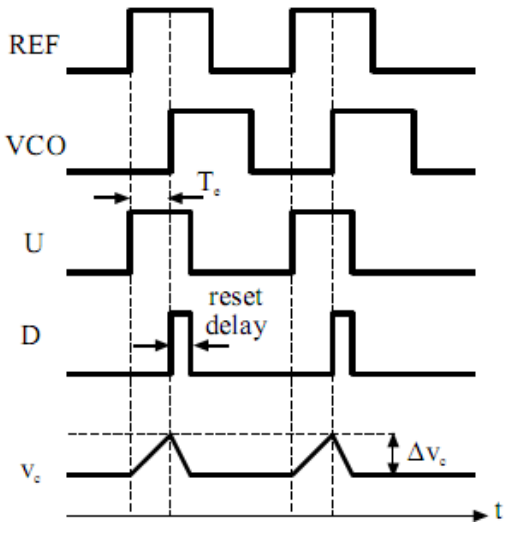


Figure 4.20: Current-mismatch problem in a charge-pump [1]

4.2 Design of Phase Frequency Detector

To compensate the problems of current mismatch, the circuit at Figure 3.11 is improved as represented at Figure 4.21. According to this figure, Up (or Down) of Figure 3.11 and $\overline{\text{Down}}$ (or $\overline{\text{Up}}$) of Figure 3.11 are the inputs of the AND gate which generates Up (or Down) of the circuit which is represented at Figure 4.21. With this improvement, time interval of both up and down signals are generated, is reduced to the AND gate delay time. In this design, AND gate is designed symmetrically.

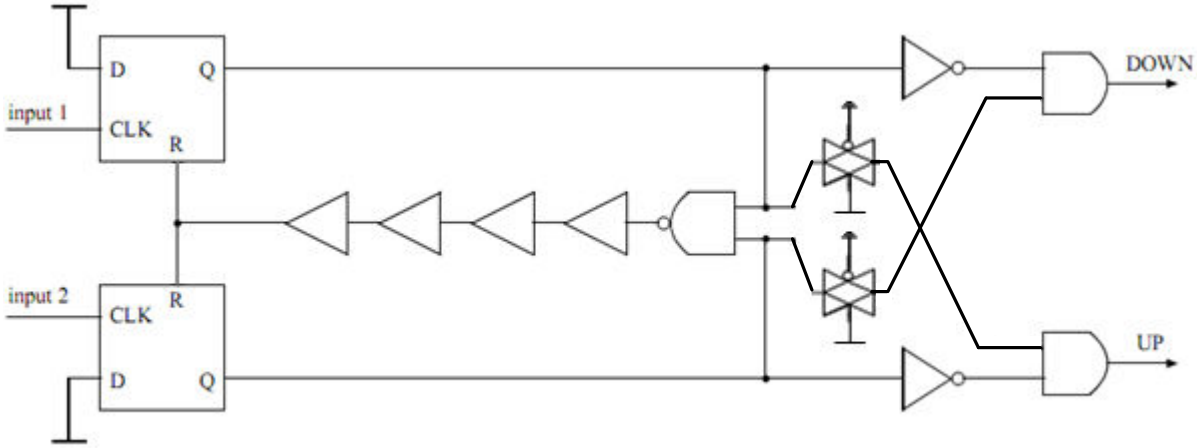


Figure 4.21: Modified phase-frequency detector

For this circuit, T_e, [1]:

$$T_e = \frac{(K-1)}{(K+1)} t_i \tag{4.5}$$

The delay at reset path is assigned as t_i. Fluctuation amplitude of control voltage is, [1]:

$$\Delta V_C = \frac{I_1}{C_p} \frac{(K-1)}{(K+1)} t_i \tag{4.6}$$

In comparison with (4.4) magnitude of the spurs which is represented at Figure 4.19 and phase-error are divided by, [1]:

$$\alpha = (K+1) \frac{t_r}{t_i} \tag{4.7}$$

Despite a huge current mismatch, none of UP and DOWN signals takes logic one value and phase error is zero. Finally not to produce a dead zone for Te ≤ ti case and gate delay must be as small as an inverter delay. Improved phase frequency detector circuit is shown at Figure 4.22.

CORELIB library's flip flops are used at these schematics. To achieve equal path delay, transmission gates are used parallel with inverters.

These phase frequency detectors are compared via transient simulations. Figure 4.23 shows output currents of PFD +charge pump block for the condition that reference frequency is higher than feedback frequency.

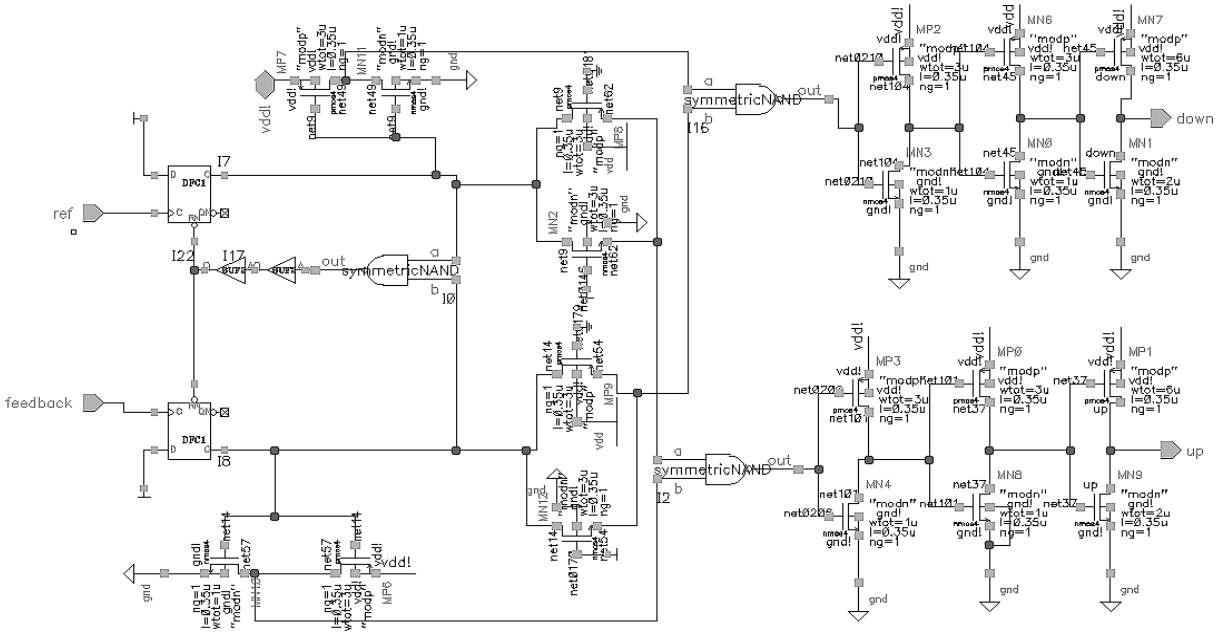


Figure 4.22: Improved Phase frequency detector Schematic

From this figure it can be seen that, first PFD has a 278 µA amplitude glitch at 1.47ns, when both up and down signals are applied to charge pump. For the improved version, no glitch occurs for this situation. In addition Figure 4.24 supports this idea which represents the contrast of condition above.

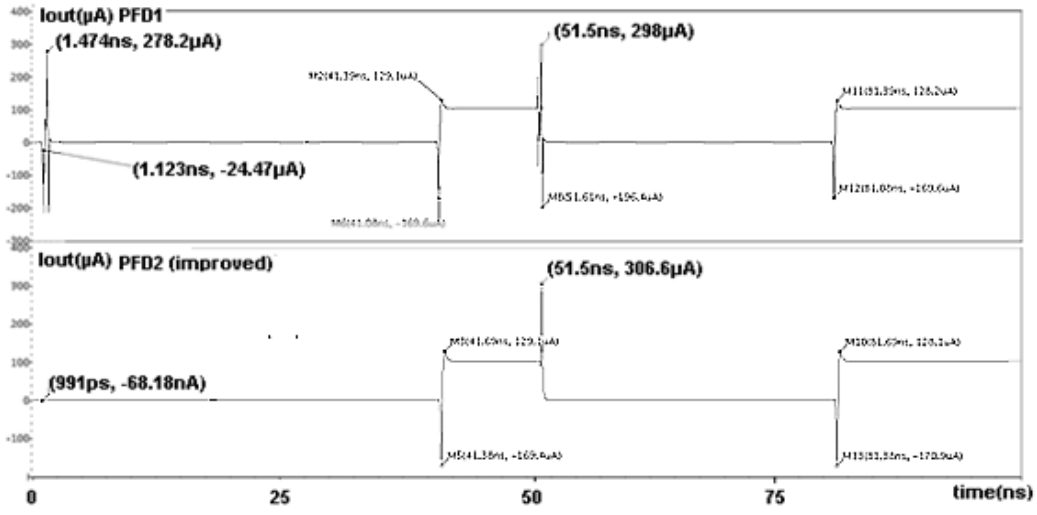


Figure 4.23: Comparison of two Phase frequency detectors for the condition that reference clock leads feedback clock which causes up signals.

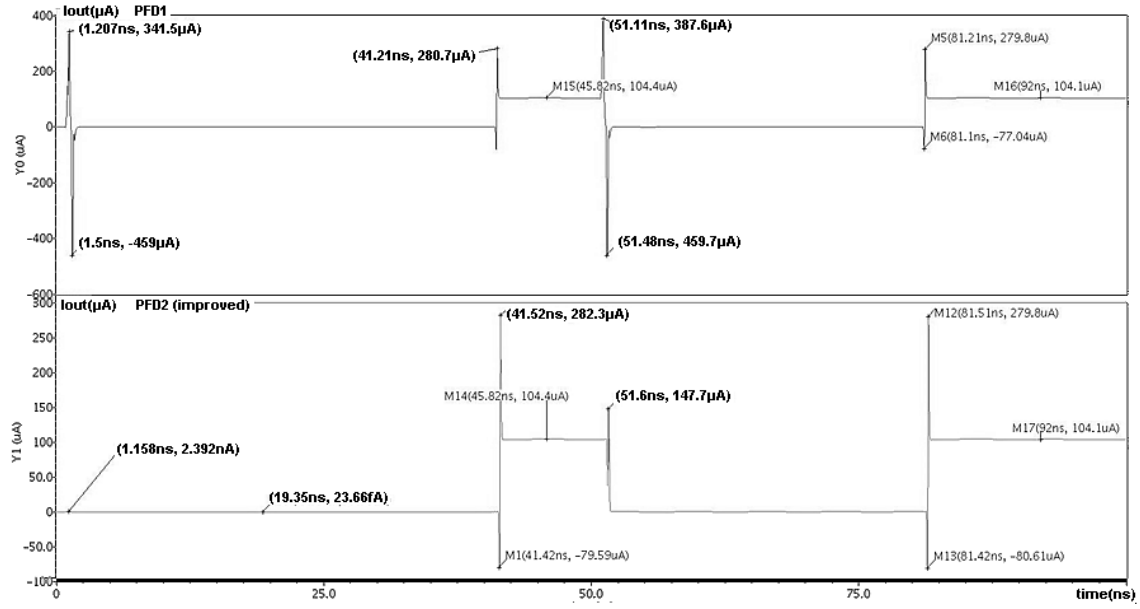


Figure 4.24: Comparison of two Phase frequency detectors for down signals.

Finally, for the lock condition, glitches are generated by charge-pump for each change of state of clock signal which is represented at Figure 4.25. This figure also includes integration of these currents, which shows us decrease of current mismatch in the order of 10^4.

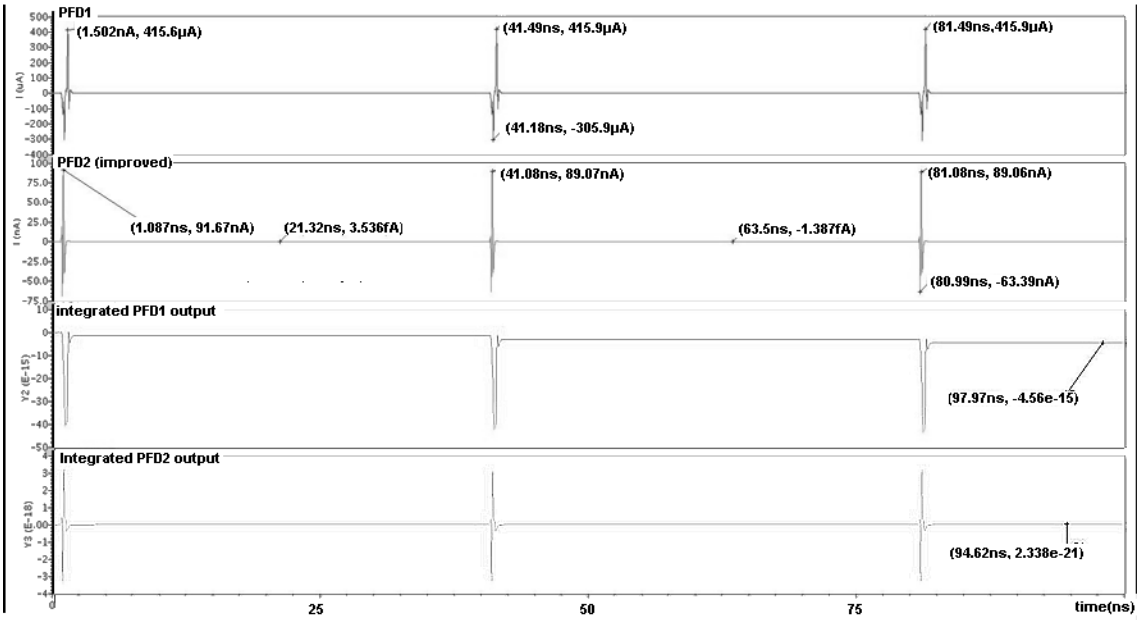


Figure 4.25: Comparison of two Phase frequency detectors for locked condition.

At integration of charge pump and PFD, XOR components from CORELIB are used to achieve equal path delay as represented at Figure 4.26. Layout of phase frequency detector is shown at appendix (AP 29). Finally the layout of integrated PFD and charge-pump is shown at appendix (AP 30) which has 150x212µm^2 area.)

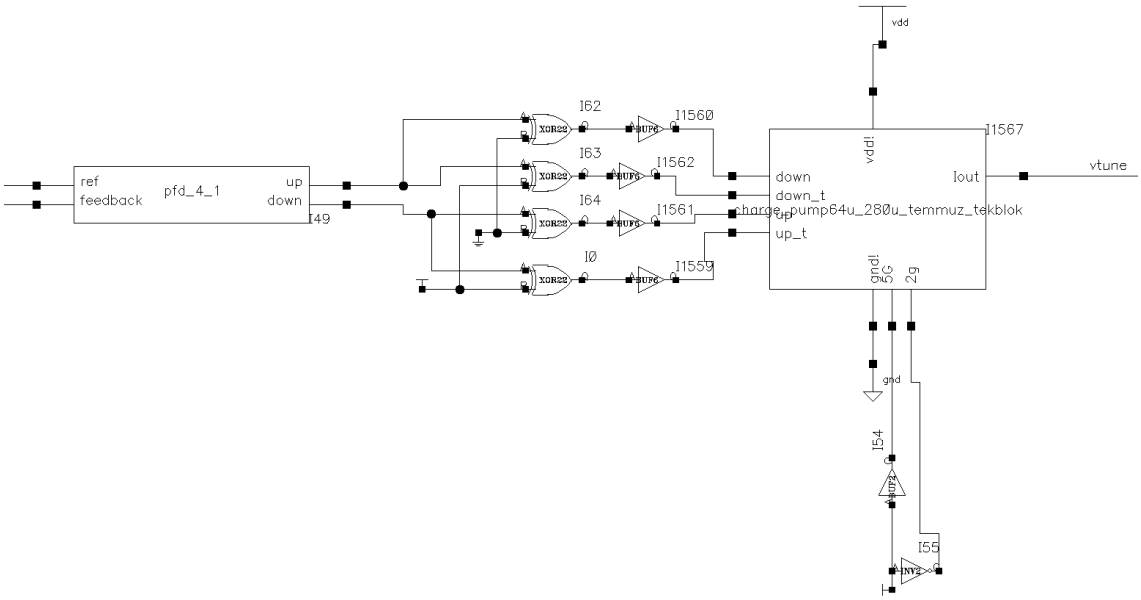


Figure 4.26: Charge Pump and PFD integration

4.3 Frequency Dividers

4.3.1 Programmable Multimodulus Frequency divider

Design of programmable multimodulus frequency divider (PMFD) is straight forward because of its relatively low operating frequency. The main operating principle is described at chapter 2. At design of this block the techniques at [35] have been used.

Figure 4.27 shows schematic of three bits programmable counter which consists of logic components which are taken from CORELIB library to save area and design time, and dual modulus prescalers (DMP). DMP which is shown at Figure 4.27, has two division ratios, two and three. If control bit is logic 1, frequency divider divides frequency by 3, else division ratio is 2. From the schematic which can be seen from Figure 4.27, DMP is made up of logic components from CORELIB library of foundry and True Single Phase Clock (TSPC) based flip flops. If the division ratio is three, DMP has worst case because the signal has to pass from two gates and two flip flops. This case determines highest operating frequency of DMP and PMFD.

TSPC technique uses only one clock signal without inversion to prevent clock skew problem. Operation at high frequencies can be achieved with this technique. Schematic of flip flop circuit is shown at Figure 4.28a, which consists nine transistors, in three stages. When the clock is low,

output of third state does not change. First stage acts like inverter while second stage is precharged. During the transition time that the value of the clock changes from low to high, seconds stage acts like inverter while writing the data at output of first stage to the output of second stage and third stage does not change its output value. When the clock is high, output of first and second stage does not change and saves the previous value while third stage acts like inverter and changes the data at output node. Thus, data is written to output of first stage when the clock is low. During low to high transition time, data is written to the output of second stage. Finally data is written to the output of third stage when clock is high. Every stage inverts data when writing, so output of third stage is Q.

Total capacitance seen from clk is around 20fF and from D is around 7fF. Figure 4.27 shows that, maximum load for dual modulus prescaler, which is driven by QB output of second flip-flop, is total input capacitance of three NANDs from library (one NAND23 and two NAND24), and last inverter of flip flop which corresponds 72fF input capacitance. To drive this load, at least three invērters are needed for digital buffer which is shown at Figure 4.28b.

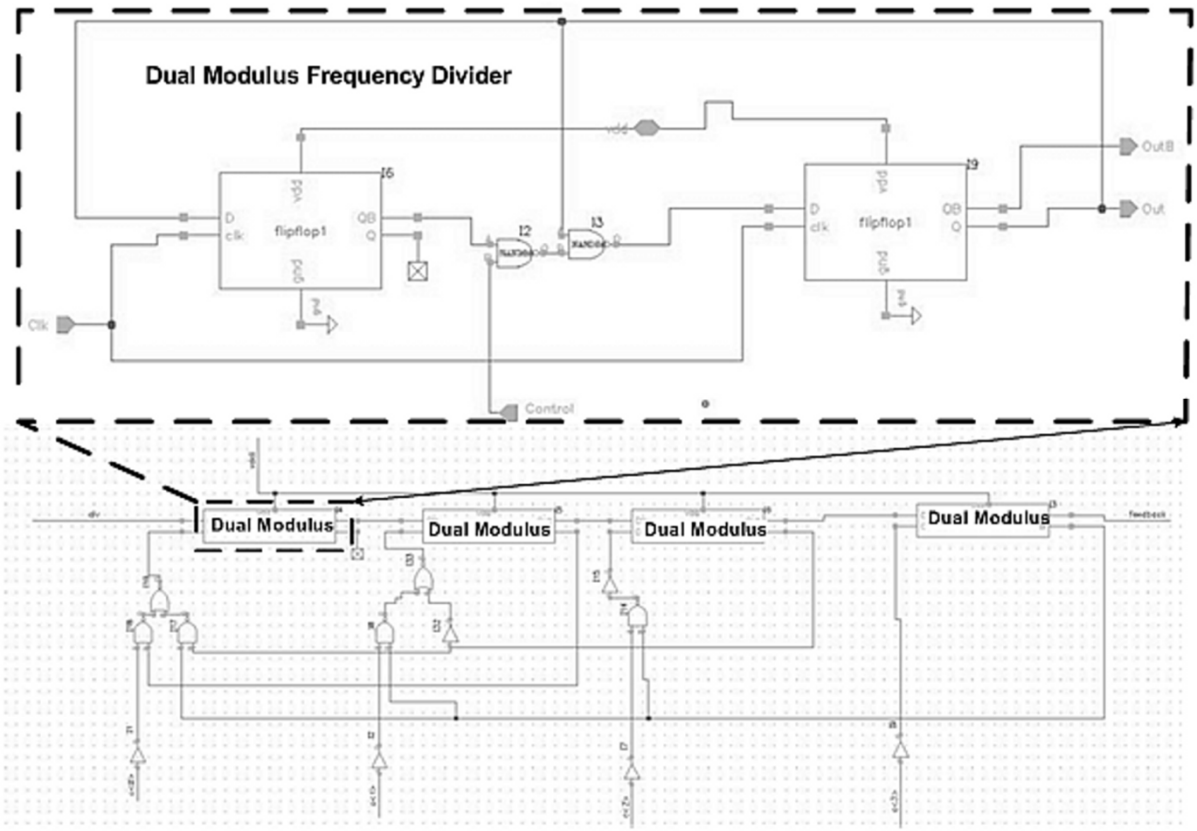


Figure 4.27: Multimodulus frequency divider made up of Dual modulus Frequency Dividers.

Because a fixed frequency divider which divides frequency by four is used before frequency divider, and maximum 6GHz is aimed for the design of PLL, DMP should operate at least 1.5GHz. From Figure 4.29 it can be seen that dual modulus divider can operate till 2GHz.

Mask layouts of these circuits can be found at appendix B3.

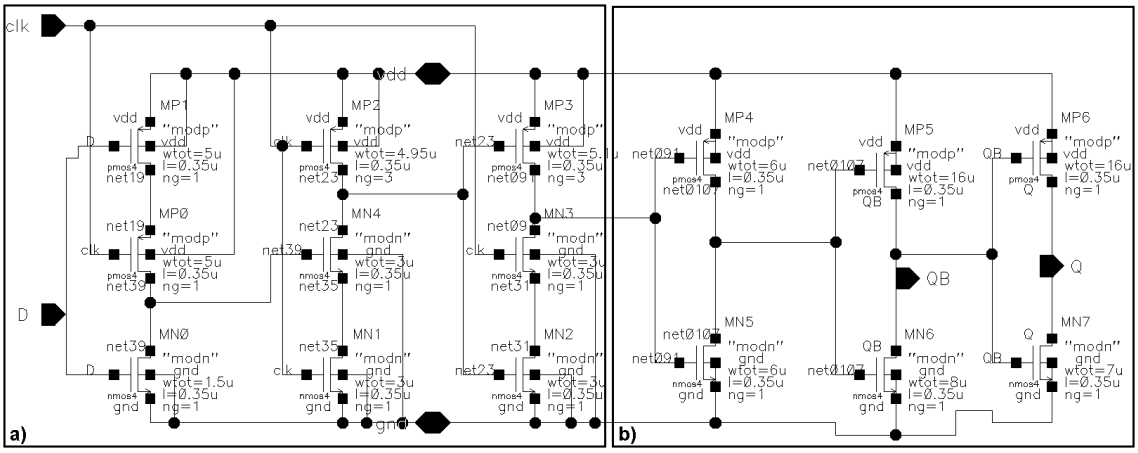


Figure 4.28:a) Schematic of True single phase clock based flip flop b) digital buffer

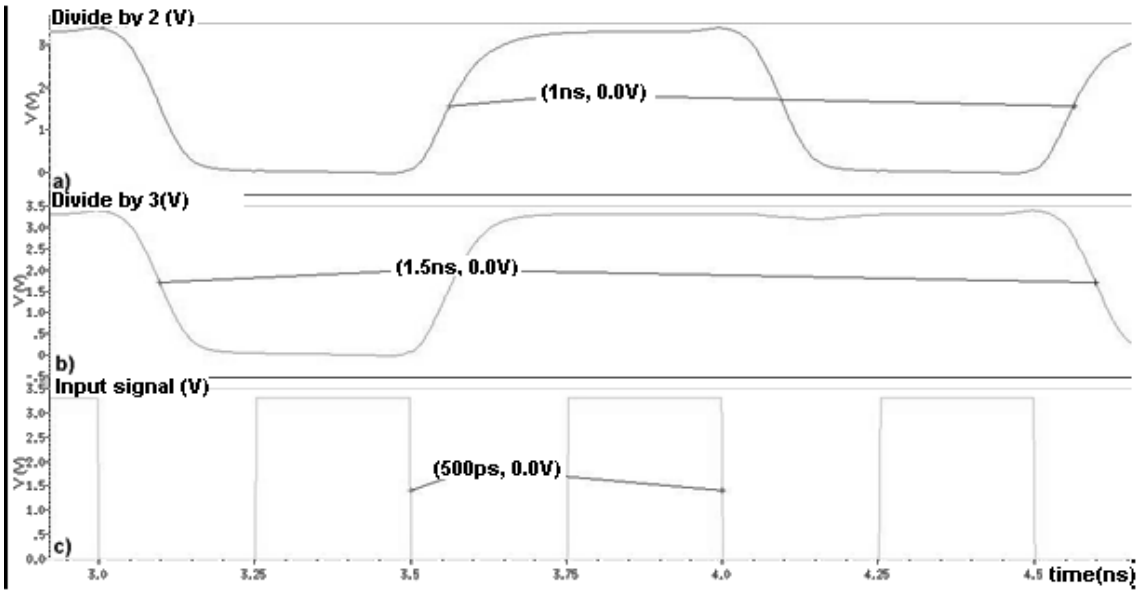


Figure 4.29: a) output of dual modulus divider for divide by 2 mode b) output of output of dual modulus divider for divide by 3 mode c) reference clock

After some modifications to the circuit at Figure 4.28, smaller and faster version, which is shown at Figure 4.30, is also designed for higher frequency operations. With this flip flop frequency division for both two and three are achieved at 3.7GH as shown at Figure 4.31.

For operation of this architecture, full swing (0 to 3.3V) rectangular clock signals are needed. However as we will see at chapter 3.5, amplitude of voltage controlled oscillator is about 1V. On the other hand, inverters which are used as amplifier to generate full swing rectangular signal does not have enough gain with an inverter load. For test of inverters, test bench at Figure

4.32 is designed. In this test bench a 3GHz sinus is applied to the inverters to generate needed signal at OUT node.

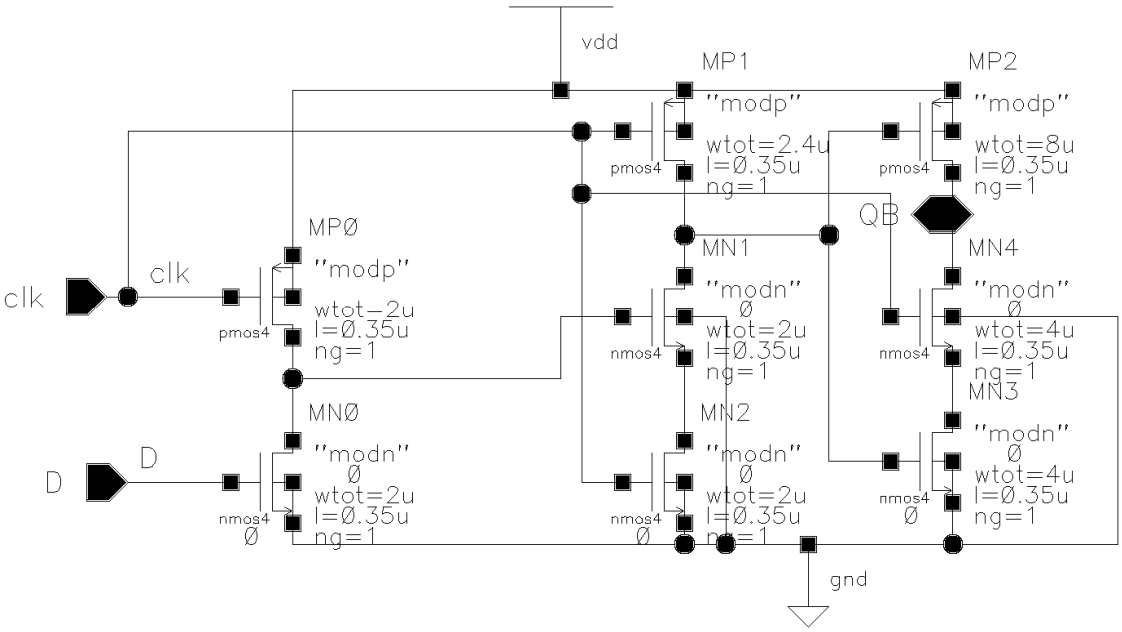


Figure 4.30: Schematic view of modified flip-flop

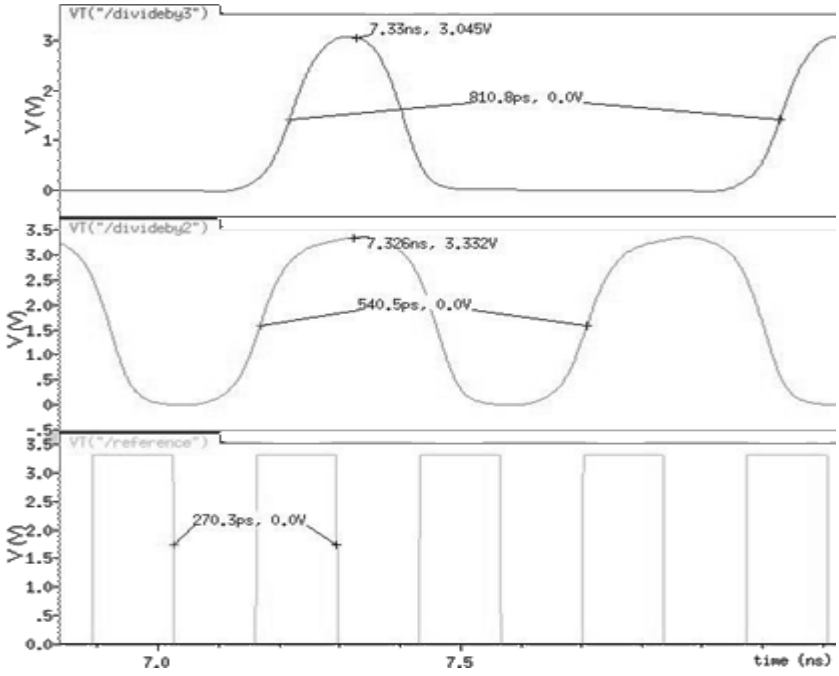


Figure 4.31:a) Output of dual modulus divider for divide by 2 mode b) output of output of dual modulus divider for divide by 3 mode c) reference clock

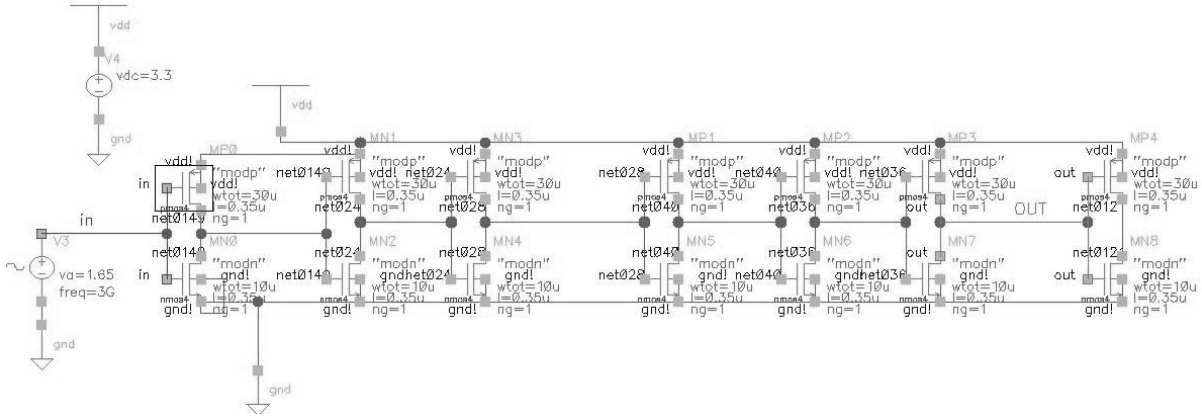


Figure 4.32: Test bench to search design limit of inverters

As seen from Figure 4.33, output of the circuit at Figure 4.32 is not enough to drive programmable divider, although six large inverter stages are placed between input and output. Thus, at a fixed frequency divider, which divides frequency by four, that is explained at next section, is needed before programmable divider.

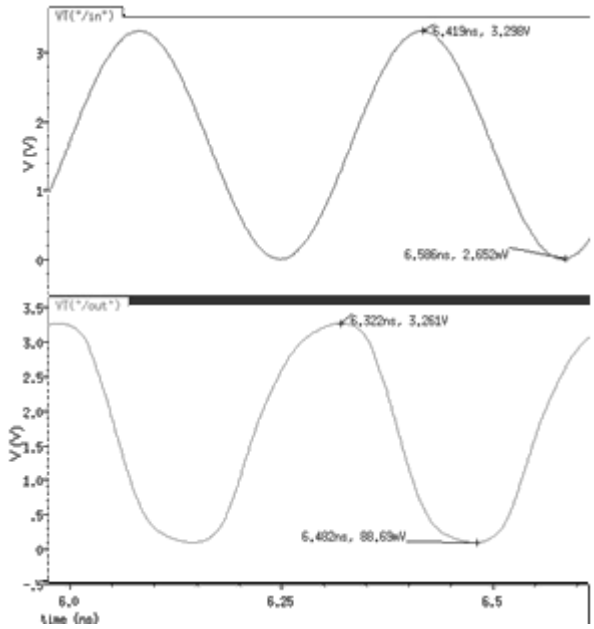


Figure 4.33: input and output of inverter stage. Output is not a square wave which is needed for programmable divider.

4.3.2 Divide-by-four Circuit

As inverter analyses show, static and dynamic design techniques are not useful for high frequency operation as high as 6GHz, for this technology. Thus, fixed frequency divider is designed via current mode logic techniques.

Figure 4.34 shows the schematic of the circuit. For this circuit, 0.5V amplitude sinusoidal signal is enough for CLK input. MP2 and MP3 are used as loads. When the clock is low, current flows at right hand side of the figure where cross coupled transistors are located. If Q (or QB) is low, which is connected to V_B of Q3 (or Q4), current of Q3 (or Q4) is also low which causes a low voltage drop over loads to set QB (Or Q) high and current of Q4 (or Q3) is also high which sets Q (or QB) low. Thus data is latched for this condition. On the other condition, when the clock is high the current flows from left hand side of the circuit. If D is high, current of Q1 is also high which sets QB low, and DB would be low thus Q is high. For this condition data is sampled and written.

In design, W of MN15 is selected three times of MN9 for effective sampling. In addition, this geometry is important for current consumption while low current is needed for data storage. Q6 and Q5 transistors are diode connected which are coupled with sampling block, to have a constant gain for a wide operation. These diodes are also extends effective sampling time. Another effect of usage of these diodes is decrease of temperature dependence. Finally, output of VCO is coupled by DC coupling capacitors and 1.2kΩ resistances are used for DC biasing of the CLK input of the circuit. The main reason is the varying DC voltage of VCO due to oscillation band, operation frequency controlled by VC and temperature. (An optimum design without coupling capacitors, which can compensate this variation, is done. However, final circuit without coupling capacitors is too sensitive for little geometry changes, thus, cannot be sent for fabrication.)

Reasonable amplitude at output is needed because this latch will possibly drive another latch. Thus, input voltage specifications are also valid for output. The amplitude of the signal is limited by loads, VBE voltage of diodes and overdrive voltage of MN9 and MN15.

This circuit is an improved version of the circuit which is proposed at [36]. First improvement is usage of HBT's instead of MOS's because of their high gm values same current levels. The other transistors remain MOS because technology does not provide a good substitute for PMOS's. In addition, MN 15 and MN 9 provide higher output swing rather than HBTs. Second improvement is usage of diode connected PMOS's as load rather than biased PMOS's which are at triode region. This improvement provides a better temperature independency of the circuit.

Schematic of fixed frequency divider, which is made up of these latches, is shown at Figure 4.35. As seen from this figure, two latches form a master slave flip flop and two flip flops are connected as sequential counter which counts four. One of the Outputs of this circuit is buffered by six inverters to generate waveform needed by programmable divider. The other output is inverted and used as divided output of the final circuit.

As seen from Figure 4.36, input of frequency divider has 166ps period and period of output of frequency divider (before buffer) is 664ps, thus, frequency division is achieved. Figure 4.37 shows temperature variance and Band variance of Divider output. From this figure it is obvious that, DC level of the output increases with the increase of temperature. Total change is around 104mV at final circuit, and before modifications and optimizations this value was around 400mV which is closer to output amplitude that would make much more complicated to decide inverter thresholds (which also varies with temperature and supply voltage noise).

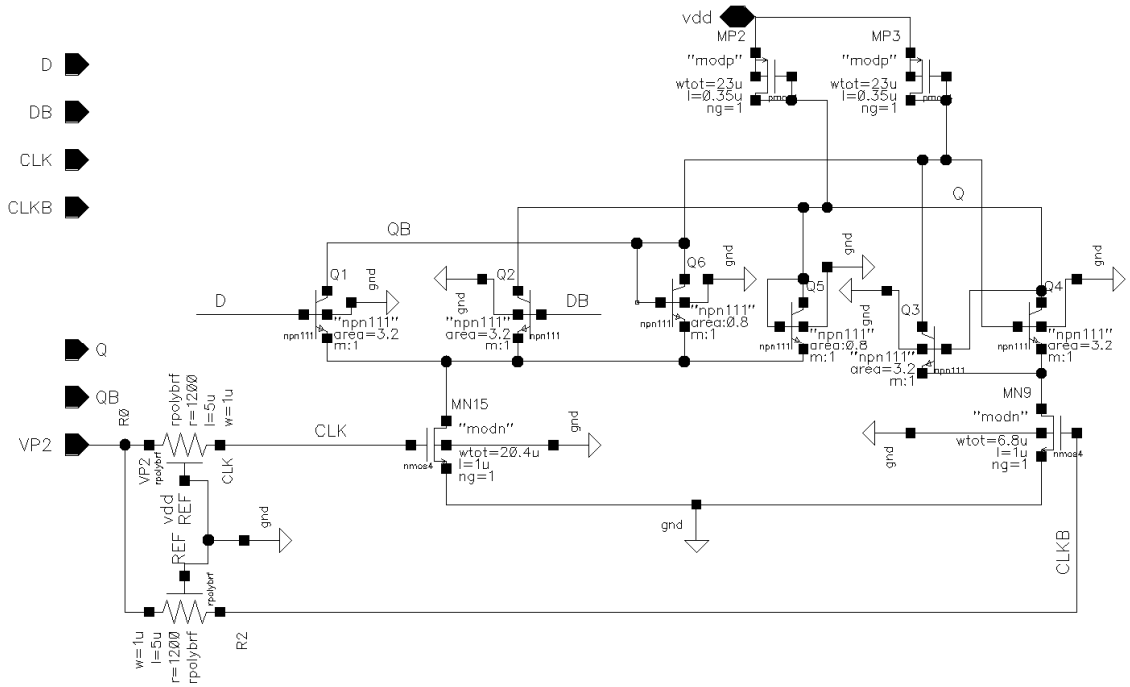


Figure 4.34: Schematic of the Current mode latch

As seen from Figure 4.35, output of frequency divider is buffered before programmable divider and the operation of inverter as amplifier is shown at Figure 4.38. As seen from Figure 4.38, first inverter increases amplitude of the wave from 586.2mV to 2.66V. Operation of buffer can be seen from Figure 4.39, that each inverter makes waveform sharper and full swing rectangular input signal need of Dynamic frequency divider is compensated.

The Mask layout of these blocks can be found at appendix B3.

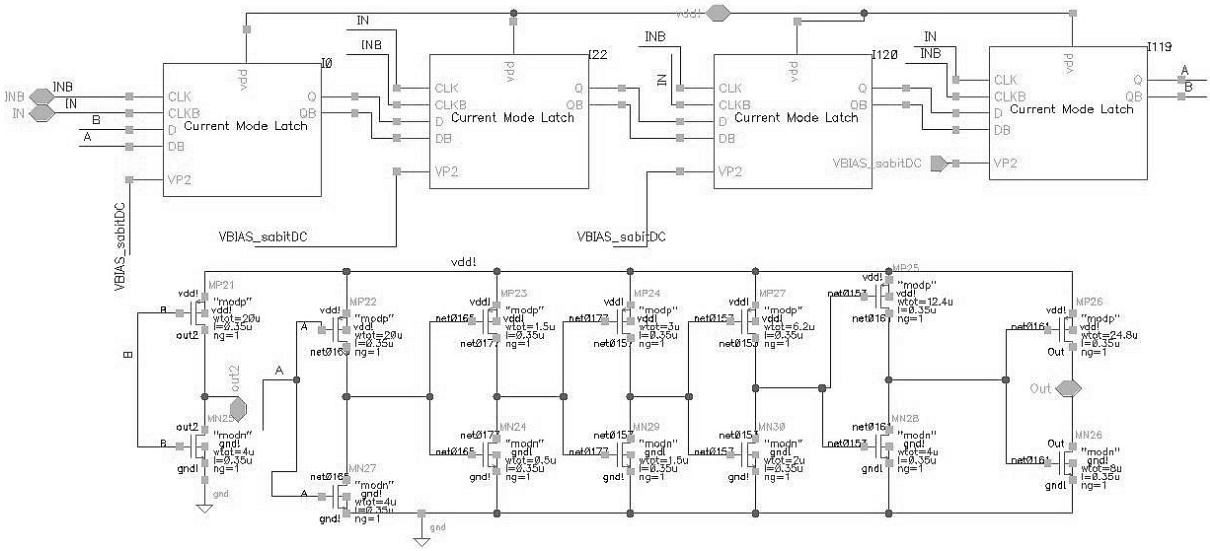


Figure 4.35: Fixed Frequency Divider Circuit (Divide-by-four-circuit).

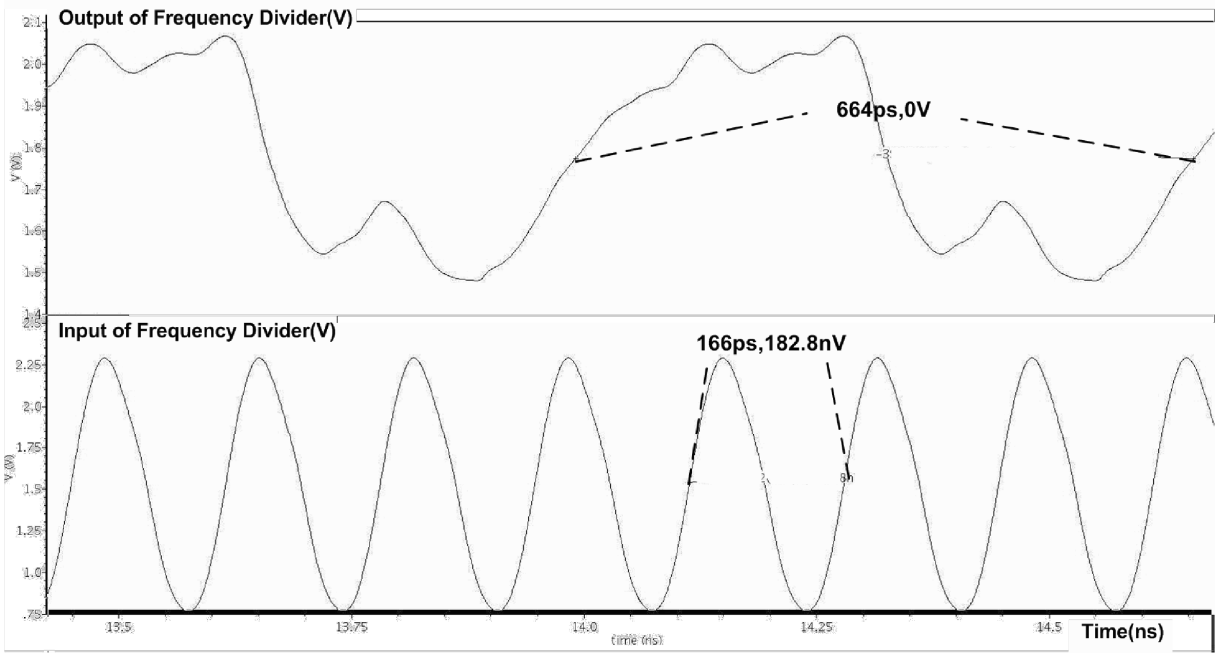


Figure 4.36: Output of fixed frequency divider has a period (664ps) which is four times of the input period (166ps).

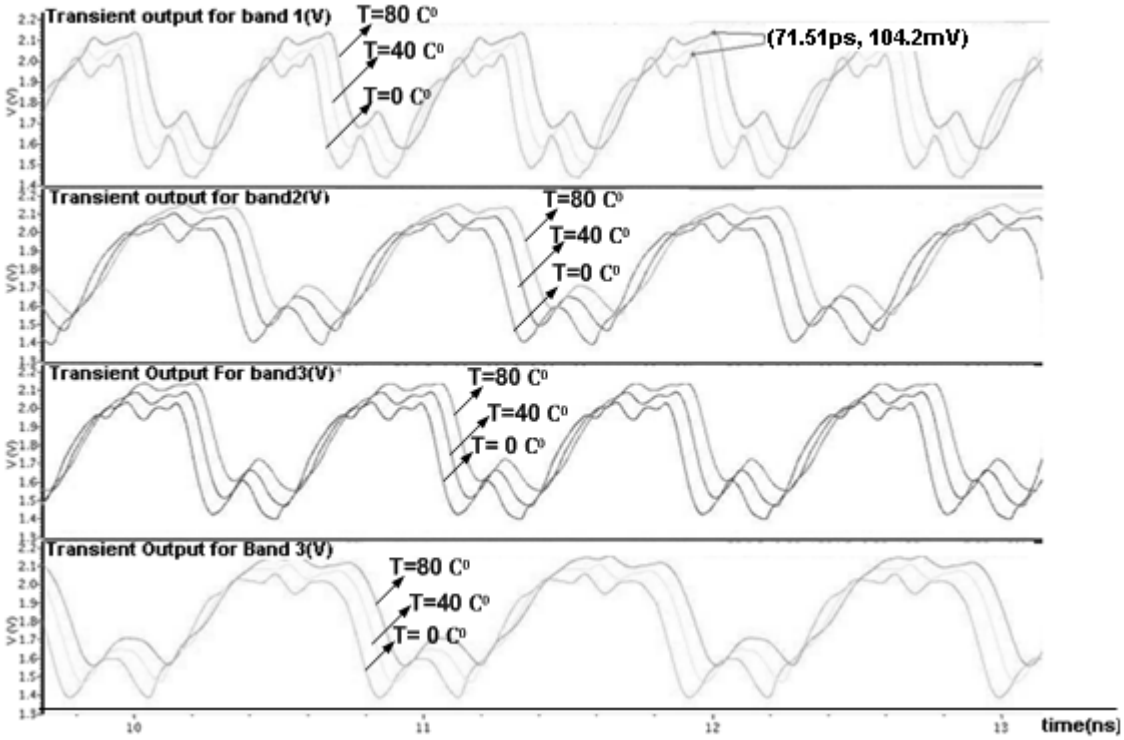


Figure 4.37: Output of frequency divider changes according to the frequency bands of the VCO and temperature. Four graphics shows all possibilities for two switches and three waves at each graphics shows temperature changes at 0 ^{0}C, 40 ^{0}C and 80 ^{0}C. According to the increase of temperature, DC value at output increases. The magnitude of the increase is 104.2mV. In addition DC value of the output is different for each frequency bands.

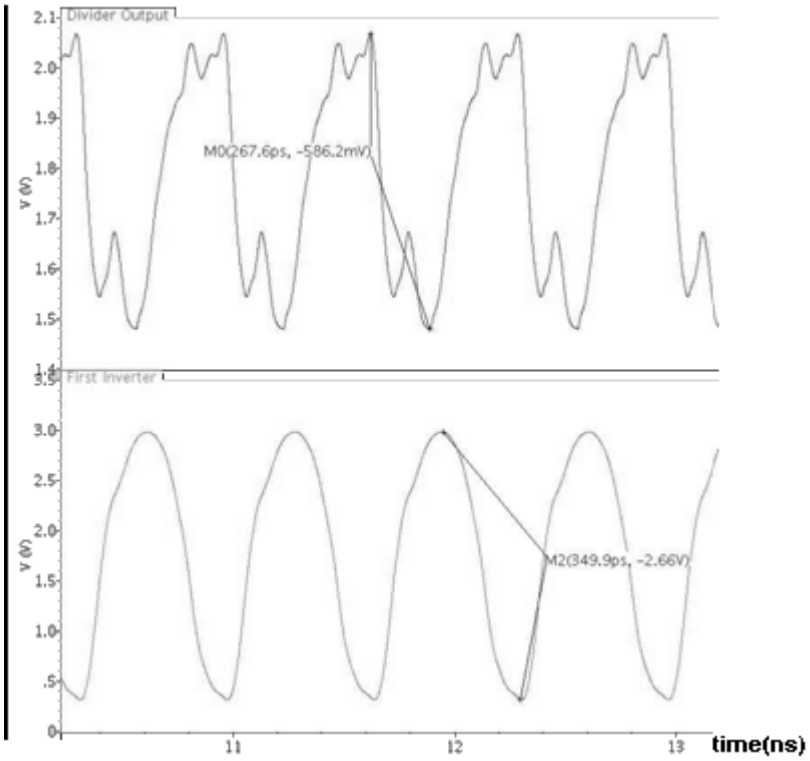


Figure 4.38: Operation of Inverter as amplifier. The gain is 4.5 for 1.5GHz signal.

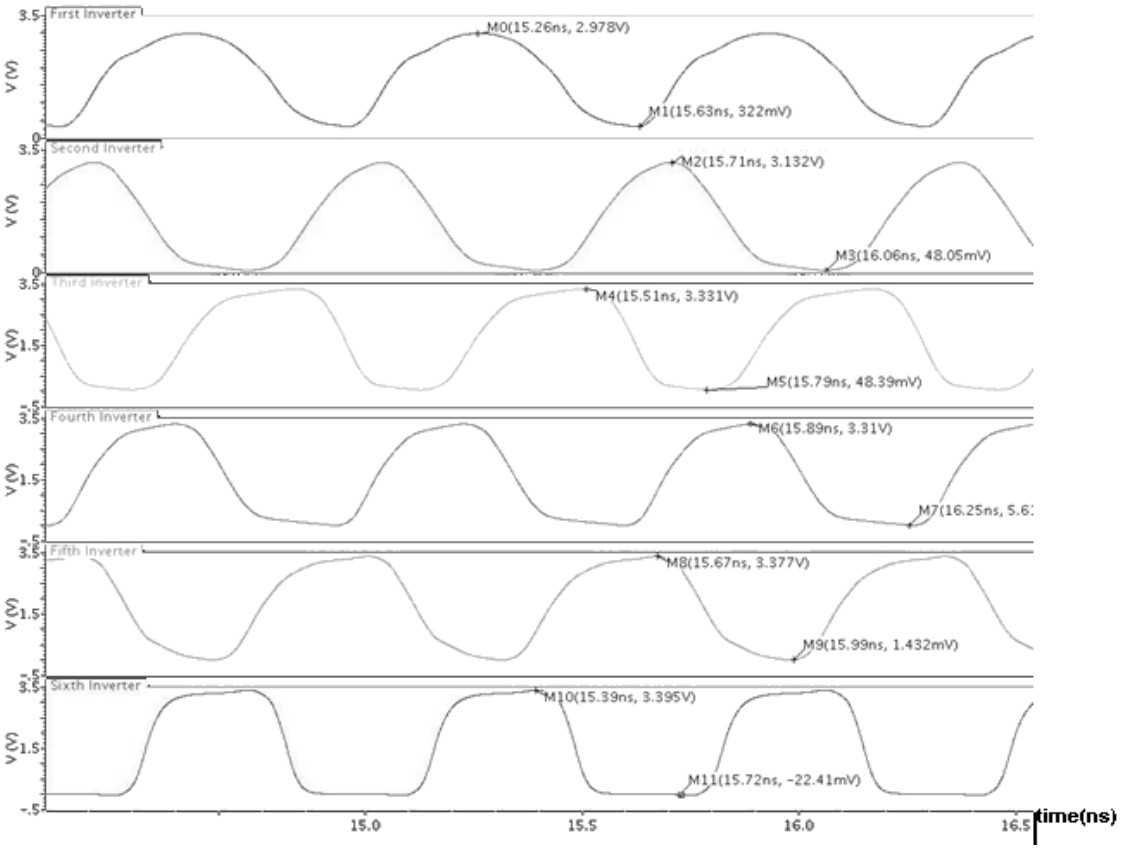


Figure 4.39: Operation of Buffer of Frequency divider. For each inverter stage, wave form becames sharper and amplitude increases

4.4 Sigma Delta Modulator (SDM)

In design of Sigma delta modulator block, full custom digital IC design techniques are used. In this block, standard cell library of foundry (CORELIB) has been used to save area and design time. Schematic of the block is represented at Figure 4.40, which is straight forward digital implementation of Figure 3.30. At output stage, a selection between output of first accumulator of third order SDM, which corresponds a first order SDM, and output of third order SDM is done via multiplexers. With this improvement the order of SDM has become selectable (or programmable).

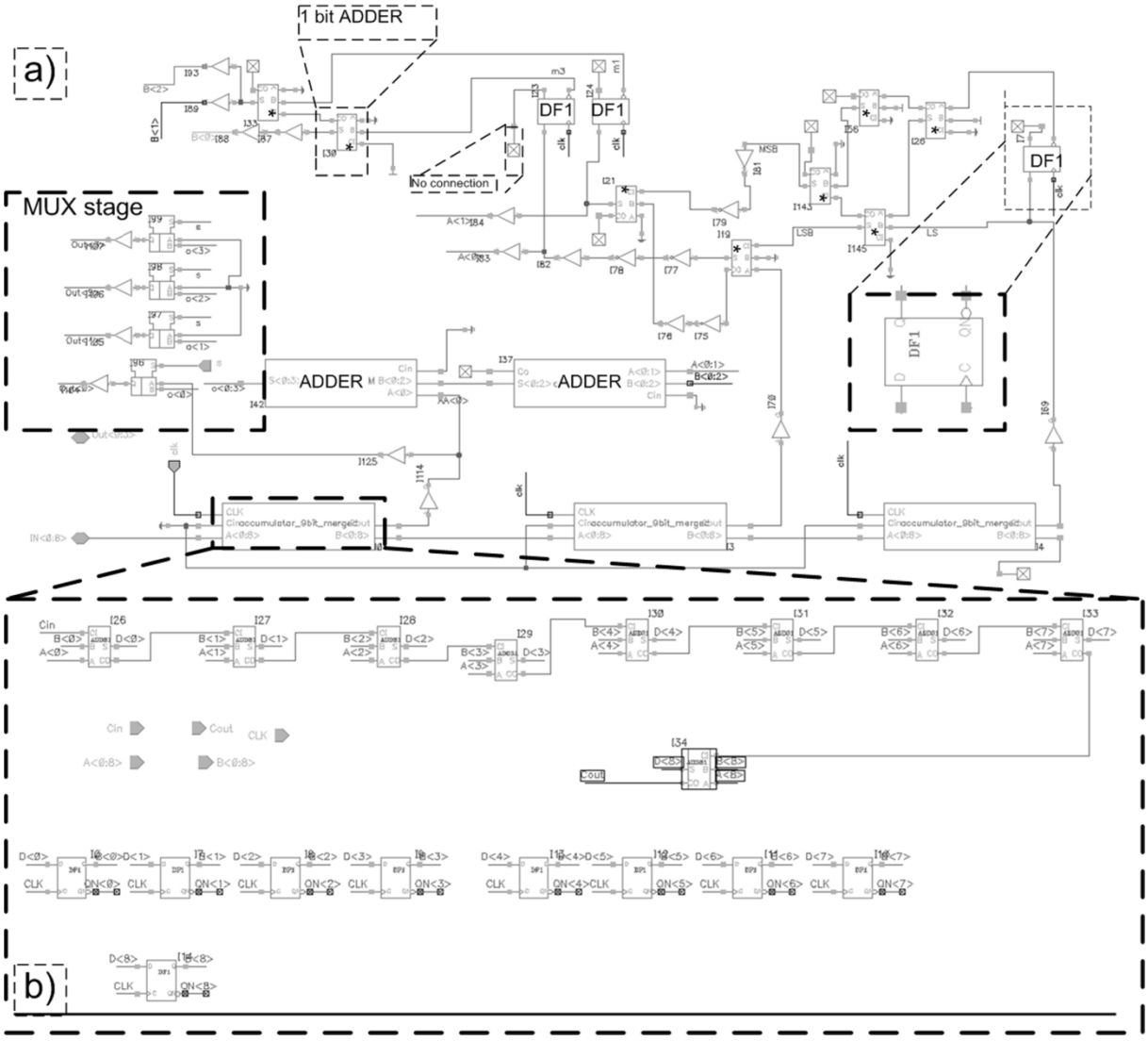


Figure 4.40: Sigma delta modulator a) block diagram of sigma delta modulator, b) inside of the accumulator (* is used to mention 1 bit adder)

In order to simulate this block an individual test bench is needed as seen at Figure 4.41. Randomization of SDM can be seen from instantaneous values. If we integrate output of sigma delta modulator, output must be identical to accumulators integrated output. Thus, two accumulators are connected to the output of these two blocks, and the results are compared. Finally, schematic simulation of accumulator is compared with Matlab® model. Output of SDM is shown at Figure 4.42. As seen at Figure 4.42, instant division ratio of SDM varies but total division ratio change catches accumulator output. Thus, randomization is achieved. As seen at Figure 4.42, schematic simulation of accumulator is identical with its Matlab® model.

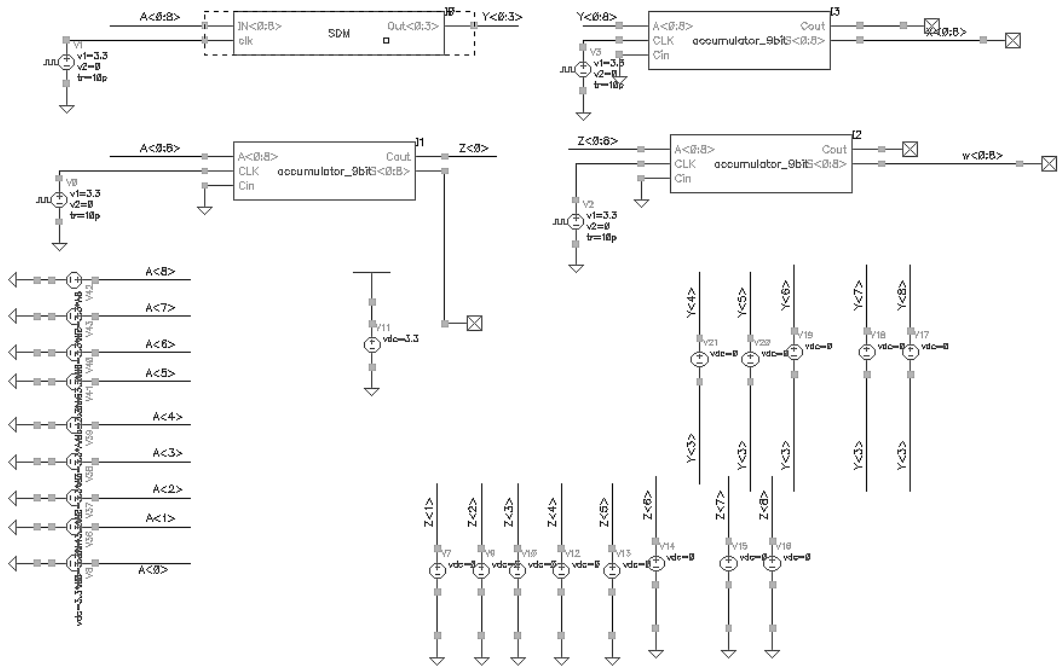


Figure 4.41: Test bench of Sigma Delta modulator, output of sigma delta modulator and an accumulator is integrated. If the sigma delta modulator works properly, integration of two blocks are identical in long term.

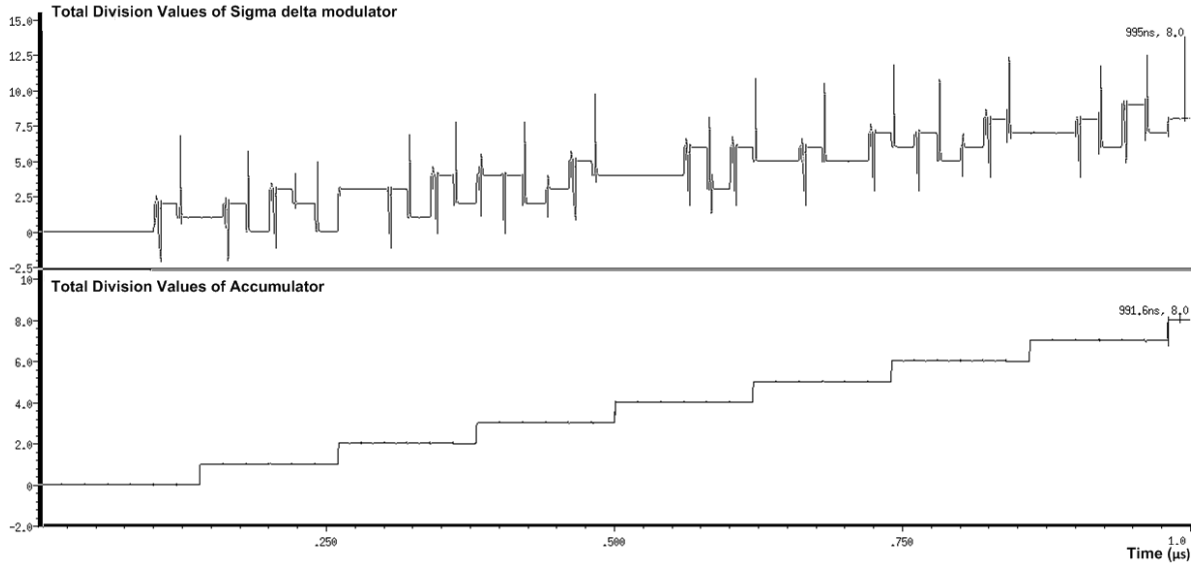


Figure 4.42: Total division value change of Sigma delta modulator and Accumulator.

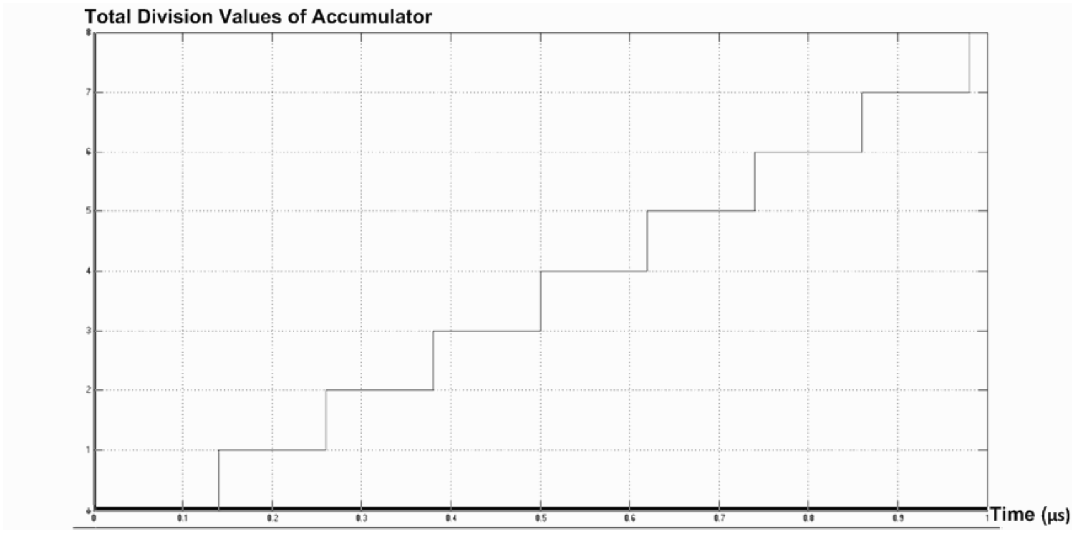


Figure 4.43: Integrated (accumulated) Output of accumulator at Matlab

4.5 VCO

There are lots of options for VCO topology such as, Multivibrator oscillators [54], Ring oscillators [55], and LC resonator based oscillators [56]. In comparison with other two topologies LC oscillators provide highest spectral purity and lowest phase noise, which are significant for meeting requirements of communication standards. In LC oscillators, a feedback is needed to achieve Barkhausen's criteria and provide permanence of oscillation. Feedback part can be provided by either a single amplifier with a tapped passive (L in Hartley oscillators, C in Collpitts oscillators) or two amplifiers ($-G_m$ oscillators). The differential negative Gm topology is chosen because differential output is crucial for fixed frequency divider, as explained at chapter 4.3.2.

A Non-complementary topology is selected rather than complementary cross coupled topology, as seen from Figure 4.44, to increase tuning range. In addition, noise sources are decreased because lower mobility and less hot carrier effect of PMOS transistors reduce 1/f noise rather than NMOS transistors. Moreover, power supply noise is reduced because of PMOS transistor based current sources [57].

Figure 4.44 shows schematic version of VCO of PLL which is modified from [36]. The design is explained in detail at [37] and [38].

Two different geometries for MOS switches of inductances (VL2 and VL3 switches) are proposed as modification in this section. First idea (LARGE switch) is to decrease small signal output resistance (r_o) of MOS's, such that, current flows from switches rather than inductance

when switch is on. This can be achieved with ultra large W and minimum L values for MOS [41-43]. Second and novel idea (SQUARE switch) is to use large square (w=L) NMOS as geometry. With use of such geometries, the parasitic capacitance seen from drain of MOS to ground is too large when the switch is on, and too small when the switch is off. Parasitic capacitances and small signal resistance of the NMOS are shown at Figure 4.45. Some of these capacitances are not physically related, such as CDS and CGB, which are generated by Spectre® and used at simulations.

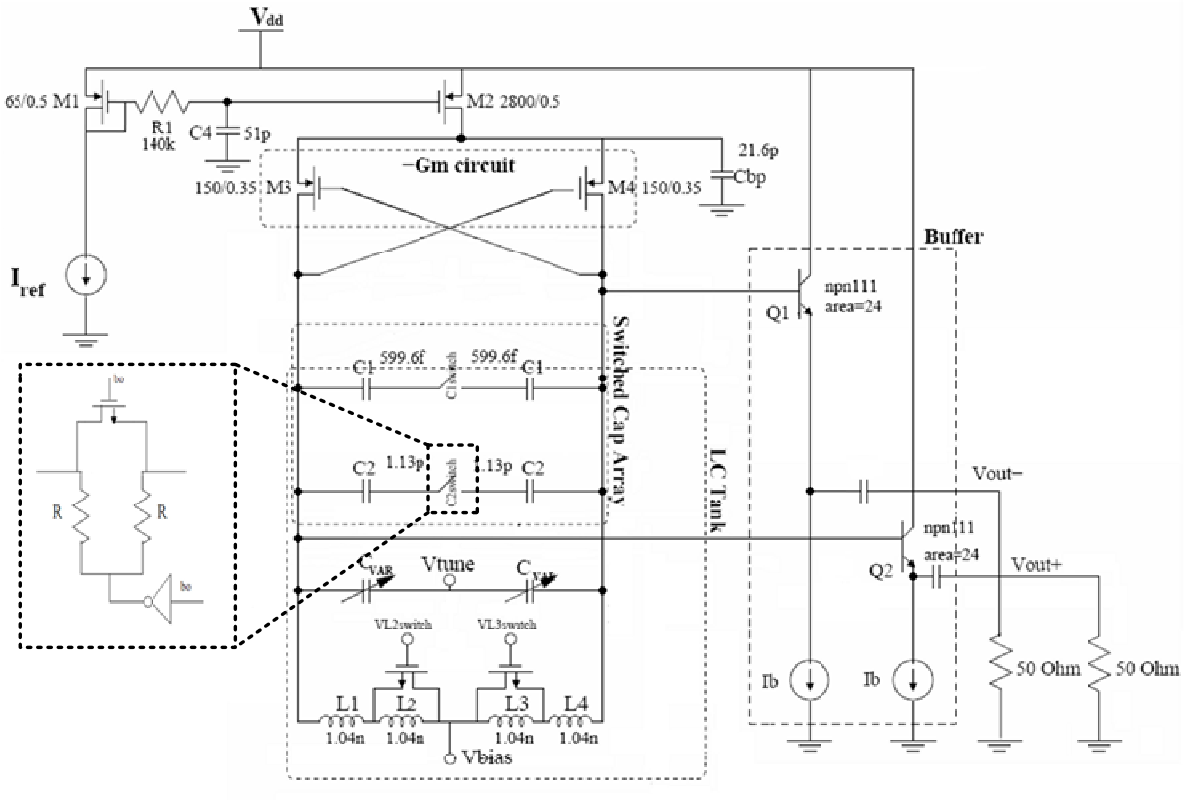


Figure 4.44: Schematic of VCO circuit.

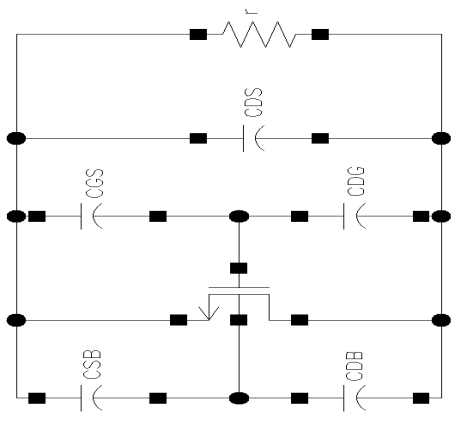


Figure 4.45: Parasitic passives of Transistor

VL2 and VL3 switch transistors are operating at triode region, thus, there is a small signal resistance, r=1/gds, occurs when the switches are on. VDS value for these transistors is very small so velocity saturation does not occur and square low is valid. According to these assumptions

$$r_{DS} = \frac{1}{g_{DS}} = \frac{1}{\frac{di_D}{dv_{DS}}} = \frac{1}{\mu_n C_{OX} \frac{W}{L}(V_{GS} - V_t)} \quad (4.8)$$

Vbias is set 1.9V, for "LARGE switch" W=2500µ, and L=0.35µ and for this technology (AMS® 035 BiCMOS) effective mobility is $370*10^8$ $\mu m^2/Vs$ and C_{OX}=4.86fF/ μm^2 (and VT is calculated as 929mV). With these values

$$r_{DS} = \frac{1}{\mu_n C_{OX} \frac{W}{L}(V_{GS} - V_t)} = \frac{1}{370*10^8 * 4.86*10^{-15} * \frac{2500}{0.35}(3.3 - 1.9 - 0.930)} = 1.653\Omega \quad (4.9)$$

From Appendix C2, r_{DS} is calculated via Spectre® as 1/428.3m=2.3348Ω

Magnitude of impedance of inductance for 5G is

$$|Z(j\omega)| = |j\omega L| = j2*\pi*5G*1.040n = 32.6726 >> r_{DS} \quad (4.10)$$

Thus, signal chooses to flow over NMOS.

Small signal model of LC tank of the circuit is represented at Figure 4.46. For this tank, C_{Switch} is total capacitance seen from drain of VL2switch (or VL3switch of Figure 4.44). C_{Fixed} is total capacitance added by switches, C_{Var} is the capacitance of varactor which is controlled by V_{tune} and $C_{Parasitics}$ is total parasitic capacitance of: Spiral; C_{GD} of M3 and M4; $C_{GS}+C_{DB}+C_{DS}$ of M3 and M4; capacitance seen from bases of Q1 and Q2. r=1/gds. Gate of VL2switch and VL3switch are DC biased, thus,

$$C_{switch} = C_{DS} + C_{SB} + C_{GS} \quad (4.11)$$

If SQUARE switch is used (W=130µ, L=130 µ) and the switch is on, total capacitance and magnitude of total inductance can be calculated from the values at appendix C2 as:

$$C_{switch} = 31.97pF + 7.12pF + 43.38pF = 82.47\text{pF}$$

$$|Z(\frac{1}{j\omega C})| = |\frac{1}{j\omega C}| = |\frac{1}{j2*\pi*5G*82.47p}| = 0.3860$$

Which is much more smaller than magnitude of impedance of inductance, thus, signal choses this path. However small signal resistance, r=1/78.12μΩ=12.8KΩ, comes parallel which must be neglected.

In addition, off capacitance of the switches must be added to $C_{Parasitics}$. Off capacintaces of the switches can be calculated from appendix C3 and C4 as:

$$\begin{aligned} C_{Off\_LargeSwitch} &= 702.8 * 10^{-27} + 288.5 * 10^{-27} + 390fF = 390fF \\ C_{Off\_SquareSwitch} &= 49.36yF + 813.8aF + 21.07fF = 21.97fF \end{aligned} \quad (4.12)$$

On the other hand oscillation frequency of the circuit can be roughly calculated as :

$$f_{osc} = \frac{1}{2\pi\sqrt{L_{Total} * (C_{Var} + C_{Fixed} + C_{Parasitics})}} \quad (4.13)$$

Where L_{Total} is total inductance value for Z_1, which is: L1, if switch is on; L1+L2 if the switch is off. As seen from (4.12) and (4.13), In terms of frequency reduction, which is caused by off capacitance values of the switches, performance of SQUARE switch is much better than LARGE switch. On the other hand, width of the LARGE switch is at the limit in the light of "off capacitance".

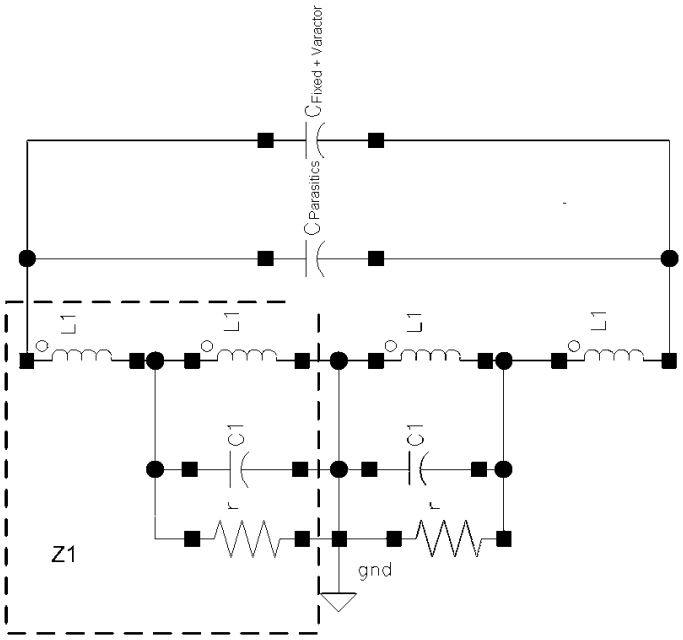


Figure 4.46: LC tank of the circuit.

Furthermore Quality factor of L1 is [40]:

$$Q_L = \frac{L_1 \omega}{R_S} \quad (4.14)$$

Where, R_S is serial parasitic resistance of inductance Quality factor of this inductance for this technology is 11.8 at 5GHz [38] so R_s (serial parasitic resistance) of inductance is 2.7689 Ω.

Quality factor of the tank can be calculated as [40]:

$$\frac{1}{Q_{TANK}} = \frac{1}{Q_L} + \frac{1}{Q_C} \quad (4.15)$$

For this application, $Q_L << Q_C$, thus, $Q_{TANK} \approx Q_L$.

For LARGE switch topology, small signal output resistance of the switch, which is calculated as 2.3348Ω at Cadence®, will be serial to R_S, if the switch is on. If we add this resistance to R_S, final quality factor will be

$$Q_L = \frac{L_1 \omega}{R_S} = \frac{1.040n * 5G * 2 * \pi}{(2.7689 + 2.3348)} = 6.4017$$

Parallel parasitic resistance for an inductance, which must be cancelled with gm of "-Gm" circuit, can be roughly calculated as,

$$R_P \approx \frac{L1^2 \omega^2}{R_S} = Q_L^2 R_S = 6.4017^2 * 5.1037 = 209.1586 \quad (4.16)$$

At negative Gm stage, in order to guarantee oscillation, each transistor must have transconductance, gm = k/R_P , where k is ~ 2-4 [39]. Thus, gm of –Gm circuit must be at least

$$Gm = \frac{k}{R_P} = \frac{4}{209.1586} = 19.1mS$$

For SQUARE switch topology, this calculation is more complicated. Z1 impendence of **Figure 4.46** is shown at Figure 4.47.

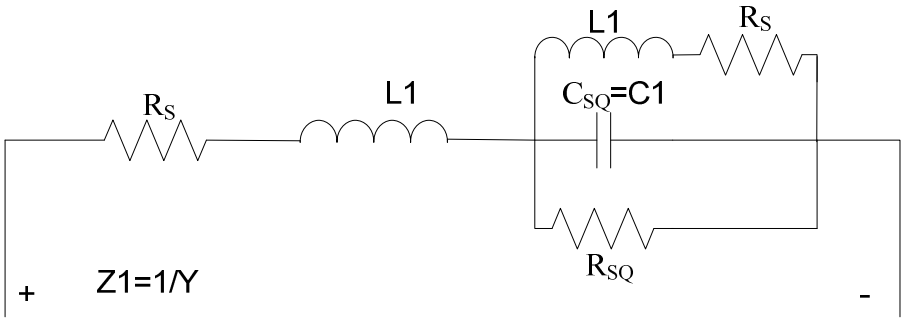


Figure 4.47: Detailed Z1 impedence of Figure 4.46 **including parasitic resistance of inductances.**

In figure 4.47, R_{SQ} is high enough to be neglected (it has been simulated at Cadence® as 12.8KΩ) If we calculate Y for this figure:

$$Y = \left[R_S + sL1 + (sC1 + \frac{1}{SL1 + R_S})^{-1} \right]^{-1}$$

$$= \left(R_S + sL1 + \left(\frac{sL1 + R_S}{s^2 C1L1 + sC1R_S + 1} \right) \right)^{-1}$$

$$= \left(\frac{R_S s^2 C1L1 + sC1{R_S}^2 + R_S + s^3 C1L1^2 + s^2 L1C1R_S + sL1 + sL1 + R_S}{s^2 C1L1 + sC1R_S + 1} \right)^{-1}$$

$$= \left(\frac{s^2 C1L1 + sC1R_S + 1}{s^3 C1L1^2 + s^2 (2L1C1R_S) + s(C1{R_S}^2 + 2L1) + 2R_S} \right)$$

(4.17)

If we replace s with jω,

$$Y = \left(\frac{(j\omega)^2 C1L1 + j\omega C1R_S + 1}{(j\omega)^3 C1L1^2 + (j\omega)^2 (2L1C1R_S) + (j\omega)(C1{R_S}^2 + 2L1) + 2R_S} \right)$$

$$= \left[\frac{j\omega C1R_S + 1 - \omega^2 C1L1}{(j\omega)(C1{R_S}^2 + 2L1 - \omega^2 C1L1^2) + 2R_S - \omega^2 (2L1C1R_S)} \right]$$

(4.18)

If we make replacements as,

$$A = (C1{R_S}^2 + 2L1 - \omega^2 C1L1^2)$$

$$B = 2R_S - \omega^2 (2L1C1R_S)$$

$$C = C1R_S$$

$$D = 1 - \omega^2 C1L1$$

(4.19)

After these rearrangements final admittance can be simplified as;

$$Y = \left(\frac{j\omega C + D}{j\omega A + B} \right) = \frac{\frac{C}{A}(j\omega A + B) + D - \frac{CB}{A}}{j\omega A + B} = \frac{C}{A} + \frac{D - \frac{CB}{A}}{j\omega A + B}$$

$$Y = \frac{C}{A} + \frac{1}{j\omega \frac{A}{D - \frac{CB}{A}} + \frac{B}{D - \frac{CB}{A}}} \qquad (4.20)$$

This admittance can be re-modeled as Figure 4.49.

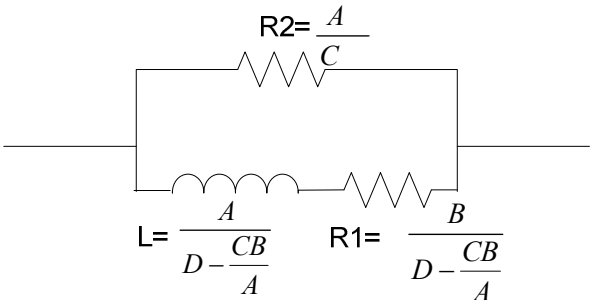


Figure 4.48: Simplified and re-arranged model of Figure 4.48

Parallel and serial inductances can be merged as Figure 4.50. For resonate frequency, which is around 5GHz and calculated via 4.13, 4.16 is valid. Thus figure 4.49 can be simplified as Figure 4.50.

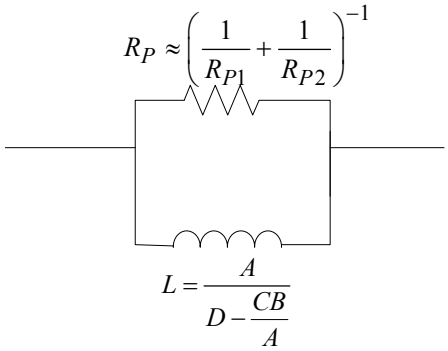


Figure 4.49: After arrangements and simplifications final model of Z1

If we calculate these values for 5GHz (m file for calculations can be found at appendix):

$$L = 1.0051nH$$

$$R_P \approx \left(\frac{R_S}{L1^2 \omega^2} + \frac{C}{A} \right)^{-1} = 357.5718\Omega$$

$$Gm = \frac{k}{R_P} = \frac{4}{357.572} = 11.19mS$$

Thus, inductance value does not change significantly and lower core current is needed for smaller Gm. In schematic simulations, the circuit with LARGE switch needs 2.708mA to oscillate, and the circuit with SQUARE switch needs 1.539mA to oscillate, while at [37], 2.4mA is needed.

Oscillation amplitude is also related with Quality factor and core current (tail current) as

$$V_{TANK} = \frac{1}{2} I_{CORE} \omega_0 L Q_L \qquad (4.21)$$

It is obvious that, the circuit with SQUARE switch oscillates with higher amplitude than the circuit with LARGE switch, for the same core current.

To conclude, in terms of, quality factor of tank, oscillation amplitude, core current, transconductance of –Gm circuit and off capacitance, SQUARE switch has better performance than LARGE switch. In addition, for applications at higher frequencies, Performance of square methodology increases. On the other hand it has lower switching speed with respect to LARGE switch. Figure 4.47, shows switching behavior of SQUARE switch in time domain. There is a buffer between inputs of two switches. At 100ns, the gate voltage of switch1 changes from zero to vdd (3.3). Gate voltage of switch2 has 5.5ns delay. At 110ns, oscillation frequency changes from 3.892GHz to 4.86GHz because two inductances are active for one side, and one inductance is active for the other side. At 117ns two inductance switches are on state and oscillation period is 174.26ps.

Modifications are not limited with switch of the inductance, width of some metal connections at layout and contact numbers of components are also increased because they would not carry the current flow over them. In addition, a guard ring is also added to surroundings of core of the VCO to add a Faraday cage effect. With these modifications at layout, a switched capacitance (467.5fF) is also removed from the circuit analyzed at [38], because at post layout simulations, expected bands can be covered with two switched capacitances. Furthermore, according to [41] and [43] W/L ratio of the switch of C_2 is increased from 50/10 to 100/5, because for larger capacitance switch must also be larger [41]. Moreover, in capacitance switch layouts, one fingered transistors are selected for transistors. As number of finger increases, contact resistances and metal resistances at drain and source increases which are series with capacitance as represented at Figure 4.44, which could degrade quality factor of capacitance. With this modification, gate resistance and gate capacitance increase but that will degrade band switching speed of VCO (which would increase settling time of PLL) which can be neglected if it is compared to settling time of PLL.

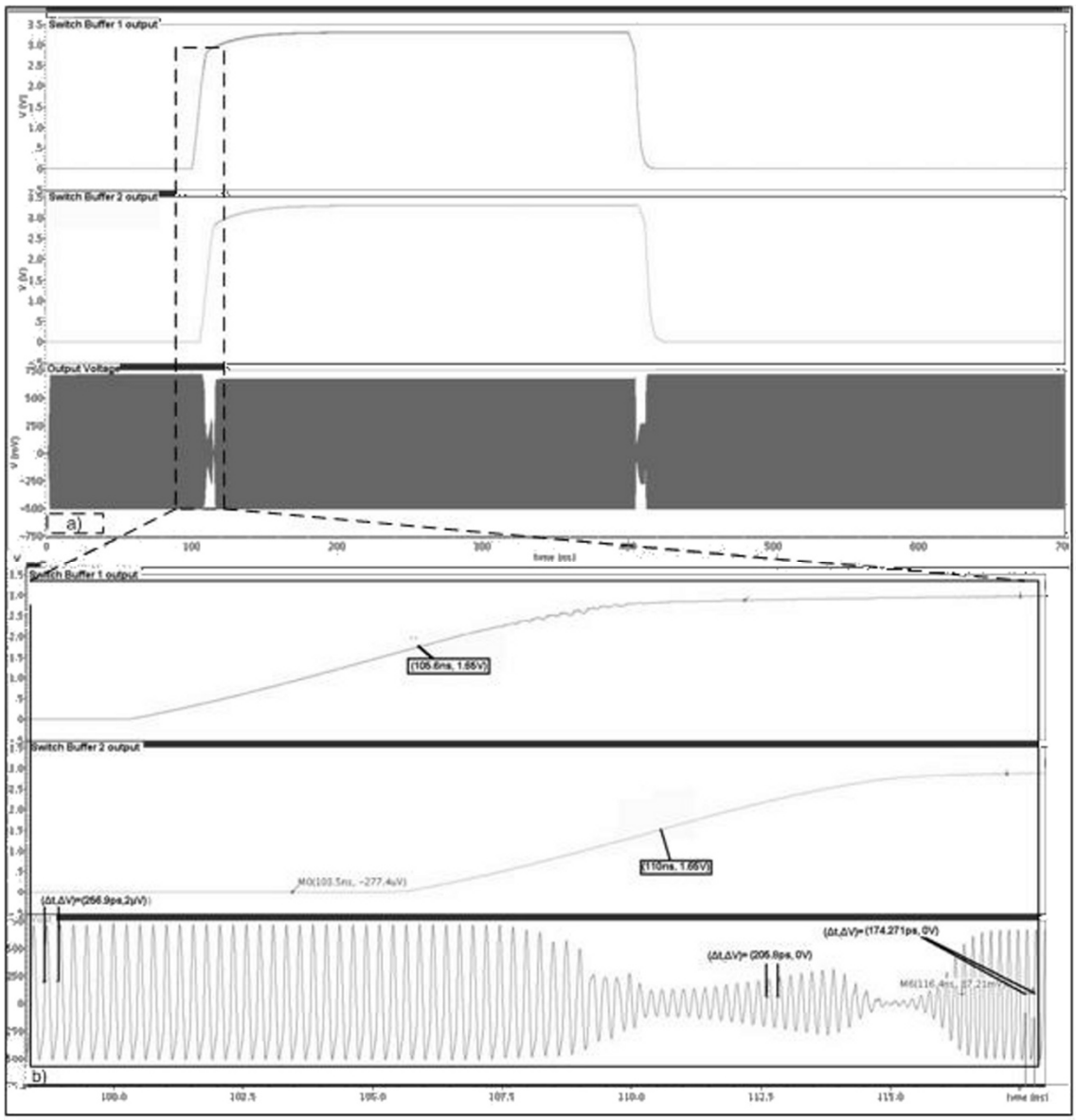


Figure 4.50:a) Switching behavior of circuit with SQUARE switch b) Zoom to selected area

Aimed Frequency bands are listed at Table 4-1. After post layout simulations achieved frequency bands with switches are at Table 4-2 for SQUARE switch and Table 4-3 for LARGE switch. These tables show us all aimed frequency bands except two WLAN bands 5.5-5.7 and 5.74-5.825GHz are achieved with one switch or two switches combinations. For example, 2.4-2.5 GHz WLAN band can be covered, if C_2 switch is on, C_1 is off and Inductor switch is off. If we compare these tables, increase at total capacitance, due to off capacitance of switch, shifted operating frequency and decreased quality factor of Capacitance. Reduction at quality factor of inductance affected phase noise dramatically and much more core current is needed. Oscillator can also be used for two bands mentioned above, which could not be achieved because of large parasitic capacitances come from layout, in a low IF based transceiver architectures (For other bands, applications can be found for oscillator both low IF and zero IF transceiver architectures).

Table 4-1: Aimed Frequency bands

Communication type		Operating Frequencies (GHz)					
Wimax	Canada	2.3-2.37	2.5-2.6	2.59-2.69	3.47-3.65	5.72-5.85	
	Brazil	2.5-2.69	3.4-3.6	5.72-5.85			
	Egypt	3.4-3.6	5.72-5.85				
	Finland	3.41-3.5	3.5-3.59				
	Singapore	2.3-2.35	2.51-2.7	5.72-5.85			
WLAN	802.11b/g/draft-n/y	2.41-2.49	3.65-3.69				
	5 GHz (802.11a/h/j/draft-n						
	United States	5.18-5.32	5.5-5.825				
	Europe	5.18-5.7					
	Japan	4.92-4.98	4.91-5.06	5.18-5.32	5.5-5.7		
	Singapore	5.18-5.22	5.74-5.83				
	China	5.74-5.83					
	Israel	5.17-5.32					
	Korea	5.17-5.32	5.5-5.64	5.74-5.83			
	Turkey	5.17-5.32	5.74-5.83				

One sample of the simulation result is located at Figure 4.49. In this figure frequency vs tuning voltage, phase noise vs tuning voltage and df/dV plot which shows linearity of the VCO are also located. As seen from Figure 4.49(c), gain of VCO cannot be represented with a constant K value. The output frequency with respect to the control voltage (and its derivative) is directly related to the capacitance change of library varactor witch is represented at Figure 4.51. It is obvious that Figure 4.49(c) is identical with Figure 4.51. This non-linearity of VCO, which comes from technology, brings additional poles to loop which degrades stability. On the other hand, Figure 4.50 is another sample of the simulation at Figure 4.49, for the condition that all the switches are on position. Additionally, for this condition, range of frequency is smaller than the condition at Figure 4.49. Because, (not the amount) but the percentage of the capacitance change is decreased with insertion of additional capacitance. Thence, VCO gain is also decreased. Thus, it can be said that VCO gain is different for all frequency bands. For this reason, second order loop filter is used at PLL.

It is expected that phase noise must increase with the decrease of frequency. Figure 4.50 and Figure 4.49 show us that, phase noise is also non linear and quality factor of varactor, which is represented at Figure 4.52, is most important reason of this non lineariyu. Simulation Results for all bands can be found at appendix D.

Definition of Figure of merit is [49]

$$FOM = L\{f_{offset}\} - 20\log(\frac{f_0}{f_{offset}}) + 10\log(\frac{P_{DC}}{1mW}) \quad (4.22)$$

Phase noise at offset frequency (f_{offset}) from carrier frequency (f_0) is denoted by L $\{f_{offset}\}$. VCO power consumption is denoted by P_{DC}, in mW. In 4.412 GHz, FOM is calculated for SQUARE switch as,

$$FOM = -117.4 - 20\log(\frac{4412M}{1M}) + 10\log(\frac{5.28mW}{1mW}) = -182.664dBc/Hz$$

At this calculation, power consumption of the core of the VCO is considered. Second and third harmonic powers at output are also important which is shown at Figure 4.53. From this figure it can be seen that Second harmonic and third harmonics are suppressed 20dBm and 30dBm.

Power dissipation is another important parameter for this circuit. The most power hungry of the circuit is Common emitter buffer which needs 9mA to operate. Minimum Core current requirement depends on operating band and operating frequency which changes from 1.7mA to 10.6 mA. Thus minimum power consumption is 35mW and maximum is 69.3mW.

Table 4-3, shows performance of designed with SQUARE switch VCO comparison with other published papers. This design has reasonable power consumption, average phase noise and good Figure of merit with respect to other designs. Because of operating technology, power consumption is below average. Phase noise performance is above average. This design is remarkable because it can operate eight different frequency bands.

Table 4-2:Post layout Simulations For SQUARE switch

	Band1	*Band 2*	*Band 3*	*Band 4*	*Band 5*	*Band 6*	*Band 7*	*Band 8*
$V_{switchC2}$ *(V)*	*0*	*3.3*	*0*	*3.3*	*0*	*3.3*	*0*	*3.3*
$V_{switchC1}$ *(V)*	*0*	*0*	*3.3*	*3.3*	*0*	*0*	*3.3*	*3.3*
V_{switch_ind} *(V)*	*3.3*	*3.3*	*3.3*	*3.3*	*0*	*0*	*0*	*0*
V_{tune} *(V)*	*0-3.3*	*0-3.3*	*0-3.3*	*0-3.3*	*0-3.3*	*0- 3.3*	*0-3.3*	*0-3.3*
Tuning Range (GHz) (PostLayout)	*5.321-4.492*	*3.379-3.727*	*3.7-4.2*	*3.352-3.101*	*3.564-2.958*	*2.29-2.54*	*2.515-2.843*	*2.107-2.298*
Phase Noise (dBc/Hz) at 1MHz offset	*(-117.4, -112.4)*	*(-120, -116)*	*(-116.9, -109.6)*	*(-123.8, -122.5)*	*(-111.2, -114.2)*	*(-120.1, -117.9)*	*(-120.7, -119)*	*(-122, -120)*
I_{vcore} *(mA) (RC extraction)*	*3.182*	*6.347*	*4.269*	*10.6*	*2.15*	*4.269*	*3.182*	*6.65*
I_{vcore} *(mA) (C extraction)*	*1.706*	*4.269*	*3.182*	*5.876*	*1.706*	*3.182*	*2.151*	*4.866*

Table 4-3:Post layout Simulations For LARGE switch

	Band1	*Band 2*	*Band 3*	*Band 4*	*Band 5*	*Band 6*	*Band 7*	*Band 8*
$V_{switchC2}$ *(V)*	*0*	*3.3*	*0*	*3.3*	*0*	*3.3*	*0*	*3.3*
$V_{switchC1}$ *(V)*	*0*	*0*	*3.3*	*3.3*	*0*	*0*	*3.3*	*3.3*
V_{switch_ind} *(V)*	*3.3*	*3.3*	*3.3*	*3.3*	*0*	*0*	*0*	*0*
V_{tune} *(V)*	*0-3.3*	*0-3.3*	*0-2.1*	*0-1.75*	*0-3.3*	*0- 2*	*0-2.1*	*0-1.8*
Tuning Range GHz (Post Layout)	*5.2-4.32*	*3.4-3.77*	*4.2-3.9*	*3.3-3.41*	*2.6-2.91*	*2.17-2.35*	*2.43-2.58*	*2.09-2.16*
Phase Noise (dBc/Hz) at 1MHz offset	*(-115, -113.5)*	*(-120, -118)*	*(-120, -109.6)*	*(-123.8, -122.5)*	*(-121, -123.5)*	*(-125, -125.5)*	*(-122, -123)*	*(-126.5, -126)*
I_{vcore} *(mA)*	*2.7mA*		*8.9mA*	*12.2mA*		*11mA*	*8.8mA*	*12mA*

Table 4-4: Performance of published VCO papers in the literature

Ref.	*Technology (μm)/ Results*	*Oscillating frequency (GHz)*	*Phase Noise (dBc/Hz)*	*Power (mW)*	f_{offset}*(MHz)/*f_0*(GHz)*	*FOM*	*Area* (mm^2)
[49]	*0.13 SOI Measurement Results*	*3.065-5.612*	*-114.6*	*1V*2mA*	*1/3.065*	*-185.8*	*0.299*
			-120.8	*1V*2mA*	*1/5.612*	*-186.6*	-
[46]	*0.35 SiGe BiCMOS Measurement Results*	*2.67-4.27*	*-111*	*4V*5.8 mA*	*1/4.37*		*0.657*
[48]	*0.18 CMOS Measurement*	*2.15-2.75*	*-121.45*	*3.88V* 1.8mA*	*1/2.4*	*-180.2*	-

	Results	*4.75-4.99*	*-118.49*	*3.1V* 1.8mA*	*1/4.8*	*-184.6*	*-*
[47]	*0.35 BiCMOS Measurement*	*3.3-5.3*	*-113*	*2.5V* 14,6mA*	*0.6/4.4*	*-174.7*	*1.512*
[51]	*0.25 CMOS Measurement Results*	*3.28-4.11*	*-117*	*2.5V* 3mA*	1/4	*-180.2*	*1*
[52]	*0.18 CMOS Measurement Results*	*2.78-3.78*	*-126.5*	*1.8V* 5.7mA*	*1/2.83*	*-185.4*	*0.806*
			-122.7	*1.8V* 4.9mA*	*1/3.77*	*-184.8*	*-*
[37]	*0.35 SiGe BiCMOS Post-Layout Simulation Results (C extraction)*	*2.27-2.51*	*-122.5*	*3.3V* 6.33mA*	*1/2.51*	*-177.31*	*1.477*
		2.48-2.78	*-121.2*	*3.3V* 5.51mA*	*1/2.78*	*-178.38*	*-*
		3.22-3.53	*-121*	*3.3V* 4.38mA*	*1/3.53*	*-180.45*	*-*
		3.48-3.91	*-119.55*	*3.3V* 3.25mA*	*1/3.91*	*-181.16*	*-*
		4.528-5.7	*-110.35*	*3.3V* 2,4mA*	*1/5.7*	*-176.48*	*-*
This work Square Switch	*0.35 SiGe BiCMOS Post-Layout Simulation Results RC extraction*	*2.107-2.298*	*-122.2*	*3.3* 6.65mW*	*1/2.292*	*-175.99*	*1.477*
		2.29-2.54	*-120*	*3.3* 4.27mW*	*1/2.54*	*-176.6*	
		2.515-2.843	*-120.7*	*3.3* 3.18mW*	*1/2.515*	*-178.5*	
		2.958-3.564	*-114.2*	*3.3* 2.15mW*	*1/3.564*	*-176.73*	
		3.352-3.101	*-123.7*	*3.3* 10.6mW*	*1/3.352*	*-178.77*	
		3.379-3.727	*-120*	*3.3* 6.35mW*	*1/3.727*	*-178.2*	
		3.7-4.2	*-116.4*	*3.3* 4.27mW*	*1/4.2*	*-177.37*	
		5.321-4.492	*-117.4*	*3.3* 3.18mW*	*1/4.492*	*182.95*	
This work Square Switch	*0.35 SiGe BiCMOS Post-Layout Simulation Results C extraction*	*2.107-2.298*	*-122.2*	*3.3* 4.87mW*	*1/2.292*	*-177.34*	*1.477*
		2.29-2.54	*-120*	*3.3* 3.18mW*	*1/2.54*	*-177.89*	
		2.515-2.843	*-120.7*	*3.3* 2.15mW*	*1/2.515*	*-180.20*	
		2.958-3.564	*-114.2*	*3.3* 1.7mW*	*1/3.564*	*-177. 75*	
		3.352-3.101	*-123.7*	*3.3* 5.88mW*	*1/3.352*	*-181.32*	
		3.379-3.727	*-120*	*3.3* 4.27mW*	*1/3.727*	*-179.93*	
		3.7-4.2	*-116.4*	*3.3* 3.18mW*	*1/4.2*	*-178.65*	
		5.321-4.492	*-117.4*	*3.3* 1.7mW*	*1/4.492*	*-182.95*	

Figure 4.51: a) Phase Noise vs Vtune, b) Frequency vs Vtune c)dFrequency/dVtune for 5GHz Band

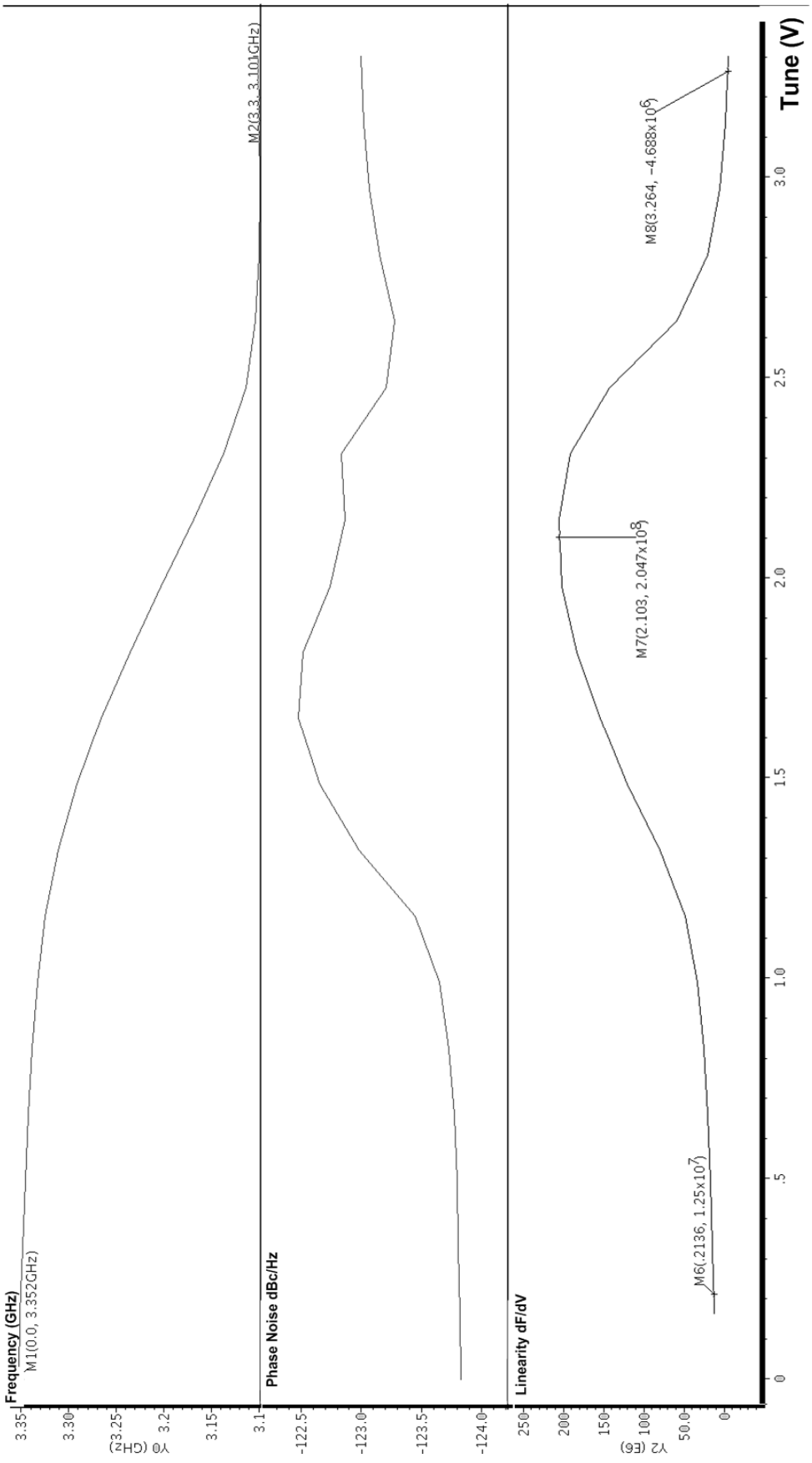


Figure 4.52: Frequency vs Vtune Behavior (left) Phase noise vs Vtune (middle) Linearity vs Vtune Behavior for SQUARE switch based circuit when all switches are on position.

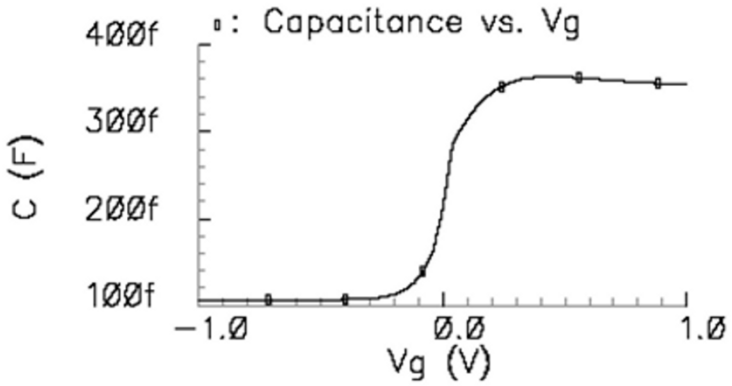


Figure 4.53: capacitance value of library varactor [37]

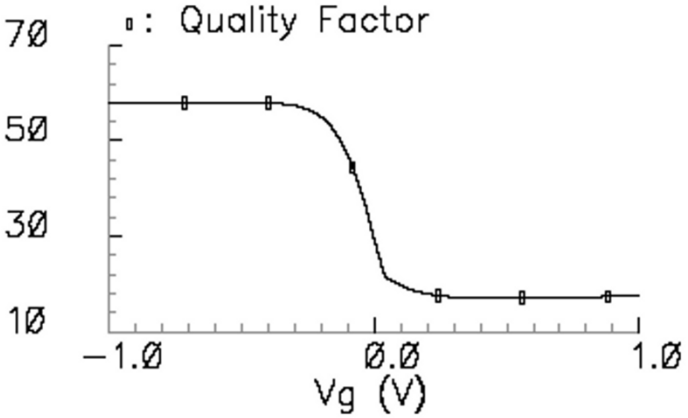


Figure 4.54: Quality factor of library varactor [37]

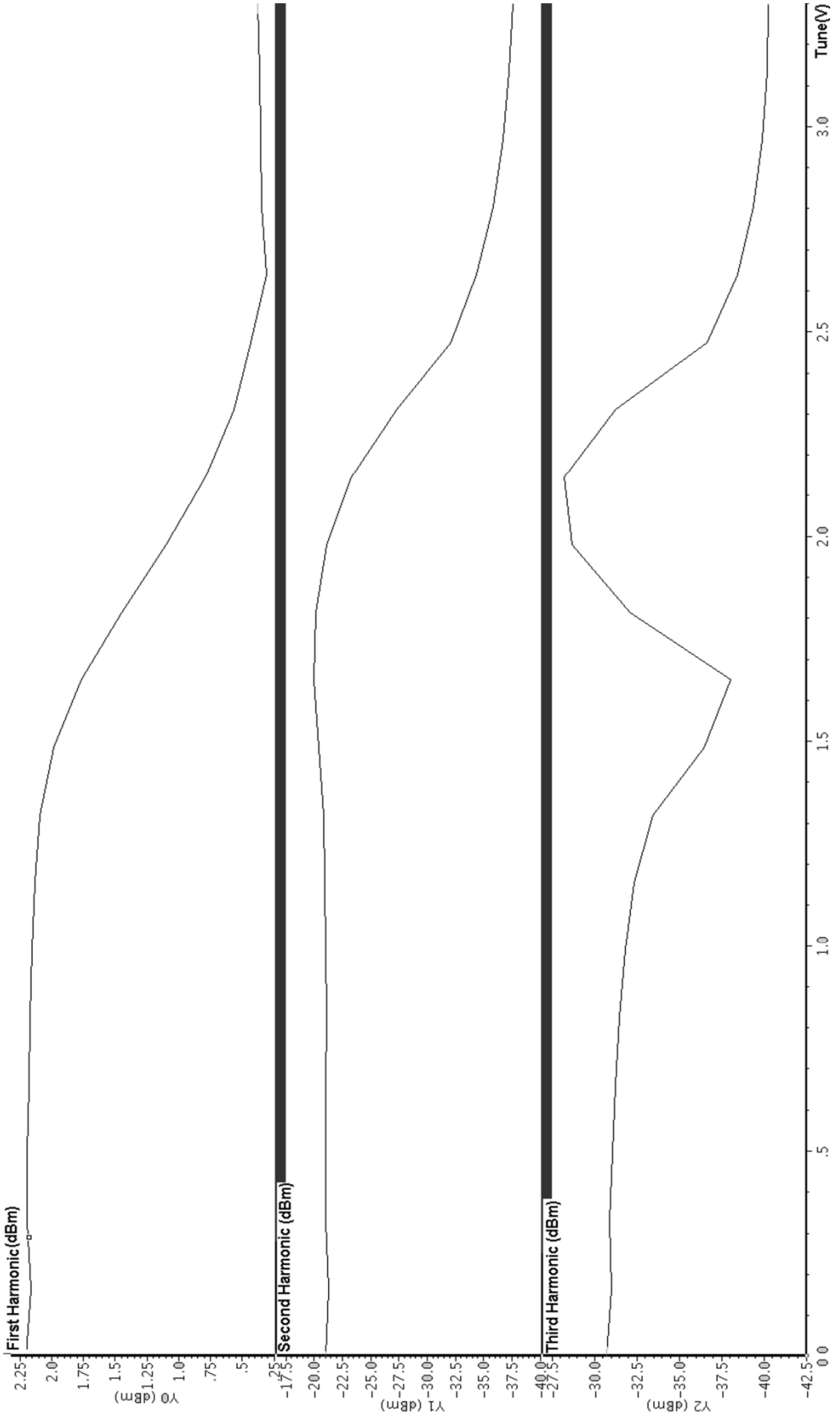


Figure 4.55: First Harmonic Second Harmonic Third Harmonic Graphics of VCO that operates 5GHz Band

5. INTEGRATION OF THE BLOCKS AT SYSTEM LEVEL

In this chapter the problems encountered at system level design are discussed. System level and simulation results are given in detail.

First of all, as stated at Chapter 4.3.5, inductor switch reduces quality factor of inductance and makes design more complex, thus, before sending circuit to fabricate, inductor switches of VCO has been removed. Thus, proposed operating bands of PLL is reduced to four bands of Table 4-2.

Secondly, if a small C2 is selected in low pass filter, such as 500fF, a signal which is at double of the operating frequency of VCO can be seen at control voltage of varactor as seen at Figure 5.1. This signal has 121mV amplitude, which corresponds to 121MHz frequency error for a 1GHz/V, VCO gain. Thus, maximum available capacitance should be used as C2.

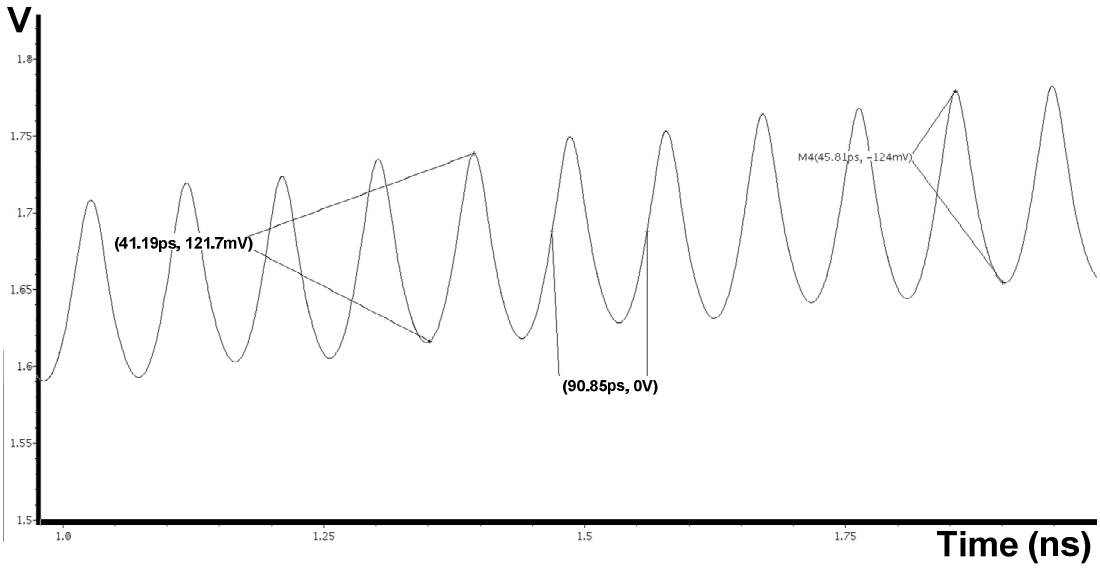


Figure 5.1: Noise at 11GHz at control voltage which is connected to varactor, for 5GHz band of VCO, if 500fF C2 capacitance is used at loop filter.

If C2 capacitance of loop filter is set to 48pF, noise voltage amplitude reduces to 2.298mV as seen at Figure 5.2. Attenuation increases with higher capacitances. However, there is an upper limit to choose this capacitance. As stated at chapter 2, if C1/C2 is 8, phase margin is 53^0 and if C1/C2 is 16, phase margin is 62^0. Thus, at least 8*C2 capacitance is needed to placed to form zero of the loop filter. To save area C1=48pF, C2= 384pF loop filter capacitances are selected at loop filter, while phase margin is set to 53^0.

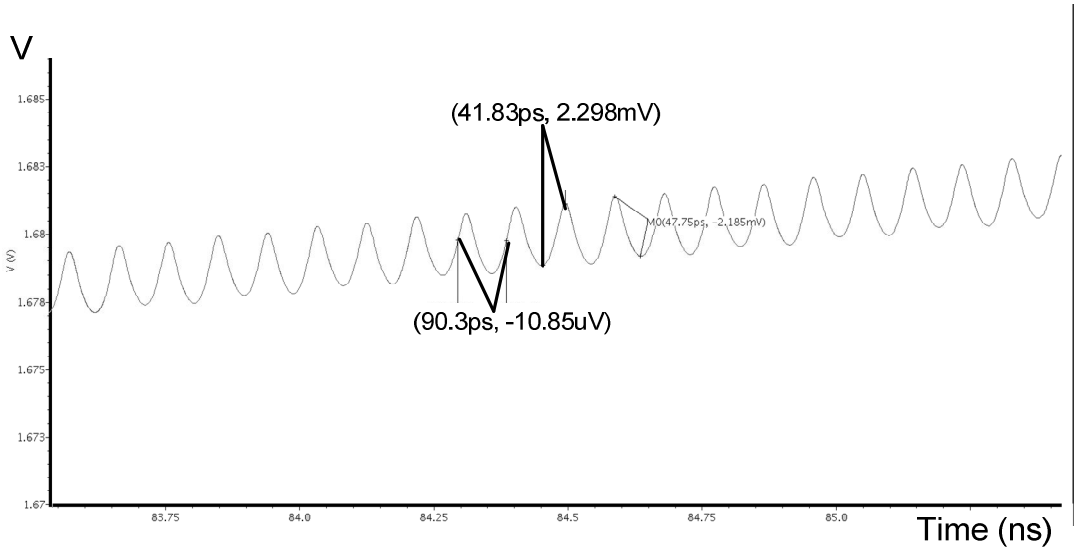


Figure 5.2:Noise at 11GHz at control voltage which is connected to varactor, for 5GHz band of VCO, if 48pF C2 capacitance is used at loop filter.

Furthermore, as stated at Chapter 4.3.2, fixed frequency divider needs a 0.5V amplitude signal as input, thus core current of VCO is increased to compensate this need.

Schematic of integrated Block diagram is at Figure 5.3, at this schematic, for simplicity, pads of the circuit and digital buffers to drive parasitic capacitances of layout are not shown.

To make measurement possible with oscilloscopes, output frequency of the VCO is divided by 16 and assigned as another output of circuit.

Settling behavior of PLL for integer N mode at band 1 is shown at Figure 5.4. This figure shows that, settling time is around 10μs. The result matches with Matlab® simulations and hand calculations. However in schematic simulations, an initial voltage is set to control voltage of VCO thus no Pull in time is needed. The difference comes from nonlinear behavior of VCO is hided with this simulation method. On the other hand, after settling is achieved, 2mV peak to peak noise which comes from VCO itself can be seen at control voltage. In addition, 1 mV noise peaks, which come from charge pump current mismatches, can be observed. The period of these peaks is 20ns, which is equal to the reference clock period.

These voltage fluctuations and phase noise VCO causes jitter, which can be calculated with eye diagram after transient analyze. Figure 5.5 shows the eye diagram which has been obtained by plot of sequential periods of output voltage for 1μs duration after settling achieved. This simulation shows us, minimum peak to peak jitter that can be obtained from this PLL is 44.56fs.

Figure 5.6 shows the settling behavior of the PLL for first order sigma delta modulator mode at band 1. According to this figure, voltage fluctuations at control voltage of VCO have increased from 3mV to 5mV. Settling time is similar to integer N mode and, small fluctuations settles after 10μs. As expected, at fractional N mode, total noise has been increased. Figure 5.7 shows the eye diagram of this system. Peak to peak jitter is calculated as 6.67ps.

Simulation results for all bands can be found at appendix. Summary has been given at Table 5-1.

Table 5-1: System level Simulation results for PLL

Mode	Peak to peak Jitter	Fluctuation Amplitude
Integer N	44.45fs	3mV
First order sigma Delta Modulator	6.67ps	5mV
First order sigma Delta Modulator	7.318ps	8mV
First order sigma Delta Modulator	22.24ps	21.8mV
First order sigma Delta Modulator	13.835ps	7mV

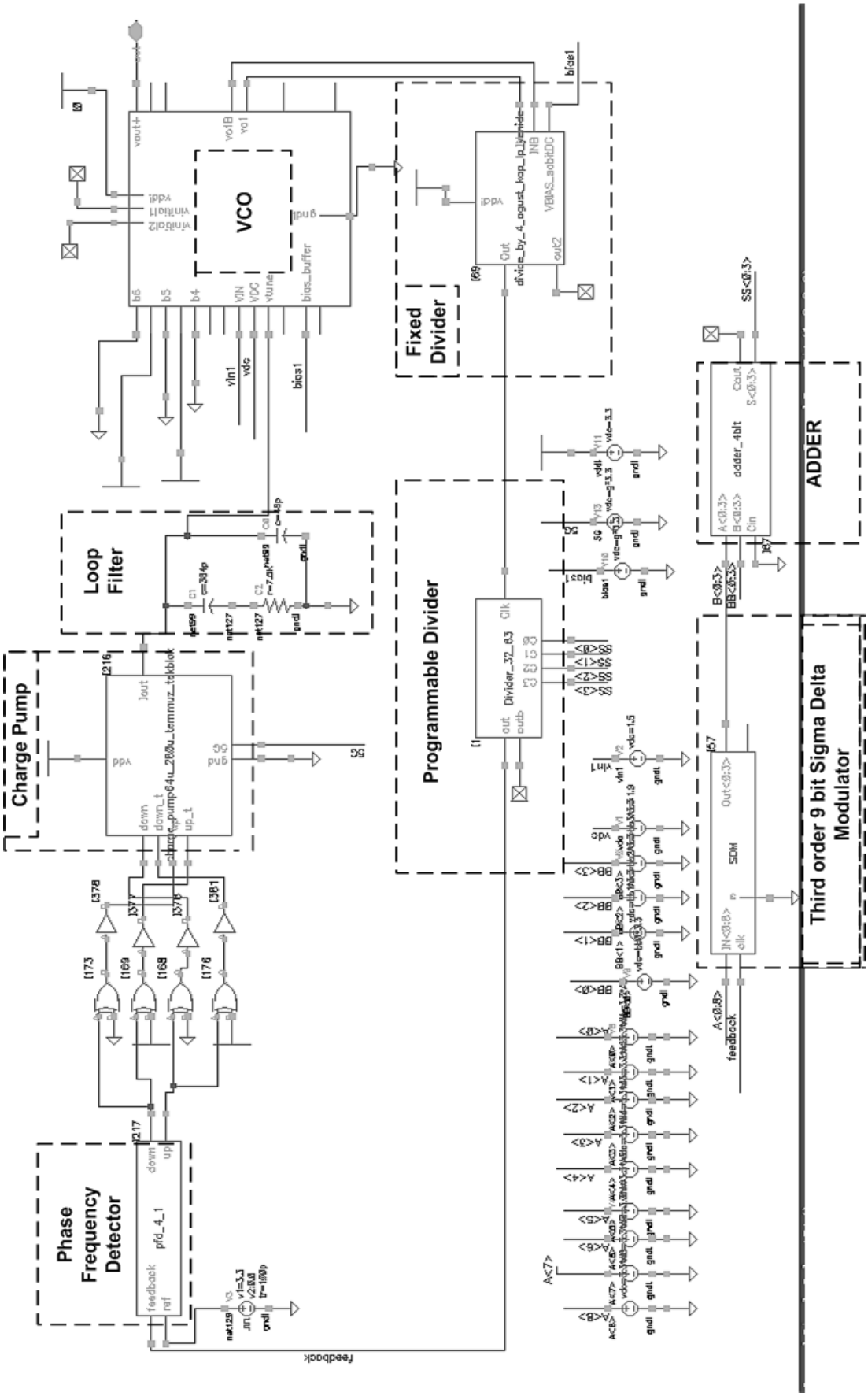


Figure 5.3: Integrated Block diagram of the system.

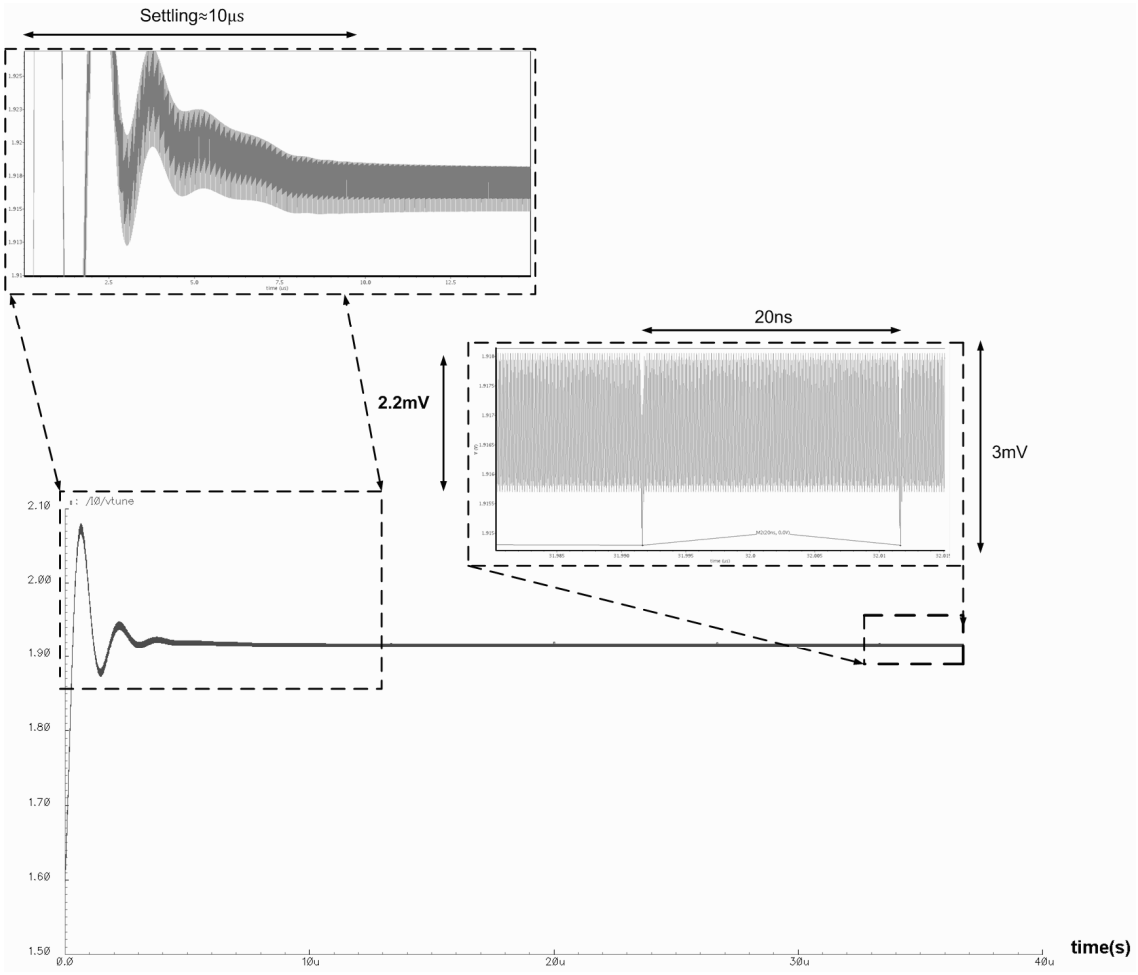


Figure 5.4: Settling behavior of PLL for integer N type at Band 1,

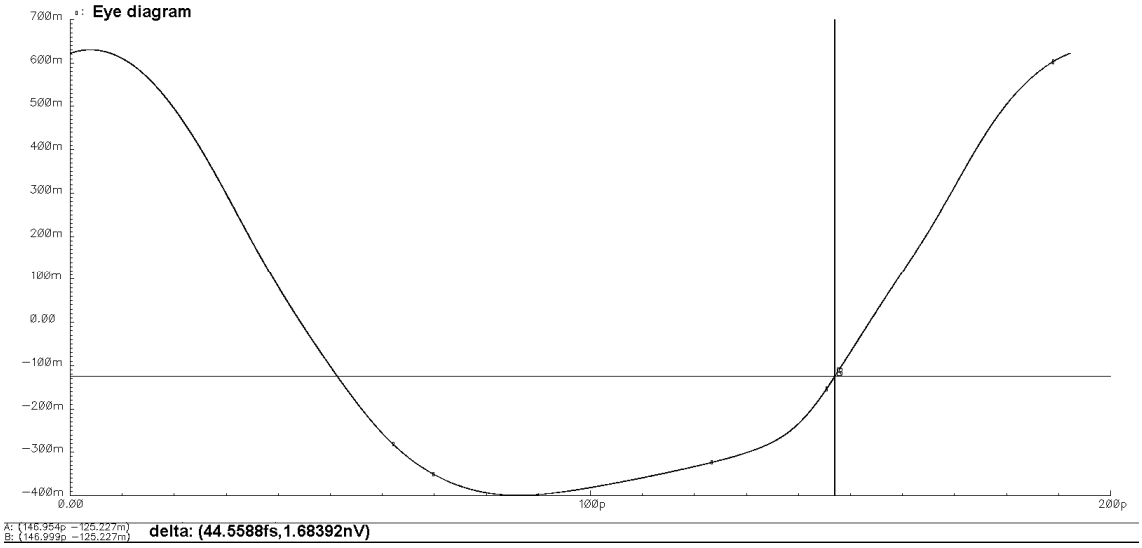


Figure 5.5: Eye diagram of PLL for integer N mode at Band 1, peak to peak jitter is around 44.56fs

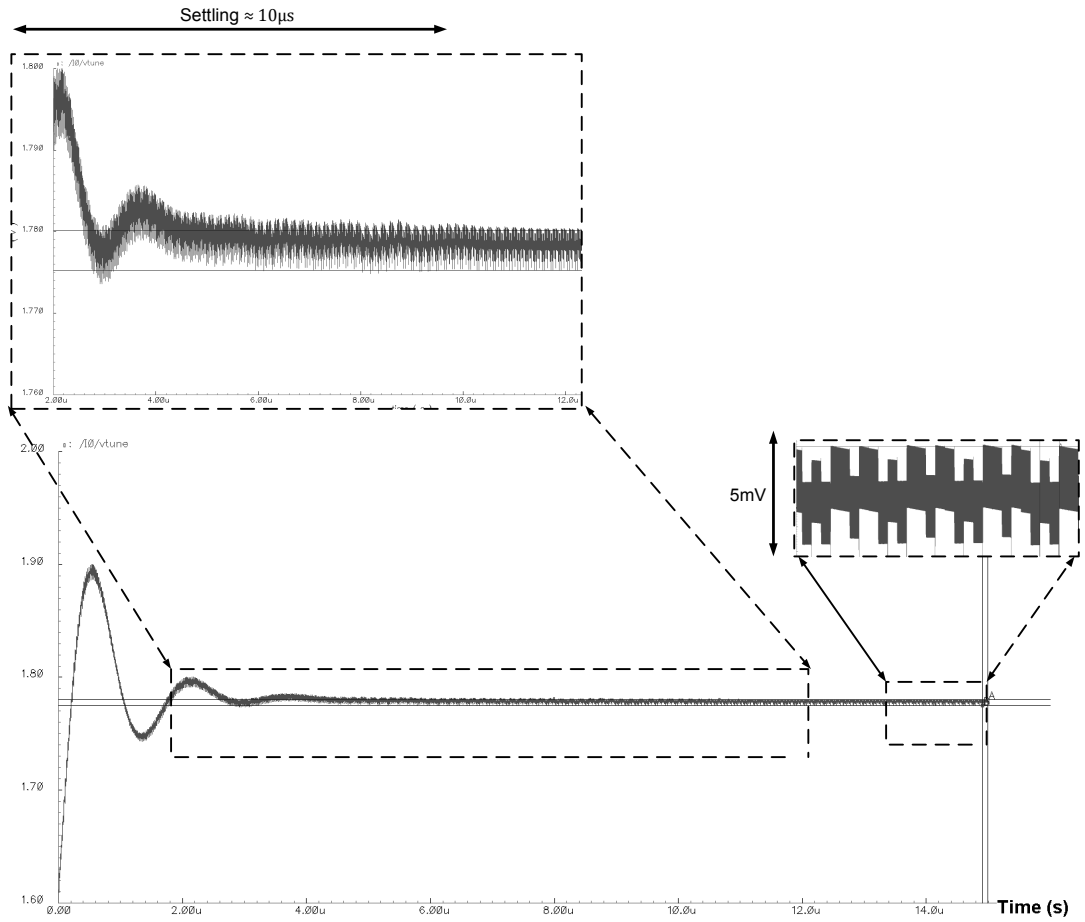


Figure 5.6: Settling behavior of PLL for First order sigma delta modulator mode, at Band 1, voltage fluctuation is around 5mV, All fluctuations settle in 10 µs

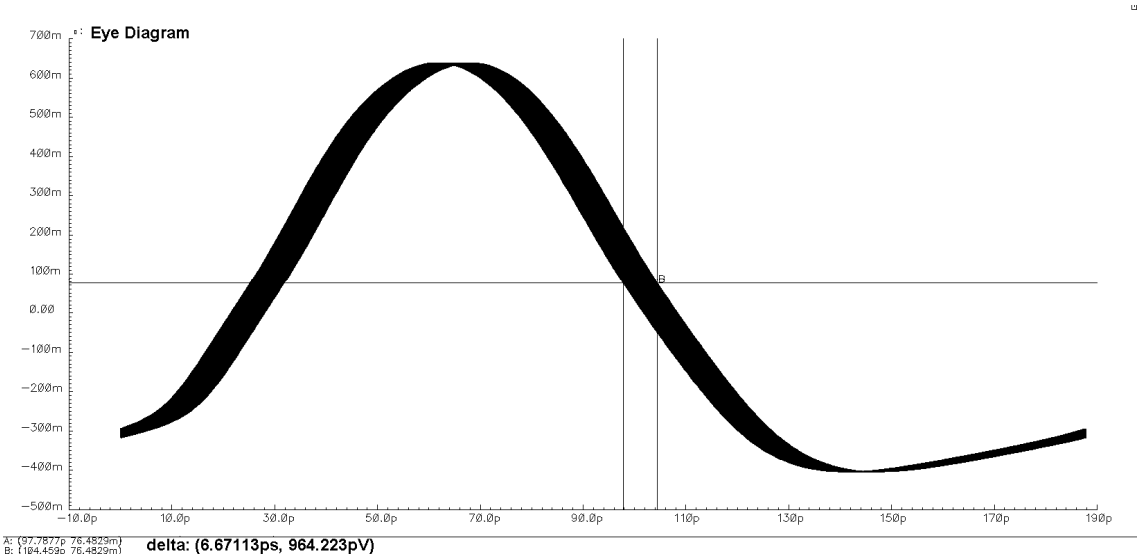


Figure 5.7: Eye diagram of PLL for first order sigma delta modulator mode. Peak to peak Jitter is 6.67113ps

6. MEASUREMENT RESULTS & POST MEASUREMENT ANALYZES

Boards at Figure 6.1 have been designed with Eagle 4.15 program, to measure VCO's and PLL's. Measurement station is shown at Figure 6.2, Figure 6.3 and Figure 6.4. ,

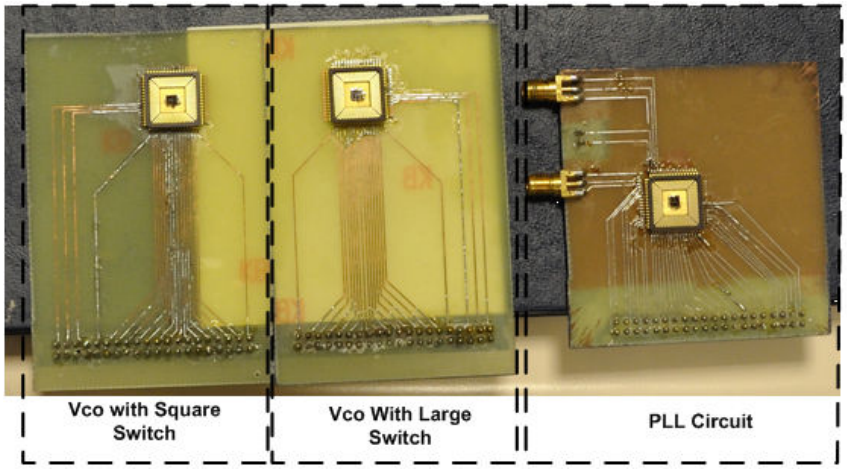


Figure 6.1: Boards for measurement

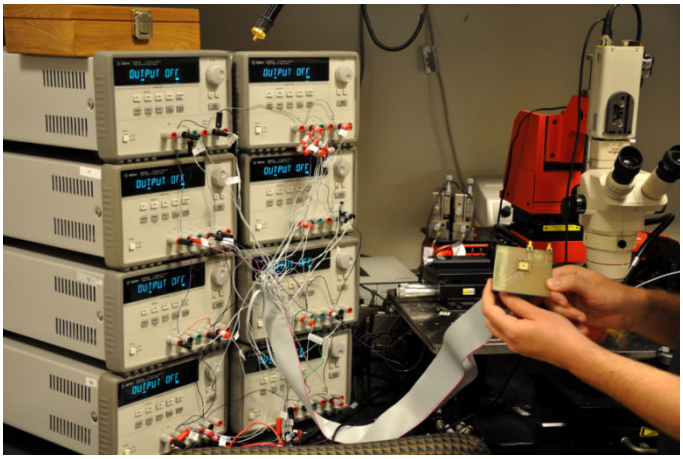


Figure 6.2: Board is connected to power supplies via 40 pins IDE cable. All of the pins are used during measurements

Measurements are started with VCO. In three of eight bands, band 5 (*2,747-3,184GHz*) band 6 (*2.48-2.78GHz) and band7 (2,747-3,184GHz)*, oscillation is achieved for SQUARE switch method. In one of eight bands, band 1 (5,36GHz), VCO with LARGE switch oscillates. One sample of measurement from each band can be found at Figure 6.5 to Figure 6.8.

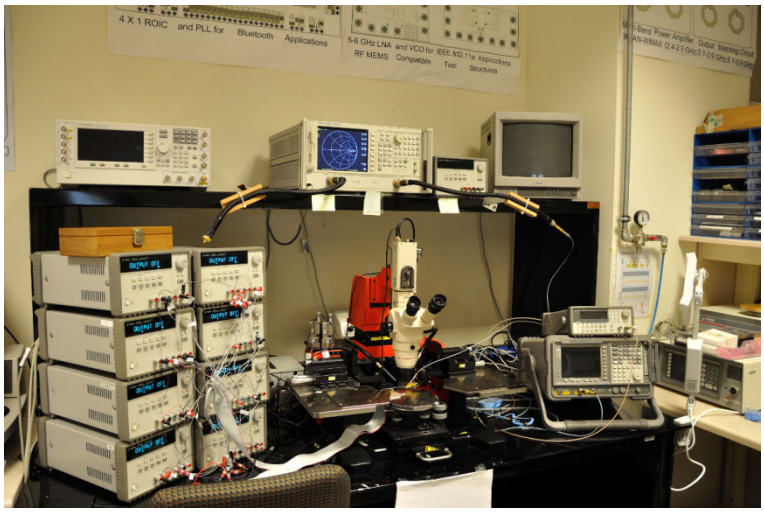


Figure 6.3: measurement station

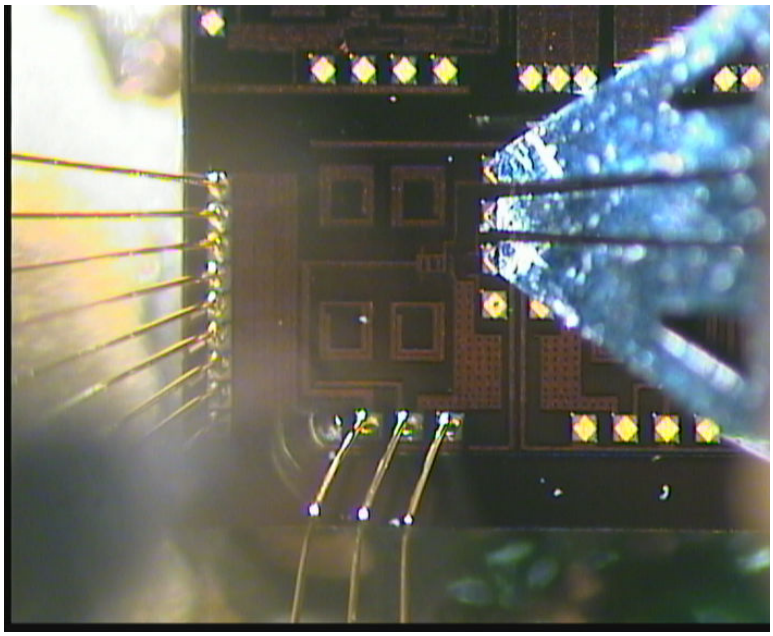


Figure 6.4: Fabricated chip

From the summary of measurements which is located at Table 6-1, it can be seen that, core current requirement is more than expected from simulation results. The reason of this handicap is mutual coupling, which is explained in detail at post measurement analyzes part of this chapter.

In order to compensate core current requirement, supply voltage of oscillator can be increased to 4V. This increase will not break PMOS of –Gm circuit and oscillation can be obtained. If we

return to Figure 4.45, Drains of PMOSs are connected to 1.9V and Sources are connected to drain of current mirror. Source voltage of PMOSs can be maximum VDD-Vov. Thus, VCE voltages of PMOSs will not exceed break down limits. However, output buffer is broken and oscillation amplitude is reduced. It can be seen that, measured oscillation amplitude is very small. This problem is caused by break down of output buffers (At band5 supply voltage is 3.3V, but the output of chip is already broken down when Figure 6.5 is taken). After break down of output buffer, signal has found a pathway made up of capacitances to output.

Due to the increase of core current, junction capacitances of MOS transistors are also increased, which has shifted operating frequency down. In addition, because of mutual coupling, the inductance values are also increased and operating frequency is shifted down. Due to large core current, measured phase noise is better than post layout simulations.

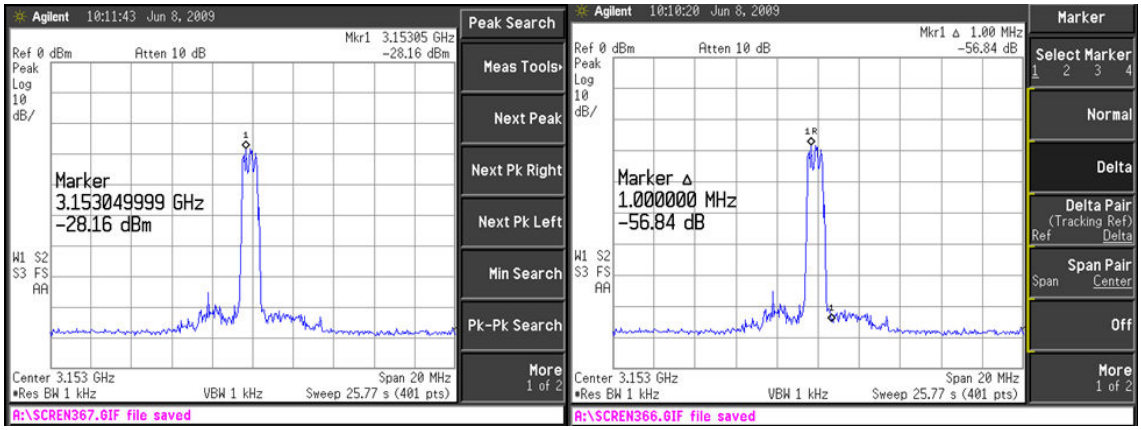


Figure 6.5: Measurement Results of Phase Noise For band 5 (SQUARE switch)

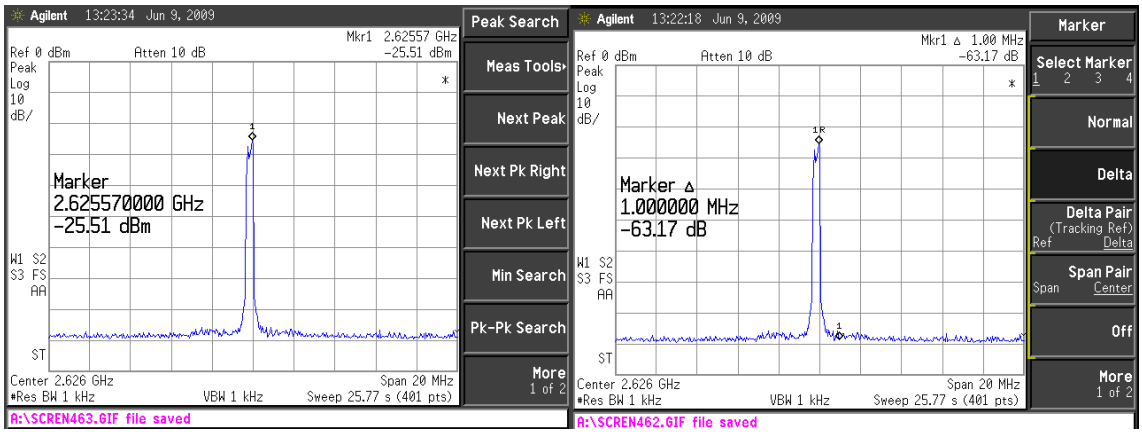


Figure 6.6: Measurement Results of Phase Noise For band 7 (SQUARE switch)

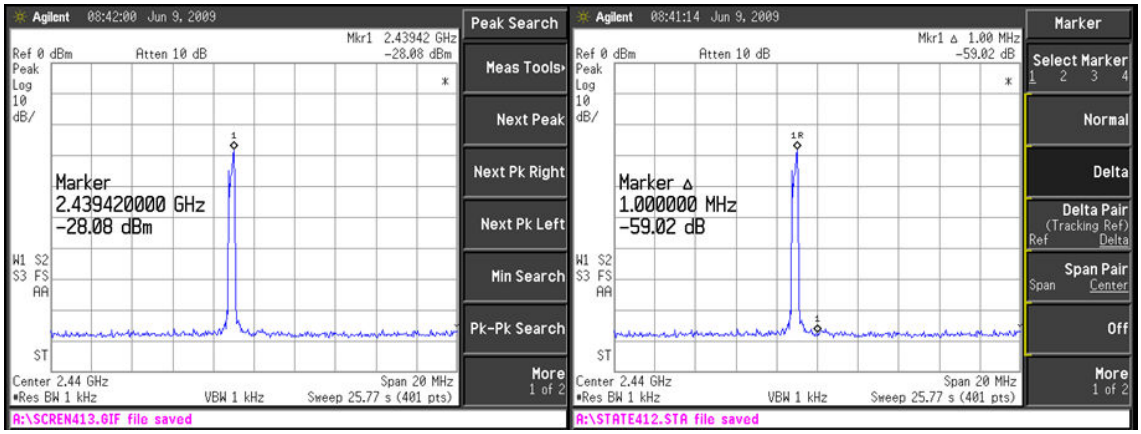


Figure 6.7: Measurement Results of Phase Noise For band 6 (SQUARE switch)

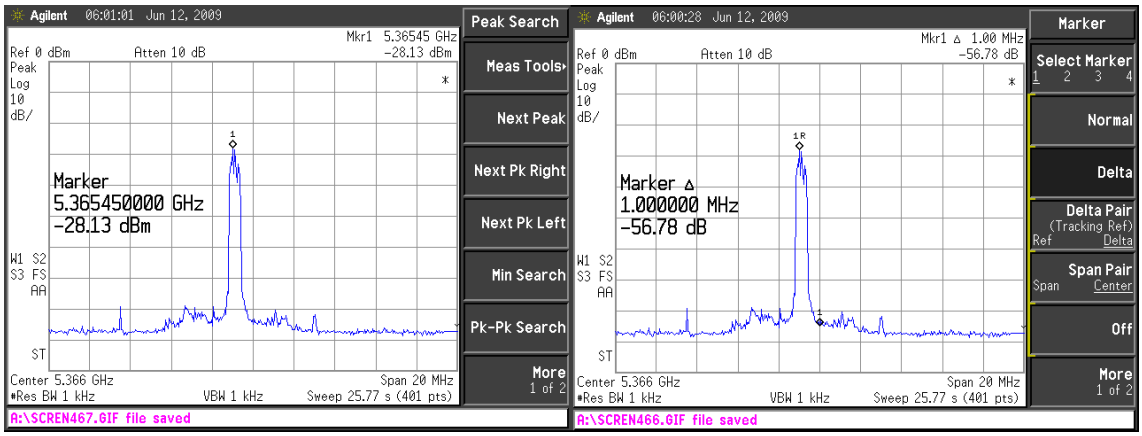


Figure 6.8: Measurement Results of Phase Noise For band 6 (SQUARE switch)

Table 6-1: Measurement Results for VCO

	Band 6(SQUARE switch)	*Band 7(SQUARE switch)*	*Bant5(SQUARE switch)*	*Bant1(LARGE switch)*
$V_{switchC2}$ *(V)*	*3.3*	*0*	*0*	*0*
$V_{switchC1}$ *(V)*	*0*	*3.3*	*0*	*0*
V_{switch_ind} *(V)*	*0*	*0*	*0*	*3.3*
V_{tune} *(V)*	*0- 3.3*	*0-3.3*	*0-3.3*	*0*
Frequency range (GHz)	(2.48-2.78)	(2,6255-2,98983)	(2,747-3,184)	5,36
Phase noise Range (dBc/Hz)	(-115.1, -125.4)	(-115.0, -123.87	(-113.28, – 124.57)	-116,78
Vdd (V)	*4*	*3.5*	*3.5*	*3.3*
I_{Core} *(mA)*	*19*	*12*	*6*	*4*

SQUARE switch is only working at off state and LARGE switch is only working at on stage. The reason of this problem has not been clarified yet, and the designer is still working on this problem.

Measurement results of SQUARE switch are plotted at Matlab®. For SQUARE switch topology, and conditions for band 5, frequency versus Vtune, Phase noise vs Vtune and Phase noise vs Frequency plots are located at Figure 6.9, Figure 6.10 and Figure 6.11. As seen from Figure 6.9, frequency change behavior of the circuit is identical with capacitance change behavior of varactor with respect to control voltage change. At middle frequencies, phase noise increases because quality factor of varactor decreases at these voltages. For other bands, similar curves are located at appendix.

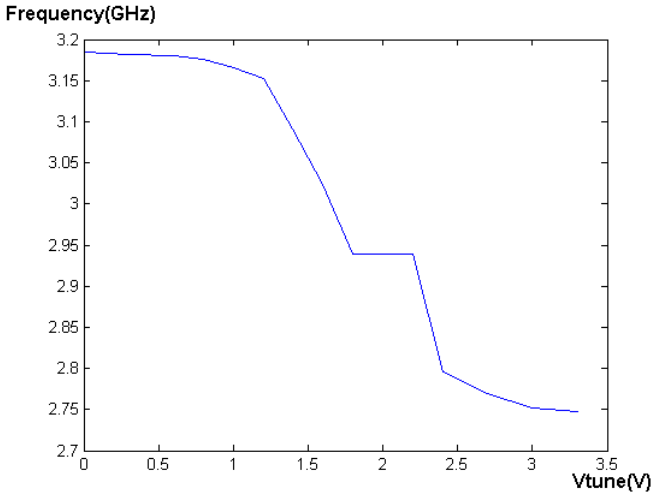


Figure 6.9: Frequency Vs Vtune graphic for Band5 of SQUARE switch based VCO

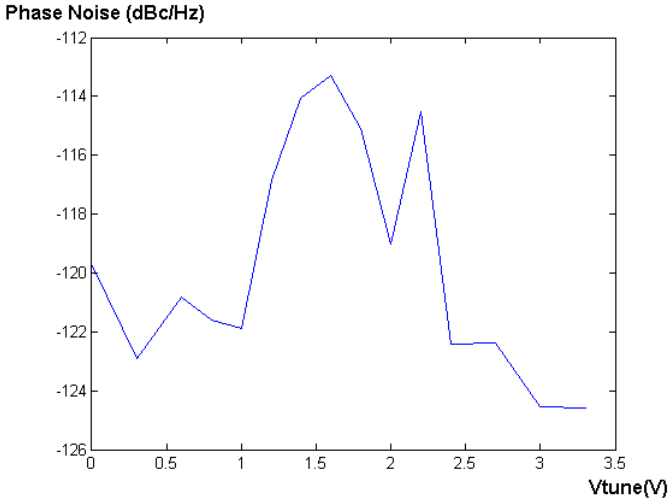


Figure 6.10: Phase Noise vs Vtune graphic for band 5 of SQUARE switch based VCO

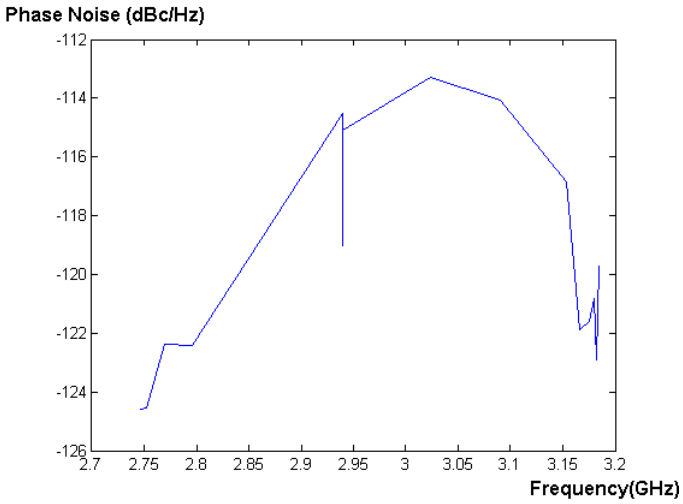


Figure 6.11: Phase Noise vs Frequency graphic for band 5 of SQUARE switch based VCO

Output of PLL can be seen at Figure 6.12. VCO of PLL is producing output at sufficient power level in only band 1, thus, PLL is working at this band only. During this measurement, accumulator value is set to zero and division value of programmable divider is set to 25, thus PLL is operating at integer N mode. As seen from this figure, output of power VCO is 3.864 dBm which is sufficient for frequency dividers. On the other hand, there are some spurs located at 50MHz offset frequencies from output. Because of operating at Integer N mode, the only noise source is charge pump current mismatch which increases phase noise of VCO, (as explained at chapter 4.1).

Output frequency of VCO is divided by 16 and set as another output of PLL. Divided output of PLL is shown at Figure 6.13. These figures are sufficient to see that all components of PLL are working, (at least one band) and loop is stable.

From these figures, it can be seen that, noise levels are very high. During measurements of PLL, reference frequencies are taken from a signal generator which has a phase noise which is represented at Figure 6.14. As seen from the equation (2.26), noise at reference input of PLL is multiplied by the frequency division value and seen at output. Thus, noise level of the circuit is determined by reference input. In measurements a better reference input can be determined by crystal oscillators.

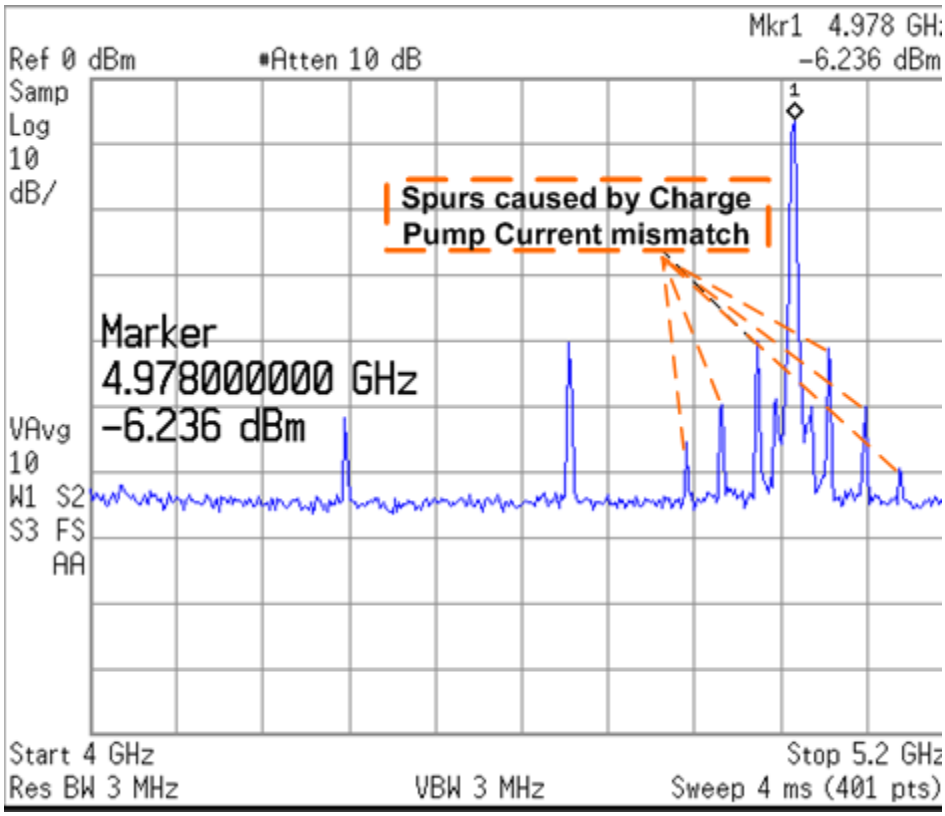


Figure 6.12: Measured Output of PLL, operating at integer N mode, Programmable divider division value is 25. Spurs are located 50MHz offset frequencies which is equal to reference frequency. These spurs are caused by charge pump current mismatch.

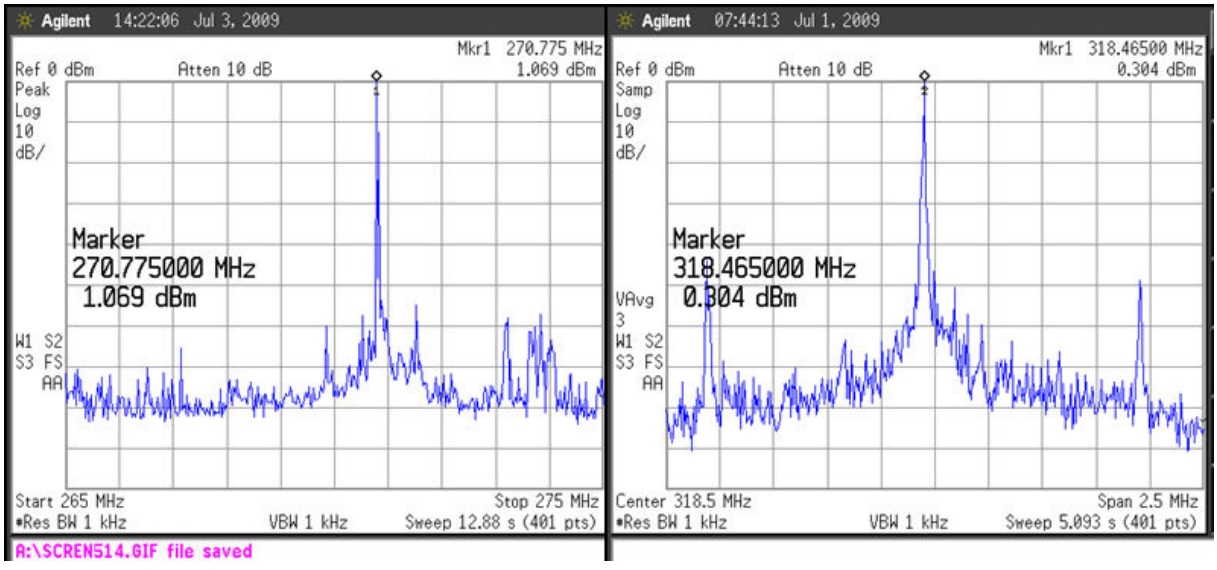


Figure 6.13: Divided output of PLL (divided by 16) which is operating at 4.332 GHz (left) and 5.095 GHz (right)

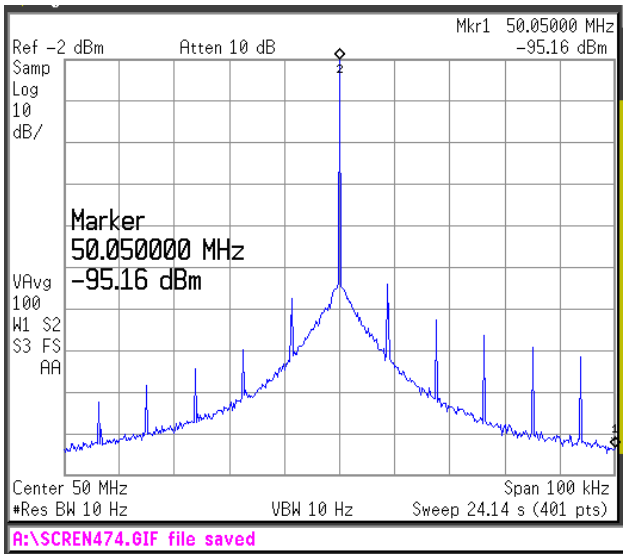


Figure 6.14: Phase noise of reference frequency of PLL

Figure 6.15 shows us full operating range of PLL, which is from 4.261GHz to 5.098GHz. Programmable divider and accumulator operation can be seen from this figure.

PLL and VCO are not working in all proposed bands and frequencies. Thus, electrical analyzes done by Cadence® are insufficient and electromagnetic analyzes are needed to be done. These analyzes are explained at chapter 6.1.

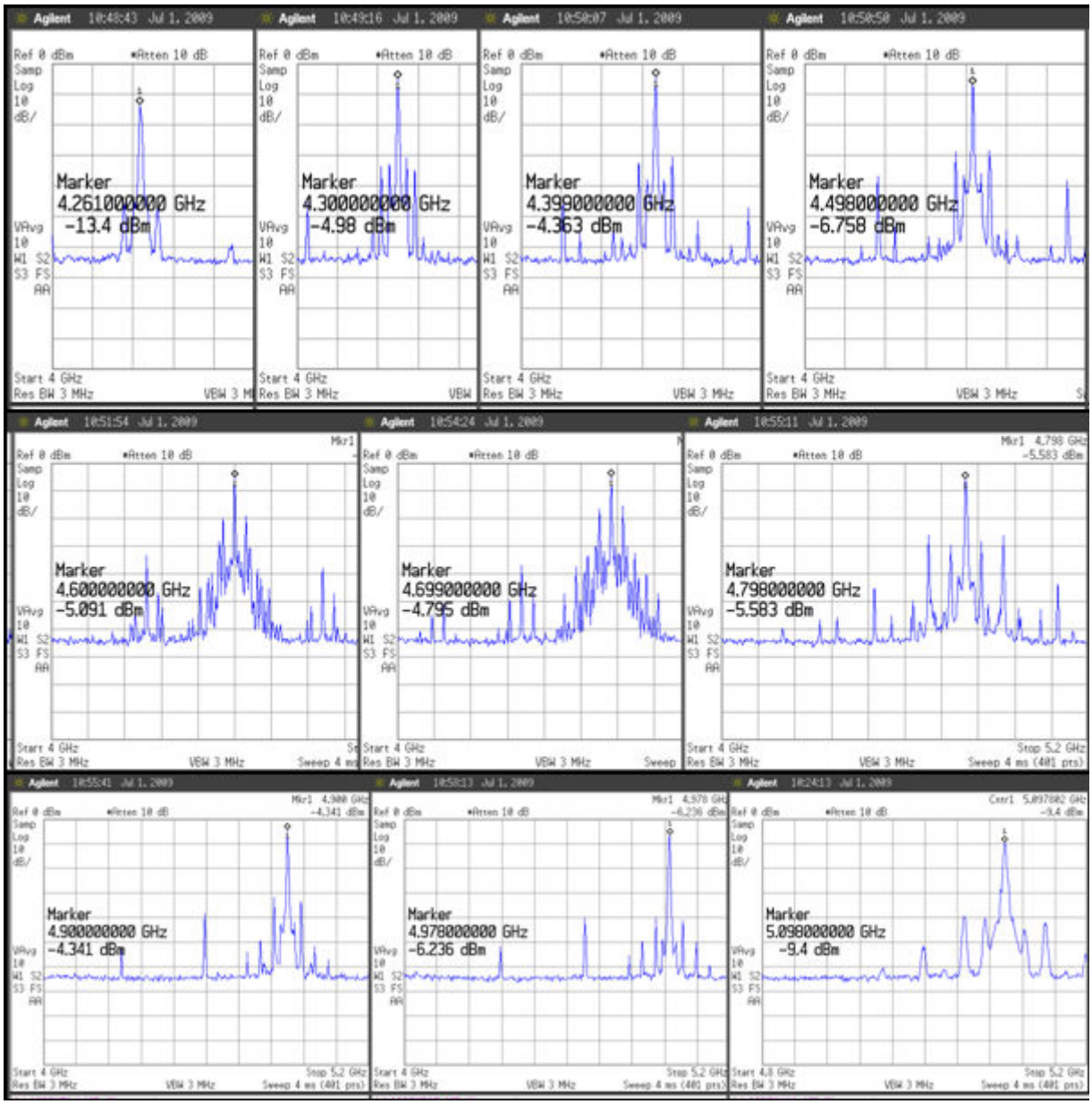


Figure 6.15: Output range of PLL is from 4.26GHz to 5.1GHz. At this figure frequency divider (and accumulator) is programmed to show full range at 100MHz steps.

6.1 Post Measurement Analyzes

Analysis of the system is continued, because the measurement results do not match with post layout measurements. Most important reason of the mismatch is mutual coupling between the inductances of VCO. If the mutual coupling in the layout results in quality factor decrement or inductance changes, oscillation frequency of the tank is affected. If the quality factor decreases, more -Gm will be needed to compensate the losses of the LC tank. Also change in the inductance value will result oscillation frequency shift. The reasons of all these effects can be understood with inductor coupling analysis tools like ADS® Momentum.

In order to analyze inductors, firstly inductor layouts are taken from Cadence® Virtuoso® to ADS® layout. For this step, Cadence® layout is converted to a GDS format and this file is opened in the ADS® layout with suitable Substrate file and Layer after this step, inductor layouts are simulated with ADS® Momentum® tool.

There are several inductance and quality factor formulas used for inductor analysis in the literature. Because these parameters are tried to be calculated from S-parameters of the structures, each approach results in different characteristics of inductors. For the single (one arm of the inductor is RF-grounded) inductor simulations, Ls (see in Figure 6.16) formula for inductance, and Qs formula for the quality factor is used. In addition, because the inductors are investigated for VCO design, differential inductance and quality factor also will be used.

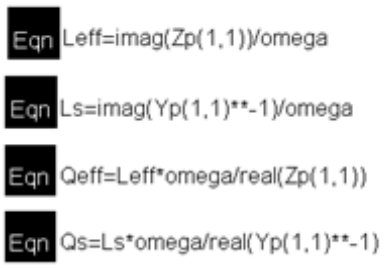


Figure 6.16: Formulas used in simulation results

For these simulations, there are several different substrate files from IHP® technology and AMS® technology. The AMS® substrate file is created according to their substrate thicknesses and conductivity of the metals from the process documents. However, the simulation results and AMS® measurements of the inductors are not very well matched. Therefore, IHP® substrate and TopMetal-1 is used for simulations because this substrate file is also used in IHP® Foundry itself. Therefore the inductance values are nearly same as AMS® measurements but the quality factors are not similar. However, the percentage of change at quality factors, gives us the information about inductors of AMS®. All the simulation results are done in IHP® substrate with

a real via values. These simulations will be helpful for understanding how mutual coupling between inductors can make VCO design depended on Electromagnetic simulations.

First of all, single inductor, which can be seen at Figure 6.17, is analyzed to see behavior of inductor without coupling.

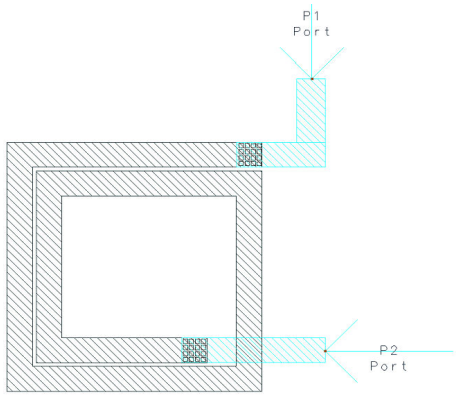


Figure 6.17: 1nH AMS® library inductor

The results of the simulation, which is represented at Figure 6.18, show that this inductance has 11.2 quality factor in 4.1GHz and nearly maximum 15 quality factor at 8GHz frequency. The inductance value is approximately is 1.015nH

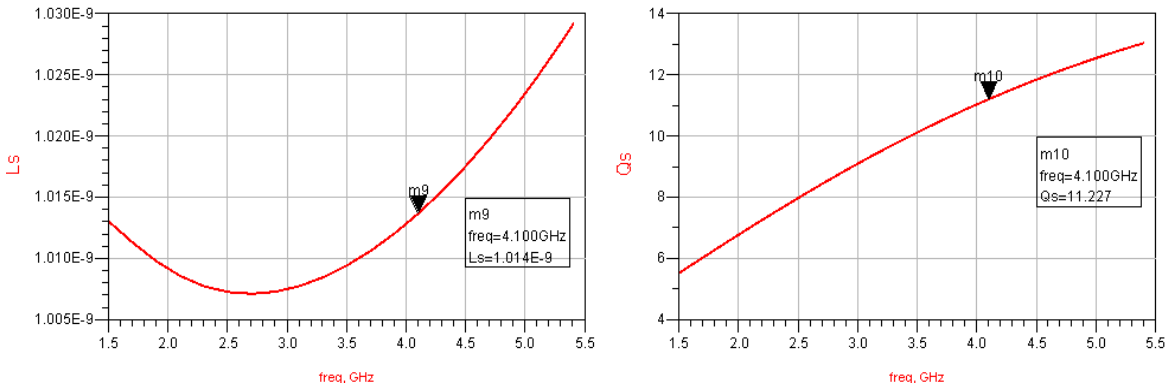


Figure 6.18: Inductance and quality factor simulation result for single inductor

Two branches of the whole inductor structure, as can be seen in Figure 6.19, are not symmetrical because of inductance switches of VCO. This difference can result these branches to have different quality factors. Therefore, first left branch is simulated. The results of the simulation show that the left branch has a quality factor of 7.6 at 4.1GHz which is nearly maximum quality factor and the inductance of 2.04nH. This analysis shows that mutual coupling between these two branches decreases quality factor of the whole structure from 14 to 7.6. The inductance value is nearly same.

The inductance group, which is shown at Figure 6.21, is simulated and results are shown at Figure 6.22. As it can be seen in Figure 6.20 and Figure 6.22, there are differences between

quality factors of two branches. One has a quality factor of 7.6 and the right one has a quality factor of 8.7 at 4.1GHz. Also right branch has higher maximum quality factor than left one. The inductance values of these branches as nearly same.

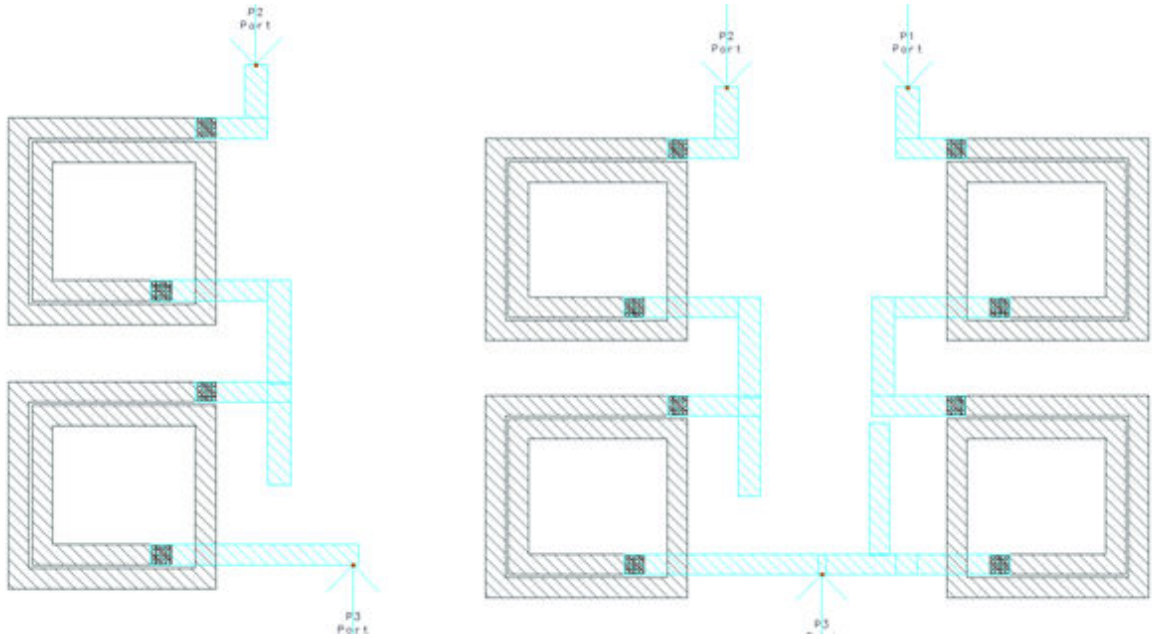


Figure 6.19 : Four 1nH inductor group (right), and left half of this group (left)

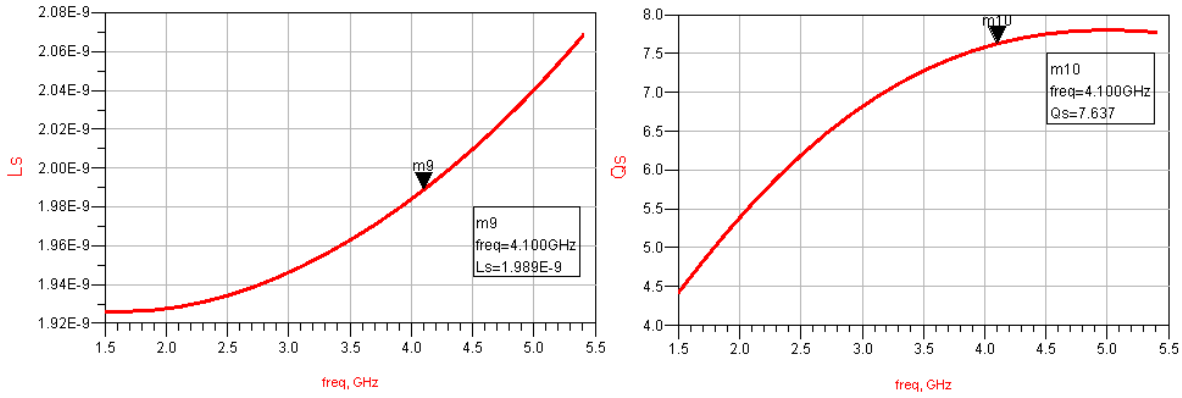


Figure 6.20: Inductance and quality factor simulation result two inductor group at Figure 6.19(left)

As stated at chapter 5, VCO, which is used at PLL, has two inductors. Inductor switch is removed from PLL. Final inductor is shown at Figure 6.23. Simulation results for this group which is represented at Figure 6.24, shows us Quality factor of inductance is 10. 213, while total inductance value is increased from 2.030nH (2 times of the value at Figure 6.18) to 2.179nH. Thus, inductance of the tank changes 7.5%, and maximum frequency at Table 4-2, 5.321GHz, will be shifted to 5.132 GHz.

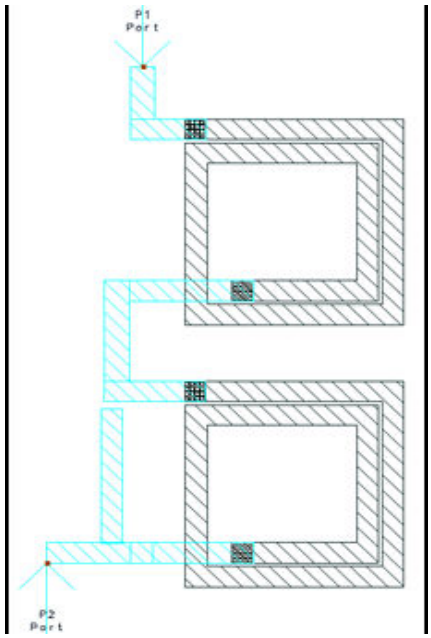


Figure 6.21: Two inductor groups at right hand side of four inductors at VCO layout.

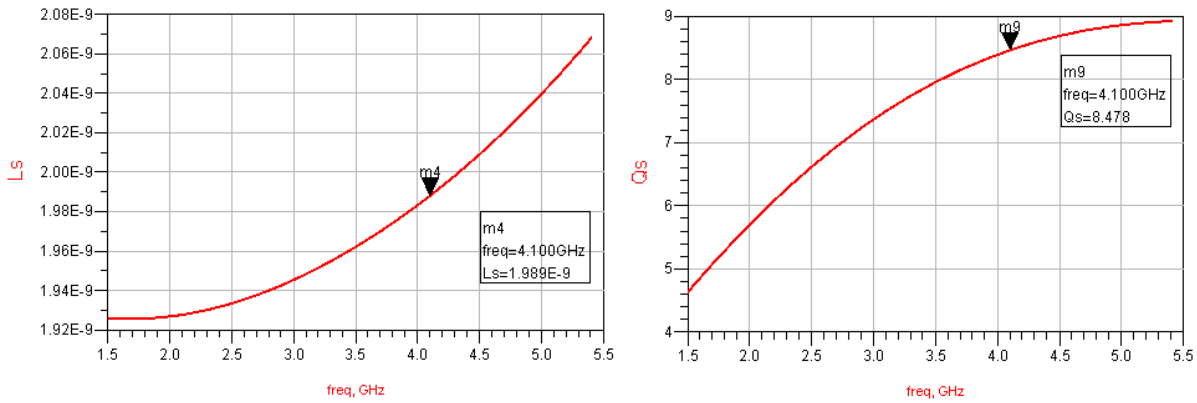


Figure 6.22: Inductance and quality factor simulation result two inductor group at Figure 6.21Figure 6.19

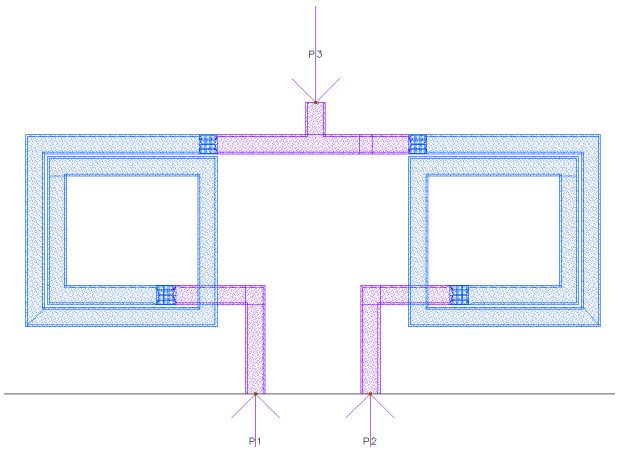


Figure 6.23: Two inductor groups which are used at VCO of PLL.

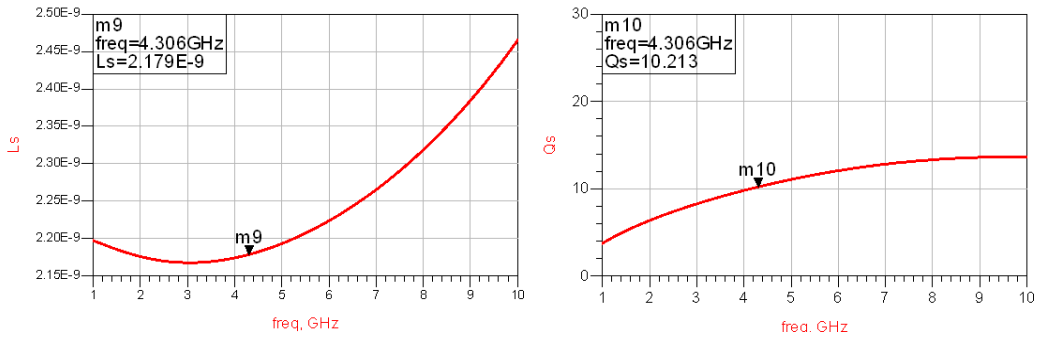


Figure 6.24: Inductance and quality factor simulation result two inductor group at Figure 6.21Figure 6.19

The whole structure which is shown at Figure 6.19 is analyzed for inductance and quality factors. As seen from Figure 6.25, the quality factor of inductance is 8.232, and total inductance of four inductors is 4.285nH, which is 5.4% different from expected.

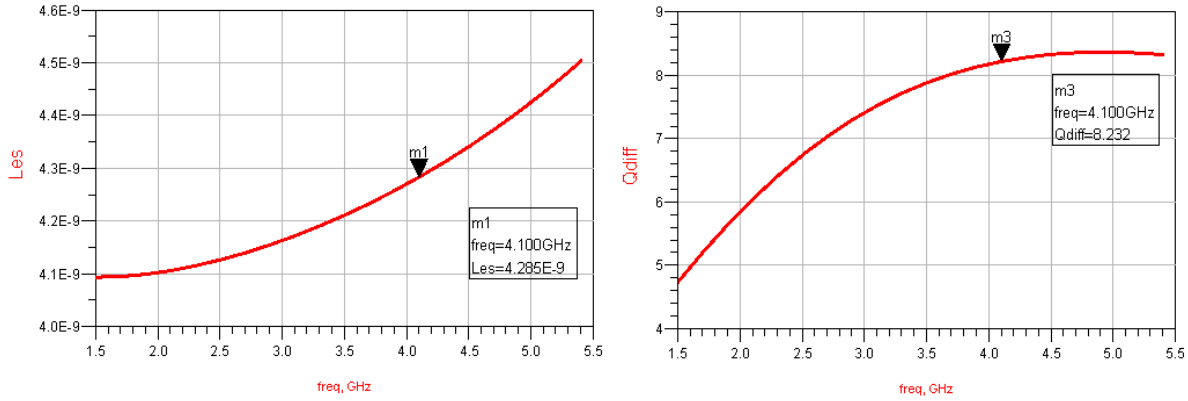


Figure 6.25: Inductance and quality factor of the whole structure

These electromagnetic analyzes shows us that, the quality factor of inductance is decreased from 11.227 to 8.232. Thus, parallel parasitic resistance of inductance is decreased as,

$$R_P \approx \frac{L1^2\omega^2}{R_S} = Q_{L\_after\_mutual\_coupling}^2 R_S = (0.733Q_L)^2 R_S = 0.537Q_L^2 R_S$$

To compensate this loss, gm of –GM circuit must increase 1.86 times. For transistors at the same size, core current must be 3.5 times of post layout results. VCO requires 3.5 times of the core currents which are summarized at Table 4-1 and Table 4-2. Because of insufficient core current and inductor switching problem which is not clarified yet, VCO is operating at three bands rather than eight bands.

7. CONCLUSION and FUTURE WORK

7.1 Conclusion

In this thesis, a 4.3-5.1GHz frequency synthesizer and Multiband VCO which operates at 2.48-3.2GHz and 3.9-5GHz are implemented in 0.35µ BiCMOS technology. During the thesis, RF integrated circuit design, Digital IC design, analog IC design and mixed signal IC design techniques are applied.

Operating frequencies and specifications such as phase noise, current consumption, and tuning range are obtained from published papers, IEEE standard documentations and Wimax forum documents.

Three different and complex modeling and simulation tools are used at this thesis. Analyzes have started from Matlab® level. System level simulations at Matlab®, match with hand calculations and post layout simulations at Cadence®. First designs of loop components are done at Simulink® and trade offs for of each block is covered in this faster design environment. Every block at loop is searched in detail and design is optimized at Cadence®, at transistor level. Layout of each block is designed with full custom methods, and optimized in considerations such as area, parasitic resistance and capacitance. Post layout simulations are done including both RC extraction and C extraction files. The finalized circuit is sent to fabrication, after measurements post measurement analyzes are done at ADS®.

Multiband and multi standard operation of frequency synthesizer is achieved by switched inductor and capacitors at VCO stage. A new idea for inductor switching is introduced and performance is compared by conventional inductor switch. With this idea, performance of circuit at [38] is improved in terms of phase noise, core current and FOM. More frequency

bands are covered despite reduces at capacitor switches. Layout problems of the circuit at [34] which could kill oscillation have been solved. Oscillation is measured for both of the VCO's, however, they are not covering all of the proposed bands and consuming much more current than expected from post layout analyzes. Post measurement analysis at ADS® shows us that, mutual coupling between the inductances at VCO decreases quality factors dramatically which increases core current. In some bands needed core current is not obtained and oscillation is killed for these bands.

In addition, for multiband operation, a fully programmable 4 bits multimodulus frequency divider circuit (division ratio can be programmed in the range between 16 and 31) which operates at 2GHz is designed. The operating frequency is prescaled by a current mode logic based frequency divider which operates at 6GHz. This prescaler has a stabile DC level which is less dependent from temperature at output. Compatibility between these different frequency dividers is also obtained by additional blocks.

Cascode technique is implemented to charge pump to decrease current variations at output current due to the output voltage. This technique was limited the output swing of circuit, which corresponds tuning range of VCO. To overcome this challenge a biasing technique is applied to this block which provides an output swing between 0.3V and 3V which is a sufficient range. Other blocks, such as VCO and fixed frequency divider are consuming high current which can increase the temperature of the circuit. In addition, output states of these blocks are changing at high speed that can produce power supply noise. Output current of this charge pump block was highly dependent to temperature and power supply noise. To decrease dependency of this block to these parameters, band gap reference circuit is used at biasing. Finally a high output swing CMOS cascode charge pump with band gap reference circuit is designed to produce output current independent from power supply noise, temperature and output voltage.

In order to obtain fractional frequency division, first order and third order sigma delta modulators are implemented. Mash 1-1-1 topology is implemented as third order sigma delta modulator, to decrease quantization noise at output. However stability could not be achieved by this block. The reason is high frequency variation at output frequency due to three bits output of this block. Fractional division is achieved by first order sigma delta modulator, and system is stable for this mode.

System level simulations resulted that PLL has a good jitter with reasonable power consumption despite the technology limitations, and the chip is sent to fabrication.

Measurement results show us that proposed frequency synthesizer is working with all blocks at least for one frequency band. For other proposed frequency bands, mutual coupling has decreased quality factor and killed the oscillation at VCO stage.

Thesis is finalized with ideas about improvements that can be done to enhance performance of the system.

7.2 Future Work

From fabrication up to the time this thesis is written, some ideas are developed. In this chapter these ideas are introduced.

First of all, rather than common collector buffers at VCO design, common emitter amplifiers should be selected to save current and produce better power level at output stage. At this amplifier stage an inductance can also be used to provide a better matching and power level at output.

Secondly, as a conclusion of post measurement analyzes, the layout of the circuit must be re-designed with mutual coupling considerations. The inductances should be selected as differential, or a differential inductance with four ports can be designed with inductance design tools. In addition, layout of core of VCO can be redesigned with a better symmetry and smaller parasitic capacitances at oscillation nodes. PMOSs which form –Gm circuit, can be merged in a single transistor at center and common collector buffer transistors (or common emitter amplifiers) should be at corners. Core circuit and capacitance switches should be far enough from inductances of voltage controlled oscillator.

Thirdly, order of Sigma Delta modulator of the circuit can be designed as programmable as shown at Figure 7.1. The modification can be done such easy that, only two AND gates are added to the feedback path and multiplexers at output stage can be removed. If both enable values are one, the system will be MASH 1-1-1. Else if the logic level at enable2 is zero and enable1 is one, the system acts like MASH 1-1 structure. Else, just accumulator works, and the system acts like accumulator. The area would be smaller and order of SDM can be elective.

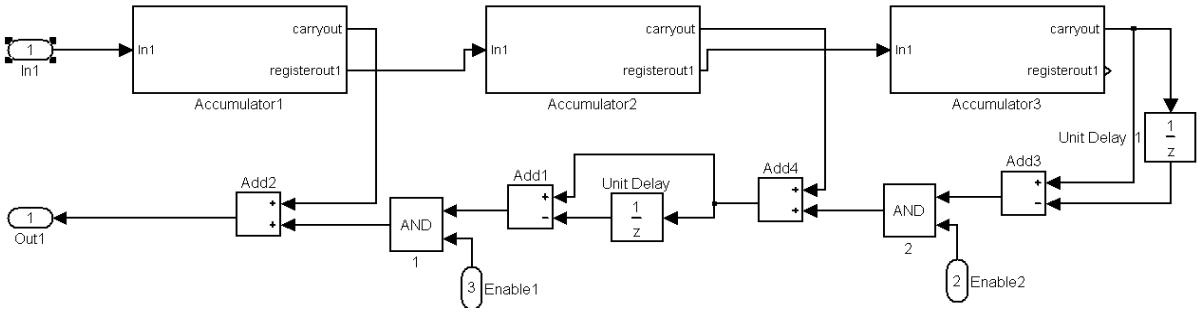


Figure 7.1: Advanced sigma delta modulator with programmable order.

Moreover, division value of fixed divider can be decreased from four to three, which provides a better phase noise.

Furthermore, as stated at chapter four, Voltage controlled oscillator is highly non linear. Linearity can be increased by usage of techniques at [52]. With the increase of linearity of VCO, loop behavior will be much more linear, and converges to the Matlab® results.

As Final improvement, capacitances at loop filter can be designed from gate capacitances of MOS transistors. Drain source and bulk of NMOS can be connected and gate capacitance as shown at Figure 7.2. The NMOS capacitance is nonlinear until it crosses the threshold voltage and enters the inversion region. After the gate voltage exceeds the threshold voltage, the device capacitance is constant. With this improvement, larger capacitances can be used at loop filter for the same area. To have same loop bandwidth, charge pump current should be increased, which can be easily done with increase of width of output transistors of charge pump. With larger capacitances, as stated at chapter 5, a better phase noise behavior and smaller jitter can be obtained.

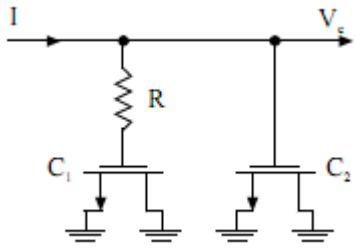


Figure 7.2: Loop-filter implementation with NMOS devices.

REFERENCES

1. B. Pak, "2.4 Ghz Cmos Pll Frequency Synthesizer," in *Institute of Science and Technology* Istanbul: Istanbul Technical University, 2002.

2. Z. Ö. Gürsoy, "Design and Realization of a 2.4gbps – 3.2gbps Clock and Data Recovery Circuit," in *Graduate School of Engineering and Natural Sciences*. Istanbul: Sabanci University, 2003.

3. Razavi B., *Monolithic Phase-Locked Loops and Clock Recovery Circuits*, IEEE Press, New York, 1996.

8. A. B. Grebene, The monolithic phase-locked loop - a versatile building block, IEEE Spectrum, vol. 8, pp.38-49, March 1971.

9. R. E. Best, *Phase Locked Loops, second edition*, McGraw Hill, New York, 1993.

10. G. S. Moschytz, Miniaturized RC filters using phase-locked loop, Bell Syst. Tech.

J., vol. 44, pp. 823-870, May 1965

11. W. F. Egan, *Frequency Synthesis by Phase Lock*, Wiley & Sons, New York, 1981

12. Adler, J., 1999. *Jitter in Clock Sources*, Vectron International

13. Gardner, F., 1979. *Phaselock Techniques*, John Wiley and Sons, Inc.

14. Soo, N., 1999. *Jitter Measurement Techniques Application Notes*, Pricom.

15. Chandler, D., 1999. Phase Jitter, Corning Frequency Control.

16. A. Aktaş and M. Ismail, *CMOS PLLs and VCOs for 4G Wireless*. Norwell, Massachusetts: Kluwer Academic Publishers, 2004.

17. J. M. Rogers, F. F. Dai, C. Plett, and M. S. Cavin, "Design and Characterization of a 5.2GHz/2.4GHz ΣΔ Fractional-N Frequency Synthesizer for Low-Phase Noise Performance," *EURASIP Journal onWireless Communications and Networking*, pp. 1–11, 2006.

18. C.S. Vaucher, *Architectures for RF Frequency Synthesizers*, Kluwer Academic Publishers, 2002.

19. D. B. Leeson, "A simple model of feedback oscillator noise spectrum," *Proceedings of IEEE*, vol. 54, no. 2, pp. 329–330, 1966.

20. J.W.M.Rogersand C.Plett, *Radio Frequency Integrated Circuit Design*, Artech House, Norwood, Mass, USA, 2003.

21. Y.Watanabe, T. Okabayashi, S. Goka, andH. Sekimoto, "Phase noise measurements in dual-mode SC-cut crystal oscillators," *IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control*, vol. 47, no. 2, pp. 374–378, 2000.

22. V. F. Kroupa, "Jitter and phase noise in frequency dividers," *IEEE Transactions on Instrumentation and Measurement*, vol. 50, no. 5, pp. 1241–1243, 2001.

23. V. F. Kroupa, "Noise properties of PLL systems," *IEEE Transactions on Communications*, vol. 30, no. 10, pp. 2244–2252, 1982.

24. http://www.mathworks.com/products/simulink/

25. J. W. M. Rogers, F. F. Dai, M. S. Cavin, and D. G. Rahn, "A multiband ΔΣ fractional-*N* frequency synthesizer for a MIMO WLAN transceiver RFIC," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 3, pp. 678–689, 2005.

26. B. C. Kuo, "*Automatic Control Systems* ". Englewood Cliffs, New Jersey: Prentice-Hall, Inc A Simon & Schuster Company, 1995.

27. K. Shu, E. Sánchez-Sinencio, J. Silva-Martínez, and S. H. K. Embabi, "A 2.4-GHz Monolithic Fractional-N Frequency Synthesizer With Robust Phase-Switching Prescaler and Loop Capacitance Multiplier Keliu Shu, StudentMember," *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, vol. 38, 2003.

28. Rogers, Platt , and Dai, *Integrated Circuit design for High Speed frequency synthesis,* Boston: ARTECH HOUSE press, 2006

29. B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: McGraw-Hill, 2001.

30. S. S. Navdeep, "High swing CMOS cascode current mirror," A. T. B. Laboratories, Ed. US, 1984.

31. K. J. d. Langen and J.H.Huijsing, "Compact low-voltage PTAT-current source and bandgap-reference circuits," presented at ESSCIRC '98. Proceedings of the 24th European, 1998.

32. A. Lacaita, S. Levantino, and C. Samori, *Integrated Frequency Synthesizers for Wireless Systems*, First ed. Cambridge: Cambridge University Press, 2007.

33. Y. Leblebici and S.-M. Kang, *CMOS Digital Integrated Circuits*, Third ed: McGraw-Hill, 2005.

34. S. Brigati, F. Francesconi, A. Malvasi, A. Pesucci, and M. Poletti, "Modeling of fractional-N division frequency synthesizers with SİMULİNK® and MATLAB," presented at Electronics Circuits and Systems, The 8th IEEE International Conference, 2001.

35. C. S. Vaucher, I. Ferencic, M. Locher, S. Sedvallson, U. Voegeli, and Z. Wang, "A Family of Low-Power Truly Modular Programmable Dividers in Standard 0.35-μm CMOS Technology " *Ieee Journal Of Solid-State Circuits*, vol. 35, 2000.

36. M.-W. Hwang, J.-T. Hwang, and G.-H. Cho, "Design of High Speed CMOS prescaler," presented at The Second IEEE Asia Pacific Conference on ASICs, 2000.

37. A. K. Bakkaloglu, A. Ergintav, E. Ozeren, I. Tekin, and Y. Gurbuz, "Design of a tunable multi-band differential LC VCO using 0.35 μm SiGe BiCMOS technology for multi-standard wireless communication systems," *Microelectronics Journal*, vol. 40, pp. 983-990, 2008.

38. A. K. Bakkaloğlu, "Realization of a Voltage Controlled Oscillator using 0.35 μm SiGe-BiCMOS Technology for Multi-band Applications," in *Graduate School of Engineering and Natural Sciences*. Istanbul: Sabanci University, 2008.

39. J. Craninckx and M. Stayaert, "A 1.8-GHz Low-Phase-Noise CMOS VCO Using Optimized Hollow Spiral Inductors," IEEE Journal of Solid-State Circuits, vol. 32, No. 5, pp. 736–744, May 1997.

40. B. Razavi, RF Microelectronics, Upper Saddle River, New Jersey: Prentice- Hall, 1998.

41. A. Berny, A. Niknejad, and R. Meyer, "A wideband low-phase-noise CMOS VCO," in *Proceedings of the IEEE Custom Integrated Circuits Conference,* Sept. 2003, pp. 555– 558.

42. N. H. W. Fong, J.-O. Plouchart, N. Zamdmer, D. Liu, L. C. Plett and N. G. Tarr, *"Design of wide-band CMOS VCO for multiband wireless LAN applications"* IEEE J. Solid-State Circuits*, vol. 38, pp. 1333-1342, August 2003.*

43. H. Sjöland, "Improved switched tuning of differential CMOS VCOs," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing,* , vol. 49, pp. 352-355, 2002.

44. Zhenbiao Li, K.O,"A 900-MHz 1.5-V CMOS voltage-controlled oscillator using switched resonators with a wide tuning range,"IEEE Microwave and Wireless Components Letters., vol. 13, Issue 4, pp.137-139, April 2003.

45. A Mazzanti, P. Uggetti, R. Battagia, and F. Svelto, "Analysis and design of a dual band reconfigurable VCO," presented at ICECS, 2004.

46. Y. Seong-Mo and K. O. Kenneth, "Switched Resonators and Their Applications in a Dual-Band Monolithic CMOS LC-Tuned VCO," *IEEE Transactions On Microwave Theory And Techniques*, vol. 54, pp. 74- 81, 2006.

47. S. Kurachi, Y. Murata,S. Ishikawa,N. Itoh and K. Yonemura, "A 4-GHz Band Ultra-Wideband Voltage Controlled Oscillator IC using 0.35 μm SiGe BiCMOS Technology" in IEEE Bipolar/BiCMOS Circuits and Technology *Meeting*, Sept. 30 2007-Oct. 2 2007 , pp. 9 – 12.

48. Jang, S.-L.; Chuang, Y.-H.; Chen, C.-C.; Lee, S.-H.; Lee, J.-F., "A CMOS Dual-Band Voltage Controlled Oscillator" in *IEEE Asia Pacific Conference on 4-7* Dec. 2006, pp. 514 – 517.

49. N. H. W. Fong, J.-O. Plouchart, N. Zamdmer, D. Liu, L. C. Plett and N. G. Tarr*, "Design of wide-band CMOS VCO for multiband wireless LAN applications"* IEEE J. Solid-State Circuits*,* vol. 38, pp. 1333-1342, August 2003.

50. P. Vaananen, M. Metsanvirta and N. Tchamov, "A 4.3-GHz VCO with 2-GHz tuning range and low phase noise," *IEEE J. Solid-State Circuits*, vol. 36, pp. 142 - 146, January 2001.

51. J. Maget, M. Tiebout and R. Kraus, "Influence of novel MOS varactors on the performance of a fully integrated UMTS VCO in standard 0.25-μm CMOS technology " *IEEE J. Solid-State Circuits*, vol. 37, pp. 953 -958, July 2002.

52. Quang Diep Bui and Chul Soon Park, “All-PMOS Wideband VCO with an Automatic Amplitude Controller for Multi-band Multi-standard Radios” in *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium,* 3-5 June 2007 , pp. 697 – 700.

53. S. Kurachi, T. Yoshimasu, H. Liu, N. Itoh, And K. Yonemura, "A SiGe BiCMOS VCO IC with Highly Linear Kvco for 5-GHz-Band Wireless LANs," *IEICE Transactions on Electronics*, vol. E90–C, pp. 1228-1233, 2007.

7. S. Ali and M. Margala, "A 5.1-GHz CMOS PLL based integer-N frequency synthesizer with ripple-free control voltage and improved acquisition time," presented at ISCAS 2004, Vancouver, BC, Canada, 2004.

4. S. I. Ahmed, R. D. Mason, " Improving The Acquisition Time Of A Pllbased, Integer-N Frequency Synthesizer," presented at ISCAS 2004, Vancouver, BC, Canada, 2004.

5. R. E. Best, *Phase-Locked Loops - Design, Simulation, and Applications*, Fourth ed: McGraw-Hill, 1999.

6. ITU-T Recommendation G.810 (08/1996), Definitions and terminology for synchronization networks

54. Y.U. Yim, J.F. McDonald, and R.P. Kraft, “12–23 GHz ultra wide tuning range voltage-controlled ring oscillator with hybrid control schemes,” *in proceedings of IEEE Computer Society Annual Symposium on VLSI,* Tampa, FL, 2005, pp. 278 – 279.

55. J. Rogers and C. Plett, *Radio frequency integrated circuit design*, Artech House, Boston, 2003

56. H. Shin, X. Zhiwei, and M.F. Chang, “A 1.8-V 6/9- GHz reconfigurable dual-band quadrature LC VCO in SiGe BiCMOS Technology”, *IEEE J Solid-State Circuits* 38, pp. 1028 – 1032, 2003.

57. S. Bahramirad, J.G. Atallah and S. Albrect, “A low Phase Noise VCO for MultiBand Wireless Transceivers,” *in International Conference on Design&Technology of Integrated Systems in Nanoscale Era, 2-5 Sept. 2007, pp. 148 - 153.*

Appendix

A1

```
% 2'nde order Loop filter transfer function generator for passive components and calculation of natural frequency damping factor and settling time
clc
k = 1e3;
p = 1e-12;
R = 7.5*k;
C1= 384*p;
C2= 48*p;
s = tf('s');
wn = (1/2)sqrt(((104e-6)/(2*pi))*(0.9e9)/(96*C1))
LF2 = (1+R*C1*s)/(s*s*R*C1*C2+s*(C1+C2))
ksi = (sqrt(((104e-6)/(2*pi))*0.9e9*R*R*C1/96))
settling=4/(wn*ksi)
ltiview('bode', LF)
```

A2

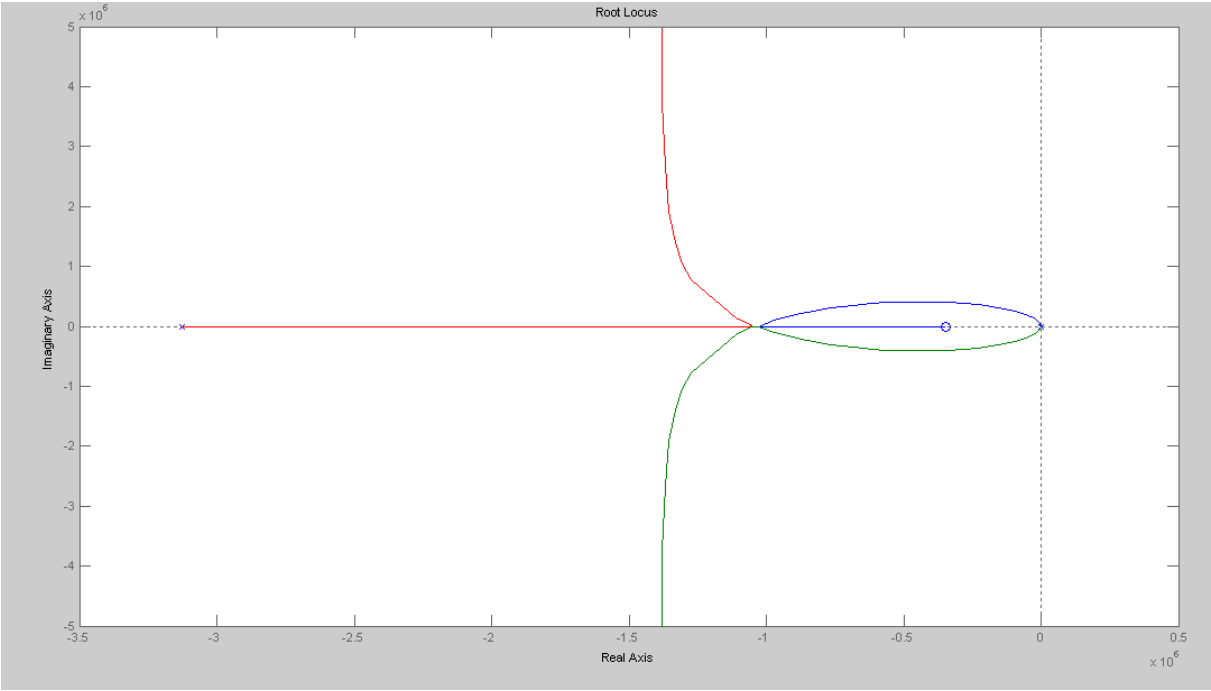
```
[t,x,y]=sim('divideracumulator');

pointnumber= numel(y);

yy =0;

for (ii = 1:pointnumber)

yy = y(ii)+yy;

end

 yy= yy/pointnumber
```

A3

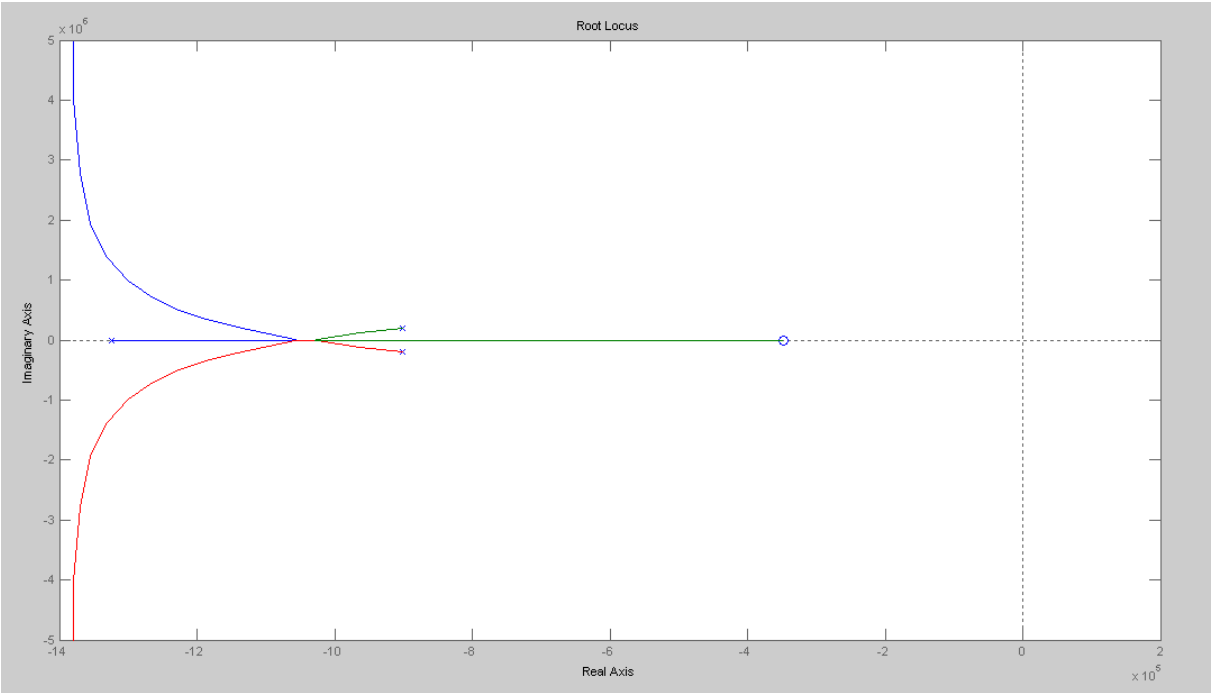
```
n = 1*10^-9
p=1*10^-12
G=1*10^9

L1 = 1.040*n
w=2*pi*5*G
C1=82.47*p
Rs=2.7689

A=(C1*Rs^2+2*L1-w^2*C1*L1^2)
B=2*Rs-(w^2)*(2*L1*C1*Rs)
C=C1*Rs

D=1-(w^2)*C1*L1
R2=(A/C)
L=A/(D-(C*B/A))
R1=B/(D-(C*B/A))
RP1=((L*w)^2)/R1
```

```
GP1=1/RP1
GP2=C/A
Gfinal=GP1+GP2
Rfinal=1/Gfinal
```

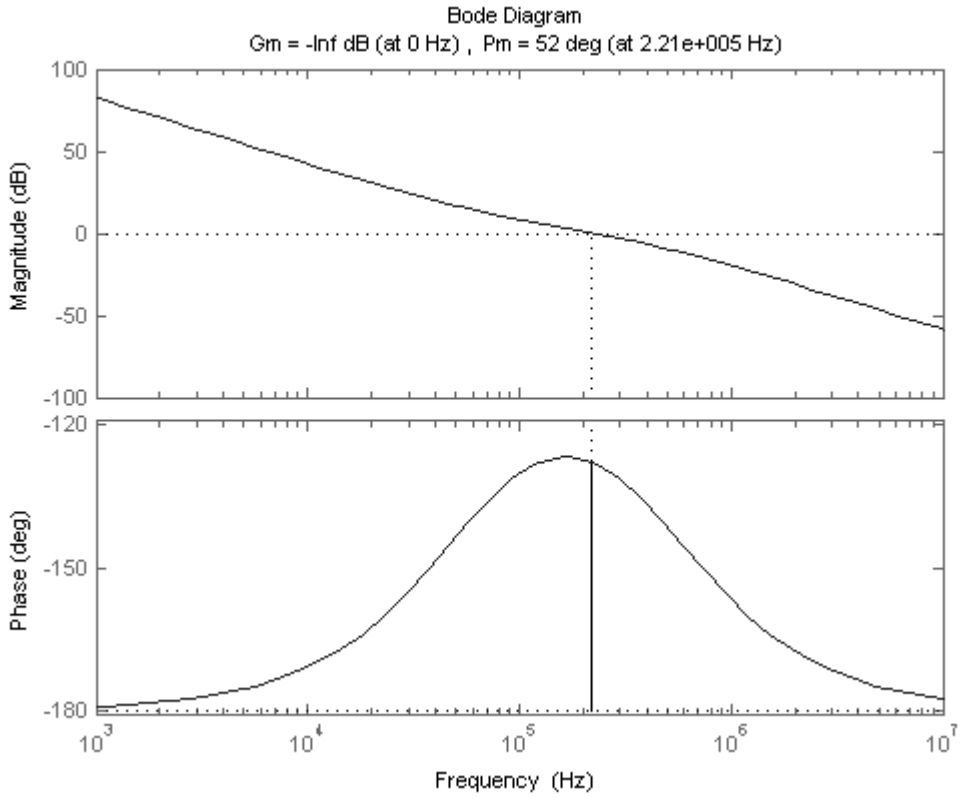
B1.



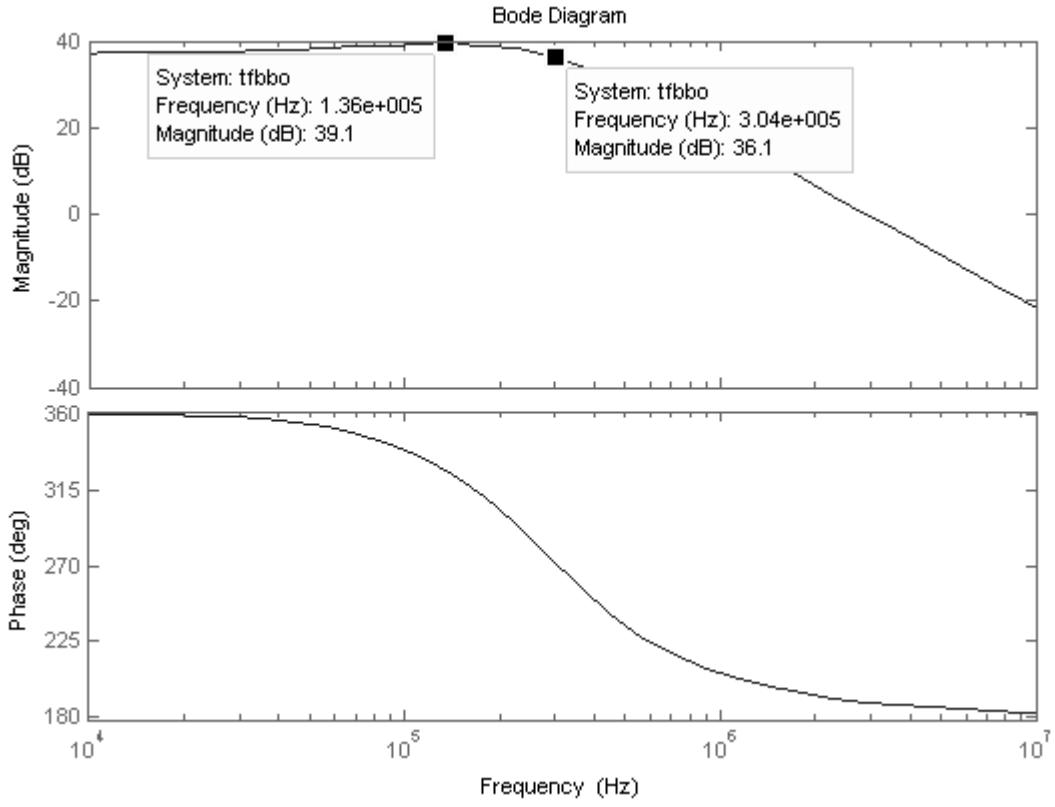
AP 1: Open loop Root locus plot of the system for 5GHz Band (band1).



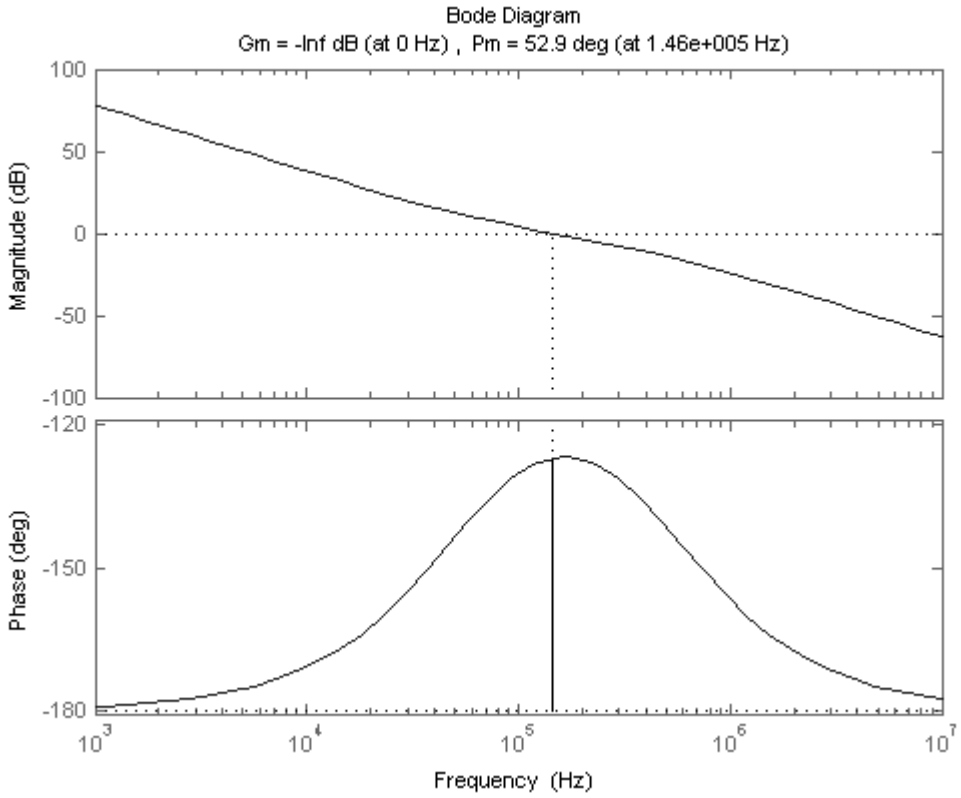
AP 2: Closed loop Root locus plot of the desired PLL system for 5GHz Band (band1).



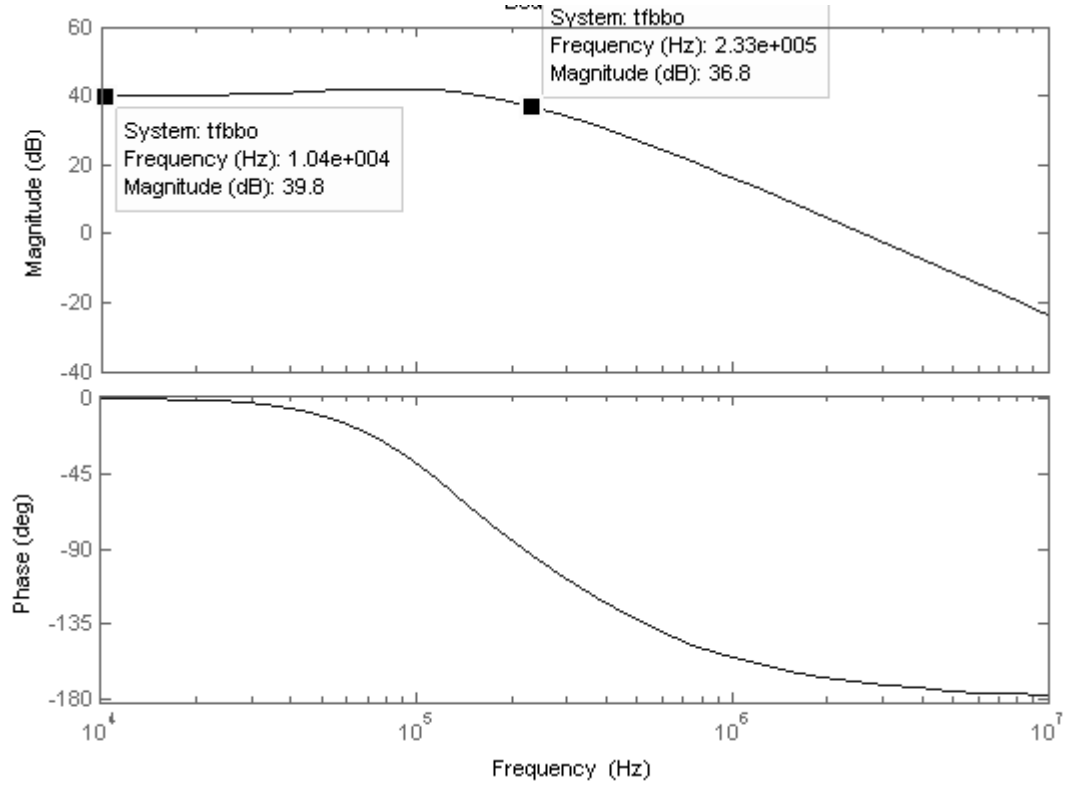
AP 3: Bode diagram for Band 2, Phase margin is 52.2^0



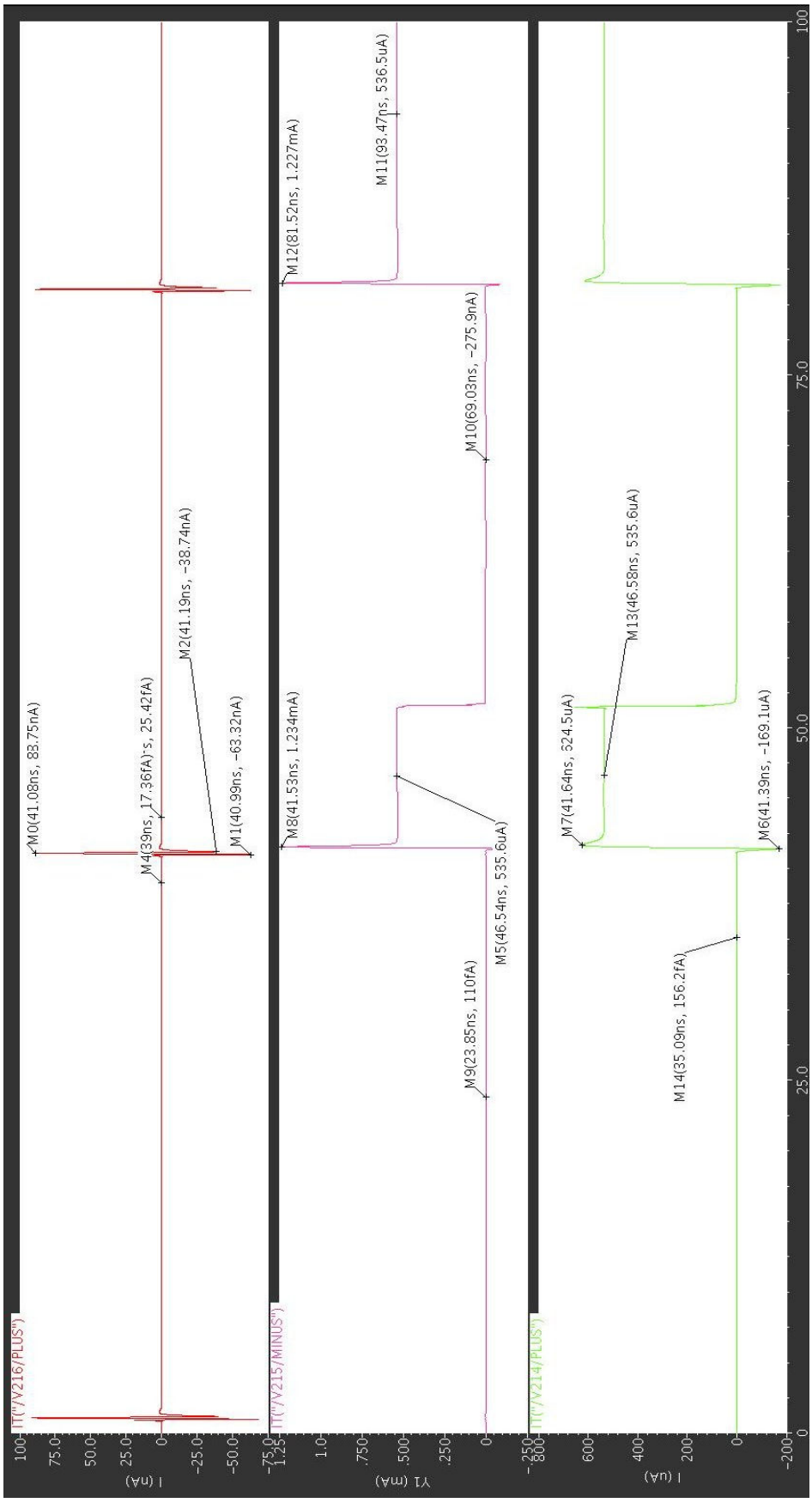
AP 4: Magnitude of the closed loop transfer function for band2. 3dB bandwidth is 300kHz.



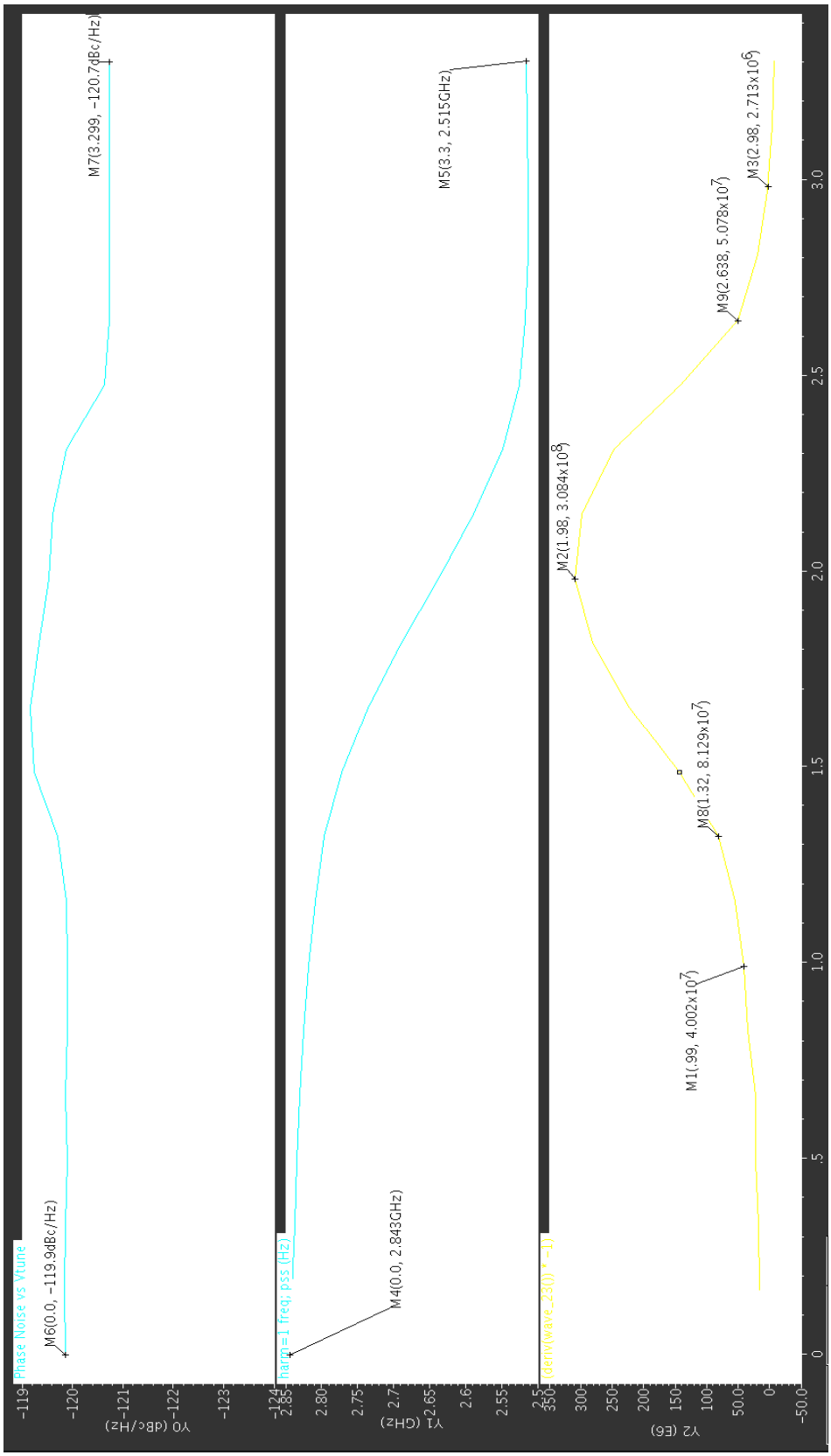
AP 5: Bode diagram for Band 3, Phase margin is 52.9^0



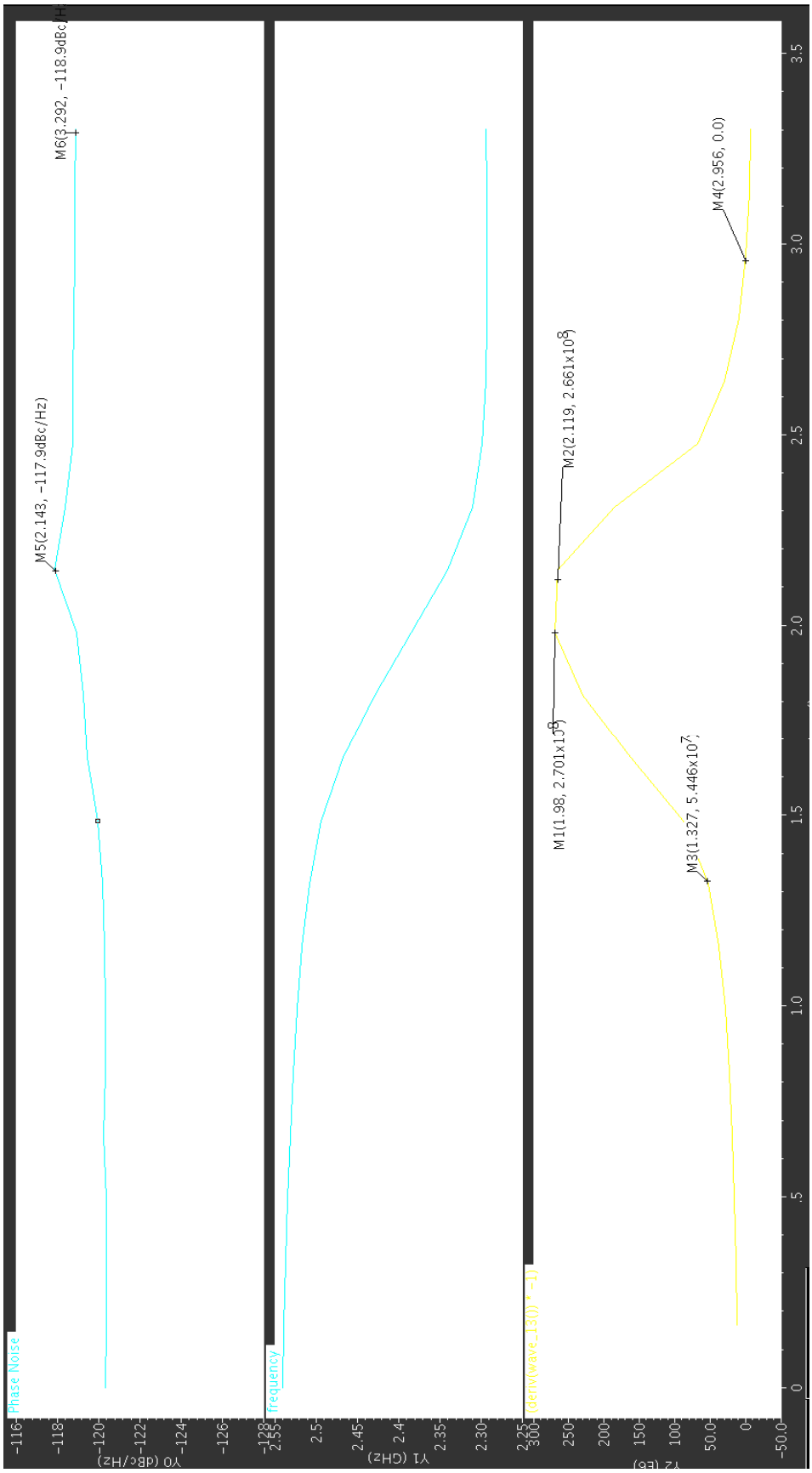
AP 6: Magnitude of the closed loop transfer function for band3. 3dB bandwidth is 233kHz.



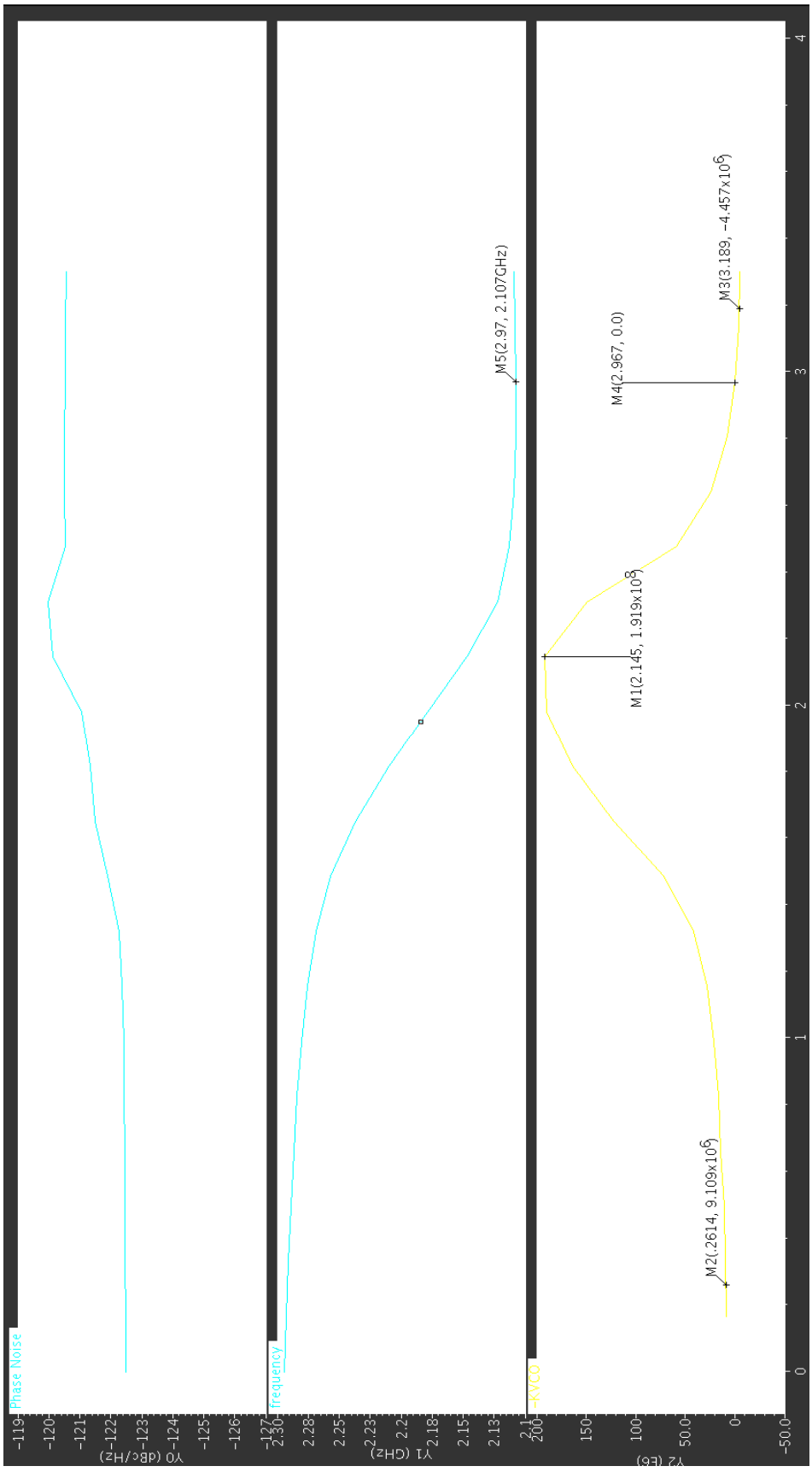
AP 7: transient mode analyze for Charge pump current ICP2



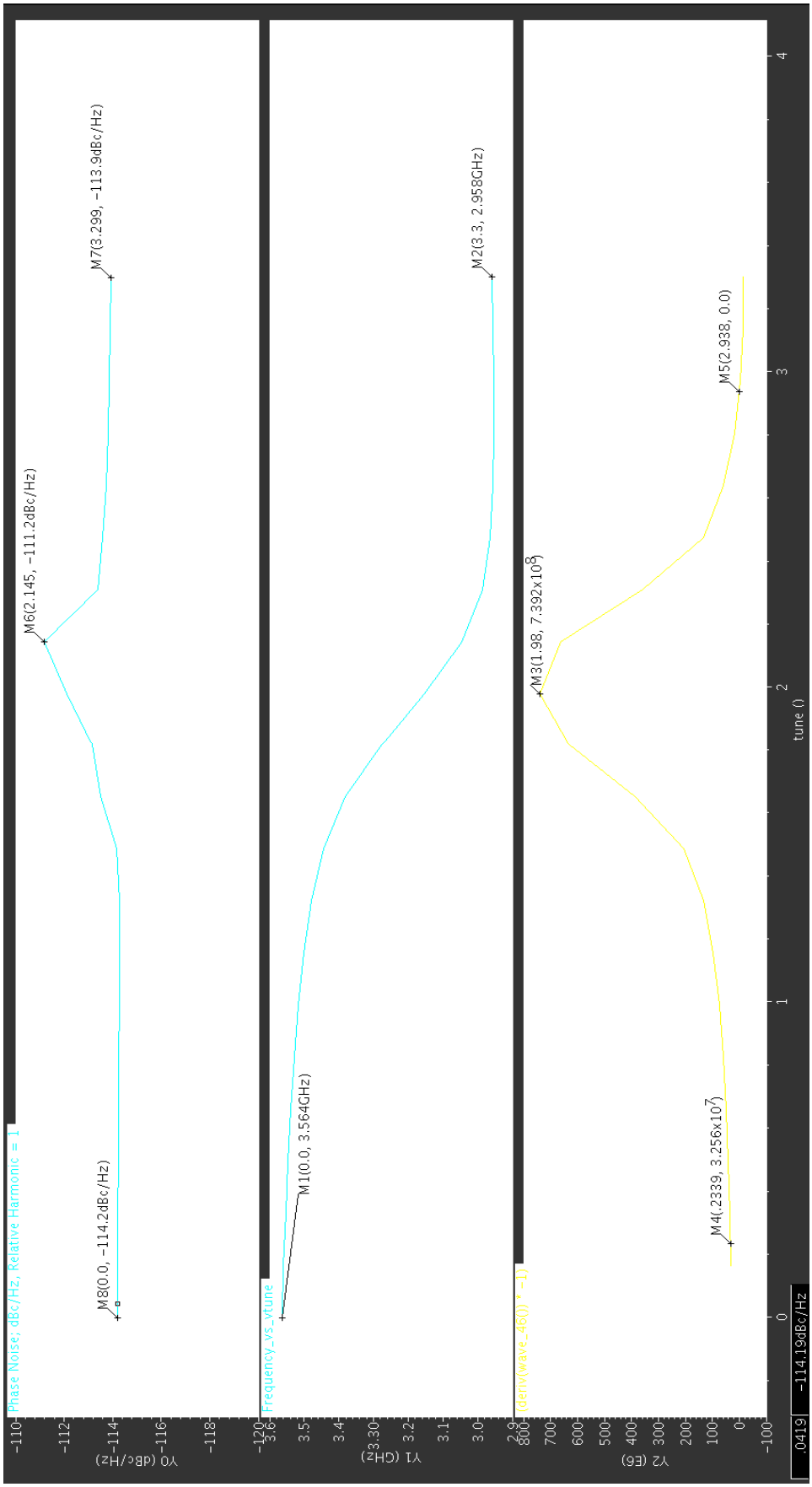
AP 8: Phase Noise vs Vtune, Frequency vs Vtune, Linearity (df/dV) vs Vtune for C1 on C2 and ind Switches are off for SQUARE switch



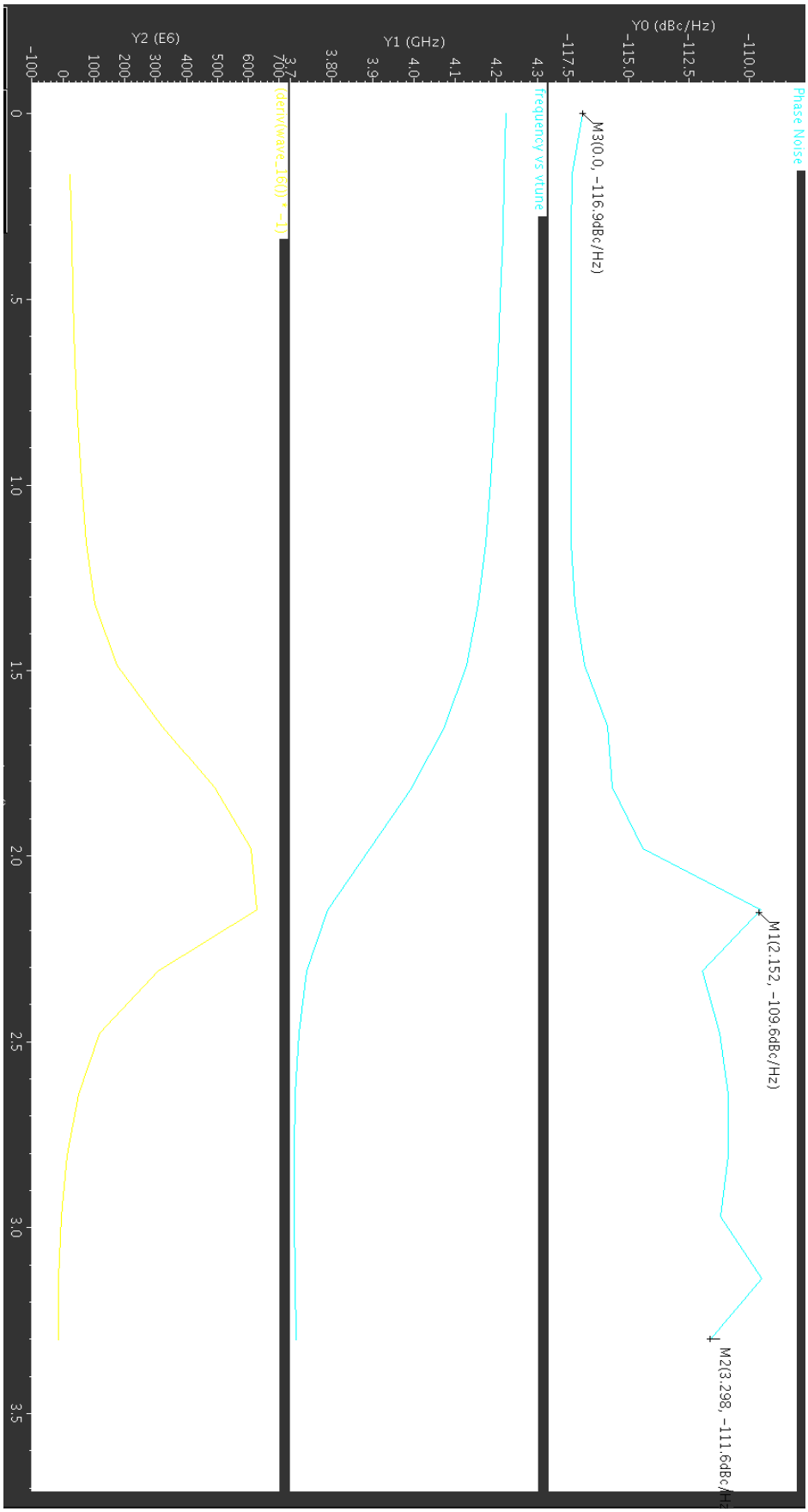
AP 9: Phase Noise vs Vtune, Frequency vs Vtune, Linearity (df/dV) vs Vtune for C2 on C1 and ind Switches are off for SQUARE switch



AP 10: Phase Noise vs Vtune, Frequency vs Vtune, Linearity (df/dV) vs Vtune for C2 and C1 are on ind Switch is off for SQUARE switch

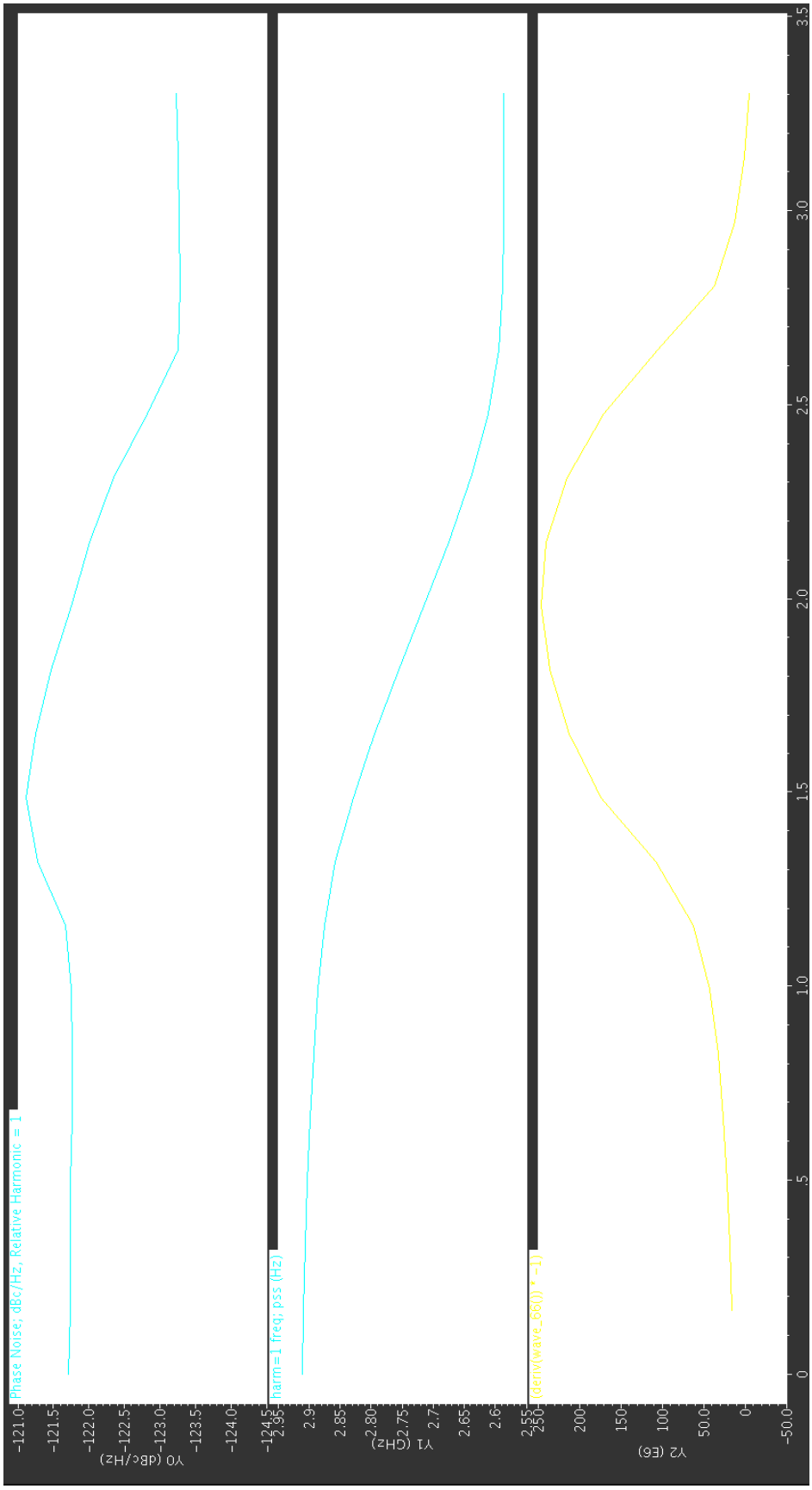


AP 11: Phase Noise vs Vtune, Frequency vs Vtune, Linearity (df/dV) vs Vtune for all Switches are off for SQUARE switch technique

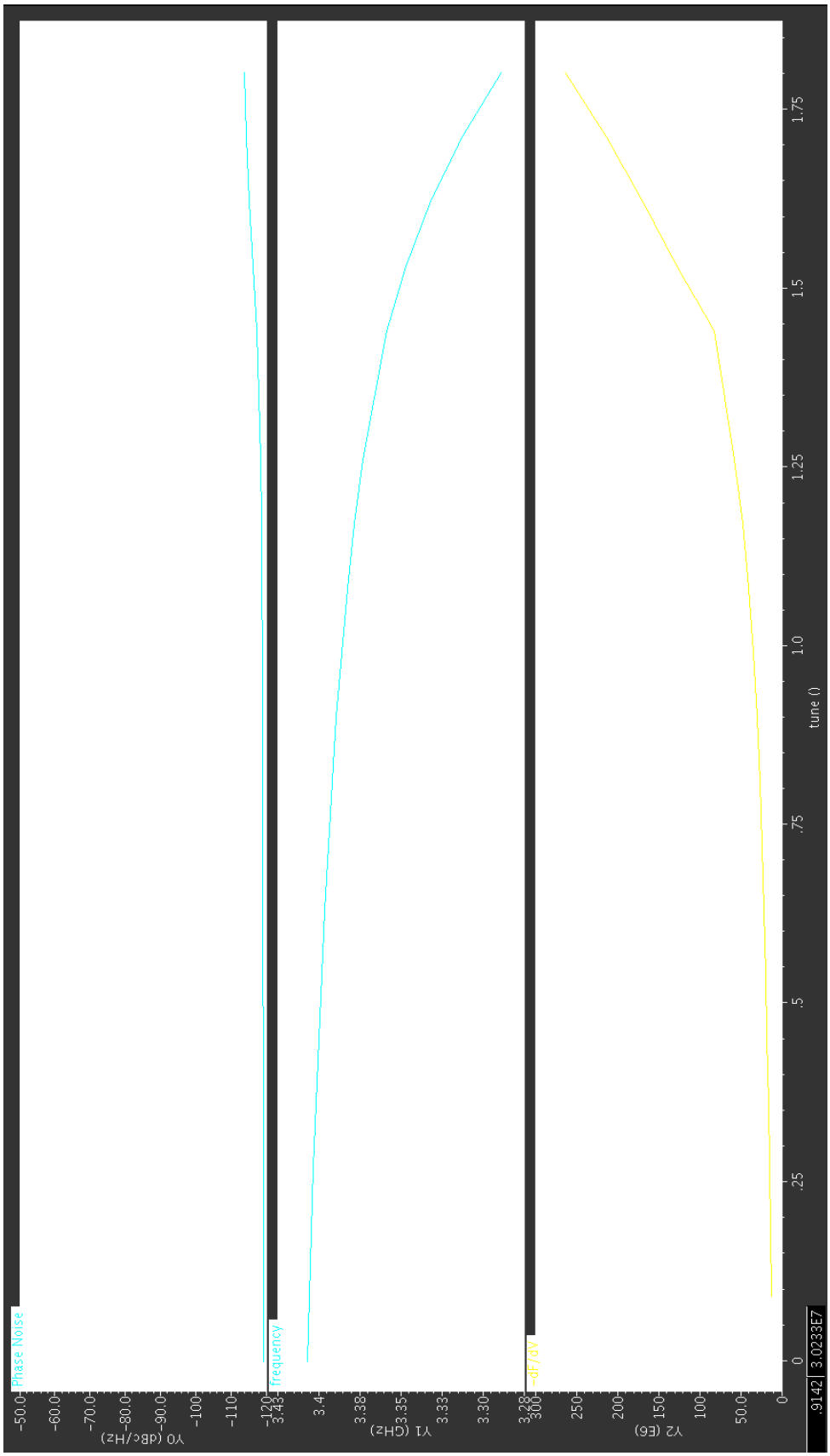


AP 12: Phase Noise vs Vtune, Frequency vs Vtune, Linearity (df/dV) vs Vtune for ind switch and C1 switches are on C2 is off for SQUARE switch technique

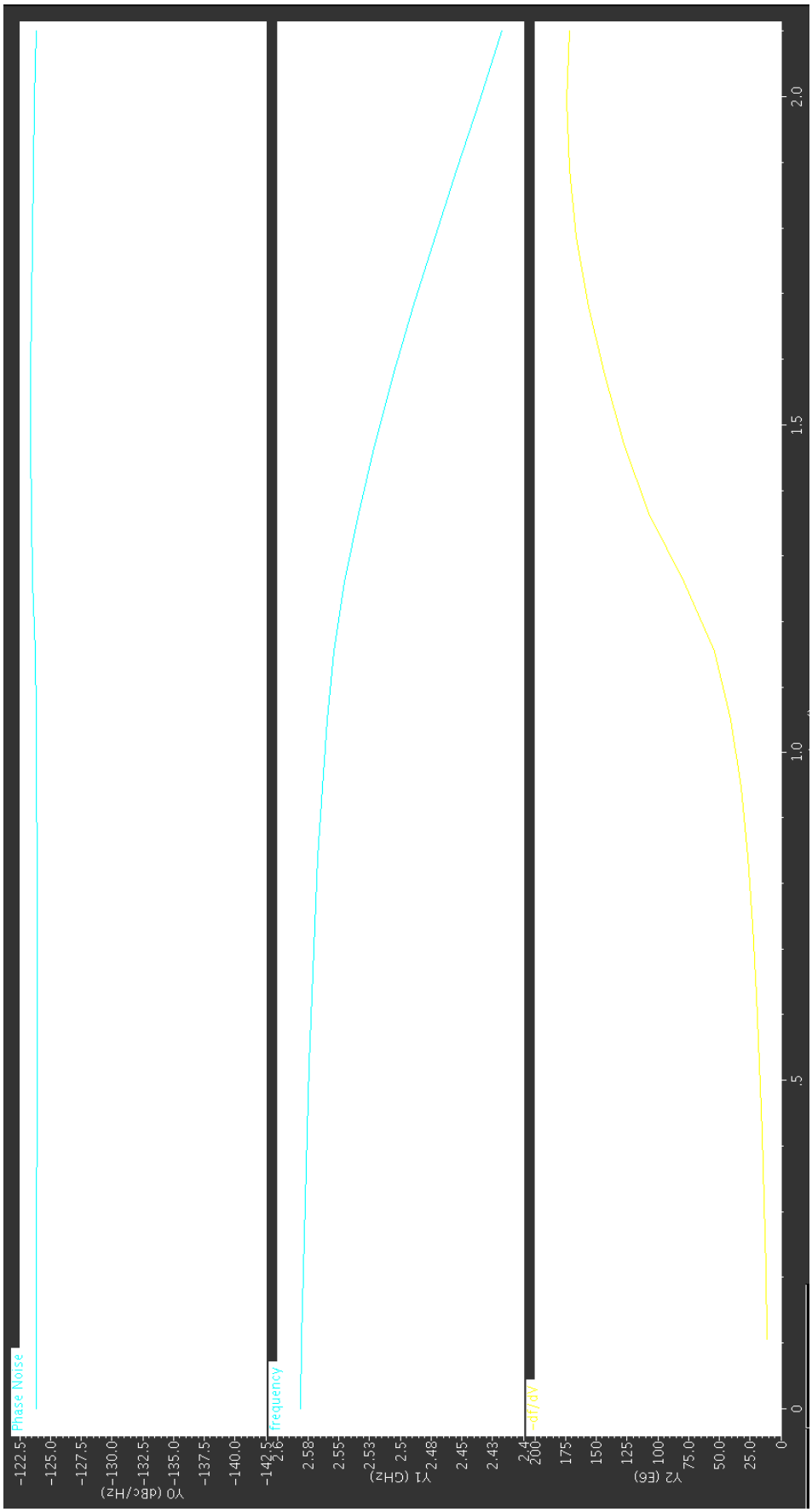
AP 13: Phase Noise vs Vtune, Frequency vs Vtune, Linearity (df/dV) vs Vtune for ind switch and C2 switches are on C1 is off for SQUARE switch technique



AP 14: Phase Noise vs Vtune, Frequency vs Vtune, Linearity (df/dV) vs Vtune for all switches are off for LARGE switch technique

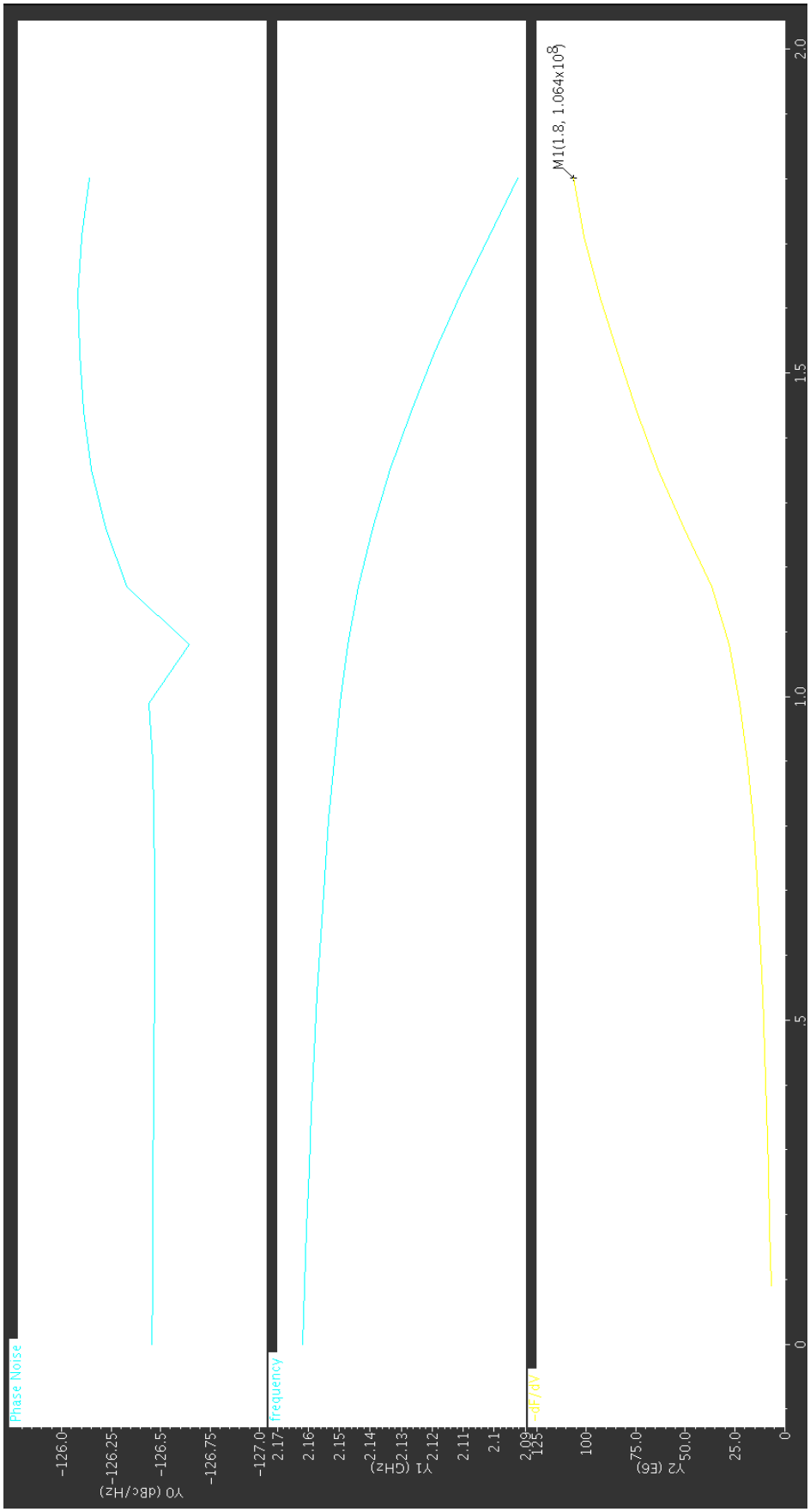


AP 15: Phase Noise vs Vtune, Frequency vs Vtune, Linearity (df/dV) vs Vtune for all switches are on for LARGE switch technique

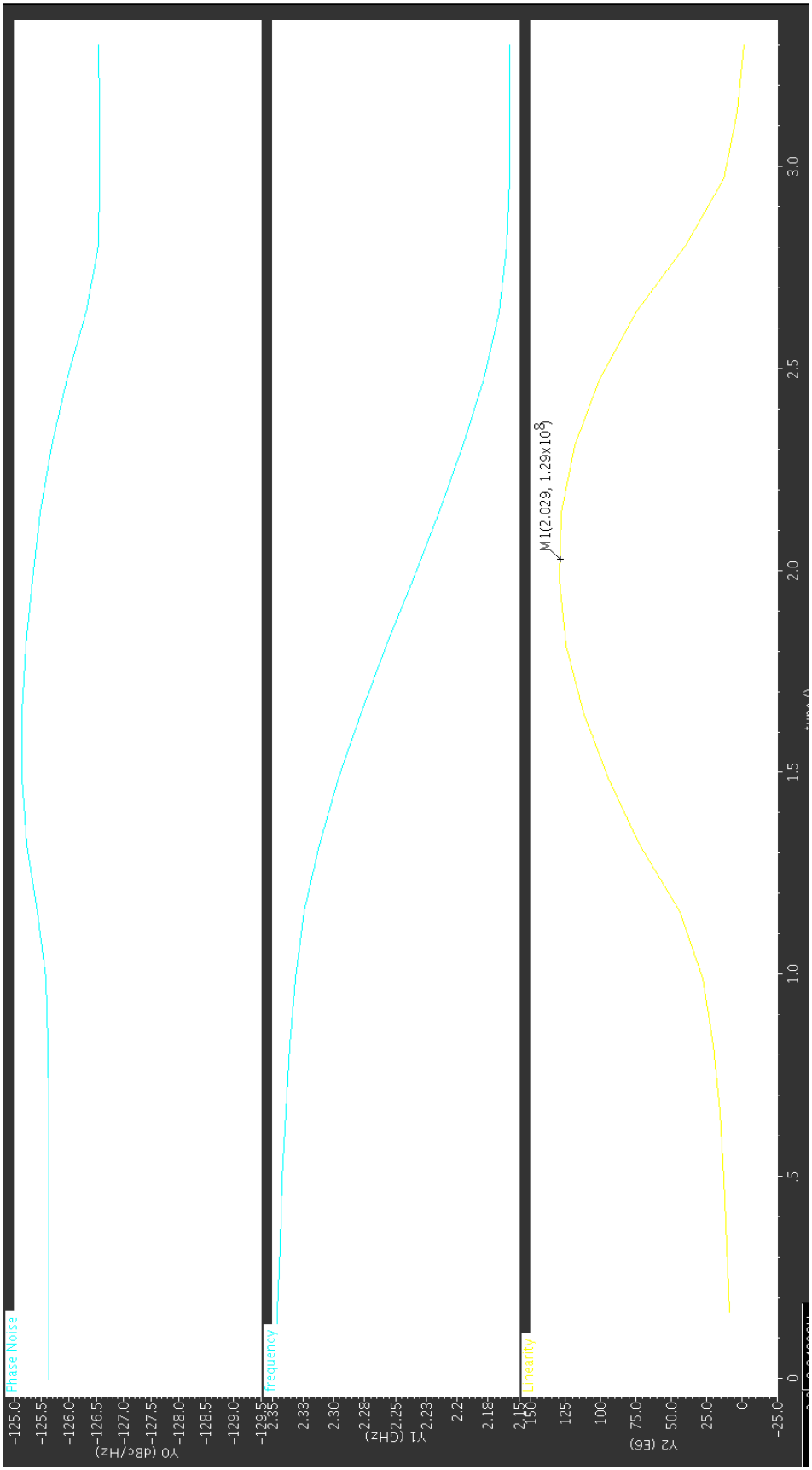


AP 16: Phase Noise vs Vtune, Frequency vs Vtune, Linearity (df/dV) vs Vtune for C1 switch is on ind and C2 swiches are off for LARGE switch technique

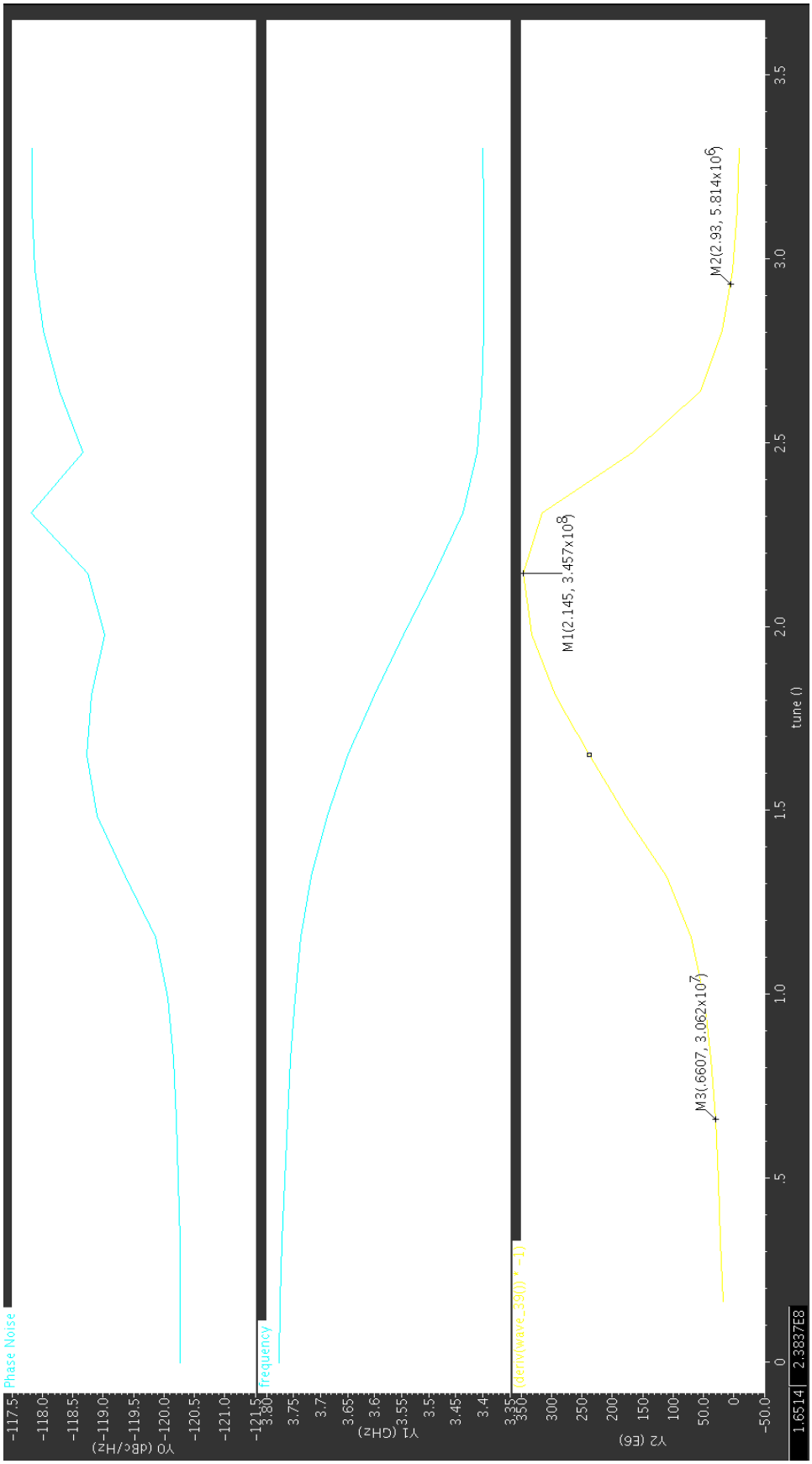
AP 17: Phase Noise vs Vtune, Frequency vs Vtune, Linearity (df/dV) vs Vtune for C1 switch and ind switches are on C1 swich is off for LARGE switch technique



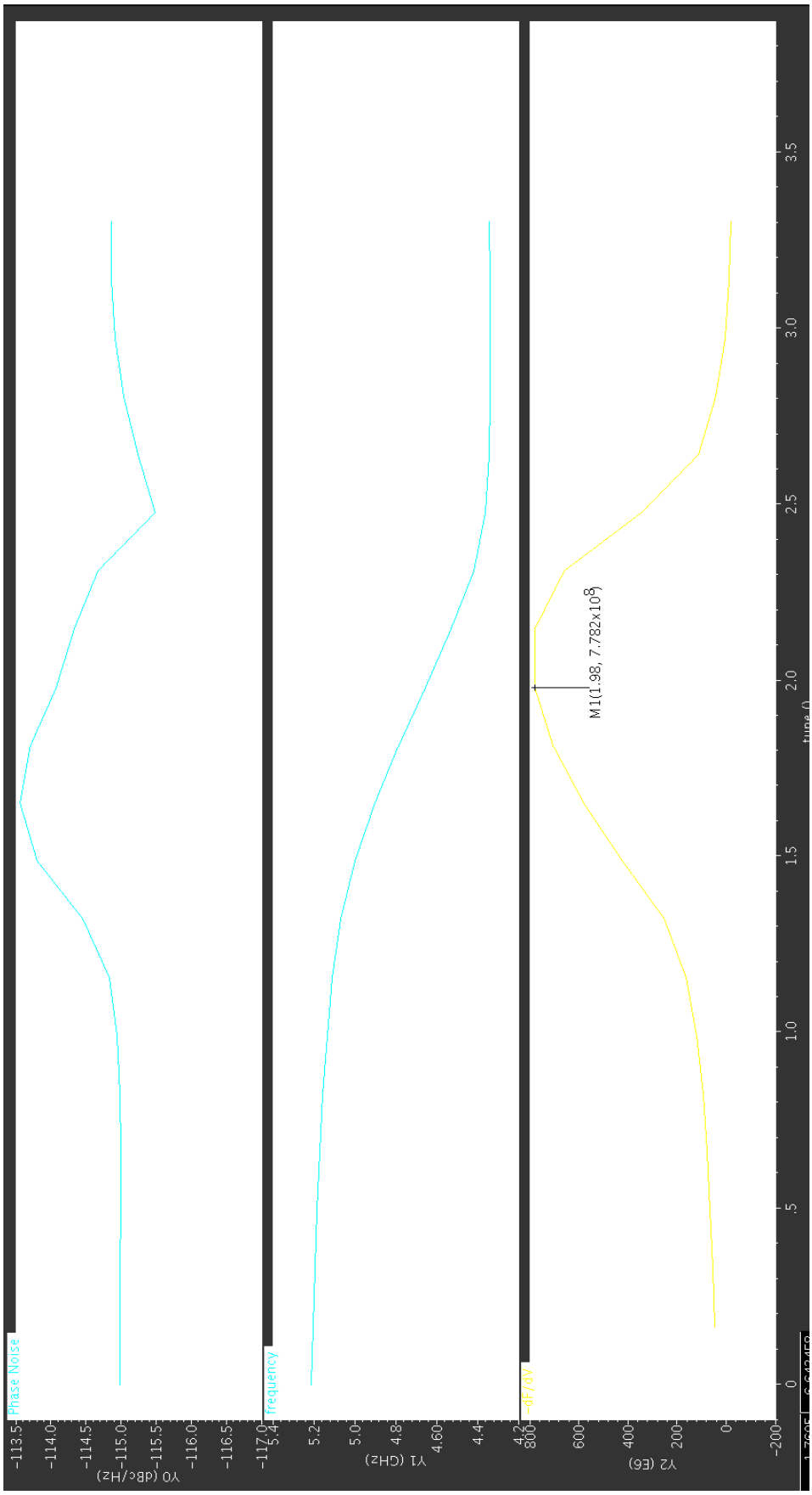
AP 18: Phase Noise vs Vtune, Frequency vs Vtune, Linearity (df/dV) vs Vtune for C1 switch and C2 switches are on ind swich is off for LARGE switch technique



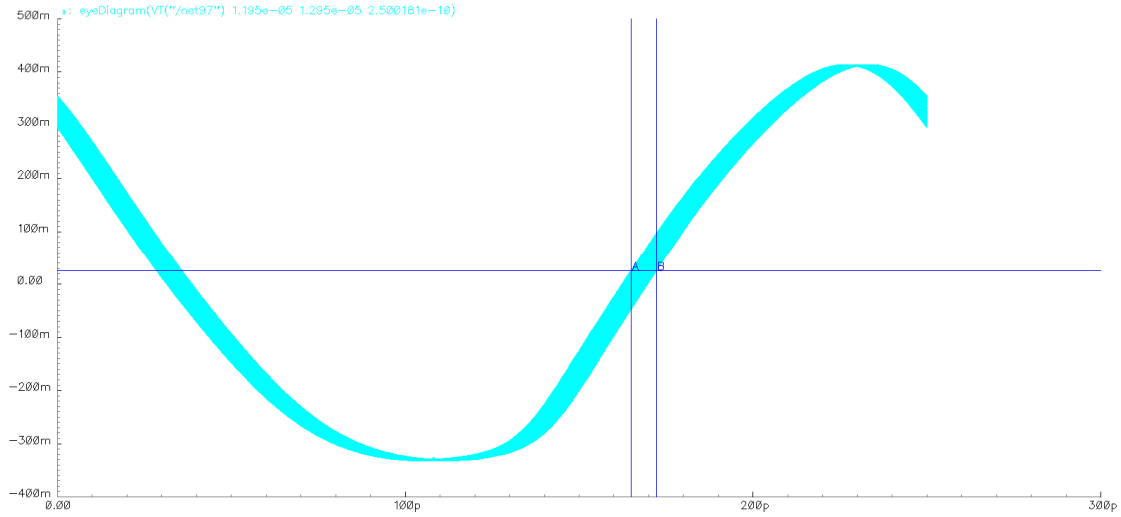
AP 19: Phase Noise vs Vtune, Frequency vs Vtune, Linearity (df/dV) vs Vtune for C1 switch and C2 switches are on ind swich is off for LARGE switch technique



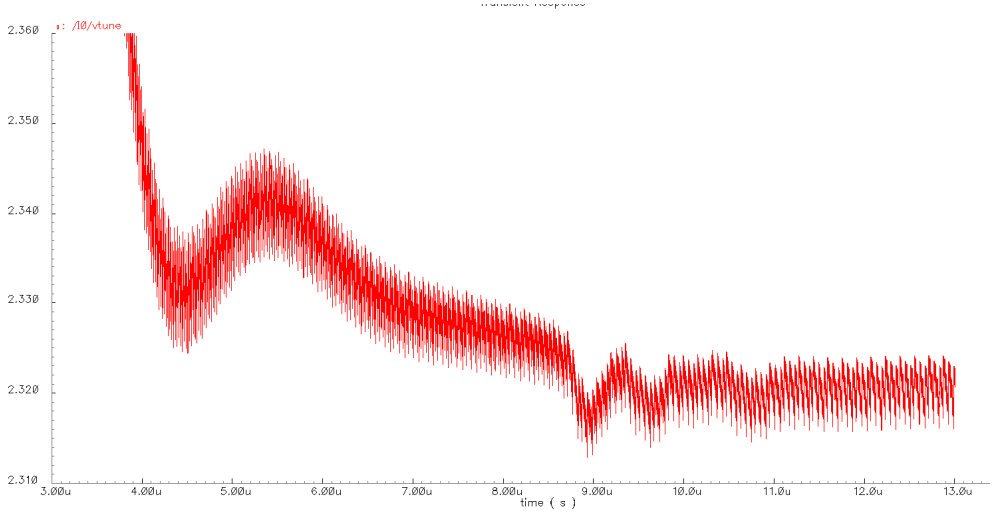
AP 20: Phase Noise vs Vtune, Frequency vs Vtune, Linearity (df/dV) vs Vtune for C1 switch and C2 switches are on ind swich is off for LARGE switch technique



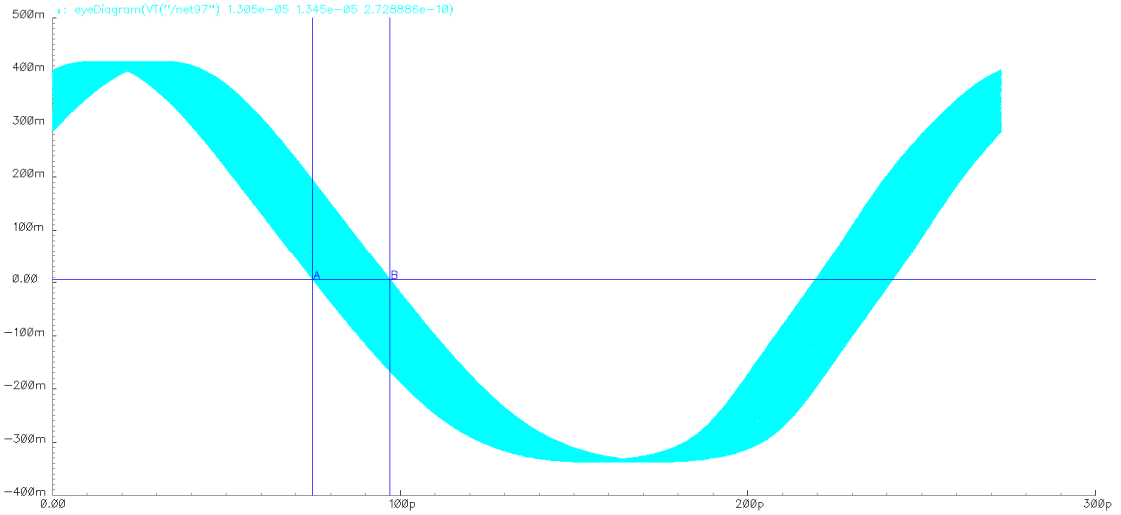
AP 21: Phase Noise vs Vtune, Frequency vs Vtune, Linearity (df/dV) vs Vtune for C1 switch and C2 switches are of ind swich is on for LARGE switch technique



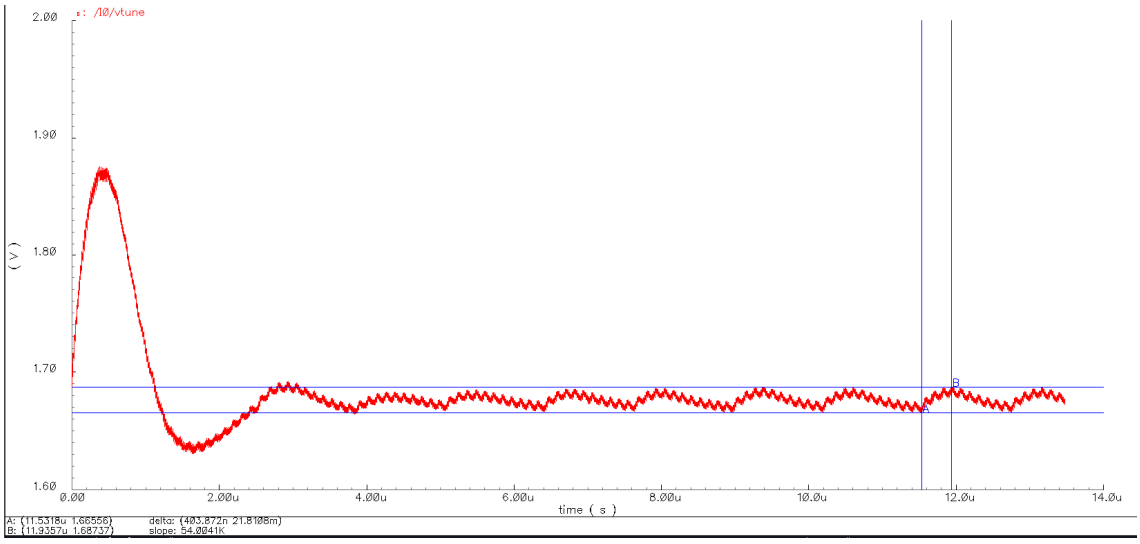
AP 22: Eye diagram for first order sigma delta modulator mode at band 3



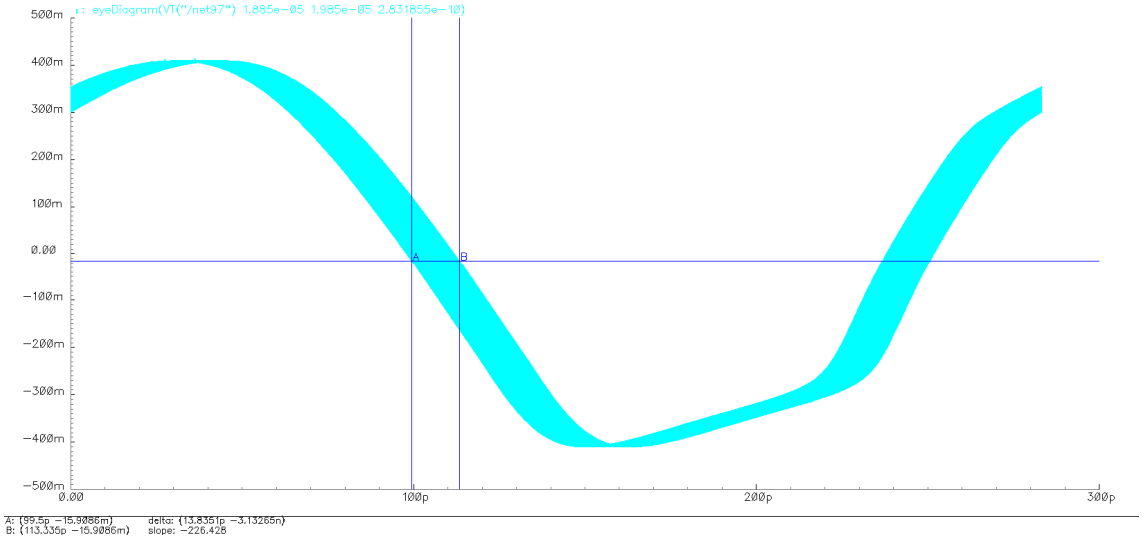
AP 23: settling behavior for PLL for first order sigma delta modulator mode at band2



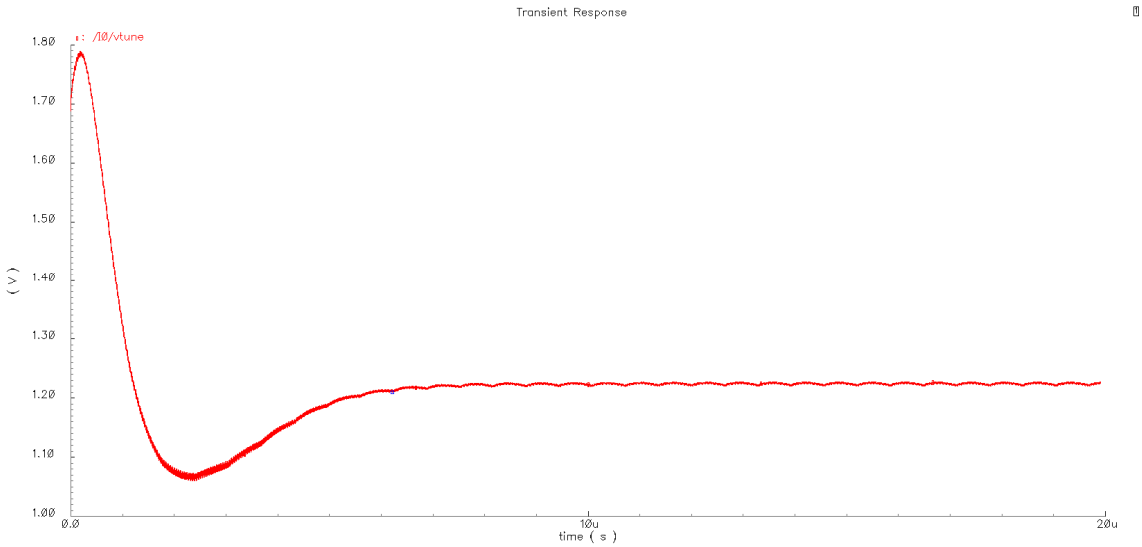
AP 24: Eye diagram for first order sigma delta modulator mode at band 3



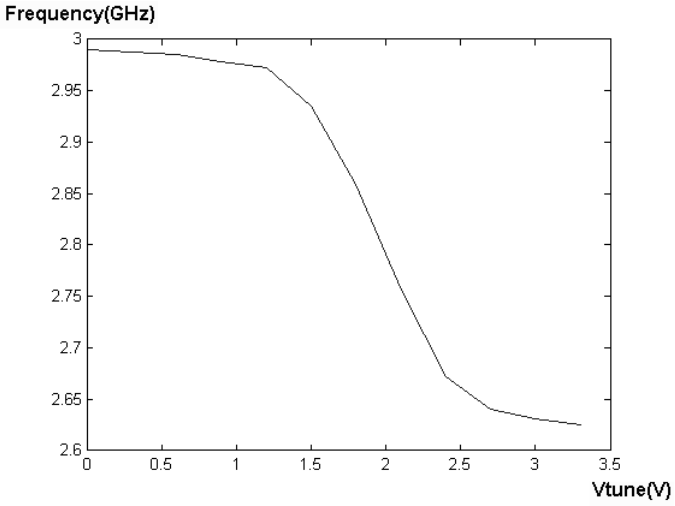
AP 25: settling behavior for PLL for first order sigma delta modulator mode at band3



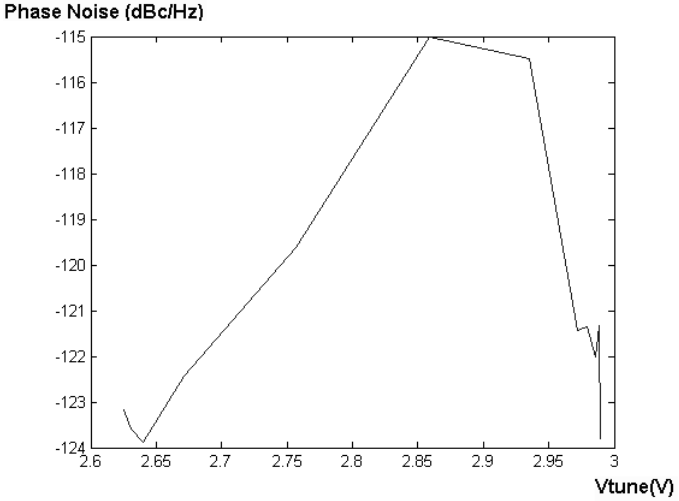
AP 26: Eye diagram for first order sigma delta modulator mode at band 4



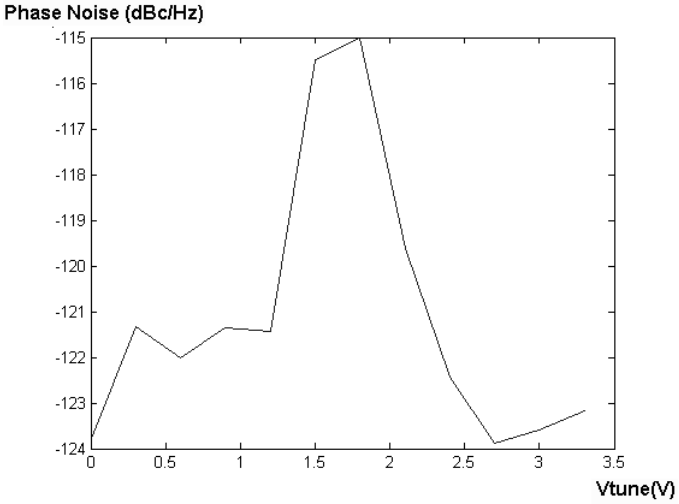
AP 27: settling behavior for PLL for first order sigma delta modulator mode at band4



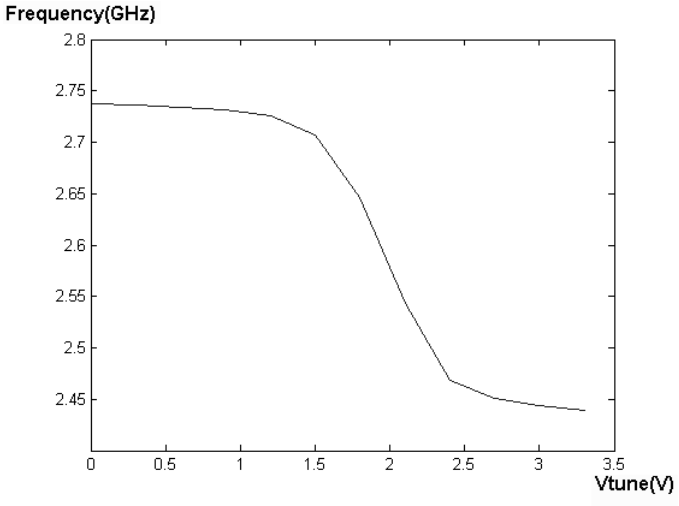
AP 28: Output frequency change of VCO with SQUARE switch with respect to Tune voltage at band 7



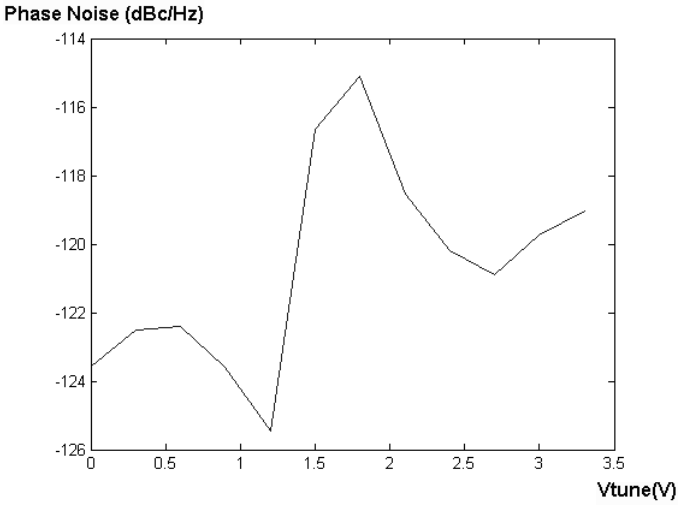
AP 29: Phase Noise change of VCO with SQUARE switch with respect to Tune voltage at band 7



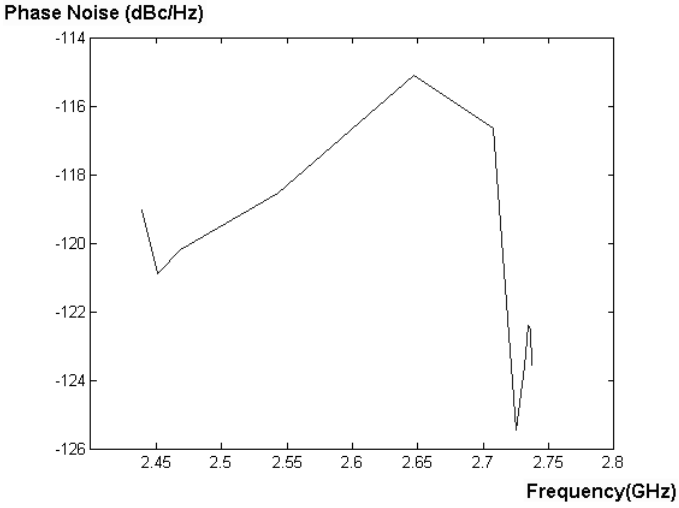
AP 30: Phase Noise change of VCO with SQUARE switch with respect to Frequency at band 7



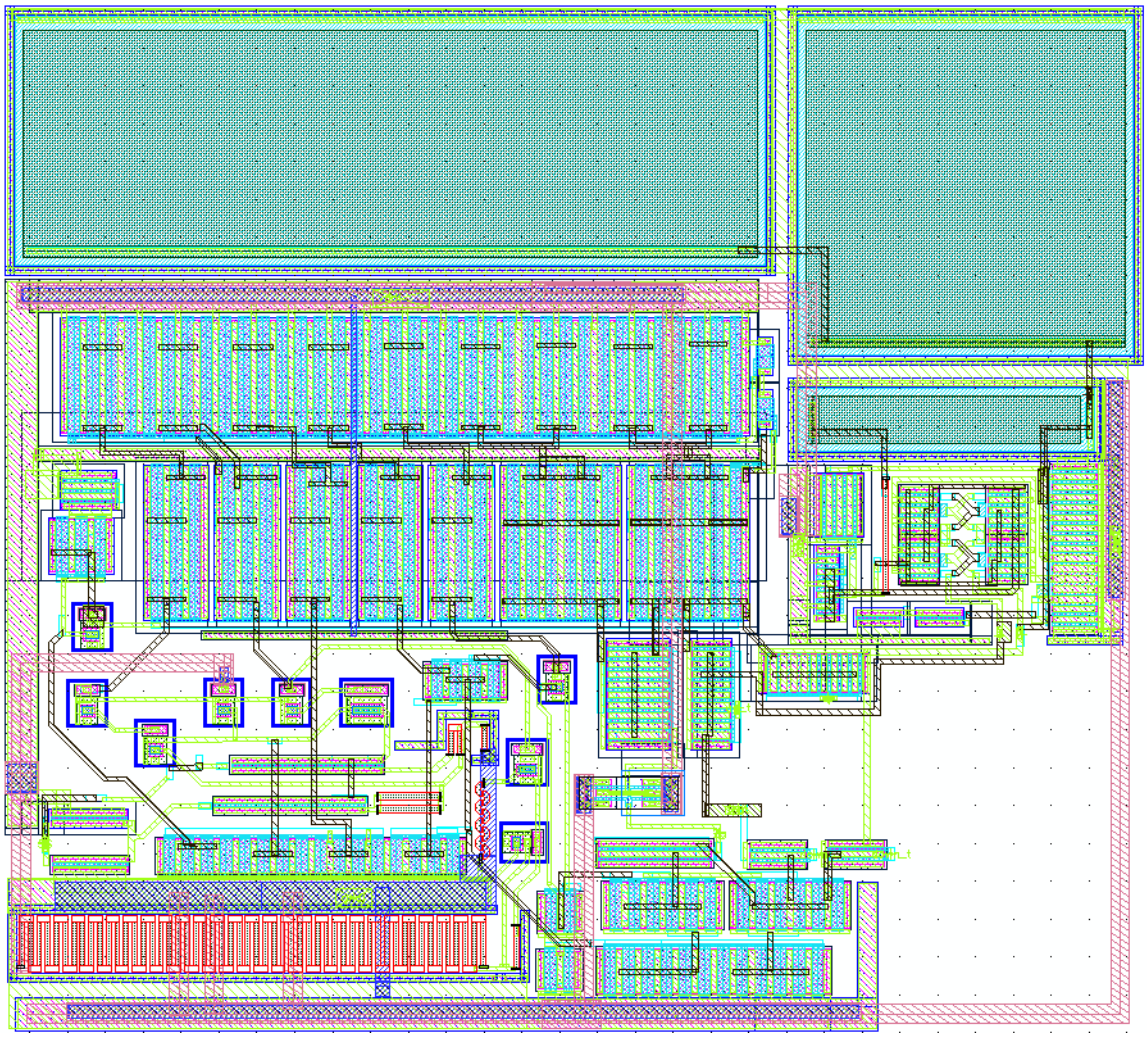
AP 31: Output frequency change of VCO with SQUARE switch with respect to Tune voltage at band 7



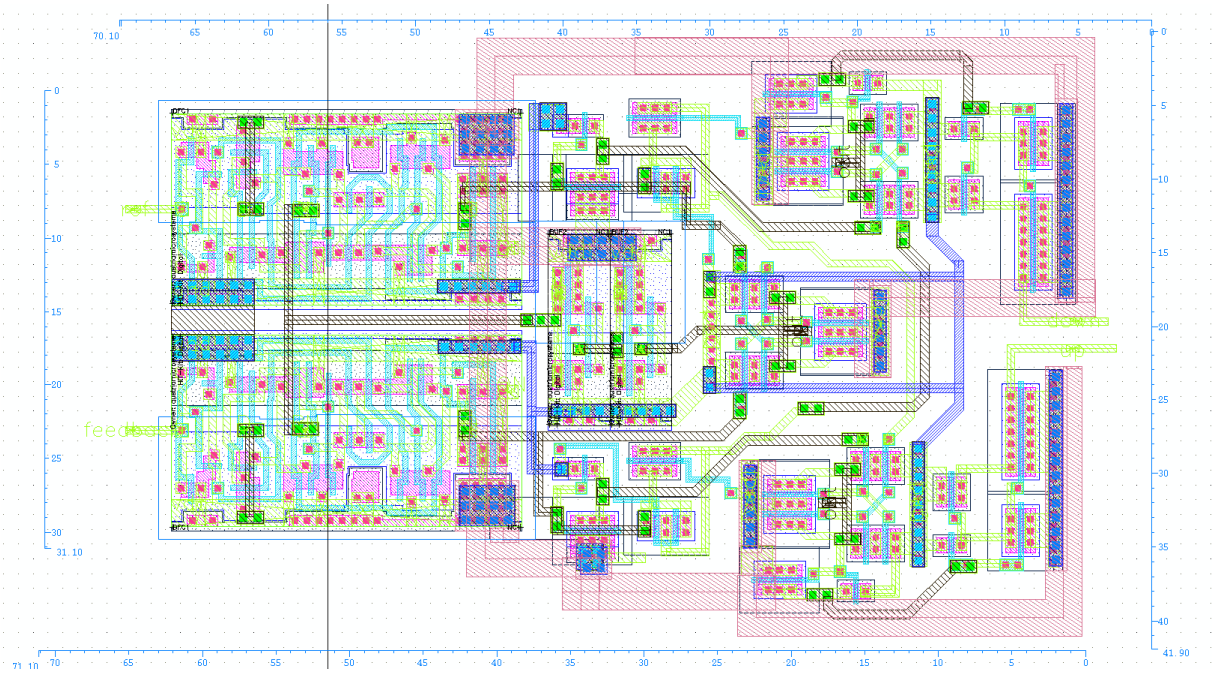
AP 32: Phase Noise change of VCO with SQUARE switch with respect to Tune voltage at band 7



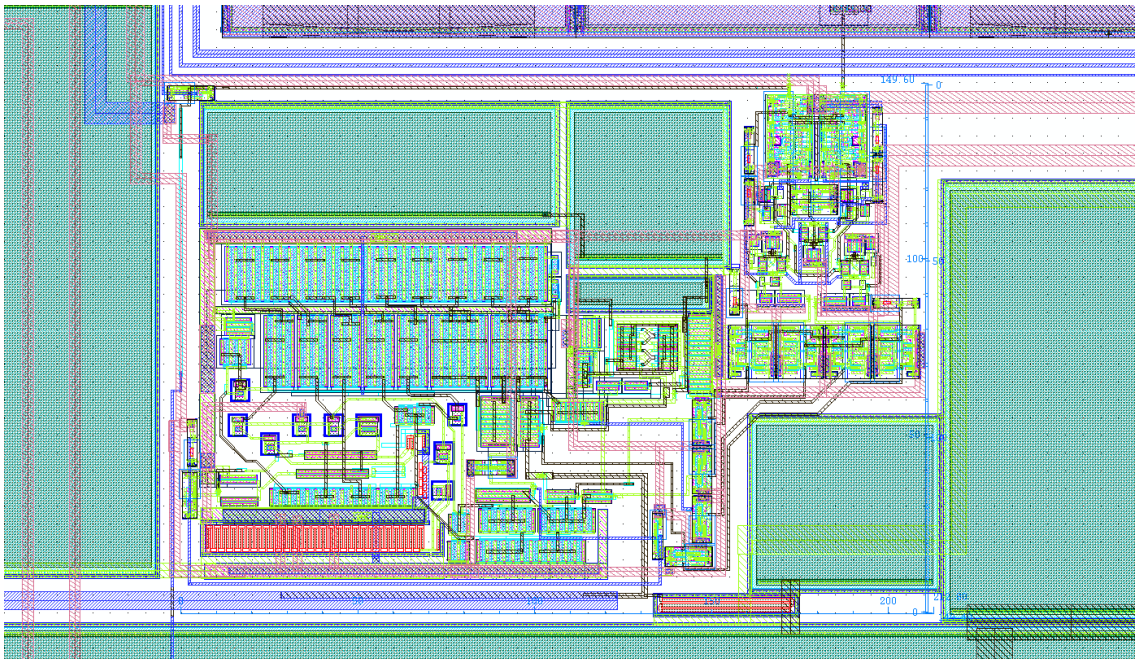
AP 33: Phase Noise change of VCO with SQUARE switch with respect to Frequency at band 6



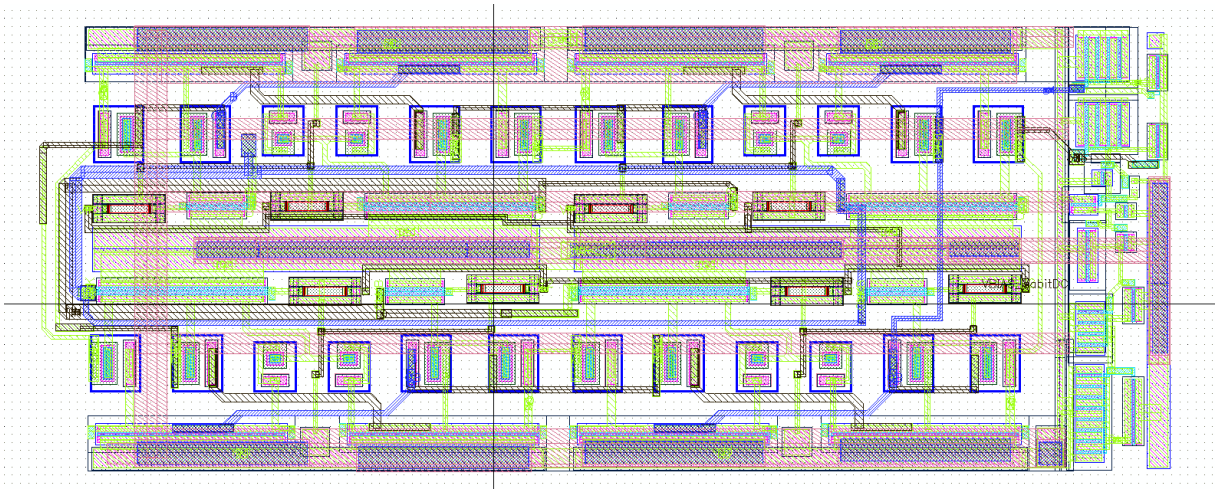
AP 34: Layout of Charge Pump



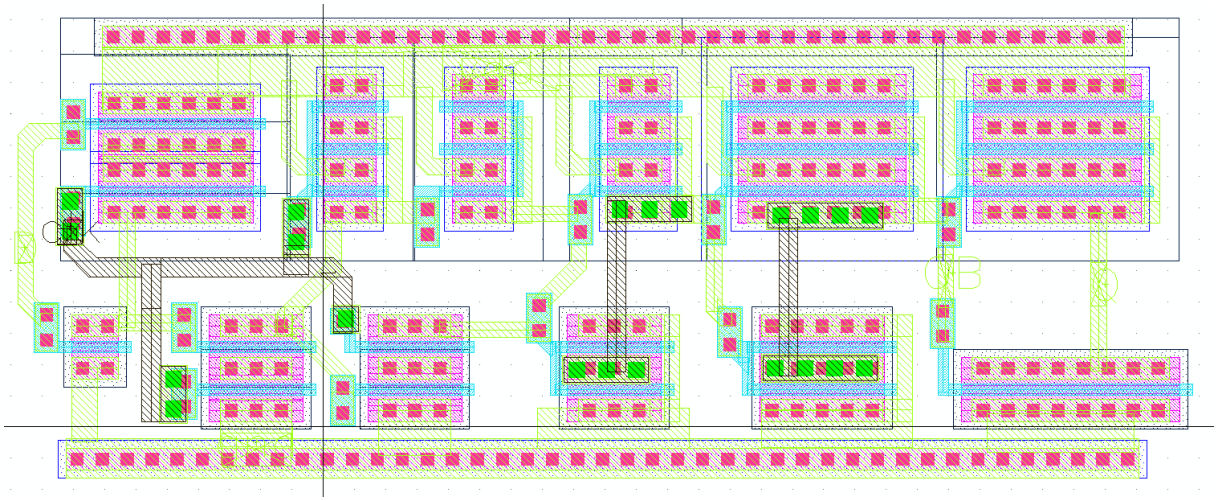
AP 35: layout of Phase frequency detector



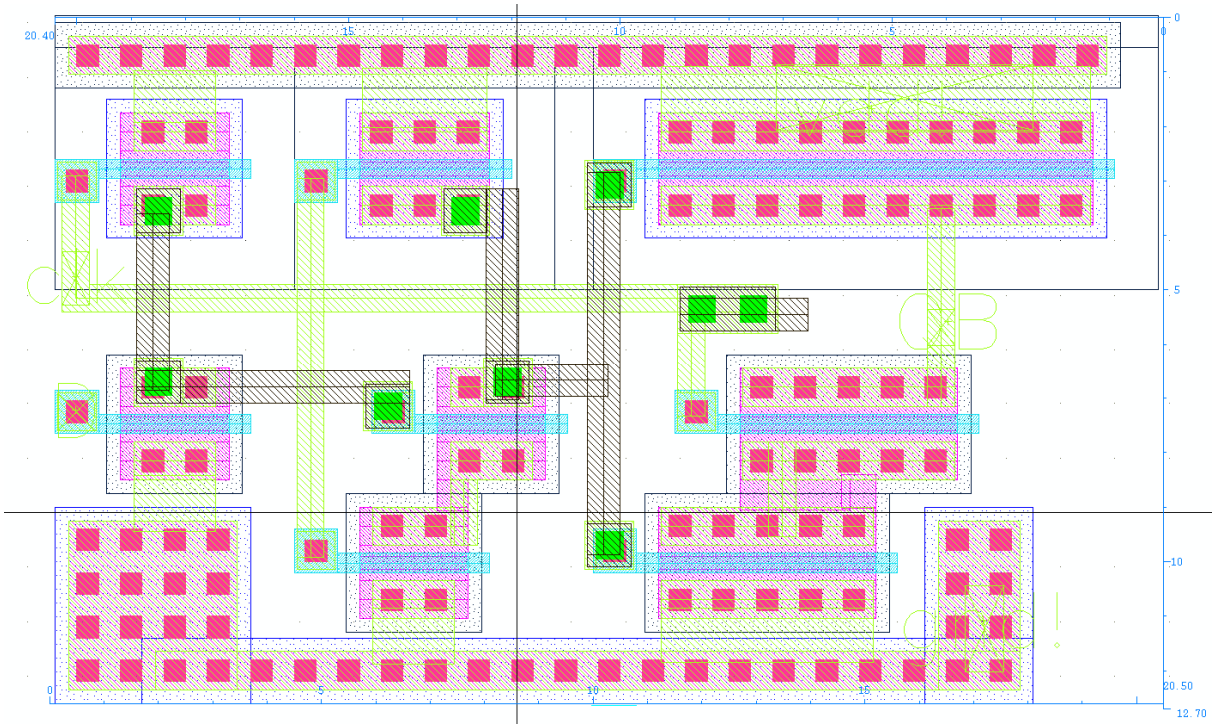
AP 36: Layout of Integrated Phase Frequency Detector inside the circuit.



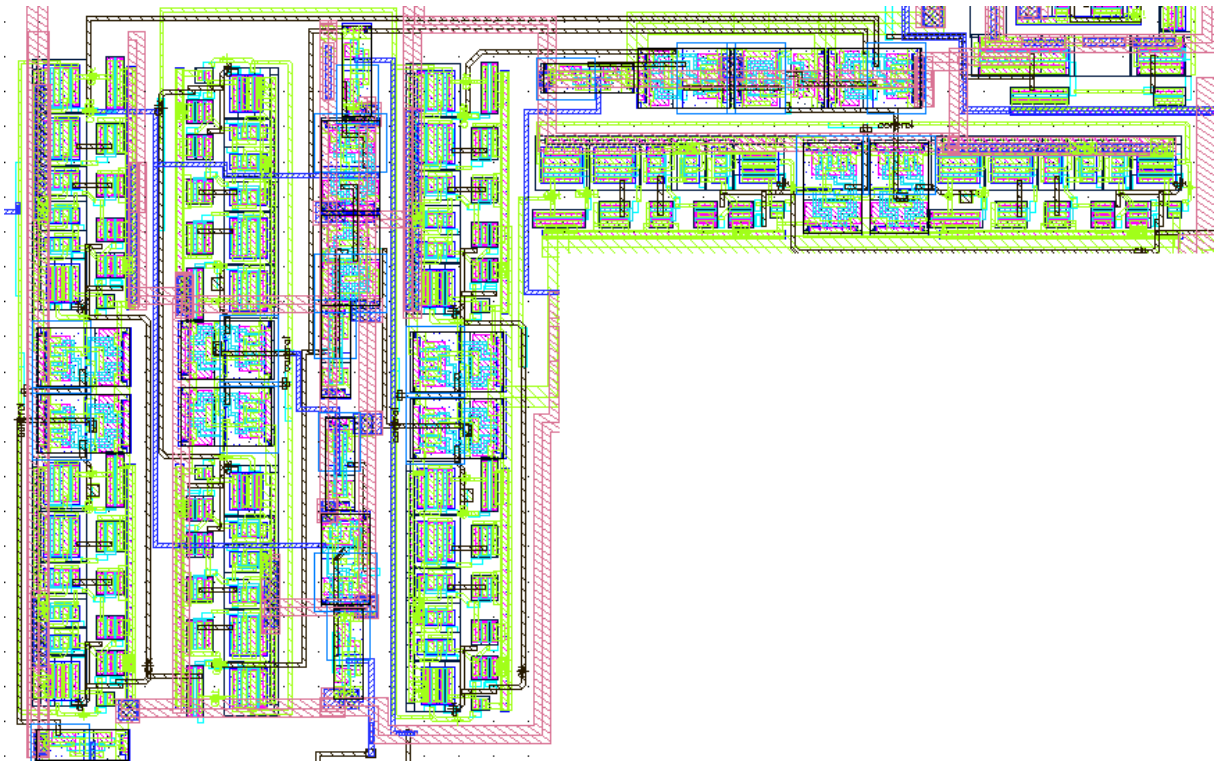
AP 37: Layout of fixed Frequency divider



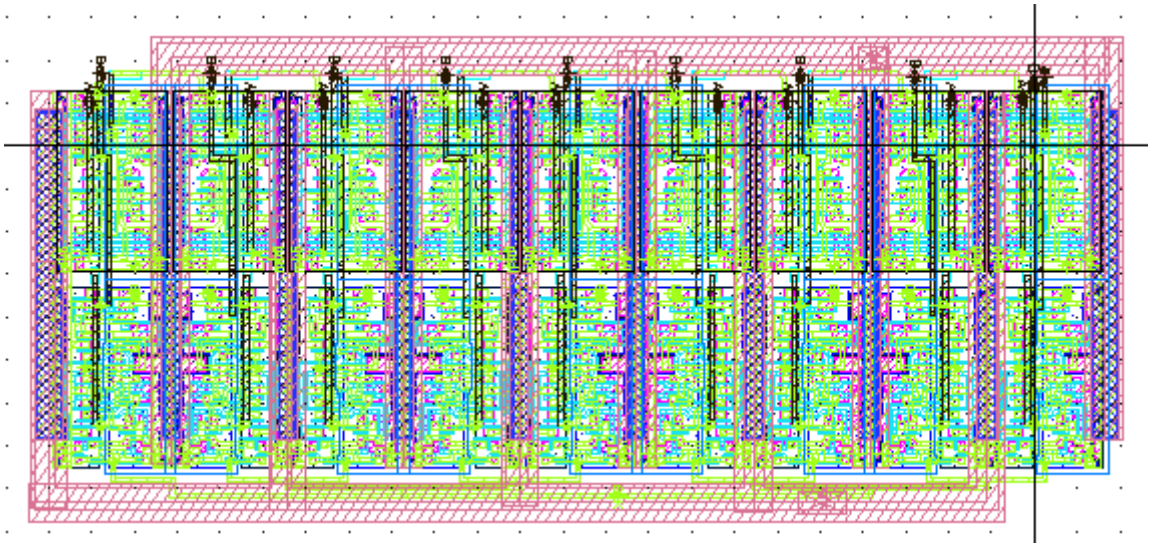
AP 38: Layout of Large TSPC flip flop



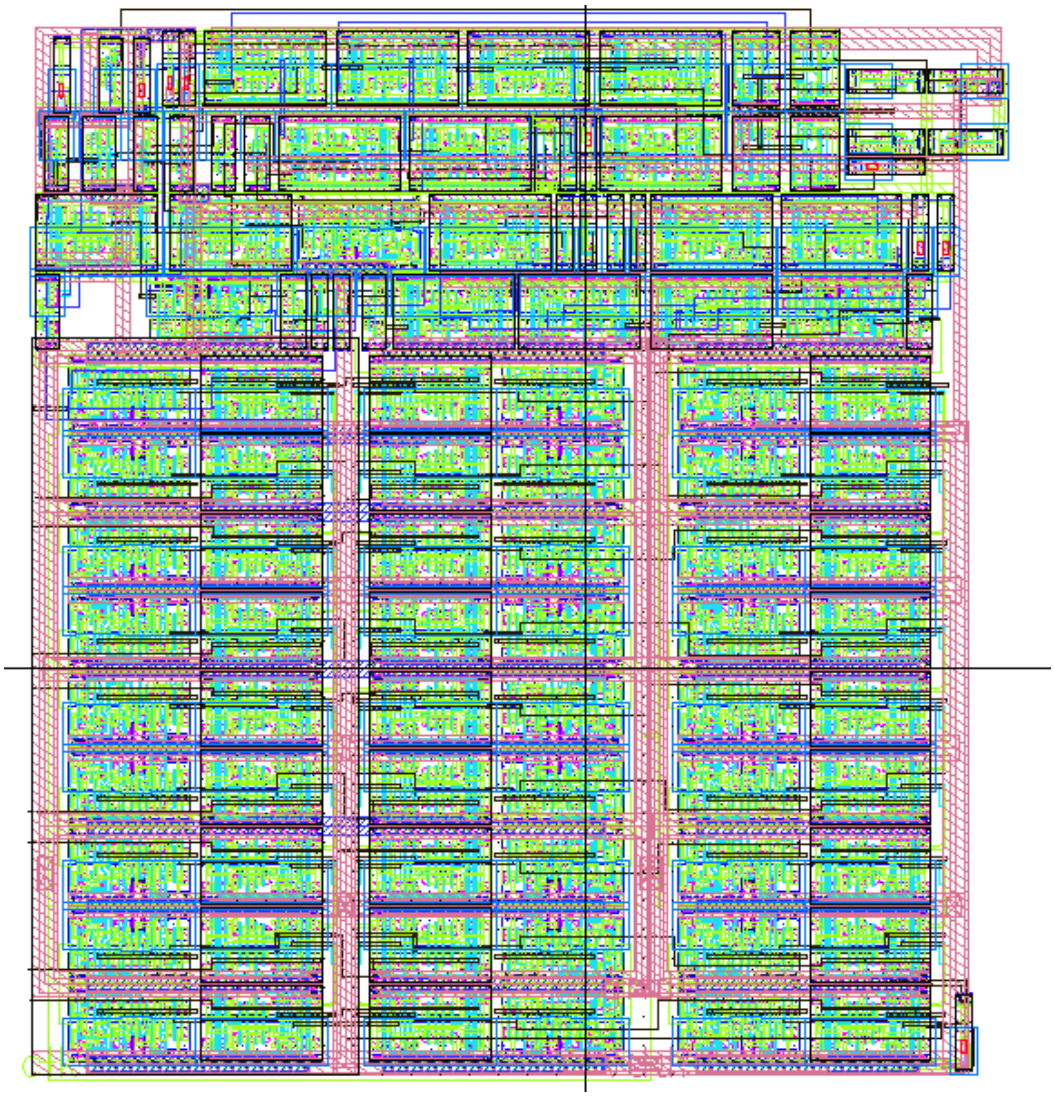
AP 39: Layout of small TSPC flip flop



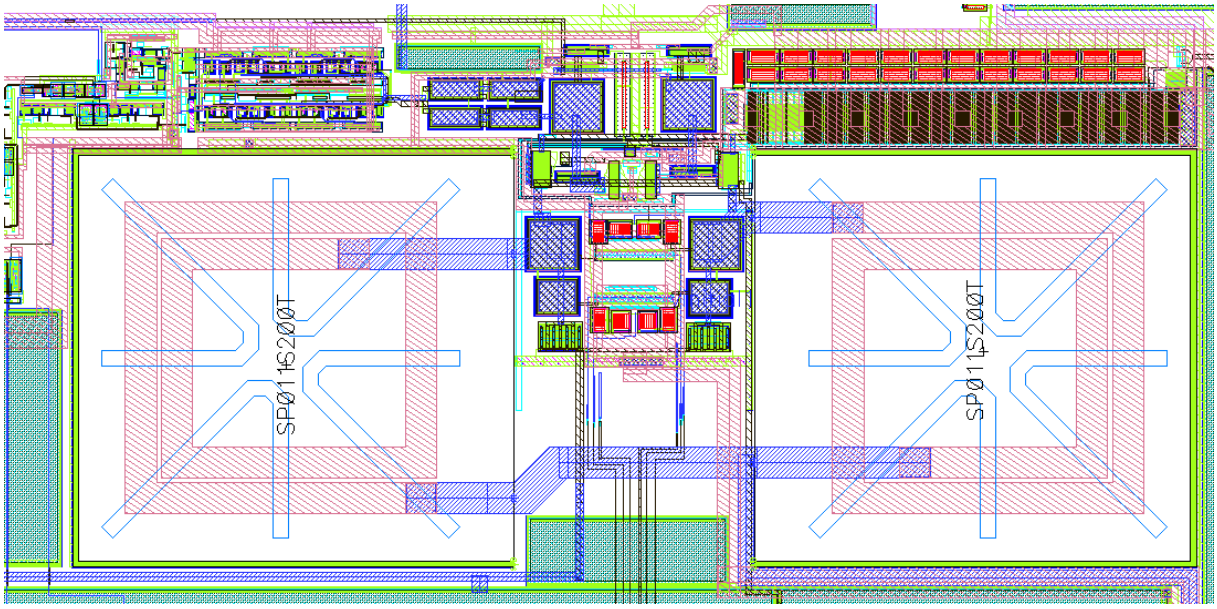
AP 40: Layout of Programmable frequency divider



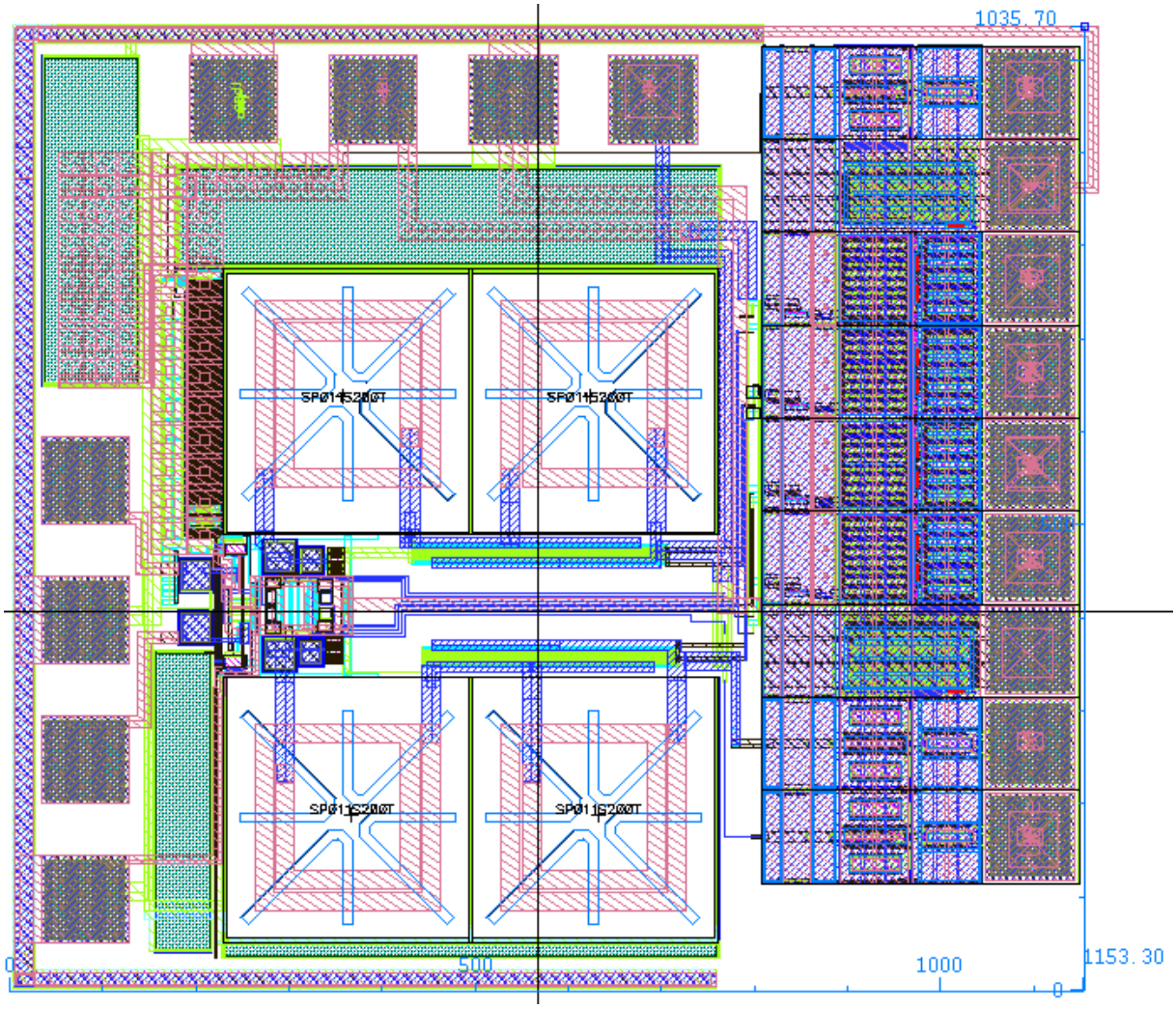
AP 41: Layout of Accumulator



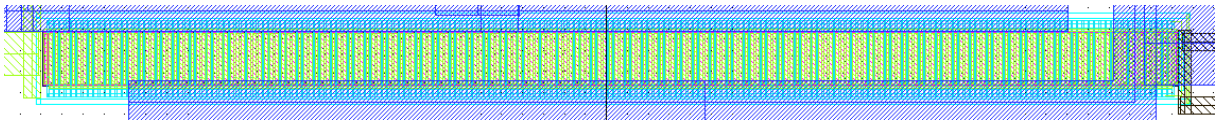
AP 42: Layout of Sigma Delta modulator



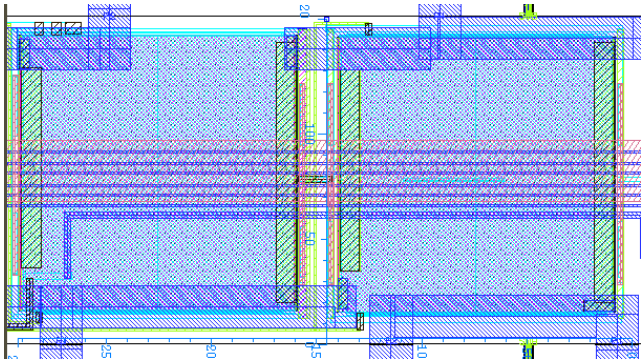
AP 43: Mask layout of VCO of PLL



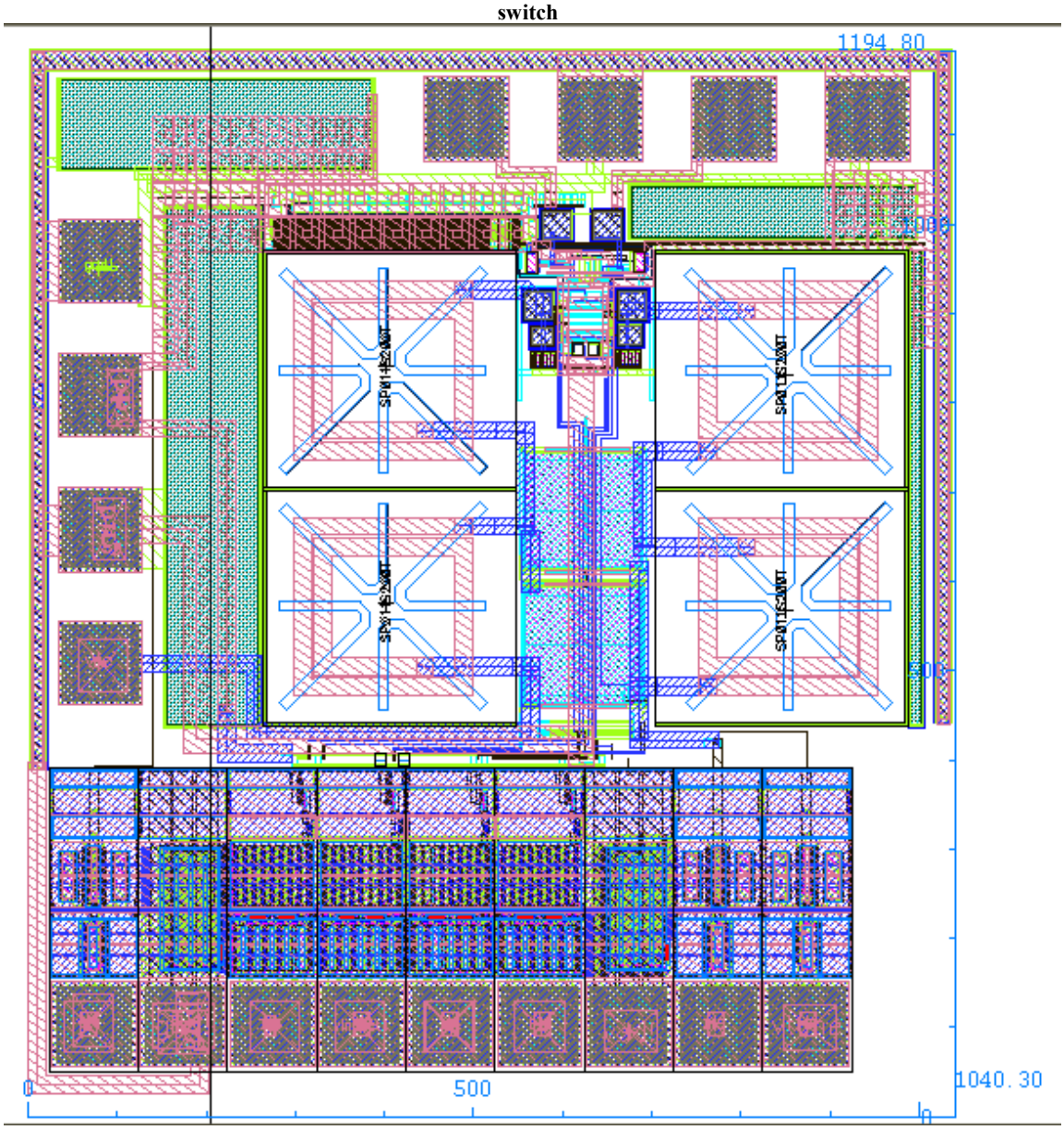
AP 44: Layout of LARGE switch based VCO



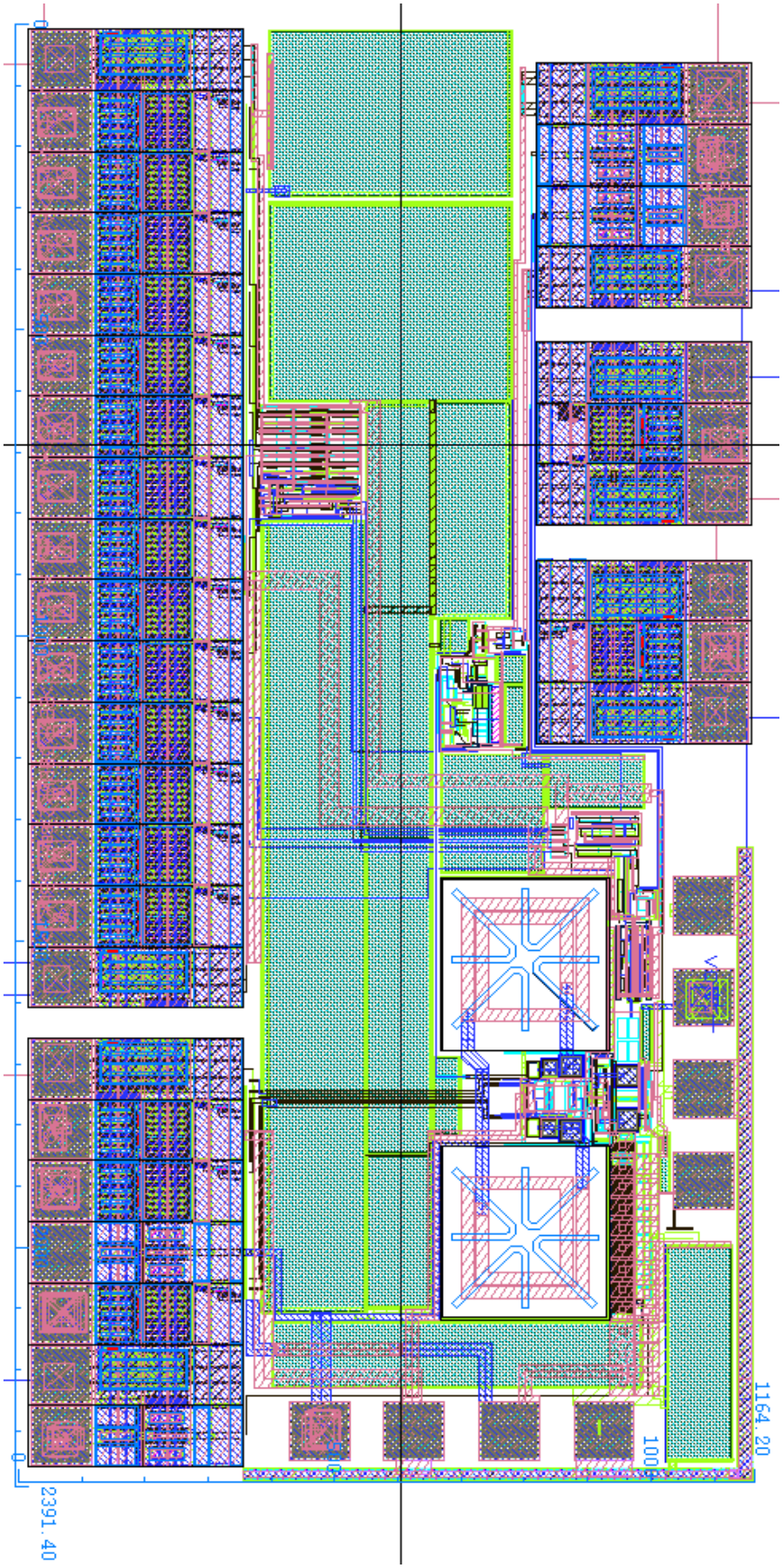
AP 45: Layout of LARGE switch



AP 46:Layout of SQUARE switch



AP 47: Layout of LARGE switch based VCO



AP 48: Layout of PLL

C DC operating points of Mos switches calculated at Spectre Cadence®

C1. SQUARE switch is On	C2 LARGE switch is On	C3 LARGE switch is Off	C4. SQUARE switch is Off
betaeff 179.9u	**betaeff** 1.001	**betaeff** 1.066	**betaeff** 191.5u
cbb 11.91p	**cbb** 499.8f	**cbb** 960f	**cbb** 21.43p
cbd -15.74p	**cbd** -98.83f	**cbd** 36.47a	**cbd** -10.04y
cbdbi -15.65p	**cbdbi** 1.501p	**cbdbi** 1.6p	**cbdbi** 83.47f
cbg -91.74f	**cbg** -2.701f	**cbg** -960.1f	**cbg** -21.43p
cbs 3.915p	**cbs** -398.3f	**cbs** -288.5e-27	**cbs** 813.8a
cbsbi 3.998p	**cbsbi** 1.201p	**cbsbi** 1.599p	**cbsbi** 84.3f
cdb -7.09p	**cdb** -238.6f	**cdb** -668.7e-30	**cdb** -8.98e-27
cdd 77.47p	**cdd** 3.528p	**cdd** 390.1f	**cdd** 20.25f
cddbi 77.37p	**cddbi** 1.628p	**cddbi** -1.51p	**cddbi** -78.79f
cdg -38.42p	**cdg** -2.28p	**cdg** -390.1f	**cdg** -20.25f
cds -31.97p	**cds** -1.01p	**cds** -702.8e-27	**cds** -49.36y
cgb 2.298p	**cgb** -22.66f	**cgb** -960f	**cgb** -21.43p
cgbovl 14.29f	**cgbovl** 31.9a	**cgbovl** 31.9a	**cgbovl** 14.29f
cgd -35.92p	**cgd** -2.388p	**cgd** -390.1f	**cgd** -20.25f
cgdovl 32.58f	**cgdovl** 627.3f	**cgdovl** 390.1f	**cgdovl** 20.25f
cgg 77.01p	**cgg** 4.562p	**cgg** 1.74p	**cgg** 21.48p
cgs -43.38p	**cgs** -2.151p	**cgs** -390f	**cgs** -21.07f
cgsovl 32.58f	**cgsovl** 627.3f	**cgsovl** 390f	**cgsovl** 20.26f
cjd 83.35f	**cjd** 1.6p	**cjd** 1.6p	**cjd** 83.47f
cjs 83.41f	**cjs** 1.6p	**cjs** 1.599p	**cjs** 83.49f
csb -7.122p	**csb** -238.5f	**csb** -543e-30	**csb** -10.41e-27
csd -25.81p	**csd** -1.042p	**csd** -2.108y	**csd** -16.46y
csg -38.5p	**csg** -2.279p	**csg** -390f	**csg** -20.26f
css 71.44p	**css** 3.56p	**css** 390f	**css** 20.26f
gbd 125z	**gbd** 276.1a	**gbd** 56.74e-36	**gbd** 4.997e-39
gbs 47.96e-48	**gbs** 1.194e-45	**gbs** 1.162e-45	**gbs** 65.36e-48
gds 78.12u	**gds** 428.3m	**gds** 7.463z	**gds** 1.289y
gm 993.2n	**gm** 956.2u	**gm** 0	**gm** 0
gmbs 208.2n	**gmbs** 154.9u	**gmbs** 431.8e-27	**gmbs** 89.64e-30
gmoverid 2.13	**gmoverid** 1.951	**gmoverid** 0	**gmoverid** 0
i1 466.4n	**i1** -490u	**i1** 2.585f	**i1** 135.4a
i3 -466.4n	**i3** 490u	**i3** 2.585f	**i3** 135.4a
i4 -270.8a	**i4** -5.17f	**i4** -5.17f	**i4** -270.8a
ibd -135.4a	**ibd** -2.585f	**ibd** -2.585f	**ibd** -135.4a
ibs -135.4a	**ibs** -2.585f	**ibs** -2.585f	**ibs** -135.4a

ibulk -270.8a
id 466.4n
ids 466.4n
igb 0
igcd 0
igcs 0
igd 0
igs 0
is -466.4n
isub 368.7y
pwr 2.761n
qb -64.92p
qbd -188.6f
qbi -64.87p
qbs -188.1f
qd -17.23p
qdi -17.21p
qg 100p
qgi 99.91p
qinv 122.7u
qsi -17.83p
qsrco -17.85p
region 1
reversed 0
ron 12.69K
type 0
vbs -1.908
vdb 1.914
vds 5.92m
vdsat 366.1m
vfbeff -837.6m
vgb 3.3
vgd 1.386
vgs 1.392
vgsteff 459m
vth 932.9m

ibulk -5.17f
id -490u
ids 490u
igb 0
igcd 0
igcs 0
igd 0
igs 0
is 490u
isub 157.6z
pwr 566.3n
qb -2.75p
qbd -3.593p
qbi -2.75p
qbs -3.595p
qd -1.656p
qdi -1.236p
qg 6.057p
qgi 5.218p
qinv 438.9m
qsi -1.232p
qsrco -1.651p
region 1
reversed 1
ron 2.359
type 0
vbs -1.9
vdb 1.901
vds 1.156m
vdsat 368.3m
vfbeff -766m
vgb 3.3
vgd 1.399
vgs 1.4
vgsteff 470m
vth 929.9m

ibulk -5.17f
id 2.585f
ids 14.16y
igb 0
igcd 0
igcs 0
igd 0
igs 0
is 2.585f
isub 52.45e-39
pwr 9.827f
qb -1.047p
qbd -3.593p
qbi -1.047p
qbs -3.596p
qd 837.2f
qdi 267.2f
qg -628.4f
qgi 512f
qinv 20.65f
qsi 267.4f
qsrco 837.9f
region 0
reversed 1
ron 130.5E
type 0
vbs -1.9
vdb 1.902
vds 1.848m
vdsat 40.53m
vfbeff -781.3m
vgb 393.9p
vgd -1.902
vgs -1.9
vgsteff 10z
vth 929.9m

ibulk -270.8a
id 135.4a
ids 2.453e-27
igb 0
igcd 0
igcs 0
igd 0
igs 0
is 135.4a
isub 4.623e-42
pwr 514.7a
qb -25.82p
qbd -187.6f
qbi -25.82p
qbs -187.5f
qd 43.51f
qdi 13.88f
qg 25.73p
qgi 25.79p
qinv 5.797a
qsi 13.88f
qsrco 43.47f
region 0
reversed 0
ron 753.4Z
type 0
vbs -1.9
vdb 1.902
vds 1.848m
vdsat 35.95m
vfbeff -852.7m
vgb 393.9p
vgd -1.902
vgs -1.9
vgsteff 10z
vth 931.4m