Design of a ROIC for Scanning Type HgCdTe LWIR Focal Plane Arrays

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ABSTRACT

Design of a silicon readout integrated circuit (ROIC) for LWIR HgCdTe Focal Plane is presented. ROIC incorporates time delay integration (TDI) functionality over seven elements with a supersampling rate of three, increasing SNR and the spatial resolution. Novelty of this topology is inside TDI stage; integration of charges in TDI stage implemented in current domain by using switched current structures that reduces required area for chip and improves linearity performance. ROIC, in terms of functionality, is capable of bidirectional scan, programmable integration time and 5 gain settings at the input. Programming can be done parallel or serially with digital interface. ROIC can handle up to 3.5V dynamic range with the input stage to be direct injection (DI) type. With the load being 10pF capacitive in parallel with 1MΩ resistance, output settling time is less than 250nsec enabling the clock frequency up to 4MHz. The manufacturing technology is 0.35μm, double poly-Si, four-metal (3 metals and 1 top metal) 5V CMOS process.

Keywords: Read-out IC (ROIC), time delay integration (TDI), direct injection (DI), focal plane array, switched current (SI), current memory, flipped voltage follower (FVF), bulk driven.

1. INTRODUCTION

Infrared imaging systems are used in a variety of applications from biomedical to astronomy and strategic imaging. An infrared system composed of two main components focal plane arrays that are responsible for detecting photons in desired region and readout circuits are responsible in converting detector outputs to ADC inputs. In this work, ROIC is designed for long-wavelength infrared (LWIR) focal plane arrays.

CCD technology has been used in many linear ROIC applications because accumulation can be achieved easily. But, this choice has drawbacks of high input voltage and difficulty in designing complex systems with more programmable functions. Thanks to rapid development in CMOS technology, without degrading performance, linear ROIC's can be designed with low cost and more complex functionality [1]. CMOS technology also offers reduced assembly cost and power due to single package possibility compared to discrete approach CCD technology inherits. Single chip application also helps to improve performance [2].

There are two types of infrared imaging systems: scanning arrays and staring arrays. A scanning sensor chip assembly (SCA) includes a row of detectors by which a scene is scanned and the resulting signal is multiplexed to generate the output. To create the entire scene, the array is scanned from one field of view to the other. A second row of elements, next to the first row produces a second image of the scene with a delay in time. If the first row is delayed by this certain time period, the two images can be added, resulting in a doubled signal level and a modest increase in noise of the two frames. By adding N rows of time delay elements and performing time delay integration (TDI), the SNR of a system can be improved by $\sqrt{N}$, assuming the system is detector limited [3]. In order to increase resolution of an image, super sampling can be used.

To apply TDI on ROIC in CMOS technology, the most practical way is integrating stored charge that comes from detector on another pack of linear capacitors [3]. Most common linear capacitor structures are poly silicon (poly-Si) and metal-insulator-metal (MIM) capacitors in recent CMOS technologies. Due to need of capacitors to store integrated charges linearly, size of layout of this type of chips determined by charge storage capability of capacitors which is dominant component in chip. To reduce area of the ROIC, unit area capacitance of capacitor should be high. In this work [4] TDI for 4 detector is realized with 26 capacitors, if the same algorithm used for 7 detectors, 77 capacitors would be

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needed. Thus elimination of capacitor dependency on TDI stage significantly reduces ROIC area for a high number of element TDI algorithms. Implementing bucket brigade technique in CMOS technology enables usage of transistors as an accumulation component [5]. An alternative way of using only transistors for TDI stage in ROIC is used in this work. Integration of 7 number of TDI elements is implemented in current domain by using switch current memory structures.

In this work, silicon ROIC's for photovoltaic HgCdTe FPA is represented. Designed manufacturing technology is 0.35µm double poly-Si, three metals and one top metal CMOS process of Austria Microsystems(AMS). ROIC structure includes seven elements TDI functioning with a super sampling rate of 3, bidirectional TDI scanning, and programmable five gain settings, and programmable integration time. ROIC has a dynamic range of 3.5V for an output load of 10pF in parallel with 1MΩ, and operates at a clock frequency of 4 MHz.

The sub-circuits of the ROIC can be categorized in four main sub-sections; input stages, voltage to current conversion stage, TDI stages and digital control circuits. Input stages consist of poly-Si integration capacitors and direct integration unit cell structure which is preferred due to low noise property. With four poly-Si integration capacitors being switched according to gain settings (1, 0.9, 0.5, 0.4 and 0.3), five different charge handling capacities can be realized. These input capacitances connected to source follower (SF) stage for converting integrated charges to voltage domain. After SF stage, converting voltage domain to current domain is required for current mode TDI stage. To realize this operation VIC stage is implemented after SF. VIC is based on simple architecture by using flipped voltage follower (FVF) concept. TDI stages consist of one current memory structure for sampling input current and 21 current memory stages to integrate super sampling property to TDI algorithm. The last stage of ROIC is an op-amp buffer to drive a load of 10pF//1MΩ within 250 ns settling time. The digital control circuit consists of a control block to create reset and TDI control signals, a 24 bit control register to program the ROIC via a serial interface and a parallel interface circuit. Digital circuit is controlled by two clock signals, CLK and INT. CLK is the master clock up to 4MHz, and INT is the integration period control signal.

2. READOUT ARCHITECTURE

The readout integrated circuit (ROIC) includes combination of analog and digital blocks. Analog blocks consist of seven current sources represents detector current for test purposes, seven DI unit cells, VIC stage, TDI stage composed of current memory structures and output buffer. The ROIC includes digital control circuit to generate required signals to drive the analog circuits according to the data in the control registers. Programming of the control registers can be done either by the parallel interface which permits only gain adjustments, scan direction and bypass mode for test purposes or by the serial interface. Moreover, digital control circuit uses 3.3V sources but transistors in analog circuit works with 5V supply voltage thus level converter is required interface between these two blocks. The readout architecture is represented as a block diagram in Figure 1 and the channel architecture is represented in Figure 2.

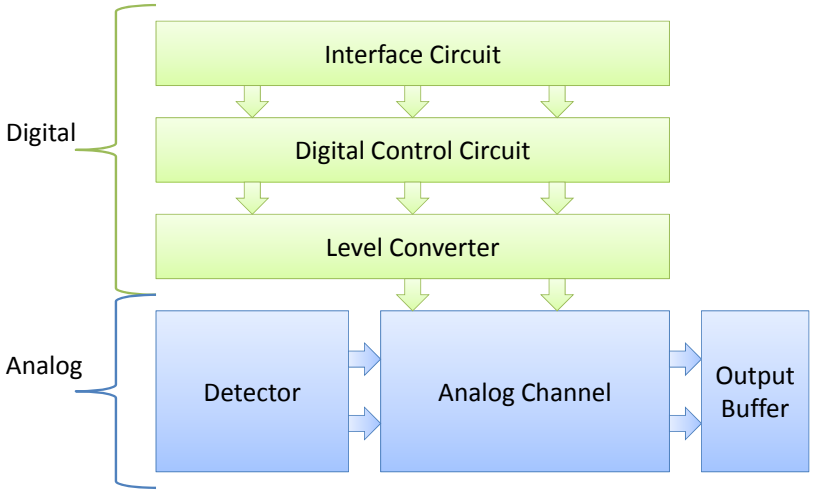

Figure 1. Block diagram of ROIC

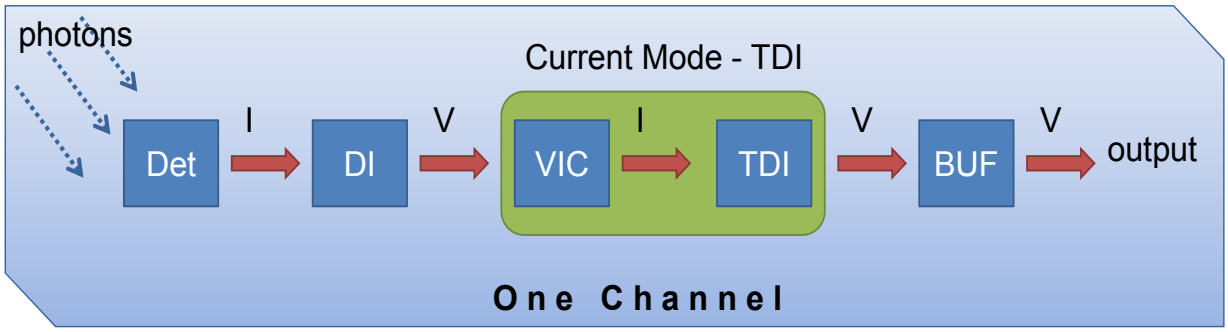

Figure 2. Block diagram of a channel consists of detector, direct injection, VIC, TDI and buffer stages.

3. CIRCUIT IMPLEMENTATION

The sub-circuits of the ROIC can be categorized in four sub-sections; input stages, VIC stage, TDI stages, digital control circuits and test structures (current sources). In the following, the details of these blocks are given.

3.1 Input stages

Input stage of the readout integrated circuit is where integration of photocurrent takes place over a capacitor. Several different circuit topologies have been studied in the literature with emphasis on various ROIC requirements dictated mainly by the detector requirements. Usually the trade off between the linearity, noise, injection efficiency, uniformity and detector bias stability set the input stage topology. Direct injection (DI) is the smallest and one of the lowest noise circuit topology. However with low-moderate impedance detectors, or in low flux applications shows poor injection efficiency. Injection efficiency problem is better solved by the use of input stages such as buffered direct injection (BDI) and capacitive trans-impedance amplifier (CTIA) topologies at a cost of higher power consumption. There are also topologies that find relatively limited use such as current mirror direct injection (CMDI) and current mirroring integration (CMI) with improved injection efficiency and good linearity at a cost of moderate power consumption and increased non-uniformity. In this work, due its smallest area and low noise performance direct injection topology is used given the high impedance detectors.

Despite the high area consumption, in order to meet the linearity requirements, poly-Si to poly-Si capacitors are preferred at the input stages. Five different gains that can vary as; 1, 0.9, 0.5, 0.4 and 0.3, is realized as shown in Figure 3 by switching the capacitors. The final in-pixel element in the architecture is the PMOS transistor of the source follower that serves as a buffer to transfer the value of the integrated voltage to the corresponding storage element in the TDI stage.

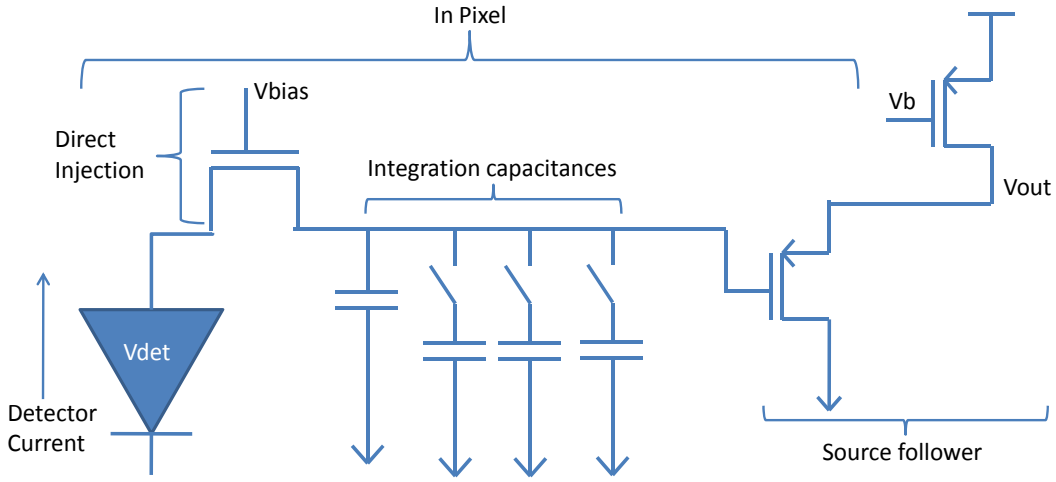

Figure 3. Schematic of input stage; DI, integration capacitances and SF structure

3.2 Voltage to Current Converter

Voltage to current conversion is essential part of this ROIC because it provides linear current with respect to integrated detector charges to the next TDI stage that will be done in current domain. Linearity of conversion and large input voltage range is very crucial and challenging design considerations of VIC. Properly designed VIC stage should cover and linearly convert large 3.5V input voltage range in this ROIC. Besides, small area is preferable property for VIC.

In this VIC, basic flipped voltage follower (FVF) architecture is used [6]. FVF architecture has some advantages over conventional voltage follower architecture such as low output impedance and nearly 1 voltage gain at the output. In the light of these properties, basic FVF architecture is used for VIC with high supply voltage in order to reach high dynamic range. Besides, FVF is driven through bulk to linearly convert voltage to current.

In this paper [7] linear VIC converter is used in system. In this structure which can be seen in Figure 4, voltage is transferred over resistor which cause to source of M2 transistor follows input voltage. In improved structure, FVF is driven on bulk of a transistor. This bulk driven structure limits range of VIC but improves linearity of conversion. Because, source of M2 transistor follows V_{in} voltage with an offset unlike first VIC. Moreover, by keeping transistors in subthreshold region and applying symmetric voltages (Vdd and Vss); high input range, low power and highly linear VIC structures is achieved.

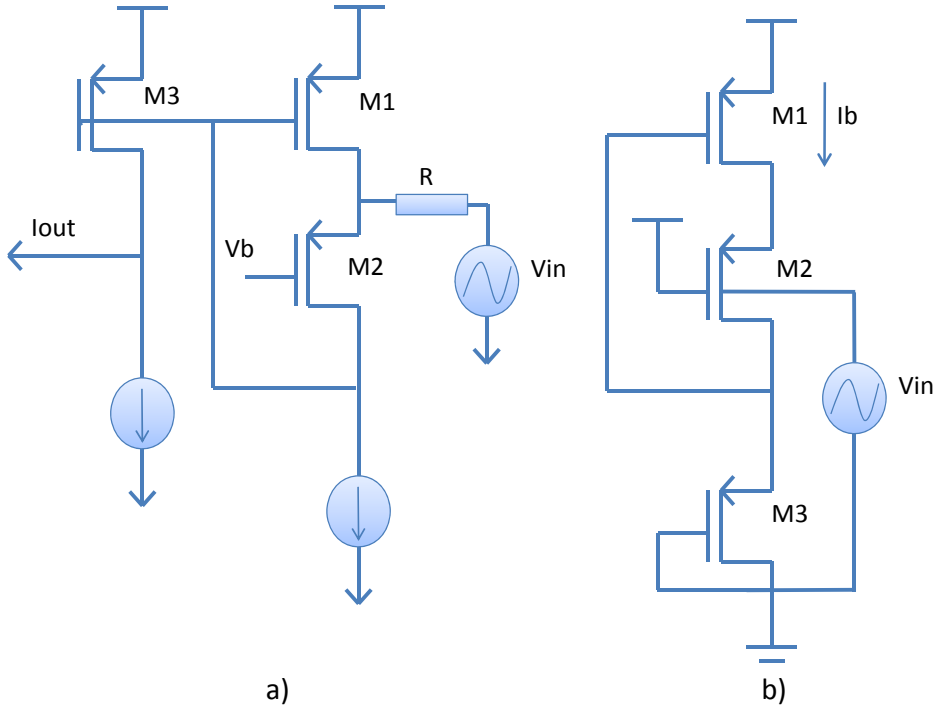

Figure 4. a) Regular FVF based V to I converter and b) New improved FVF based VIC

3.3 TDI stages

In linear ROIC circuits, TDI is used as an effective signal process for increasing the integration time and signal-to-noise ratio (SNR) of line array [8]. SNR in infrared detectors is proportional to the square root of the integration time; TDI is used as a method to effectively increase the integration time without changing frame rate and resolution. By implementing TDI technique, diodes on the same row are used to detect the same image and the signal is integrated from these photo-diodes [9]. Hence, TDI realized on N detectors, results in an improvement of $\sqrt{N}$ in SNR, effectively increasing integration time by N.

In order to realize the TDI property on seven detectors with a super sampling rate of 3, each detector should have 3 numbers of memories and in total 21 memories required. If this TDI algorithm implemented by using capacitors rather

than switched current memory architecture at least total 77 (20, 17, 14, 11, 8, 5, 2 for seven detector) capacitors required [4]. Thus, this architecture requires less area than charge storage approach.

After voltage is converted on VIC, output current is delivered to input SI cell. Input SI cell captures input current and transfers it to necessary memory SI cell. Each memory SI cell stores image information that comes from each detector to realize TDI algorithm. Firstly, input SI cell captures input current memory I_{in} with active S4 and S3 switches. While tail current (total current) is constant, I_{m1} is reduced as $I_{in.}$ Then S1 switch becomes active and S4 & S3 switches turn off. At this time, I_{in} is no longer connected to memory cell and total current should be constant, thus I_{m1} is increased as $I_{in.}$ It results integration on memory cells as follows;

$$I_{m1(n)} = I_{m1(0)} + I_{in(1)} + \cdots + I_{in(n)} \quad (1)$$

$$I_{m2(n)} = I_{m2(0)} - I_{in(1)} - \cdots - I_{in(n)} \quad (2)$$

According to equations above this operation is linear together with an offset current. This means we can linearly store and integrate detector information with only transistors. After TDI is completed no more fine adjustment like offset cancellation operation is required. Integrated current is transferred to output buffers over a resistor.

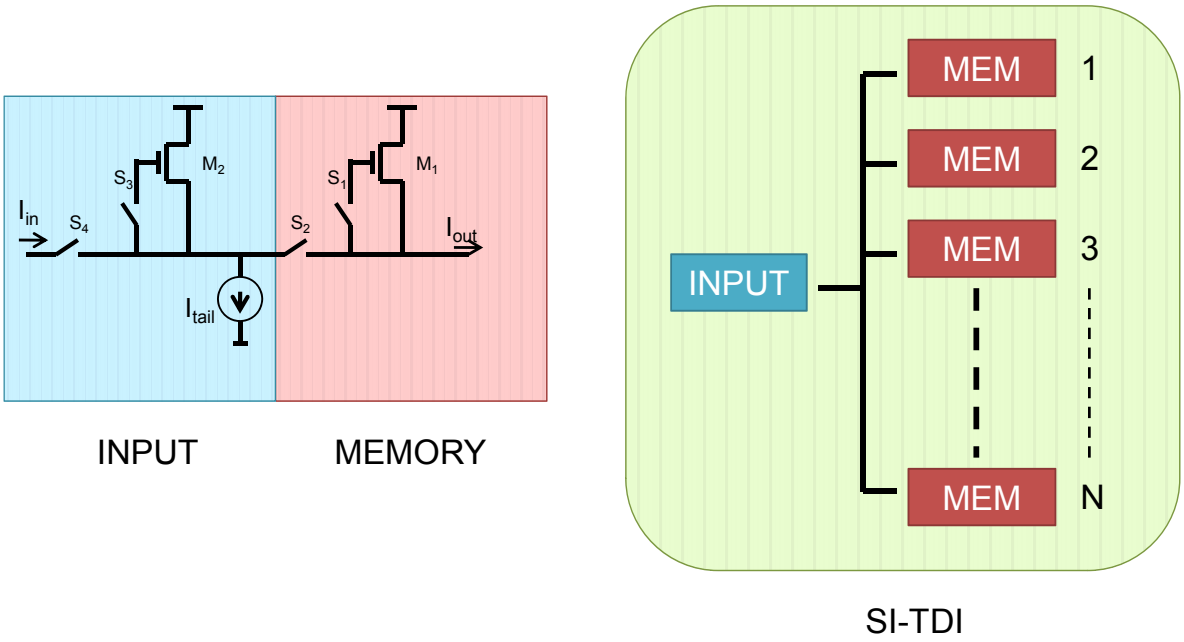

Figure 5. Switched current TDI structure, SI input and memory cells

3.4 Digital control circuits

The digital circuits consists of a control block to create reset, S1, S2, S3 and S4 signals to control TDI stage, a 24 bit control register to program the ROIC, a serial interface and a parallel interface circuit.

In order to operate, readout uses two separate clocks, INT and CLK. Integration occurs as long as the INT signal is high and frame period is defined in between the two falling edges of INT. CLK is the master clock of all digital circuitry. A frame can be 256 cycles at maximum. In order to increase integration time, CLK frequency can be reduced, with a cycle count of 76 to 256 for a frame. The maximum applicable CLK frequency is 4MHz.

The readout can be programmed through both serial and parallel interface. In parallel mode, control registers only hold the data for gain settings, TDI scan direction and bypass mode.

In addition to gain setting, TDI direction and bypass mode features, pixel deselection functionality is available through serial interface. The control register includes 8 bit address register and 4 bit data register corresponding to the functionality of the detectors addressed.

3.5 Test Structures

In order to test and measure manufactured chips in room and cryogenic temperatures without a detector process and temperature compensated current sources are designed and used. These current sources replace behavior of input currents that come from detector.

Compensation for process variation is realized by cancellation of the threshold voltage variations. Current reference can be tuned and is optimized within a range of 1nA - 50nA which is enough coverage for representing detector currents. Uncompensated conventional current sources has a standard deviation of %64.2, with this current reference for a nominal current of 25nA %8 standard deviation is observed due to process variations and mismatches. This ensures the amount of current being injected will be in a controllable range after fabrication as observed in simulations.

4. SIMULATION RESULTS

In this section, simulation results of switched current based ROIC for HdCdTe FPA LWIR FPA is presented. Simulation is done on Cadence® environment with Spectre® simulator.

In Figure 6 simulation results demonstrating the linearity performance of input stages are represented for input currents of 1nA, 5nA, 10nA, 20nA, 30nA, 40nA, 50nA. Simulation results are presented with nominal gain setting of 1 and integration time of 12.5µs for aforesaid photocurrents.

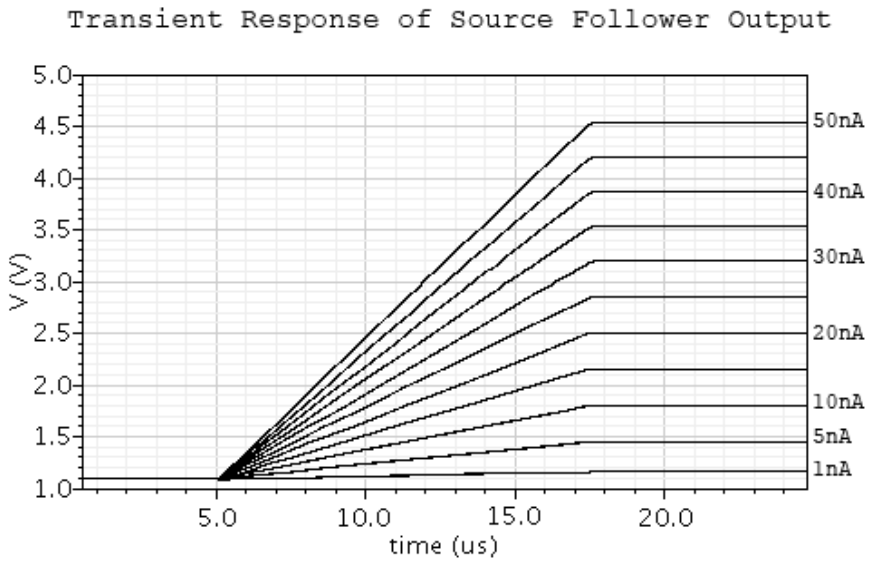

Figure 6. Simulation result with gain setting of 1, integration time of 12.5us, with an input photocurrent of 1nA, 5nA, 10nA, 20 nA, 30 nA, 40nA and 50nA

After input stage, following stage is VIC. Simulation result in Figure 7 demonstrates DC characteristics of VIC. As shown in Figure 7, VIC covers 0V to 5V input voltage range, results 610nA to 320nA output current. Linearity of VIC is the best between 0.5V to 4.3V with less than 0.02% linearity error. Output range of VIC can be adjusted according to needs of designer. This DC simulation is simulated independent from ROIC.

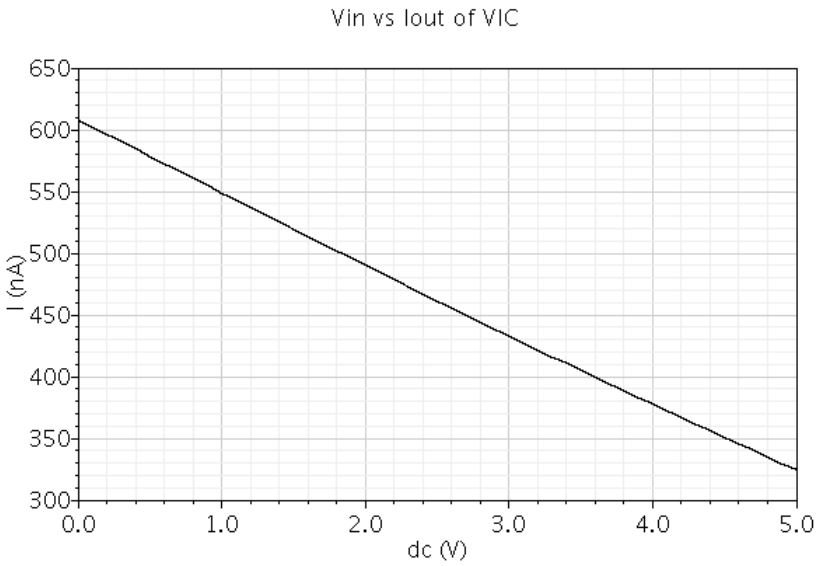

Figure 7. DC characteristics of VIC.

Another crucial stage is TDI stage, linearity of this stage is also important. Figure 8 demonstrates how SF output voltages are transferred to current memory cells on TDI. For different integrated charges on input stage with same integration time, TDI memory cells react 99.98% linearly.

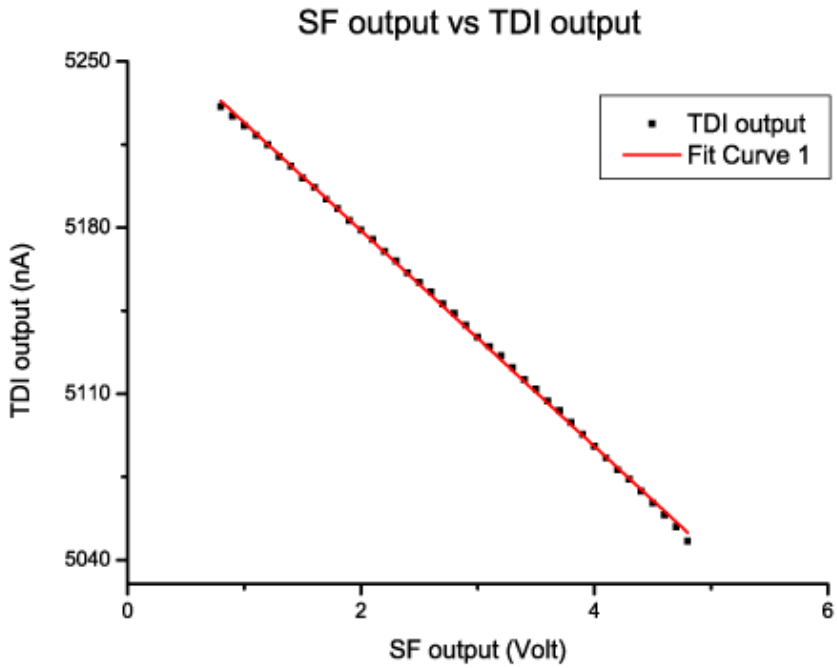

Figure 8. SF output (V) vs integrated currents on TDI memory stage (nA)

Finally, in Figure 9, seven times integrated current inside TDI stage and corresponding output result of our system are demonstrated below. Simulation is done with 5 different (10nA, 20nA, 30nA, 40nA, 50nA) input photocurrents with

same 12.5µs integration time. Output result of ROIC system is 2.89V, 3.21V, 3.53V, 3.84Vand 4.15V for 10-50nA input currents.

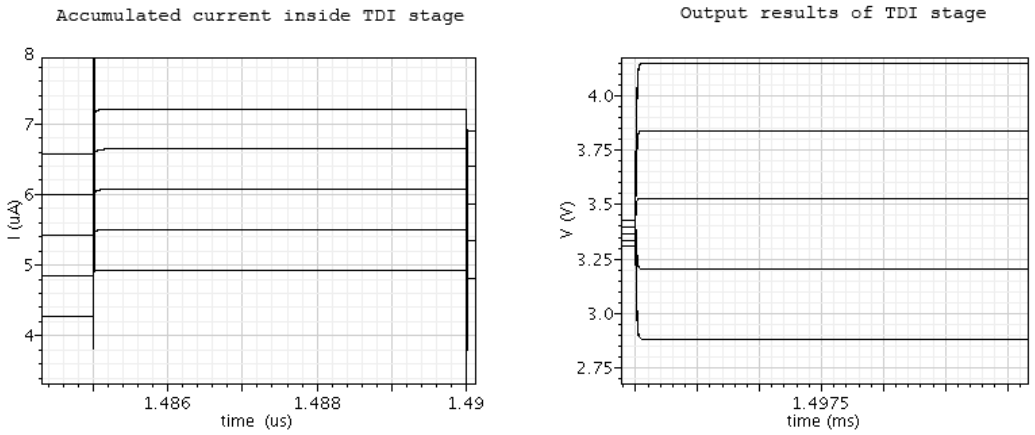

Figure 9. 7 element TDI applied result on TDI memory cell and corresponding output voltage for 10nA, 20nA, 30nA, 40nA, 50nA photocurrents

5. CONCLUSION

CMOS ROIC's for photovoltaic type HgCdTe FPA for LWIR is designed; this ROIC is also in fabrication phase for the time being. Moreover, temperature and process compensated current references are also designed replace detectors to confirm for matching simulation results with measurements. The manufacturing technology is 0.35µm double poly-Si, four metal CMOS process of AMS. ROIC structure includes direct injection input stage that contains programmable five gain settings with source follower, VIC for converting integrated charges to current domain and seven elements TDI functioning with a super sampling rate of 3. TDI operation is done in current domain by using switch current memory structures which helps to reduce chip area. Besides programmable integration time and bi directional scanning is adjusted through digital interface which is also responsible for controlling switched inside analog circuitry. ROIC has a dynamic range of 3.5V for an output load of 10pF in parallel with 1MΩ, and operates at a clock frequency of 4 MHz.

REFERENCES

[1] G. Jun, L. Weiigao, L. Jing, C. Wentao, T. Ju, C. Zhongjian, J. Liiu, "Design of High Performance CMOS Linear Readout Integrated Circuit", *Proc. Of 5th Int. Conference on ASIC*, **1**, 607-610 (2003)

[2] J. A. McNeill, C. A. Raanes, J. Stander, "A CMOS analog integrated circuit for detector readout at a 50MHz pixel rate*", SPIE Proc. Of 22nd International Congress on High Speed Photography and Photonics*, **2869** (1996)

[3] J. L. Vampola, "Readout Electronics for Infrared Sensors," The Infrared and Electro-Optical Systems Handbook, **3**, SPIE Optical Engineering, Press, 1993

[4] H. Kayahan, A. Ergintav, O. Ceylan, A. Bozkurt, Y. Gurbuz, "Realization of a ROIC for 72×4 PV-IR detectors", Proc. SPIE, Vol. 6890, 68900F (2008)

[5] F.L. J. Sanster and K. Teer, "Bucket-brigade electronics-New possibilities for delay, time-axis conversion, and imaging," IEEE J. Solid-state circuits, vol. SC-4, pp. 131-136, June 1969.

[6] R. G. Carvajal, J. Ramírez-Angulo, A. J. López-Martin, A. Torralba, J. A. G. Galán, A. Carlosena, and F. N. Chavero, "The Flipped Voltage Follower: A Useful Cell for Low-Voltage Low-Power Circuit Design," *IEEE trans on Circuits and Design I*, vol 52, no. 7, pp. 1276 – 1291, July 2005

[7] S. Karthikeyan, A. Tamminneedi, E.K.F.Lee, "Design of low-voltage front-end interfaces for switched-opamp circuits," *IEEE TCAS-II*, vol.48, no. 7, pp. 722-726, July 2001.

[8] B. Kim and H. C. Lee, "Smart TDI readout circuit for long-wavelength IR detector," **38(16)**, 854-855 (2002)

[9] J.L. Vampola, "Readout electronics for infrared sensors", SPIE OPI. Eng., 1993.3