A Fully Integrated Multiband Frequency Synthesizer for WLAN and WiMAX Applications

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***Abstract*— This paper presents a fractional N frequency synthesizer which covers WLAN and WiMAX frequencies on a single chip. The synthesizer is fully integrated in 0.35µm BiCMOS AMS technology except crystal oscillator. The synthesizer operates at four frequency bands (3.101-3.352GHz, 3.379-3.727GHz, 3.7-4.2GHz, 4.5-5.321GHz) to provide the specifications of 802.16 and 802.11 a/b/g/y. A single on-chip LC -Gm based VCO is implemented as the core of this synthesizer. Different frequency bands are selected via capacitance switching and fine tuning is done using varactor for each of these bands. A bandgap reference circuit is implemented inside of this charge pump block to generate temperature and power supply independent reference currents. Simulated settling time is around 10µsec. Total power consumption is measured to be 118.6mW without pad driving output buffers from a 3.3V supply. The phase noise of the oscillator is lower than -116.4dbc/Hz for all bands. The circuit occupies 2.784 mm^2 on Si substrate, including DC, Digital and RF pads.**

I. INTRODUCTION

Exponential growth in wireless communication systems offers wide range of applications to the customers. Among these, WLAN and WiMAX communication standard/ technologies have found largest use in indoor – outdoor communication and entertainment system applications. Future of these standards, such as IEEE 802.11n, is usage of more than one frequency band to support higher data rates (130Mb/s up to 600Mb/s). One of the recent trends in this area of technology is to utilize compatible standards on a single chip, while meeting the requirements of each, to provide systems with small size, lower power consumption and cheap cost for customers.

This paper presents a fully integrated synthesizer designed for WLAN and WiMAX applications. The system is integrated in low cost 0.35µ BiCMOS AMS technology, where the requirements for these standards can be achieved. Charge pump is designed based on 3rd order type II, phase locked loop system is chosen as frequency synthesizer architecture and second order low pass loop filter is selected to obtain unconditional stability for all frequency bands. Proposed standards are covered by a -Gm LC tank based VCO, and capacitor switching technique is used to achieve multiband-multi-standard operation [1]. In order to meet low phase noise demands of these standards, fractional N type architecture is adopted to allow high reference frequency, low division ratio and fine step size. To achieve delicate step sizes, fractional part of the division ratio is controlled by 9-bit accumulators. In order to decrease quantization noise of fractional-N division, a multi-bit output ΔΣ modulator, which has programmable order, is implemented. Multi-bit output of ΔΣ modulator needs a programmable frequency divider which has more than one division ratio. In order to satisfy this requirement a multi-modulus frequency divider is designed. In addition, this frequency divider has an important role in multiband operation with its high division range. Operating frequency of multi-modulus frequency divider is decreased by a single-ended current-mode logic based frequency divider stage. For the charge pump block of synthesizer, high output swing CMOS cascode technique is implemented. To achieve power supply independence for charge pump block, bandgap reference circuit is implemented.

II. BLOCK DIAGRAM

Fig. 1 shows the system consists of VCO, single mode frequency divider, multi-modulus frequency divider, charge pump, loop filter, phase frequency detector and an off-chip 50MHz crystal. For the first step of design, a high level model of the system is built using Matlab® - Simulink® in order to determine loop behavior and optimization of loop parameters which are shown at Table I.

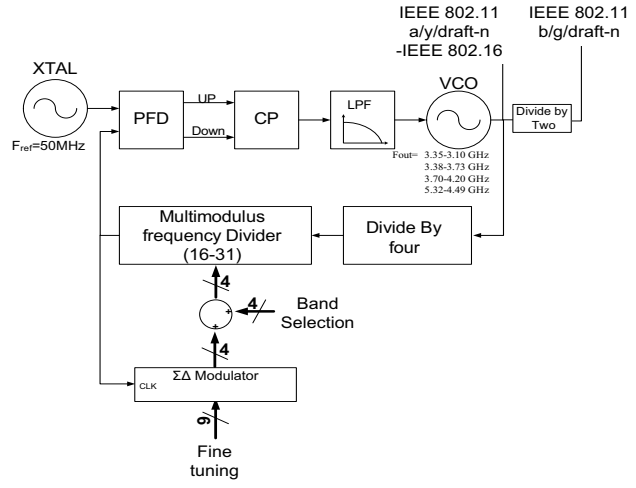

Fig. 1 Block diagram of PLL

TABLE I
OPTIMIZED LOOP PARAMETERS

Expression	Value	Unit
Gain of The VCO for band 1	0.8	GHz/V
Gain of The VCO for band 2	0.6	GHz/V
Gain of The VCO for band 3	0.37	GHz/V
Gain of The VCO for band 4	0.21	GHz/V
Loop filter Capacitor C1	384	pF
Loop filter Capacitor C2	48	pF
Loop filter resistor	7.5	kΩ
Charge pump current for band 1 and 2	104	µA
Charge pump current for band 3 and 4	270	µA
Division Ratio of the Frequency Divider Circuit	64-124	-
Loop bandwidth	267	KHz
Reference Frequency	50	MHz
Phase Margin	53º	-

III. DESIGN OF LOOP COMPONENTS

A. VCO

A non-complementary topology is selected rather than complementary cross coupled topology to decrease parasitic capacitances from complementary part and increase tuning range. -Gm configuration is implemented with PMOS transistors rather than NMOS transistors because of lower mobility and less hot carrier effect of PMOS. Moreover, power supply noise is reduced with usage of PMOS transistor based current sources [2]. Multiband approach is achieved by capacitor switching technique which has been designed with the techniques presented at [3]. The VCO that has been already reported [1] has been used in this paper and details are given in that paper. The design has good temperature and supply independency performance in four frequency bands.

B. Frequency Divider

For different frequency bands, different division values are required. In addition, multi-bit output ΣΔ modulators require frequency dividers which have several division ratios. To meet these requirements a four bit programmable divider is designed by using the techniques presented at [4]. Multi-modulus frequency divider consists of four dual modulus prescalers (DMP) (2/3) as represented at Fig. 2. These four DMPs provide a division range between 2^4 and 2^5-1. Dual modulus prescalers are designed with dynamic logic based TSPC flip flops. Dynamic logic is preferred since it provides low power consumption and high frequency operation. However, full swing rectangular input signal is required for the operation of this block. Due to the technology, this signal can be obtained in a limited frequency range which results in an additional prescaler part before this block to reduce frequency.

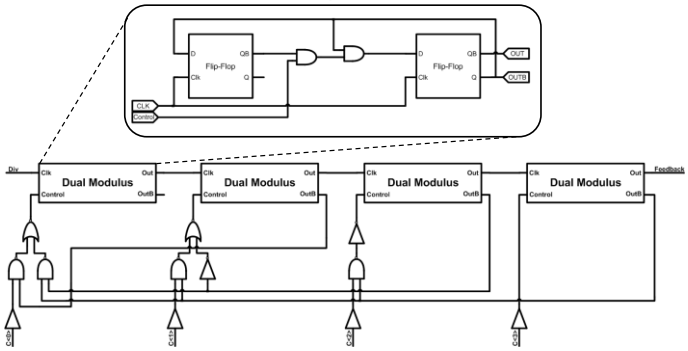

Fig. 2 Multi-modulus frequency dividers

C. Charge Pump

In general, a charge pump consists of current sources and switches. Current sources are mostly designed with MOS current mirrors. Switches can be connected any location in a charge-pump; source, gate or drain terminal of the MOS transistor. Switch-at-source causes variations in V_{GS} voltage of MOS current mirror which results in unstable output current in charge pump. On the other hand switch-at-gate suffers from high power consumption and charge pump speed degradation [5]. Consequently, drain switched topology is selected as depicted in Fig. 3 because of the advantages in high speed and stable output current at the cost of glitches. High output swing technique is applied at bias of these transistors not to limit VCO tuning range [6]. With the usage of this technique simulation results show that output current of charge pump is constant in the range 0.3V to 3V.

Output current of charge pump can vary due to power supply noise and temperature variations which can cause instabilities and current mismatches. In order to prevent these variations, band gap reference circuit which is introduced at [7] is implemented. Post-layout simulation result for power supply voltage variations on charge pump output current is given in Fig. 4(a). For the output current 104uA, less than 1% variation is simulated with proposed circuit.

D. Loop Filter

As can be seen from Table I, Gain of VCO (KVCO) changes according to operating band frequencies. Additionally, in practice, VCO gain produces additional poles to system, which makes it impossible to model with a single constant KVCO. Thus, unconditional stability of the loop must be

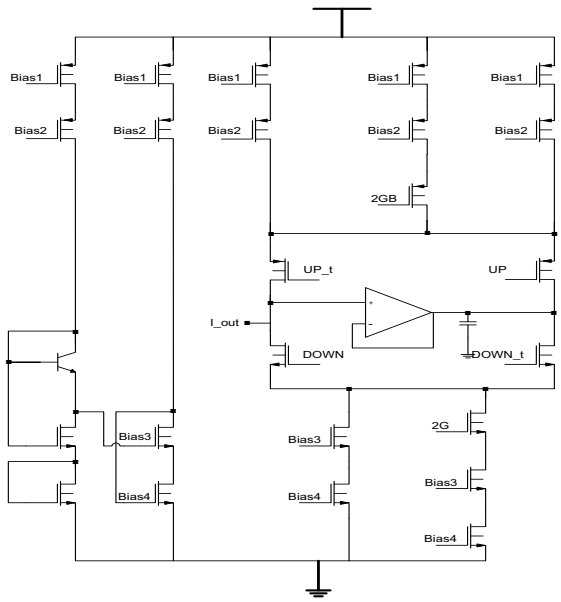

Fig. 3 High output swing CMOS charge pump circuit. Bias 1 and 2 are obtained from band gap reference circuit

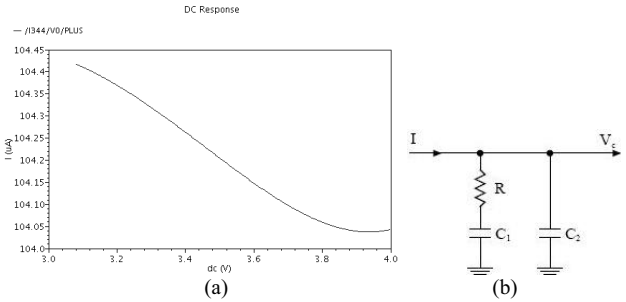

Fig. 4 (a) Output current variation of proposed charge-pump with supply voltage change, (b) Second order Loop filter

obtained for at least ideal models. This signal must be suppressed by loop filter. In consideration of these requirements, second order loop filter, which is presented in Fig. 4(b), is selected.

E. Phase Frequency Detector

Proposed phase frequency detector block, shown in Fig. 5(a), is composed of two flip flops, logic part and buffers. Reset delay is optimized with buffers to eliminate the dead zone problem. Output of the first flip flop and inverted output of the second flip flop are inputs of AND gates which generate "up" and "down" signals. Time interval of the same level "up" and "down" signals (both "up" or both "down") are reduced to the AND gate delay time to minimize current mismatch. Additionally, the transmission gate delay and inverter delay are equalized and AND gate at the output is designed symmetrically to equalize path delay.

F. ΣΔ Modulators

These structures have high pass filter behaved transfer functions, and the order of these transfer functions is equal to the number of accumulators. These transfer functions are applied to the quantization noise while attenuating low frequency components. Higher order ΣΔ modulator has better attenuation of quantization noise at low frequencies while high frequency components are suppressed by loop filter. However, for a better suppression at high frequencies, higher order loop filters are required for higher order modulators which results in degradation of stability and increase of complexity.

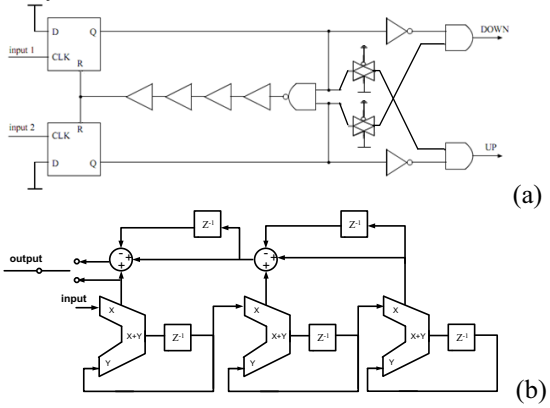

Fig. 5 (a) Phase frequency detector , (b) ΔΣ topology used in design which provides selectivity between Accumulator and MASH 1-1-1

Introduction of 90^0 phase shift by each integrator brings about 270^0 phase shift for oscillation in three stage cascade integrator. In this design, for a stable triple integration, a MASH 1-1-1 configuration that uses cascade of three stable first order sigma delta modulators is implemented [8]. This topology is also one of the best topology in terms of close in noise shaping (low frequency attenuation). In addition, it operates at high speed, consumes small area at the cost of reasonable high frequency attenuation and lots of artificial tones [9]. Moreover, output variations 4 bits-output modulator causes large instantaneous phase error [10]. For this reason, a switch has been added to select this topology or a first order ΣΔ modulator as shown in Fig. 5(b).

IV. Post-Layout Simulation and Measurement Results

The circuit has been integrated in 0.35µm BiCMOS AMS technology, operating with 3.3V supply voltage. The layout and photograph of the frequency synthesizer including a multi-band VCO, frequency divider, charge-pump, loop-filter, phase frequency detector and ΣΔ modulator is already labeled in Fig. 6(a) and Fig. 6(b) respectively. Size of the chip is 1.164mm x 2.391mm including digital and RF pads.

Oscillator output frequency spans between 5.32-4.49 GHz for band-1 and frequency tuning range is around 15% of central frequency. With additional switching capacitances, operating frequency can be tuned to 3.35-3.1 GHz for band-4, with a tuning range of 7.7%. Phase noise of the circuit varies with respect to tuning voltage. According to the simulation results, maximum phase noise at 1MHz offset is -109.6dBc/Hz. Simulation is run for band-1 and the data input of ΣΔ modulator is set to zero for this simulation. Maximum 3mV amplitude variation at control voltage is simulated with a settling time around 10µs. For this simulation, eye diagram is shown in Fig. 8. Output jitter is around 44.56fs for 1µs period after settling achieved.

Simulated performance summary of the synthesizer can be found in Table II. Power dissipation is around 118.585mW where pad driving buffers for test purposes are not included.

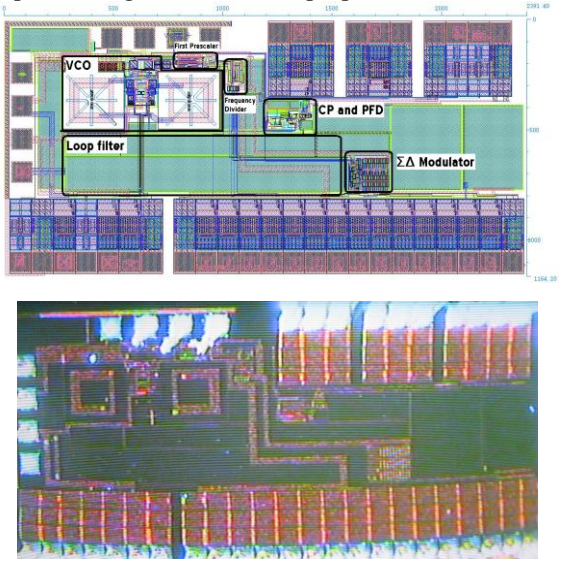

Fig. 6 (a) Layout and (b) the photo of the chip

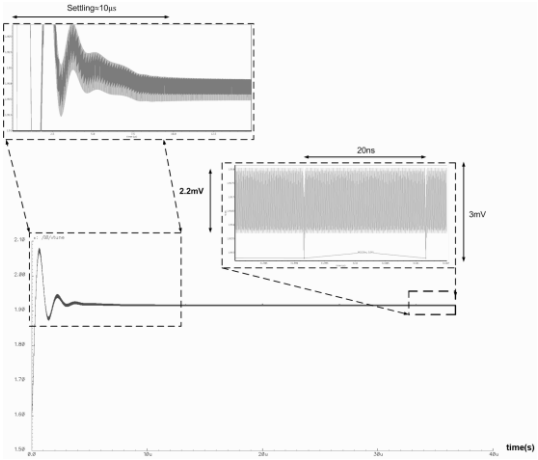

Fig. 7 Settling behavior of PLL for integer N type at Band 1

After the fabrication the circuit operates at one of the proposed bands. Measurement results for frequency range 4.26-5.1GHz is available and the measured output spectrum at 4.978 GHz with a divider division value of 25 is shown in Fig. 9. The output power of the PLL is measured as -6.236dBm. Multiband operation could not be obtained after fabrication because output voltage of the VCO in lower bands is smaller than expected. As it is mentioned before, at least rail to rail 1V signal is required for the first frequency division block. One of the first reason of this small oscillation amplitude can be unexpected parasitic that loads LC tank which decrease LC tank quality factor and oscillation amplitude.

V. Conclusions

A Fully integrated 3.1-5.3 GHz Multiband ΣΔ frequency synthesizer is designed for covering WiMAX and WLAN frequencies for Wireless Communication systems, utilizing 0.35-µm SiGe BiCMOS technology. First of all, these results show that minimum 118mW power dissipation of this work is higher than these state-of-art designs. This reasonable power consumption is rooted from technology limitations. On the other hand, phase noise (maximum -109.6dBc/Hz, minimum -123.8dBc/Hz @ 1MHz offset) and area consumption (2.784 mm^2) including on chip loop filter and pads (RF, DC and digital) of this work are comparable with literature. Finally, this work is remarkable with its high frequency coverage range (3.2-5.32GHz) and fast settling time (<20 µs).

TABLE II
SIMULATED SYNTHESIZER PERFORMANCE SUMMARY

Technology	0.35µm BiCMOS			
Vsupply	3.3 V			
$f_{reference}$	50 MHz			
Freq. Resolution	391 KHz			
	Band 1	Band 2	Band 3	Band 4
Output Freq. (GHz)	5.321-4.492	3.7-4.2	3.379-3.727	3.352-3.101
Phase Noise of VCO (dBc/Hz @ 1 MHZ)	(-117.4, -112.4)	(-120, -116)	(-116.9, -109.6)	(-123.8, -122.5)
Total Power Dis.	118.585mW: 154,12mW			
Jitter	44.56 fs			
Settling Time	<20µs			
Area	2.784 mm^2			

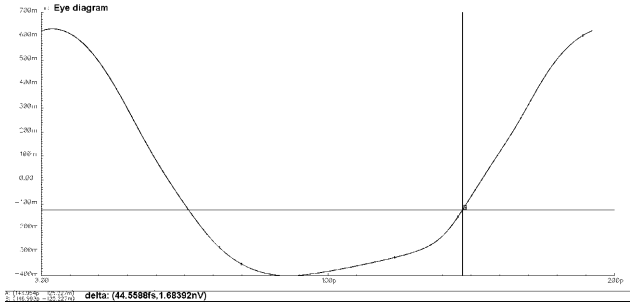

Fig. 8 Eye diagram of PLL for integer N mode at Band 1, peak to peak jitter is around 44.56fs

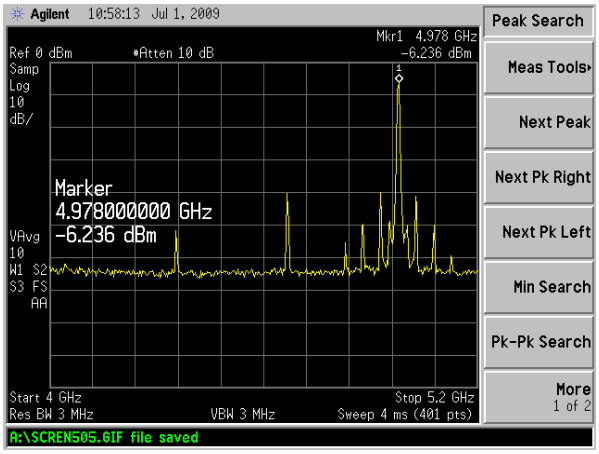

Fig. 9 PLL measurement result for 4.978GHz. Output power is -6.236dBm

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