A Tunable X-Band SiGe HBT Single Stage Cascode LNA

Mustafa DOGAN[1,2]
[1] TUBITAK – UEKAE, ETTM – EMC Division
Kocaeli, Turkey
mdogan@uekae.tubitak.gov.tr

Ibrahim TEKIN[2]
[2] Sabanci University
Faculty of Engineering and Natural Science
Istanbul, Turkey
tekin@sabanciuniv.edu

***Abstract*— This paper presents an X-band silicon-germanium (SiGe) single stage cascode tunable low-noise amplifier (LNA) for active phased array transmit/receive modules. LNA is implemented by using IHP SiGe heterojunction bipolar transistors (HBTs) 0.25-µm SGB25V technology. Cadence is used in collaboration with ADS during schematic and layout design and the results depict that designed LNA dissipates 15.36 mW from an 2.4 V DC power supply and the maximum gain around 18 dB in X-band while not exceeding the 2.4 dB noise figure (NF). Reverse gain of the LNA is very low (<-40 dB). Input terminal is matched so that S_{11} is below -10 dB in X-band.**

Keywords- Low-noise amplifier (LNA); silicon-germanium (SiGe); heterojunction bipolar transistor (HBT); noise figure (NF); X-band.

I. INTRODUCTION

The need for transmitting high power to far distances in the desired direction and improving the receiver sensitivity to any incoming signals increases the number of antenna elements that are used in phased array antenna systems. Each antenna element needs separate feeding structure to control the individual amplitude and the phase.

Currently most phased array antenna systems are active which means that they have solid-state T/R module to feed each antenna element [1]. Military systems require high power transmission therefore they require semiconductors that can handle large current and power. Unfortunately, these systems are highly expensive to manufacture and operate. Phased array systems that are for civil applications are highly focused on the reducing the cost while improving the efficiency by implementing T/R modules with affordable integrated circuit technology such as SiGe HBT [2].

Silicon-Germanium (SiGe) HBT technology improves the transistor efficiency while keeping the manufacturing cost as low as possible. Since the SiGe HBT technology reaches 300 GHz peak cutoff (f_T) and oscillation frequency ($f_{\max}$), it is now commonly used microwave and millimeter-wave phased array systems [3]. SiGe technology now combines the performance of previous semiconductor technologies with additional advantages such as high integration, high yield and low cost [4].

This letter presents design and implementation steps of an X-band silicon-germanium (SiGe) single stage cascode tunable LNA for active phased array antenna systems transmit/receive modules. LNA is implemented by using IHP SiGe HBTs 0.25-µm SGB25V technology. Cadence is used in collaboration with ADS during schematic and layout design and the results depict that designed LNA dissipates 15.36 mW from an 2.4 V DC power supply and the maximum gain over 20 dB in X-band while not exceeding the 2.5 dB noise figure (NF) in the whole band. Reverse gain of the LNA is very low as it is supposed to be for any amplifiers. Input terminal is matched so that S_{11} is below -10 dB in X-band.

II. CIRCUIT DESIGN

A. Schematic of Designed LNA

In the design of LNAs, there are common criteria's that the designer should take care of. These are minimizing the noise figure (NF), obtaining the maximum possible gain with enough linearity, stability, good impedance matching at the input and output terminals etc. All these design criteria's cannot be thought separate from others; they are all dependent to one another. Therefore designer should specify the importance level of each criterion to perform the best tradeoff.

The final schematic of designed LNA is given in Fig. 1. A two-transistor inductive degenerated cascode LNA is implemented due to its increased stability, low large reverse isolation, and reduced input capacitance. The input transistor Q_1 is acts as a transconductor and provides the gain of the amplifier. Designer is only allowed to change the emitter length of the Q_1. This will change the base-emitter capacitance and the input impedance which has direct effect on the noise performance of the amplifier. Adding Q_2 improves the gain performance while enhancing the isolation by reducing the Miller Capacitances. The emitter length of the Q_2 affects the output impedance. Using cascode transistor has a disadvantage of decreasing the output swing of the circuit when compared to a single transistor LNA, because cascode transistor requires additional supply voltage V_{CC}. L_E and L_B are for input impedance matching and noise matching. L_D is for loading, output matching and also biasing. C_d is used in collaboration with L_D for regulating the center frequency.

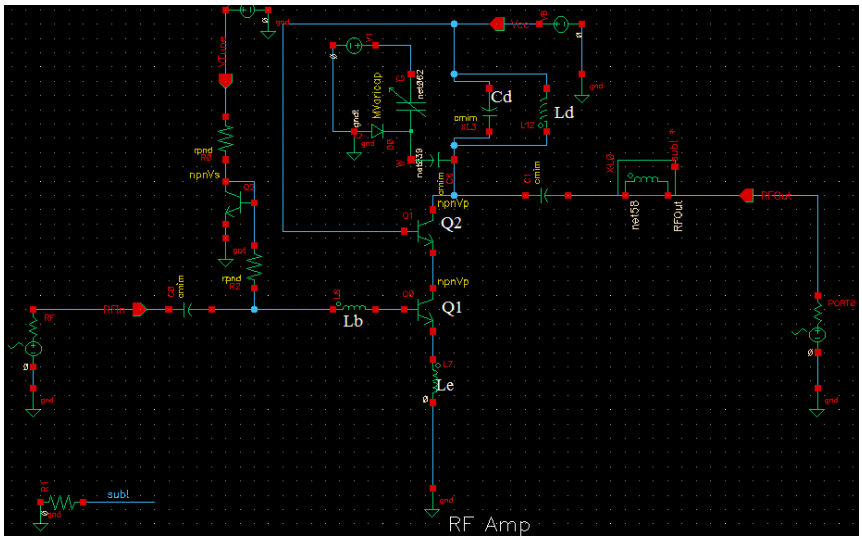

Figure 1. Final schematic of designed single stage cascode tunable LNA.

B. *Input and Noise Impedance Matching*

LNA design is done with Cadence Spectre by applying the following common design steps to match the input impedance and noise impedance in order to minimize NF and the loss due to the input reflections:

- Optimum collector current density ($J_{C,\,opt}$) at minimum NF is obtained with the most basic structures of Q_1 and Q_2 as shown in Fig. 2. Basic transistor has an emitter length of 840nm and width of 420nm. Emitter length is free to be updated and maximum 16 of BJTs will be used in parallel to lower the input impedance
- Emitter lengths of Q_1 and Q_2 are increased so that optimum source resistance is equal to the 50 Ω. By doing so resistive part of the noise impedance is matched.
- Emitter degeneration inductor, L_e, is calculated as in (1). Now resistive part of input impedance is matched.

$$L_e = \frac{R_s C_\pi}{g_m} = \frac{R_s}{w_T} \qquad (1)$$

- Base inductor of Q_1 , L_b, is calculated by the formulas given in (2) to get zero input reactance. Now both input impedance and noise impedance matching is done completely. As shown in Fig. 3, NF is very close to the minimum NF value around the design frequency.

$$L_b = \frac{1}{C_\pi w^2} - \frac{R_s C_\pi}{g_m} \qquad (2)$$

- L_d-C_d tank circuit should be specified to setup the design frequency. Output matching is done with tank circuit, DC block capacitor and the inductor used after DC block capacitor.
- Frequency tuning is going to be performed via variable capacitor which is connected to the collector of Q_2 by tuning its bias voltage.

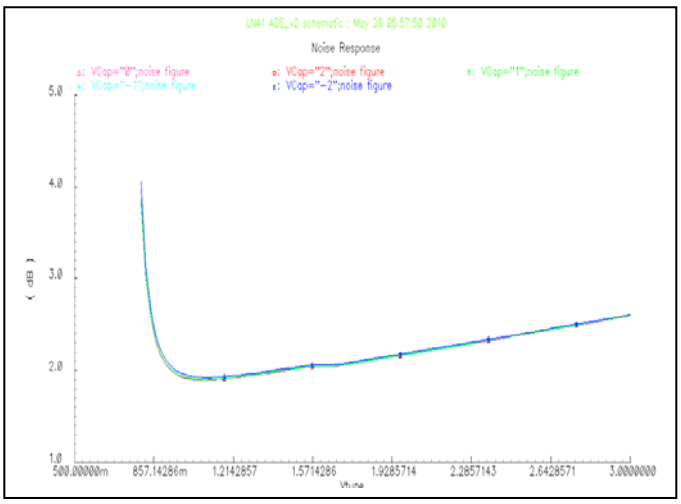

Figure 2. Optimum bias voltage for the BJTs to get minimum NF

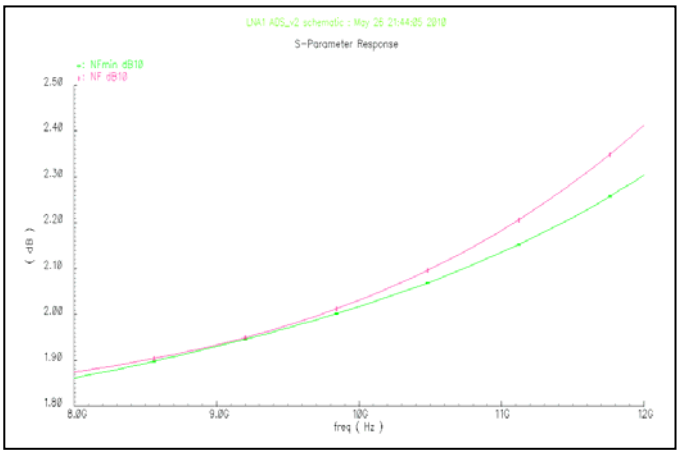

Figure 3. NF (red line) vs NF_{min} (green line) in desired frequency range

Identify applicable sponsor/s here. If no sponsors, delete this text box. (sponsors)

III. SIMULATION RESULTS AND FREQUENCY TUNING

At single frequency, designed LNA works pretty well in terms of NF, forward and reverse gain, input impedance and linearity performance. In this section by varying the supply voltage of variable capacitor from -2V to 2 V, center frequency is swept from 10 GHz - 12 GHz. In order to have a good tunable LNA design; NF, S-parameters and linearity of the circuit should not be changed significantly.

Input reflection coefficients, $S_{11,}$ are well below -10 dB for all tuning steps as shown in Fig. 4. The frequency response also gets wider and better impedance matching is obtained as the tuning frequency increases. Output matching is not as broad as input matching, it is pretty well match in proximity of the design frequency as shown Fig. 5. Opposed to the input matching, output matching gets worse as the tuning frequency increases, fortunately S_{22} gets acceptable values. As voltage of variable capacitor (VCap) decreases from 2V to -2V, center frequency shifts towards 12 GHz and gets better input impedance matching performance and worse output impedance matching performance.

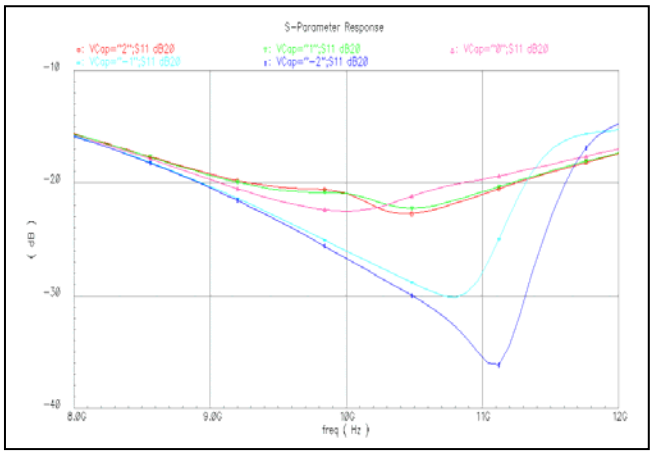

Figure 4. Input reflection coefficient of designed LNA

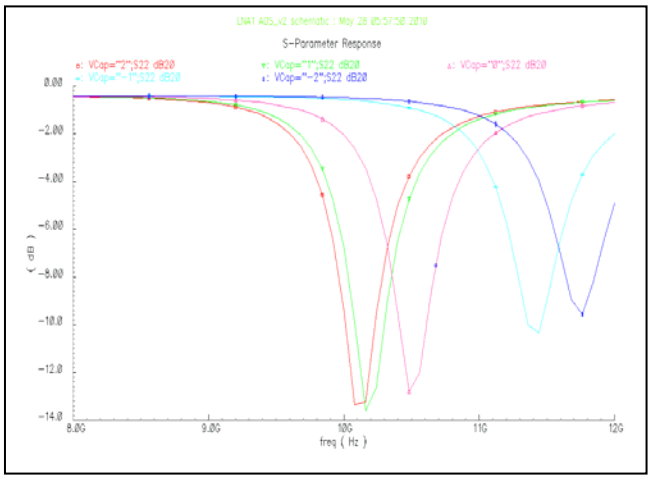

Figure 5. Output reflection coefficient of designed LNA

Gain performance of tunable LNA is given in Fig. 6. As VCap varies, the frequency which the maximum gain obtained varies and the peak gain value lowers from 18dB to 17.5dB. Tuning the VCap voltage changes the frequency but does not affect the gain performance of LNA.

One of the best important aspects of frequency tuning of LNA is that how the NF is affected as the frequency tunes. Simulation results predict that NF performance of LNA is not changed significantly while tuning the design frequency. Fig. 7 tells that as the VCap decreases from 2V to -2V, NF increases from 2.05 to 2.4 dB which is in the acceptable range for the NF performance.

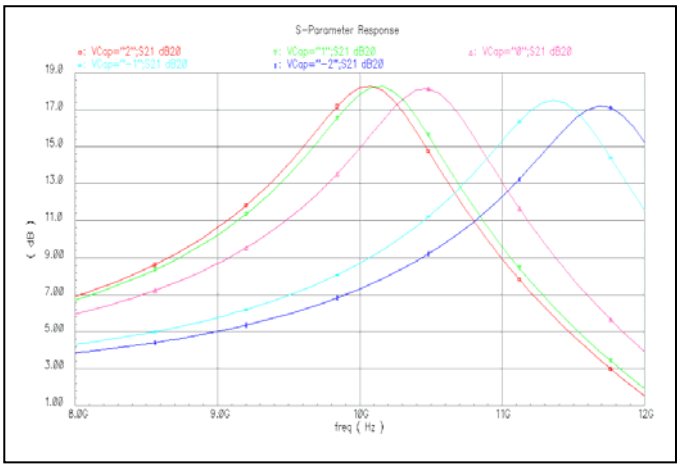

Figure 6. Gain tuning of designed LNA

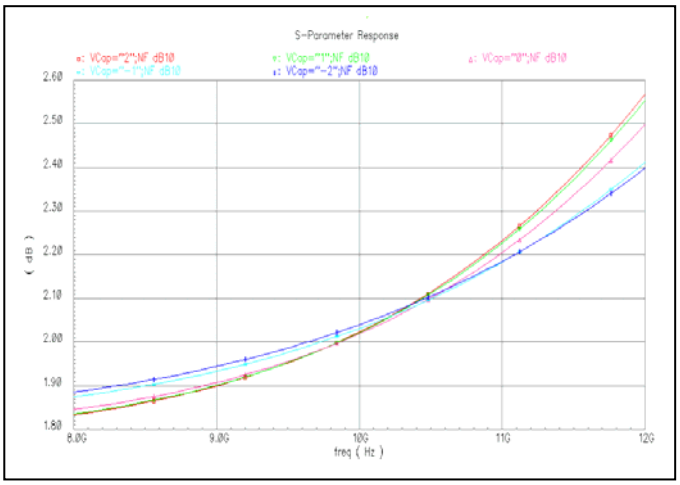

Figure 7. Variation of NF with frequency tuning

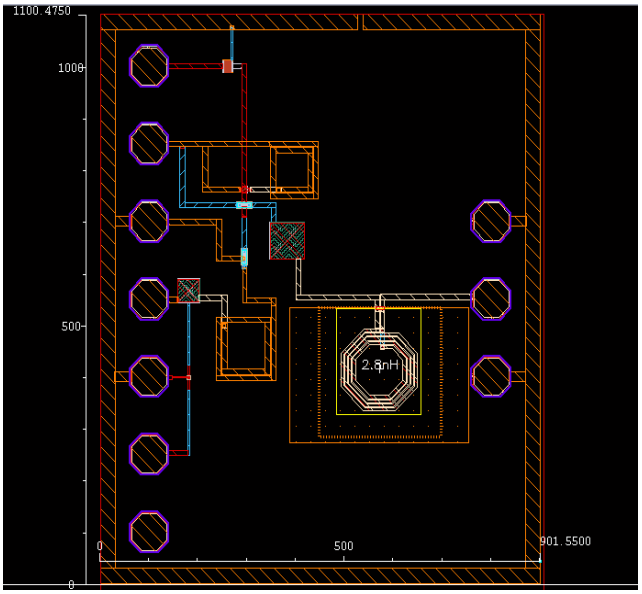

Figure 8. Complete layout of designed LNA

IV. LAYOUT DESIGN

Layout design of LNA is implemented by using ADS. The overall dimension of the LNA is *1.1 mm x 0.9 mm* including the bond metals as shown in Fig. 8. Since L_E, L_B and L_D inductors are defined in the library of the manufacturer we designed by using the spiral inductors. Since the value of L_E is small enough (150 pH), we used transmission line as a replacement. But L_B is 650pH and L_D is 500 pH, therefore spiral inductors are used to design. The advantage of ADS for layout design is that it gives opportunity for the designer to see the effect of additional transmission line (which means additional inductance and capacitance) and the effect of parasitic capacitances which are due to the crossed metal areas which are in different metal layers. Every piece of additional lines is though as 2-port networks with corresponding s-parameters. After importing them to the overall design with their s-parameters matrix, effect of additional elements is examined.

V. SUMMARY

In summary the design steps of X-band SiGe HBT single stage cascode tunable LNA is explained with details. Designed LNA demonstrates good impedance and noise performance with a gain of 18 dB. Reverse is gain very low (<-40dB) and provides good isolation between input and output.

As a future work we will perform measurements on the manufactured LNA and hopefully we will present them during the conference and compare them with simulated results.

REFERENCES

[1] R. Tang et al., “Array Technology,” Proc. IEEE, vol. 80, p 173, Jan. 1992

[2] M. Mitchell et al., “Low power density arrays” presented at 50th Annual Tri-Service Radar Symp., Albuquerque, NM, 2004

[3] J.-S. Rieh, D. Greenberg, M.Khater, K. T. Schonenberg, S.-J. Jeng, F. Pagette, T. Adam, A. Chinthakindi, J. Florkey, B. Jagannathan, J. Johnson, R. Krishnasamy, D. Sanderson, C. Schnabel, P. Smith, A Stricker, S. Sweeney, K. Vaed, T. Yanagisawa, D. Ahlgren, K. Stein, and G. Freeman, “SiGe HBTs for millimeter-wave applications with simultaneously optimized f_T and f_{max} of 300 GHz,” in IEEE RFIC Symp. Dig. 2004, pp.395-398..

[4] W.-M. L. Kuo, Q. Liang, J. D. Cressler and M.A.Mitchell, “ An X-band SiGe LNA with 1.36 dB Mean Noise Figure for Monolithic Phased Array Transmit/Receive Radar Modules,” IEEE RFIC Symp. 2006, pp. 498-501.