Impedance Matching Wilkinson Power Dividers in 0.35µm SiGe BiCMOS Technology

Ercan Kaymaksut, Yasar Gürbüz and Ibrahim Tekin

Electronics Engineering, Sabanci University, 34956 Istanbul, Turkey

e-mail: tekin@sabanciuniv.edu

Phone: +90 216 4839534, Fax: +90 216 4839550

Abstract - This paper presents two miniature Impedance Matching Wilkinson Power Divider circuits in 0.35µm SiGe BiCMOS technology for on-chip power combining techniques for WLAN applications. The Impedance Matching Wilkinson Power Divider circuits are used as splitter/combiner for a 5.2 GHz fully integrated class-A mode combined power amplifier. The splitter and combiner are designed to match the input and output impedances of the amplifier, respectively, so that no additional impedance matching is needed. Two fabricated impedance matching Wilkinson power divider circuits (splitter and combiner) have insertion losses better than 1.4dB, return losses less than -13dB and port-to-port isolation > 12 dB at 5.2GHz.

Key words: On-chip power divider, impedance matching, power amplifier

1. Introduction

Wilkinson power divider is one of the most widely used passive devices in high frequency. A quarter-wavelength transformer is easily realisable in microstrip form using distributed transmission line structures for microwave frequencies. However, for WLAN frequencies below 10GHz, the length of the transmission line structures become too long to be placed in a reasonably small-sized chip. The designs can be miniaturized by using lumped element equivalent circuits [1], [2]. The lumped element Wilkinson dividers can be realized in standard CMOS technology and 1.4dB insertion loss is already reported at 24 GHz [3]. Using Wilkinson power dividers as splitter and combiner is a well known power combining technique in RF industry. However, this technique is usually used for transmission line distributed elements. In [4], this technique is applied by using on-chip transmission line Wilkinson power combiners. Typically, Wilkinson power dividers are designed for 50 ? and additional matching networks are used to match the amplifier's input and output impedances to 50 ? . The proposed technique in this paper is to design on-chip Wilkinson power dividers for the input and output impedances of the amplifiers so that no additional matching circuit is needed. This will reduce the chip area as well as the cost of the combined power amplifier.

In this paper, design methodology of impedance matching Wilkinson power divider circuits is presented with measurement results of two fabricated impedance matching Wilkinson power divider circuits. The organization of the paper, after introduction, will be as follows: Section 2, impedance matching Wilkinson power divider design will be explained, in Section 3, measurement results will be presented, and finally the paper will be concluded.

2. Impedance matching Wilkinson power divider design

Wilkinson power divider was invented in 1960's. In this early topology, quarter wave transmission lines and a resistor are used to match 3 ports in a lossless manner as shown in Fig. 1

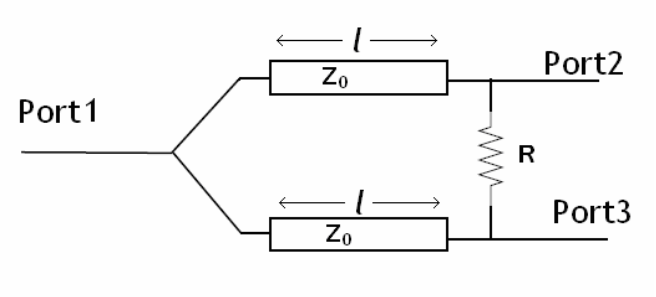


Fig. 1 A transmission line two-way Wilkinson power combiner

Assume that Port1 is terminated with impedance Z_1 and Port 2 and Port 3 are terminated with impedance Z_2 where Z_1 and Z_2 are purely resistive. For perfect match condition at all ports, the following equations should be satisfied.

$$\begin{aligned} l &= l/4 \\ Z_0 &= \sqrt{2Z_1Z_2} \\ R &= 2Z_2 \end{aligned} \qquad (1)$$

The lumped equivalent of the circuit in Fig. 1 is given in Fig. 2 where the transmission lines are replaced by a p-network of L-C elements.

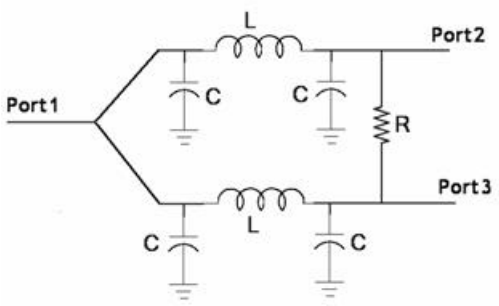


Fig. 2 A p-network lumped equivalent two-way Wilkinson power divider

The values of inductance L and capacitance C are given by

$$L = \frac{Z_0}{2pf}$$
$$C = \frac{1}{2pfZ_0} \qquad (2)$$

The p-network accomplishes the 90° phase shift and matching duty at the same time. However, the network suffers from high insertion loss when realized with low quality factor inductors which are generally less than 15 in silicon based technologies. On the other hand, the L-type matching network offers better insertion loss, but does not satisfy the 90° phase shift; so degraded isolation is expected by the L-network realization. For combined power amplifier application, insertion loss of the combiner is more important than the isolation performance; so impedance matching Wilkinson power divider circuits are realized by using L-type matching networks. The L-type matching network is designed for matching $2Z_1$ to Z_2 (Port 1 to Port 2 and Port 3) ; by this way very low return loss at all three ports of impedance matching Wilkinson power divider circuits are obtained. It should be noted that by using L-type matching networks, the restriction of choosing Z_1 and Z_2 purely resistive is cancelled out. The schematic view of proposed L-network lumped element impedance matching Wilkinson power divider circuit is given in Fig. 3.

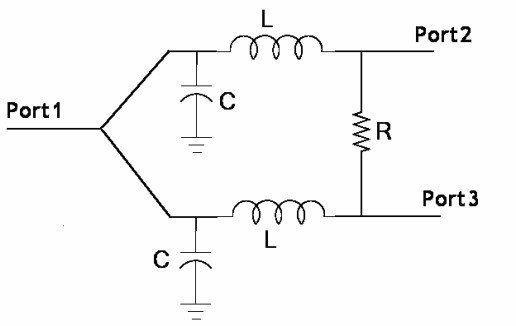


Fig. 3. L-network lumped element impedance matching Wilkinson power divider circuit

Two impedance matching Wilkinson power divider circuits are designed for the combined power amplifier application. One of these circuits is used as a splitter; the other circuit is used as combiner. Impedance matching Wilkinson power dividers are designed and optimized in SpectreRF Cadence programs. The splitter is designed such that Port1 is matched to 50 Ω and Port 2 and Port 3 are matched to input impedances of the power amplifier which is 9.5+ j3.5 Ω at 5.2 GHz. The design of the splitter results in values of L = 0.9 nH, 2C = 1.9 pF (including pads and trace capacitances) and R=18.6 Ω. DC block capacitances are used before Port 2 and Port 3 for dc isolation of the base terminals of the amplifiers. The combiner is designed such that Port 1 is matched to 50 Ω and Port 2 and Port 3 are matched to the optimum output load impedance of the amplifier, 28.5-j3 Ω. The design results in L=1.4 nH, 2C=0.9 pF and R=57 Ω. DC block capacitances are used before Port 1 for the combiner. The layout of splitter/combiner are designed such that two amplifiers with on-chip RF choke inductors can be placed in between these circuits. The layout of impedance matching Wilkinson power divider used as splitter/combiner is given in Fig. 4 a and b.

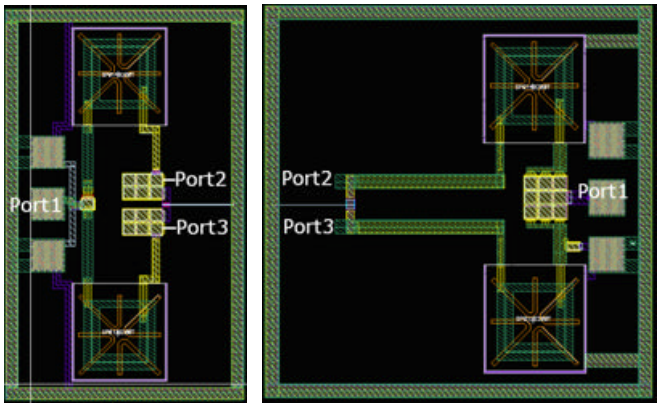


Fig. 4. Layout of impedance matching power divider used as Splitter (left) and Combiner (right)

The post layout simulation results for the splitter are shown in Fig. 5. Port 1 is terminated with 50 Ω and Port 2 and Port 3 are terminated with 9.5+j3.5 Ω for this simulation.

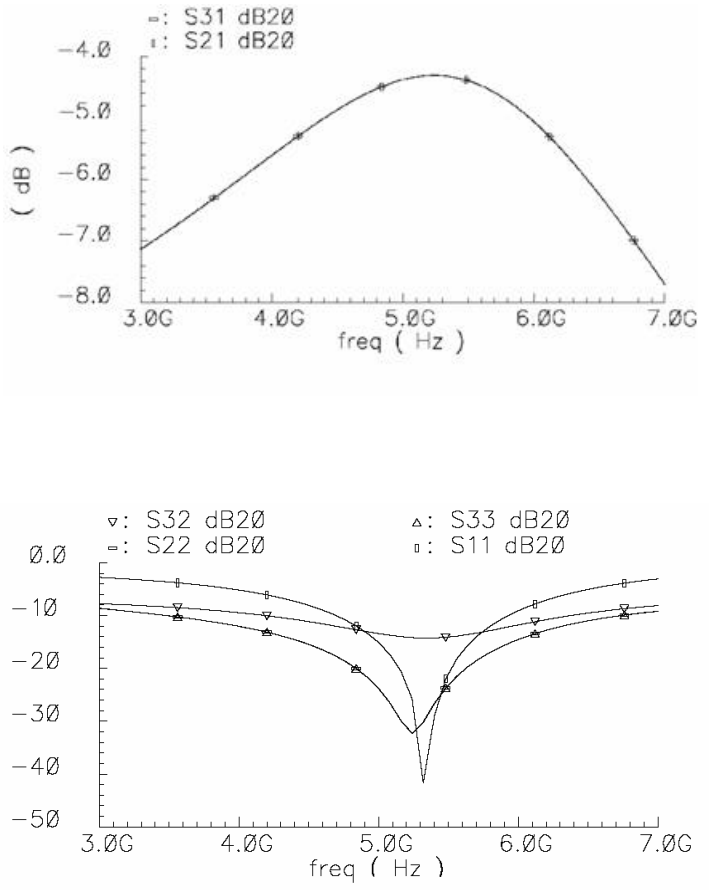


Fig. 5. S-Parameter Simulation Results for impedance matching Wilkinson power splitter

Insertion loss of 1.4 dB is achieved at 5.2 GHz with all ports matched to the desired impedances (S11, S22, S33< -20 dB) and good isolation (S23<-14 dB) is obtained as shown in Fig. 5. Low source impedances needed by the amplifier stage degrade the insertion loss performance of the splitter. The post layout simulation results for the combiner is given in Fig. 6. Port 1 is

terminated with 50 Ω and Port 2 and Port 3 are terminated with 28.5-j3 Ω; for the simulation of the output impedance of the amplifier obtained from load-pull analysis.

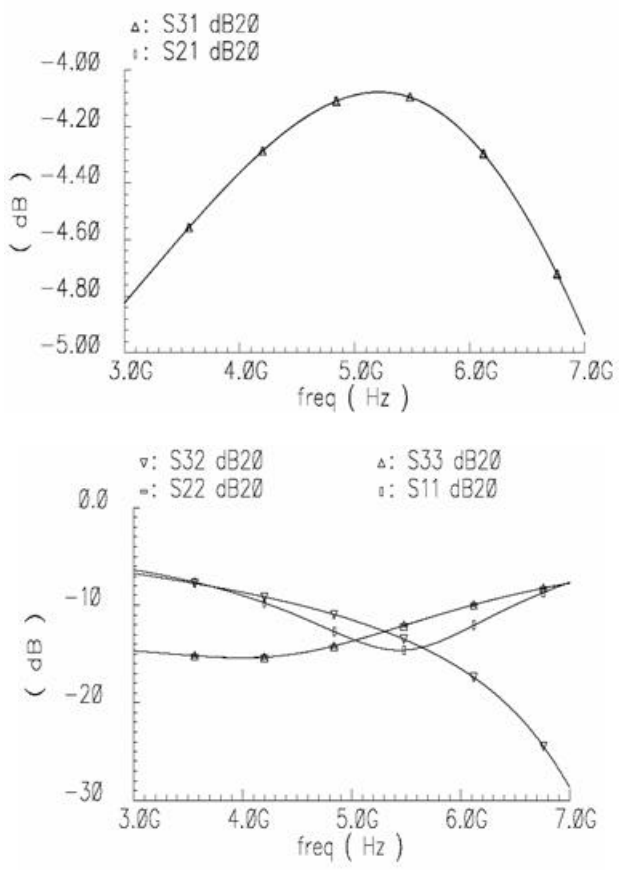


Fig. 6 S-Parameter Simulation Results of impedance matching Wilkinson power combiner

An insertion loss of 1.1 dB is achieved at 5.2 GHz with all ports are matched to the desired impedances (S11, S22, S33 <-13 dB) and reasonable isolation level (S23<-12 dB) is also obtained as shown in Fig. 6. The S21, S31 curves are very flat with respect to the splitter case, because the impedance matching ratio for the combiner is lower than the splitter.

For measurement purposes, Port 2 of the splitter/combiner is internally terminated with the port impedances of 9.5+j3.5 Ω (9.5 Ω resistor, 100 pH inductor) for the splitter and 28.5-j3 Ω (28.5

Ω resistor, 10pF capacitor) for the combiner. Additional pads are placed for Port 3 of the combiner/splitter. The microphotograph of the fabricated splitter and combiner are given in Fig. 7.a, b respectively.

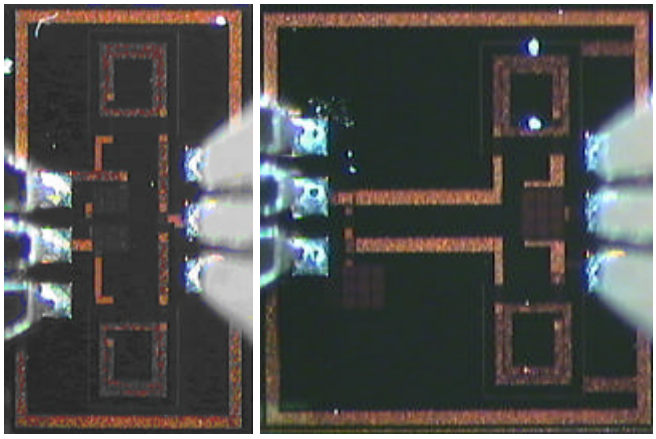


Fig. 7 Microphotograph. of Splitter (left) Combiner (right)

3. Experimental Results

The measurements are done using Agilent 8720ES Network Analyser with a 50 Ω measurement setup. The SOLT calibration is done with the calibration kit and port extension calibration is applied for the proper measurement of the input impedance. The reference plane is defined as the pads of the measured port. The effects of the pads are not de-embedded during the calibration. The S-parameter measurements of the splitter are given in Fig. 8 in comparison to post layout simulation results with 50 Ω measurement system.

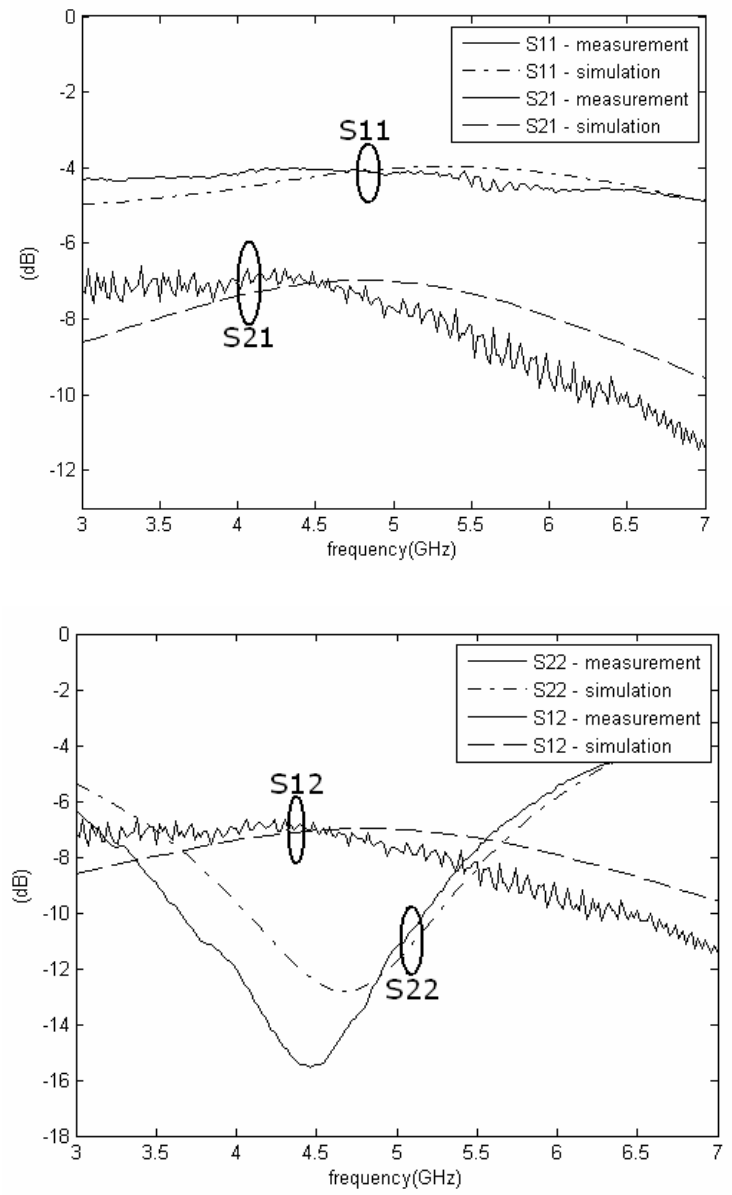


Fig. 8 Measured and Simulated S-Parameters of the Splitter with 50 Ω measurement setup

Around 5 GHz, measured results are in-line with the simulated results. The measurement results seemed to be shifted to the lower frequencies which could be caused by the extra capacitances of the pads added for measurement purposes. Note that S11 which is the return loss for Port 3 in Fig. 4.a is approximately -4.5 dB. This should not be considered as a bad return loss since this

circuit is meant to be used with a low impedance amplifier. The measured S21 and S12's are very close to the post-layout simulated curves which show that the circuit does not demonstrate additional loss other than simulations.

As Port1 and Port2 are terminated with optimum port impedances (50 Ω and 9.5+j3.5 Ω), the input impedance of Port 3 shows the impedance matching performance of the splitter. The measured and simulated input impedance from Port 3 of splitter is given in Fig. 9.

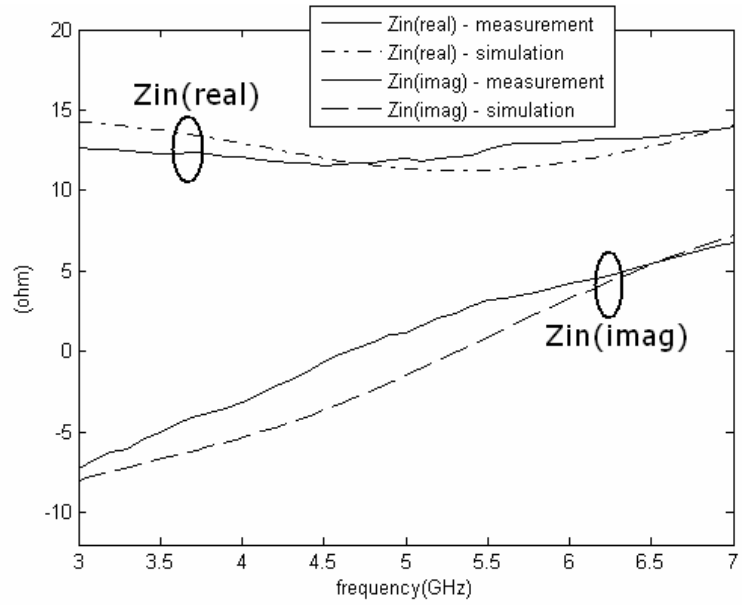
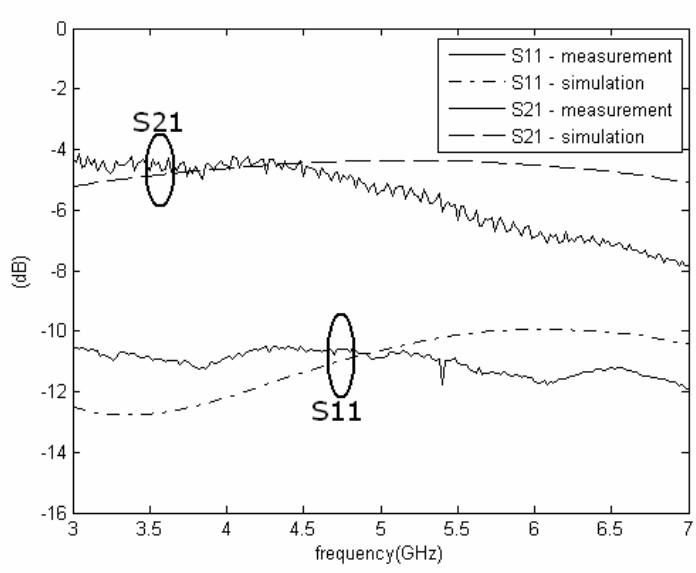


Fig. 9 Measured input impedance seen from Port 3 of splitter

The measured input impedance of Port 3 of the splitter is in close agreement with simulations. Note that this measurement result does not show the exact input impedance of the splitter given in Fig. 4.a because of the added pads for measurement purposes. The input impedance is measured as 12+j2 Ω at 5.2 GHz which is close to 9.5+j3.5 Ω.

The S-parameter measurement results of the combiner are given in Fig. 10 compared with post-layout simulation results with the 50 Ω measurement system. The measurement results seem to be slightly shifted to the lower frequencies; as in the splitter case. The measured S21 and S12's are very close to simulated curves up to 4.5 GHz. Hence, it can be assumed that the circuit does not demonstrate additional loss other than the components considered in simulations. The measured and simulated input impedance seen from Port 3 of combiner is given in Fig. 11.



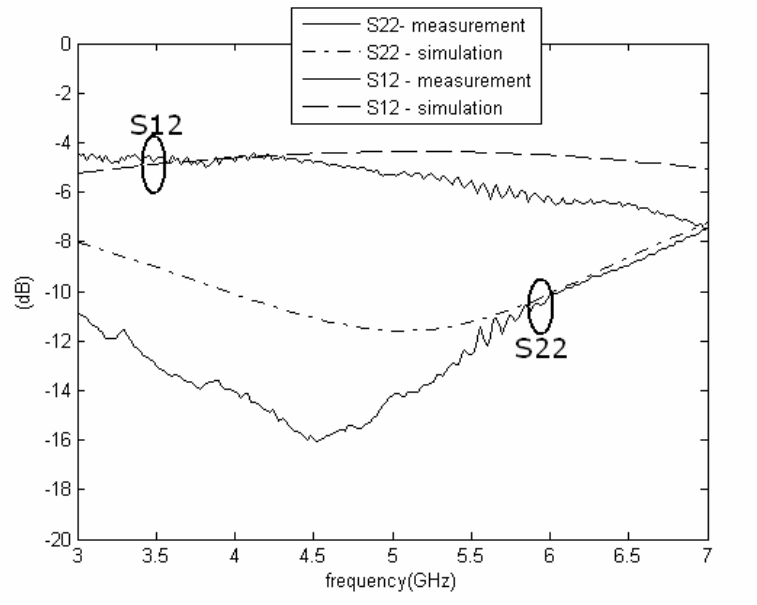


Fig. 10 Measured and Simulated S-Parameter Results of Combiner with 50 Ω measurement setup

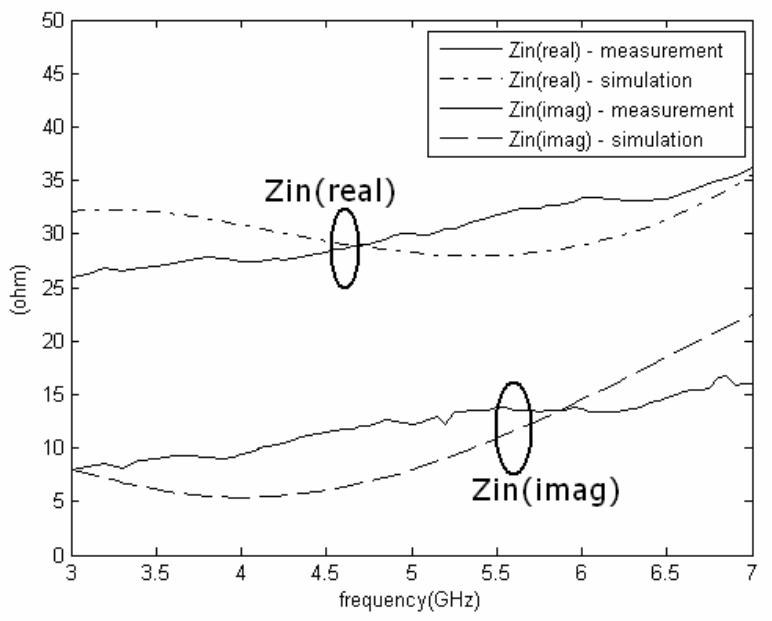


Fig. 11 Measured input impedance seen from Port 3 of combiner

The measured input impedance of Port3 of combiner is in-line with simulations. Although the pads are added for measurement purposes, the input impedance of combiner is measured as 31+j13 Ω at 5.2 GHz; which is close to 28.5-j3 Ω. The power gain/loss of a two port network excluding the reflection losses can be calculated by the following equation

$$G = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)} \qquad (3)$$

where S_{ij} are the scattering parameters of the two port network. The gain excluding the reflection losses is very meaningful as the circuit is measured with 50 Ω measurement setup. For ideal equal split of the RF signal (two-way Wilkinson power divider with ideal transmission lines), the insertion loss is 3 dB between the input and the output ports. This can be regarded as splitting loss. However, if the elements are lossy, the insertion loss will be higher. The measured loss of the splitter/combiner are calculated by (3) and plotted in Fig. 12 and Fig. 13 respectively in comparison with lossy (layout extracted) simulated results and lossless (with ideal components) simulated results.

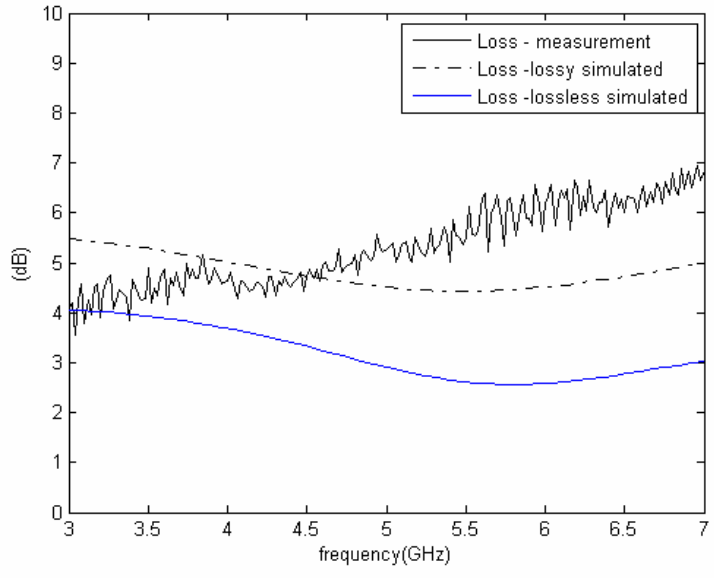


Fig. 12 Measured loss of Splitter

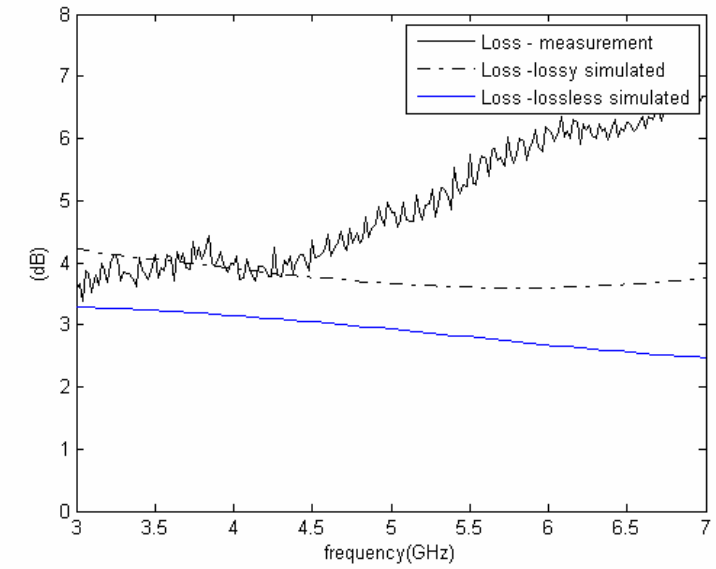


Fig. 13 Measured loss of Combiner

Measured results are in-line with the simulated results for both combiner and splitter up to 4.5 GHz. The measurement results seemed to be shifted to the lower frequencies which could be caused by the extra capacitances of the pads added for measurement purposes. Note that additional loss introduced by the splitter and combiner is around 2 dB and 1.5 dB respectively at 5 GHz with respect to the equal split two-way Wilkinson power divider. The total insertion loss for an isolated design of the splitter and combiner circuits and the matching circuits for the amplifier will be higher than the losses reported in the paper.

4. Conclusion

This paper presents L-network lumped element impedance matching Wilkinson power dividers in 0.35µm SiGe BiCMOS technology. The impedance matching Wilkinson power divider can be used in various applications where dividing and matching is needed. To validate the combined

power technique, a splitter and a combiner have been fabricated and measured. Measurement results show that the impedance values required for the combining technique can be obtained and the loss introduced by the substrate is within reasonable tolerances. Both of the implemented circuits are measured and results are in-line with the post-layout simulated results. Hence, it can be concluded that impedance matching Wilkinson power divider circuits can be used in power combining for RF power amplifiers.

5. Acknowledgment

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Author’s Biography

Ercan Kaymaksut (B.Sc. 2006) He received his B.Sc. degree from the Electronics and Communication Engineering Department of Istanbul Technical University (ITU) in 2006. Currently he is continuing his M.Sc. degree at the Electronics Engineering Program of Faculty of Engineering and Natural Sciences of Sabanci University, Istanbul, Turkey. His research interests are RF and microwave IC design.

Yasar Gurbuz (MS’93–PhD’97) received the BS degree in electrical engineering with high honors from Erciyes University, in 1990. He received the MS degree in 1993 and the PhD degree in 1997 in electrical engineering from Vanderbilt University in the USA. He worked as a senior research associate at Vanderbilt between 1997 and 1999. His responsibilities included directing and performing research projects, teaching courses and advising graduate students in the areas of solid-state devices and sensors. From 1999 to 2000 he worked at Aselsan Inc. In 2000, he joined Sabanci University, Faculty of Engineering and Natural Sciences, as an assistant professor and was promoted to associate professor in 2002. His research areas include analog and mixed-signal integrated circuits, solid-state devices and sensors, microelectromechanical systems (MEMS) and

wide-band gap semiconductor technologies. He has more than 20 peerly-reviewed journal papers and more than forty conference papers in his area of research. He is a member of IEEE and SPIE.

Ibrahim Tekin (MSc'92–PhD'97) He received his B.S and M.S degrees from Electrical and Electronics Engineering Department of Middle East Technical University (METU) in 1990 and 1992, respectively. From 1993 to 1997, he was with the Electrical Engineering Department of the Ohio State University (OSU) where he received his Ph.D degree in 1997. During 1990-1993 he was a research assistant at METU, and from 1993 to 1997 he worked as a Graduate Research Associate at the ElectroScience Laboratory, OSU. 1997 to 2000, he worked as a researcher in Wireless Technology Lab of Bell Laboratories, Lucent Technologies. He is now with the Telecommunications program at Sabanci University, Istanbul. His research interests are RF and microwave design, UWB antennas and circuits, numerical methods in electromagnetics. He is a member of the societies of IEEE Antennas and Propagation and IEEE Communications.