Realization of a ROIC for 72x4 PV-IR detectors

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ABSTRACT

Silicon Readout Integrated Circuits (ROIC) for HgCdTe Focal Plane Arrays of 1x4 and 72x4 photovoltaic detectors are represented. The analog circuit blocks are completely identical for both, while the digital control circuit is modified to take into account the larger array size. The manufacturing technology is 0.35μm, double poly-Si, three-metal CMOS process. ROIC structure includes four elements TDI functioning with a super sampling rate of 3, bidirectional scanning, dead pixel de-selection, automatic gain adjustment in response to pixel deselection besides programmable four gain setting (up to 2.58pC storage), and programmable integration time. ROIC has four outputs with a dynamic range of 2.8V (from 1.2V to 4V) for an output load of 10pF capacitive in parallel with 1MΩ resistance, and operates at a clock frequency of 5 MHz. The input referred noise is less than 1037 μV with 460 fF integration capacitor, corresponding to 2978 electrons.

Keywords: Readout Integrated Circuits (ROIC), time delay integration (TDI), current mirroring integration (CMI), focal plane array (FPA)

1. INTRODUCTION

Infrared imaging systems are used in a variety of applications from biomedical to astronomy and strategic imaging. Focal plane arrays are one of the key assemblies in these systems and readout circuits are responsible in converting detector outputs to ADC inputs.

Due to the fact that accumulation can be achieved easily, CCD technology has been used in many linear ROIC applications. But this choice has drawbacks of high input voltage and difficulty in designing complex systems with more programmable functions. Attributed to rapid development in CMOS technology, without degrading performance, linear ROIC's can now be designed with low cost and more complex functionality [1]. CMOS technology also offers reduced assembly cost and power due to single package possibility, compared to discrete approach CCD technology inherits. Single chip application also helps to improve ROIC performance [2].

A scanning sensor chip assembly (SCA) includes a row of detectors by which a scene is scanned and the resulting signal is multiplexed to generate the output. To create the entire scene, the array is scanned from one field of view to the other. Dwell time, which is equivalent to the time during which the detector is focused to a specific point, determines the sensitivity in this sensor system. High scene resolution, large field of view or short scan time, will tend to decrease the dwell time. A second row of elements, next to the first row produces a second image of the scene with a delay in time. If the first row is delayed by this certain time period, the two images can be added, resulting in a doubled signal level and a modest increase in noise of the two frames. By adding rows of time delay elements and performing time delay integration (TDI), the Signal-to-Noise Ratio (SNR) of a system can be improved by $\sqrt{N}$, assuming the system is detector limited, where N is the number of elements TDI is realized [3]. In order to increase resolution, super sampling can be used.

In this work, silicon ROIC's for photovoltaic HgCdTe FPAs with sizes of 1x4 and 72x4 are presented. The manufacturing technology is 0.35μm double poly-Si, three metal CMOS process. ROIC structure includes four elements TDI functioning with a super sampling rate of 3, bidirectional TDI scanning, dead pixel deselection, automatic gain adjustment in response to pixel deselection besides programmable four gain settings (up to 2.58pC storage), and programmable integration time. ROIC has four outputs with a dynamic range of 2.8V (from 1.2V to 4V) for an output

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load of 10pF capacitive in parallel with 1MΩ resistive, and operates at a clock frequency of 5 MHz. The input referred noise is less than 1037 μV with 460 fF of integration capacitor, corresponding to 2978 electrons referring to 68.6dB.

The ROIC system can be categorized in four sub-sections; input stages, TDI stages, offset cancellation/automatic gain adjustment stage and digital control circuits. Input stages consist of poly-Si integration capacitors and current mirroring integration unit cell structure, preferred because of its high injection efficiency, stable detector bias and high linearity properties. With four poly-Si integration capacitors switched according to gain settings, four different charge handling capacities can be realized. TDI stages consist of a single charge amplifier for 72 channels, with 26 TDI registers in every channel to integrate super sampling property to TDI algorithm. An offset cancellation stage is necessary in order to eliminate offset error, coming from TDI circuit and constant charge injection errors, generated in resetting integration and TDI capacitors. This is realized by subtracting the error generated by a channel with zero input current. Pixel deselection is achieved via enabling the function through serial interface, and programming the address of the pixel to be deselected. When the functionality is enabled with the presence of a dead pixel, the output of the specific channel is multiplied by 1.33. The last stage of ROIC is an op-amp buffer to drive a load of 10pF//1MΩ within 100 ns settling time. The digital control circuit consists of a control block to create a reset and TDI control signals, a 24 bit control register to program the ROIC, a 7x72 channel select decoder, a 7x72 address decoder for loading pixel selection data, a serial interface and a parallel interface circuit. Digital circuit is controlled by two clock signals, CLK and INT. CLK is the master clock up to 5MHz and INT is the integration period control signal.

2. READOUT ARCHITECTURE

The readout integrated circuit has four operating modes to be programmed with the following features:

- Integration period adjustment
- Variable gain adjustment
- TDI scanning bidirectionality
- Pixel deselection

The ROIC includes analog blocks of 72 channels; each consisting of four current sources for test purposes, four CMI unit cells, integration capacitors, registers for holding pixel functionality data and bi-directionality switches, TDI stage consisting of a charge amplifier, an offset reduction and automatic gain adjustment stage and output buffer. The ROIC includes digital control circuit to generate required signals to drive the analog circuits according to the data in the control registers. Programming of the control registers can be performed by either the parallel interface which permits only gain adjustments, scan direction and bypass mode for test purposes or by the serial interface that also permits the pixel deselection property. The readout architecture is represented as a block diagram in Figure 1 and the channel architecture is represented in Figure 2. Here in Figure 2, current sources are used for testing purposes instead of detectors. Input stage (or unit cell U.C.) is CMI. During the channel read operation in Figure 2, the G1.33 bus is set to high through the NAND gate if there is a dead pixel according to the specified channel register's data.

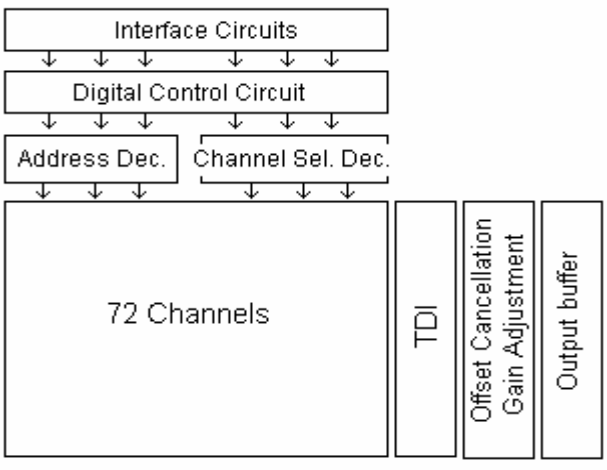

Figure 1: Block diagram of 72x4 ROIC

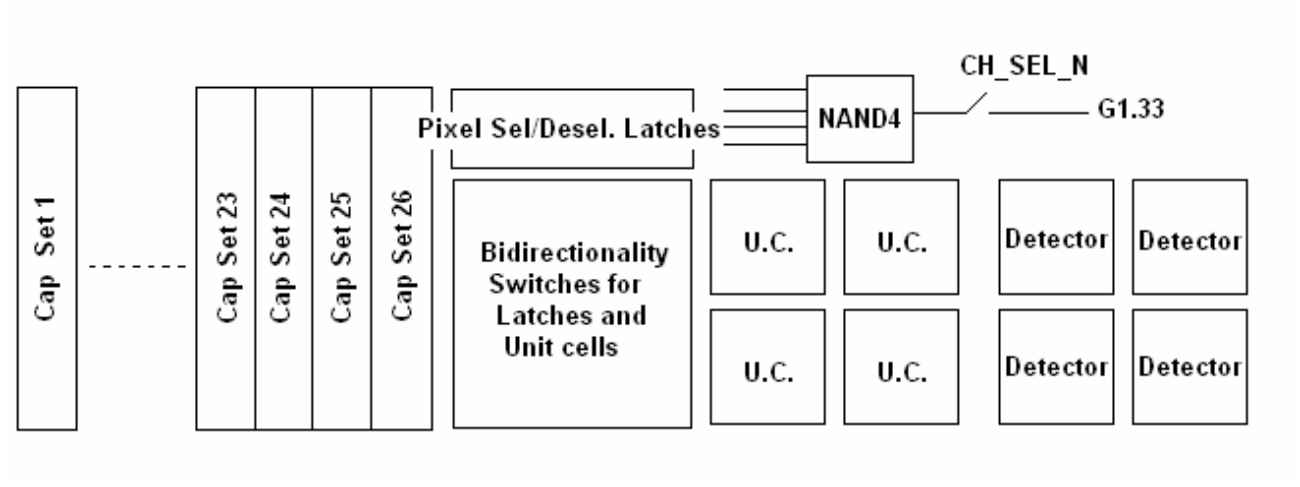

Figure 2: Block diagram of a channel

3. CIRCUIT IMPLEMENTATION

The sub-circuits of the ROIC can be categorized in four sub-sections; input stages, TDI stages, offset cancellation and automatic gain adjustment and digital control circuits. In the following, the details of these blocks are given.

3.1 Input stages

Input stage of the readout integrated circuit integrates the photocurrent over a capacitor. There are several different topologies of input stages such as direct injection (DI), buffered direct injection (BDI), capacitive feedback trans-impedance amplifier (CTIA), current mirror direct injection (CMDI) and current mirroring integration (CMI). Each one can be compared with others with respect to their performance on injection efficiency, noise, linearity and detector voltage stability. DI comes with the smallest area and lowest noise input stage. However its impedance is strongly dependent on photocurrent and it has poor bias stability over the FPA. BDI and CTIA use an in-pixel amplifier to obtain lower input impedance; however, it is difficult to obtain a high gain in a small pixel area [4, 5]. CMDI unit cell can reach to 100% efficiency, but it uses an in-pixel integration capacitor, limiting the dynamic range. CMI unit cell can reach to 100% efficiency with very low input impedance; its integration capacitor is not required to be in-pixel but it has a moderate noise performance compared to DI [5]. Hence, CMI unit cell is preferred in this application.

Despite the high area consumption, at the input stages poly-Si to poly-Si capacitors are preferred due to their high linearity. The TDI algorithm on four detectors with super sampling of three also makes it inevitable to use many numbers of capacitors which in return increases the chip-size. Parallel to the chip size, routing and parasitics associated to routing increases. Hence it is a better approach to carry the last stage of CMI unit cell close to the integration capacitor blocks. This results in carrying the mirroring voltage rather than the photocurrent itself. Schematic of CMI unit cell with the integration switch is presented in Figure 3.

The ROIC can operate with four different gains, with charge handling capacitances of 0.98pC, 1.29pC, 1.96pC and 2.58pC over a dynamic range of 2.8V. In order to obtain equivalent capacitance values, capacitors of 350fF, 110fF, 240fF and 220fF are switched with control signals G1, G0.65 and G0.50 in an additive manner to obtain total capacitance values of 350fF, 460fF, 700fF and 920fF.

3.2 TDI stages

In linear ROIC circuits, TDI is used as an effective signal process for increasing the integration time and signal-to-noise ratio (SNR) of line array [6]. SNR in infrared detectors is proportional to the square root of the integration time; TDI is used as a method to effectively increase the integration time without changing frame rate and resolution. By implementing TDI technique, diodes on the same row are used to detect the same image and the signal is integrated from

these photo-diodes [7]. Hence, TDI realized on N detectors, results in an improvement of $\sqrt{N}$ in SNR, effectively increasing integration time by N.

In order to realize the TDI property on four detectors with a super sampling rate of 3, each detector should have different number of memories. There is a delay of ten images between detector 1 (D1) and detector 4 (D4) because of scanning with super sampling rate of three. Thus, D1 should have 10 capacitors to store ten frames before its contribution added to D4. Also an additional capacitor for every detector is necessary since it is impossible to integrate detector's current into a storage capacitor and read at the same time. Detector 2 (D2) should have 3 less storage capacitor than D1 since there is a delay of 7 frames between D2 and D4. According to this principle, D1 has 11, D2 has 8, D3 has 5 and D4 has 2 capacitors. For bidirectional scanning, either D1, D2, D3, D4 should have 11, 8, 8, 11 capacitors respectively, or unit cells should be switched in between the capacitor sets of 11, 8, 5, 2 as in this case.

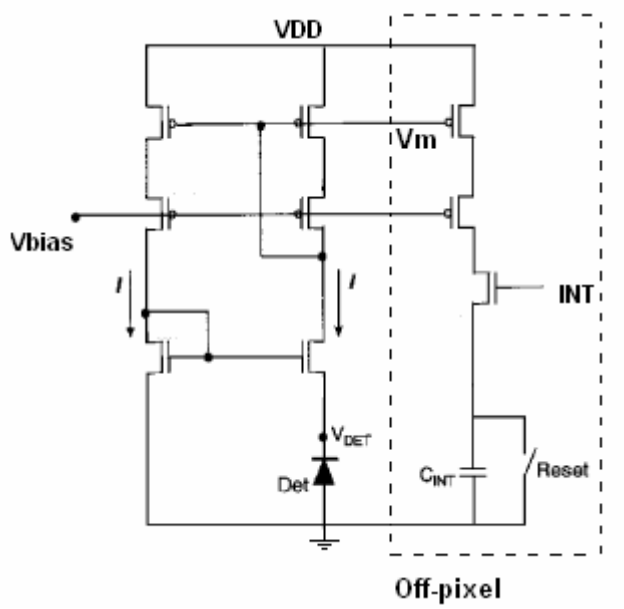

Figure 3: Schematic of CMI unit cell. The last stage is off-pixel, V_m and V_{bias} is carried through the ROIC to regenerate photocurrent near the integration capacitors

At each frame, an integration switch between a detector and one of the storage capacitors is on while all others are off, enabling integration of all detectors, simultaneously. Also there are switches (S1 and S2) which allow storage capacitors to discharge over integrator's capacitor. In order to produce TDI effect on correct capacitors, control logic operates according to frame counters counting up to 11, 8, 5 and 2, associated to each detector. Advantage of this architecture is that it requires only a single amplifier for summation which results more power efficient circuit in cost of a larger area.

Charge transfer to TDI register is realized with the use of an op-amp. Together with S1 and S2 switches, this circuit forms a switch capacitor integrator, as represented in Figure 4. C_p is the parasitic capacitance associated with the bottom plate of integration capacitors. S1 is on during integration, assigning the bottom plate voltage to ground level and off during charge transfer to TDI stage. S2 is off during integration and on during charge transfer to TDI stage, forcing zero voltage drop between the plates of capacitor, moving the stored charge to TDI register.

3.3 Offset cancellation and automatic gain adjustment

The TDI circuit, as discussed in the previous section, involves parasitics between the bottom-plates of integration capacitors to the substrate creating a constant offset added to the TDI output (Figure 4).

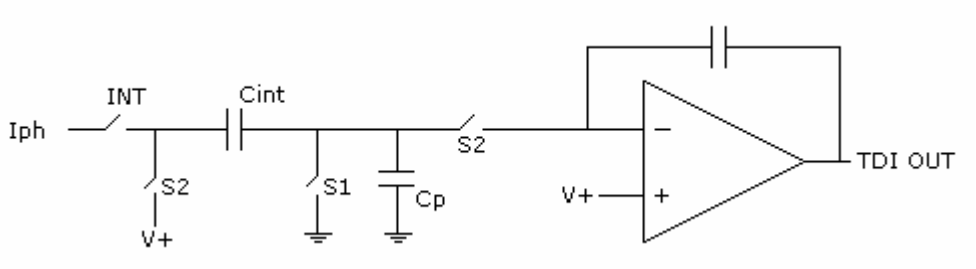

Figure 4: Schematic of TDI stage, parasitic capacitance C_p formed between bottom plate (poly1) and substrate is shown.

At an instant of time, a total charge of $Q_{int}=V_{int}*C_{int}$ is stored at the top plate of the integration capacitor. When S2 switches are closed, voltage on the integration capacitor is forced to be zero which results a discharge over C_{TDI}. At this instant, a charge movement of $Q_p=V_+ \ x \ C_p$ results an additional increase at the output. Following the end of integration, at bottom plate of integration capacitor, charges on the bottom plate of C_{int} and top plate of C_p plates are as;

$$Q_{\text{int},bottom} = -V_{\text{int}} \times C_{\text{int}} \ , \quad Q_{p,top} = 0 \tag{1}$$

When this charge is transferred to TDI stage, with S2 on and S1 is off, charges on the bottom plate of C_{int} and top plate of C_p plates are as;

$$Q_{\text{int},bottom} = 0 , \quad Q_{p,top} = V_+ \times C_p \tag{2}$$

Hence at the output, there is a total charge movement of;

$$Q_{out} = V_+ \times C_p + V_{\text{int}} \times C_{\text{int}} \tag{3}$$

Resulting an output voltage of;

$$V_{TDI} = V_+ + \frac{V_+ \times C_p}{C_{TDI}} + \frac{C_{\text{int}} \times V_{\text{int}}}{C_{TDI}} \tag{4}$$

It is important to eliminate the term associated with C_p, V_+ can be set according to output requirement which is in this case 1.2V. In order to cancel the offset associated with C_p term, a subtract circuit involving an op-amp and a zero input current channel to create the offset is realized. This methodology also removes the constant errors due charge injection and clock feed through effects, mainly formed by resetting of integration capacitors and TDI capacitors. This circuit, as presented in Figure 5, also realizes automatic gain adjustment in existence of a malfunctioning pixel in the channel by switching the resistors. In case of malfunctioning of one ore more of the four detectors of a channel, the readout multiplies the output voltage by 1.33, with the use of G1.33bar control signal. This signal is generated from the data of pixel functionality registers, programmed through the serial interface. Following the offset cancellation stage, the output stage consists of an op-amp buffer that is capable of driving a load of 10pF, 1MΩ to 2.8V dynamic range within 100ns.

3.4 Digital control circuits

The digital circuits consists of a control block to create reset, S1 and S2 signals to control integration capacitors and TDI registers, a 24 bit control register to program the ROIC, a 7x72 channel select decoder, a 7x72 address decoder for loading pixel selection data, a serial interface and a parallel interface circuit.

The ROIC uses two separate clocks, INT and CLK. Integration occurs as long as the INT signal is high and frame period is defined in between the two falling edges of INT. CLK is the master clock of all digital circuitry. For 72 channels to be carried out, a minimum of 76 cycles is required with the first four cycles being invalid. A frame can be 256 cycles at

maximum. In order to increase integration time, CLK frequency can be reduced, with a cycle count of 76 to 256 for a frame. The maximum applicable CLK frequency is 5MHz.

The readout can be programmed through both serial and parallel interface. In parallel mode, control registers only hold the data for gain settings, TDI scan direction and bypass mode. Parallel mode does not include the pixel deselection property.

In addition to gain setting, TDI direction and bypass mode features, pixel deselection functionality is available through serial interface. The control register includes 8 bit address register and 4 bit data register corresponding to the functionality of the detectors addressed. The readout is first programmed through the serial interface to set all functionality registers for 72 frames, programming one channel per frame. This data is kept as long as readout power is on.

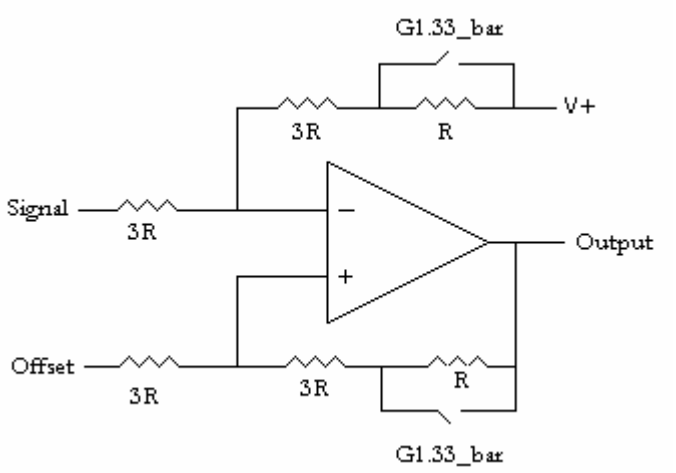

Figure 5: Schematic of TDI offset cancellation and automatic gain adjustment.

4. SIMULATION AND MEASUREMENT RESULTS

In this section simulation results of 72x4 ROIC is presented as well as measurement results of a previously manufactured single channel with similar analog functionalities. Transient noise analysis is also represented.

4.1 Measurement results

A single channel ROIC is fabricated using 0.35μm 3 metal 2 poly-Si CMOS process. In Figure 6 and Figure 7 two measurement results are represented. In these measurements, the chips are not bonded to FPA, but the input to the systems is the current to represent the detector photocurrent. In both measurements, the integration time is doubled and also the doubling at the output in response to this integration time difference is observed. For this ROIC, output signal is accumulated over 1.2V level, reaching up to 4.5V with a dynamic range of 2.8V. The ramp seen in both measurements is due to the offset, as discussed in section 3.3, that is being successfully removed at the beginning of the next frame, with a time delay for testing purposes.

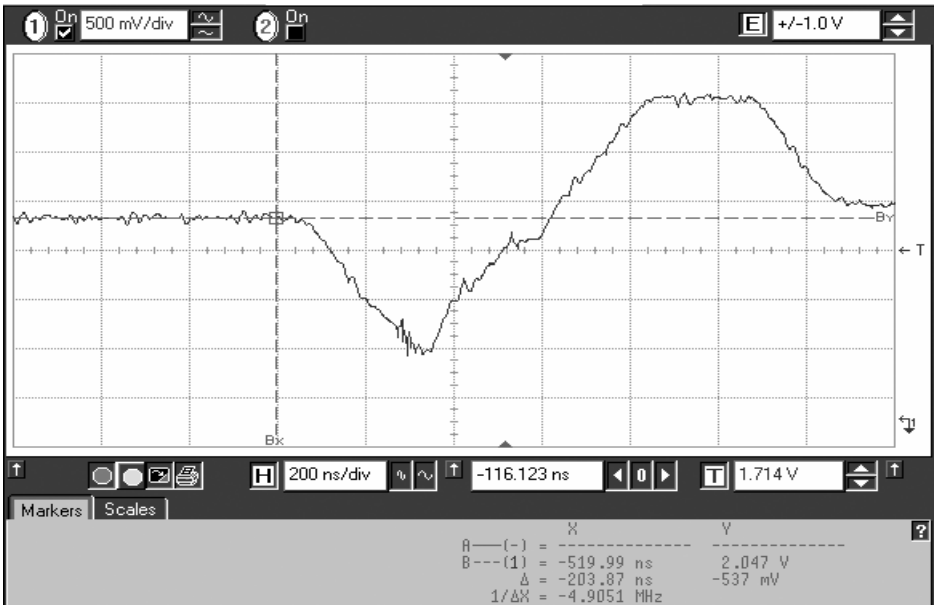

Figure 6: Measurement result with gain setting of 1.30 (350fF), integration time of 32us, with an input photocurrent of 4nA, results an output voltage of 2047 mV (347mV added to output)

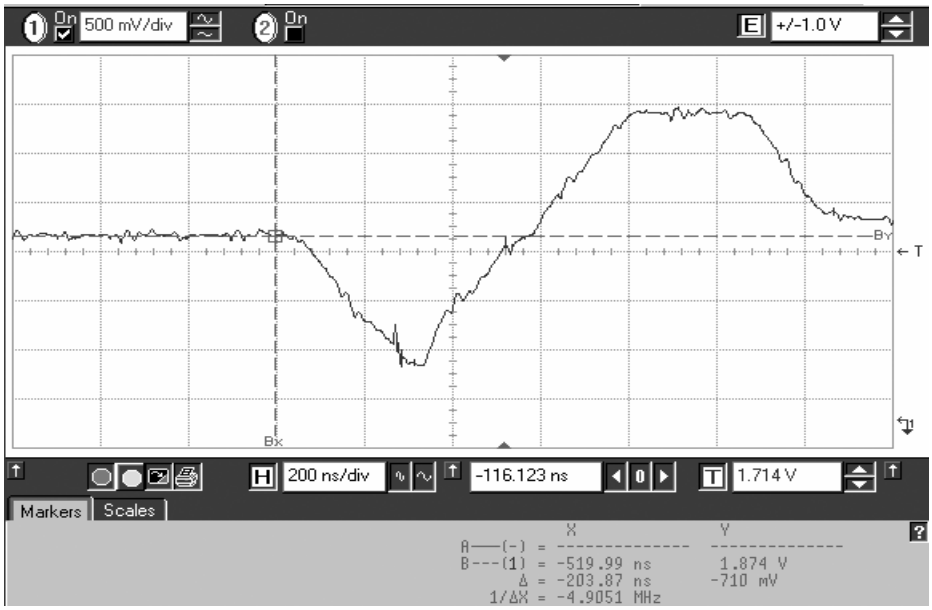

Figure 7: Measurement result with gain setting of 1.30 (350fF), integration time of 16us, with an input current of 4nA, results an output voltage of 1874 mV (174mV added to output)

4.2 Simulation results

In Figure 8, simulation results demonstrating the linearity performance of input stages are represented for input currents of 1nA, 10nA, 50nA and 100nA. Simulation results are presented with gain setting of 1 (460fF) and integration time of 10us for input photocurrents of 1nA, 10nA, 50nA and 100nA, resulting integrated voltages at the input 11.61mV, 116.09mV, 585.45mV and 1144.5mV, respectively, well representing the linearity of input stage. Figure 9 represents the voltage on integration capacitors in response to an input current of 10nA with an integration capacitor of 460fF as well as the corresponding output signal resulting from contributions of four detectors through the TDI stage. A gain setting of 1

(460fF) and integration time of 10us for a test current of 10nA (9.1nA at the input) results an output voltage of 1398 mV (198mV added to output). The voltage at the integration capacitor is 202mV. Figure 10 shows a similar simulation, showing the voltage on integration capacitors with an input current of 100nA, an integration capacitor of 460fF as well as the corresponding output signal resulting from contributions of four detectors through the TDI stage. The simulation, for gain setting of 1 (460fF), integration time of 10us, and a test current of 100nA (93.4nA at the input), results an output voltage of 3272mV (2032mV added to output). The voltage at the integration capacitor is 2071mV.

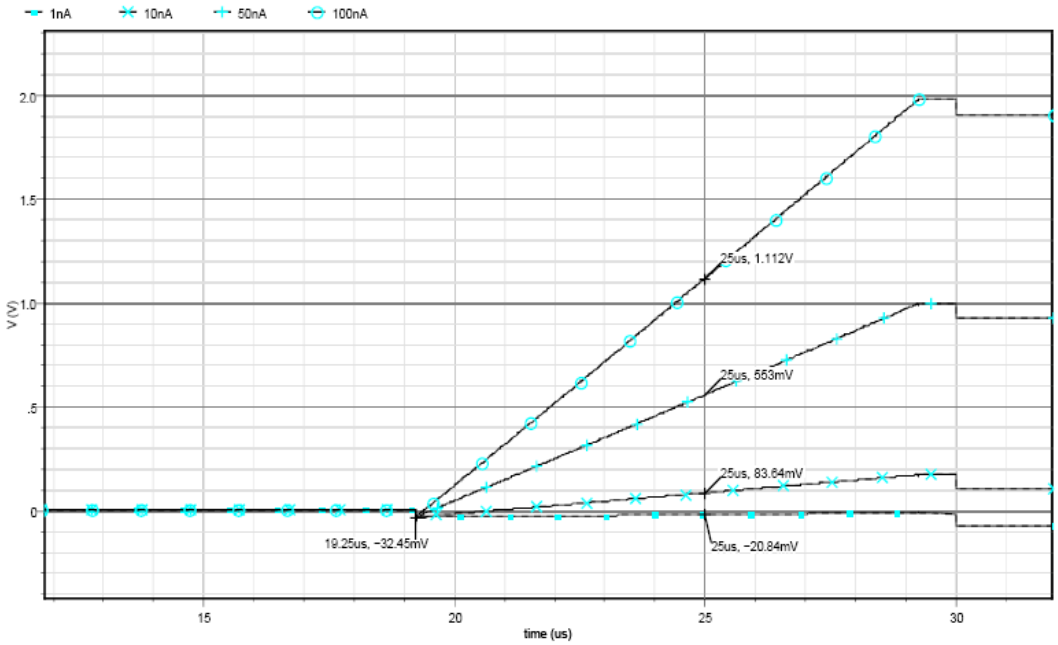

Figure 8: Simulation result with gain setting of 1 (460fF), integration time of 10us, with an input photocurrent of 1nA, 10nA, 50nA and 100nA.

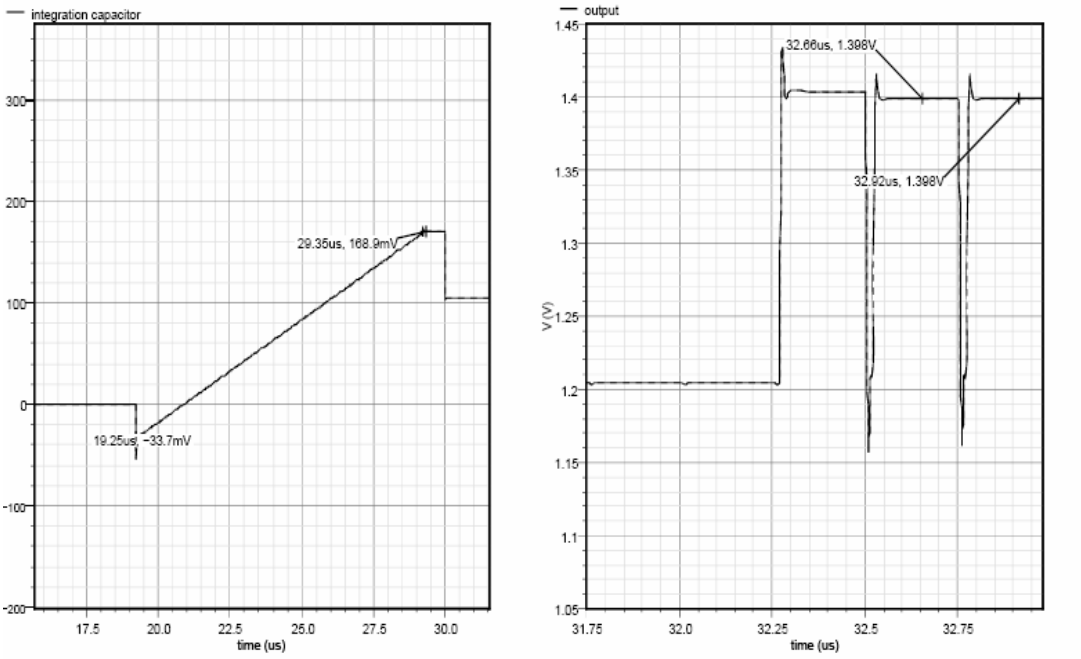

Figure 9: Simulation result with gain setting of 1 (460fF) and integration time of 10us for a test current of 10nA

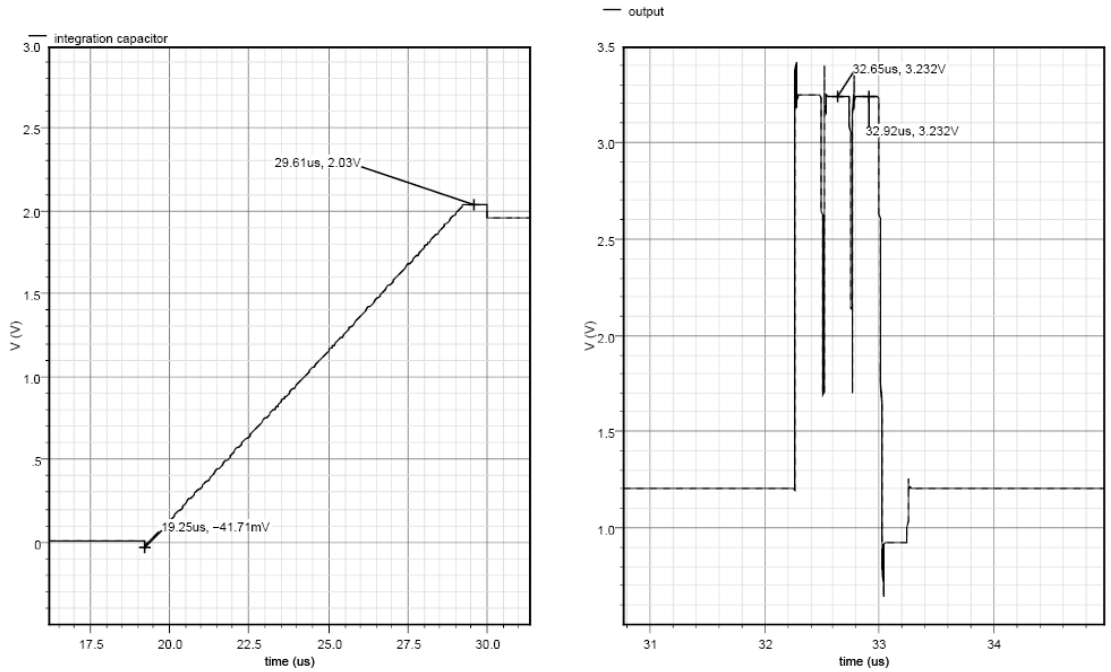

Figure 10: Simulation result for a gain setting of 1 (460fF), integration time of 10us, and test current of 100nA

4.3 Noise analysis

An iterative noise analyses is performed using Cadence Spectre®. Two simulations, one with ideal elements (no noise sources) and other with noise for all elements are performed, iteratively. The noise levels are obtained by subtracting the ideal simulation from the simulations with noise. It is known that for a continuous function *f(t)*, *rms* value is obtained by,

$$f_{rms} = \sqrt{\frac{1}{T_2 - T_1}\int_{T_1}^{T_2} [f(t)]^2 \, dt} \tag{5}$$

and *rms* values of N collection of data are obtained by

$$x_{rms} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} x_i^2} = \sqrt{\frac{x_1^2 + x_2^2 + \ldots + x_N^2}{N}} \tag{6}$$

From each simulation, *rms* values of noise are evaluated first and then the rms values of whole noise iterations are evaluated according to Eqns. 5 and 6. With this described methodology, it is observed that input referred noise, after the CMI stage, is 821 e^-, after the TDI stage is 1289 e^-, after the offset cancellation and automatic gain adjustment stage is 2969 e^-. Simulations show an input referred noise of 2978 e^- after the output buffer stage.

5. CONCLUSION

The design, simulation and test results of CMOS ROIC's for photovoltaic type HgCdTe FPA's of sizes 1x4 (designed, fabricated and tested) and 72x4 (designed) are presented in this study. The analog circuit blocks are completely identical for both, while the digital control circuit is modified to take into account the larger array size. The manufacturing technology is 0.35µm double poly-Si, three metal CMOS process. ROIC structure includes four elements TDI

functioning with a super sampling rate of 3, bidirectional scanning, dead pixel deselection, automatic gain adjustment in response to pixel deselection besides programmable four gain setting (up to 2.58pC storage), and programmable integration time. ROIC has four outputs with a dynamic range of 2.8V (from 1.2V to 4V) for an output load of 10pF in parallel with 1MΩ, and operates at a clock frequency of 5 MHz. The simulated input referred noise is less than 1037 μV with 460 fF integration capacitor corresponding to 2978 electrons which refers to 68.6dB readout dynamic range. The design specifications, functional and performance features, are also summarized in Table I and Table II.

Table I: ROIC design parameters

Summary of ROIC Design Parameters	
Array size	72 x 4 pixel^2
Detector type	HgCdTe FPA
Sensor interface	Current mirroring integration
Supply voltage	5V for analog, 3.3V for digital
Clock rate	up to 5 MHz
Pixel size	25μm x 28μm
Pixel pitch	43μm in *x*-direction, 56μm in *y*-direction
Technology	0.35μm double poly_Si, three metal CMOS

Table II: ROIC functional and performance features

Summary of ROIC Functional and Performance Features	
Pixel random deselection	with automatic gain adjustment
Reverse TDI scan	
Adjustable integration time	up to 63μs
Programmable 4 gain settings	0.98pC, 1.29pC, 1.96pC, 2.58pC
Integration charge storage capacity	$1.6x10^7$ electrons
TDI bit	4 with super sampling of 3
Serial/parallel interface	
Output dynamic range	2.8V
Readout Noise (simulated)	1037μV
# of output video channels	4
Power consumption	< 50mW
Chip area	3.5 mm x 6 mm

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