DESIGN AND REALIZATION OF A HIGH-SPEED 12-BIT PIPELINED ANALOG / DIGITAL CONVERTER IP BLOCK

by

ZEYNEP TOPRAK

Submitted to the Graduate School of Engineering and Natural Sciences
in partial fulfillment of
the requirements for the degree of
Master of Science

Sabancı University

Spring 2001

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APPROVED BY:

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DATE OF APPROVAL: 14 Eylül 2001

To my parents,

my sister

and

to my Doc.

ACKNOWLEDGEMENTS

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This thesis presents the design, verification, system integration and the physical realization of a monolithic high-speed analog-digital converter (ADC) with 12-bit accuracy. The architecture of the ADC has been realized as a pipelined structure consisting of four pipeline stages, each of which is capable of processing the incoming analog signal with 4-bit accuracy. A bit-overlapping technique has been employed for digital error correction between the pipeline stages so that the influence of possible errors that occur during analog signal processing can be minimized. The entire circuit architecture is built with a modular approach, consisting of identical blocks organized into an easily expandable pipeline chain.

All analog as well as digital sub-blocks of the ADC architecture presented in this work operate on a single clock signal (and its inverse), which significantly simplifies the design while ensuring a more robust performance. Other important features of this ADC include small area, single power supply, low power consumption, capability to operate at very high sampling clock rates, and the ability to handle a wide range of input signal amplitudes. The analog processing modules were designed using single-ended signals and the single-ended building blocks (as opposed to differential signals and building blocks) for simplicity. The ADC architecture was realized using a conventional 0.18 micron digital CMOS technology (Foundry: UMC), which ensures a lower overall cost and better portability for the design.

The ADC architecture presented in this work is capable of operating at sampling frequencies of up to 200 MHz, and still can achieve the nominal bit-resolution that was

intended for 12-bit accuracy. The entire circuit is designed with single 1.8 V power supply. The maximum range of the input signal amplitude that the ADC can handle is 1.6 Vpp, with 1.8 V supply voltage. The input signal range as well as the operating points of critical components can be adjusted externally using dedicated control pins. The overall power consumption is estimated as 67.5 mW at 200 MHz sampling rate. Each 4-bit pipeline stage consists of a 4-bit flash A/D converter, a fully capacitive multiplying DAC (MDAC) and the corresponding digital encoding circuitry. The overall silicon area of the ADC is approximately 0.25 mm^2.

The ADC architecture presented in this thesis is intended as a state-of-the-art data converter for very high-speed applications such as digital video transmission or high bandwidth wireless communication needs. It can be used either as a stand-alone single-chip unit, or as an embedded IP block that can be integrated with other modules on chip.

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Bu tez, 12-bit doğrulukla çalışan bir monolitik yüksek hızlı analog-sayısal dönüştürücünün (ADC) tasarımı, sınanması, sistem düzeyinde tümleştirilmesi ve fiziksel tasarımının gerçekleştirilmesi aşamalarından oluşmuştur. ADC'nin mimarisi, herbiri gelen analog işareti 4-bit doğrulukla işleyebilen dört kademeden oluşan bir veri yolu yapısı olarak gerçekleştirilmiştir. Analog işaret işlenmesi sırasında meydana gelebilecek olası hataların etkisini en aza indirebilmek amacı ile veri yolu kademeleri arasındaki sayısal hataları düzeltmek için bir bit-çakıştırma tekniği kullanılmıştır. Devrenin tüm mimarisi, benzer blokların kolayca genişletilebilir bir veriyolu zinciri biçiminde dizilmesinden oluşan, modüler bir yaklaşımla şekillendirilmiştir.

Bu çalışma kapsamında ele alınan ADC mimarisinin tüm analog ve sayısal alt-blokları, tasarımı belirgin biçimde basitleştirmek ve aynı zamanda blokların daha güvenli olarak çalışmalarını sağlamak amacıyla, tek saat işareti (ve tersi) ile işlem yapabilecek şekilde tasarlanmıştır. Bu ADC'nün diğer önemli özellikleri arasında küçük kırmık alanı, tek güç kaynağı kullanılması, düşük güç gereksinimi, çok yüksek örnekleme hızlarında ve geniş bir giriş işareti genliği alanı içinde çalışabilme kabiliyeti sayılabilir. Çalışma kolaylığı nedeniyle, analog işlem modülleri, diferansiyel işaret ve yapısal bloklar yerine, tek uçlu işaretler ve tek sonlu yapısal bloklar kullanılarak tasarlanmıştır. Bu tezde sunulan ADC mimarisi, daha düşük toplam maliyet ve tasarıma daha iyi taşınabilirlik sağlamak amacıyla, endüstride yaygın olarak kullanılan 0.18 mikron sayısal CMOS teknolojisi (Foundry: UMC) kullanılarak gerçekleştirilmiştir.

Tasarlanan dönüştürücü devresi, 200 MHz örnekleme frekansına kadar doğru çalışabilme ve bu yüksek örnekleme hızında hedeflenmiş olan 12-bit çözünürlüğü elde edebilme özelliklerine sahiptir. Devrenin tamamı bir tek 1.8 V güç kaynağı ile beslenebilecek şekilde tasarlanmıştır. ADC'nin 1.8 V besleme gerilimi ile işleyebileceği en yüksek giriş işareti genliği (tepeden tepeye) 1.6 Vpp'dir. Giriş işareti genliği ve bununla birlikte kritik modüllerin çalışma noktaları, denetleme girişleri yardımıyla dışarıdan ayarlanabilir. 200 MHz örnekleme hızında, toplam güç tüketimi 67.5 mW olarak öngörülmektedir. Her 4-bitlik veri yolu kademesi, bir adet 4-bit flash A/D dönüştürücü, bir adet tamamen kapasitif çarpıcı DAC (MDAC) ve bunlarla birlikte çalışacak sayısal çözümleyici devrelerden oluşmaktadır. ADC'nin toplam silikon alanı yaklaşık 0.25 mm^2'dir.

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1 . INTRODUCTION

Our physical world produces a vast variety of analog signals, while most of the signal processing systems operate exclusively on digital signals. Consequently, it is necessary to be able to convert back and forth between the two types of signals. Therefore analog-to-digital and digital-to-analog converters are an important part of a signal processing system. From this point of view a state of art, four stage pipelined analog-to-digital converter using flash algorithm is proposed and discussed in detail in this thesis. The thesis is organized as follows: Chapter 1 includes a brief summary of A/D converter topologies. In Chapter 2 performance measures of A/D converters, such as INL, DNL etc. are examined. Chapter 3 introduces the concept of the proposed pipelined ADC architecture in detail. Chapter 4 and Chapter 5 handles the building blocks of proposed ADC such as comparators and sample-hold amplifiers respectively; in Chapter 6 assembling a 4-bit pipeline stage is introduced and Chapter 7 reviews the digital building blocks. Then Chapter 8 introduces the four stage pipelined ADC. Finally conclusions are presented in Chapter 9.

The objective of an A/D (analog-to-digital) converter is to determine the digital output corresponding to an analog input signal. In other words, an Analog-to-Digital converter is a device that converts a continuous range of input amplitude levels into a discrete finite set of digital outputs. In this chapter, the fundamental aspects of Analog-to-Digital converters with different architectures are presented, in order to establish the basic classification of ADCs.

Analog-to-Digital converter architectures can be classified on the basis of the sequence of operations used to digitally encode an analog input. At the top of this classification hierarchy, converters are partitioned into two groups, Nyquist-Rate ADCs and Oversampling ADCs, based on the rate at which the input signals sampled relative to its bandwidth.

- Nyquist-rate Converters: We loosely define Nyquist-Rate data converters as those converters that generate a series of output values in which each value has one-to-one correspondence with a single input value. However, it should be noted that Nyquist-Rate converters are seldom used at the Nyquist-Rate due to the difficulty in realizing practical anti-aliasing real reconstruction filters. In most cases, Nyquist-Rate converters operate at 1,5 to 10 times the Nyquist-Rate (i.e., 3 to 20 times the input signal's bandwidth. As a summary, Nyquist-Rate converters:
    * Can digitize input signals with bandwidths approaching half the sampling rate
    * Operate at or near the minimum sampling rate for a given input bandwidth
    * Ensure that each sample is quantized to the full precision of the converter, i.e., the quantization error is minimized for each individual sample [2].

- Oversampling Converters: Oversampling converters are those converters that operate much faster than the input signal's Nyquist-Rate (typically 20 to 512 times faster) and increase the output's signal-to-noise (SNR) by filtering output quantization noise that is not in the signal's bandwidth. In A/D converters, this filtering is performed digitally. Most often, oversampling converters use noise shaping to place much of the quantization noise outside the input signal's bandwidth. Thus, the main characteristics of oversampling converters are as follows:
    * Sample signals at rates well above the signal bandwidth.
    * Digital encoding obtained by digitally "averaging" sequence of samples encoded at the oversampling rate.

* Coarse amplitude quantization is combined with feedback and digital filtering to obtain a precise estimate of the input.
* Minimize quantization error power in sequence of samples rather than in a single sample; therefore must use metrics like SNR and mean squared baseband error, not INL or DNL [2].

The block diagram representation of an A/D Converter is shown in Figure 1.1, where B_{out} is the digital output word while V_{in} and V_{ref} are the analog input and reference signals respectively. Also, we define V_{LSB} to be the signal variation corresponding to a single LSB change.

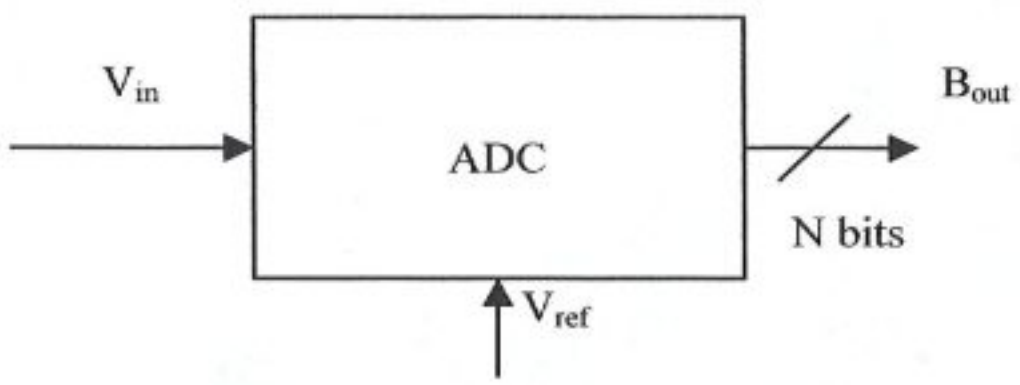


Figure 1.1 Black box representation of an A/D converter.

For an A/D converter, the following equation relates these signals as,

$$V_{ref}\left(b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}\right) = V_{in} \mp V_x$$

where

$$-\tfrac{1}{2}V_{LSB} \le V_x < \tfrac{1}{2}V_{LSB} \qquad (1.1)$$

and V_x represents the quantization error, which will be explained in the next chapter. Note that there is now a range of valid input values that produce the same digital output word. It should be noted that the relation shown above holds only if the input signal remains within 1LSB of the two last transition voltages.

After examining the ideal analog-to-digital converter, this section follows with the brief explanations of the types of A/D Converters, such as the serial, successive

approximation, parallel (flash) and high performance A/D converters, which are under the Nyquist-rate converter branch.

1.1 Serial A/D Converters

This type of converters performs serial sequential operations in time domain until the conversion is complete. Two architectures can be examined, called the single-slope and dual-slope. These are level-at-a-time integrating converters where input is converted to a timing pulse as "pulsewidth modulating" converters and the width of this pulse is measured by counting clock cycles (also referred to as "pulse-width modulating" converters). Offering high resolution and accuracy but slow conversion speed (2^N clock/sample), these types of converters are used in applications of high resolution, low frequency.

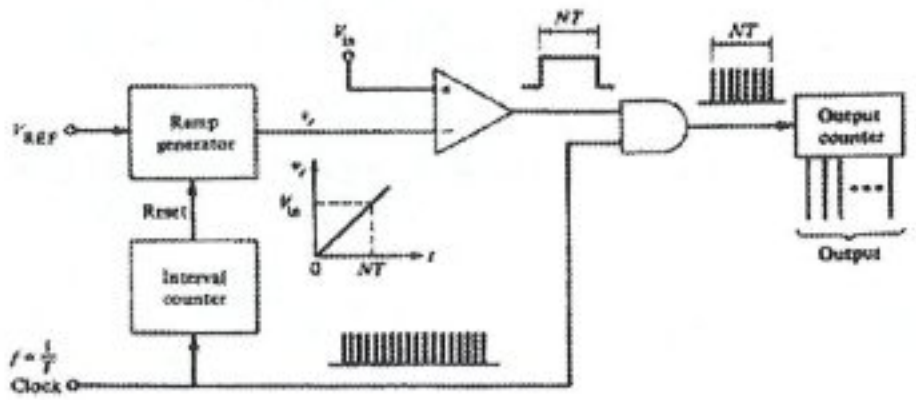


Figure 1.2 Block diagram of a single slope serial A/D converter [3].

Figure 1.2 shows the block diagram of a single-slope serial A/D converter. This type of converter consists of a ramp generator, an internal counter, a comparator, an AND gate, and a counter that generates the output digital code. At the beginning of a conversion cycle the analog input is sampled, held and applied to the positive terminal of the comparator. The counters are reset, and a clock is applied to both the time interval counter and the AND gate. On the first clock pulse, the ramp generator begins to integrate the reference voltage, V_{REF}. If V_{IN} is greater than the initial output of the ramp

generator, which is applied to the negative terminal of the comparator, begins to rise. Because V_{IN} is greater than the output of the ramp generator, the output of the comparator is high and each clock pulse applied to the AND gate causes the counter at the output to count. Finally, when the output of the ramp generator is equal to V_{IN}, the output of the comparator goes low and the output counter is now inhibited. The binary number representing the state of the output counter can now be converted to the desired digital format. The serial A/D converter has the advantage of simplicity of operation. Disadvantages of the single-slope A/D converter are that it is subject to error in the ramp generator and it is unipolar. Another disadvantage of this type of A/D converter is that a long conversion time (2^N clock cycles in the worst case) is required if the input voltage is near the value of V_{REF}. A block diagram of a Dual-Slope A/D Converter is shown in Figure 1.3.

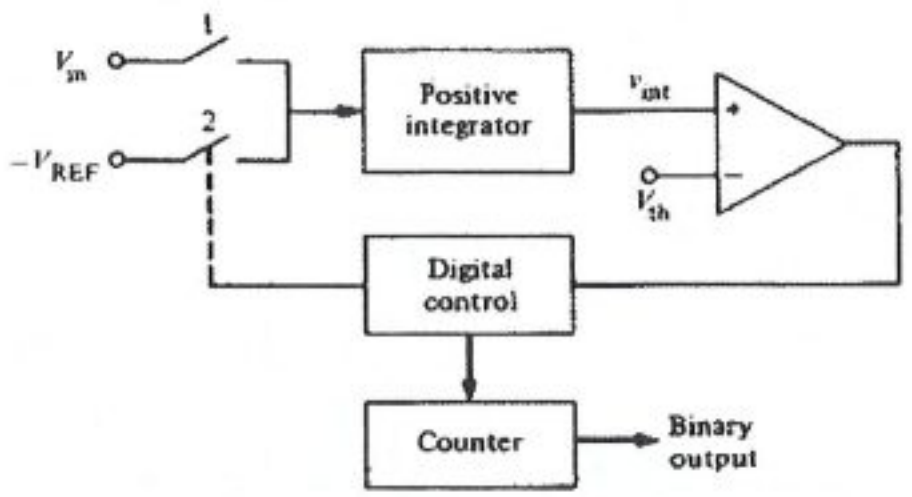


Figure 1.3 Block diagram of a dual-slope A/D converter [3].

The basic advantage of this circuit architecture is the elimination of the dependence of the conversion process on the linearity and accuracy of the ramp generator. Initially, V_{int} is zero, and the input is sampled and held. In this scheme, it is necessary for V_{in} to be positive. The conversion process begins by resetting the positive integrator until the output of the integrator is equal to the threshold, V_{th}, of the comparator. Next, S1 is closed, and V_{IN} is integrated for N_{ref} number of clock cycles. Figure 1.4 illustrates the conversion process. It is seen that the slope of the voltage at V_{int} is proportional to the amplitude of V_{IN}. The voltage, $V_{int}(t)$, during this time is given as

$$V_{\text{int}}(t) = K \int_0^{N_{ref}T} V_{IN}\,dt + V_{\text{int}}(0) = KN_{ref}TV_{IN} + V_{th} \tag{1.2}$$

where T is the clock period. At the end of the N_{ref} counts, the carry output of the counter is applied to switch S2 and causes $-V_{ref}$ to be applied to the integrator. Now the integrator integrates negatively with the constant slope because V_{ref} is constant. When $V_{int}(t)$ becomes less than the value of V_{th}, the counter is stopped, and its binary count can be converted into digital word. This is demonstrated by considering $V_{int}(t)$ during the time designated as t_2 in Figure 1.4. This voltage is given as

$$V_{\text{int}}(t) = V_{\text{int}}(0) + K \int_0^{N_{out}T} (-V_{ref})\,dt \tag{1.3}$$

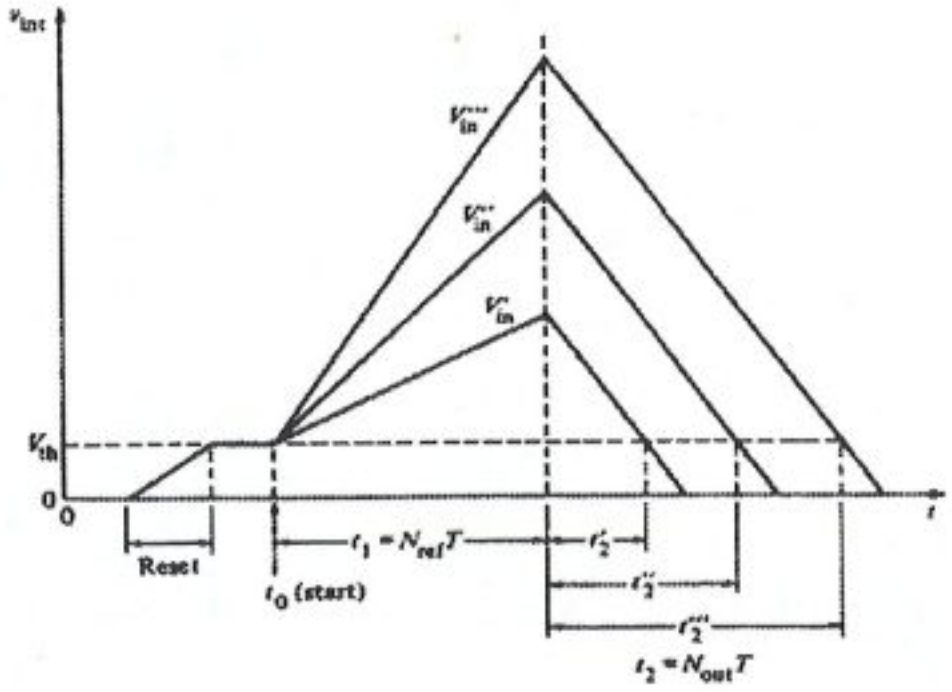


Figure 1.4 Waveforms of the dual-slope A/D converter in Figure 1.3 [3].

However, when $t = N_{out}T$, then Eq. (1.3) becomes

$$V_{\text{int}}(N_{out}T) = (KN_{ref}TV_{IN} + V_{th}) - KV_{ref}N_{out}T \tag{1.4}$$

because $V_{int}(N_{out}T) = V_{th}$, then Eq.(1.4) can be solved for N_{out}, giving

$$N_{out} = N_{ref}\left(V_{IN}/V_{ref}\right) \tag{1.5}$$

It is seen that N_{out} will be some fraction of N_{ref}, where that fraction corresponds to the ratio of V_{IN} to V_{ref}.

The output of the serial dual-slope A/D converter (N_{out}) is not a function of the threshold of the comparator, the slope of the integrator, or the clock rate. Therefore, it is a very accurate method of conversion. The only disadvantage is that it takes a worst-case time of $2(2^N)$ T for a conversion, where N is the number of the bits of the A/D converter; a T is the clock period. [3]

1.2 Successive Approximation A/D Converters

This class of A/D converters converts an analog input into an N-bit digital output in N clock cycles. Also called "bit-at-a-time" converters, their operation principle is based on a binary search, beginning with the most significant bit (MSB). This type of converters includes comparators, Digital-to-Analog converter, and Successive Approximation Register (SAR). Starting with the MSB, the fraction of V_{ref} corresponding to each bit is successively added to the fraction corresponding to already determined bits and the sum is compared to the input sample. There exists a trade-off between accuracy and speed (N comparisons per conversion). Different DAC topologies can be implemented in this type of A/D converters.

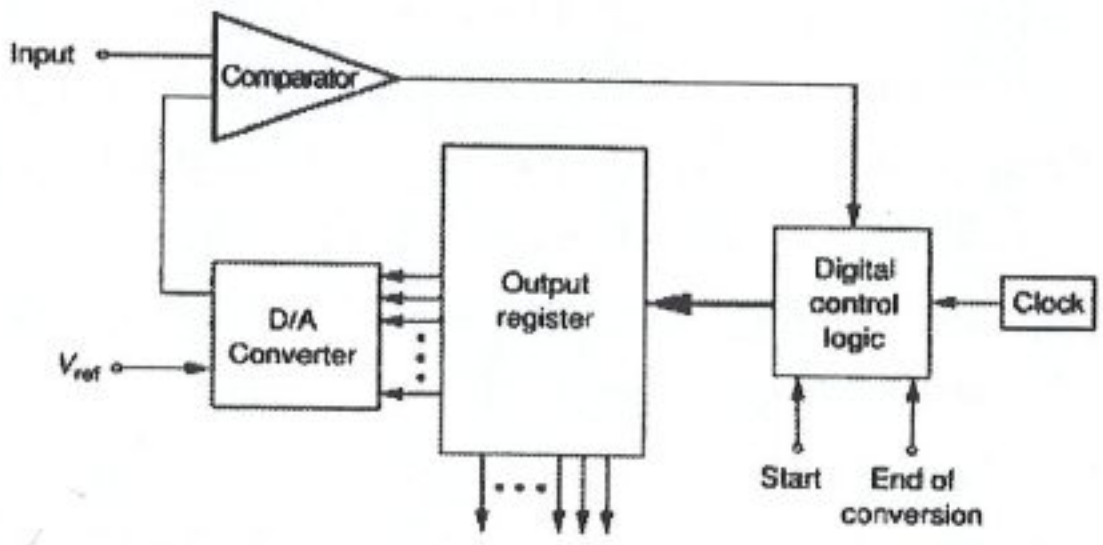


Figure 1.5 Example of a Successive Approximation A/D converter [17].

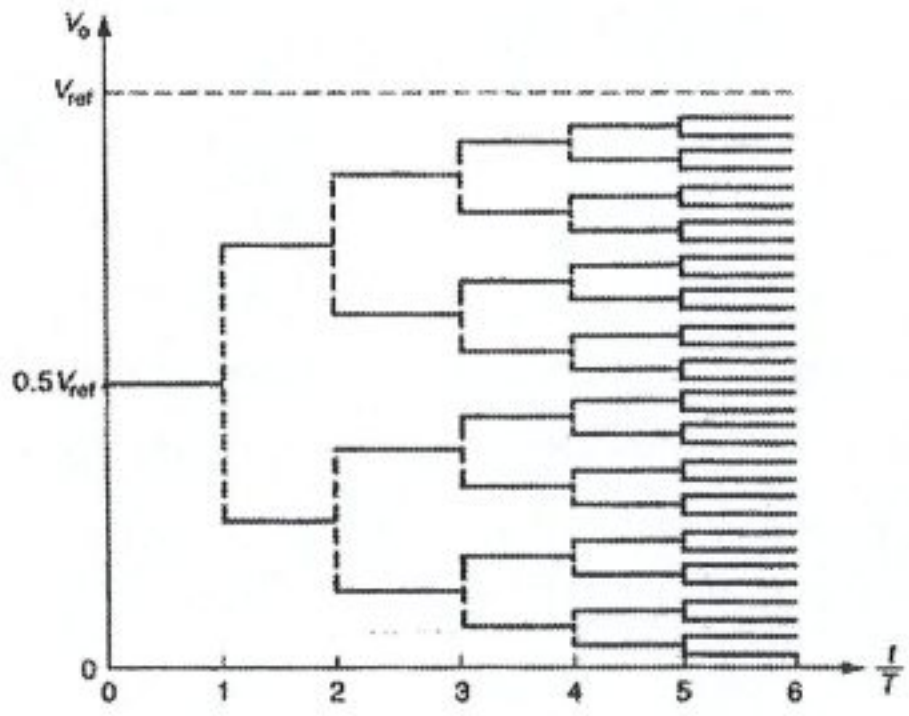


Figure 1.6 The successive approximation process [17].

The function of the digital control logic is to determine the value of each bit in a sequential manner based upon the output of the comparator. The conversion cycle begins by sampling the analog input signal to be converted. Next, the digital control circuit assumes that the MSB is "1" and all other bits are "0". This digital word is applied the DAC, which generates an analog signal of $0.5V_{ref}$, which is compared to the sampled analog input, V_{IN}. If the comparator output is high, then the digital control logic decides that the MSB is equal to "1". If the comparator output is low, the digital control logic decides the MSB is "0". This completes the first step in the approximation sequence. At this point, the value of MSB is known. The approximation process continues by applying the digital word to the DAC, with the MSB having its proven value, the next lower bit a "guess" of "1", and all other remaining bits having a value of "0". Again, the sampled input is compared to the output of the D/A converter with this digital word applied. If the output of the comparator is high, the second bit is proven to be "1". If the output of the comparator is low, the second bit is "0". The process continues in this manner until all bits of the digital word have been decided by the successive approximation process.

Figure 1.6 shows how the successive approximation sequence works in converting the analog output of the D/A converter to the sampled analog input. It is seen that the number of cycles required for the conversion to an N-bit word is N. It is also observed

that as N becomes large, the requirement of the comparator to distinguish between almost identical signals must increase.

A successive approximation A/D converter using an Algorithmic D/A converter is often called an Algorithmic A/D Converter.

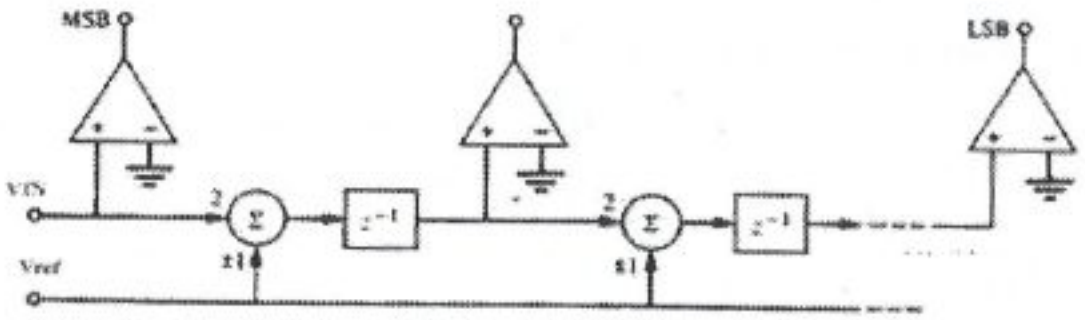


Figure 1.7 Pipeline implementation of the algorithmic A/D converter [3].

An algorithmic A/D converter patterned after the algorithmic D/A converter of the preceding stage is shown in Figure 1.7. This N-bit A/D converter consists of N stages and N comparators for determining the signs of the N outputs. Each stage takes its input, multiplies by 2, and adds or subtracts the reference voltage depending on the sign of the previous output. The comparator outputs form an N-bit digital representation of the analog input to the first stage. The algorithmic ADC of Figure 1.7 has the disadvantage that the time to convert a sample is N clock cycles, although one complete conversion can be obtained at each clock cycle. As it is obvious, an algorithmic A/D converter does not need any reference voltage generators, which are usually implemented with capacitor or resistor arrays. Thus, the algorithmic A/D converter is considered to be ratio-independent because the performance does not depend on the ratio accuracy of a capacitor or resistor array. The multiplication by 2 of the first stage must be accurate to within 1 LSB, which is a distinct disadvantage of this configuration of the algorithmic A/D converters. The analog output of the ith stage can be expressed as

$$V_{Oi} = \left[2V_{Oi-1} - b_i V_{ref}\right] z^{-1} \tag{1.6}$$

where b_i is +1 if the ith bit is "1" and –1 if the ith bit is "0".

The iterative version of algorithmic A/D converter given in Figure 1.8 consists of a sample-hold amplifier circuit, a gain-of-2 amplifier, a comparator, and a reference subtraction circuit. The operation of the converter involves first sampling the input signal by connecting switch S1 to V_{IN}. Sampled V_{IN} is then applied to the gain-2-amplifier. To extract the digital information from the input signal, the resultant signal, denoted as V_A is less than V_{ref}, the corresponding bit is set to "0" and V_A is uncharged. The resultant signal, denoted by V_B, is then transferred by means of switch S1 back into the analog loop for another iteration. This process occurs until the desired number of bits have been obtained, whereupon a new sampled value of the input signal will be processed. The digital word is processed in a serial manner with the MSB first. A distinct advantage over the pipeline configuration is that all of the gain-of-2 amplifiers are identical because only one is used in an iterative manner. Sources of error for this A/D converter include low operational amplifier gain; finite input offset voltage in the operational amplifier, charge injection from the MOS switches, and capacitance voltage dependence.

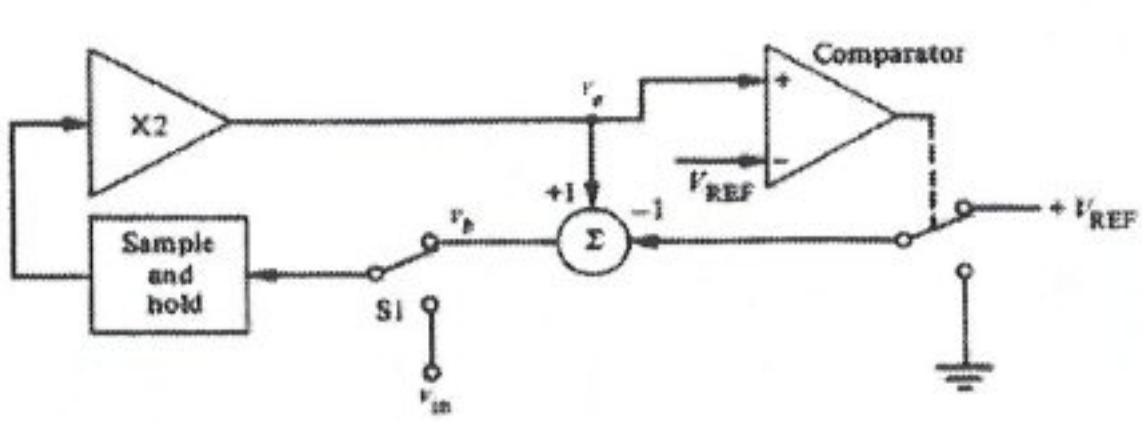


Figure 1.8 Implementation of the iterative, algorithmic A/D converter [3].

The successive approximation A/D architecture is a very general one, as has been shown. If serial D/A converters are used, the conversion time is increased and the area required is decreased. In general, successive approximation A/D converters can have conversion times that fall with in the range of 10^4 to 10^5 conversions/second. They are capable of 8 to 12 bits of accuracy. The number of bits can be increased if trimming is permitted.

1.3 Parallel A/D Converters

This type of converters are commonly referred to as parallel or flash converters. In this type of converters the analog input is simultaneously compared with 2^N-1 reference voltages where the reference voltages are typically derived from a resistor string.

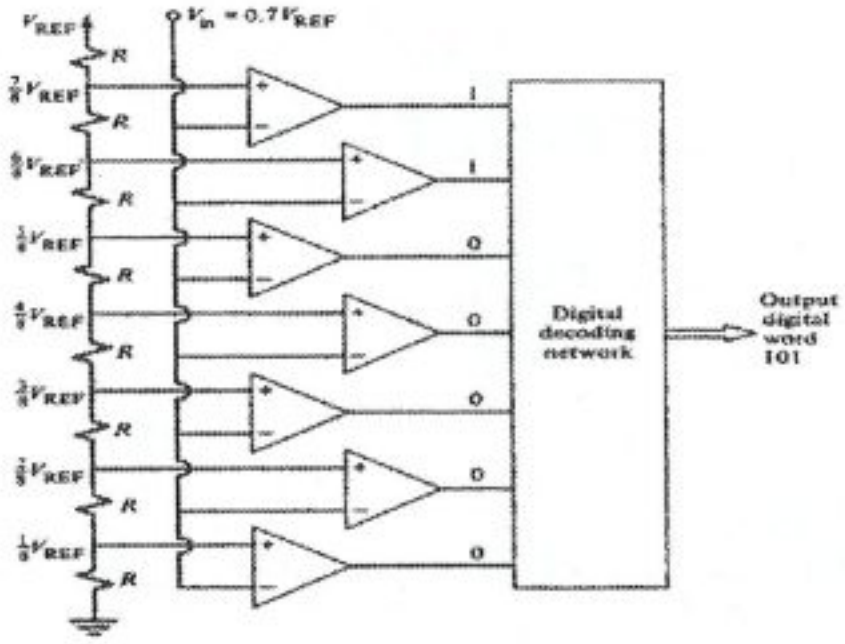


Figure 1.9 A 3-bit, parallel (flash) A/D converter [3].

The parallel A/D converter of Figure 1.9 converts the analog signal to a digital word in one clock cycle, which has two phases. So that this type of converters usually defined "word-at-a-time" converter. During the first phase, the analog input voltage is sampled and applied to the comparator inputs. During the second phase, the digital encoding network determines the correct digital output and stores it in a register/buffer. Thus the conversion is limited by how fast this sequence of events can occur. Complexity and power dissipation are problems for larger resolution.

In Figure 1.10, M successive approximation A/D converters are used in parallel to complete the N-bit conversion of one analog signal per clock cycle, often referred as time-interleaved conversion. The sample and hold circuits consecutively sample and apply the input analog signal to their respective A/D converters. N clock cycles later, the A/D converter provides a digital word output. If M = N, then a digital word is output at every cycle. If one examines the chip area for an N-bit A/D converter using the parallel A/D converter architecture (M=1) compared with the time-interleaved

architecture for M = N, the optimum point for area *and* throughput will be found for a value of M between 1 and N, for realizing the same resolution.

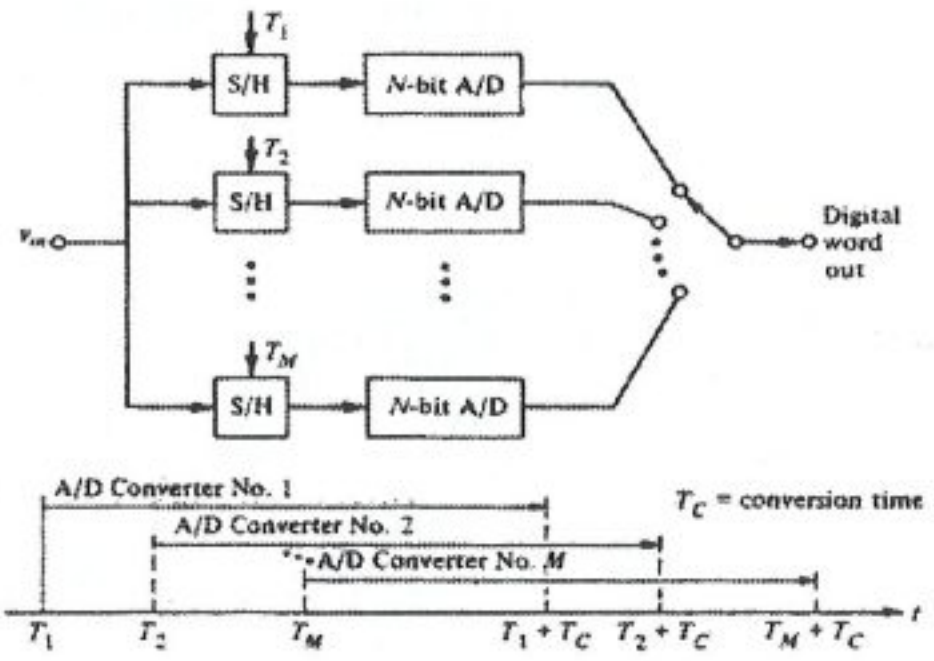


Figure 1.10 A time-interleaved A/D converter array [3].

Combining the parallel approach with a serial approach results in an A/D converter architecture with high speed and reasonable area. This approach is often called a "Pipeline A/D Converter", particularly if the number of series stages is greater than two. If the number of the series stages is exactly two then the topology is called "Series-Parallel" or often referred to as "Two-Step Flash" converters.

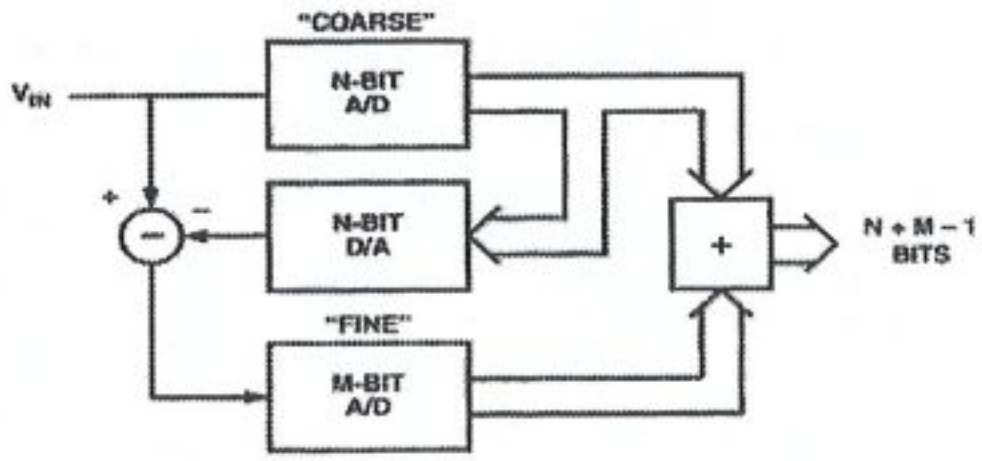


Figure 1.11 Block representation of two-step flash A/D converter architecture [23].

Two-step flash converters are used successively to exchange speed for reduction in complexity and power. The topology can be pipelined. Overlapping LSB of "coarse" stage and MSB of "fine" stage eases constraints on the A/D converter in the "coarse" (first) stage. Only DAC and subtractor circuits need (N+M-1) bit accuracy in this topology.

Two-step architecture described in Figure 1.11 can be generalized to multiple stages, where each stage finds a single bit. Specifically, the first stage finds the most significant bit, b_1; the second stage finds the next bit b_2, and so on. Unfortunately, a straightforward implementation of this approach would be too slow, since the final bit would not be available until residual errors ripple through the entire converter. A better approach is to also incorporate pipelining such that once the first stage completes its work, it does not sit idle while the remaining lower bits are found, but immediately starts to work on the next input sampled. A block diagram of a two-stage pipelined A/D converter is given in Figure 1.12. Using a pipeline architecture allows the designer to make trade-offs between area and conversion time. This topology is attractive for low power, high-speed data conversion applications, such as video and imaging.

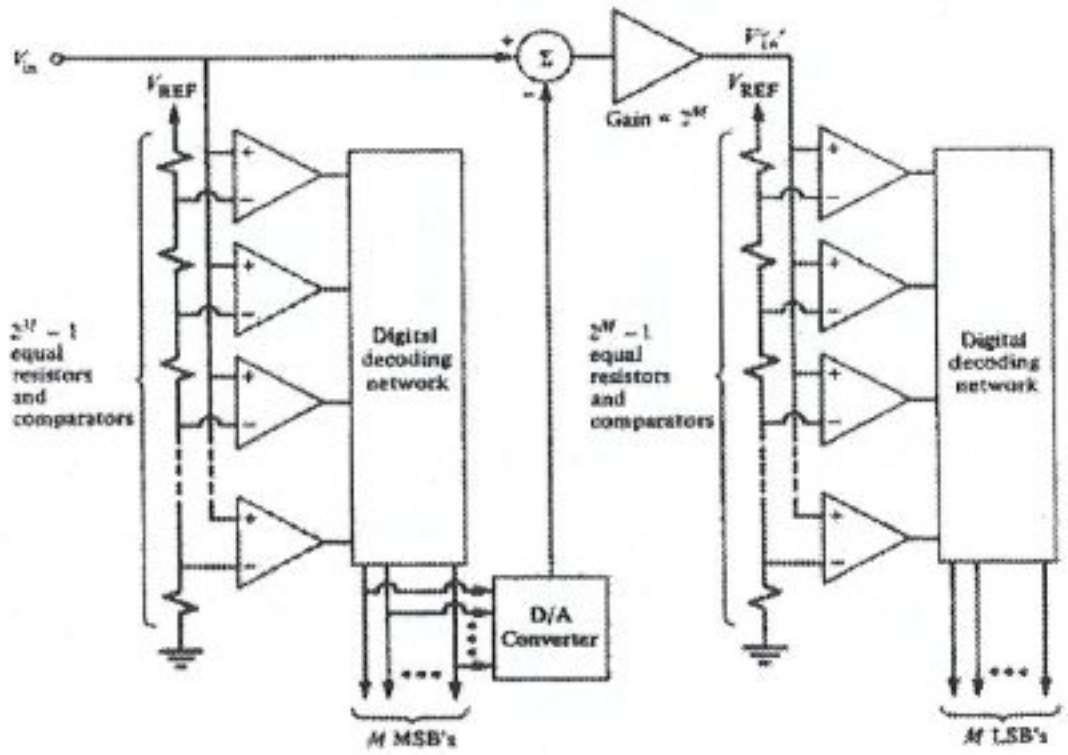


Figure 1.12 Two-stages Pipelined A/D converter configuration [3].

In Figure 1.12 a pipelined A/D converter using two M-bit parallel A/D converters is shown. The method first converts the M MSBs and then converts the M LSBs. Consequently only 2^{M+1}-2 comparators are required to convert a 2M-bit digital word.

For the configuration given in Figure 1.12, the analog input is applied to the left-hand string of 2^M-1 comparators during the first clock phase and the M MSBs are decoded during second clock phase. During the third clock phase, the M MSBs are converted to an analog equivalent, which is subtracted from V_{ref}, multiplied by a gain of 2^M, and applied to the right-hand string of 2^M-1 comparators. Finally, during the fourth clock phase, the M LSBs are encoded. Thus, if the clock has two phases, then in two clock cycles a 2M-bit digital word will be converted.

A/D converters including self-calibrating, pipelined, oversampled, subranging and delta-sigma converters are classified as high performance A/D converters. As a brief explanation, in subranging A/D converter, the conversion is done in several cycles. In each successive cycle the gain of the residue amplifier is increased, until the full scale of the amplified residue voltage is reached. In this manner, errors can be corrected and removed on each successive cycle.

Oversampled A/D converters offer a means of exchanging resolution in time for resolution in amplitude in order to circumvent the need for complex precision analog circuits. This architecture includes a clocked feedback loop, which produces a coarse estimate that oscillates about the true value of the input, and a digital filter, which averages this coarse estimate to obtain a finer approximation. This approximation is more accurate to more bits at a lower sampling rate. If the resolution of digital estimator N is equal to "1" than the oversampling converter becomes a "Delta-Sigma A/D Converter". One advantage of Delta-sigma A/D, oversampling converters is that because they obtain resolution by linearly interpolating between two-states, they do not require an array of precision binary scaling elements for the D/A converter. This means that non-linearity errors will not exist. The output of the $\Delta\Sigma$ modulator is applied to a low-pass digital filter whose function is to operate on the 1-bit signal to remove frequencies and quantization noise above the desired signal bandwidth. The output of the filter is a multi-bit digital representation at a lower sampling rate. [17]

To review the current state-of-the-art of ADC topologies, an extensive literature survey was done covering past twelve years. A/D converters published are classified according to their resolution, speed, linearity, power consumption, area, topology and the application it is used in. Results of this work can be seen in Appendix A.

From all these tables, typical applications that require high-speed A/D converters can be distinguished with the desired resolution information given below:

• NTSC/PAL Decoders	8bit, 14-17MS/sec
• HDTV A/D Converters	8-10b,50-75MS/sec
• CATV channel modems	8-12b, 10-15MS/sec
• ADSL/HDSL Transceivers	12-16b, 3MS/sec
• CDDI Transceivers, VG	8-10b, 30-60MS/sec
• Mag Storage Read Channels	6-8b, 75-150MS/sec
• High-Performance Imagers	12b, 75MS/sec
• Supercollider Data Analyzers	12-16b, 60MS/sec

Table 1.1

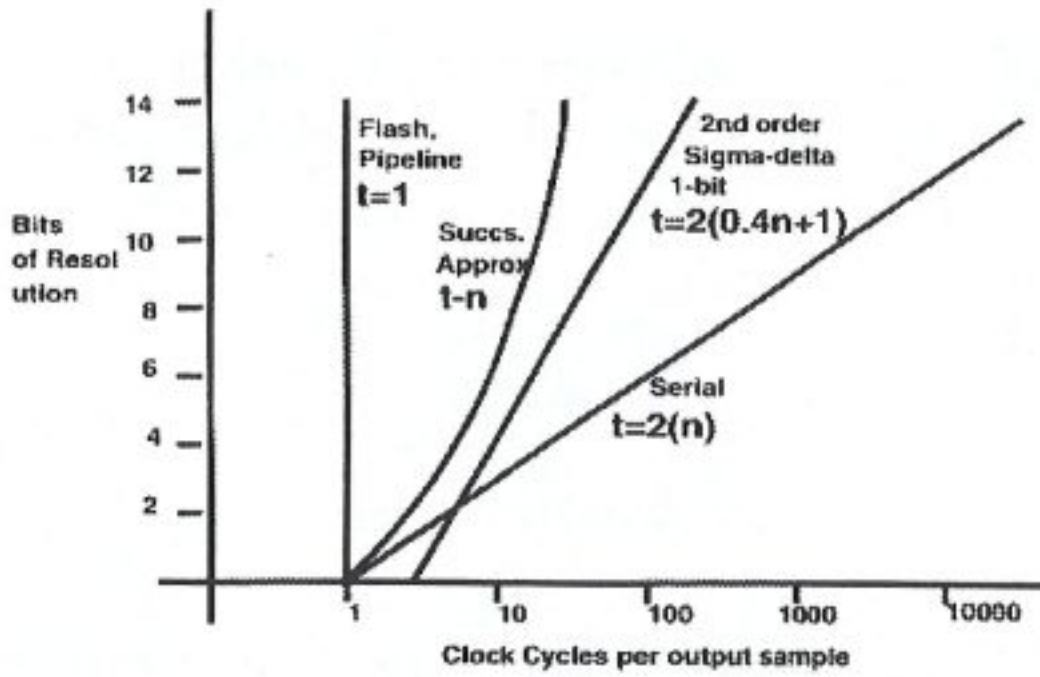


Figure 1.13 Qualitative comparison of ADC techniques.

As can be seen from Figure 1.13, for fastest applications a Flash or a Pipelined A/D Converter is needed. In the following chapter, proposed design specifications and topology will be examined in detail, giving the reasons of the design decisions made in this work.

2 . PERFORMANCE MEASURES OF ANALOG-TO-DIGITAL CONVERTERS

In this chapter, we concentrate on specific performance measures and metrics that are commonly used to specify and to quantify the operational characteristics of ADCs. Many of the performance metrics discussed here will be used in the design phase.

2.1 Quantization Error

Quantization error (V_Q) is the difference in magnitude between analog input and the resulting digital code for the entire input range of the converter.

This phenomenon is an unavoidable result of the fact that every A/D (or D/A) converter must operate with finite number of quantization levels to represent the original input signal. Figure 2.1 shows the DC input-output characteristic of an "ideal" 3-bit ADC with 8 quantization levels, and the corresponding quantization error.

A number of error/performance criteria have been developed to quantify this error. Note that the majority of the measures are defined on the DC input-output transfer characteristics.

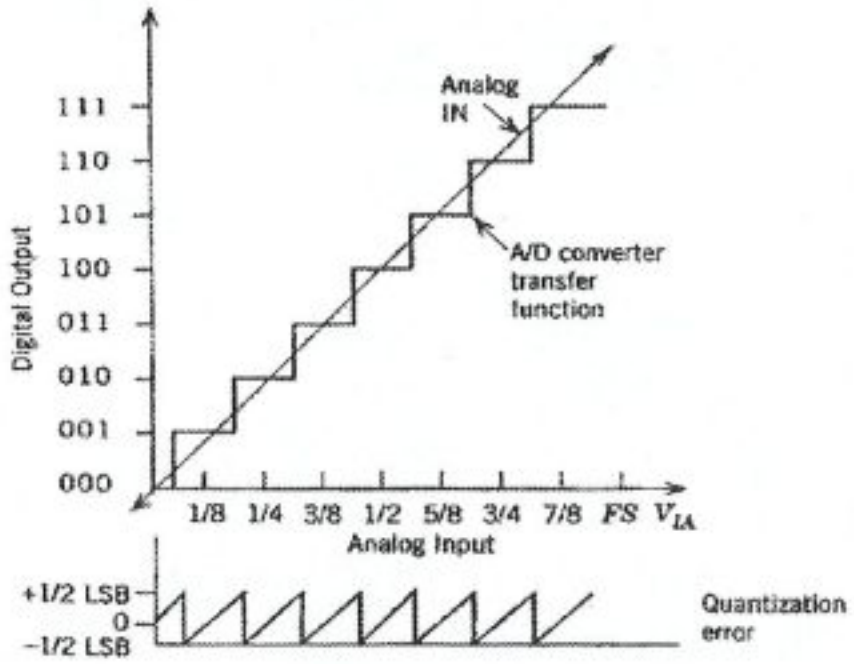


Figure 2.1 Input-output characteristic of an ideal 3-bit A/D converter and its quantization error [12].

2.2 Quantization Noise

Assume that the input signal is varying rapidly such that the quantization error signal, V_Q, is a random variable uniformly distributed between $\pm V_{LSB}/2$. The probability density function for such an error signal will be a constant value. The average value of the quantization error is found to be zero "0"; in a similar fashion, the rms value of the quantization error is given as $V_{LSB}/\sqrt{12}$. Recalling that the size of V_{LSB} is halved for each bit and assuming V_{REF} remains constant, we see that the noise power decreases by 6 dB for each additional bit in the A/D converter. Thus, given an input signal waveform, a formula can be derived giving the best possible signal-to-noise ratio (SNR) for a given number of bits in an ideal ADC. [2]

$$SNR = 20\log\left(\frac{V_{in(rms)}}{V_{Q(rms)}}\right) = 20\log\left(\frac{V_{REF}/\sqrt{12}}{V_{LSB}/\sqrt{12}}\right) dB \qquad (2.1)$$

$$SNR = 20\log\left(2^N\right) = 6.02N \ dB$$

Alternatively, a more common SNR formula is to assume V_{in} as a sinusoidal waveform between 0 and V_{REF}. Thus, the ac power of the sinusoidal wave is $V_{REF}/2\sqrt{2}$, which results in Eq. 2.2.

2.3 Dynamic Range

The dynamic range of a converter is usually specified as the ratio of the rms (root mean square) value of the maximum amplitude input sinusoidal signal to the rms of output noise plus the distortion measured when the same sinusoid is present at the output [2]. The rms output noise plus distortion is obtained by first eliminating the sinusoid from the measured output. To determine this component for an A/D converter, the output can be converted by FFT and the fundamental of the output signal can be eliminated, or a least-mean-squared fit can be used to find the amplitude and phase of sinusoid at the input signal's frequency and then subtracting the best-fit sinusoid from the output signal [2]. The dynamic range is also defined as the ratio of the largest input that can be converted to the smallest step size of the converter [12]. For example:

Vin(0,4V), resolution is 10 bits $\Rightarrow$ quantization step size = (4-0) / 2^{10} = 3.9062 mV

$\Rightarrow$ dynamic range of this converter can be found from

$\Rightarrow$ 4V / 3.9062mV = 1024

$\Rightarrow$ this number can also be expressed in decibels

$\Rightarrow$ 20log(1024) = 60 dB

Dynamic range can also be expressed as an effective number of bits using the Eq. 2.2.

$$SNR = 20\log\left[V_{in}(rms)/V_Q(rms)\right]$$

$$SNR = 20\log\left[\frac{V_{ref}/2\sqrt{2}}{V_{LSB}/\sqrt{12}}\right] \qquad (2.2)$$

$$SNR = 2\log\left(\sqrt{2/3}\,2^N\right)$$

$$SNR = 6.02N + 1.76dB$$

where the non-integer number N is called the effective number of bits (c.f. Eq. 2.3).

Finally, it should be mentioned that the distortion level (or nonlinearty performance) of many converters remains at a fixed level and is not a function of the input signal level. Thus, as the input signal level is decreased, the signal-to-distortion ratio decreases. This behavior occurs because the distortion level is often determined by component matching and thus is fixed once the converter realized. However, in some converters, the distortion level decreases as the input signal level is decreased, which is often a desirable property to have.

2.4 Resolution

The resolution of a converter is defined to be the number of distinct analog levels corresponding to the different digital words. Thus, an N-bit resolution implies that the converter can resolve 2^N distinct analog levels. Resolution is not necessarily an indication of the accuracy of the converter, but instead it usually refers to the number of digital input or output bits.

2.5 Effective Number of Bits (ENOB)

ENOB of a converter is defined with the equation given in Eq. 2.2.

$$ENOB = \frac{SNR - 1.76}{6.02} \tag{2.3}$$

For a perfect 12 bit A/D converter, SNR can be calculated as 72dB from Eq. 2.2, then

$$ENOB = \frac{72dB - 1.76}{6.02} = 11.68bits \tag{2.4}$$

2.6 Differential Nonlinearity (DNL)

In an ideal converter, each analog step size is equal to 1LSB(Least Significant Bit). In other words in an A/D, the transition values are precisely 1LSB apart.

Differential nonlinearity (DNL) is the measure of how uniform the transition step sizes are. Each step size is compared to the ideal step size:

$$DNL = LSB\ width - Code\ width$$
$$DNL = 1 - \frac{V(x) - V(x+1)}{LSB} \tag{2.5}$$

Thus an ideal converter has its maximum DNL of "1" for all digital values. If DNL is less than 1LSB then there will not be any missing codes. Whereas if DNL is less than 0.5LSB; the converter will be called "monotonic". The DNL is illustrated for a 4-bit ADC in Figure 2.2.

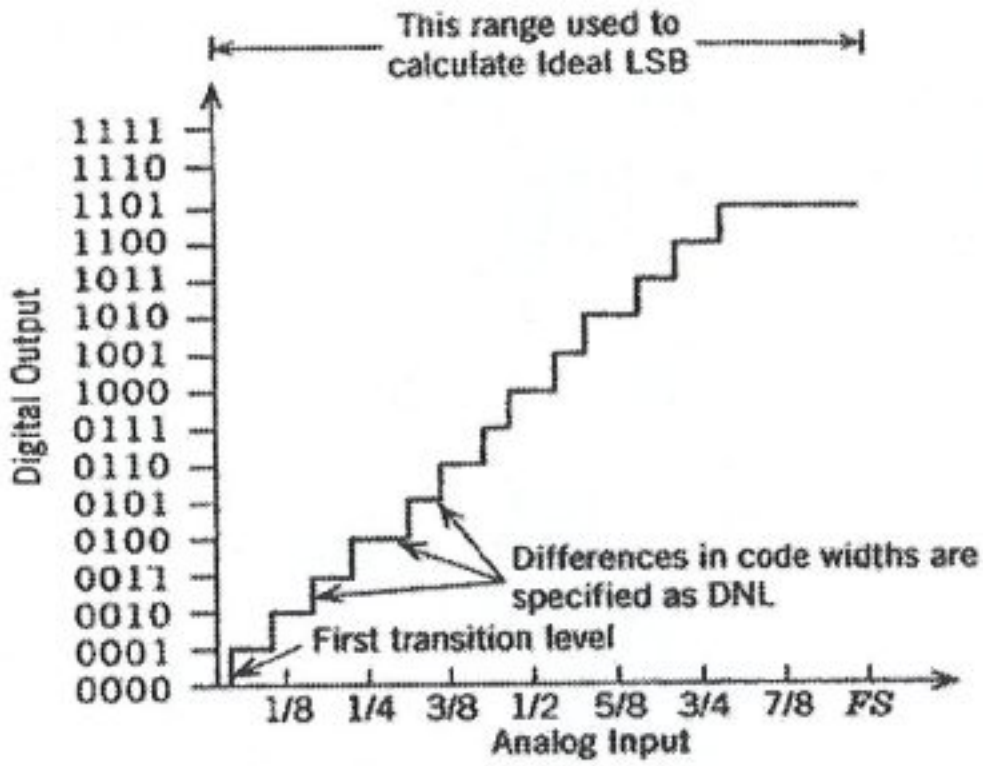


Figure 2.2 Illustration of DNL [12].

2.7 Integral Nonlinearity (INL)

The integral nonlinearity (INL) error is defined to be the deviation of the code midpoints from a straight line, or from their ideal location. Note that there exist different conventions concerning the definition of this "ideal line". Consequently, each convention will result in a slightly different INL value.

1. Drawing a straight line between the first and last code endpoints of the converter's transfer response.
2. Drawing the best-fit line using all measured code midpoints, such that the maximum difference (or perhaps the mean squared error) is minimized.
3. Drawing a straight line between the ideal location of the first and last code midpoints and using the ideal LSB to calculate the other midpoint locations.

$$INL = M(x) - \left(V_z - 0.5LSB\_DUT + xLSB\_DUT\right) \tag{2.6}$$

where M(x) is the midpoint of code x, V_z is the midpoint of the first code and DUT is the abbreviation for device under test in Eq. 2.6. The definition of INL is illustrated in Figure 2.3.

Note that a differential error is a particular step size at any specific location in the converter transfer function. Integral error is equivalent to the integration (summation) of the errors along the converters transfer function. (cf. Figure 2.4)

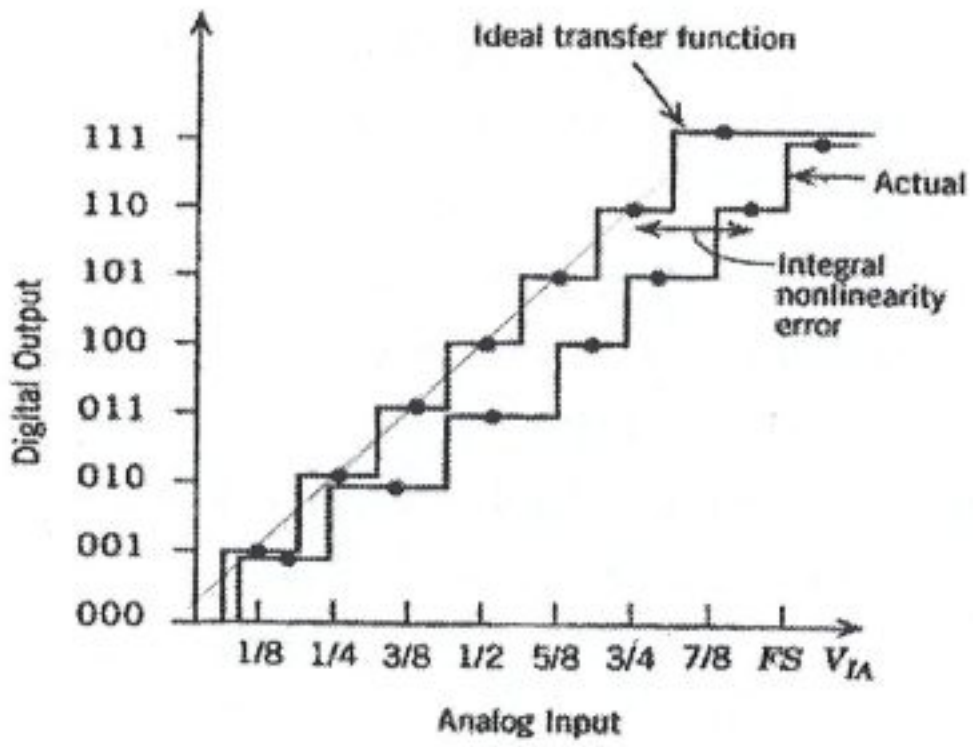


Figure 2.3 Illustration of INL for a 3-bit A/D converter [12].

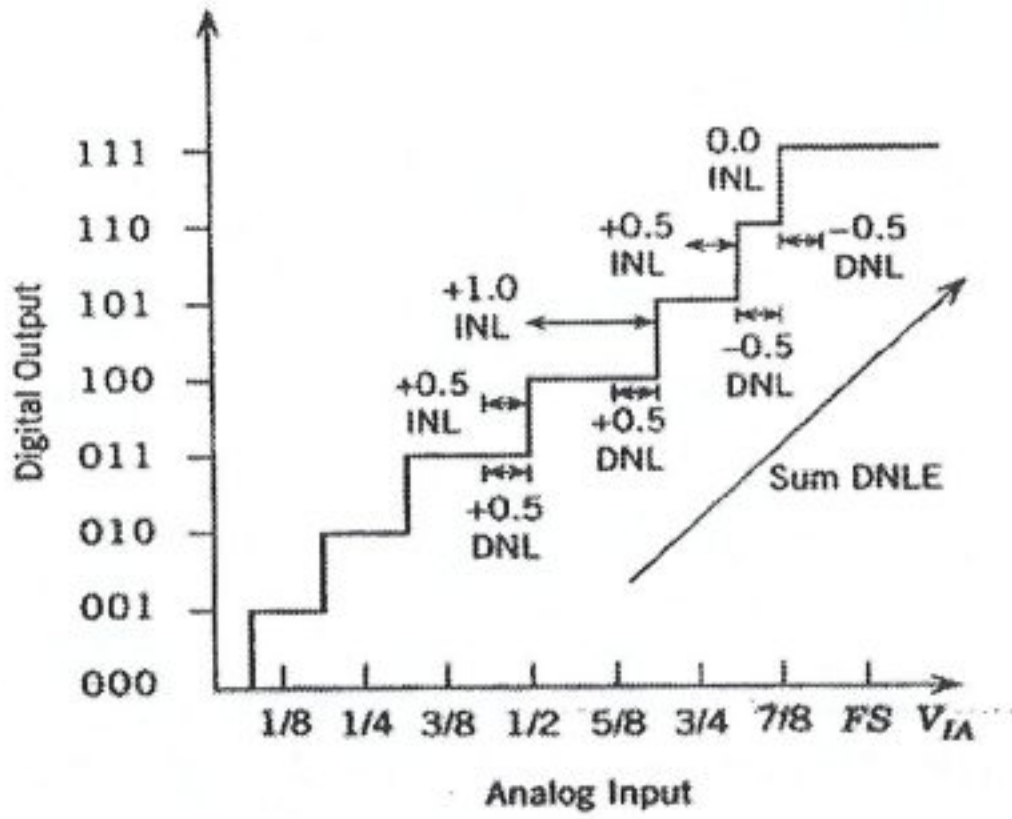


Figure 2.4 Relation of DNL and INL [12].

2.8 Absolute Accuracy

The magnitude of the deviation from the actual to the ideal transfer function of an ADC is called the absolute accuracy of the converter. The absolute accuracy includes the offset, gain and linearity errors (Figure 2.5).

Accuracy can be expressed as a percentage error of full-scale value, as the effective number of bits, or as a fraction of an LSB. For example; a 12-bit accuracy implies that that converter's error is less than the full-scale value divided by 2^{12}.

The term relative accuracy is sometimes used and is defined to be the accuracy after the offset and gain errors have been removed. It is also referred to as the maximum integral nonlinearity error (described in section 2.6) and we will refer to it as such.

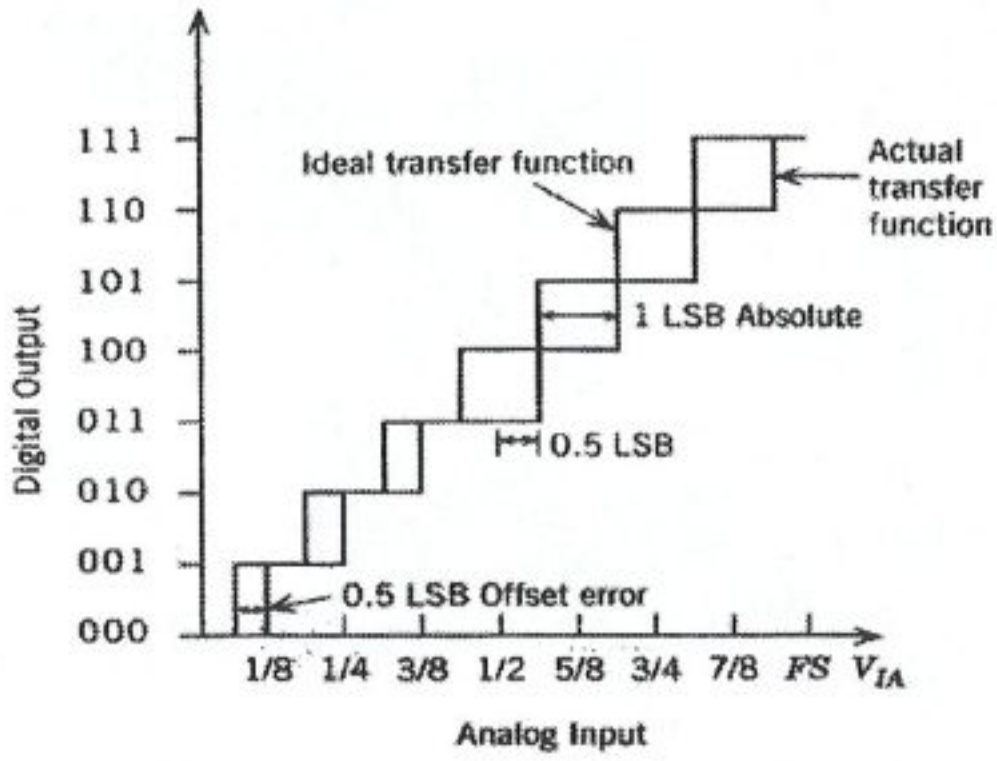


Figure 2.5 Absolute accuracy is the summation of other error sources [12].

2.9 Gain error

Gain is equal to slope of the converter's transfer function. The ideal slope of the transfer function is found by $V_{FULLSCALE}$ / (2^n - 1). The gain error is defined to be the difference (at the full-scale value) between the ideal and actual curves when the offset error has been reduced to zero in units of LSBs in Eq. 2.7. Gain error can also be specified as the deviation of the highest transition level on the ADC transfer function from its ideal location.

$$E_{gain(A/D)} = \left(\frac{V_{FULLSCALE}}{V_{LSB}} \right) - (2^N - 2) \tag{2.7}$$

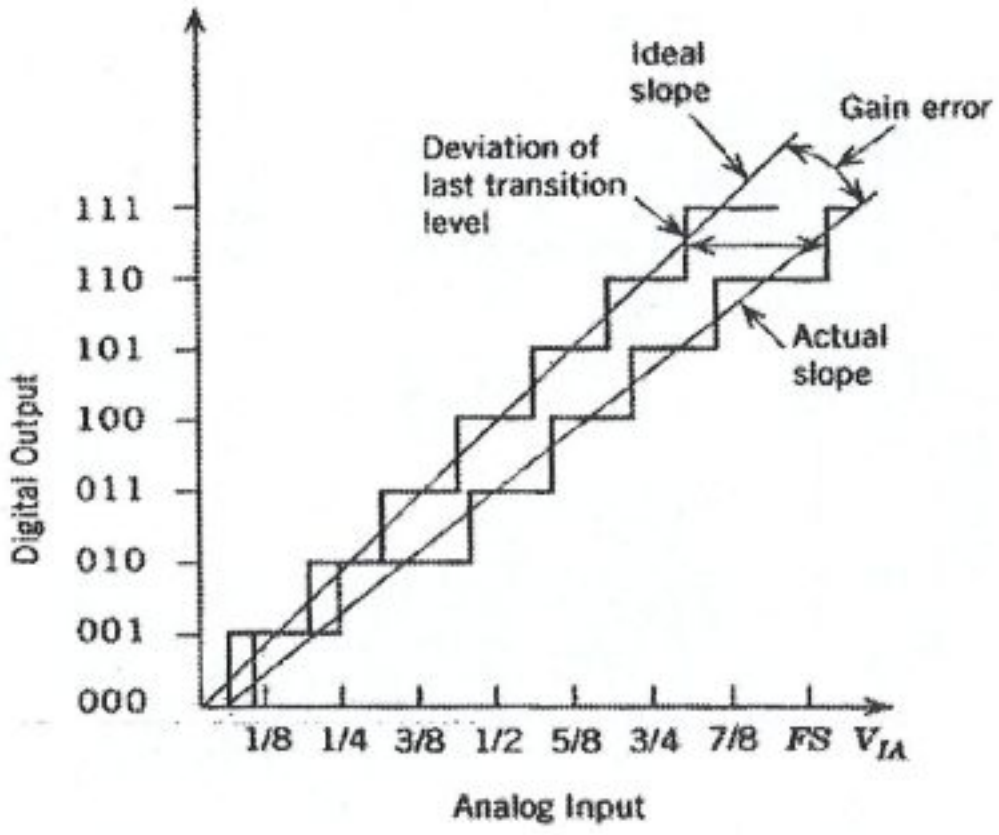


Figure 2.6 Illustration of gain error [12].

2.10 Offset Error

Identifies the deviation of the lowest transition level from its ideal location.

$$V_{off} = V_Z - (0.5LSB) \tag{2.8}$$

where V_Z is the first transition level voltage. The offset error between an actual and an ideal ADC transfer function is illustrated in Figure 2.7.

2.11 Transition Level

Each digital output code has associated with its two bounding transition levels. When the magnitude of the input lies between these two transition levels the code is generated and is the digital output. Ideally these transition levels are infinitely narrow thresholds; however, because of noise and other error sources the transition level will have a noise band with it. In this transition band there is a varying probability of the converter generating one code or the other. The point where there is a 50% chance of

converting one code or the other code is defined as the transition level illustrated in Figure 2.8.

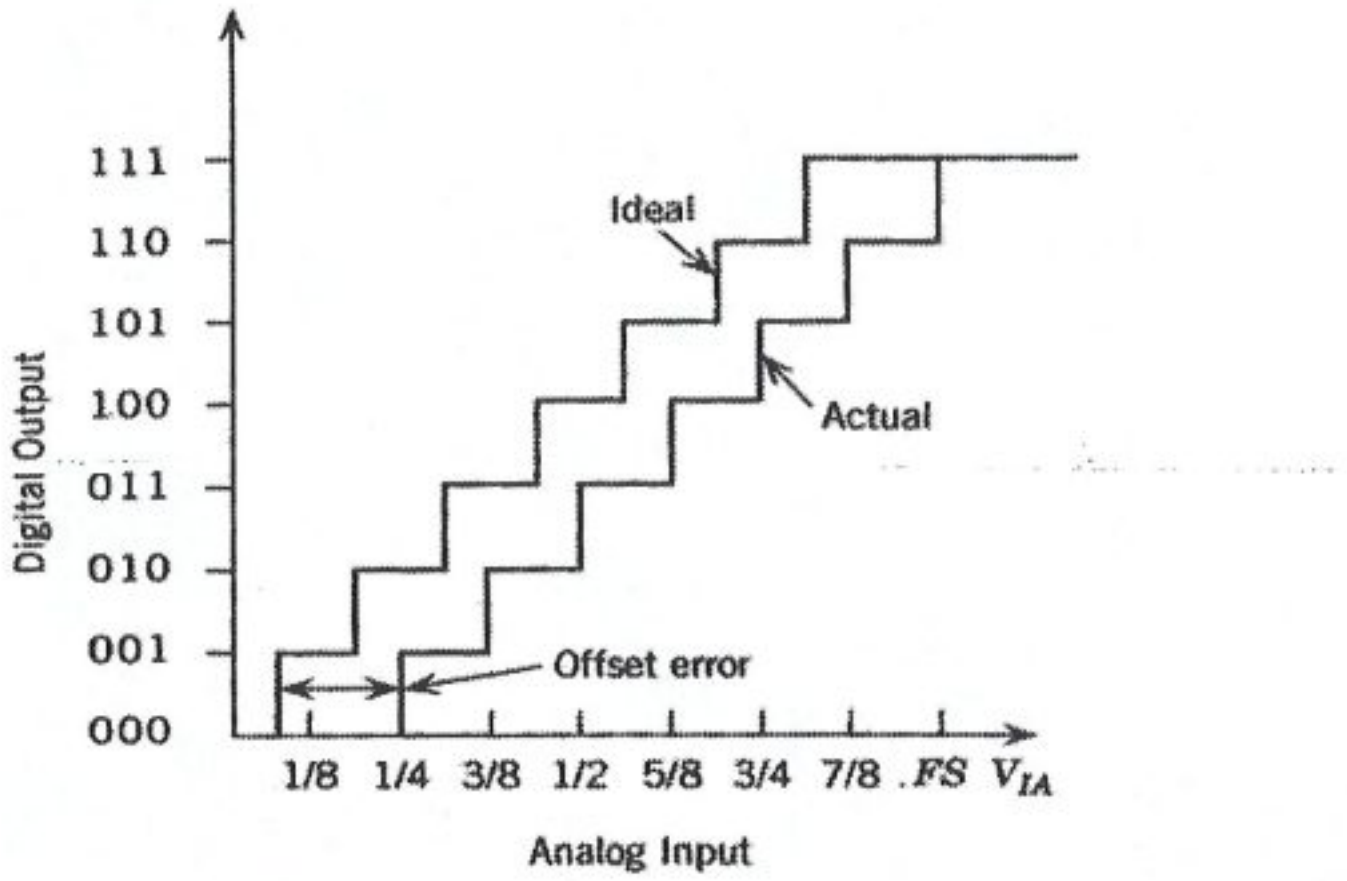


Figure 2.7 Illustration of offset error [12].

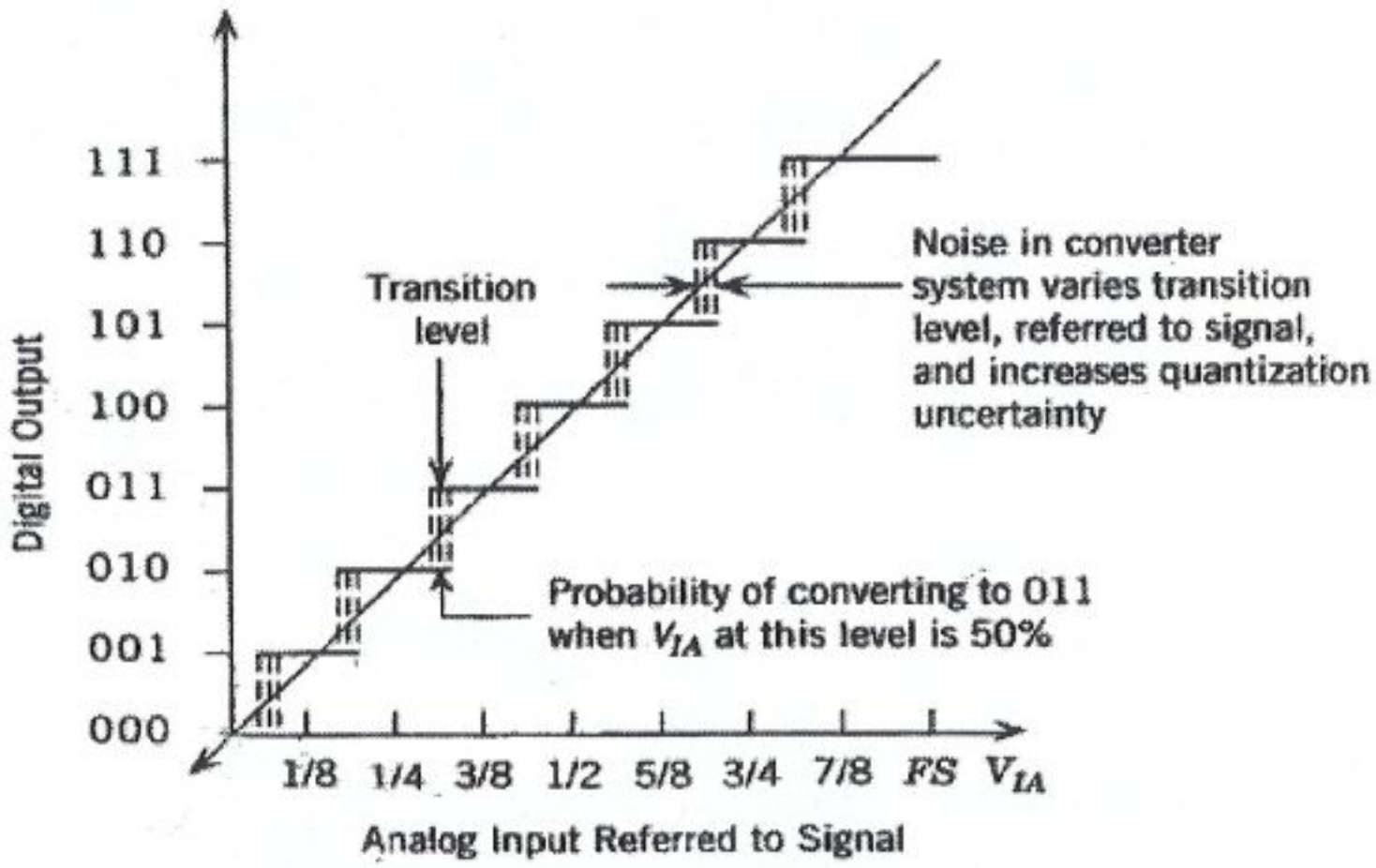


Figure 2.8 Illustration of transition level [12].

2.12 Monotonicity

In an ideal ADC, the converted digital output code is always expected to increase as the input signal increases. In other words, the slope of the converter's transfer response curve must always be positive. Thus, a converter is guaranteed to be monotonic, i.e., its transfer curve exhibits monotonically increasing behavior, if the maximum INL is less than 0.5LSB.

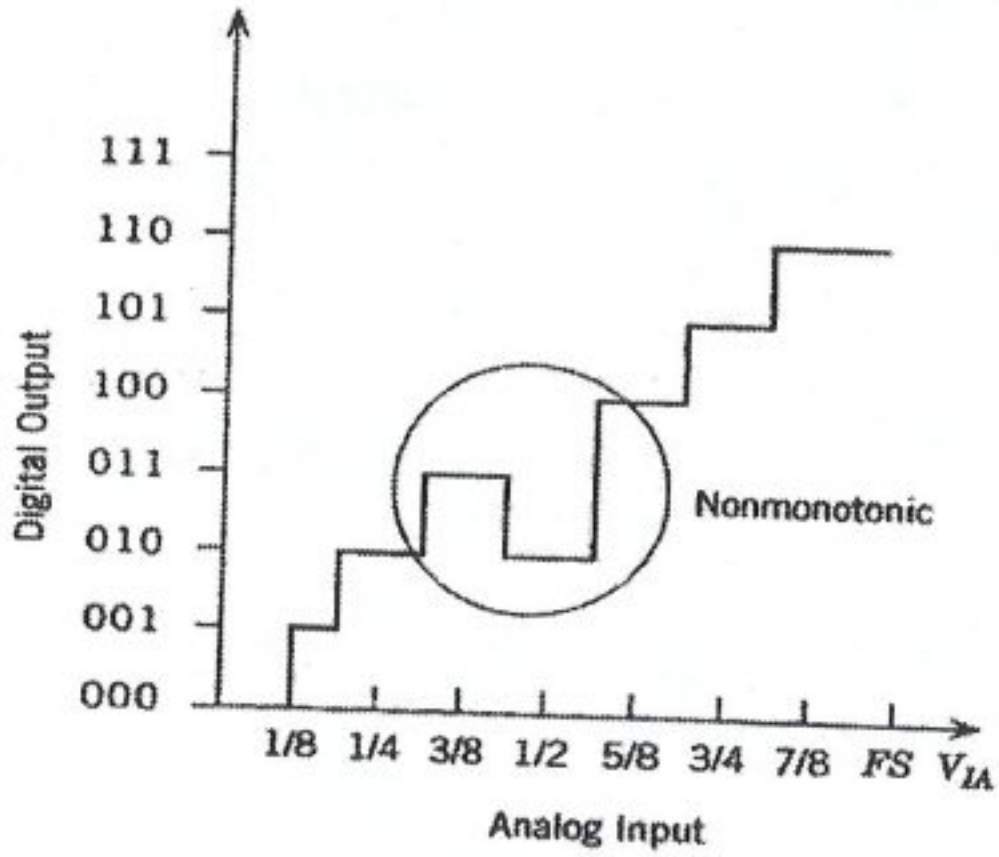


Figure 2.9 A nonmonotonic ADC transfer function [12].

2.13 Missing Code

A converter must be able to correspond all possible digital outputs to an analog input. An A/D converter is guaranteed not to have any missing codes if the maximum DNL error is less than 1LSB or if the maximum INL is less than 0.5LSB.

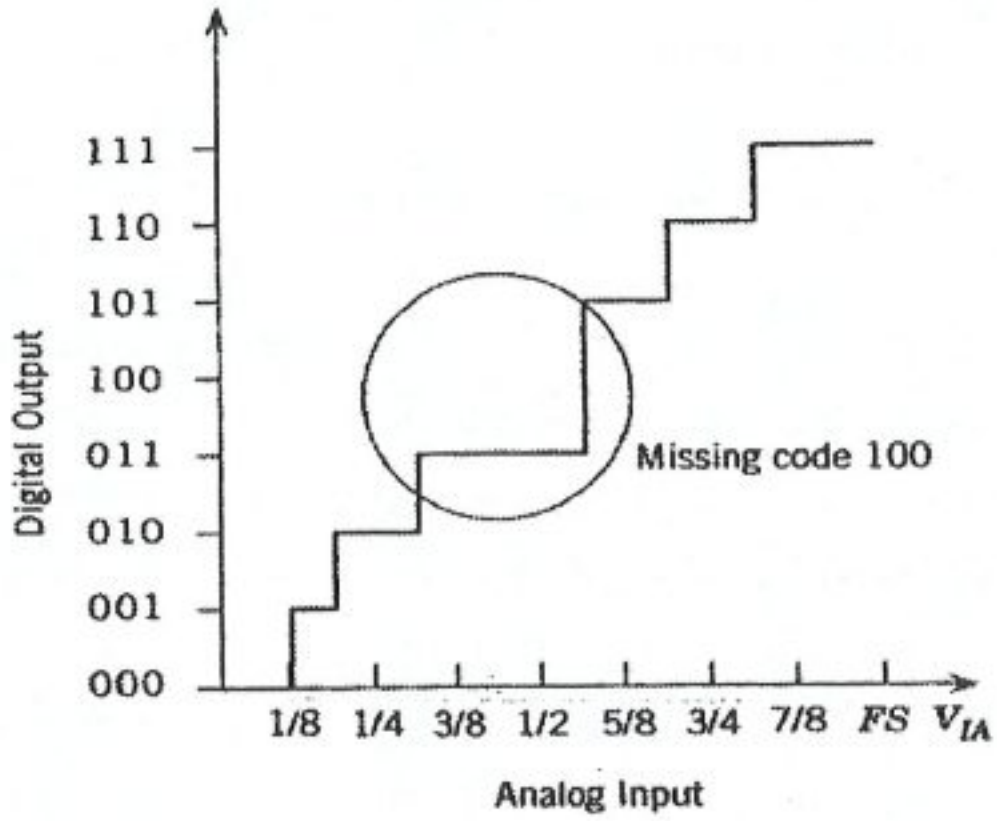


Figure 2.10 An ADC transfer function with a missing code (100) [12].

2.14 Differential Phase and Gain

Differential phase is the difference in the output phase of an A/D converter when a small high frequency sine-wave signal is superimposed on a low frequency signal at two predescribed amplitudes.

Differential gain is the ratio of the output amplitudes of an A/D converter with this small high frequency sine wave superimposed on the low frequency signal at the two predescribed amplitudes.

2.15 Conversion Time and Sampling Rate

The conversion time is the time taken for the converter to complete a single measurement including acquisition time of the input signal. Is also called the "Latency", the interval when the analog input is sampled and when the associated digital code is valid at the output of the converter.

On the other hand, the maximum sampling rate is the speed at which samples can be continuously converted and is typically the inverse of the conversion time. Note that, some converters have a large latency between the input and the output due to pipelining

or multiplexing, yet they still maintain a high sampling rate. The relation between sampling rate and conversion time (latency) is illustrated in Figure 2.11.

2.16 Sampling-Time Uncertainty

ADC's have limited accuracy when their sampling instances are ill defined. To quantify this sampling time uncertainty, also known as "Apperture Jitter", for sinusoidal waveforms, consider a full-scale signal, V_{in}, applied to an N-bit A/D converter with frequency f_{in}. Since the slope of V_{in} at the peak of a sinusoidal waveform is small, sampling time uncertainty is less of a problem near the peak values. However, the maximum rate of change for this waveform occurs at the zero crossing and can be found by differentiating V_{in} with respect to time and setting t=0. At zero crossing

$$\left.\frac{\Delta V}{\Delta t}\right|_{\max} = \pi f_{in} V_{amplitude} \tag{2.9}$$

If Δt represents some sampling-time uncertainty, and if we want to keep ΔV less than 1LSB, so that

$$\Delta t < \frac{V_{LSB}}{\pi f_{in} V_{ref}} = \frac{1}{2^N \pi f_{in}} \tag{2.10}$$

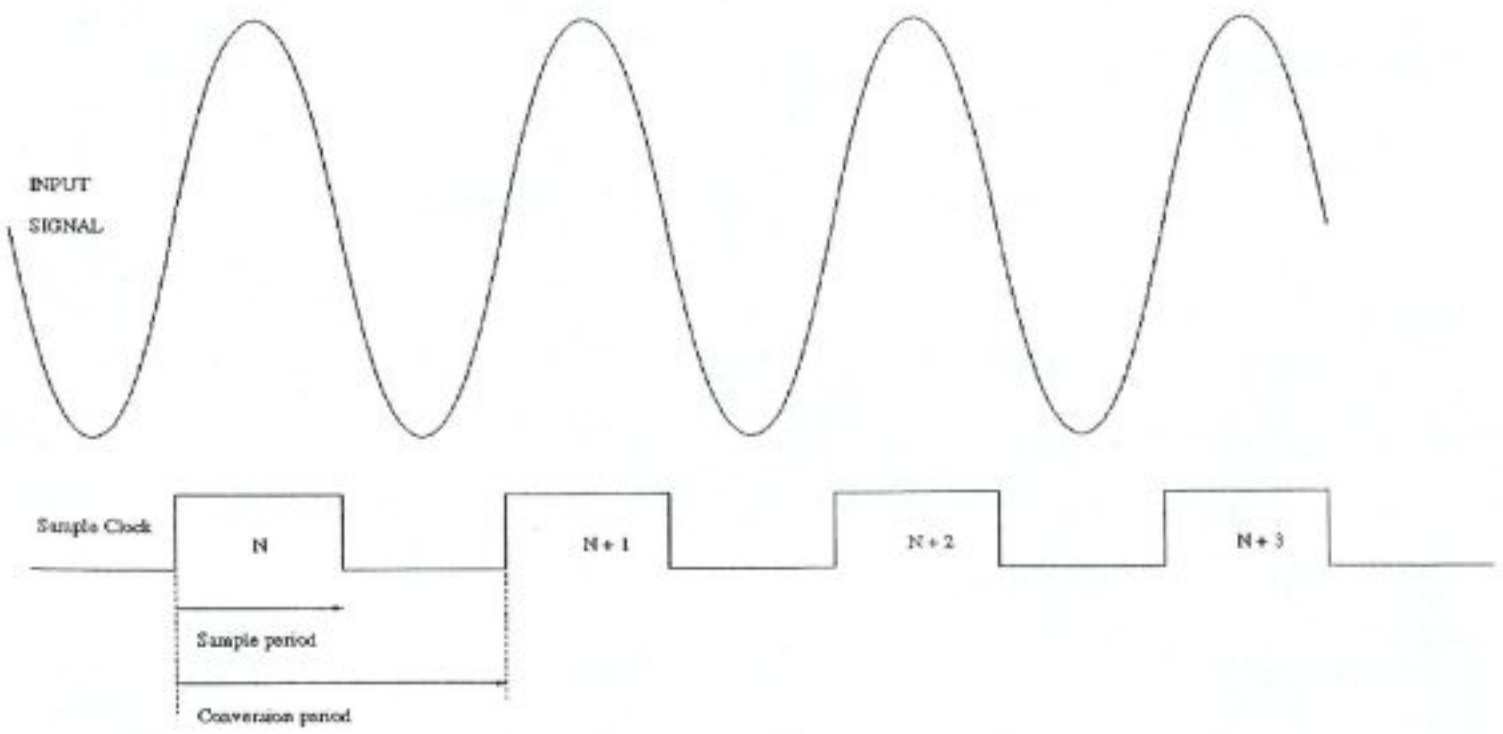


Figure 2.11 Illustration of sample period and conversion time.

2.17 Input Bandwidth

Input bandwidth specifies the highest frequency analog signal an ADC can convert and still meet its performance specifications. Usually converters are required to convert input signals with bandwidths up to $\frac{1}{2}$ their sampling rate (Nyquist rate). Input bandwidth is very a dependent quantity on maximum sampling rate.

Maximum sampling rate of a converter is a difficult to define number. In some cases the reduction in dynamic range (S/N ratio) can be used to define the maximum sampling rate. A definition can be given as:

The maximum sampling frequency of the converter for which the dynamic range measured over the Nyquist bandwidth is reduced with 3dB or 0.5 bit.

This definition gives a rough indication about the maximum sampling frequency. Thus, the input bandwidth can roughly be defined as the half of the maximum sampling rate.

3. PIPELINED ANALOG-TO-DIGITAL CONVERTERS

In this chapter, we will examine high-throughput A/D converters that are capable of producing high-resolution output (greater than 10-bits), and specifically concentrate on pipelined converter architectures. To start the discussion, we first summarize the main properties of various ADC architectures in the following, to serve as a means of comparison.

- Flash Converters
    - * Exponentially increasing hardware complexity with resolution
    - * Impractical above 8-bit resolution
    - * Large power dissipation and input capacitance.

- Two-Step Flash Converters
    - * Requires multiple clocks cycles per conversion
    - * Hardware increases exponentially with resolution.

- Pipelined Converters
    - * High degree of concurrency
    - * One output sample per clock cycle
    - * Approximately linear hardware cost with resolution
    - * Same throughput as Flash, with the cost of fast interstage processing
    - * Much less hardware than Flash converters
    - * Amenable to self-calibration and digital correction.

- Parallel Pipelined Converters
    - * Increase throughput by time-interleaving
    - * Share resources across multiple channels, keeping area and power reasonable
    - * Performance is limited by channel offset mismatch, channel gain mismatch, multiphase clock generation resulting jitter and skew.

The two-stage architecture described in Chapter 1 can be generalized to multiple stages, where each stage determines a single bit. Specifically, the first stage determines the most significant bit, b_1; the second stage finds the next bit b_2, and so on. Unfortunately a straightforward implementation of this approach would be too slow, since the final bit would not be available until residual errors ripple through the entire converter. So, multi-step A/D converters have replaced two-stage architectures, given in Figure 3.1, for higher speed applications.

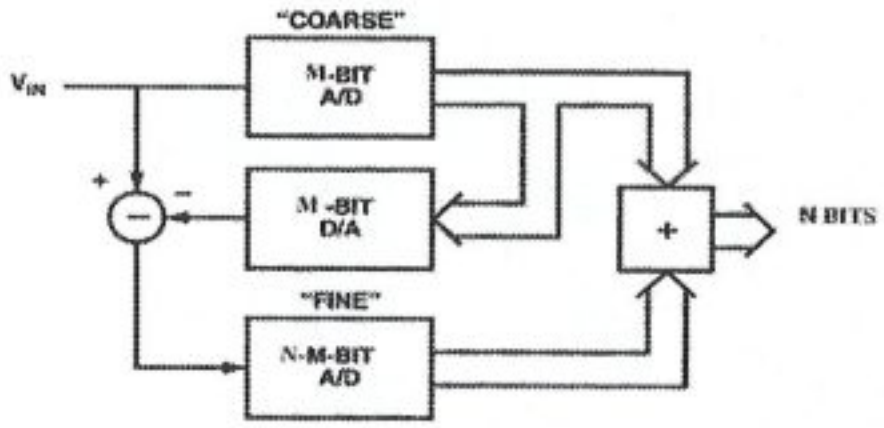


Figure 3.1 Typical two-step A/D converter architecture [21].

This topology substitutes speed for reduction in complexity and power, and it can use digital correction to ease the constrains on the coarse A/D converter. Performance limitations of this topology can be listed as follows:

- A front-end sample-hold amplifier is required.

$$V_{in} = V_A \sin(w_n t)$$
$$\frac{dV_{in}}{dt}\Big|_{\max} = V_A w_{in} \tag{3.1}$$

without a sample-hold (S/H) amplifier, the input is not allowed to change more than 0.5LSB during the time it takes to perform the coarse quantization, D/A conversion, and subtraction. If this time is denoted as t_{coarse}, then

$$t_{coarse} \leq \frac{1}{\pi f_{in} 2^{N+1}} \tag{3.2}$$

- The second "fine" A/D converter must have a resolution equal to N-bits. (Figure 3.2). In order to relax this demanding constraint for the stage-two ADC, residue voltage can be amplified by a factor of 2^M *before* the second A/D conversion step. This allows the second step ADC to have a lower resolution, and still produce the lower-order bits properly. (Figure 3.3)

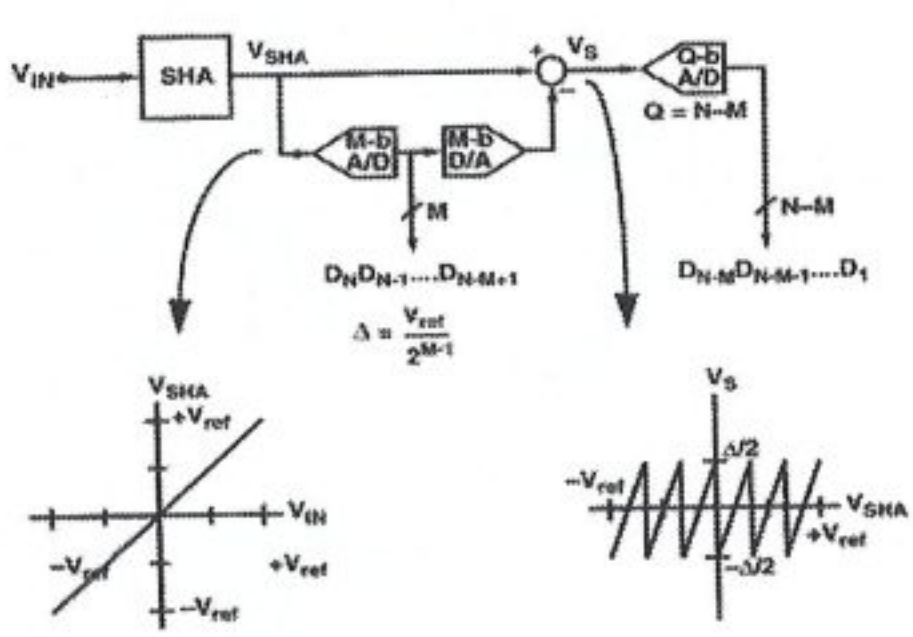


Figure 3.2 Multi-Step A/D converter figure of performance illustration [21].

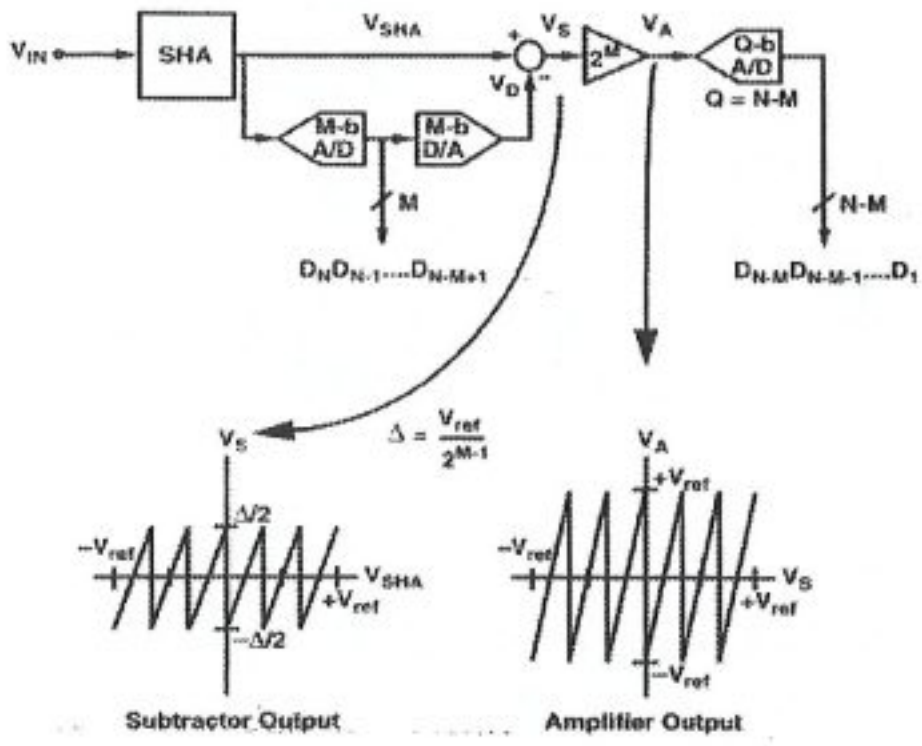


Figure 3.3 Multi-Step A/D converter's figure of performance illustration with internal amplification [21].

Thus, the front-end SHA, D/A converter, and subtractor directly affect overall performance. Conversion speed is set by the time needed to perform multiple operations. Note that there still exists an exponential dependence of circuit area and power dissipation with the desired resolution. Multi-step A/D converter's speed is proportional to the number of stages employed.

Combining series-parallel topologies together with a small number of bits/stage; results in a "Pipelined" topology which is very attractive for low power, high speed data conversion in applications such as video and imaging. A simple pipelined architecture is illustrated in Figure 3.4.

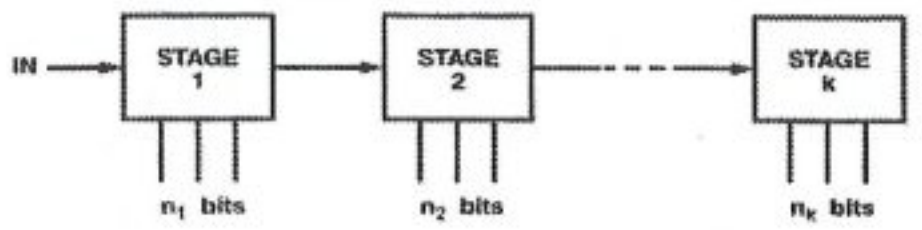


Figure 3.4 A simple Pipelined A/D converter architecture [21].

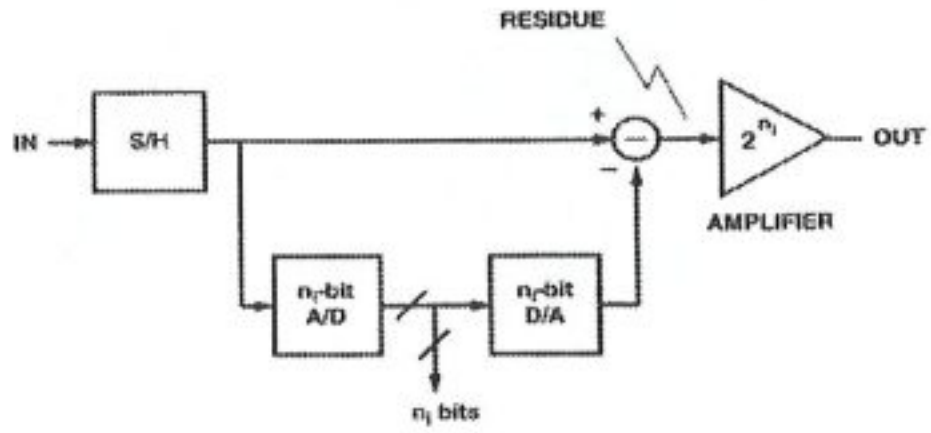


Figure 3.5 Implementation of i^{th} stage of a pipelined converter [21].

This topology trades conversion speed for latency by using interstage sample-hold amplifiers. Speed is limited by conversion speed of one stage in this topology. The number of components grows linearly with resolution, and scaling can be employed to minimize power dissipation and circuit area; if interstage amplification is employed.

Performance limitations of the topology and some possible remedies can be listed as follows:

* Pipelined ADC architectures require additional analog processing such as interstage sample-hold amplifier, D/A converter, subtractor and amplification,
* Latency may be a problem is some systems,
* D/A converters nonlinearity and amplifier gain error are the principal contributors to the overall converter' nonlinearity; these can be corrected using techniques such as self-calibration and error averaging.
* A/D nonlinearity and amplifier offset can be compensated by using digital error correction.

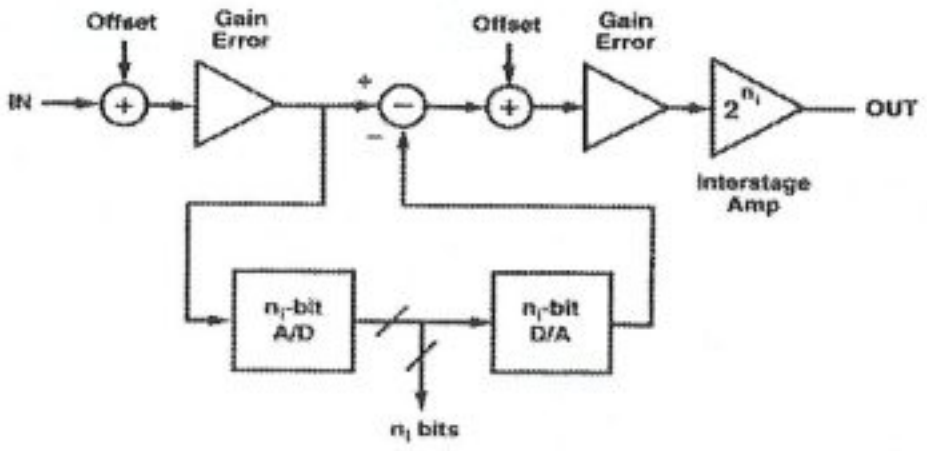


Figure 3.6 A pipelined A/D converter architecture model with offset and gain error for both the S/H amplifier and the residue amplifier [21].

3.1 Pipelined Operation

To understand how errors in a pipeline stage affect the converter's overall performance it is necessary to understand the ideal pipeline behavior.

Consider the 3-bit pipeline given in Figure 3.7, based on a 1-bit per-stage topology.

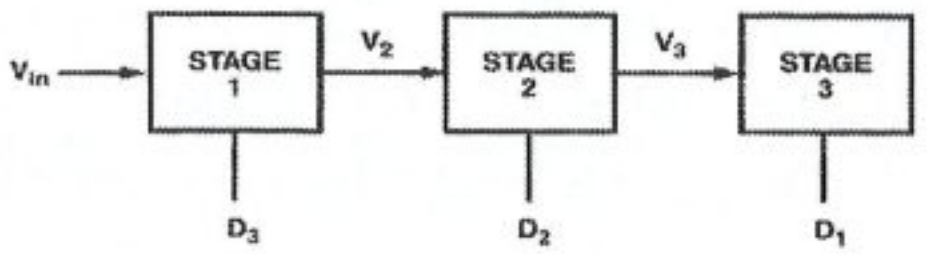


Figure 3.7 A 3-bit (1-bit per stage) pipelined A/D converter [21].

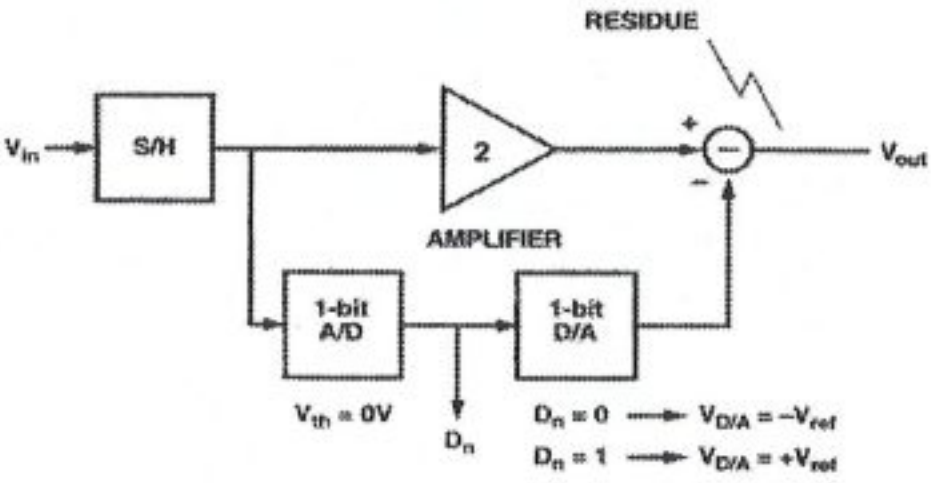


Figure 3.8 Implementation of each stage in Figure 3.7 [21].

The transfer function for the 1-bit pipelined stage is given in Eq. 3.3 and plotted in Figure 3.9.

$$V_{out} = 2V_{in} - D_n V_{ref} + \bar{D}_n V_{ref} \tag{3.3}$$

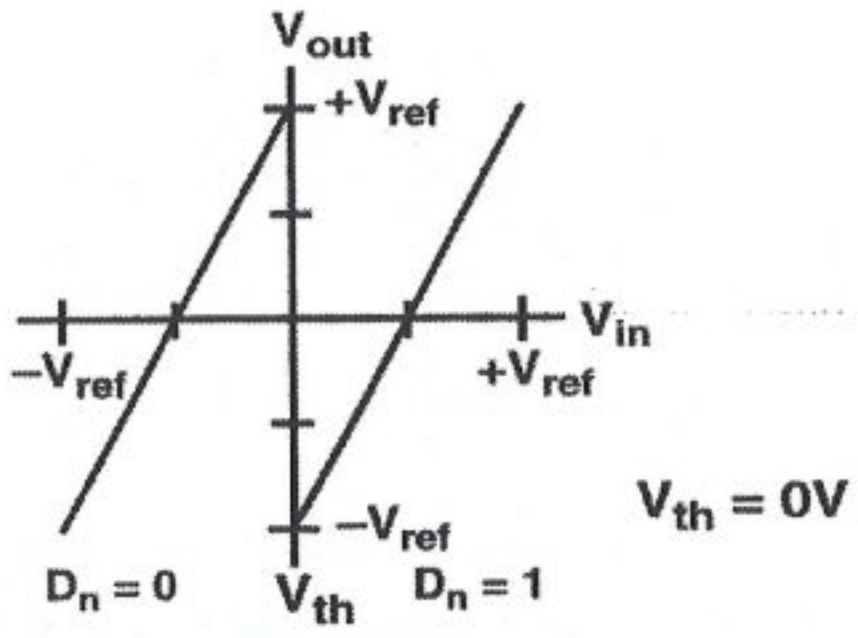


Figure 3.9 The transfer function of the 1-bit stage shown in Figure 3.8 [21].

For a pipelined A/D converter, the overall transfer characteristic can be generated by starting at the LSB stage (the final stage) and proceeding back to the MSB stage. For the pipeline example given above, the 3-bit A/D has the following transfer function:

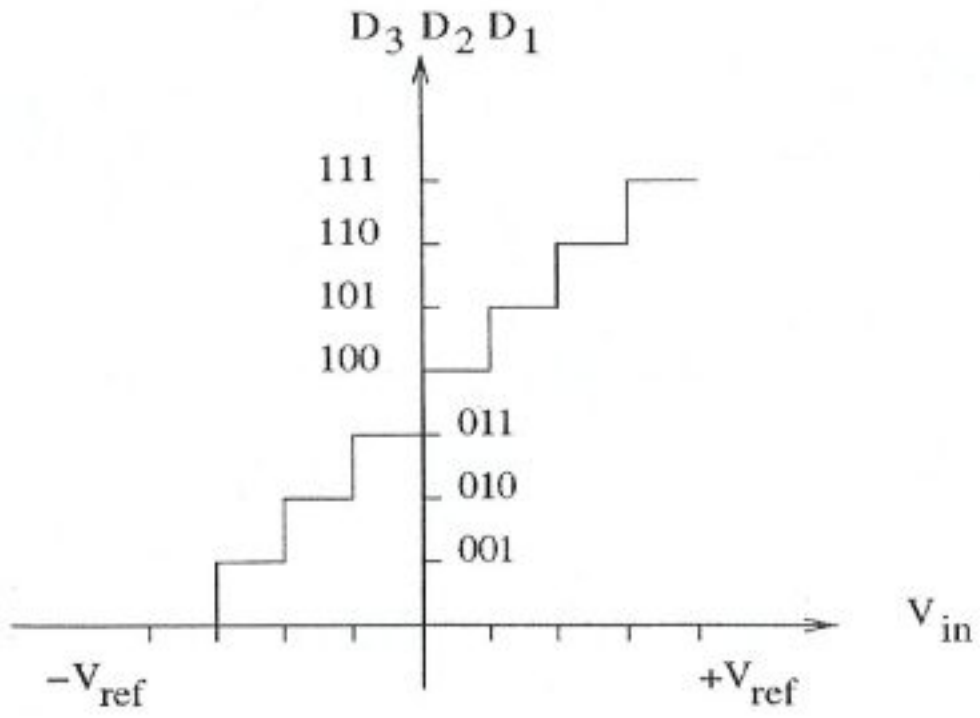


Figure 3.10 Transfer function of 3-bit pipelined A/D converter [21].

To derive the transfer function given in Figure 3.10; first the threshold voltages of the stages' comparators are found. For ideal comparators, as the analog input to the converter passes through these thresholds the digital output will change by 1LSB. So for stage "n":

$$\begin{aligned} V_n < 0V &\Rightarrow D_n = 0; \\ V_n > 0V &\Rightarrow D_n = 1 \end{aligned} \tag{3.4}$$

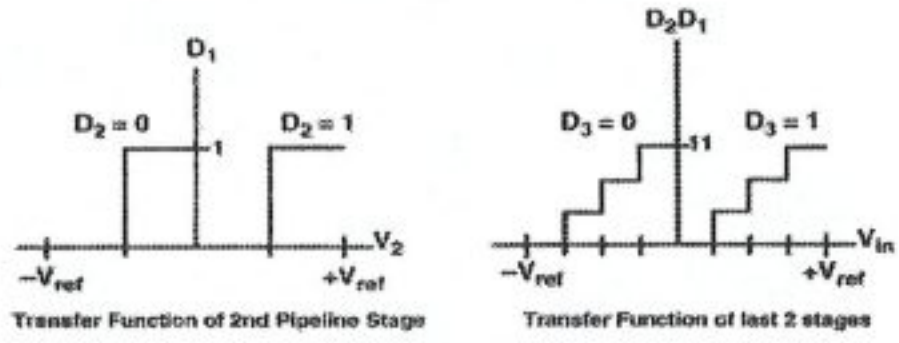


Figure 3.11 Detailed transfer function characteristics [21].

The transfer function stated above; points out an important fact about the pipeline architecture. Each group of stages is itself an A/D converter. This A/D simply quantizes the outputs of the preceding stage. Because both portions of each stage's transfer characteristics completely span the resolvable input range of the following group of stages, all digital codes of the group of stages are ideally accessed.

In Table 3.1 a brief summary of high speed pipelined ADC performance figures are given for comparison purposes. It can be seen from Figure 3.12 and Figure 3.13, that pipelined converters usually achieve a favorable balance between high resolution ($\geq$ 10 bits), high sampling rate, and "acceptable" silicon area. The price for these advantages, however, is paid in terms of a more complicated signal flow path, additional functions such as interstage DACs, and residue amplifiers. In these figures, FM1 is the ratio of sampling rate to equivalent technology f_t multiplied by 10^3 and FM2 is a power figure of merit normalized to technology f_t. It is given by

$$FM2 = \frac{2^B (SR)}{Pf_t} \tag{3.5}$$

where P is power dissipation, B is number of bits, Sr is sampling rate and f_t is the effective unity current gain frequency of the technology.

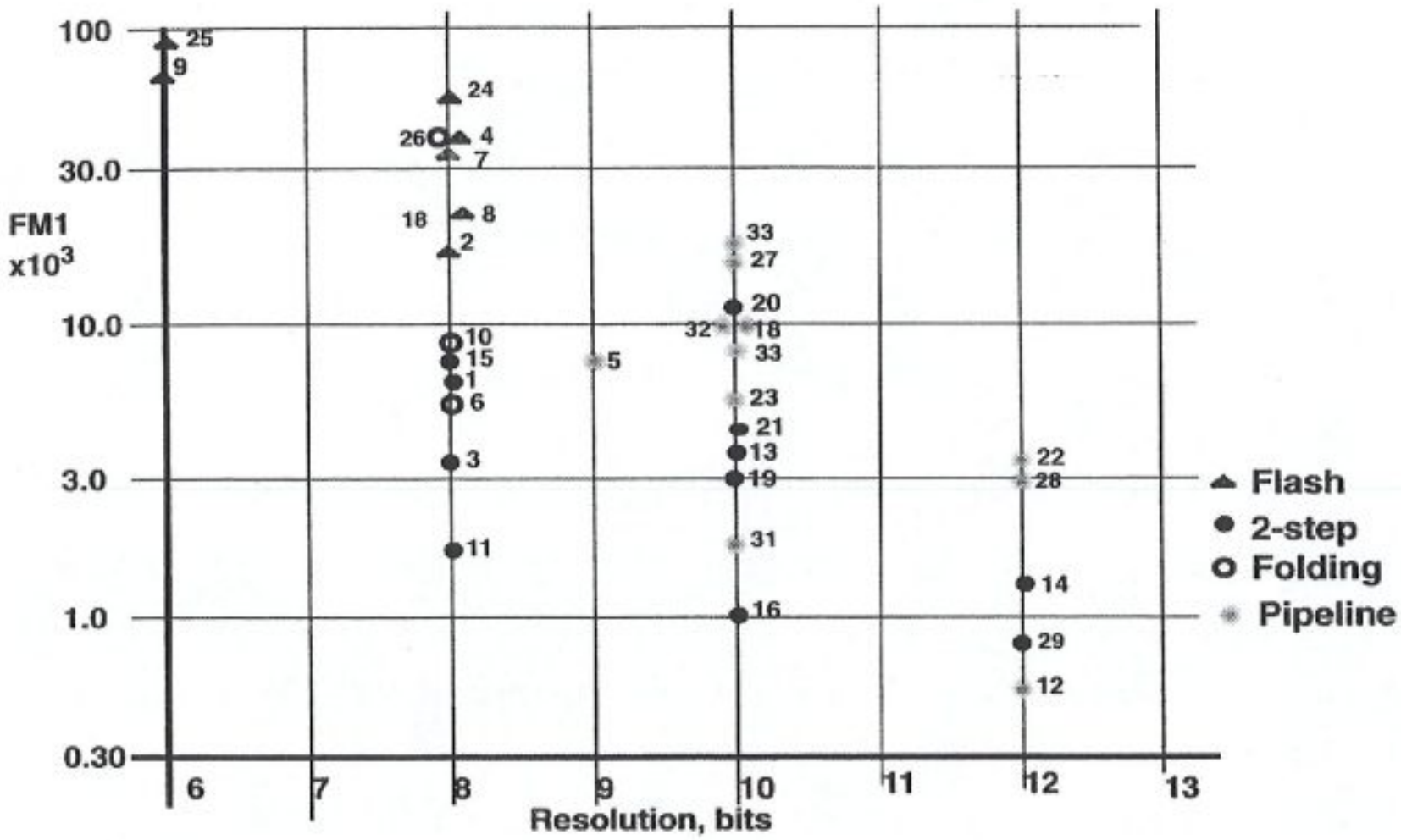


Figure 3.12 Comparison of speed figure of merit, between Flash, 2-Step, and Pipeline ADCs

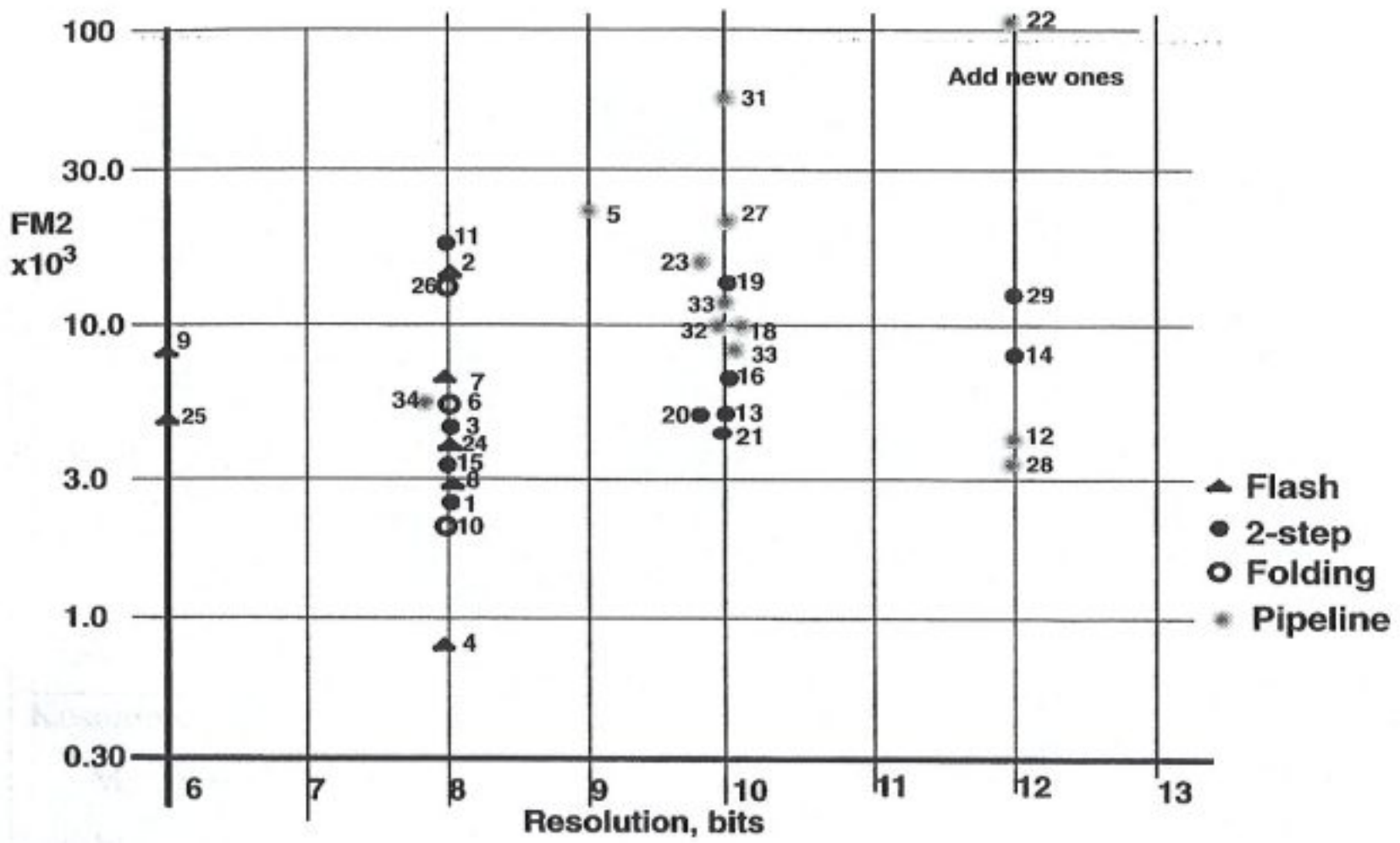


Figure 3.13 Comparison of power figure of merit, between Flash, 2-Step, and Pipeline ADCs

Author	Rate (MS/s)	Resolution (bits)	Technology	Power (W)	Area
Lewis, UCB, ISSCC86	5	9	3uCMOS	0.18	10k
Song, U.Ill. ISSCC88	1	12	1.5uCMOS	0.4	7.8k
Robertson, AD,ISSCC90	20	10b	BICMOS	1.0	85k
Lin, UCB, VLSI90	2.5	13b	3uCMOS	0.1	40k
Lewis, ATT, CICC91	20	10b	1uCMOS	0.3	12k
Corcora, HP, ISSCC92	2	12b	7Gbip	3.5	26k
Karanico,MIT, ISSCC93	1	15b	4G,2.4u BiCmos	1.8	100k
Kusumoto, Mats, ISSCC93	20	10b	0.8uCMOS	0.03	10k
Sone, Nec,ISSCC93	100	10b	0.8u BiCMOS	0.95	32k
Colleran,UCLA, ISSCC93	100	10b	12Gbip	0.8	30k
Conroy, VLSI92	85	8b	1.2uCMOS	0.8	35k

Table 3.1 Pipelined A/D converter performance summary.

3.2 Circuit Implementation of a Pipeline Stage

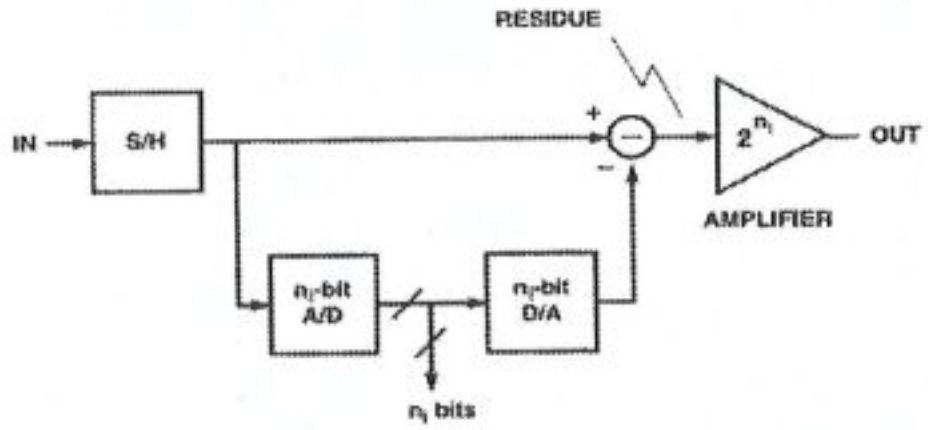


Figure 3.14 Implementation of i^{th} stage of a pipelined converter. [21]

A pipelined stage given in Figure 3.14, consists of a sample-hold amplifier in order to achieve analog pipelining, an A/D converter (usually flash A/D converters are preferred because of speed considerations), a D/A converter (current based or multiplying), a residue amplifier which will generate the analog input signal for the next pipelined stage, also called interstage amplifier, flip-flops for digital pipelining and fast adders to assemble the final digital output. A flash ADC generally consists of a resistor chain to generate the reference voltages, which is followed by an array of voltage comparators. Outputs of these voltage comparators are directly fed into the following D/A converter to establish digital-to-analog conversion for the rest of the operations. This converted analog signal, usually called the "residue" voltage, is applied to the interstage amplifier. Thus, an amplified residue voltage is obtained, which replaces the analog input signal for the following pipeline stage.

The most common error sources for these circuits are:

* Capacitor mismatch for Multiplying D/A converter
* Sampling switch charge injection
* Comparator offset
* Op-Amp gain error
* Resistor mismatch
* Offset of sample-hold amplifier and interstage amplifier

The general effect of these sources of error is to cause output voltages of a stage to not exactly match the resolvable input range of the remaining pipeline stages. Capacitor mismatch, op-amp gain error and D/A nonlinearty directly affect the converter's overall linearity. Calibration techniques or trimming must be employed if high linearity is desired. Comparator offset, which causes nonlinearity in the interstage A/D converter, and switch charge injection can be corrected by using digital correction. The basic idea of digital correction is to provide overlap between the quantization ranges of adjacent stages by using extra comparators. Using the proper digital encoding; a linear transfer characteristic can be obtained.

3. 3 MATLAB Simulation Results

In this section, we study the influence of various design parameters on the performance of a 4-bit ADC, which may form the main building blocks of a pipelined converter. MATLAB is used to model a four-bit flash Analog-to-Digital converter consisting of a resistor chain and an array of voltage comparators. The inaccuracy of resistor chain, comparator offset, supply voltage variation and input voltage range, which are the most important and most effective parameters on converter's performance, are modeled in order to see the effects on DNL and INL. Each of the parameters were set to vary one-by-one and also all together. Possible inaccuracies of the resistor chain that is used to obtain the reference voltages was modeled by a variation of the individual reference voltages. While modeling these parameters, process variation information and preliminary specifications of the Analog-to-Digital converter were taken into account. In the presence of this knowledge, the range of variation of the four parameters was set as follows.

PARAMETER (Individual)	MIN	MAX
Input Voltage Range	0.2 V	1.8 V
Supply Voltage	1.71 V	1.89 V
Comparator Offset	± 1 mV	± 160 mV
Reference Voltage Variation	-7 mV	7 mV

Table 3.2 Parameter limit values applied to MATLAB code.

MATLAB simulations were run on these parameters for one thousand different points per simulation. In each simulation only one of the parameters changed while others were set to their nominal value. In order to see what effects will occur because of this specified parameter variation. From the results obtained it was decided to do mixed simulations (all four parameters vary independently from each other in one simulation run) within a specified range for all parameters. These parameter set is given below.

PARAMETER(Mixed)	MIN	MAX
Input Voltage Range	0.8 V	1.6 V
Supply Voltage	1.71 V	1.89 V
Comparator Offset	± 5 mV	± 20 mV
Reference Voltage Variation	-7 mV	7 mV

Table 3.3 Parameter limit values that will be used in the input stimuli for combined parameter set MATLAB simulations.

It can be seen from the DNL and INL envelope graphs that each parameter has different influence on the performance of the 4-bit A/D converter. A deeper investigation of the graphs shows the following results:

PARAMETER	DNL (maximum)	INL (maximum)
Input Voltage Variation	± 0.01 LSB	± 0.01 LSB
Reference Voltage Variation	± 0.52 LSB	± 0.01 LSB
Comparator Offset	0.56 LSB	0.08 LSB
Supply Voltage Variation	- 0.6 LSB	0.01 LSB
MIXED	4 LSB	0.18 LSB

Table 3.4 Maximum and minimum values obtained for INL-DNL characteristic for each parameter.

DNL and INL values for input voltage variation does not change too much because reference voltages for fifteen levels of comparators are determined due to the input voltage level in order to be able to do comparison with all comparators.

A maximum tolerable DNL value -which is 0.52 LSB - occurs for a +/- 7 mV resistor voltage variation. Also it could be seen that the integral nonlinearity is not affected too much with changing the reference voltages obtained with a resistor voltage divider.

Comparator offset of 50 mV creates a DNL equal to 0.56 LSB, while an INL of 0.08 LSB is observed for 160 mV comparator offset. It could be dictated that comparator offset must not exceed 50 mV.

A ± %5 supply voltage variation creates ± 0.6 LSB DNL and the integral nonlinearity is not affected too much with supply voltage variation.

PARAMETER	Value
Input Voltage	1 V
Resistor Voltage Variation	± 7 mV
Comparator Offset	± 10 mV
Supply Voltage Variation	± % 5

Table 3.5 Maximum tolerable input parameter set.

As a result analog input voltage range should not be less than $0.8V_{pp}$; 7mV is the upper limit for resistor voltage variation; similarly 20mV is the critical value for comparator offset and 1.89Vis the maximum tolerable supply voltage in order not to

exceed 0.5LSB Integral-differential nolinearity ranges. All possible INL-DNL envelopes are given above for all parameters individually and for also combined set of input parameters. It was decided to use the limit values shown in Table 3.5 as a general guideline for the transistor level design of the 4-bit flash ADC components.

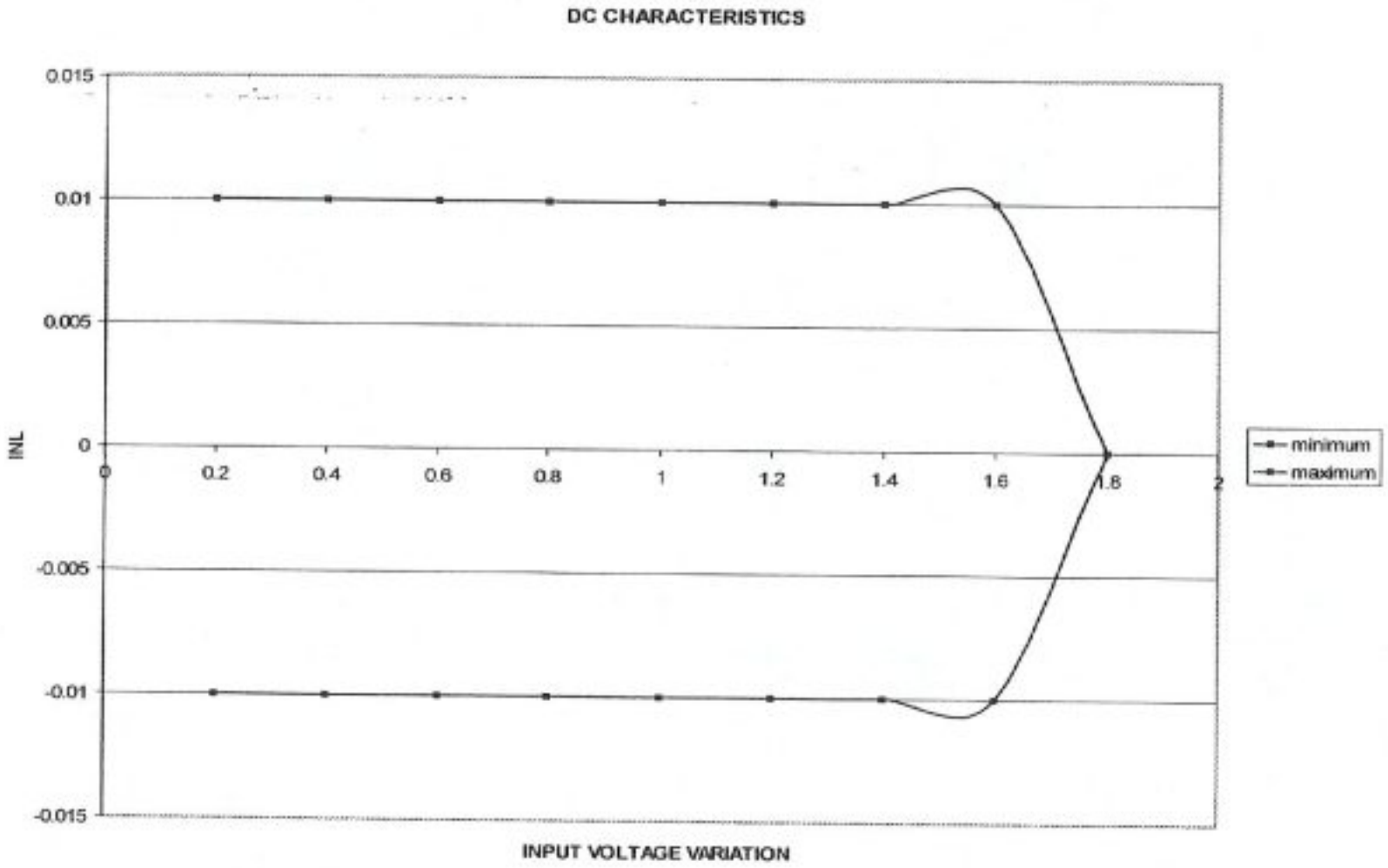


Figure 3.15 INL envelope obtained for different input voltage ranges.

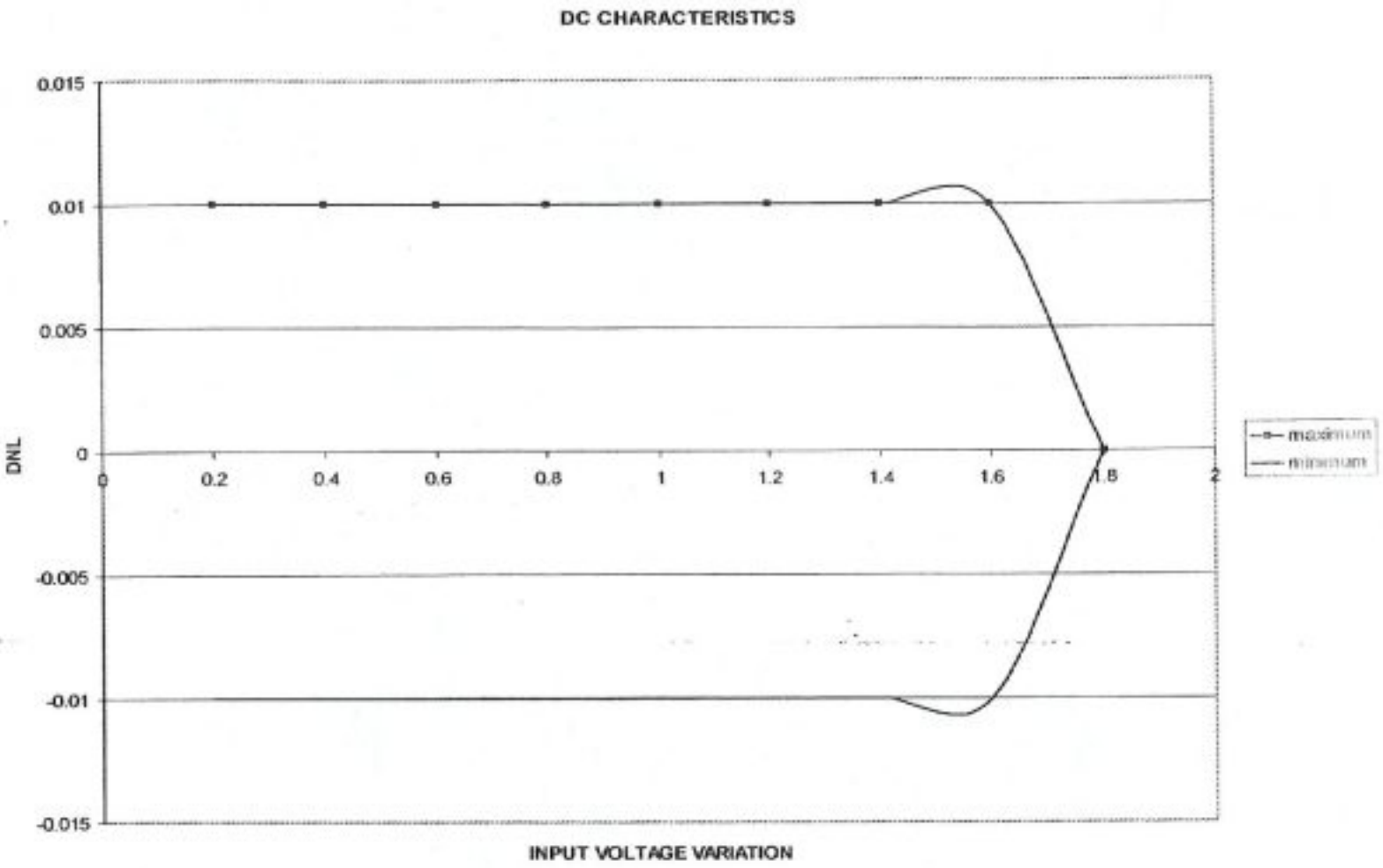


Figure 3.16 DNL envelope obtained for different input voltage ranges.

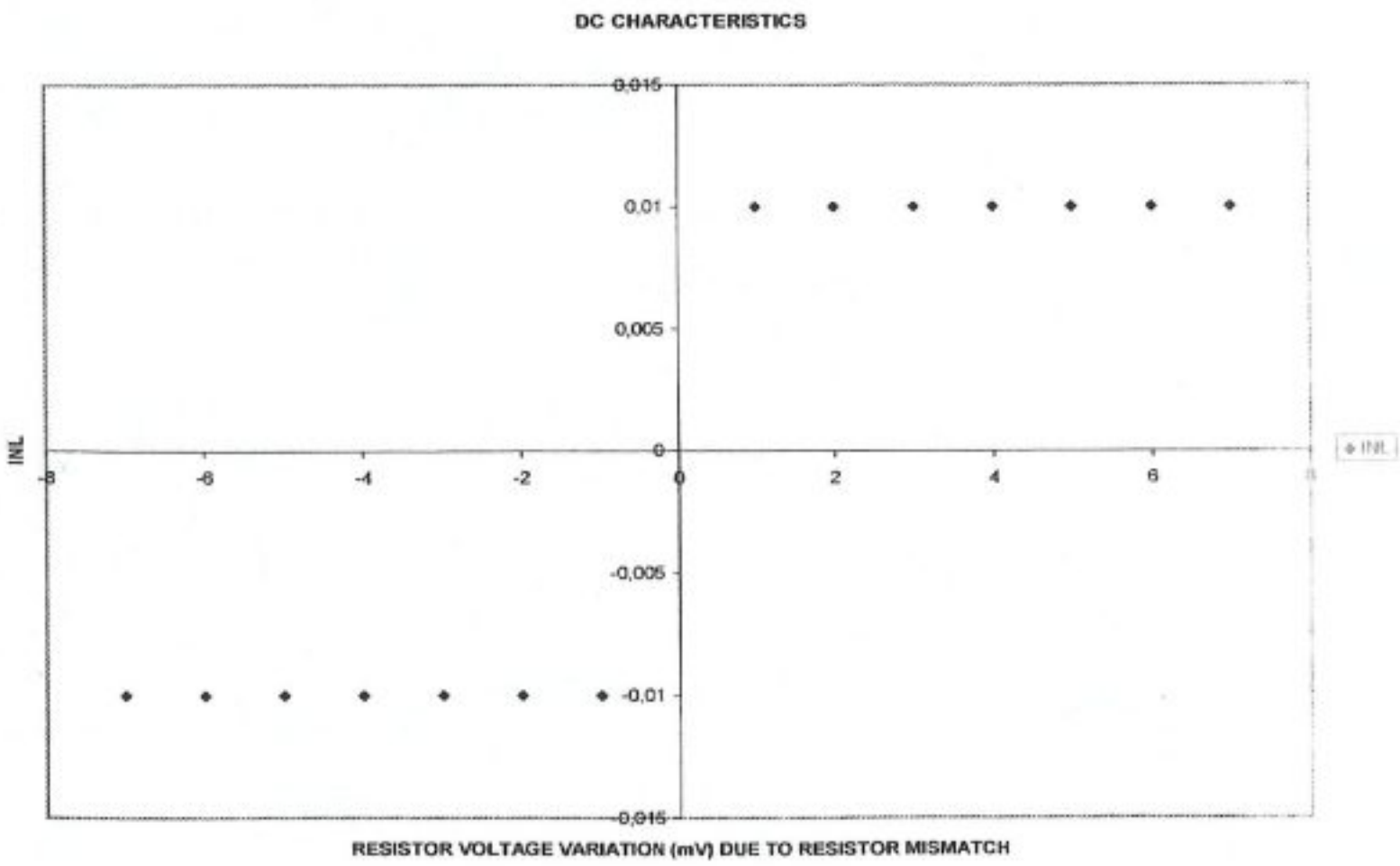


Figure 3.17 INL envelope obtained for different resistor voltage variations.

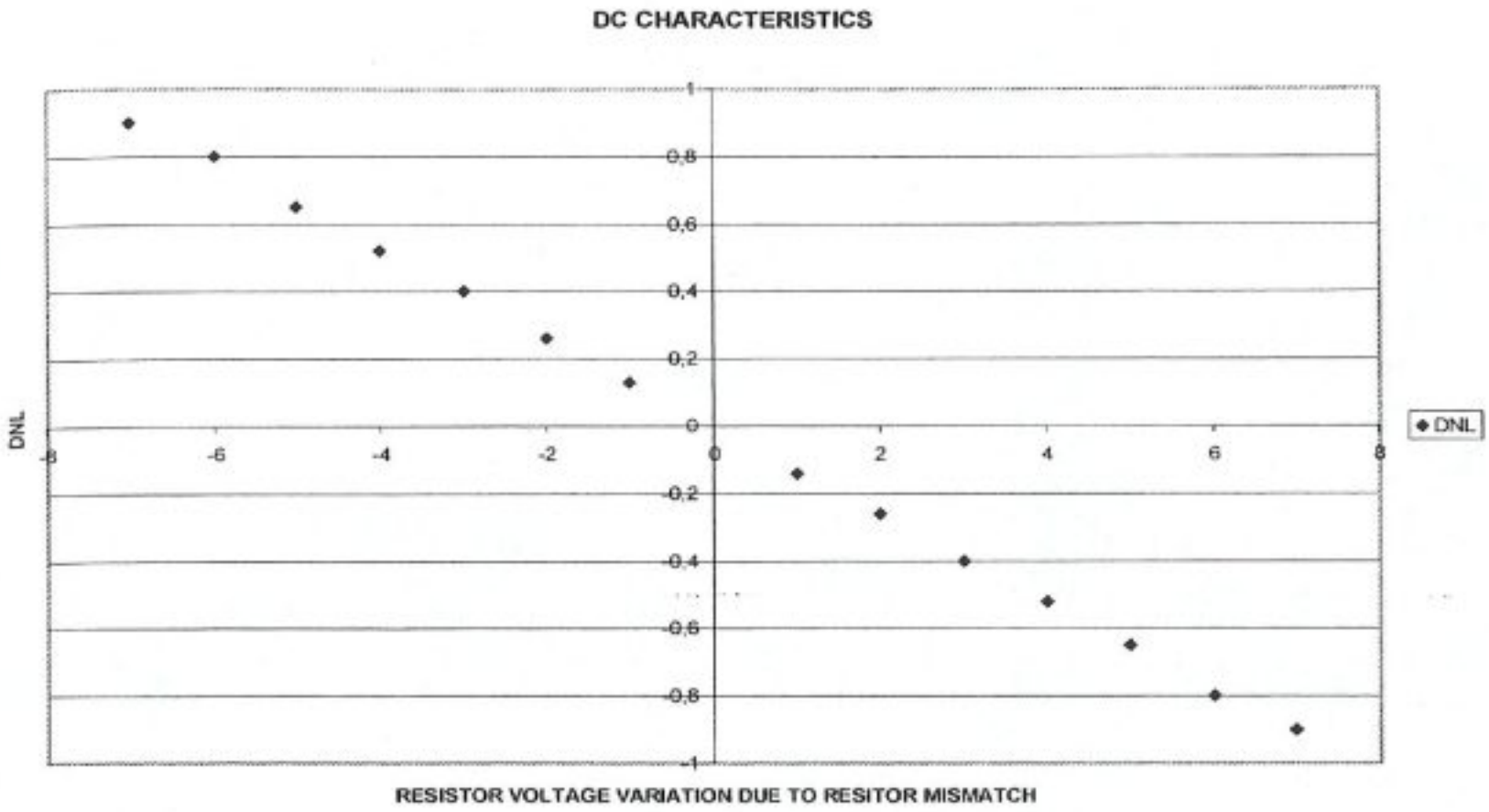


Figure 3.18 DNL envelope obtained for different resistor voltage variations.

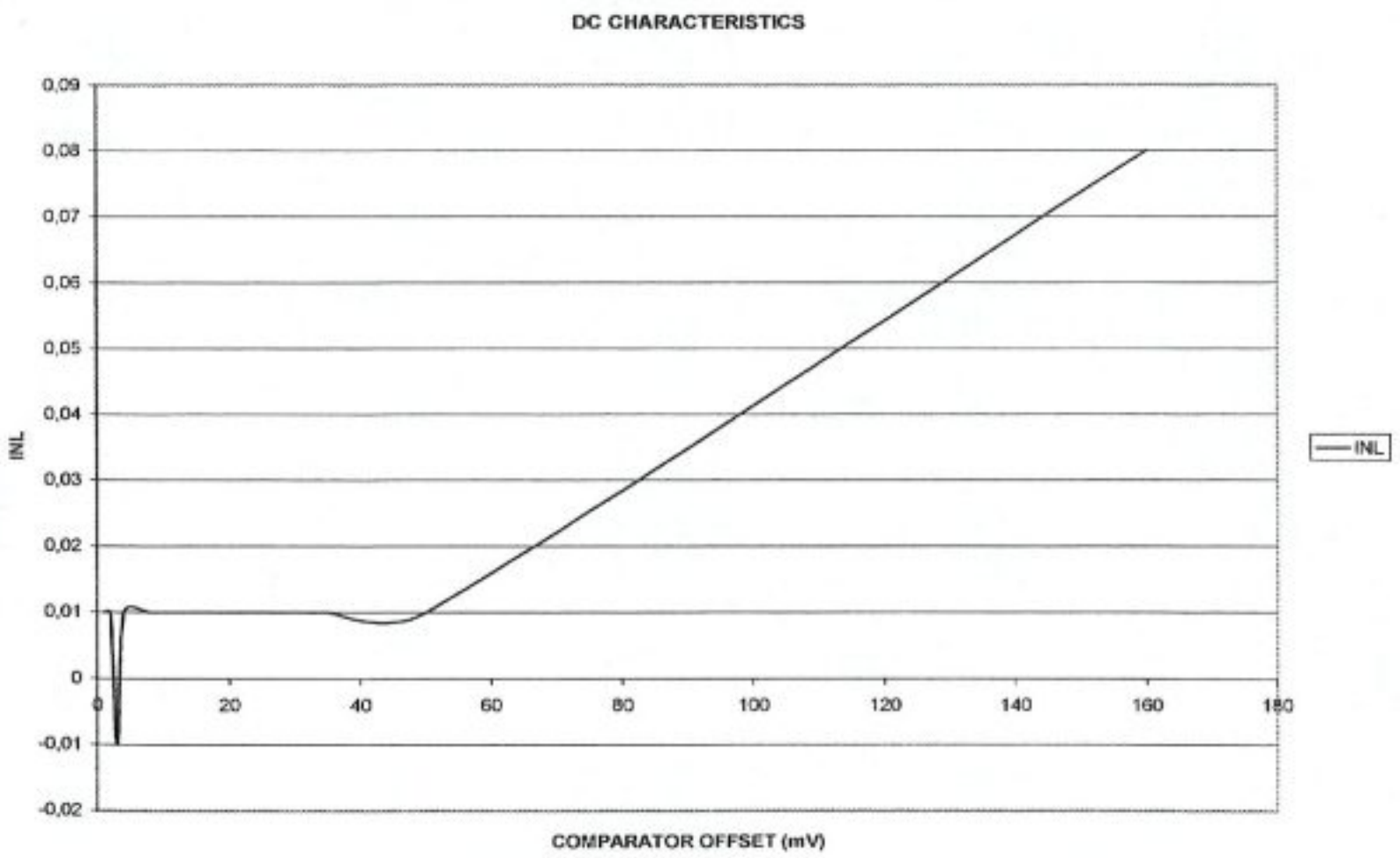


Figure 3.19 INL envelope obtained for different comparator offsets.

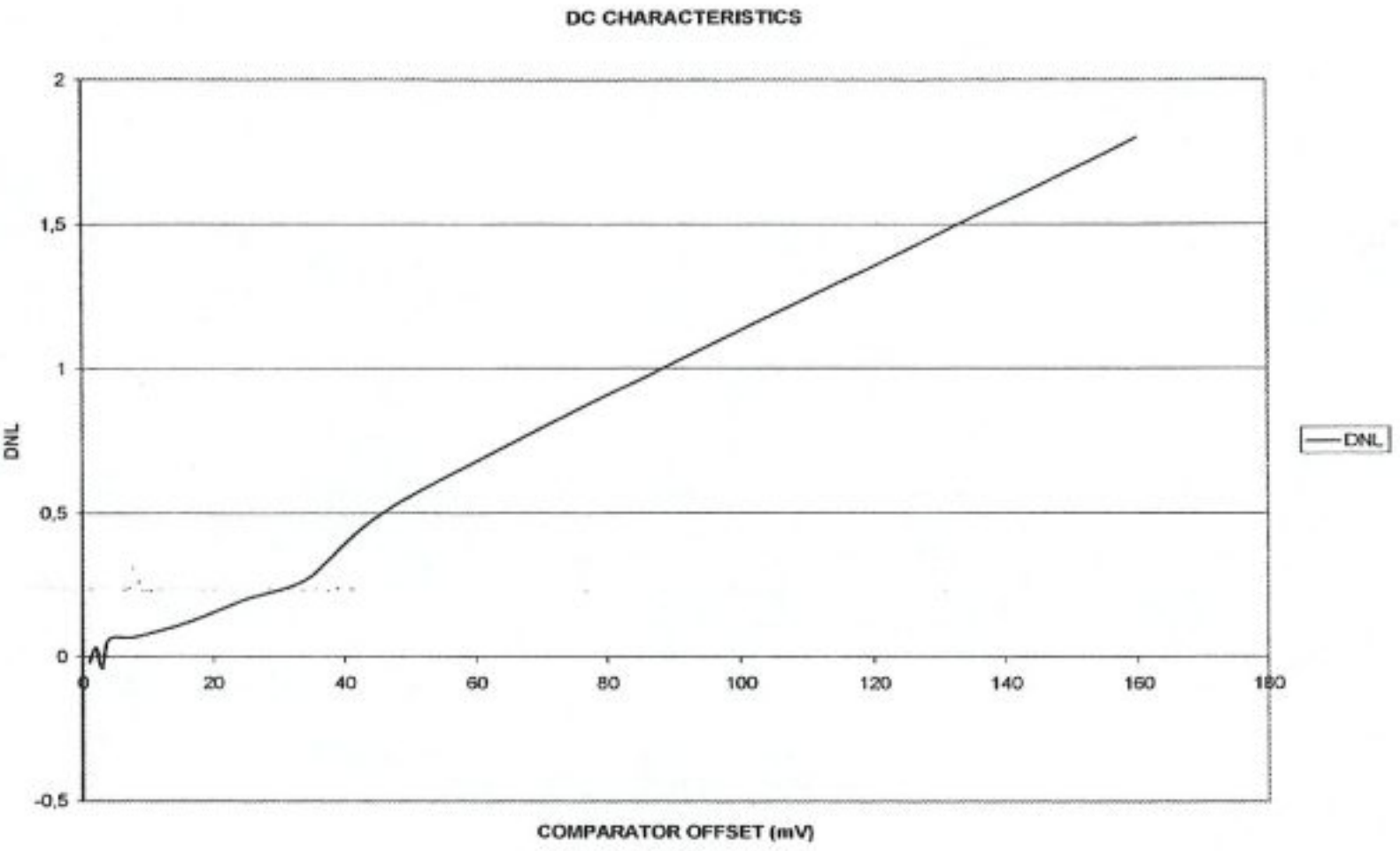


Figure 3.20 DNL envelope obtained for different comparator offsets.

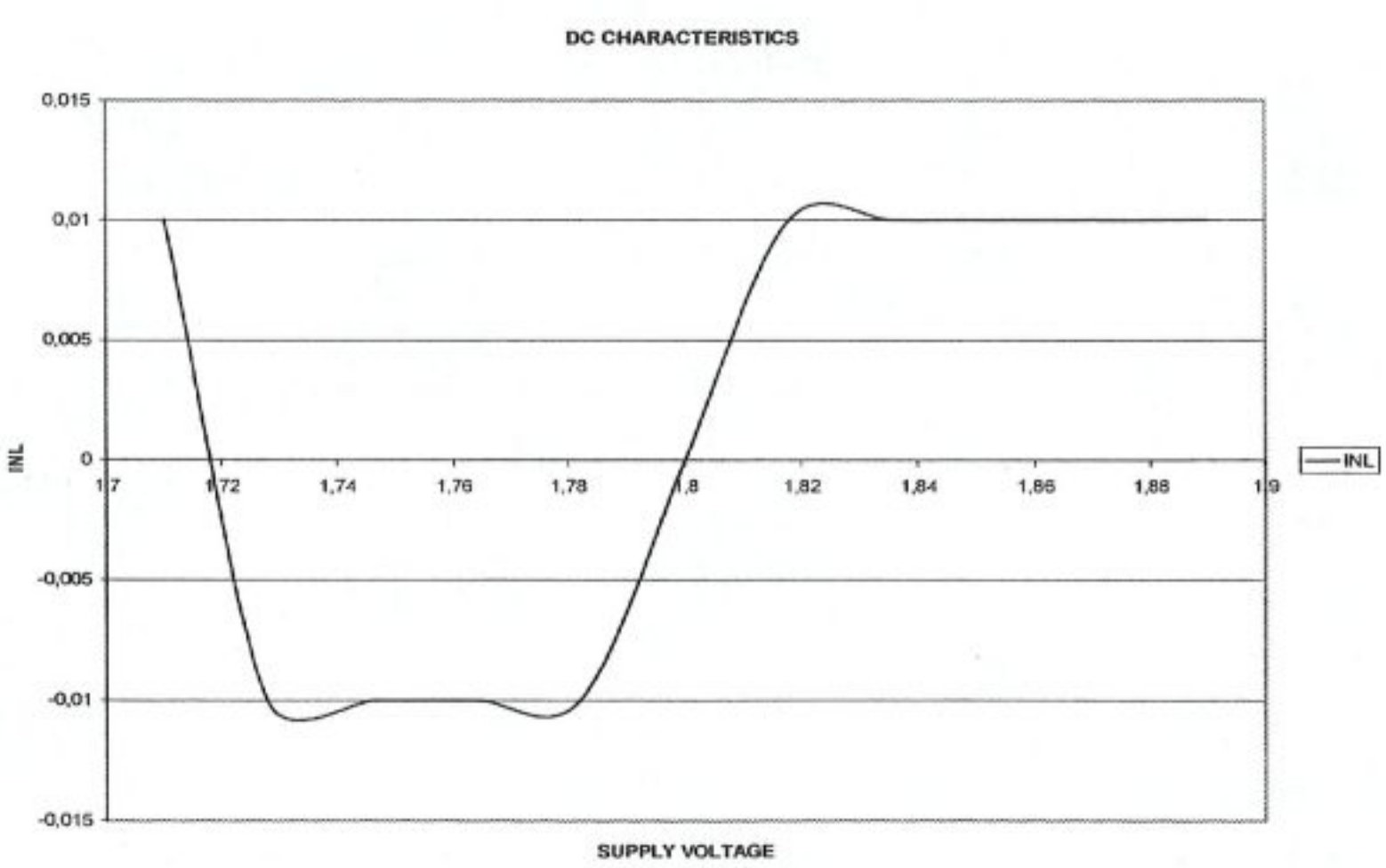


Figure 3.21 INL envelope obtained for different supply voltage variations.

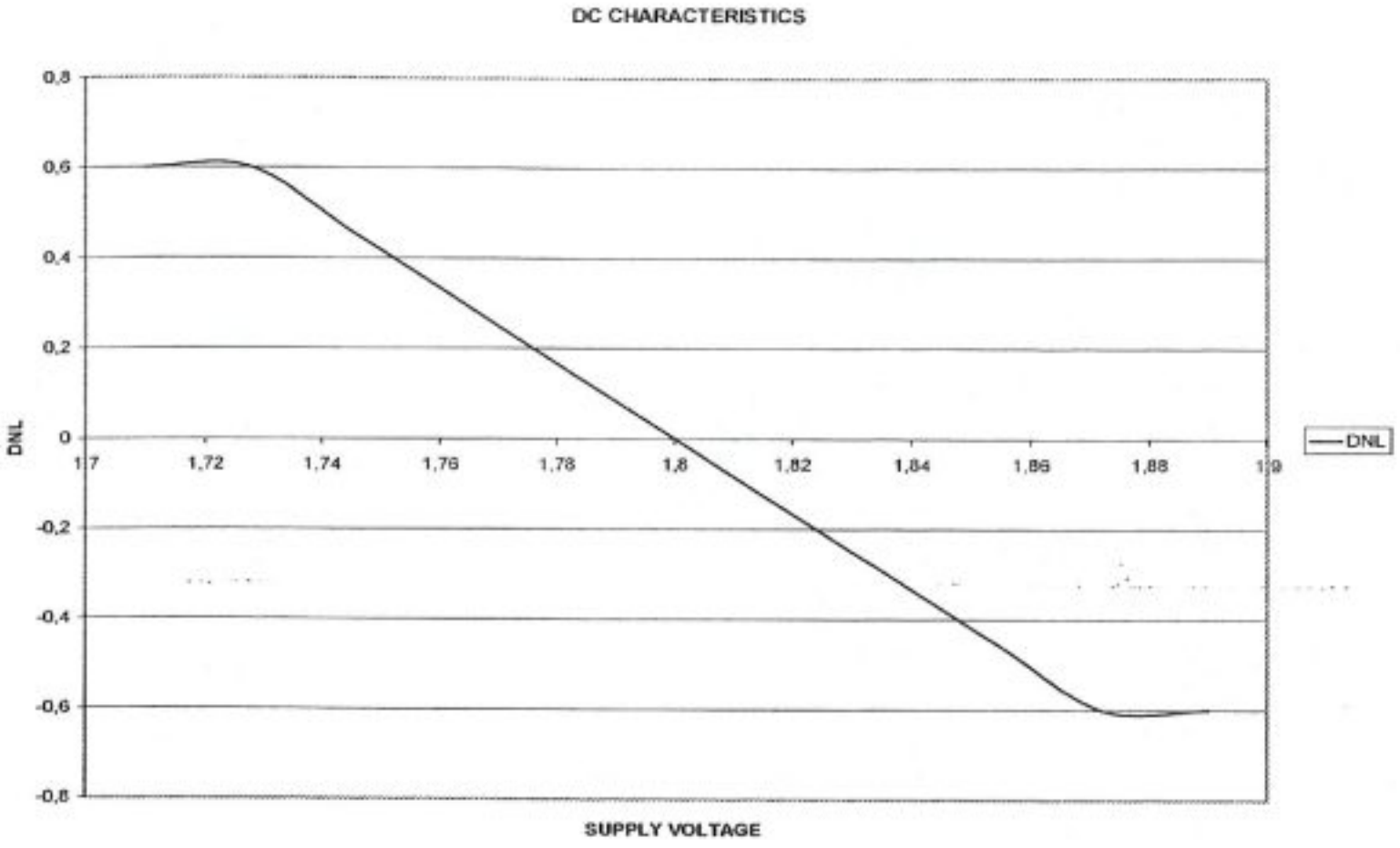


Figure 3.22 DNL envelope obtained for different supply voltage variations.

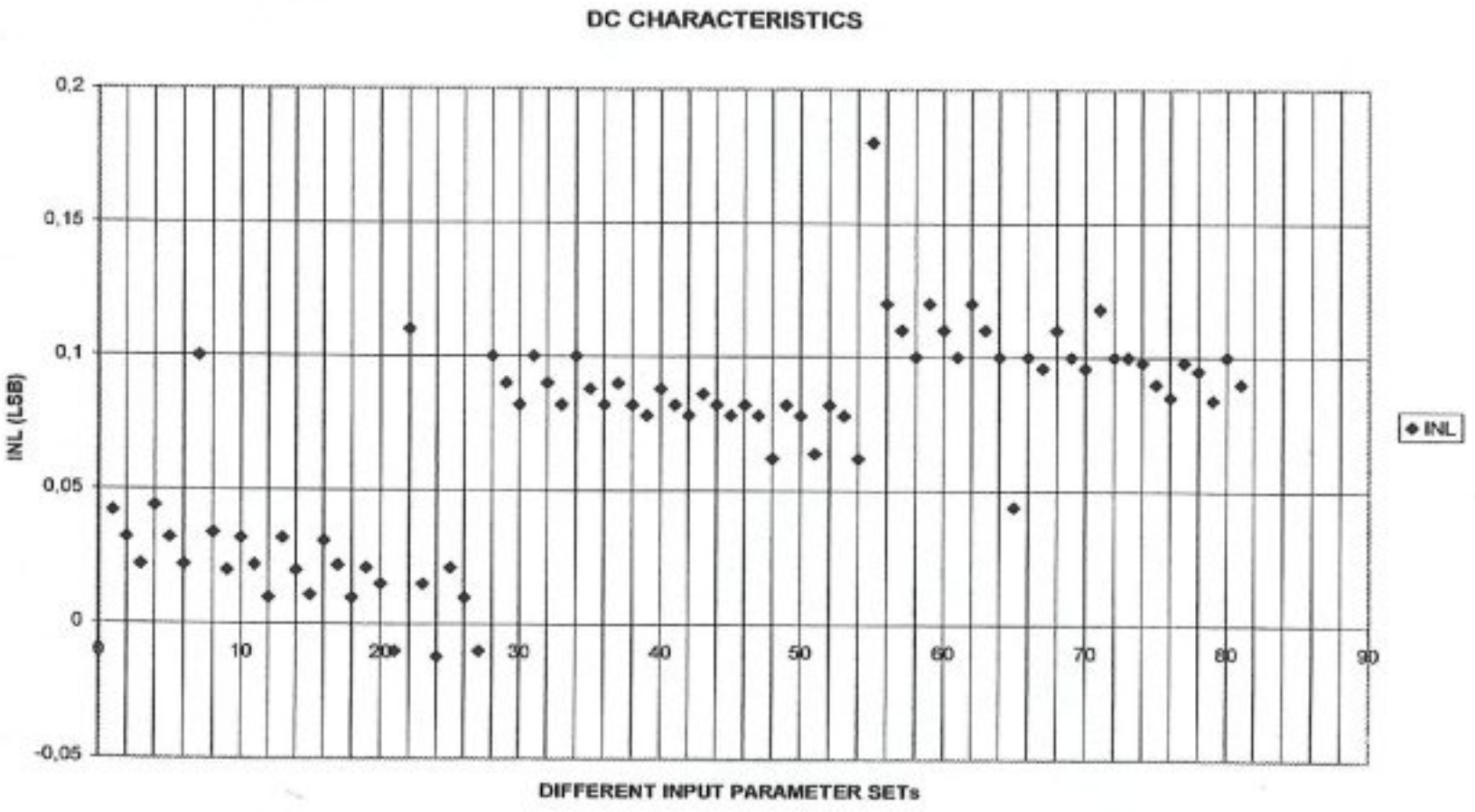


Figure 3.23 INL envelope obtained for combined parameter set simulations.

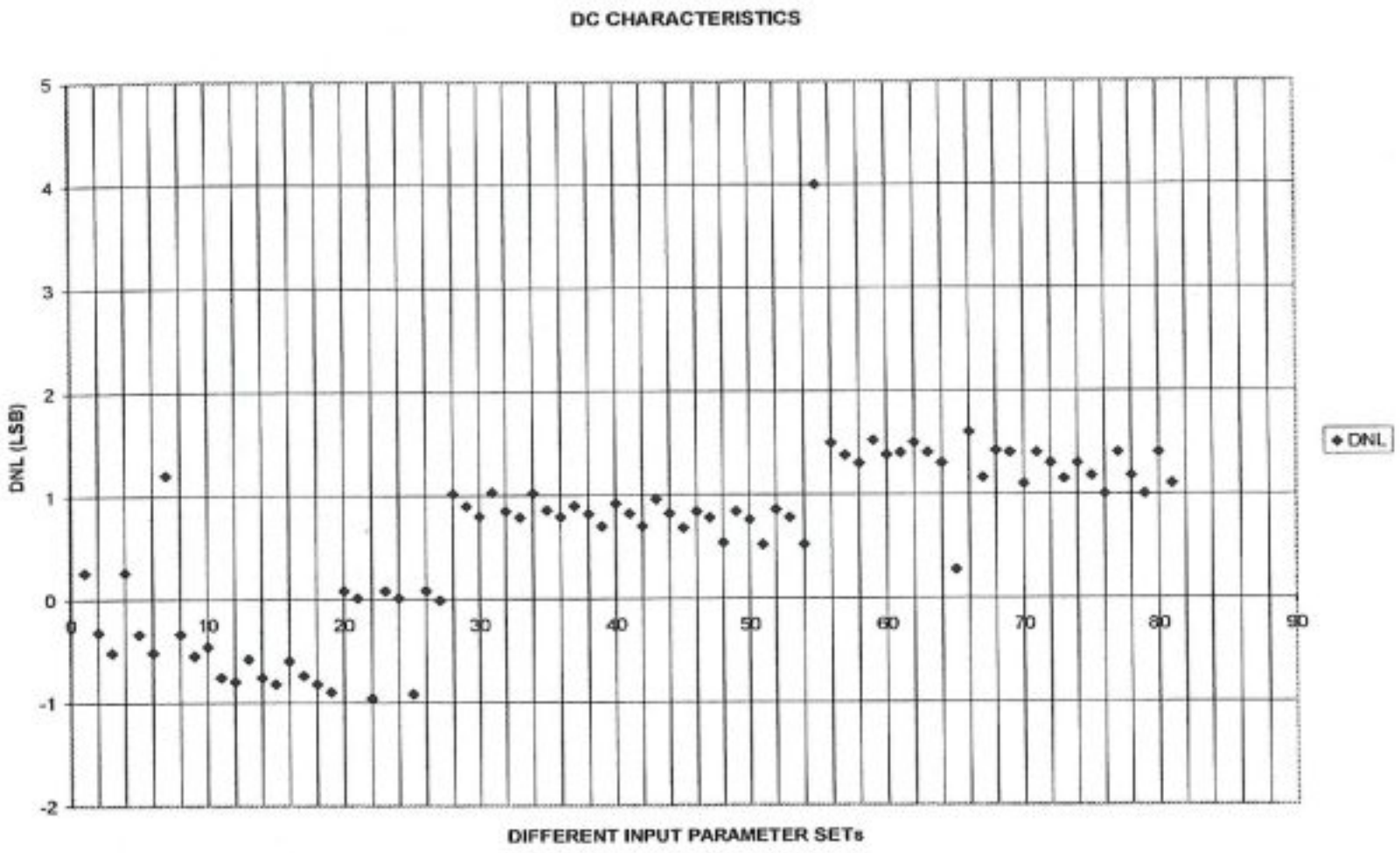


Figure 3.24 DNL envelope obtained for combined parameter set simulations.

4. ARCHITECTURE COMPONENTS: VOLTAGE COMPARATOR DESIGN

4.1 Pipelined ADC Architecture Overview

Based on the observations outlined in Chapter 3, we propose a Pipelined A/D converter that is formed by four stages of 4-bit Flash A/D converters, followed by the corresponding D/A converters, subtraction circuits and residue amplifiers (Fig. 4.1). Brief design specifications of the proposed Analog-to-Digital converter are given in Table 4.1.

- Architecture : Pipelined (4 stages)
- Sampling Rate : 200 MS/s
- Resolution : 12 bits (4-bits per stage)
- Technology : 0.18 μm CMOS, 1.8V technology.
- Power dissipation : <100mW
- Die size : <10-15 mm^2

Table 4.1 Design specifications of proposed pipelined A/D converter.

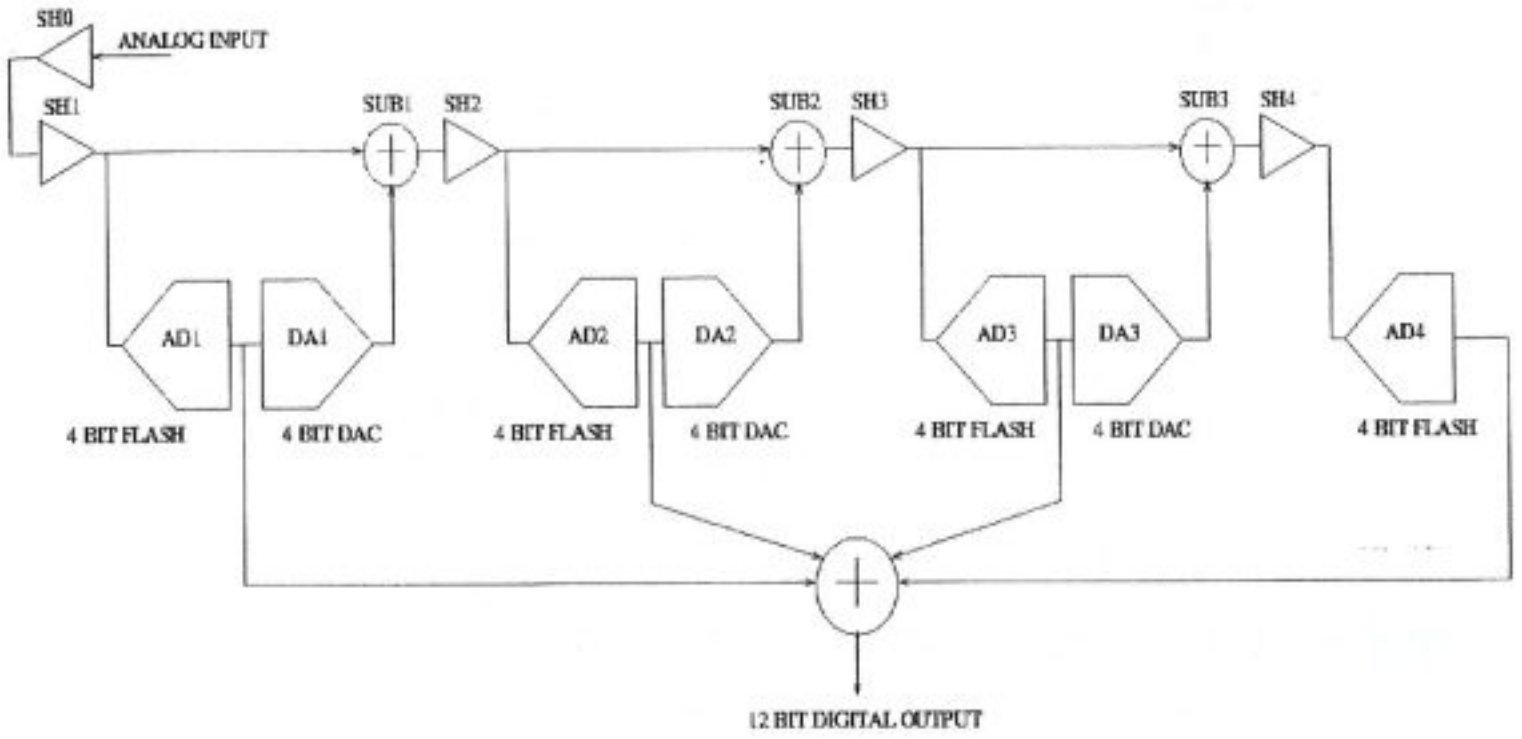


Figure 4.1 Simplified block diagram of the proposed A/D converter architecture.

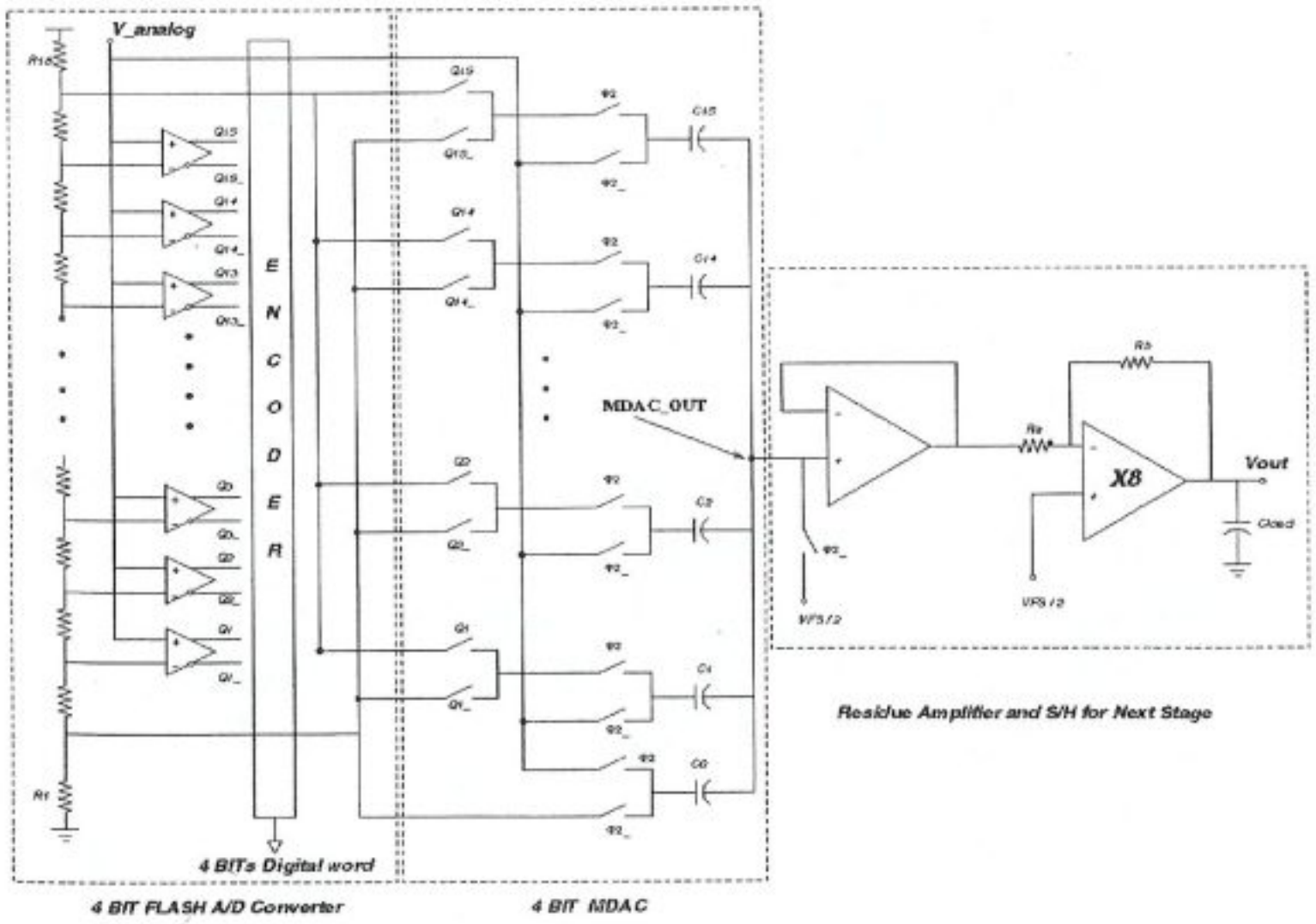


Figure 4.2 Detailed circuit architecture for one of the four proposed pipelined stages.

The detailed circuit architecture of one of the proposed pipeline stages is shown in Fig. 4.2. The 4-bit flash ADC consists of a resistor chain to generate the reference voltages, followed by an array of voltage comparators. The outputs of the comparators are fed directly into a capacitive MDAC (Multiplying DAC) that simultaneously performs the subtraction of the re-constructed digital output from the original analog signal, as well as the amplification of the residue signal voltage for further processing by the next pipeline stage. Note that single-ended signals (as opposed to differential) are used in the entire circuit architecture. In the following, we will investigate the design of the main components of this architecture, starting with the voltage comparator.

4.2 Voltage Comparators: Basic Concepts

The most important component in flash A/D converters is the voltage comparator. The comparator is a circuit that compares an analog signal with another analog signal, and outputs a binary signal based upon the comparison. What is meant here by an analog signal is one that can have any value of a continuous range of amplitude values at a given point in time. In the most strictt sense a binary signal can have only one of the two given values at any point in time, but this concept of a binary signal is too ideal for real world situations, where there is a transition region between the two binary states.

The realization of high-speed, high-precision voltage comparators is one of the key issues in the design of data conversion systems. Traditionally, the main trade-off is between speed and accuracy, where device mismatch effects tend to limit the achievable accuracy in high-speed configurations. Silicon area and power dissipation are also among the main concerns. In addition, the complexity of the clocking schemes used in high-sped comparators can easily be one of the limiting factors in system design.

The widespread dominance of low-voltage digital CMOS process in mixed-signal IC design implies that high-performance analog circuit blocks such as voltage comparators must be designed with the restriction of a single, relatively low power supply voltage. Also, on chip noise considerations introduce the need to utilize an increasing percentage of the available power supply range as the input dynamic range. Consequently, the design of high-speed low voltage comparators becomes a serious challenge.

4.2.1 Model of a Voltage Comparator

Figure 4.3 shows the circuit symbol for a comparator. This symbol is similar to that of an operational amplifier, because a comparator has many of the same characteristics as a high-gain amplifier. A comparator was defined in the introduction as a circuit that has a comparison of two analog inputs. This is illustrated in Figure 4.4. As shown in this figure the output of the comparator is high (V_{OH}) when the difference between the non-inverting and inverting inputs is positive and low (V_{OL}) when this difference is negative.

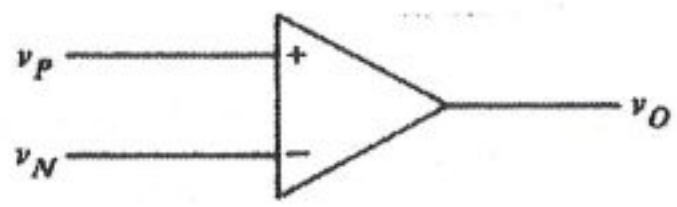


Figure 4.3 Circuit symbol for a comparator [3].

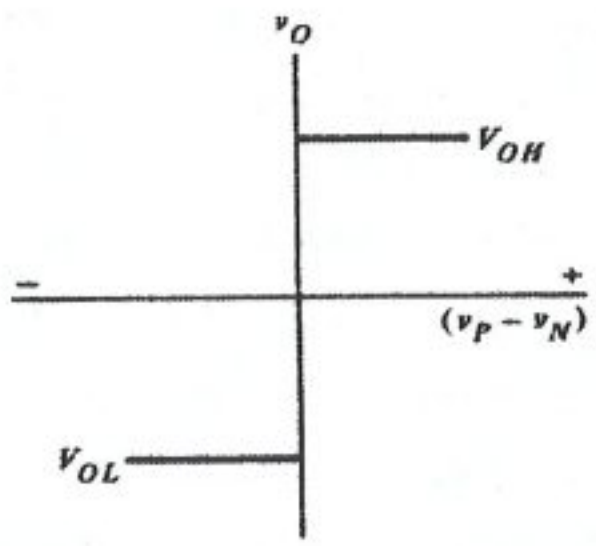


Figure 4.4 Zero-order transfer curve of a comparator [3].

Even though this type of behavior is impossible in a real-world situation, it can be modeled with ideal circuit elements with mathematical descriptions. One such circuit model is shown in Figure 4.5. It comprises a non-linear voltage-controlled-voltage source (VCVS) whose characteristics are described by the mathematical formulation given on the figure.

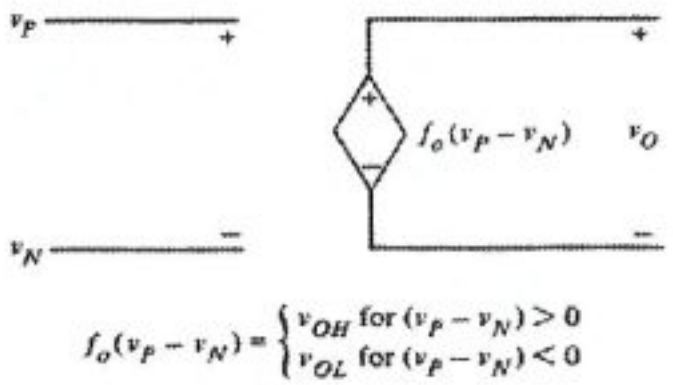


Figure 4.5 Zero-order model for a comparator [3].

The ideal aspect of this model is the way in which the output makes a transition between V_{OL} and V_{OH}. The output changes states for an input change of ΔV, where ΔV approaches to zero. This implies a gain of infinity, as shown below

$$Gain = A_v = \lim_{\Delta V \to 0} \frac{V_{OH} - V_{OL}}{\Delta V} \tag{4.1}$$

Figure 4.6 shows the DC transfer curve of a first-order model that is an approximation to a realizable comparator circuit. The difference between this model and the previous one is the gain, which can be expressed as

$$A_v = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}} \tag{4.2}$$

where V_{IH} and V_{IL} represent the input-voltage difference v_P-v_N needed to just saturate the output at its upper and lower limit respectively.

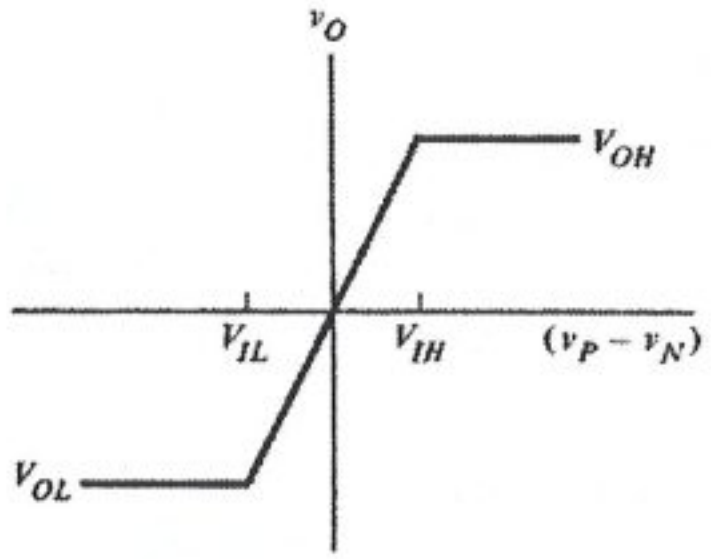
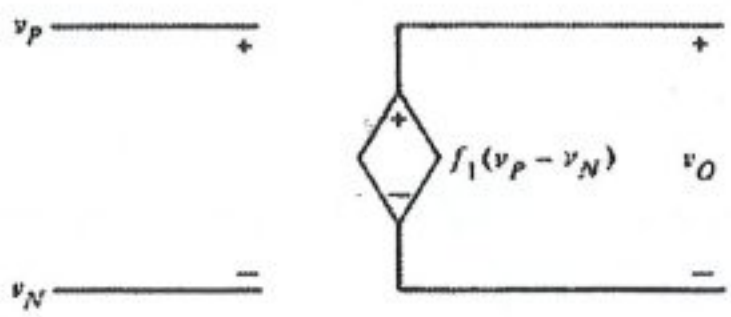


Figure 4.6 First-order transfer curve of a comparator [3].

Gain is a very important characteristic describing comparator operation, for it defines the minimum amount of input charge necessary to make the output swing between the two binary states. The voltages V_{OH} and V_{OL} must be adequate to meet the V_{IH} and V_{IL} requirements of the following digital state.

The transfer curve of Figure 4.6 is modeled by the circuit of Figure 4.7. This model looks similar to the one for zero-order model, the only difference being the functions f_1 and f_0. The second non-ideal effect seen in comparator circuits is input-offset voltage. In Figure 4.4, the output changes as the input crosses zero. If the output does not change until the input difference reaches a value $+V_{OS}$, then this difference would be defined as the offset voltage (Figure 4.8). The corresponding equivalent circuit model of a comparator with input offset is shown in Figure 4.9 [3].



$$f_1(v_P - v_N) = \begin{cases} V_{OH} \text{ for } (v_P - v_N) > V_{IH} \\ A_1(v_P - v_N) \text{ for } V_{IL} < (v_P - v_N) < V_{IH} \\ V_{OL} \text{ for } (v_P - v_N) < V_{IL} \end{cases}$$

Figure 4.7 First-order model of comparator [3].

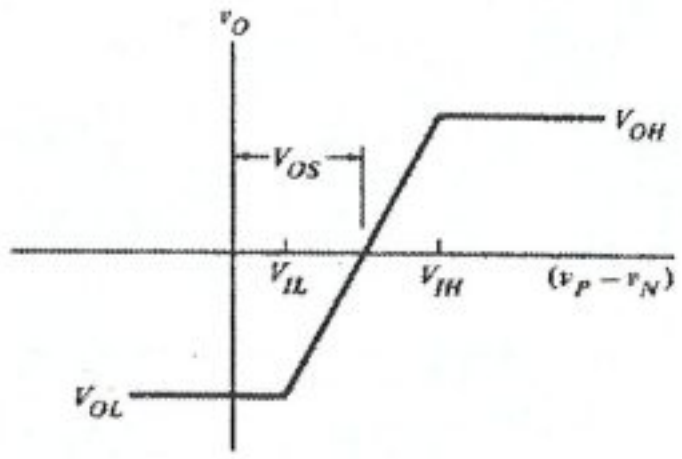


Figure 4.8 First-order transfer curve of a comparator including offset [3].

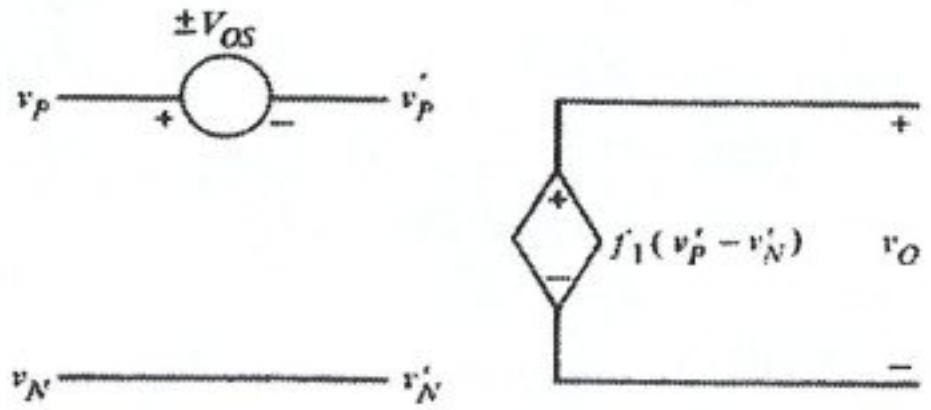


Figure 4.9 First-order model of a comparator including offset. The ± sign of the offset voltage accounts for the fact that V_{OS} is unknown in polarity [3].

Up to this point in our discussion we have considered only the DC model for a comparator. This model includes the parameters of gain, amplitude saturation and offset voltage. The comparator must also be modeled in the time domain. Figure 4.4 and Figure 4.6 show that the output of the comparator changes from one state to another for a given amount of differential output. The point of question is, how long it takes for the comparator to respond to the given differential input. The characteristic delay between input excitation and output transition is the time response of the comparator. Figure 4.10

illustrates the response of a comparator to an input as a function of time. Notice that there is a delay between the input excitation and the output response.

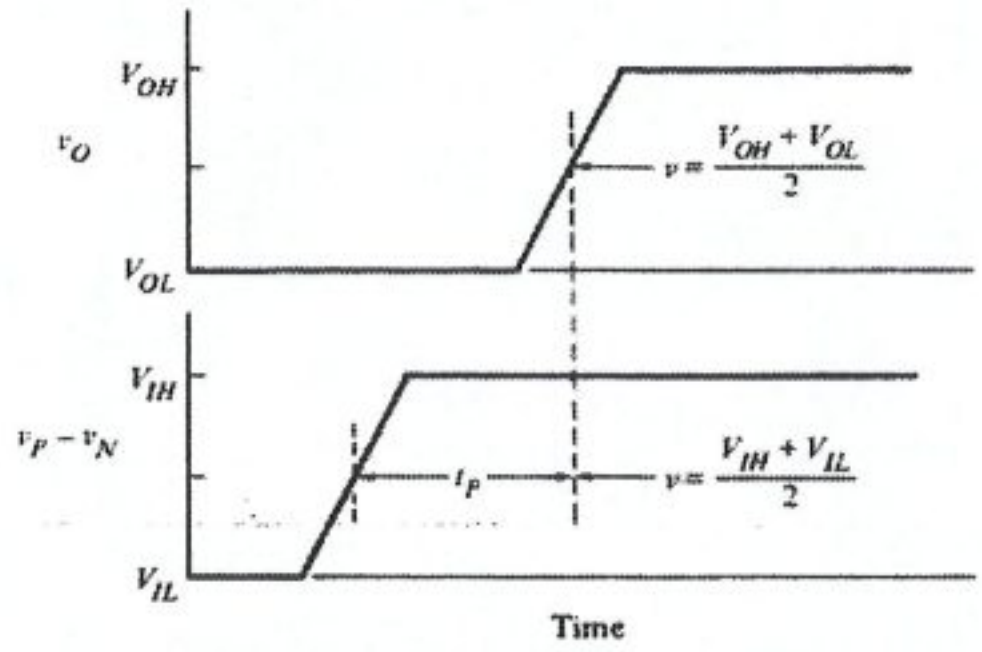


Figure 4.10 Time domain response of a non-inverting first-order comparator [3].

This time difference is called the propagation delay of the comparator. It's a very important parameter since it's often the speed limitation in the conversion rate of an A/D converter. The propagation delay in comparators usually varies as a function of the amplitude of the input. A larger input will result in a smaller delay time. There is an upper limit at which a further increase in the input voltage will no longer affect the delay.

Perhaps the major limitation on the resolution of comparators is due to charge injection, also commonly called clock feed through. This error is due to unwanted charges being injected into the circuit when transistors turn-off. When MOS switches are on, they operate in the triode region and have zero volts between their drain and source terminals. When MOS switches turn-off, charge errors occur by two mechanisms. The first is due to the channel charge, which must flow out from the channel region of the transistor to the drain and the source junctions. The channel charge of a transistor that has zero V_{DS} is given by,

$$Q_{CH} = WLC_{ox}V_{eff} = WLC_{ox}(V_{GS} - V_T) \tag{4.3}$$

This charge often dominates the second charge (typically smaller, unless V_{eff} is very small) which is due to the overlap capacitance between the gate and the junctions.

4.2.2 Examples of CMOS Comparator Circuits

This section describes a number of high-speed comparators that are preferred in flash ADC circuit structures.

One of the simplest circuits available in CMOS technology that can function as a comparator is the current-sink inverter given in Figure 4.11.

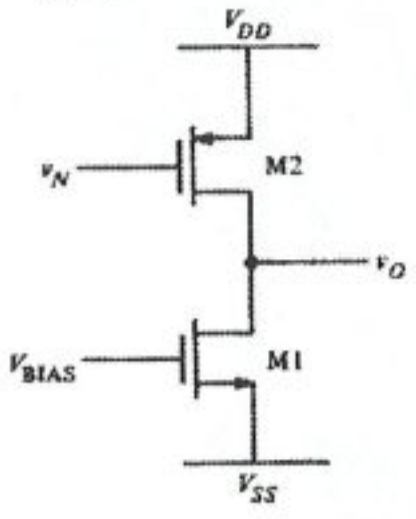


Figure 4.11 Current-sink inverter functioning as a comparator [3].

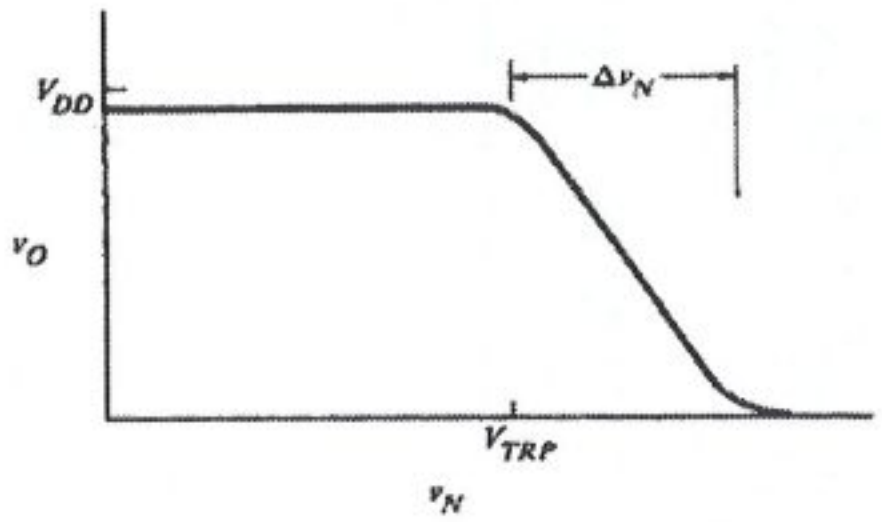


Figure 4.12 DC transfer curve of simple comparator [3].

The transfer curve of this inverter is shown in Figure 4.12. The input voltage range of the comparator is approximately determined by the gain of the comparator. The larger

the gain, the smaller the input-voltage drive requirements. The major drawback of this circuit is not gain, however, but the fact that the trip point is dependent upon power supply. In addition, there is a limited range at which the trip point can be placed, while still maintaining adequate gain. All these problems can be solved by using a differential input scheme.

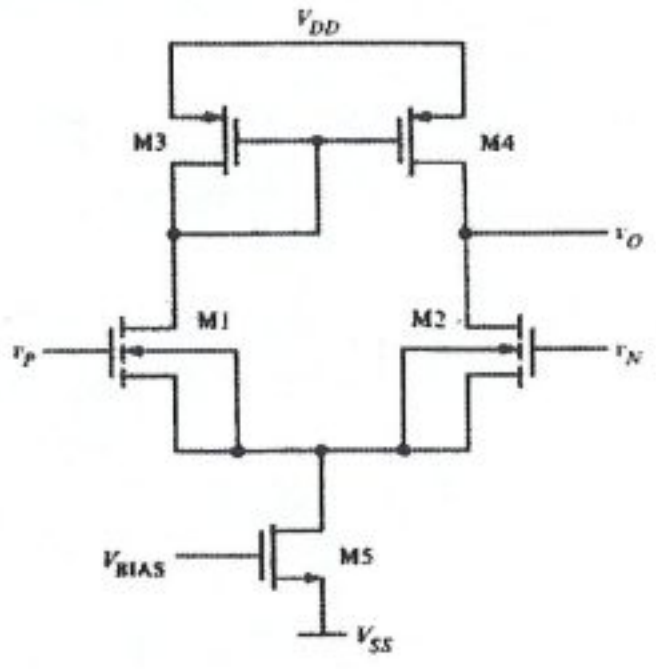


Figure 4.13 Differential voltage comparator schematic [3].

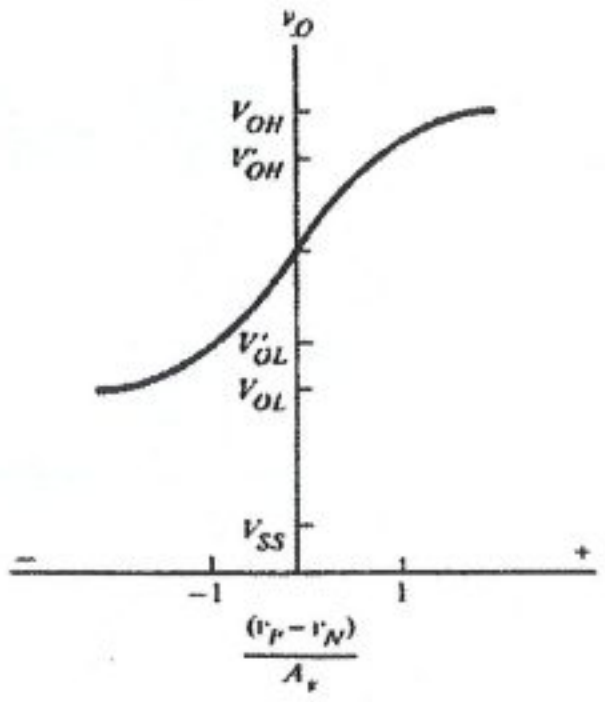


Figure 4.14 DC transfer curve of a differential voltage comparator [3].

Figure 4.13 shows the differential amplifier stage with n-channel input devices and a single ended output stage. The key attribute of this circuit is its ability to amplify the difference between the inverting and non-inverting inputs. As a result the trip-point of a comparator can be made independent of process and supply variation to the first order. The major drawback of using the differential stage alone as a comparator is the limited output range, which would probably not be useful for driving digital circuitry. The limit of the output swing range is given in Eq. 4.4. Also the limited gain of this single stage is one of the problems.

$$V'_{OL} \cong V_P - V_{TM1}$$

$$V'_{OH} = V_{DD} - \left[\frac{I_5}{K'_3\left(W_3/L_3\right)}\right]^{1/2} \tag{4.4}$$

Thus far, two circuit techniques to implement the comparator function have been presented. However, neither of the presented circuits performs the comparator function satisfactorily by itself. But, although these two circuits do not perform well alone; they can have satisfactory performance if they are combined. Figure 4.15 shows the circuit diagram of a two-stage comparator.

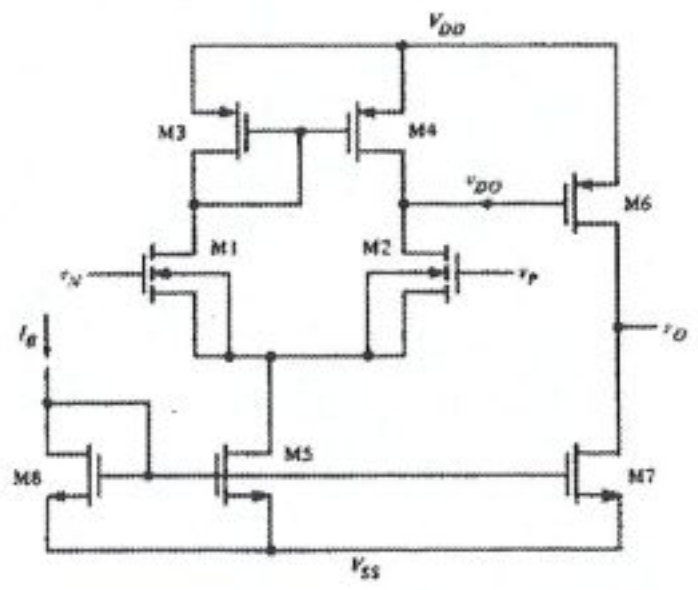


Figure 4.15 Two-stage voltage comparator [3].

The poor gain of the differential stage is augmented by the gain of the inverting stage. The output of the differential stage that lies closest to V_{DD} is in the vicinity of the trip-point of the inverting stage that follows. Therefore the limited output range, which is a problem for the differential stage by itself, now becomes a good feature in the combination shown. In Figure 4.15 the total offset seen at the input of the comparator is due to the second-stage offset rectified to the input and added to the offset in the first-stage. There also exists some error in the output resulting from the current mismatches. This error is then reflected back to the input as a systematic offset.

Often a comparator is placed in a very noisy environment in which it must detect signal transitions at the threshold point. Specifically, hysteresis may be needed in the comparator. Hysteresis is the quality of the comparator in which the input threshold changes as a function of the input (or output) level. In particular, when the input passes the threshold, the output changes and the input threshold is subsequently reduced so that the input must return beyond the previous threshold before the comparator's output changes state again.

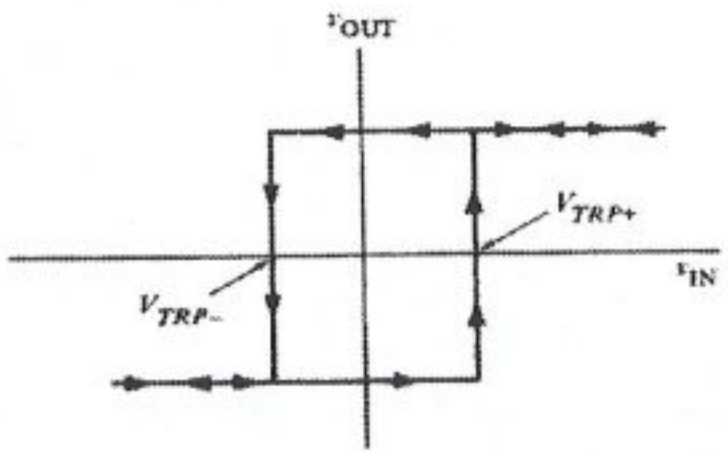


Figure 4.16 Comparator hysteresis curve [3].

The output uncertainty of the comparator can be minimized by adding hysteresis equal to or greater than the amount of the largest expected noise amplitude.

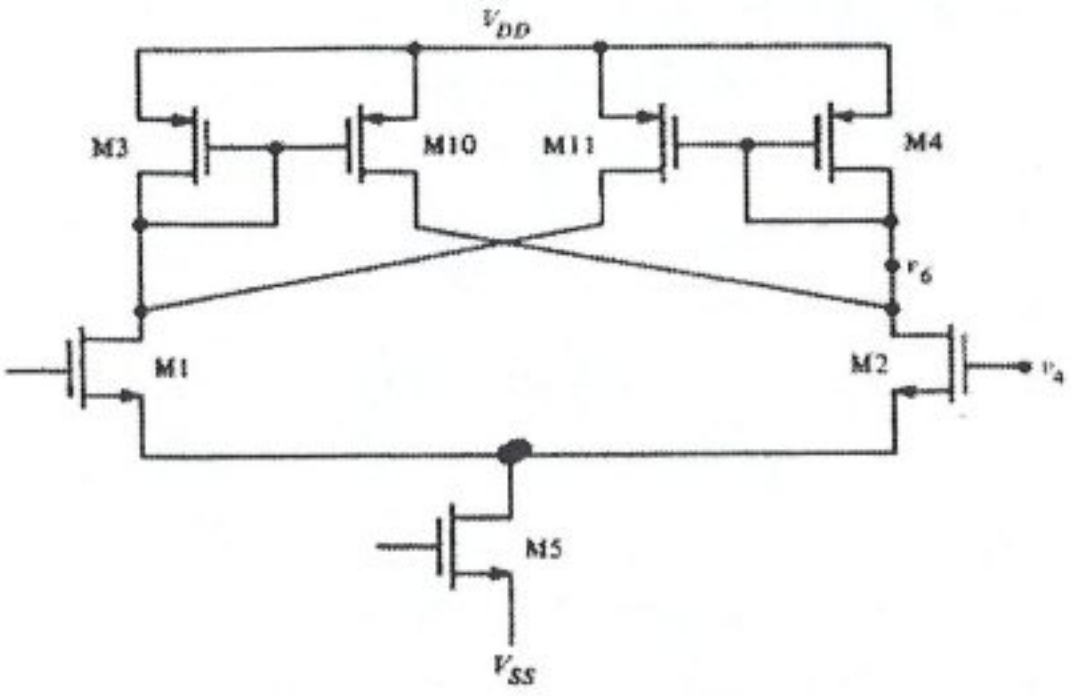


Figure 4.17 Comparator with hysteresis applied to the input differential stage only [3].

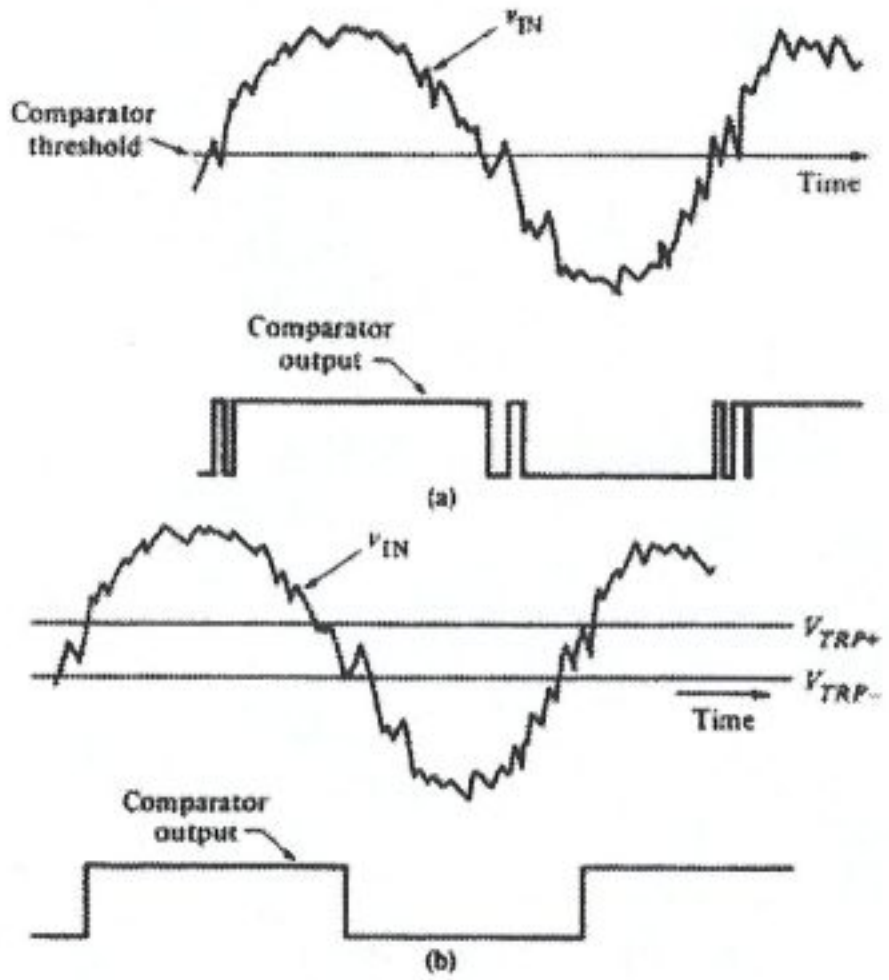


Figure 4.18 (a) Comparator response to a noisy input. (b) Comparator response to noisy input when hysteresis is added [3].

In this circuit there are two paths of feedback. The first is current-series feedback through the common source node of transistors M1 and M2. This feedback path is

negative. The second path is the voltage-shunt feedback through the gate-drain connections of transistors M10 and M11. This path of feedback is positive. If the positive feedback factor is less than the negative feedback factor, then the overall feedback will be negative and no hysteresis will result. If the positive feedback factor becomes greater, the overall feedback will be positive, which will give rise to hysterresis in the voltage transfer curve. As long as the ratio β_{10} / β_3 is less than one, there is no hysteresis in the transfer function. When this ratio is greater than one, hysteresis will result [3].

Input-offset voltage can be a particularly difficult problem in comparator design. Offset cancellation techniques are available in MOS technology because of the nearly infinite input resistance of MOS transistors. This characteristic allows long-term storage of voltages on the transistor's gate. As a result, offset voltages can be measured, stored on capacitors, and summed with the input so as to cancel the offset.

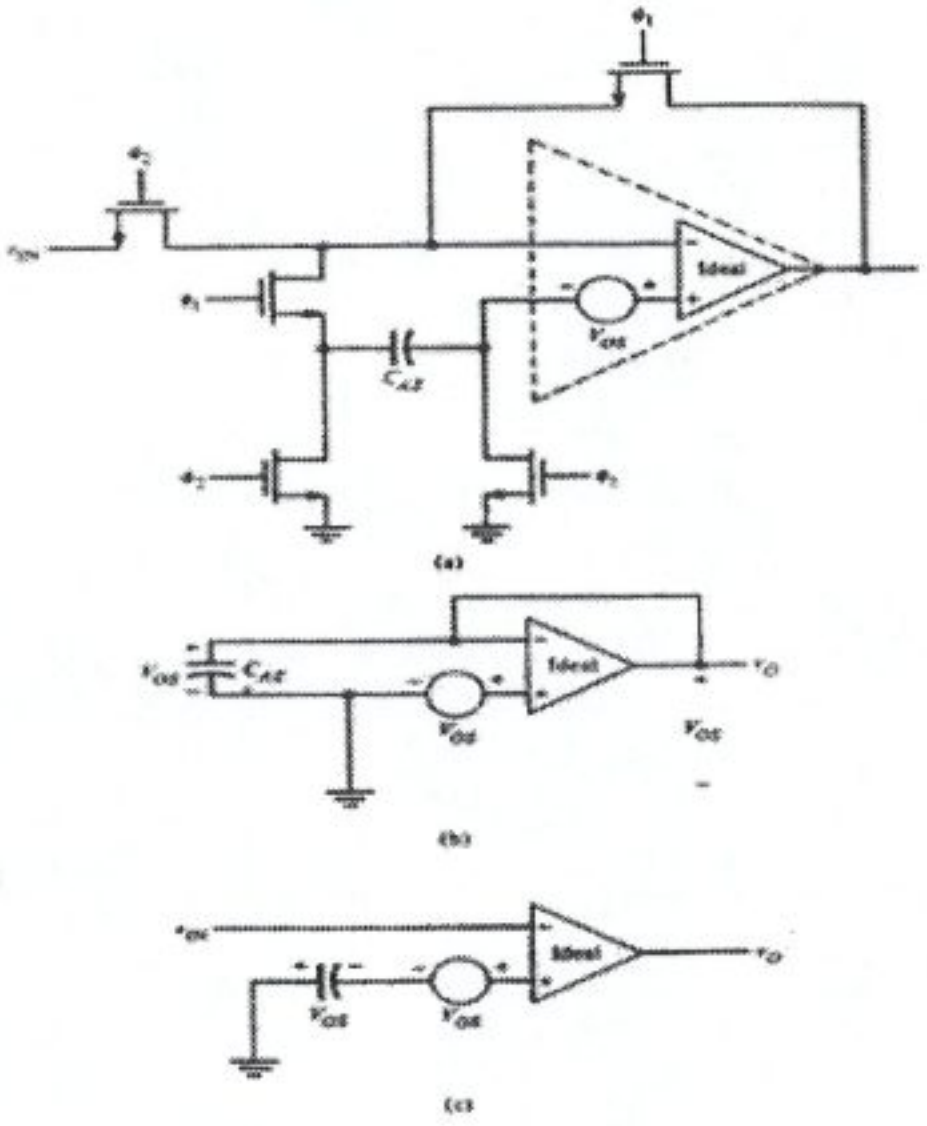


Figure 4.19 (a) Circuit implementation of an auto-zeroed comparator. (b) Comparator during ϕ_1 auto-zero state. (c) Comparator during ϕ_2 state [3].

One possible implementation of an auto-zeroed comparator is shown in Figure 4.19. In order for this circuit to work properly, it is necessary that the comparator be stable in the unity-gain configuration. NMOS switches were drawn instead of CMOS transmission gates for the sake of simplicity. It is also very important to use non-overlapping clocks to drive the switches so that any given switch turns-off before another turns-on. Auto-zero techniques can be very effective in removing a large amount of comparator's input offset, but the offset cancellation is not perfect. Charge injection resulting from clock feed trough can by itself introduce an offset.

The literature on integrated circuit technology has many examples of latched comparators, such as the example shown in Figure 4.20. This comparator has the positive feedback of the second stage always enabled. In track mode, when two diode-connected transistors of the gain stage are enabled, the gain around the positive feedback loop is less than one, and the circuit is stable. The combination of the diode-connected transistors of the gain stage and the transistors of the positive feedback loop acts as a moderately large impedance and gives gain from the preamplifier stage to the track-and-latch stage. The diode-connected loads of the preamplifier stage give a limited amount of gain in order to maximize speed, while still buffering the kickback from the input circuitry.

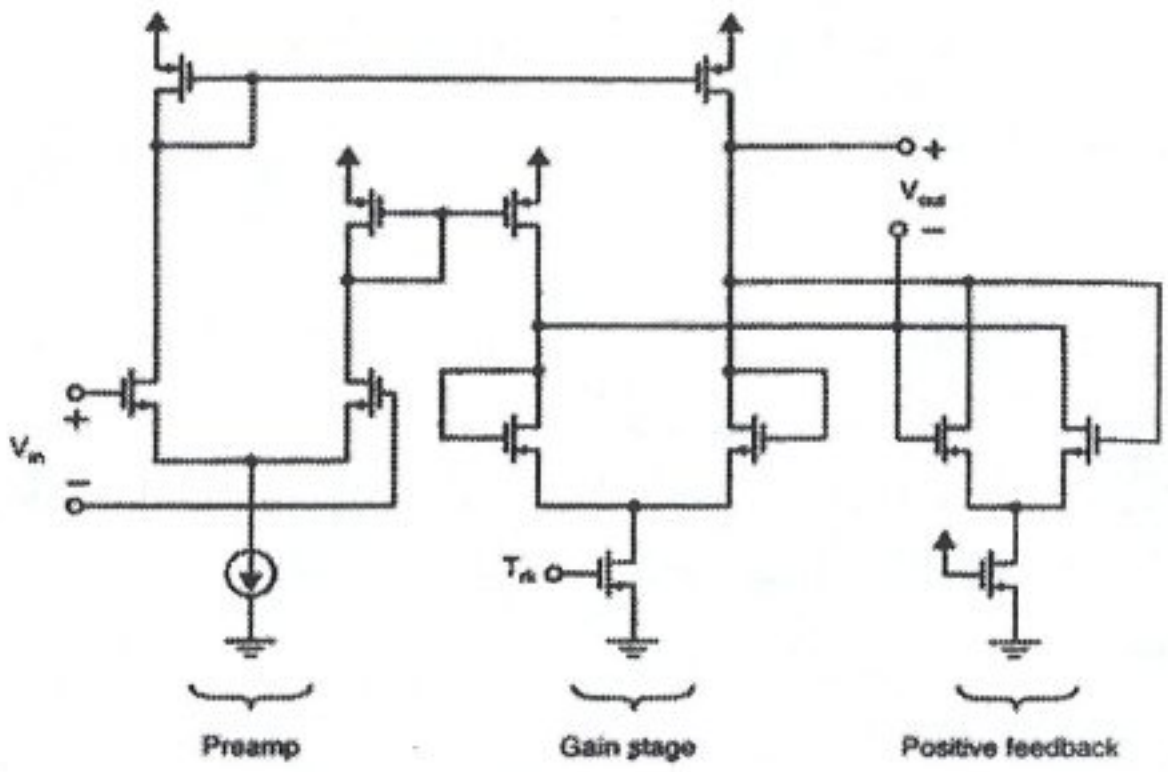


Figure 4.20 A two-stage comparator that has a preamplifier and a positive-feedback track-and-latch stage [2].

A second comparator shown in Figure 4.21, also uses diode-connected loads to keep all nodes at relatively low impedance (similar to current-mode circuit design techniques), thereby keeping all node time constants small and resulting in fast operation. This design also uses precharging to eliminate any memory from the previous decision. For example, the positive-feedback stage is precharged low, whereas the digital-restoration stage is precharged high, somewhat similar to what is done in Domino CMOS Logic.

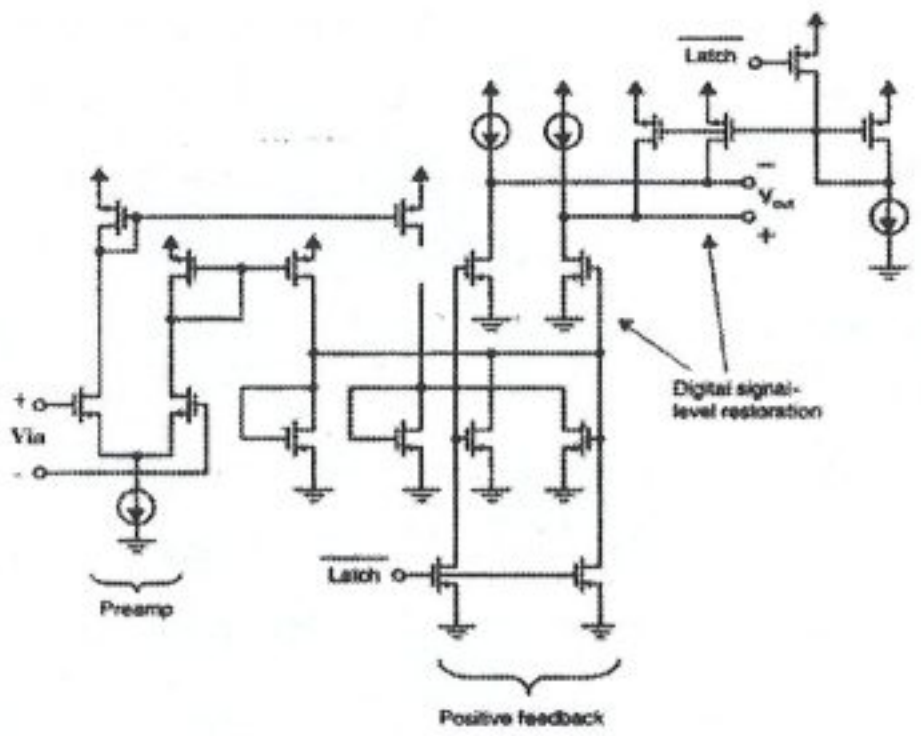


Figure 4.21 A two-stage comparator [2].

A third comparator is shown in Figure 4.22, with appropriate wave forms given in Figure 4.23. This design eliminates any input-offset voltages from both the first and second stages by using capacitive coupling. It also has common-mode feedback circuitry for the first preamplifier stage, which allows for input signals that have large common-mode signals.

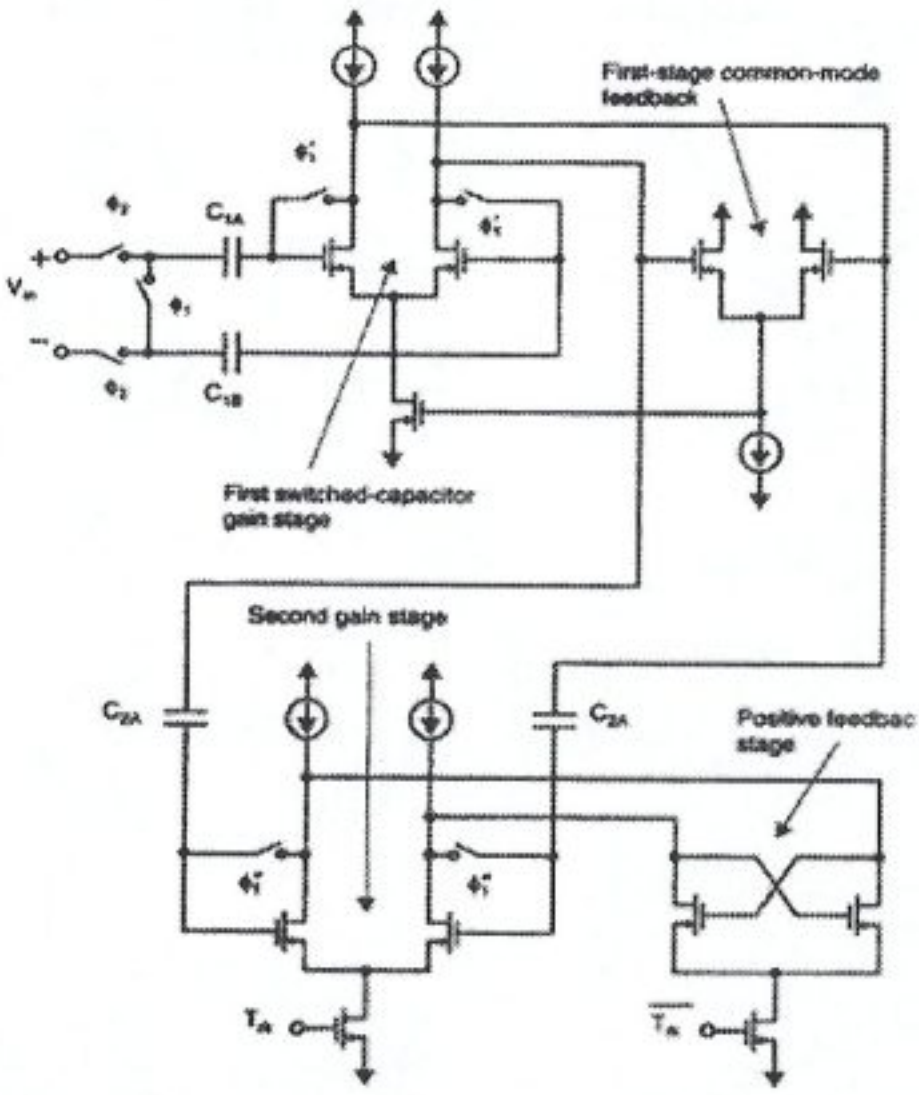


Figure 4.22 A two-stage comparator with capacitive coupling to eliminate input-offset voltage and clock-feedthrough errors along with positive feedback for fast operation [2].

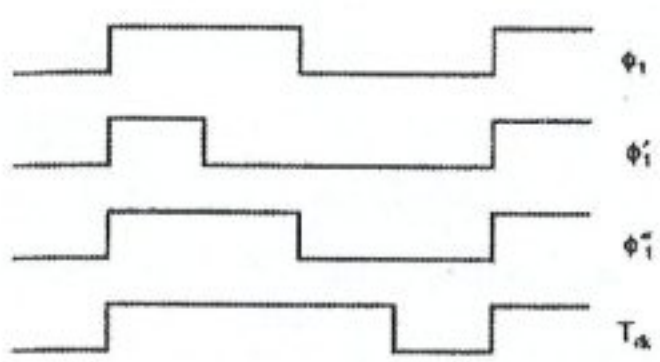


Figure 4.23 The clock waveforms required by the comparator in Figure 4.22 [2].

With a firm understanding of the basic operational characteristics and the design requirements of voltage comparators, we search for high-speed, high-gain, differential out, low power and resetable comparator architectures with low input offset. Some examples of the state-of-art voltage comparators will be given in the following section.

4.3. Examples of State-of-the-Art Voltage Comparators

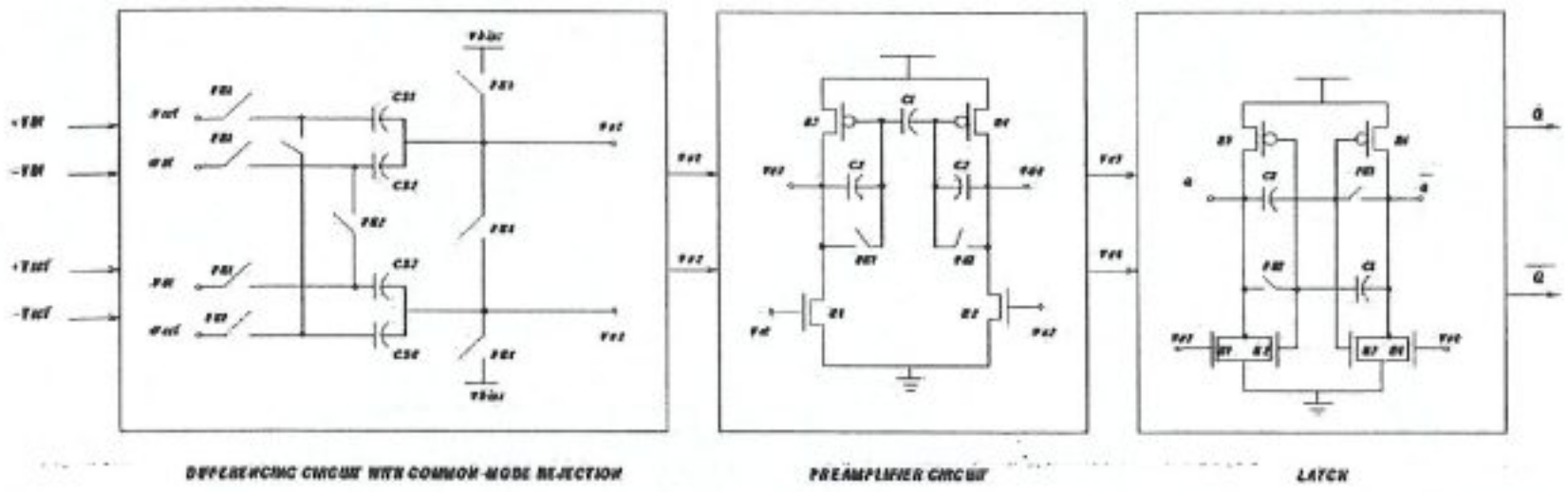


Figure 4.24 A fully differential comparator with two nonoverlapping clocks by Lewis and Hurst [34].

The voltage comparator given in Figure 4.24 is a fully differential high-speed comparator. During PH1, +VIN and –VIN are connected to CS2 and CS3, and $+V_{ref}$, $-V_{ref}$ are connected to CS1 and CS4 respectively. Thus, input voltages are sampled and superimposed to the V_{bias} voltage. During PH2, the left sides of CS1 and CS4 are connected together as are the left sides of CS2 and CS3 and common mode rejection is established. The key advantage of this circuit is; with ideal switches and perfect matching, the samples of V_{common_mode} at the end of PH2 are constant and equal to V_{bias}, independent of the samples of the input and the reference at the end of PH1. Also the preamplifier circuit can be different than the conventional circuits, because the allowed common-mode gain for the preamplifier is increased by the differencing circuit that is used. A tail current source connected in a standard differential-pair may not be required. Thus, eliminating the tail current source would allow an operation at a reduced supply voltage, consecutively low power. The key disadvantage of this circuit is, the differential gain here is about half that of a conventional differencing circuit because four sampling capacitors are required instead of just two. This comparator is a building block of a 3-bits flash ADC in 2-μm CMOS technology with a power supply voltage of 3.3V, a sampling rate of 25MHz, dissipates 1.05mW and occupies 0.25 mm^2 [34].

A second high-speed comparator is given in Figure 4.25. This is a voltage comparator circuit by Razavi and Wooley [33]. It was realized in 1-μm CMOS

technology with single supply of 5V, it dissipates 0.55mW and its measured input offset is less than 5mV at 5MHz sampling rate. Input offset is cancelled during PH1 phase. In this phase switches S3 through S7 are on, nodes P and Q are charged to Vref+ and Vref- respectively, and the amplifier's offset is stored on C1 and C2 capacitors. In the transition from this mode to comparison mode, PH1 goes low, turning off switches S3-S7 and turning on S1 and S2. The circuit then begins to regenerate, amplifying the voltage difference between +VIN and –VIN and +Vref and –Vref. Since regeneration begins with M1-M4 already on, its offset voltage is relatively independent of the clock fall time. Nonetheless, if S5-S7 turn off simultaneously any mismatch in the charge injected onto the gates and drains of M1 and M2 can cause false regeneration around M3-M4, resulting in a large input referred offset. In order to avoid this problem, phased clocks are used to turn-on and off the switches as: first turn S3-S6 off to end the reset mode, than turn S1-S2 on to begin the tracking mode and finally turn S7 off to allow regeneration around M3-M4. The clocking scheme of this comparator is too complicated although it is shown as a single clock circuit in Figure 4.25.

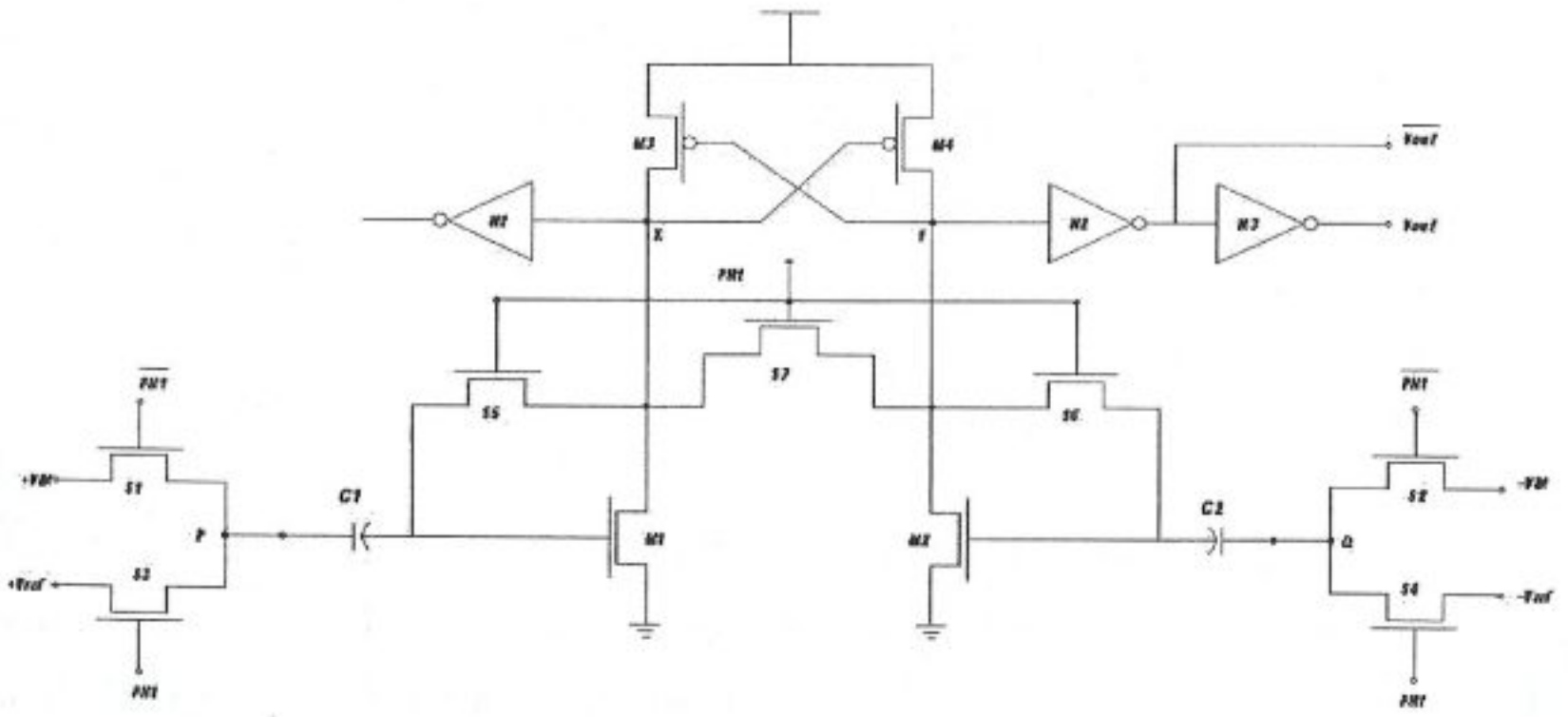


Figure 4.25 A comparator by Razavi and Wooley [33].

A third and very suitable voltage comparator example is given in Figure 4.26. This is a comparator circuit by Frank Op't Eynde and W.Sansen [32]. An experimental version of this comparator has been integrated in a standard double-poly-metal 1.5-μm

n-well process with a die area of only 140 × 100μm^2. This comparator operates under a ±2.5V power supply, performs comparison to a precision of 8-bits, thus its resolution is equal to ±4.9mV. The highest operation speeds of MOS comparators with 8-bits precision previously introduced than this comparator have been limited to sampling rates of 30MHz for the same technology. But the experimental prototype achieving 8-bit accuracy with the sampling rates up to 65MHz is obtained. The power consumption of the comparator is only 0.85mW at 65MHz clock rate.

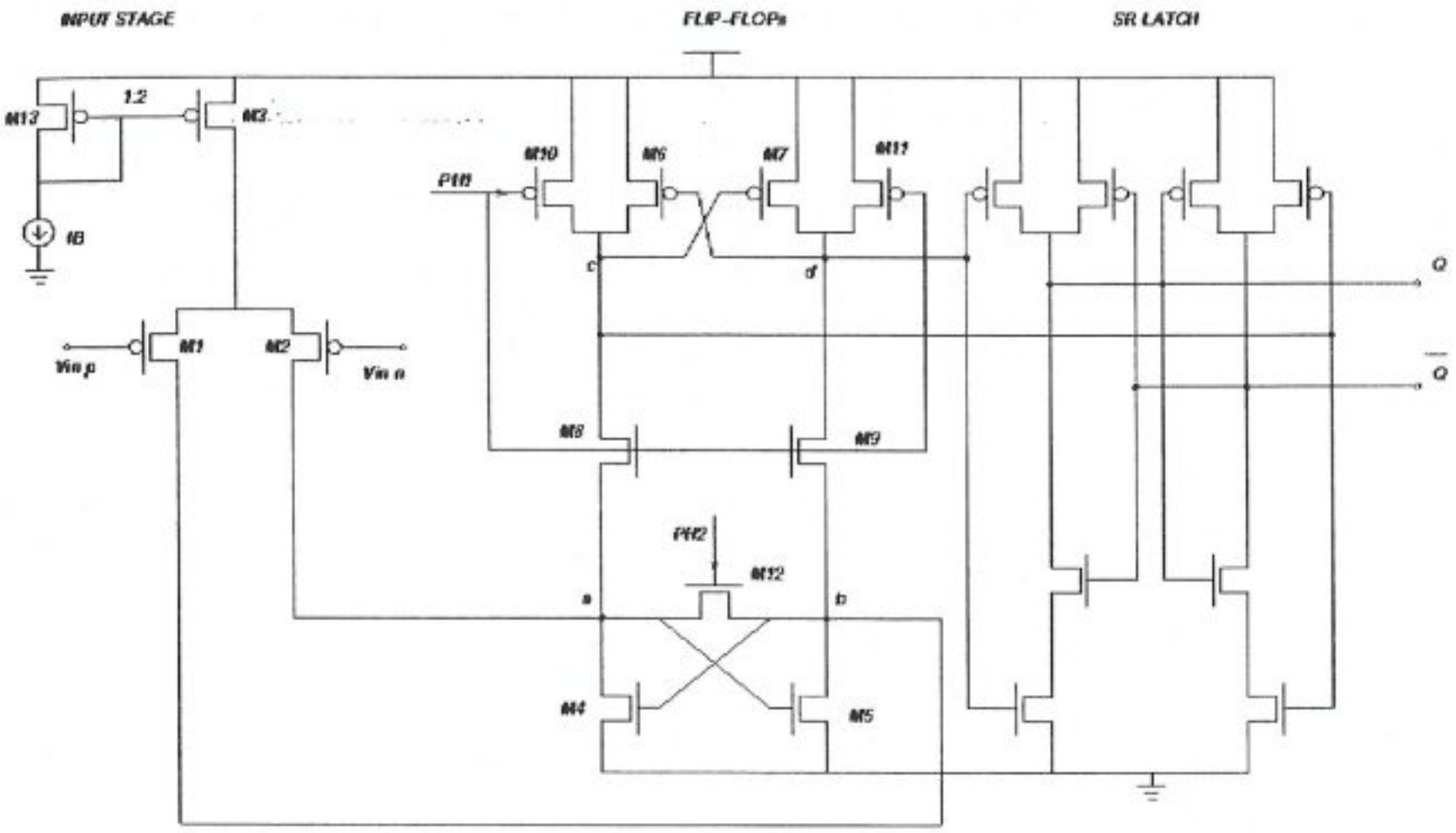


Figure 4.26 A fully differential, high-speed voltage comparator [32].

The dynamic operation of this circuit is divided into a reset time interval and a regeneration time interval. The two intervals are approximately between time interval t1 and t2 and between t2 and t4 respectively, as shown in Figure 4.26. During PH2, the comparator is in reset mode. Current flows through the closed resetting switch M12, which forces the previous two logic state voltages to be equalized. After the input stage settle on its decision, a voltage proportional to the input voltage difference is established between nodes a and b in the end. This voltage will act as the initial imbalance for the following regeneration time interval. In the meantime, as the n-channel flip-flop is reset, the p-channel one is also reset by the two closed precharge transistors, which charge

nodes c and d to the positive power supply voltage. As a result the CMOS latch is set to the astable high-gain mode.

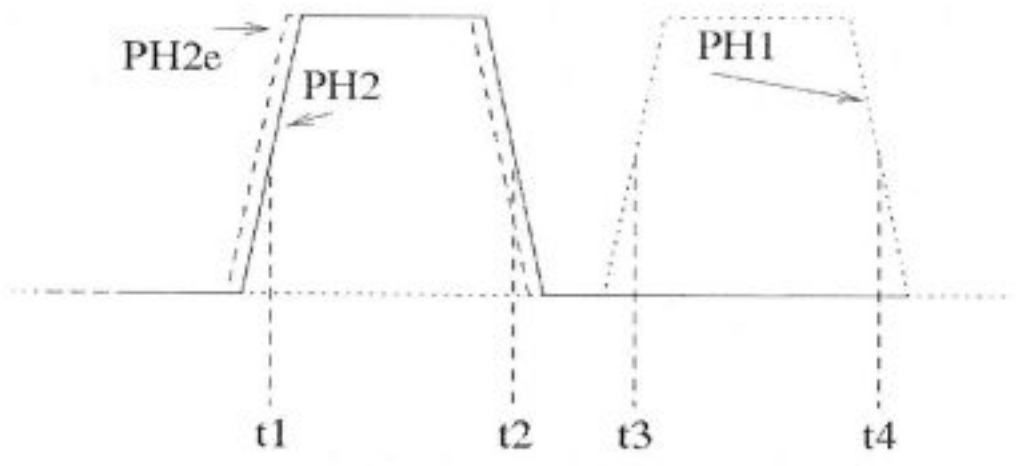


Figure 4.27 Timing information for the comparator given in Figure 4.26 [32].

The regeneration phase is initialized by the opening of switch M12. Since the strobing transistors M8 and M9 isolate the n-channel flip-flop from the p-channel flip-flop where PH1 is low, the use of two non-overlapping clocks perform the regenerative process in two steps. The first step of regeneration is within the short time slot between PH2 getting LOW and PH1 getting HIGH. The second regeneration step starts when PH1 gets HIGH and M8-M9 are closed. The n-channel flip-flop, together with the p-channel flip-flop regenerates the voltage differences between nodes a and b and between c and d. The voltage difference between c and d is soon amplified to a voltage swing nearly equal to the power supply voltages. The following SR latch is driven to full complementary digital output levels at the end of the regenerative mode and remains in the previous state in reset mode.

The first regeneration step is very important; not only in raising the regeneration speed but also in reducing the total input offset voltage. The differential errors caused by the charge injection from M8 and M9, mismatches in the p-channel flip-flop, two precharge transistors and the S-R latch are divided by the amplification gain in the first regeneration step, when referred to the input as an equivalent offset voltage. Therefore, their contribution to the total equivalent input offset voltage can be neglected if the gain is large enough.

At the time when PH2 falls, voltages at nodes a and b decrease because if the clock injection, and in the meantime the currents from M1 and M2 charge the two nodes to resume their voltages. Later, as the conductance of switch M12 becomes smaller than

half of the transconductance of M4 and M5, the n-channel flip-flop starts the first step of regeneration. This regeneration process can be approximately analyzed using a small-signal model as shown in Figure 4.28.

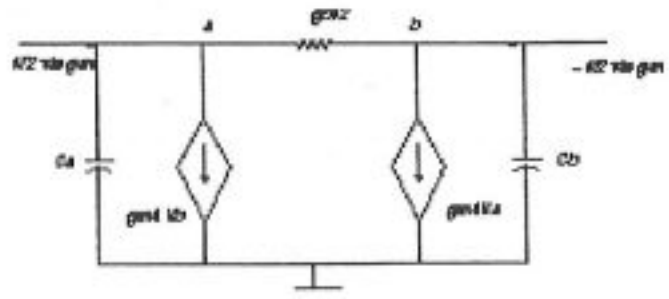


Figure 4.28 Regeneration process small signal equivalent [32].

$$\tfrac{1}{2}\, v_{in} g_{m1} = C_a\, dv_a/d_t + g_{m4} v_b + g_{o12}(v_a - v_b) \tag{4.5}$$

$$-1/2\; v_{in} g_{m1} = C_a\, dv_b/d_t + g_{m4} v_a - g_{o12}(v_a - v_b) \tag{4.6}$$

In these equations v_{in} is equal to $v_{inp1} - v_{inp2}$. Voltages v_a and v_b stand for the increments relative to the voltage at nodes a and b with zero input difference. Solving Eq. 4.5 and Eq. 4.6 gives

$$v_{ab} = [v_{a0} - v_{b0} - g_{m1} / (2g_{o12} - g_{m4}) v_{in}] \exp(t/\tau) + g_{m1} / (2g_{o12} - g_{m4}) v_{in} \tag{4.7}$$

$$\tau = C_a / (g_{m4} - g_{o12}) \tag{4.8}$$

Eq. 4.7 and Eq. 4.8 shows that when g_{o12} is smaller than half of g_{m4} τ becomes positive and the first regeneration step starts.

To optimise the speed of the first regeneration step, the most efficient way is to minimize the time constant. When M12 is off, the time constant only depends on the capacitance at node a and b and the transconductance of M4 or M5. The capacitance is related to the sizes of M1, M2, M4, M5, M8, M9 and M12.

The voltage difference between nodes a and b reduces very quickly at the beginning of the reset. Later the reduction rate slows down. It will have a local minimum at some instant if the current through M12 is equal to the current through M5 while M4 just reaches the edge of conducting, which should be avoided in high-speed

applications. Therefore, the width of M4 or M5 and M12 should satisfy the inequality of $I_{12} > I_5$ at that moment to ensure that there is still some extra current to charge node b. By using a simplified current model, the inequality is

$$W_{12} / L\, K_{pn}[(V_{dd} - V_b - V_{Tn12})(V_a - V_b) - 0.5(V_a - V_b)^2)] \quad >$$

$$W_5 / L\, K_{pn}[(V_a - V_{ss} - V_{Tn5})(V_b - V_{ss}) - 0.5(V_b - V_{ss})^2)] \qquad (4.9)$$

In the second period of the reset mode, the circuit behavior can be derived using the small signal model given in Figure 4.28. Under the resetting conditions, we obtain

$$v_{ab} = g_{m1} v_{in} / (2g_{o12} - g_{m4}) + A \exp(t/\tau)$$
$$v_a + v_b = B \exp(-g_{m4} / C_a t) \qquad (4.10)$$

Eq. 4.7 and Eq. 4.8 indicate that if $2g_{o12}$ is smaller the g_{m4} it is impossible to have the comparator reset. If $2g_{o12} < g_{m4}$ it is impossible to reset the comparator. For the regeneration time optimization, when M12 is off the time constant in the first regeneration step can be written as

$$\tau_{reg} = (\alpha W_4 + C_p) / \sqrt{2I_4 W_4 / L_4 K_{pn}} \qquad (4.11)$$

αW4 represents the capacitance related to the width of M4 or M5, and it will also include the capacitances from M12 and M8 or M9 if W12, W8 and W9 are all chosen to be proportional to W4. The reference current can be increased to raise the comparison speed, however $V_{GS1} - V_{TP1}$ will be larger and a larger offset voltage will result. [32]

Based on the discussions presented in this section, we present a new voltage comparator circuit in the next section that satisfies all of the strict design requirements set by the high speed pipelined ADC architecture specifications.

4.4. Proposed Voltage Comparator Architecture

This chapter presents the design of the novel voltage comparator circuit that is based on a simple symmetric cross-coupled latch structure that operates with a single clock signal. This circuit is capable of responding to a very wide range of input voltages (almost equal to the power supply range of the circuit), that makes it a very attractive option for low-voltage applications. At the same time, the response speed of the proposed comparator circuit is high enough to allow operation at 200 MHz (in fact, up to 1 GHz) sampling clock frequency.

4.4.1 Basic Comparator Circuit

The basic version of the proposed voltage comparator circuit is shown in Figure 4.29. Here, the cross-coupled latch core consisting of M1-M4 produces the output decision based on a small imbalance of the branch currents. The nMOS transistor M5 is used to reset the latch, while M6 and M7 receive the input signals V_n and V_p. The parallel-connected nMOS transistors M8 and M9 simply provide robust current path for the output latch during the decision phase.

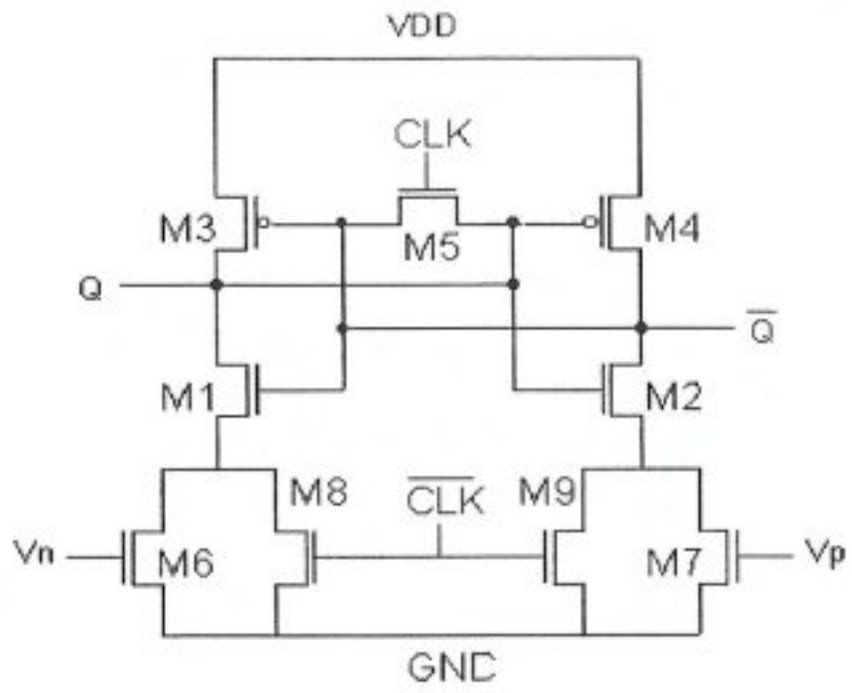


Figure 4.29 Basic voltage comparator schematic.

The dynamic operation of the circuit is controlled by a single clock signal (CLK). When the clock is HIGH, the output latch (and consequently, the comparator) is in reset

mode. Both output nodes are stabilized at inversion threshold, and the output latch operates at its highest gain point. Meanwhile, the two input voltages V_n and V_p are applied to M6 and M7, producing a slight difference in the drain-to-source voltage levels. When the clock signal returns to zero, M5 releases the cross-coupled latch from its reset mode while M8 and M9 are turned on to provide a robust current path for the latch circuit. The output decision is produced in a very short amount of time based on the previously established current / voltage difference between the two symmetric branches.

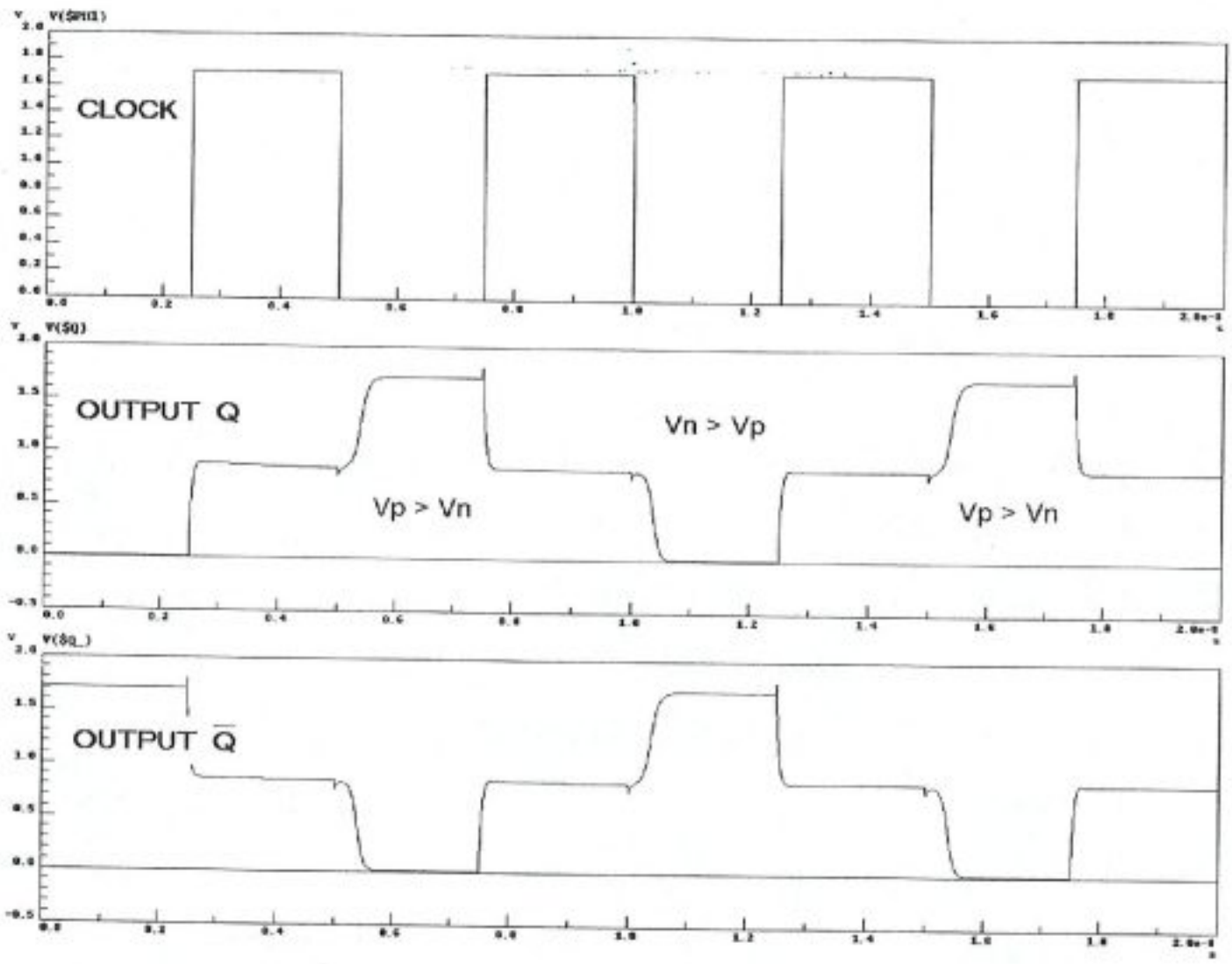


Figure 4.30 Output waveforms of basic voltage comparator circuit.

The typical output voltage waveforms of the basic comparator circuit are shown in Figure 4.30. The input voltage difference reverses its sign in consecutive clock cycles, and the corresponding output decision is generated with a very short response time following the falling edge of the clock signal. The basic comparator circuit has the significant advantages of a very simple structure, small area, relatively high-speed and low power dissipation.

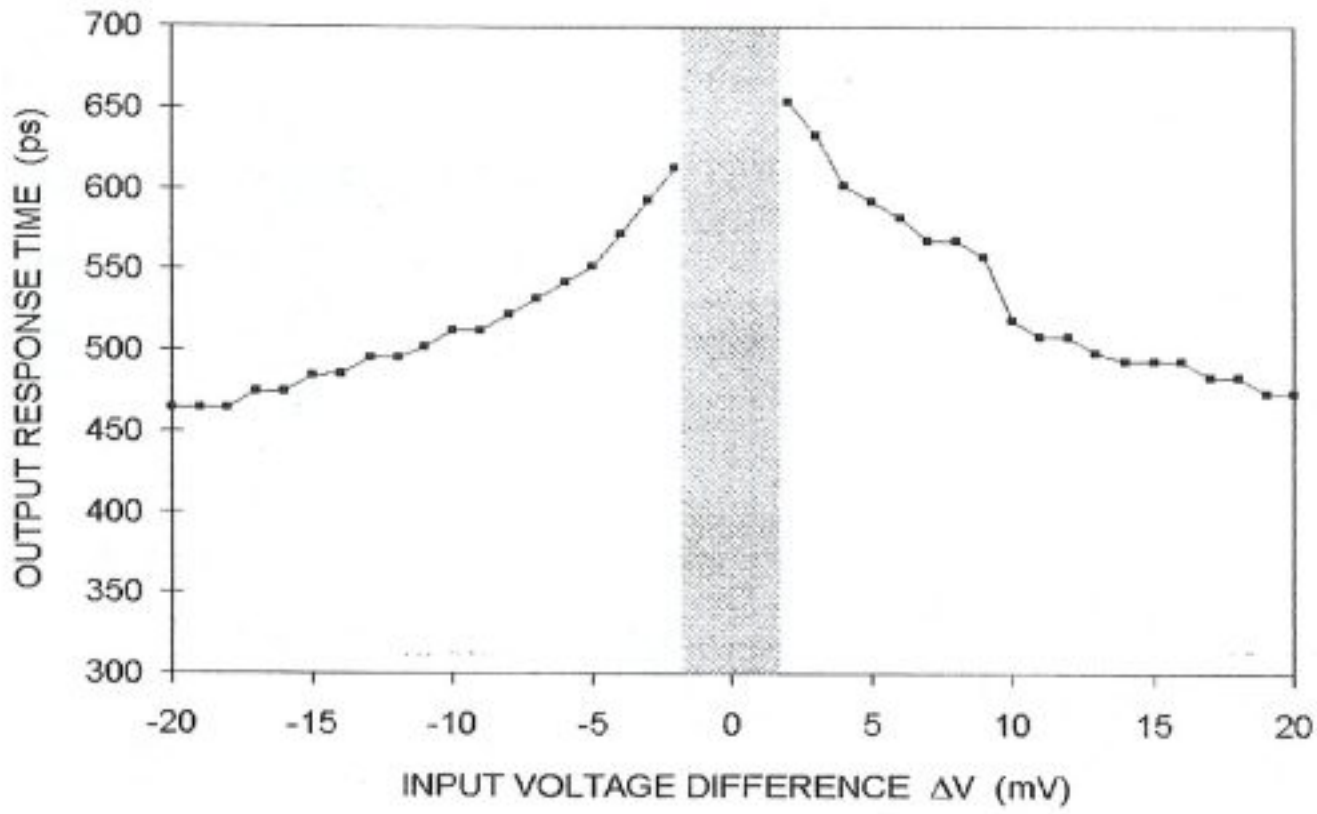


Figure 4.31 Response time vs. input voltage difference.

The output response time of the basic comparator circuit is shown in Figure 4.31 as a function of the input voltage difference ΔV. The response time is seen to increase as the voltage difference becomes smaller, but does not exceed 650 ps even within 2mV of decision threshold. The response time drops significantly, as the input voltage difference becomes larger. Typical response times for ΔV = 500mV were found to be less than 200 ps when driving a capacitive load of 50 fF on both outputs. Note, however, that this basic comparator circuit cannot produce a reliable output decision when both of the input voltages are below the threshold voltage level of nMOS transistors M6 and M7. Response times for the full input range that can produce a reliable output for the basic comparator circuit can be seen in Figure 4.32. Note that, V_n is held constant at V_{full_scale} / 2 in this figure.

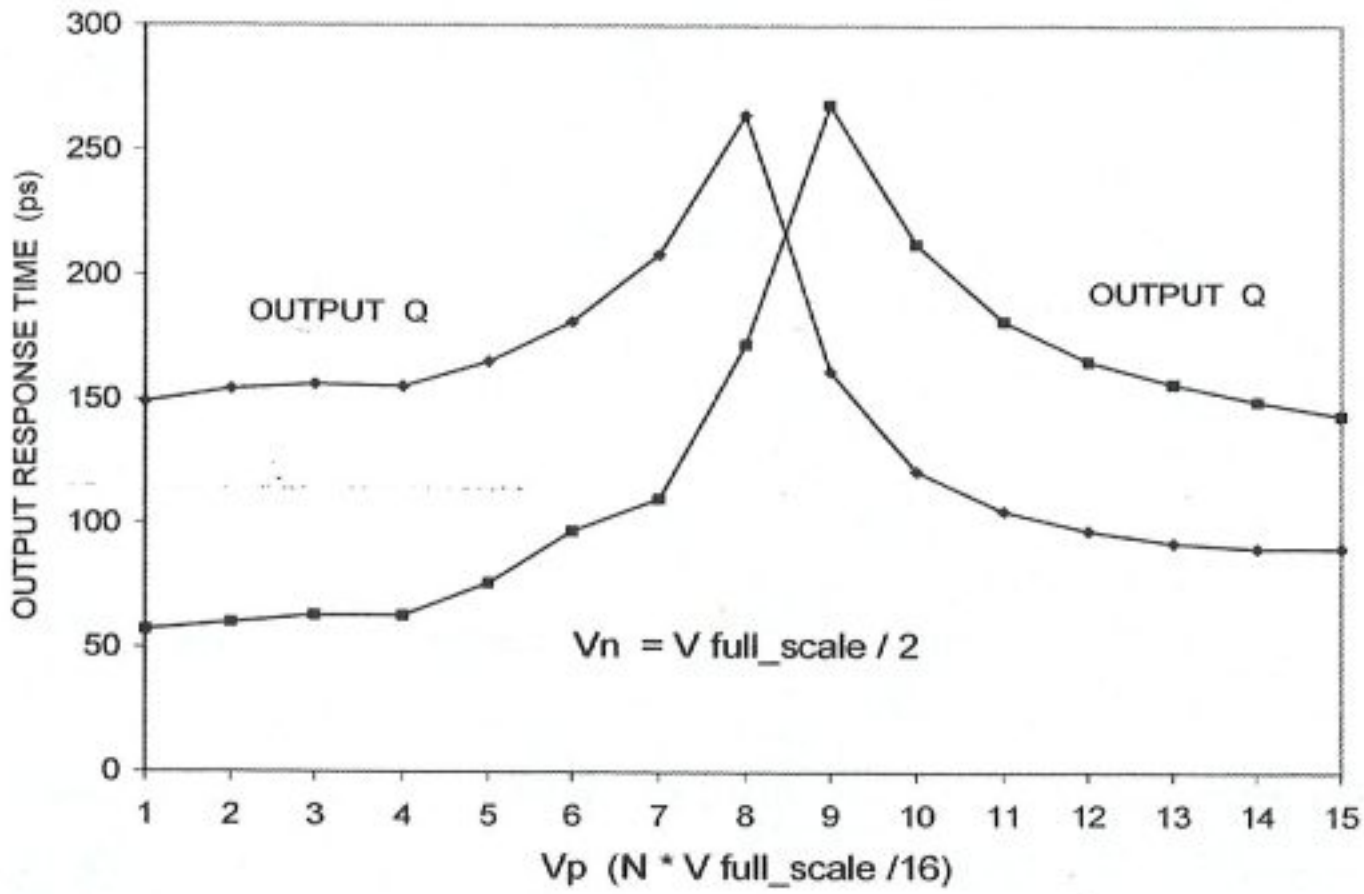


Figure 4.32 Response time variation along the entire input dynamic range for basic voltage comparator. ($V_{full\_scale} = 1.8V$)

4.4.2 Full Complementary Voltage Comparator

As already mentioned in the previous section the basic comparator circuit suffers from a limited input dynamic range. To further increase the input dynamic range the basic topology is modified with four additional transistors. The circuit diagram of the improved comparator circuit is shown in Figure 4.33.

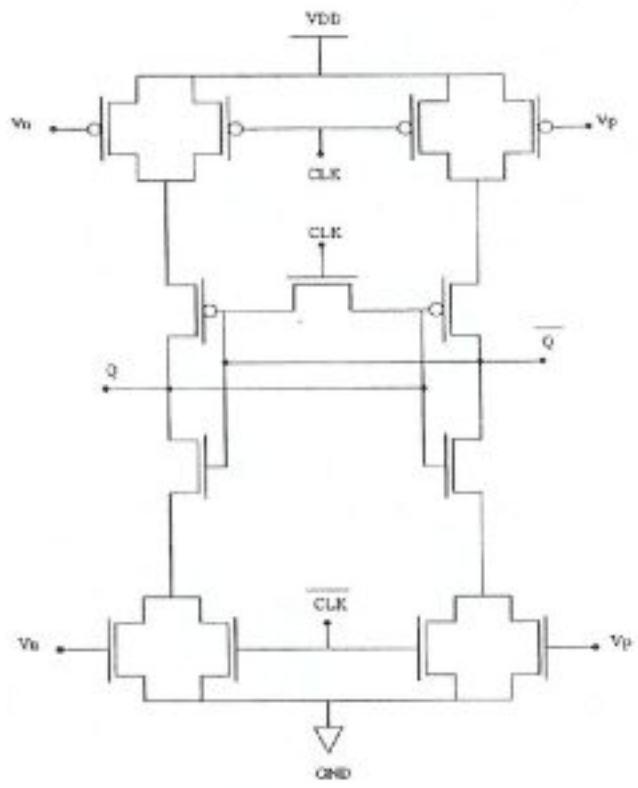


Figure 4.33 Full-complementary voltage comparator circuit diagram.

The added complementary pMOS transistors in the pull-up path of the latch core act the same way as the nMOS transistors in the pull-down path. During the reset phase, the pMOS transistors driven the input voltages create a small current difference between the two symmetric branches, and during the decision phase, the two pMOS transistors driven by the clock signal establish a current path for the latch circuit. The complementary pMOS transistors become especially important when both input voltages are lower than the threshold voltage of the nMOS transistors. Thus, the circuit has the ability to respond a very wide input dynamic range, which practically extends to full range of the power supply voltage.

After the simulations done to identify the input voltage range that this topology can handle, it is confirmed that almost rail-to-rail input voltage range in 1.8V supply voltage is achievable. This improved comparator topology can produce a reliable output decision in all process corners when $1.6V_{pp}$ input voltage range is used. It can also produce reliable outputs for typical and best case simulation conditions for $1.8V_{pp}$ input voltage range for the simulations done from schematic view.

The disadvantage of this topology is the insufficient response times (typically 600 ps) for 200 MHz pipelined A/D converter structure. Still, the complementary comparator with improved input voltage range has the significant advantages of a very simple structure, small area, low power dissipation and almost rail-to-rail input dynamic range.

4.4.3 Improved Full Complementary Voltage Comparator

As already mentioned in the previous section, the improved basic voltage comparator with the full complementary input stage suffers from a limited output response time. To further improve the response speed, the new circuit was modified with four additional transistors. The circuit diagram of the improved complementary comparator circuit is shown in Figure 4.34. The operating principles of the improved full-complementary comparator are exactly the same as the original complementary voltage comparator described in Section 4.4.2, with the exception that the output stage provides significantly better drive capability to improve the response times.

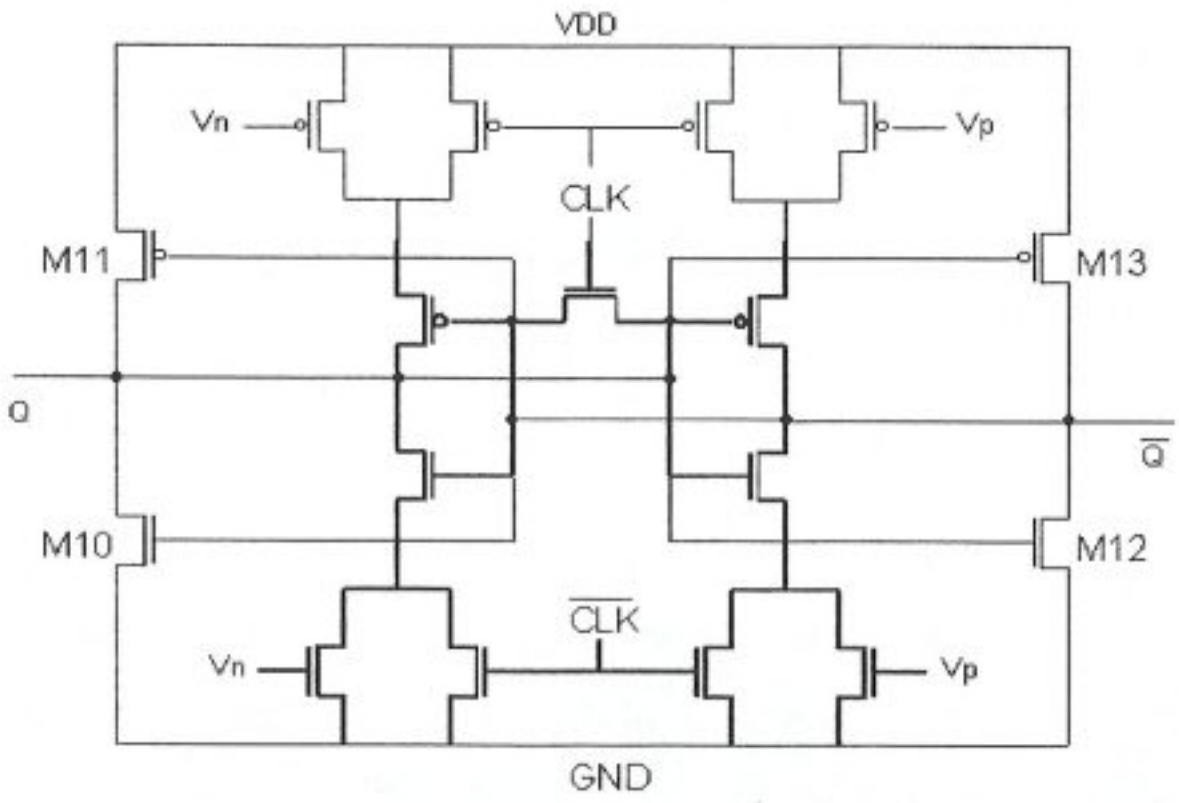


Figure 4.34 Improved full complementary voltage comparator circuit.

Note that in Figure 4.34, the transistors that correspond to the basic voltage comparator circuit are highlighted. The transistors M10-M13 are used to further improve the output response speed. Note that the CMOS pair at each output node is driven by the output signal of the other output, resulting in an accelerated pull-up (and pull-down) of the corresponding output levels. Figure 4.35 shows the output response time of the improved comparator circuit as a function of the input voltage difference, when both outputs are loaded with 50 fF load capacitance.

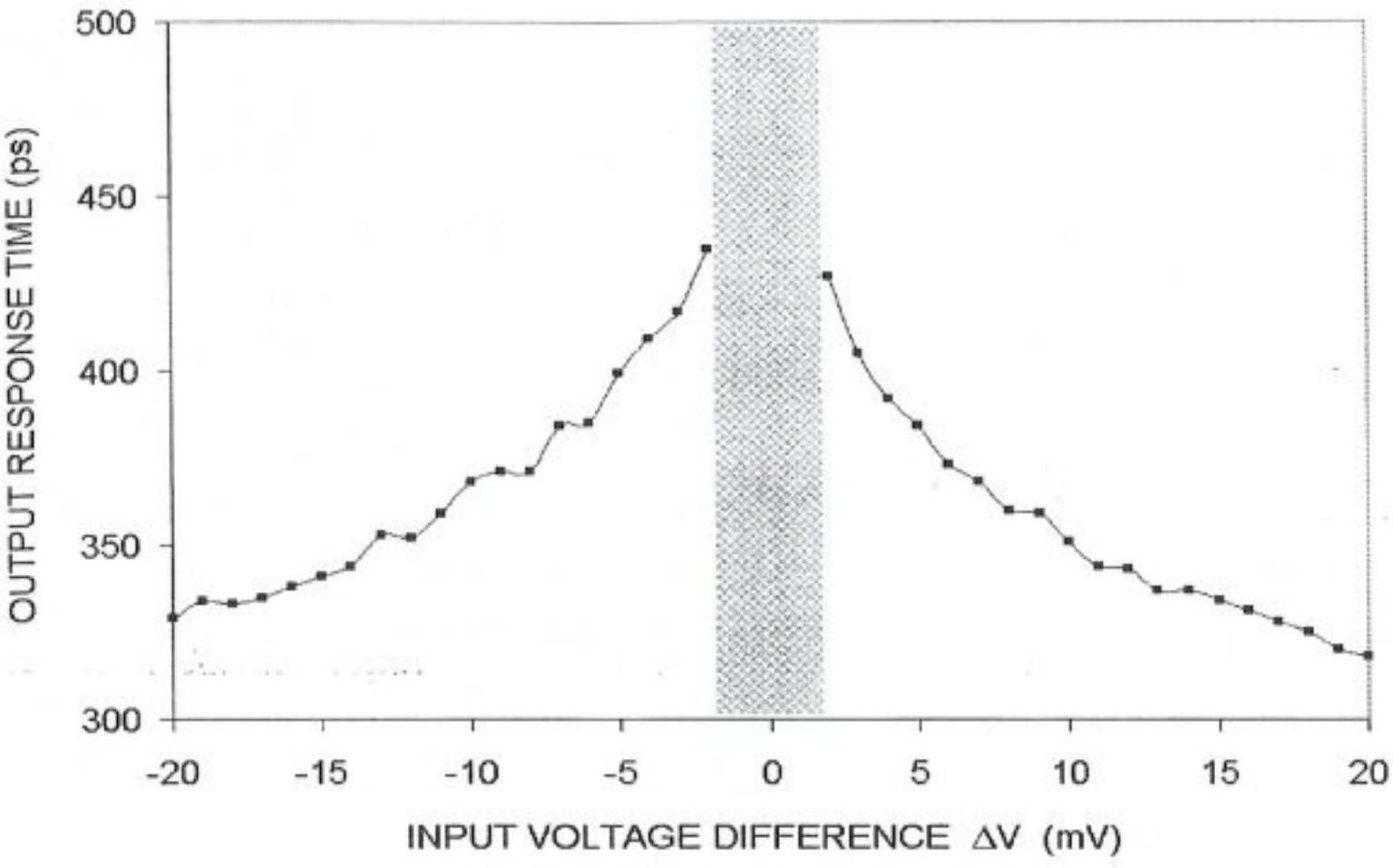


Figure 4.35 Response time of improved full complementary comparator with respect to input voltage difference.

The response times of the improved complementary comparator circuit were found to be about 150 ps shorter than those of the basic comparator circuit (Figure 4.32) for larger input voltage ranges (which includes threshold levels of both nMOSs and pMOSs). As a result sampling frequencies up to 1 GHz were obtained. The worst case response times for larger input voltage differenced are plotted in Figure 4.36, where one of the input voltage is held constant at $V_{FS} / 2 = 0.9V$, the other input is progressively increased with 10mV steps, and the response times were recorded. It can be seen that the response times exhibit a very symmetric distribution for the entire input range.

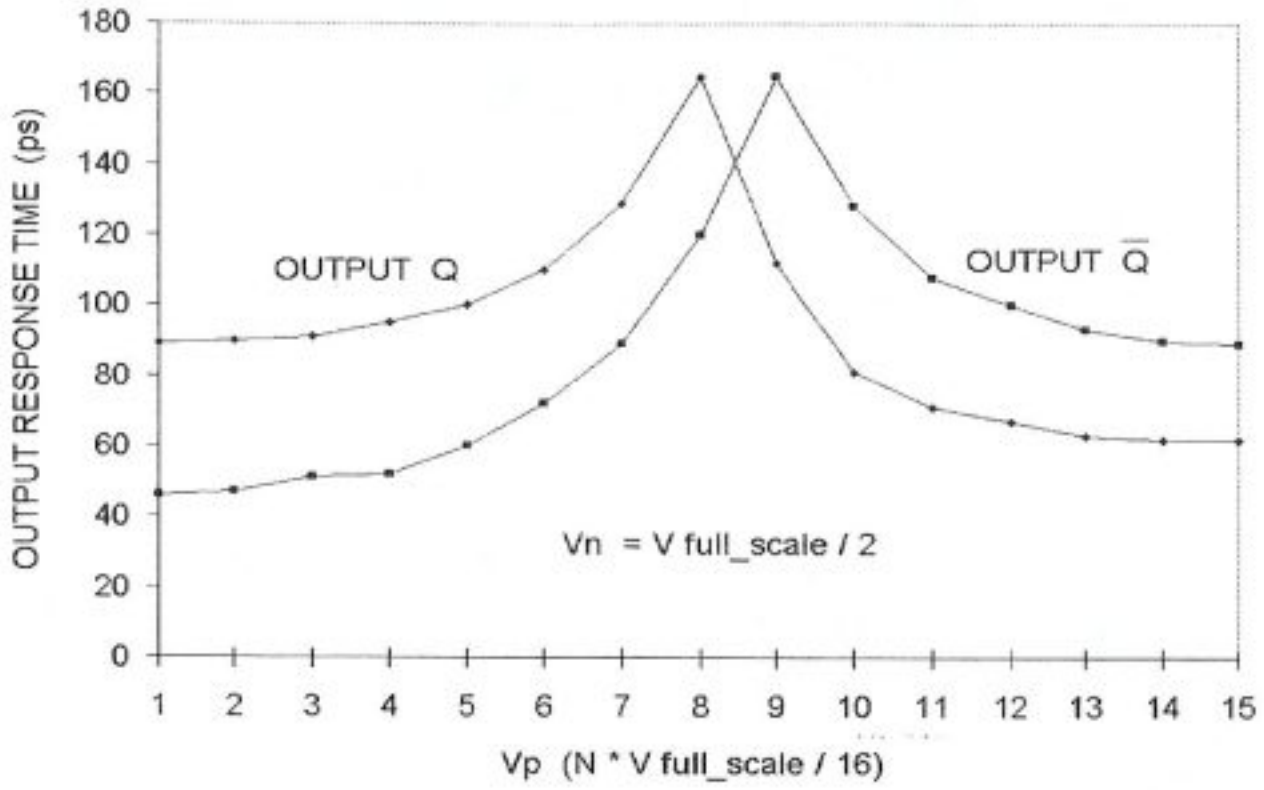


Figure 4.36 Response times of the improved full complementary voltage comparator, obtained for the entire input range.

Also response times for different input voltage differences can be seen in Figure 4.37 while one of the input is held constant at LSB reference voltage level (0.1 V) and the other is increased by 100mV voltage steps.

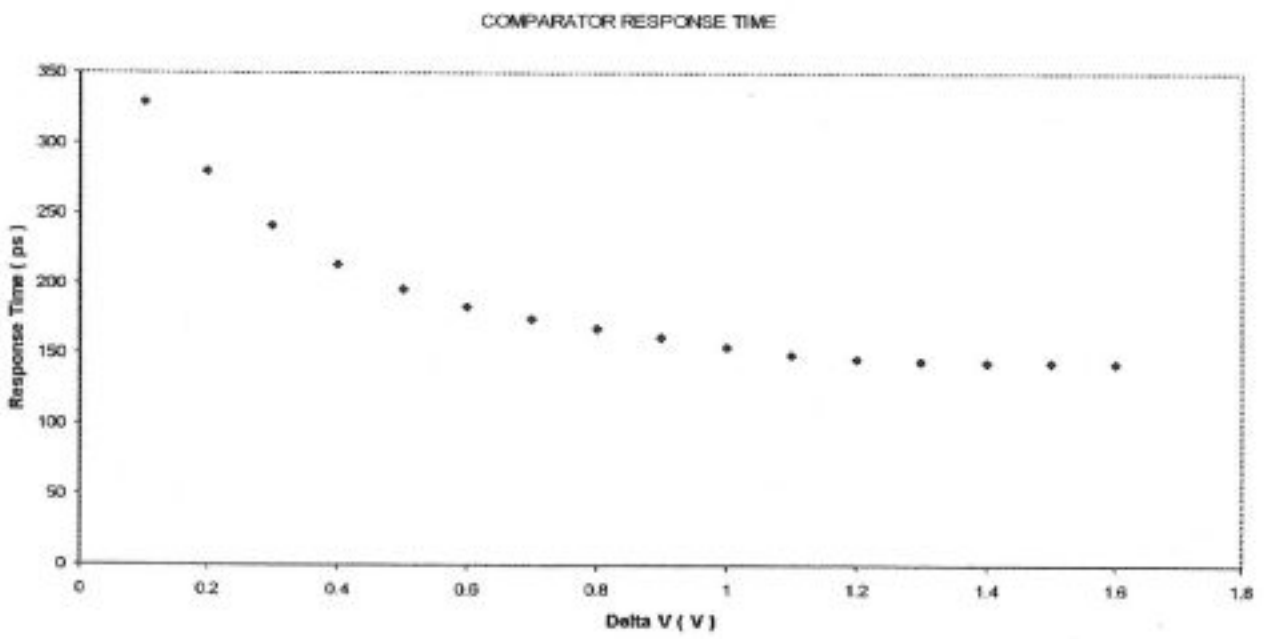


Figure 4.37 Response times obtained for different input voltage differences.

Power consumption of the improved complementary voltage comparator is examined in two different ways. First, consumed power is examined with changing the

voltage difference applied to the two inputs (Figure 4.38), second; power consumption is plotted for different sampling frequencies (Figure 4.39).

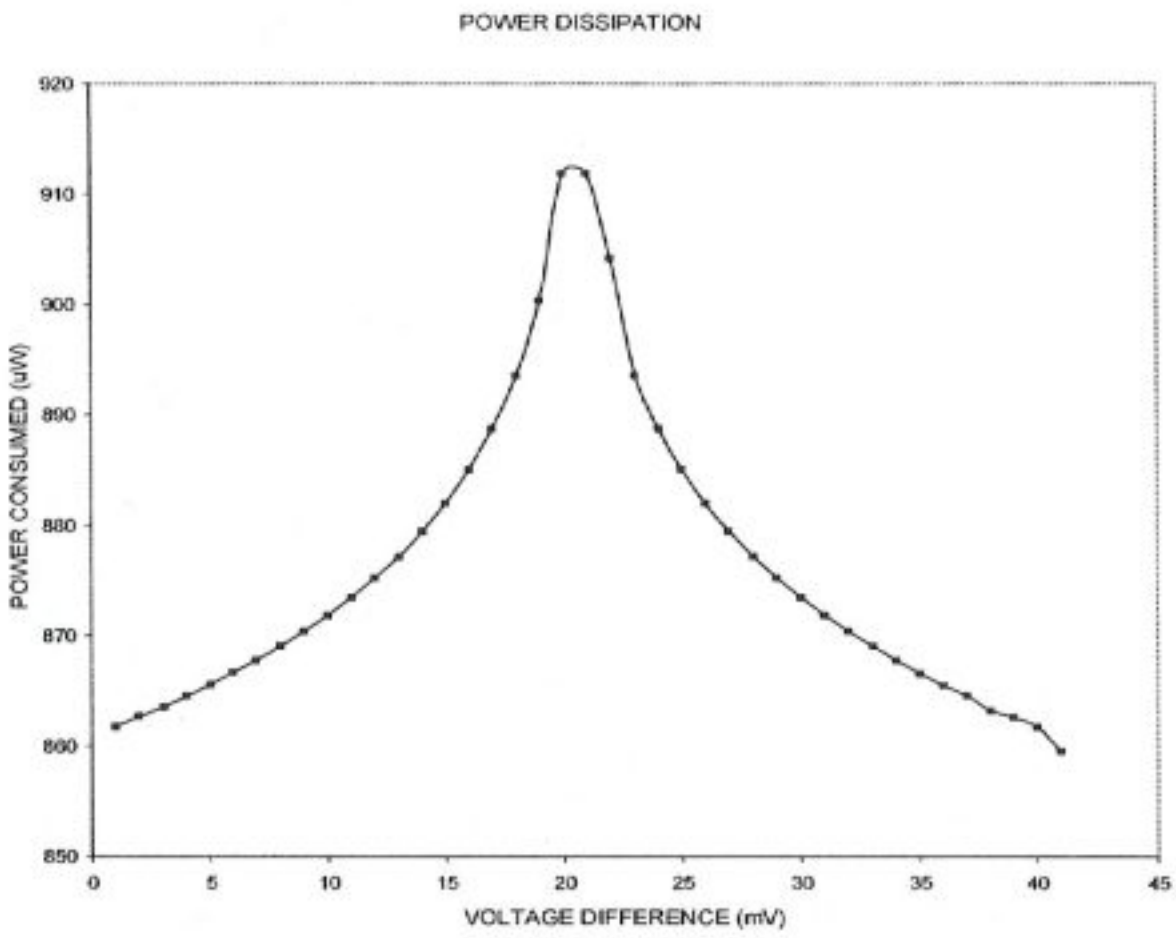


Figure 4.38 Power consumption for different input voltage differences.

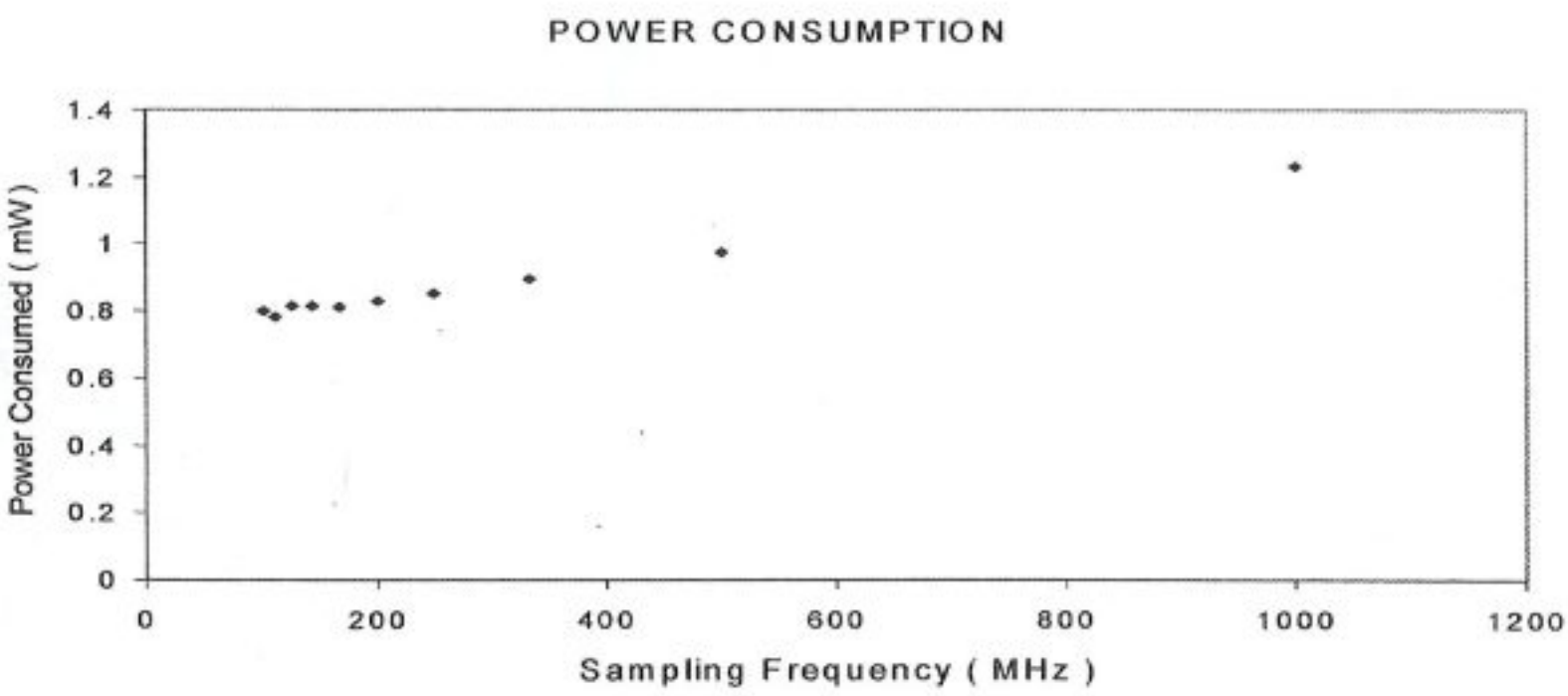


Figure 4.39 Power consumption for different sampling frequencies.

The worst-case input voltage offset of the improved complementary comparator was found to be ≤ 10 mV, allowing conversion with greater than 10-bit accuracy at a dynamic input range of $1.6V_{pp}$. The INL and DNL error values remain with in ± 0.1LSB for this 4-bit application, due to the fact that the maximum offset does not exceed 10 mV. To evaluate the performance of the proposed improved complementary voltage comparator circuit in ADC applications, we have constructed and extensively simulated four bit flash A/D converter architecture consisting of a resistor voltage divider chain and fifteen identical comparators (Figure 4.41). Each comparator in the simulated converter chain drives dual CMOS transmission gates, which represent a combined load capacitance of approximately 50 fF. Characterization of the improved full complementary comparator for all three corners (best-typical-worst) in response time, power consumption, integral and differential nonlinearities, offset and also sampling speed simulations were done for the given 4-bit flash topology. These simulation results are given below with detailed information specified underneath of each figure. The mask layout of the improved complementary comparator is shown in Figure 4.40. The circuit occupies a silicon area of about 320 μm^2 in 0.18 μm CMOS technology.

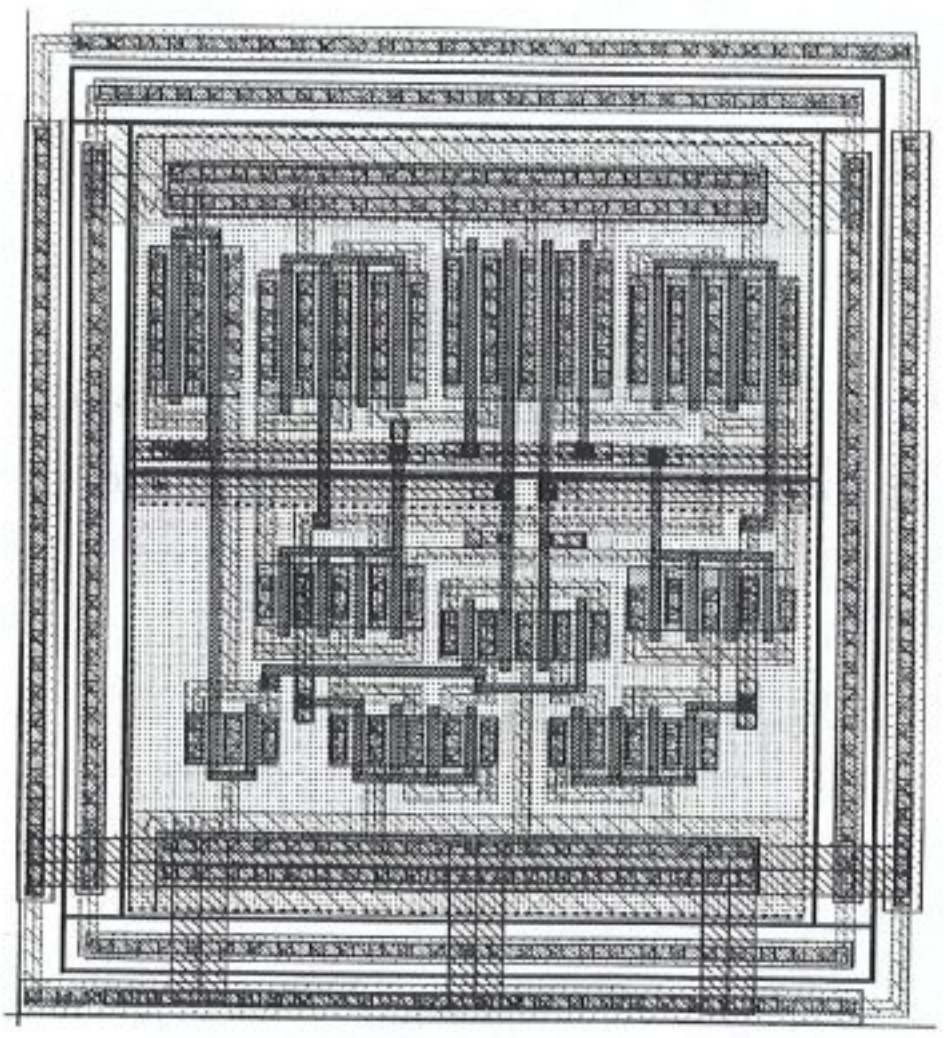


Figure 4.40 Layout of the improved complementary-in voltage comparator.

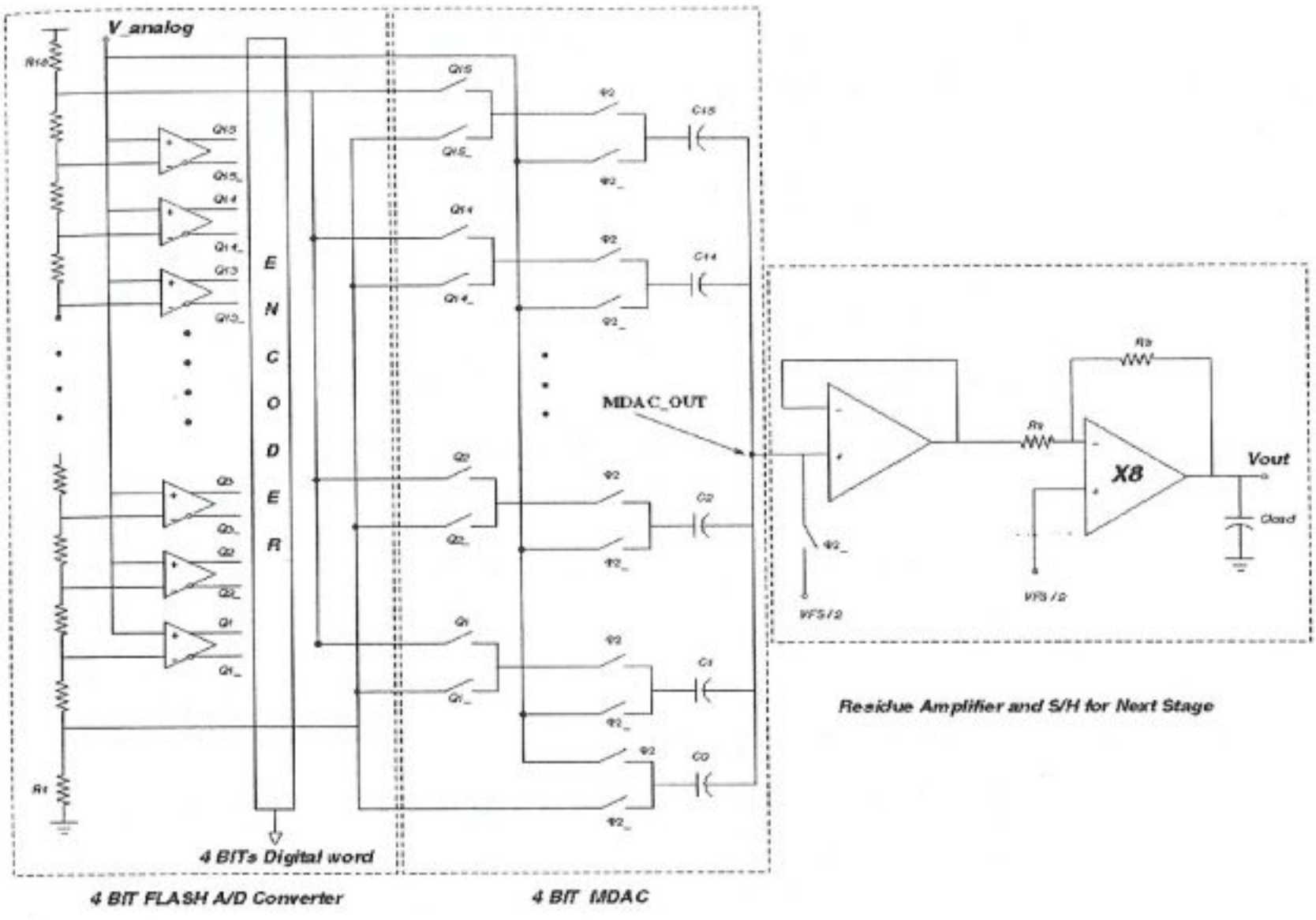


Figure 4.41 4-bit ADC / MDAC schematic used in improved full complementary voltage comparator verification.

A 4-bit flash ADC and MDAC were simulated for the entire input dynamic range in ideal simulation conditions for all three corners of silicon parameters. Delays of Q and Q_ outputs were recorded for the corresponding falling edge of the CLK as well as the delay of the multiplying DAC output. This data obtained for typical corner silicon is given in Figure 4.42. Then, possible mismatch errors that can occur in the input transistors were taken into consideration and simulations modeling these effects were done on the schematic given in Figure 4.41. Mismatch that can occur in nMOS transistors was set to a maximum of ±%3.58 and ±%2.85 for pMOS transistors in the design rule manual for 0.18μm CMOS technology. Thus, three corner simulations were done to identify these effects on comparators with manually mismatched input stages for different input voltage levels. The strategy of these simulations was to apply manual mismatch information to only one input stage transistor at a time. Consequently, nMOS

and pMOS input stages were disturbed independently from each other. Only typical corner simulation results will be given for LSB, MSB and V_{full_scale} / 2 voltage levels.

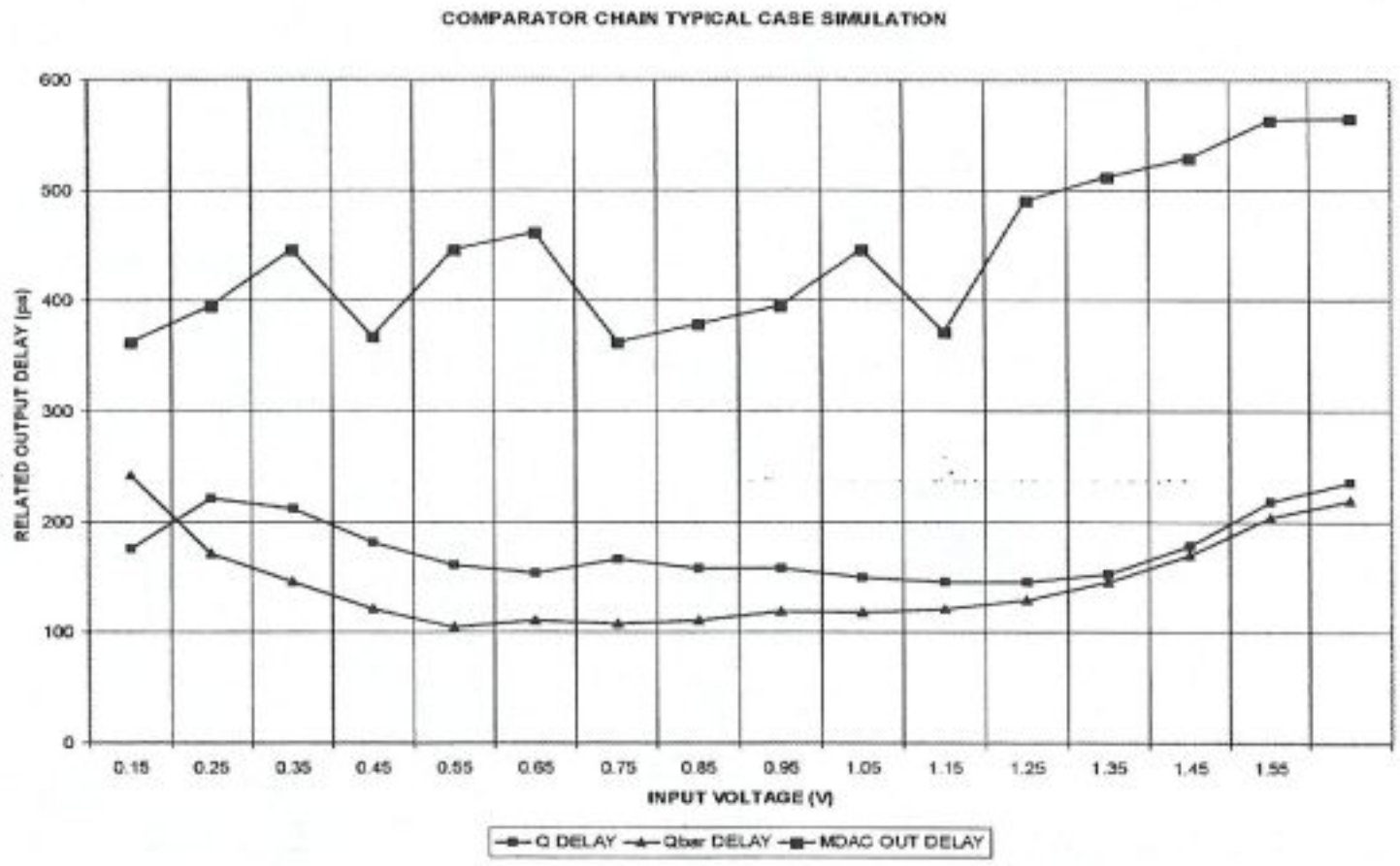


Figure 4.42 Response times for Q, Q_ and MDAC output voltage in ideal conditions.

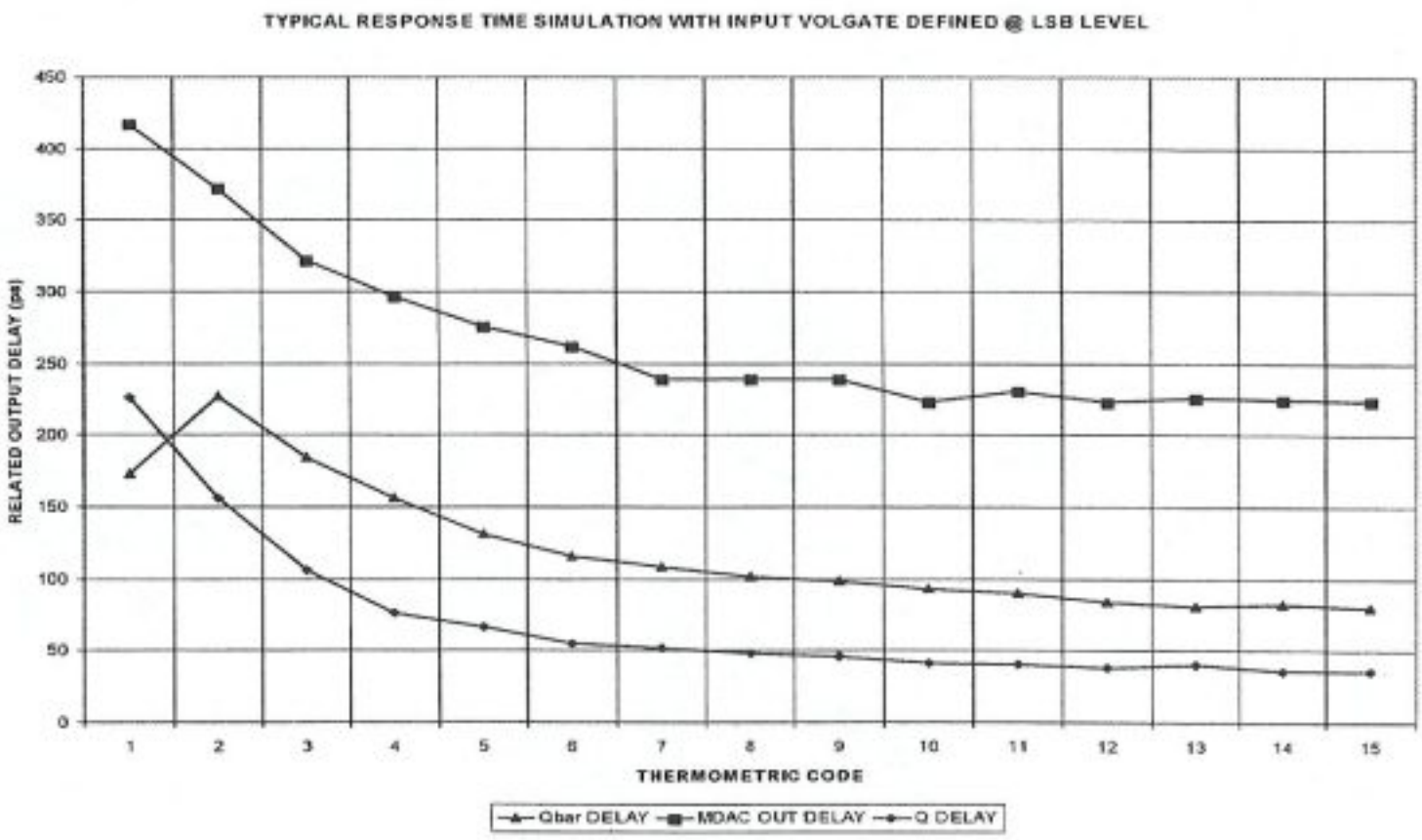


Figure 4.43 Response times obtained for input voltage at LSB level, typical corner and nMOS input stage transistors with mismatch.

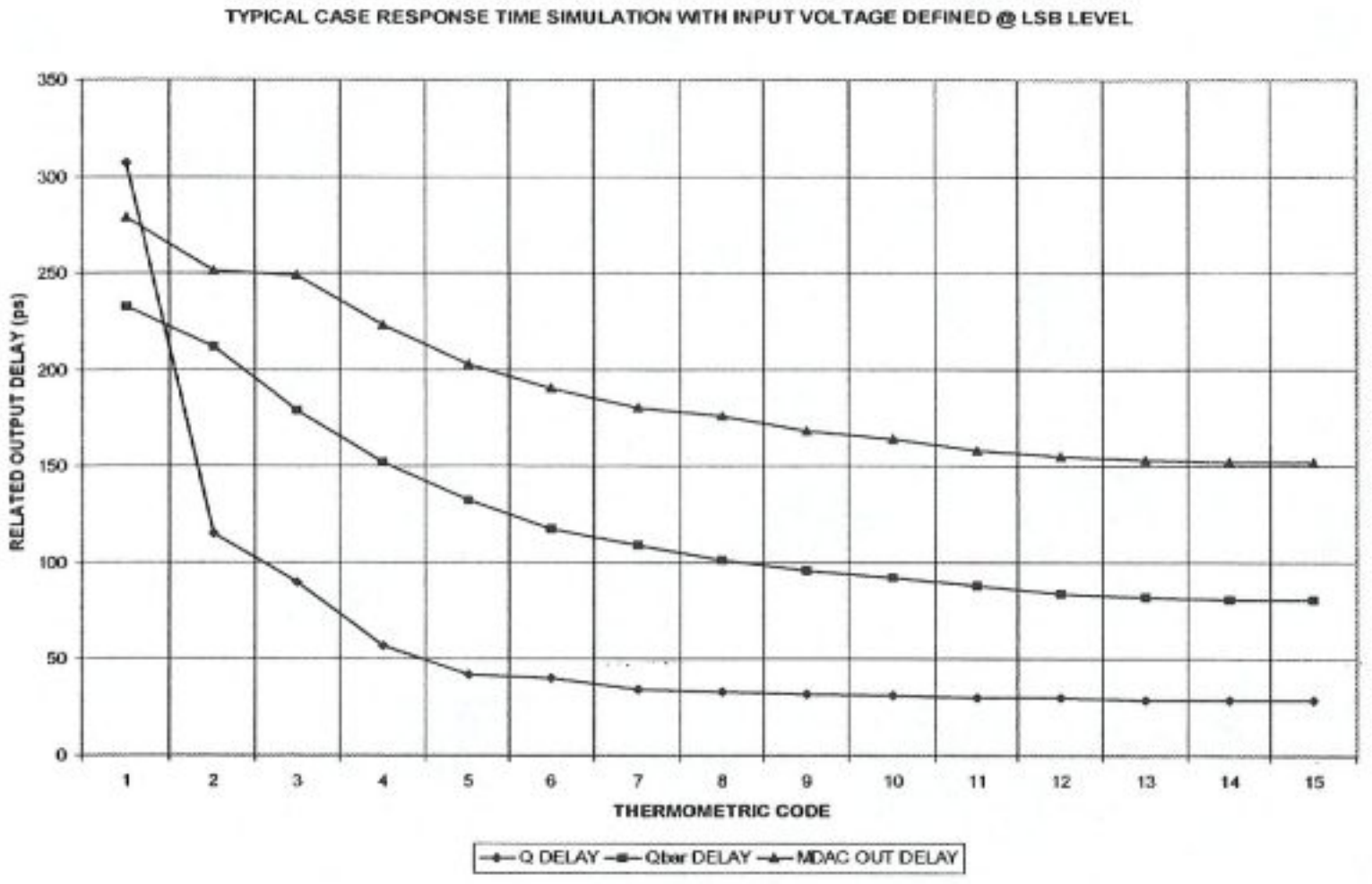


Figure 4.44 Response times obtained for input voltage at LSB level, typical corner and pMOS input stage transistors with mismatch.

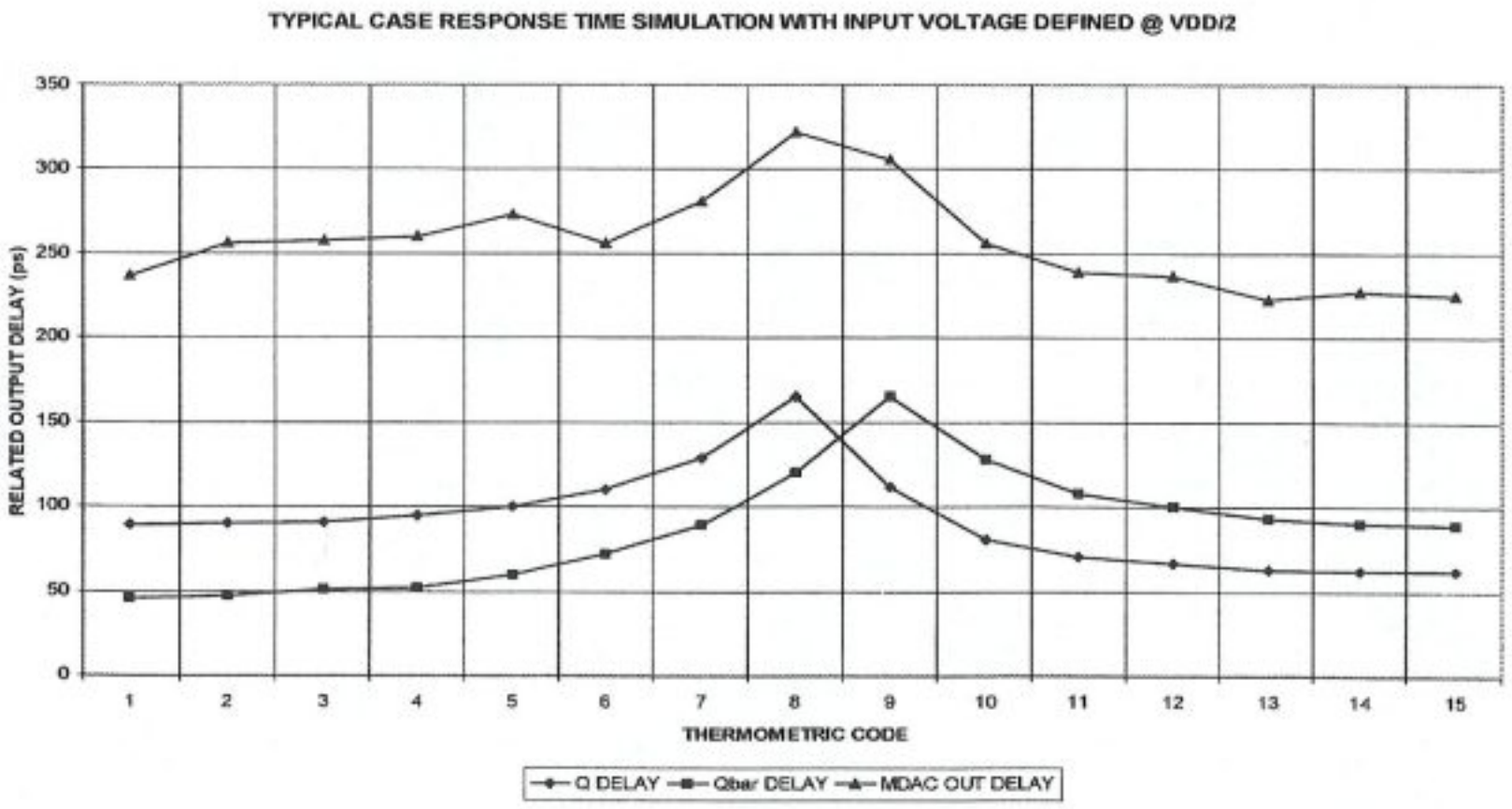


Figure 4.45 Response times obtained for input voltage at $V_{full\_scale}/2$ level, typical corner and nMOS input stage transistors with mismatch.

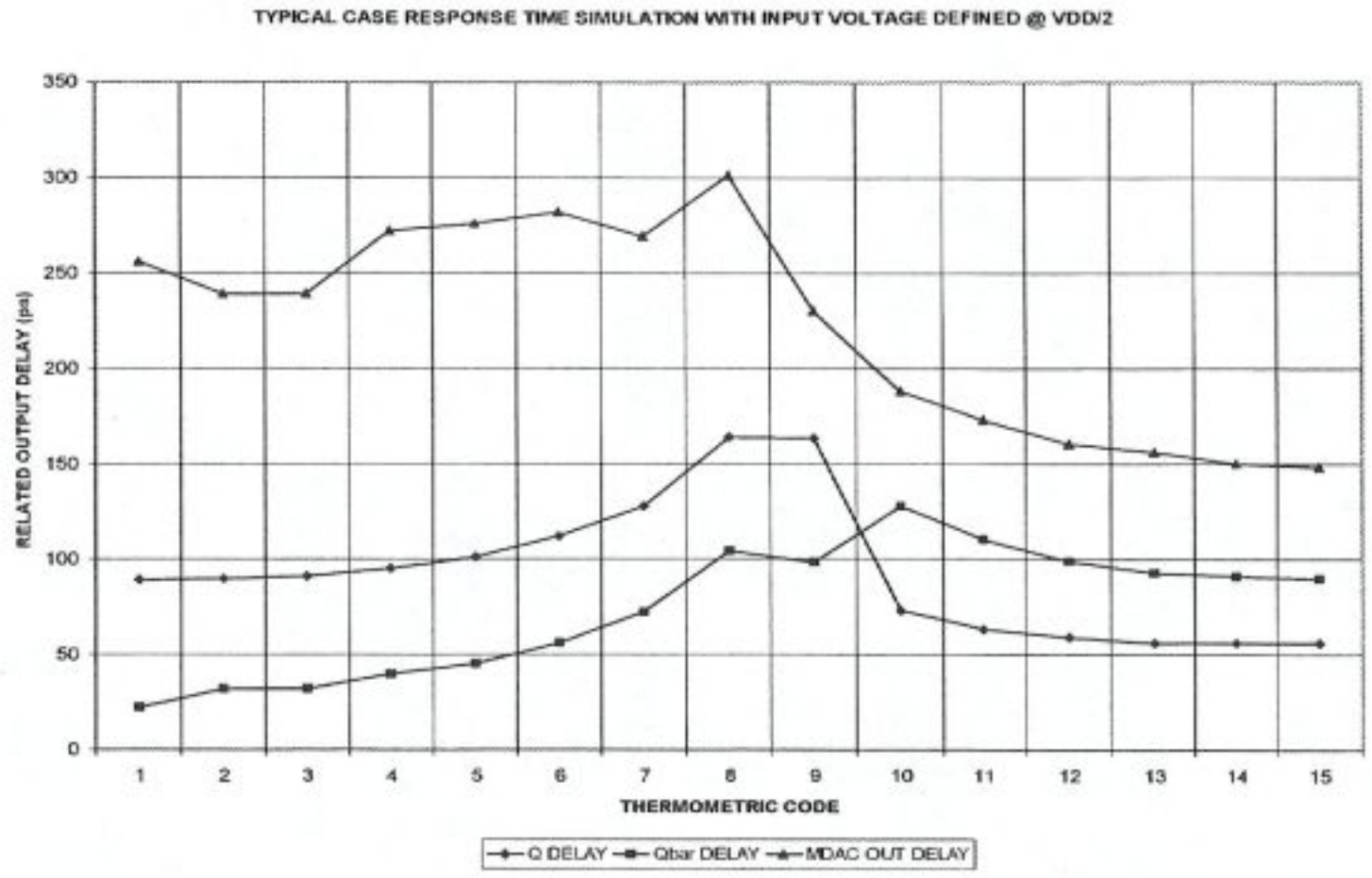


Figure 4.46 Response times obtained for input voltage at $V_{full\_scale}/2$ level, typical corner and pMOS input stage transistors with mismatch.

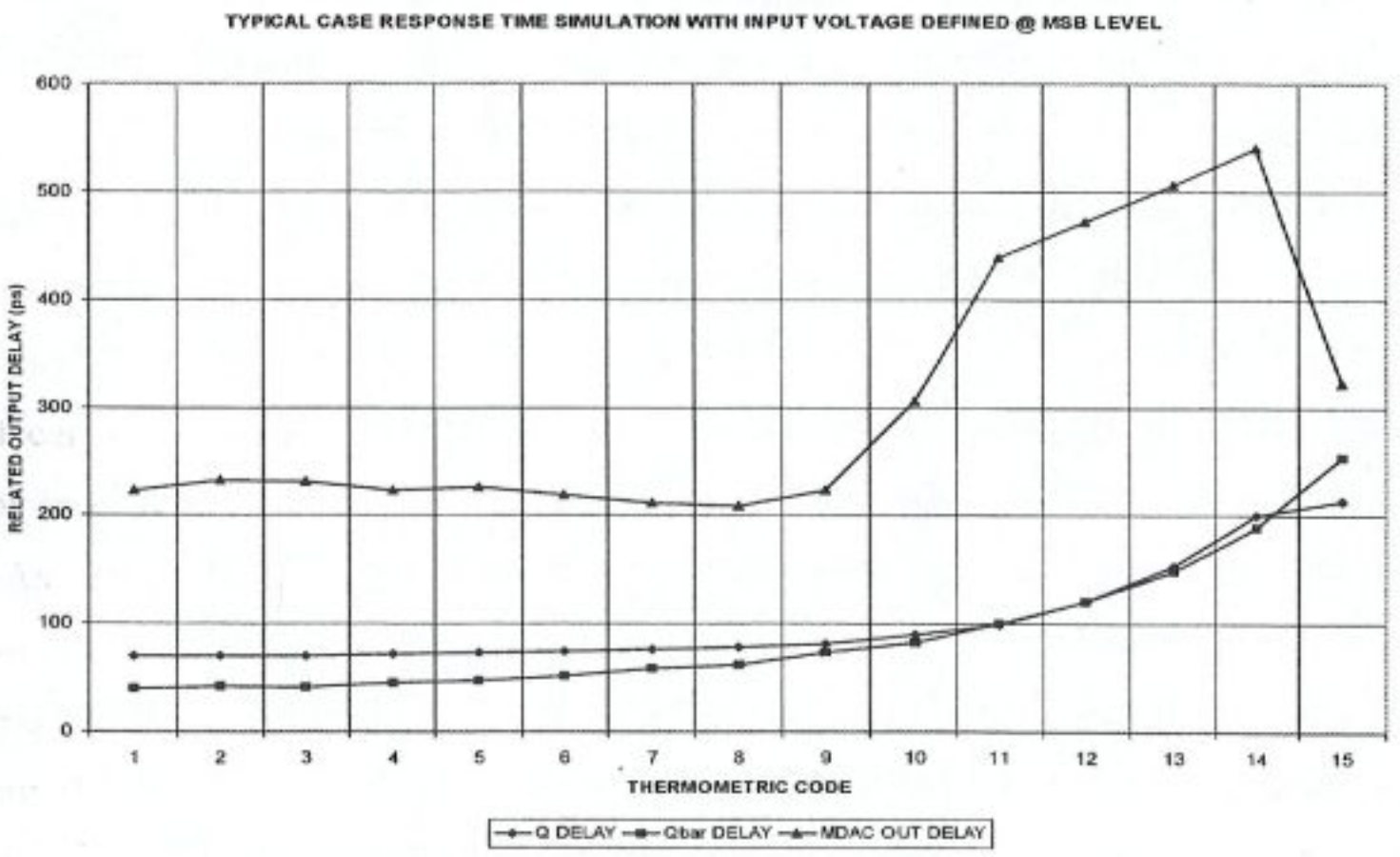


Figure 4.47 Response times obtained for input voltage at MSB level, typical corner and nMOS input stage transistors with mismatch.

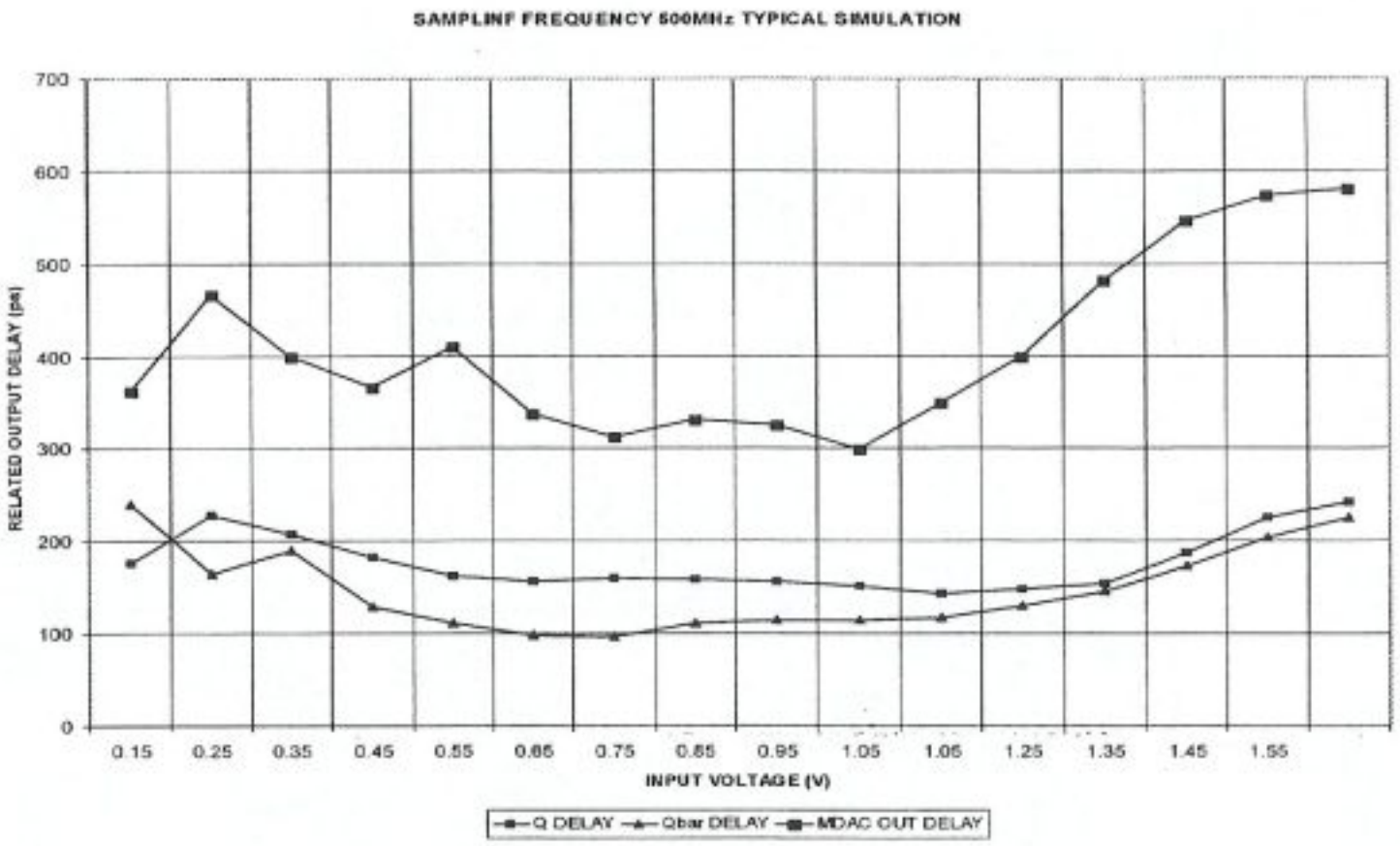


Figure 4.48 Response times obtained for typical corner simulations for 500MHz clock frequency.

From Figure 4.48 to 4.50 the influence of clock frequency can be seen on response time for the improved complementary voltage comparator circuit. Increasing the clock frequency does not result in a significant deterioration of response times. Thus applications are found out to be feasible up to 1 GHz of clock frequency.

With these characteristics, the proposed voltage comparator structure emerges as a good candidate for high-speed Flash A/D converter applications where accuracy and response speed are crucial. In addition, the improved full complementary comparator circuit can utilize the entire power supply range as its dynamic input voltage range, thereby improving its noise performance.

As can be seen from the characteristics given above, the dynamic power dissipation of the basic and improved comparator circuits was also simulated in detail, since power consumption typically represents one of the most important limitations. The only significant power dissipation was observed during the reset phase, when the cross-coupled latch circuit is forced to operate at inversion threshold. When the clock signal switches to zero, the circuit quickly reaches its stable

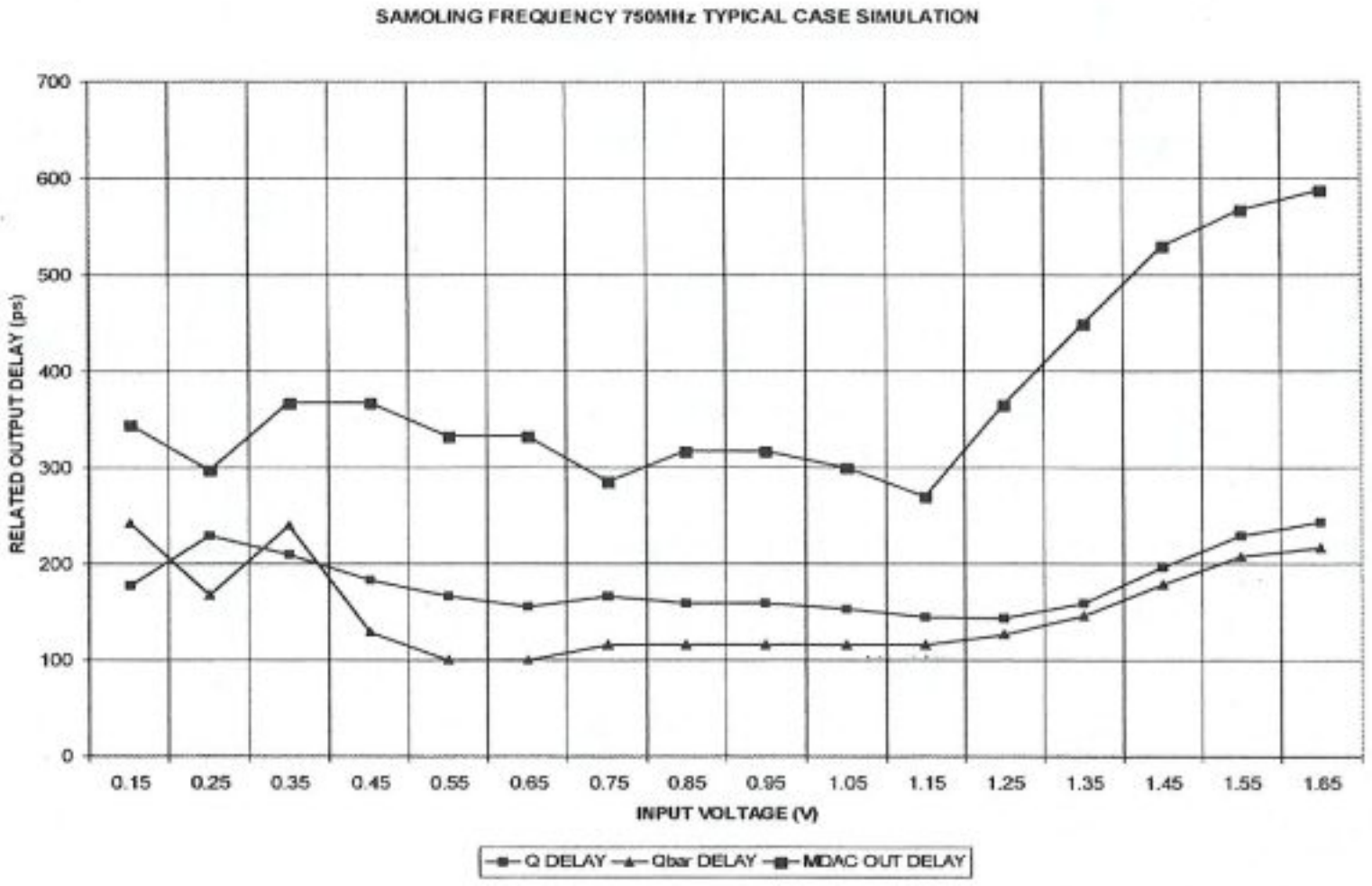


Figure 4.49 Response times obtained for typical corner simulations for 750MHz clock frequency.

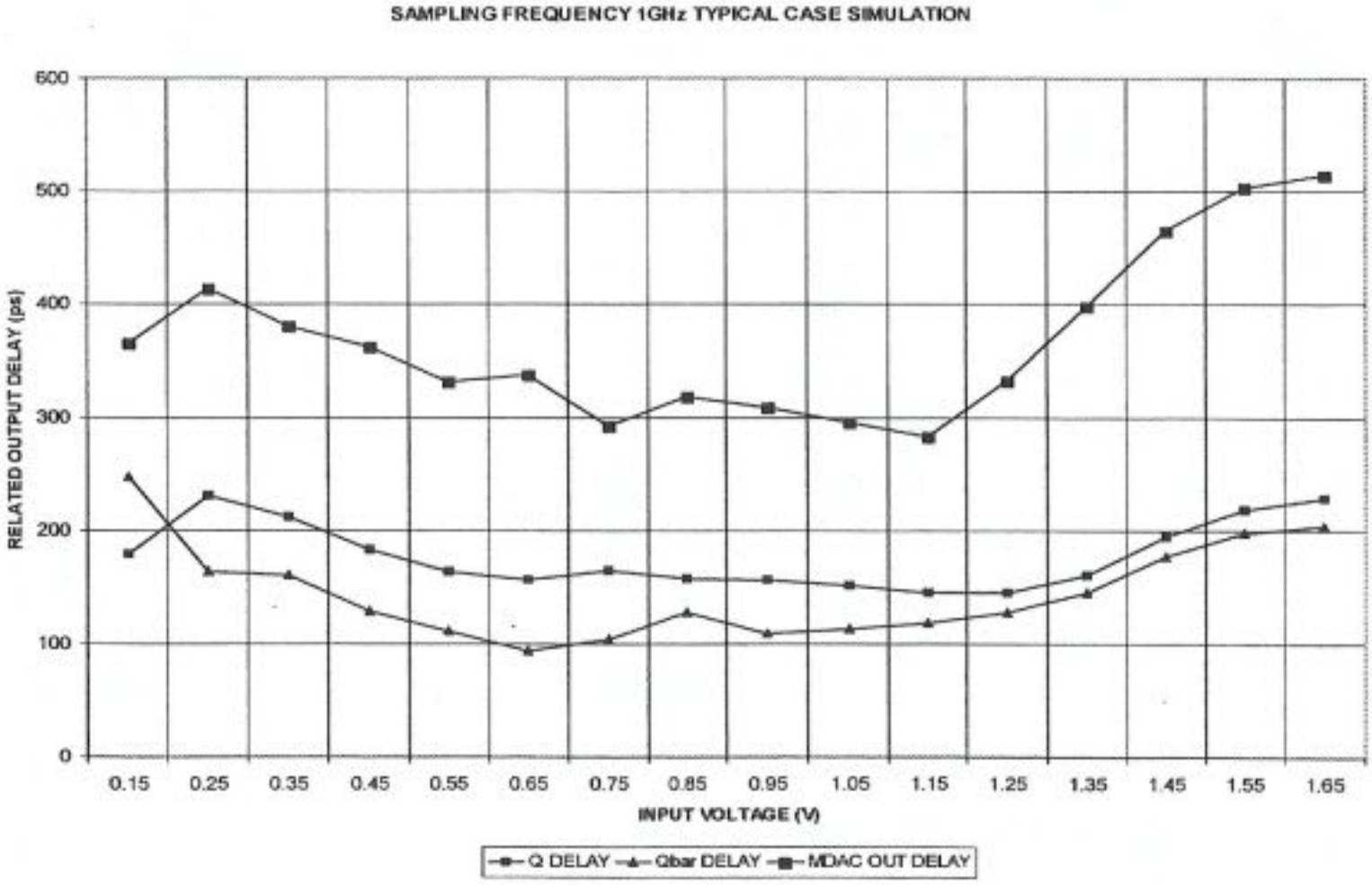


Figure 4.50 Response times obtained for typical corner simulations for 1GHz clock frequency.

decision state and it ceases to conduct current. In terms of power dissipation, the basic voltage comparator circuit is expected to perform better than the improved complementary-in version, since the current path during the reset phase is defined only by M6 and M7 in the basic comparator circuit topology. By contrast, the improved complementary voltage comparator circuit draws a larger amount of current from the power supply because the cross-coupled latch and the external pull-up / pull-down transistors are biased at inversion threshold (saturation current) during the reset phase.

Finally, worst case response times observed at the output nodes of the converters are plotted in Figure 4.51, as a function of the input voltage level, simulated at a clock frequency of 200MHz.

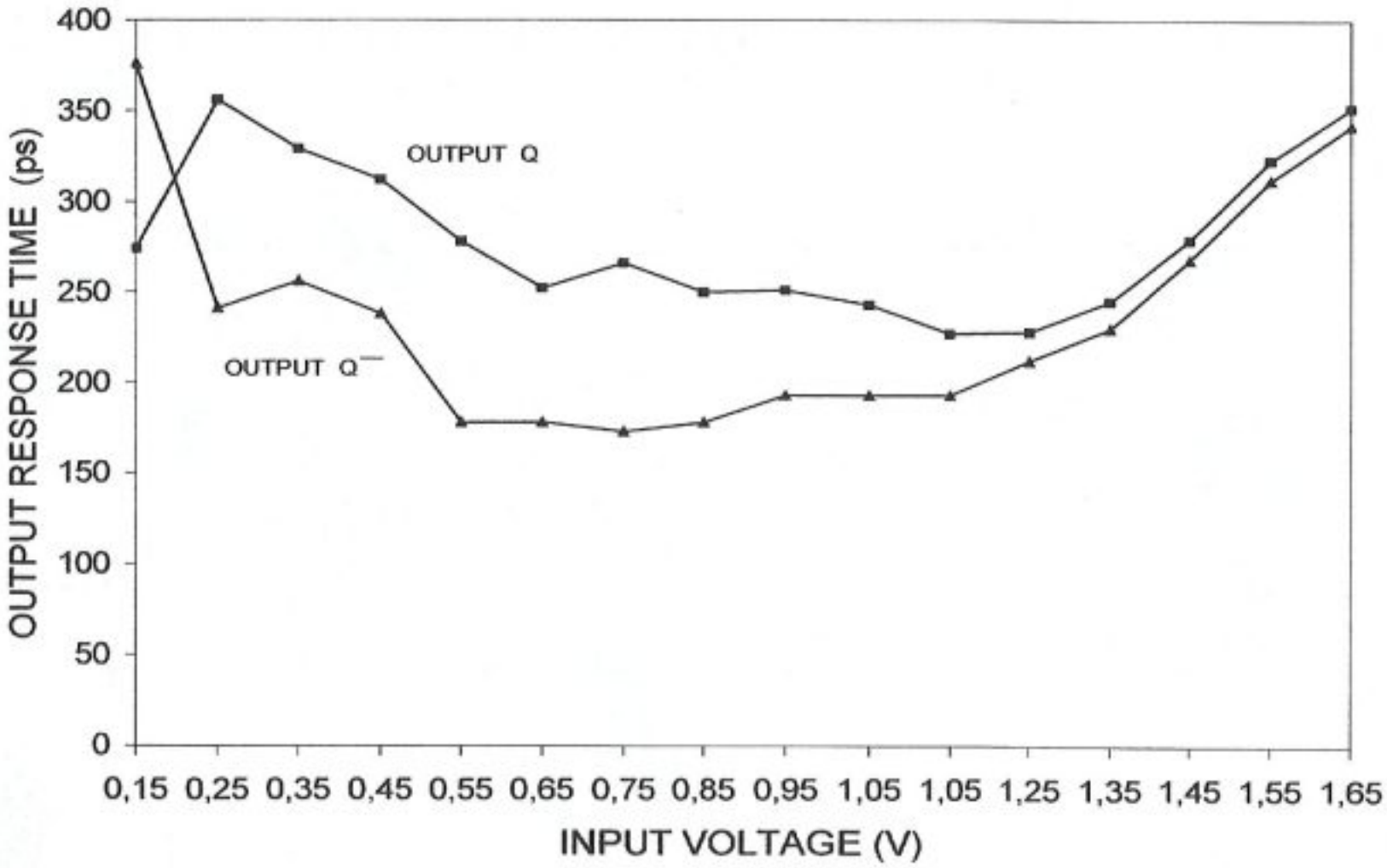


Figure 4.51 Worst-case response time vs. input voltage in a simulated 4-bit flash ADC.

Figure 4.52 shows the simulated average power dissipation of the two comparator circuits (basic comparator vs. improved complementary comparator), as a function of the sampling frequency. It is observed that the basic voltage comparator dissipates significantly less power compared to the improved version of the circuit. Still the average power dissipation of the improved complementary-in comparator remains at

about 0.8mW for 200 MHz sampling frequency, and increases to about 1.2mW only at 1 GHz sampling frequency.

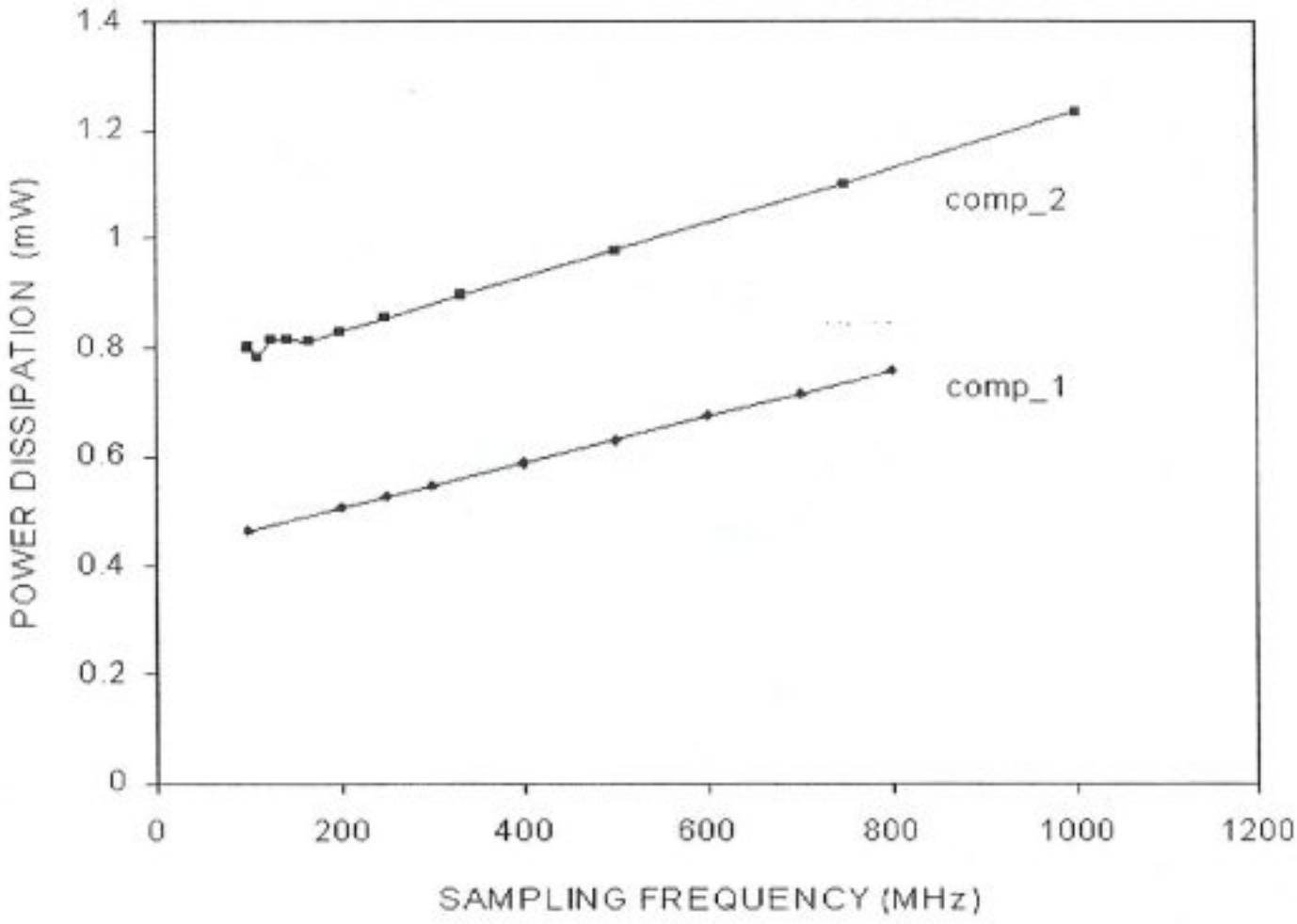


Figure 4.52 Average power dissipation of the comparator circuits vs. sampling frequency.

The integral non-linearity (INL) and differential non-linearity (DNL) error worst case values remain within ± 0.1 LSB for this 4-bit flash application (typically $< \pm 0.01$ LSB), due to the fact that the maximum offset does not exceed 10 mV. Three corner simulations were done to clarify the performance measures such as INL and DNL. Typical corner simulation results can be seen in the graphs provided.

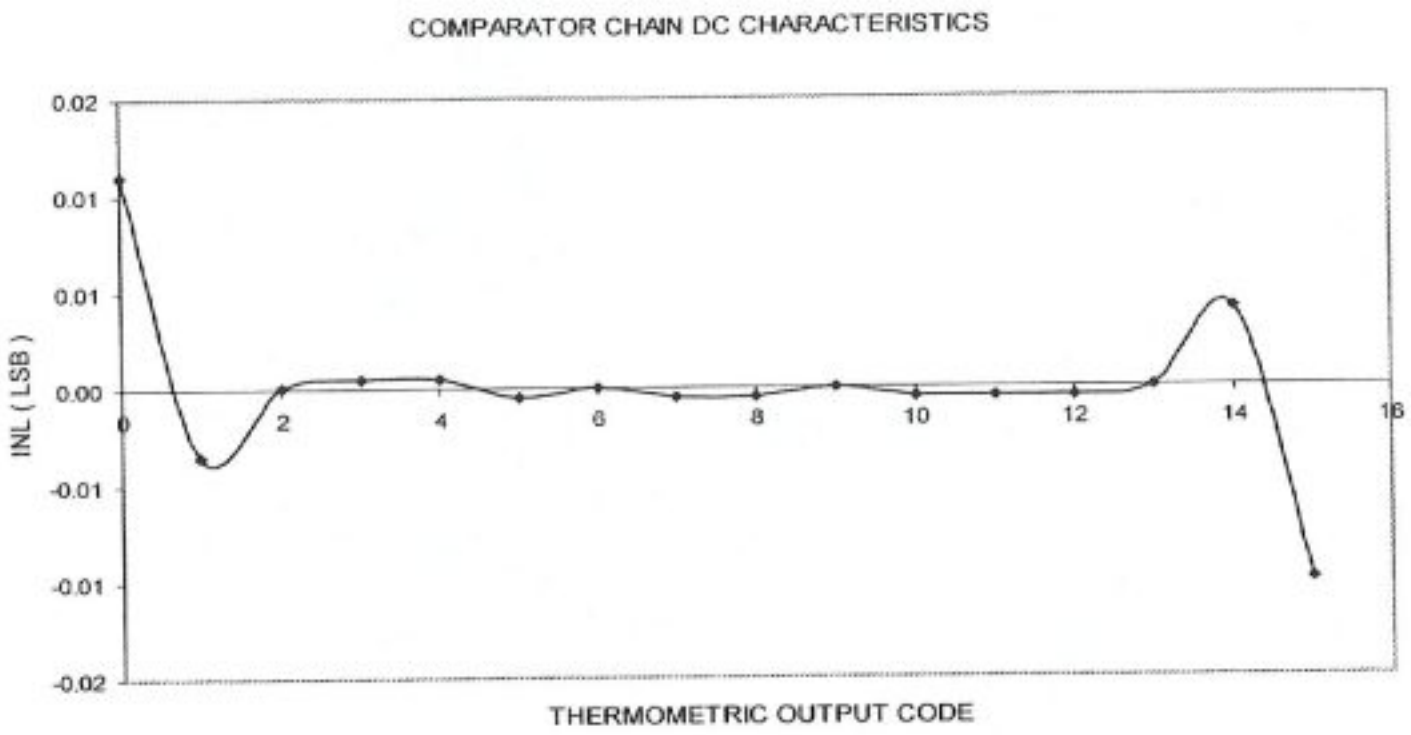


Figure 4.53 Integral non-linearity obtained with improved full complementary comparator for typical simulation corner.

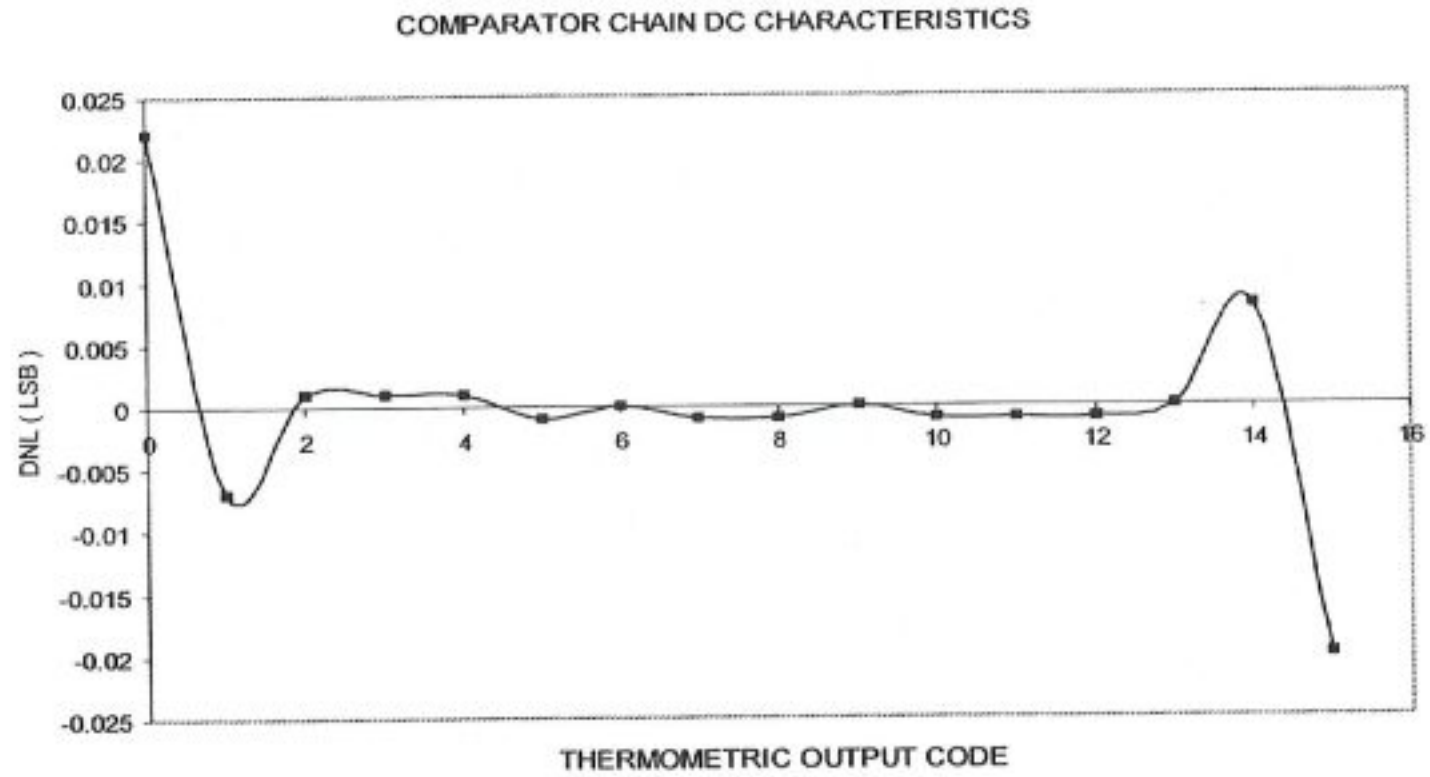


Figure 4.54 Differential non-linearity obtained with improved full complementary comparator for typical simulation corner.

Both INL and DNL graphs obtained for the comparator chain shows peak values at the first and last thermometer codes because of the input related offset of the first and last components of the comparator chain.

4.4.4 Low Power Version of the Complementary Comparator

After determining how much power is dissipated by the improved complementary comparator circuit we decided to find a low-power solution without changing any of the response speed, input-offset and simplicity of the topology.

As already mentioned in the previous section, significant part of power dissipation was observed during the reset phase because of the cross-coupled latch and the external pull-up / pull-down transistors which were implemented in the topology to further improve the response speed. As a result response time and power consumed are two trade-offs of our voltage comparator design.

Response speed being one of the most critical design specification of flash A/D converters and also our A/D converter, which will work at 200 MHz, we do not want to give up the response times we reached. By contrast we also do not want to consume that much power. So, to further reduce the power consumption of the improved complementary comparator circuit we propose the low power version that includes four additional transistors implemented in the output stage to latch the decision levels during the reset mode, which in return lowers the power dissipated. The low power version of the improved comparator circuit is given in Figure 4.55.

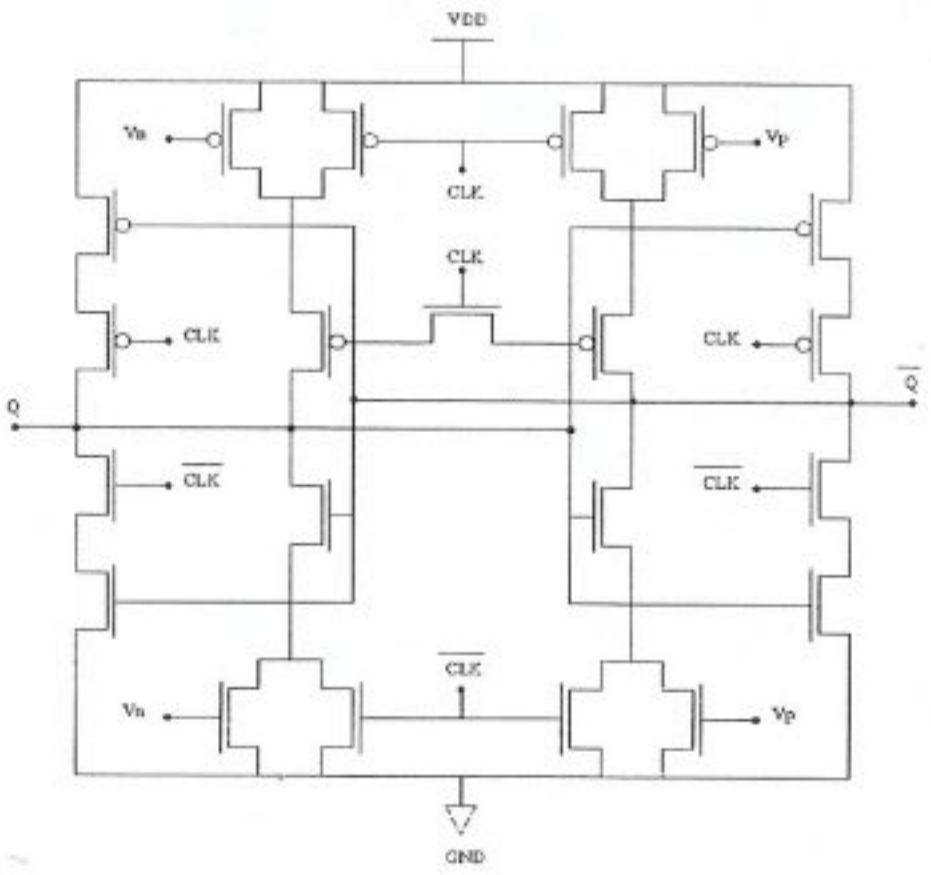


Figure 4.55 Comparator circuit with latched output stage during reset mode (Low power comparator version.)

The latching pMOS transistors are enabled with the clock signal and nMOS transistors with its complementary. During reset phase (while CLK is HIGH) the output is in latch state so that the outputs stay at their previous decision levels. Because there does not exist any DC path for current in this mode, the output stage of the voltage comparator does not consume any power during reset phase. After reset phase in which CLK is LOW, evaluation phase is entered and all the latching MOS transistors are turned-on and a new decision is made within very small time interval.

By the simulations done it is found out that power consumption of the improved complementary version is halved in this low power version. But in return response times increase about 50 ps. The input offset is also increased due to the clock feedthrough from the latch transistors implemented. So we decided to use the improved full complementary version presented in Section 4.4.3 in our 12-bit pipelined A/D converter structure, despite the higher power dissipation.

5. ARCHITECTURE COMPONENTS: HIGH-SPEED OP-AMP DESIGN

5.1 Introduction of Basic Concepts

An important analog building block, especially in data-converter systems, is the sample-and-hold circuit. Before proceeding, it is worthwhile to mention that sample-and-hold circuits are also referred to as "track-and-hold" circuits. Normally, these two terms are synonymous except for a few switched-capacitor sample-and-hold circuits that do not have a phase where the output signal is tracking the input signal. Sample-and-hold circuits are necessary components in many data-acquisition systems such as A/D converters. In many cases, the use of sample and hold (at the front of the data converter) can greatly minimise errors due to slightly different delays times in the internal operation of the converter [2].

Before discussing the basic principles of sample-and-hold circuits, it is necessary to mention some performance parameters used in characterisation.

- The first of these parameters is a sampling *pedestal* or a *hold step*. This is an error that occurs each time a sample and hold goes from sample mode to hold mode. During this change in operation, there is always a small error in the voltage being held that makes it different from the input voltage at the time of sampling. Obviously, this error should be as small as possible. Perhaps more importantly, this error should be signal independent; otherwise it can introduce nonlinear distortion (Figure 5.1).

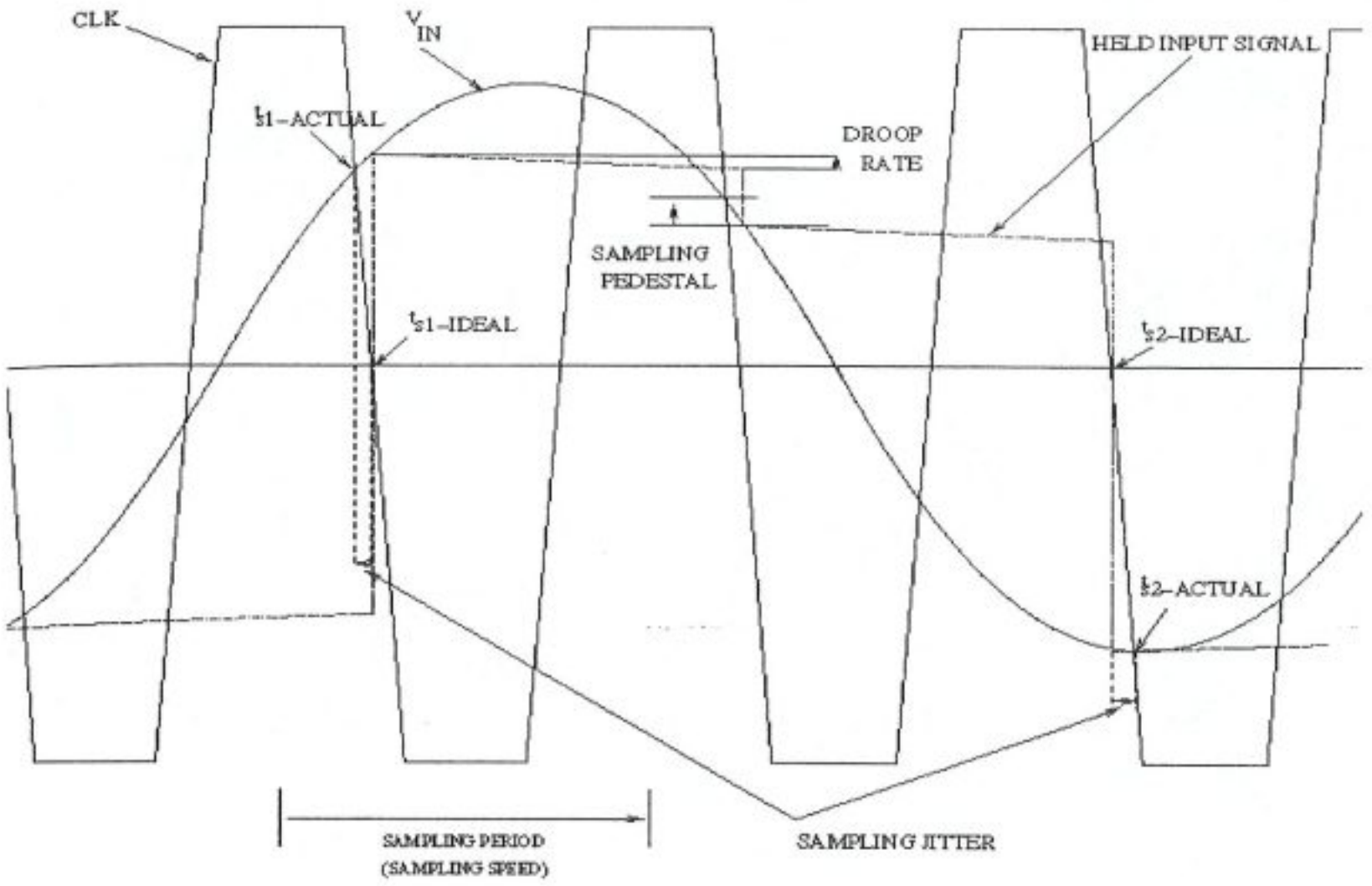


Figure 5.1 Input and output waveforms of a conventional sample-and-hold amplifier illustrating some errors possible.

- Another parameter is a measure of how isolated the sampled signal from the input signal during hold mode. Ideally, the output voltage will no longer be affected by changes in the input voltage. In reality, there is always some signal feedthrough, usually through parasitic capacitive coupling from the input to the output. In well-designed sample and holds, the signal feedthrough can be greatly minimised.
- A third important parameter is the speed at which a sample and hold can track the input signal, when in sample mode. In this mode, a sample and hold will have both small-signal and large-signal limitations due to its –3dB bandwidth and finite slew rate, respectively. Both –3dB bandwidth and slew rate should be maximised for high-speed operations (Figure 5.1).
- Yet another limitation (somewhat less important in high-speed designs) is the *droop rate* in hold mode. This error is a slow change in output voltage, when in hold mode, caused by effects such as leakage currents due to the finite base

currents of bipolar transistors and reversed-biased junctions. In most CMOS designs, this droop rate is so small it can be often be ignored (Figure 5.1).

- A fifth limitation is *aperture time uncertainty*. This error is the result of the effective sampling time changing from one sampling instance to the next and becomes more pronounced for high-speed signals. Specifically, when high-speed signals are being sampled, the input signal changes rapidly, resulting in small amounts of aperture uncertainty causing the held voltage to be significantly different from the ideal held voltage (Figure 5.1) [2].

Other performance parameters are also important when realizing sample and hold circuits. These include parameters such as dynamic range, linearity, gain, and offset error.

Operational amplifiers (op-amps), being the heart of the sample-and-hold circuits, will be examined deeply here after. In addition to the classic sample-and-hold function, a pipelined A/D converter architecture also requires fast and accurate amplification of the residue signal at the end of each pipeline stage. Again, a highly linear op-amp with small offset and high slew rate is preferred for this function.

We loosely define an op-amp as a "high-gain differential amplifier". By "high" we mean a value that is adequate for the application, typically in the range of 10^1 to 10^5. Since op-amps are usually employed to implement a feedback system, their open-loop gain is chosen according to the precision required of the closed-loop circuit.

Up to two decades ago, op-amps were designed to serve as "general-purpose" building blocks, satisfying the requirements of many different applications. Such efforts brought to create an "ideal" op-amp with very high voltage gain (several hundred thousand), high input impedance and low output impedance, but at the cost of many other aspects of the performance, eg., speed, output voltage swing, and power dissipation.

By contrast, today's op-amp design proceeds with the recognition that the trade-offs between parameters eventually require a multi-dimensional compromise in the overall implementation, making it necessary to know the adequate value that must be achieved for each parameter. For example, if the speed is critical while the gain error is not, a topology is chosen that favours the former, possibly sacrificing the later.

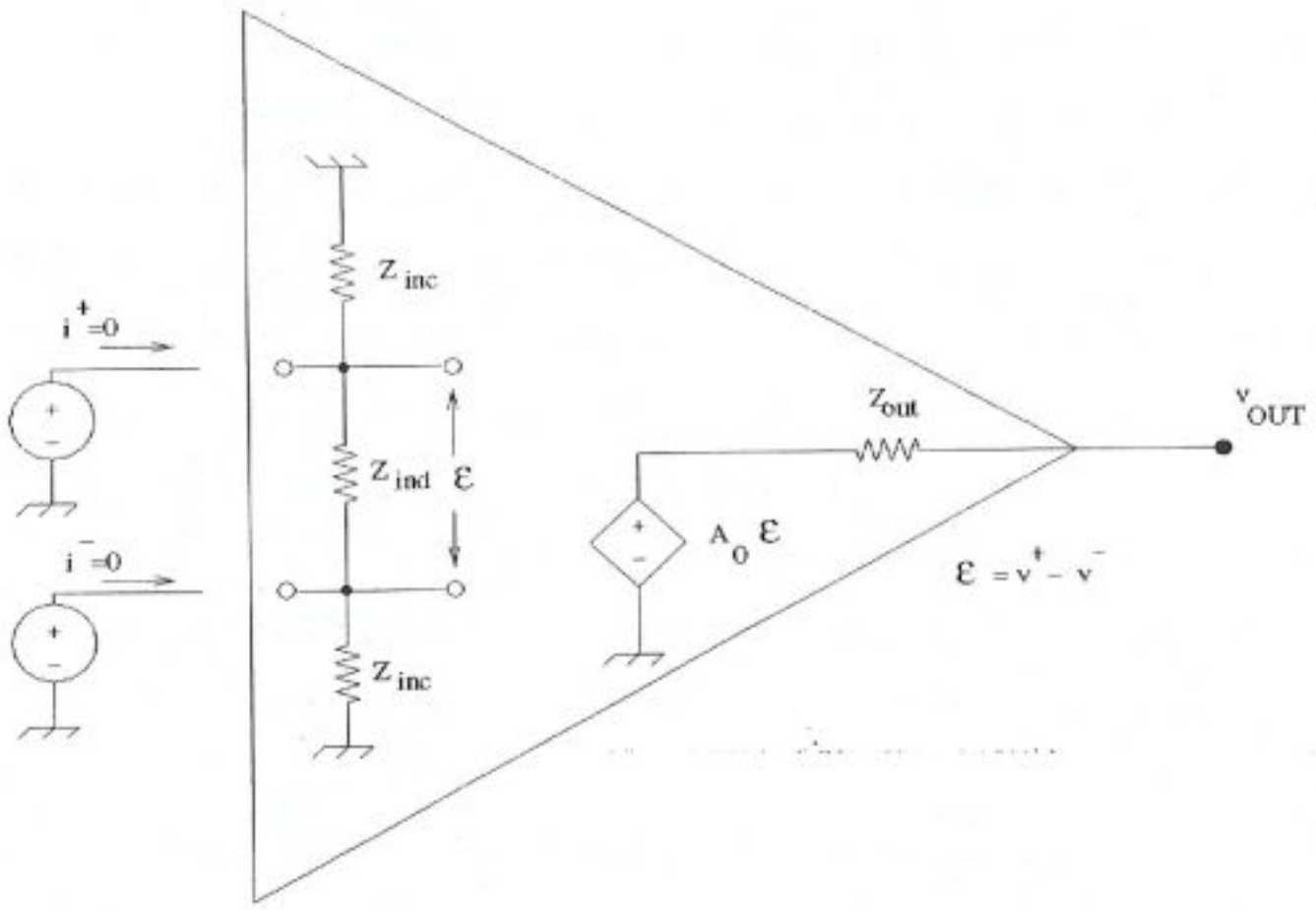


Figure 5.2 Behavioral model for ideal differential input, single-ended output op-amp[1].

Ideally, an op-amp has infinite differential voltage-gain, infinite input resistance, and zero output resistance as shown in Figure 5.2. In practice, the operational amplifier only approaches the ideal characteristics. Some of its other non-ideal characteristics are illustrated in Figure 5.3. The finite differential-input impedance is modelled by R_{id} and C_{id}. The output resistance is modelled by R_{out}. The common-mode input resistances are given as resistances of R_{icm} connected from each of the input to ground. V_{os} is the input-offset voltage necessary to make the output voltage zero if both the inputs of the op-amp are grounded.

I_{os} (not shown) is the input-offset current, which is necessary to make the output voltage zero if the op-amp is driven from two identical current sources. Therefore, I_{os} is defined as the magnitude of the difference between the two input-bias currents I_{B1} and I_{B2}. Since the bias currents for a CMOS op-amp are approximately zero, the offset current is also zero. The common-mode rejection ratio (CMRR) is modelled by the voltage controlled voltage source indicated as V_1/CMRR. This source approximately models the effects of common-mode input signal on the effects of common-mode input signal on the op-amp. The two sources designated as $\overline{e_n}^2$ and $\overline{I_n}^2$ are used to model the

op-amp noise. These are voltage- and current-noise spectral densities with units of mean square volts and mean square amperes, respectively [3].

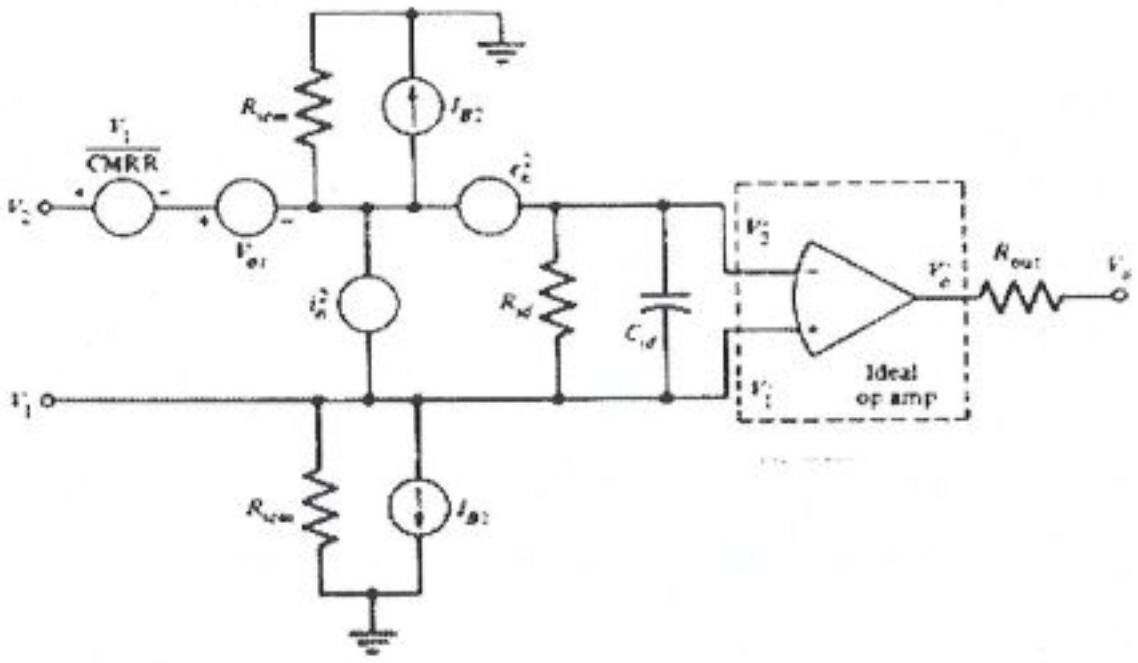


Figure 5.3 A model for an ideal op-amp showing some of the nonideal characteristics [3].

Not all of the non-ideal characteristics of the op-amp are shown in Figure 5.3 [6]. Other pertinent characteristics of the op-amp will now be defined. The output voltage of Figure 5.2 can be defined as

$$V_{out}(s) = Av(s)\left[V^{+}(s) - V^{-}(s)\right] + Ac(s)\left[\frac{V^{+}(s) + V^{-}(s)}{2}\right] \tag{5.1}$$

where the first term on the right is the differential portion of Vout(s) and the second term is the common-mode portion of the Vout(s). The differential-frequency response is given as $A_v(s)$ while the common-mode frequency response is given as $A_c(s)$. A typical differential-frequency response of an op-amp is given as

$$Av(s) = \frac{Av_0}{\left(s/p_1 - 1\right)\left(s/p_2 - 1\right).....} \tag{5.3}$$

where p_1, p_2.... are poles of the operational amplifier (op-amp) open-loop transfer function. In general, a pole designated as p_i can be expressed as

$$p_i = -w_i \tag{5.4}$$

where w_i is the reciprocal time constant or break-frequency of the pole p_i. While the op-amp transfer function may have zeros, they will be ignored now. A_{v0} or A_v (0) is the gain of the op-amp as the frequency approaches zero. Figure 5.4 shows a typical frequency response of the magnitude of $A_v(s)$. In this case we see that w_1 is much lower than the rest of the break-frequencies causing w_1 to be the dominant influence in the frequency response. The frequency where the –6dB/oct slope from the dominant pole intersects with the 0dB axis is designated as the *unity-gain bandwidth*, abbreviated GB, or GBW, of the op-amp.

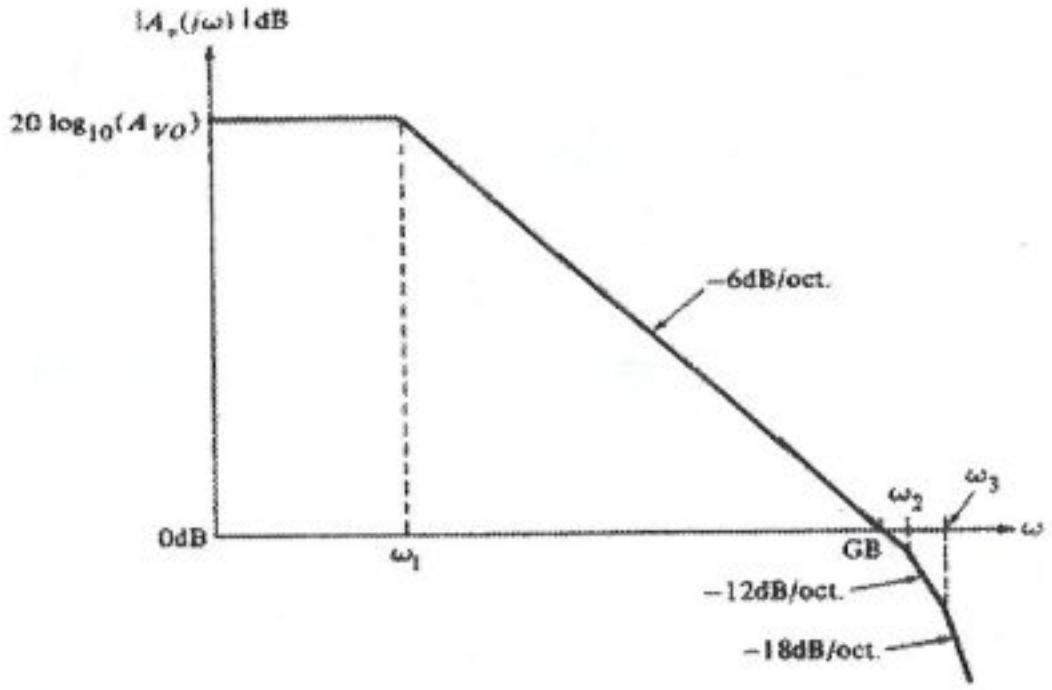


Figure 5.4 Typical frequency response for an op-amp [3].

Other non-ideal characteristics of the op-amp not defined by Figure 5.3 include the power-supply rejection ratio, PSRR. The PSRR is defined as the product of the ratio of the output voltage of the op-amp caused by the change in power supply and the open-loop gain of the op-amp. Thus,

$$PSRR = \frac{\Delta V_{DD}}{\Delta V_{out}} * A_v(s) = \frac{\left.\frac{V_o}{V_{in}}\right|_{V_{DD}=0}}{\left.\frac{V_o}{V_{DD}}\right|_{V_{in}=0}} \tag{5.5}$$

The common-mode input range is the voltage range over which the input common-mode signal can vary. Typically, this range is several volts less than V_{DD} and several volts more than V_{SS}.

The output of the op-amp has several important limits, one of which is the maximum output current sourcing and sinking capability. There is a limited range over which the output voltage can swing while still maintaining high-gain characteristics. The output also has a voltage rate limit called *slew rate*. The slew rate is generally determined by the maximum current available to charge or discharge a capacitance. Normally slew rate is not limited by the output, but by the current-sourcing capability of the first stage. The last characteristic of importance in analog sampled-data circuit applications is the *settling time*. This is the time needed the output of the op-amp to reach a final value (to within a predetermined tolerance) when excited by a small signal. This is not to be confused with slew rate, which is large-signal phenomenon. Many times, the output response of an op-amp is a combination of both large- and small-signal characteristics. Small-signal settling time can be completely determined from the location of the poles and zeros in the small-signal equivalent circuit whereas slew rate is determined from the large signal conditions of the circuit.

The importance of the settling time to analog sampled-data circuits is illustrated by Figure 5.4. It is necessary to wait until the amplifier has settled to within a few tenths of a percent of its final value in order to avoid errors in the accuracy of the processing analog circuits. A longer settling time implies that the rate of the processing analog signal must be reduced.

Fortunately the CMOS op-amp does not suffer from all of the nonideal characteristics previously discussed. Because of the extremely high input resistance of the MOS devices, both R_{id} and I_{os} are of no importance. A typical value of R_{id} is in the range of 10^{14} ohms. Also R_{icm} is extremely large and can be ignored.

Before the actual design of an op-amp can begin, though, one must set out all of the requirements and boundary conditions that will be used to guide the design. The fundemental boundray conditions and specifications are listed below, in Table 5.1. Note

that the typical values (expected values) given here are intended for an op-amp that is designed using a single power supply (1.8 V), and that should be capable of handling tasks such as high-speed sampling and amplification (at frequencies above 200 MHz) while driving a relatively small on-chip capacitive load. The design trade-offs that are involved for the realization of the indicated specifications are also listed in Table 5.1, emphasizing the fact that the improvement of one particular specification is usally dependent on other parameters that must be sacrificed.

- Boundary conditions:
  - * Process specifications (V_T, K', C_{ox}, etc.)
  - * Supply voltage range
  - * Supply current range
  - * Operating temperature and range.

Specifications	Typical Requirements	Trades-off with
Gain	$\geq$ 70 dB	Linearity, PSRR
Gain Bandwidth	$\geq$ 500 MHz	SR, Offset
Settling Time	$\leq$ 1 ns	SR, GBW
Slew Rate	$\geq$ 1 V / ns	GBW, Settling time
Input CMR	$\geq \pm$ 0.4 V	
CMRR	$\geq$ 60 dB	
PSRR	$\geq$ 60 dB	
Output Swing	$\geq$ 1.4 V_{pp}	Noise, Settling time, GBW, SR
Output Resistance	$\geq$ 100 MΩ	Output-voltage swing
Offset	$\leq \pm$ 10 mV	Gain, GBW
Noise	$\leq$ 100 nV / $\sqrt{Hz}$ at 1 KHz	Output-voltage swing
Layout area	$\leq$ 120.000 μm^2	Gain

Table 5.1 Typical specifications of a CMOS op-amp.

5.2 OTA Based Op-Amp Design Flow

An operational transconductance amplifier (OTA) given in Figure 5.5, also called a transconductance element or a transconductor, is a device that translates voltage inputs to current outputs, such that $i_{out} = G_m v_{IN}$. Recently, OTAs have emerged as compelling alternatives to conventional op-amps in the realisation of fully integrated continuos-time active filters. Part of the interest in OTAs stems from their relative simplicity in comparison to a standard op-amp circuits. For example, CMOS OTAs are single stage circuits, essentially comprised of a simple differential stage. Hence, at high frequencies where large excess phase significantly degrades the performance of a conventional op-amp, a properly designed OTA can still maintain near ideal behaviour.

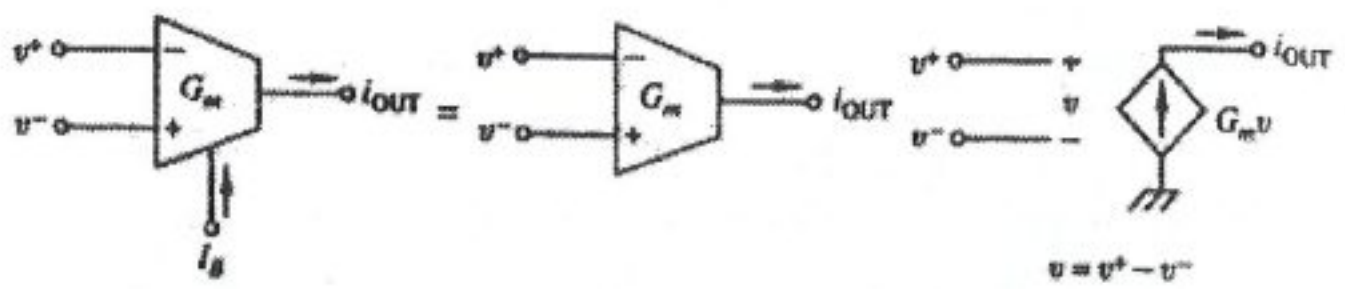


Figure 5.5 The differential OTA symbol and ideal model [1].

An OTA has a large open-loop output resistance at low frequencies. Its gain is characterised by a transconductance G_m that can be quite large.

Manual analysis of a symmetrical CMOS OTA will be examined in detail in the following paragraphs.

The circuit schematic of the CMOS OTA with symmetrical input stage is given in Figure 5.6. The differential pair is formed by input transistors M1 and M2. They drive their output currents in two transistors, M3 and M4, which are connected as diodes. They are the inputs of two current mirrors with current multiplication factor B. Typical values are B = 1 to 3. The output current of transistor M5 (see Figure 5.6) is then mirrored once more in current mirror M7, M8, with B = 1, as indicated [1].

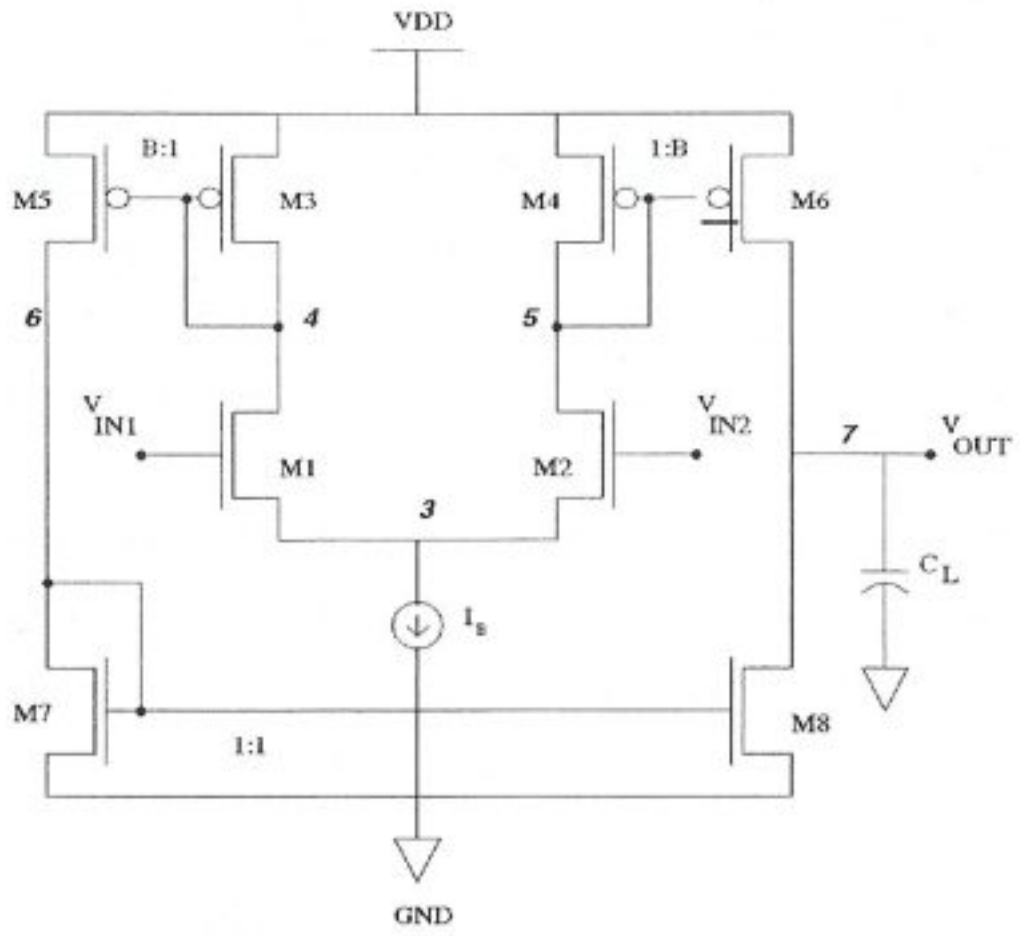


Figure 5.6 Symmetrical CMOS OTA schematic [1].

Gain of the symmetrical CMOS OTA: At nodes 4, 5, and 6, a diode connected MOS is driven by a current source. A diode connected MOS represents only a small signal resistance of $1/g_m$, whereas the current source has an output resistance r_o, which is much higher than $1/g_m$. As a result, at each of these nodes, the small-signal resistance with respect to ground is quite small, ie. $1/g_m$.

The small–signal resistance is high only at the output node 7. It is formed by the two output resistances of r_{o6} and r_{o8} in parallel. For equal values of $r_{o6} = r_{o8}$, output resistance R_{OUT} equals $r_{o6}/2$. On the other hand, the transconductance of symmetrical OTA is Bg_{m1}.

The voltage gain A_v is then given by multiplication of transconductance and R_{OUT}, or by Eq. 5.6.

$$A_v = B \times g_{m1} \times R_{OUT} = \sqrt{\frac{2K_n'}{I_B}\left(\frac{W}{L}\right)_1} \times (r_{o6} // r_{o8}) \qquad (5.6)$$

Note that factor B is not present in the expression of the gain A_v. The transconductance increase B times whereas R_{OUT} decreases B times. The voltage gain A_v can thus be increased by increasing r_{o6} or r_{o8}. With this additional degree of freedom, the output resistance R_{OUT} and the voltage gain A_v can be increased without effecting OTAs transconductance.

Up until this point, the total gain A_v of the OTA has been considered. The gain of the first stage A_{v1} alone is also important as well, as it determines the noise performance of the OTA. It is given by the ratio of $(v_5 - v_4) / v_{IN1}$, if v_{IN2} is grounded. It is found by inspection to be

$$A_{v1} = \frac{g_{m1}}{g_{m3}} = \sqrt{\frac{K_n'}{K_p'}}\sqrt{\frac{(W/L)_1}{(W/L)_3}} \tag{5.7}$$

For the noise purposes, we must ensure that the noise of the input stage is dominant over the noise of the output transistors referred to the input. Therefore, the gain must be larger than unity, ie. the gain must have a minimum value of three, the reasons for which will be explained shortly [1].

GBW of the symmetrical CMOS OTA: The values of the dominant and nondominant poles can be determined as well as the value of the GBW (Gain Bandwidth). There exist more nondominant poles than a simple OTA because of the higher number of signal carrying nodes. They must be shifted to sufficiently high frequencies in order to ensure a phase margin (PM) of more then 60°.

The dominant pole f_d is evidently realised at node 7, which exhibits the highest resistance, ie. R_{OUT}. Its value is given by

$$f_d = \frac{1}{2\pi R_{OUT}(C_{n7} + C_L)} \tag{5.8}$$

in which C_{n7} includes all parasitic capacitances connected to node 7, due to the OTA (see Figure 5.6). The value of GBW is given by

$$GBW = A_v f_d = \frac{Bg_{m1}}{2\pi(C_{n7} + C_L)} = B\frac{\sqrt{2K_n' I_B}}{2\pi}\frac{\sqrt{(W/L)_1}}{C_{n7} + C_L} \tag{5.9}$$

the value of GBW is increased by the design parameter B at the expense of more current consumption. In order to be able to effectively use this value of GBW, the nondominant poles are evaluated first. The calculation of phase margin will show that the factor of B can never be made large [1].

Phase margin (PM) of the symmetrical CMOS OTA: Nondominant poles occur at all other nodes, ie. at nodes 4, 5, and 6, due to the capacitances on these nodes. Nodes 4 and 5 carry small signals, which have the same amplitude but the opposite phase. Therefore, the poles at nodes 4 and 5 are the same. Together, they form one single nondominant pole f_{nd5}. It is found by inspection and is given by

$$f_{nd5} \approx \frac{g_{m4}}{2\pi C_{n5}} = \frac{\sqrt{2K_p' I_B}}{2\pi}\frac{\sqrt{(W/L)_4}}{C_{n5}} \tag{5.10}$$

The other nondominant pole occurs at node 6, ie. f_{nd6}, but acts on only half of the output signal. Indeed, only the current flowing in M3, M5, M7, and M8 is subject to this pole. A thorough analysis shows that, when a pole acts on only half of the signal, a zero must be added at twice the frequency. A pole-zero doublet is thus created. This pole is again found by inspection an is given by

$$f_{nd6} \approx \frac{g_{m7}}{2\pi C_{n6}} = \frac{\sqrt{2K_n' I_B}}{2\pi}\frac{\sqrt{B(W/L)_7}}{C_{n6}} \tag{5.11}$$

$$f_{z6} = 2f_{nd6}$$

The value of phase margin is given in Eq. 5.12.

$$PM = 90^{\circ} - \varphi_{n5} - \varphi_{n6}$$

$$where\,\varphi_{n5} = \arctan BA_{v1}\frac{C_{n5}}{C_L + C_{n7}} \tag{5.12}$$

$$and\,\varphi_{n6} = \arctan\sqrt{\frac{B\left(W/L\right)_1}{\left(W/L\right)_7}}\frac{C_{n6}}{C_L + C_{n7}} - \arctan\frac{1}{2}\sqrt{\frac{B\left(W/L\right)_1}{\left(W/L\right)_7}}\frac{C_{n6}}{C_L + C_{n7}}$$

It can be noted that the phase margin can be increased by

* decreasing node capacitances C_{n5} and C_{n6}
* decreasing B
* increasing $\left(W/L\right)_7$

provided we keep $A_{v1}$and C_L constant.

It is not acceptable to decrease B too much. Factor B is normally increased to increase the slew rate (to be explained later). A good compromise is B = 3. For a given C_L, this leaves us thus only $\left(W/L\right)_7$ to adjust in order to ensure sufficient phase margin. However, the phase margin is not very sensitive to $\left(W/L\right)_7$ because φ_{n6} is only a weak function of $\left(W/L\right)_7$ [1].

Slew rate: Slew rate of a symmetrical CMOS OTA is determined by the load capacitance C_L. The current available to charge this capacitance is BI_B, thus, the slew rate can be given as in Eq. 5.13.

$$SR = B\frac{I_B}{C_L + C_{n7}} \tag{5.13}$$

Factor B can be used to increase the slew rate of the symmetrical CMOS OTA in the excess of current consumption determined as (1+B) I_B [1].

Noise performance: The total output noise voltage power $\overline{d\,v_{out}^2}$ is the sum of the equivalent input noise voltage powers $\overline{d\,v_{in}^2}$ of each transistor, multiplied by their gain squared. The equivalent input noise voltage power $\overline{d\,v_{in}^2}$ then obtained by division of the total gain squared. Excess noise *y* is the normalised total equivalent input noise to equivalent input noise of one of the input transistors can be given as in Eq.5.14.

$$y = 2\left\{1+\frac{1}{A_{v1}}\left[1+\frac{1}{B}\left(1+\sqrt{\frac{K_n'\left(W/L\right)_7}{K_p'\left(W/L\right)_5}}\right)\right]\right\} \tag{5.14}$$

The total equivalent input noise can thus be reduced to the equivalent input noise of only the two transistors provided the gain of the first stage A_{v1} is large. Since this implies lower stability, as shown in Eq. 5.12, a compromise is taken for A_{v1}, such as three to five. Increasing B helps, but it also reduces the phase margin, thus a good compromise for B is one to three.

We need to convert current output of the symmetrical CMOS OTA into voltage thus, we used an inverter with a feedback resistor and a Miller compensation capacitance placed between input and output nodes of that inverter. Manual analysis of this inverter will be examined here after [1].

5.3 Inverter-Based Output Stage Frequency Analysis

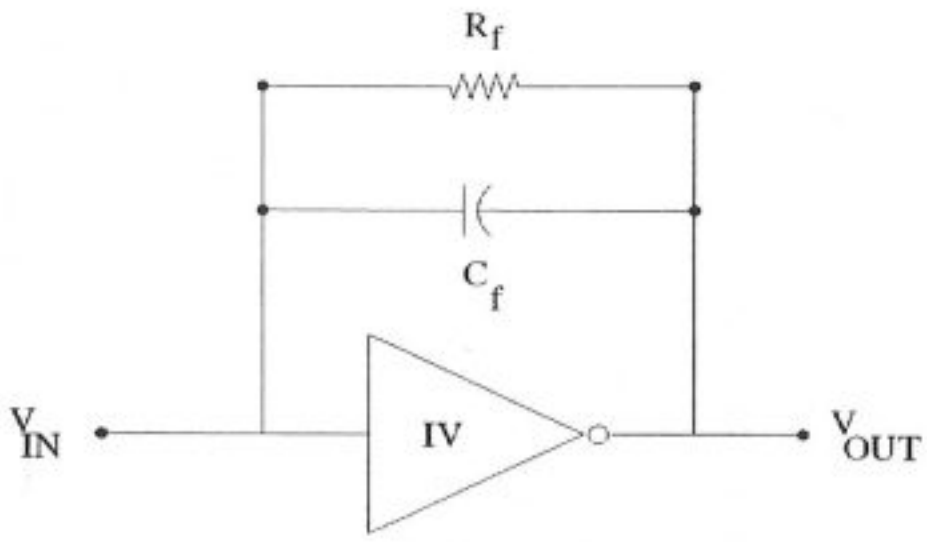


Figure 5.7 Inverter-based output stage schematic.

We use a CMOS inverter as given in Figure 5.7 in order to convert the current output of the symmetrical CMOS OTA in to voltage output. An inverter topology was choosen in order to have rail-to-rail output swing that is essential for both the sample-

and-hold and residue amplifiers. Simplicity of the topology, easily obtained high gain, almost rail-to-rail input and output swing properties were the leading specialities of such an architecture. A feedback resistor is used to establish analog output in between the input node and output nodes of inverter, which will degrade the inverters operational characteristics considerably. Using a feedback resistor between input and output of an inverter will obviously decrease the voltage gain, but still sufficient enough for our purpose. Frequency response of such a circuit will be examined here after.

Miller compensation is also used for enough phase margin thus the circuit will be simplified into a two pole system with the help of Miller conversion. Small signal equivalent of the inverter given in Figure 5.7 can be seen in Figure 5.8. Manual analysis will be carried on this schematic now on. We used *Miller theorem* in order to derive the poles and zeros of the inverter based output stage. (Figure 5.9)

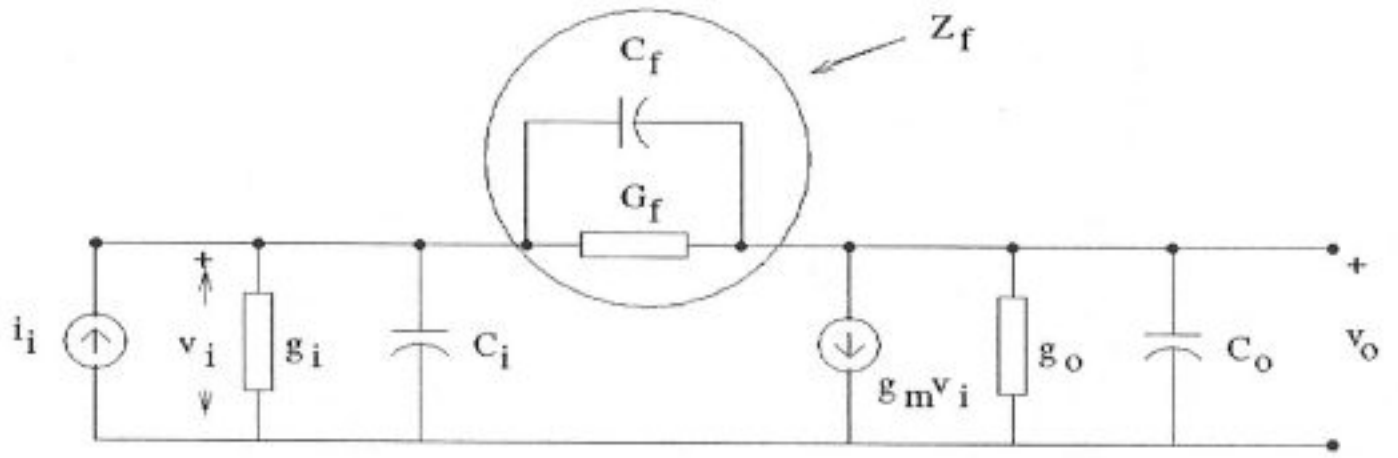


Figure 5.8 Simplified small signal equivalent of the inverter [26].

By simply writing the RC equivalents of both independent parts in Figure 5.9, poles and zeros can be found out. From the input part

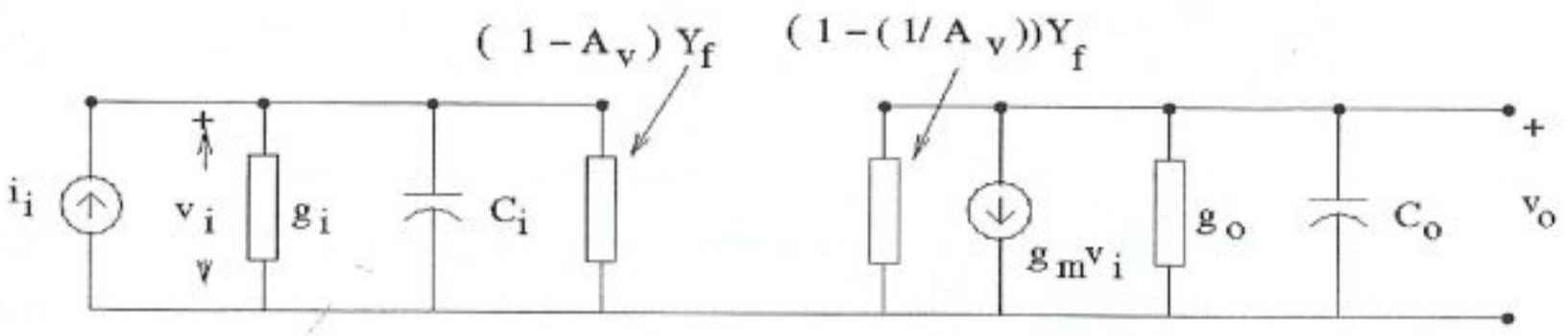


Figure 5.9 Equivalent circuit of Figure 5.8 [26].

$$z_1 = \frac{-1}{\frac{R_f}{1-A_V}\left(C_i + \frac{C_f}{1-A_v}\right)}$$

$$z_1 = \frac{-\left(\frac{R_f}{1-A_v} + R_i\right)}{R_i \frac{R_f}{1-A_v}\left(C_i + \frac{C_f}{1-A_v}\right)} \tag{5.15}$$

From the second part we obtain:

$$z_2 = \frac{r_o + \left(\frac{R_f}{1-\frac{1}{A_v}}\right)}{\left[C_o + \left(\frac{C_f}{1-\frac{1}{A_v}}\right)\right]\left[ro\frac{R_f}{1-\frac{1}{A_v}}\right]} \tag{5.16}$$

Thus it is proved out that the inverter with feedback resistance and capacitor gives two poles and one zero in the frequency domain.

After deriving out the AC characteristics of such an inverter used in a feedback architecture, we found out that the op-amp formed by symmetrical OTA cascaded to an inverter has five poles and two seros. Special care must be taken for stability issues in the required bandwidth.

5.4 OTA Based High-Gain Op-Amp Design

An op-amp with high open loop gain, high slew rate, small input / output offset, highly linear and stable for a very wide frequency range is needed for amplifiying the residue voltage in each pipeline stage.

This op-amp will be used in a negative feedback with a feedback gain of eight (refer to Chapter 6). Absolute value of the feedback gain is so critical that it could effect

directly the INL, DNL of the over all analog-to-digital converter. Applied resistive feedback will result in a closed loop gain of

$$A_v = \frac{A_{v0}}{1 + \beta A_{v0}} \tag{5.17}$$

where β is the loop gain and A_{v0} is the open loop gain of the op-amp. Eq. 5.17 can easily be simplfied as $1/\beta$ if A_{v0} is sufficiently large. Otherwise there will arise amplifying gain error inevitably that will result in degradation in converter performance directly. High slew rate is essential in high-speed pipeline A/D converters because the amplified residue will be used as the analog input signal for the proceeeding pipeline stage. Thus, it has to settle to a specified – tolerable – range with in a very small period of time. Output offset has to be minimized, otherwise the value of the analog signal that will be processed in the next stage will totally be different from the analog signal formed in the preeceding pipeline stage from the residue. The op-amp will be used in a feedback loop, thus it has to be stable in a wide frequency range, at least satisfiying the Nyquist rate condition, in order to avoid any ringing or oscillation in application. What is more almost rail-to-rail output swing is also neccessary for an op-amp to be used as a residue amplifier, because out of this amplifier will be processed as the input analog signal, which represents the held analog input applied to the pipeline stage's input. If direct concatination of produced digital bits used to form the valid output of the A/D converter.

Consequently, we have to design an op-amp satisfiying all the specifications dictated above for an application at 200MHz sampling rate.

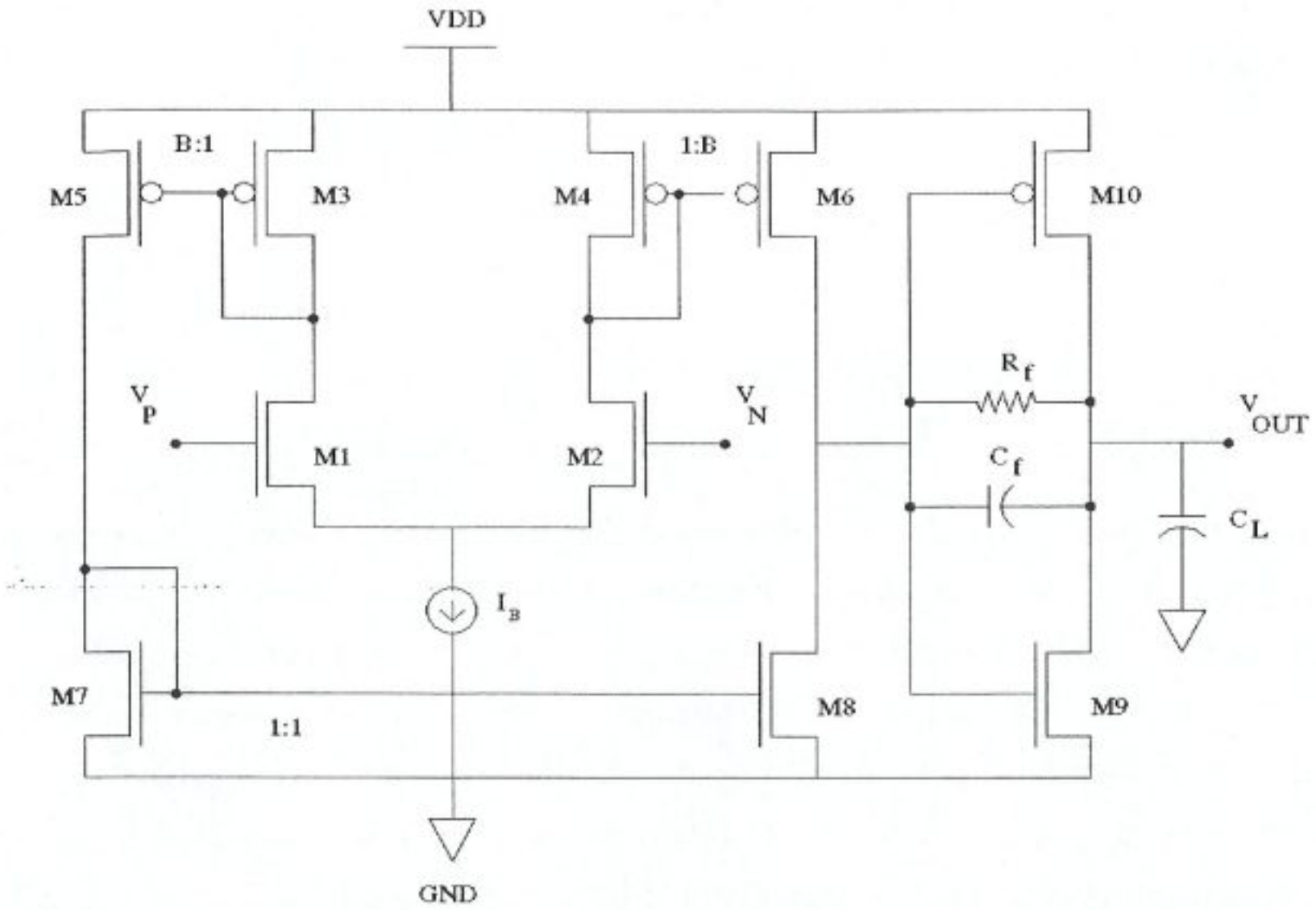


Figure 5.10 High open loop-gain OTA based op-amp schematic [26].

	W (μm)	*L(μm)*
M1	10	0.5
M2	10	0.5
M3	0.36	0.18
M4	0.36	0.18
M5	3.6	0.18
M6	3.6	0.18
M7	2	0.18
M8	2	0.18
M9	7.2	0.18
M10	18	0.18
R_f	75 kΩ	
C_f	50 fF	

Table 5.2 Aspect ratio table for high open loop-gain OTA.

The designed op-amp satisfies all the specification for a residue amplifier. But in unity gain configuration needed for sample-and-hold circuit, op-amp given in Figure 5.10 has stability problems because of the poor phase margin. In addition to poor stability, the unity gain configuration suffers from a limited output voltage swing due to the fact that the first stage OTA can only provide an output voltage that is limited by the amount of one threshold voltage from both rails. Thus, we decided to lower the open loop-gain to establish stability and use the op-amp in a configuration with a negative feedback gain of two, in order to overcome output swing limitation. We did not give up with using this high open loop-gain configuration because we also need a residue amplifier to achieve analog pipelining between two pipeline stages. This residue amplifier must be used in a configuration of feedback gain of 16 without error correction or 8 with error correction (refer to Chapter 6) for a 4-bit A/D pipeline stage. Stability problem of this topology is eliminated by using it in a feedback loop with high voltage gain that is a must in a residue amplifier. Simulation results are given for both DC and AC characteristics in Figure 5.11 to Figure 5.14.

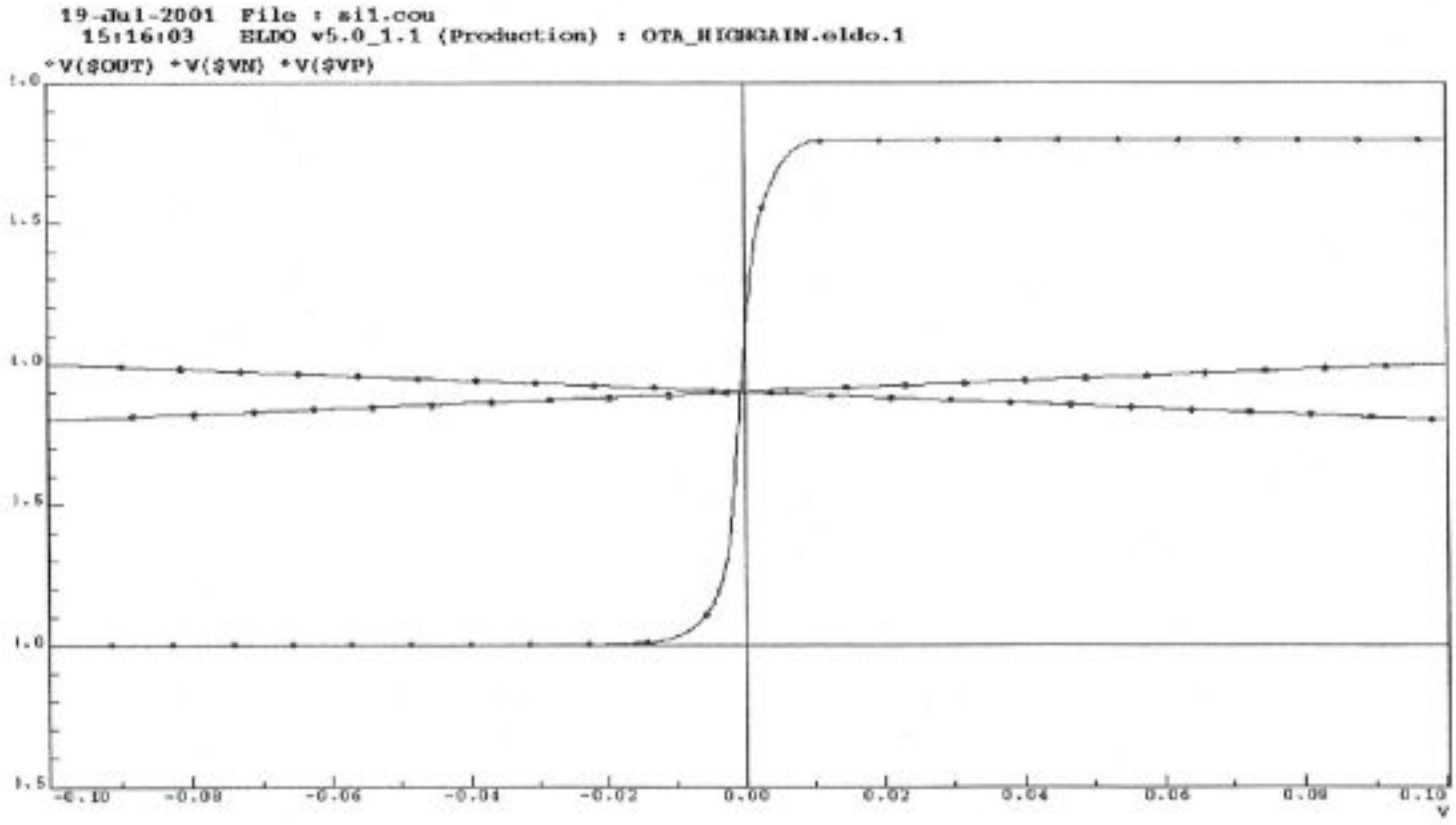


Figure 5.11 DC characteristics of high open loop gain OTA based op-amp.

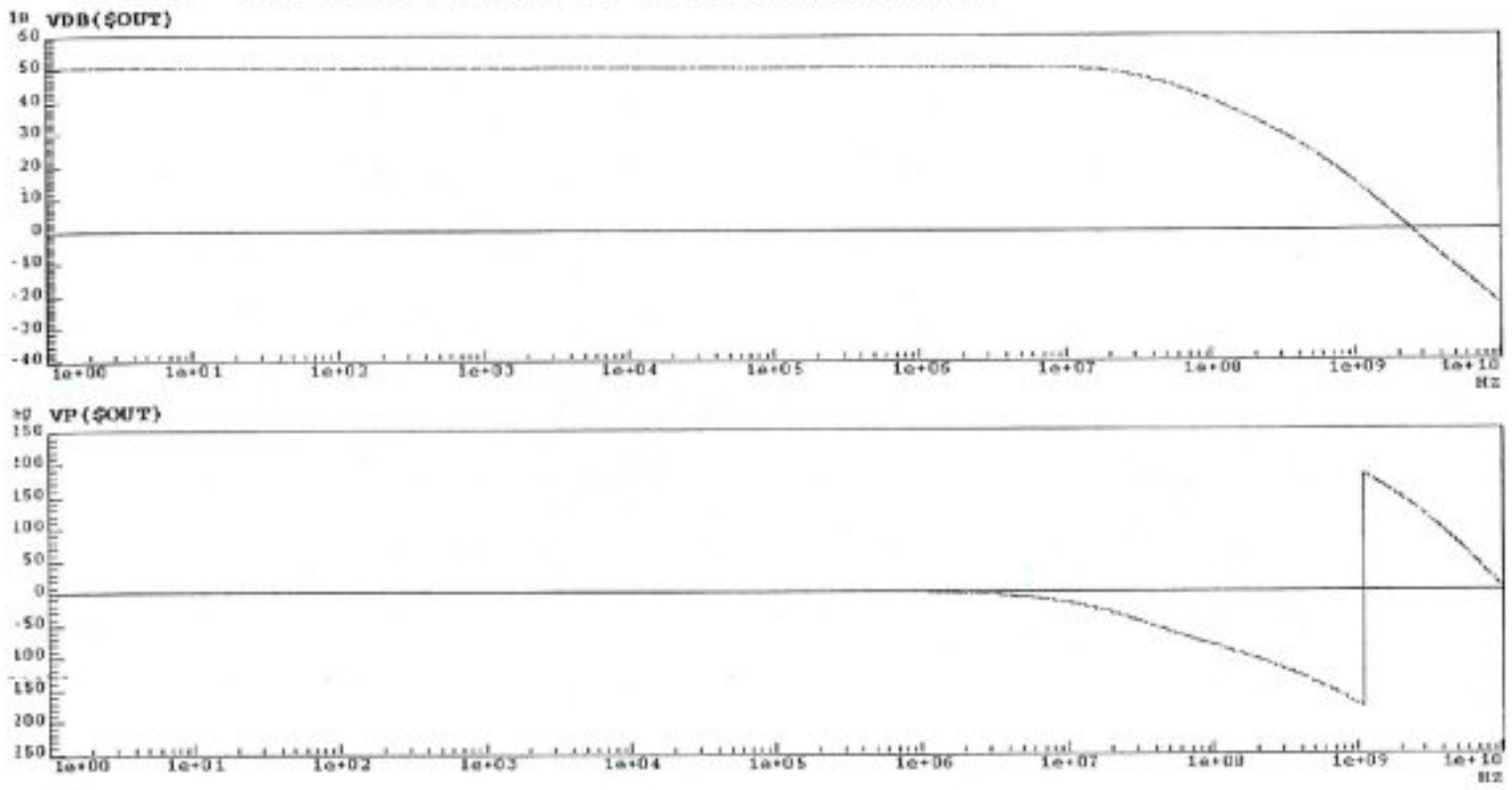


Figure 5.12 Open loop AC characteristics of high open loop gain OTA based op-amp.

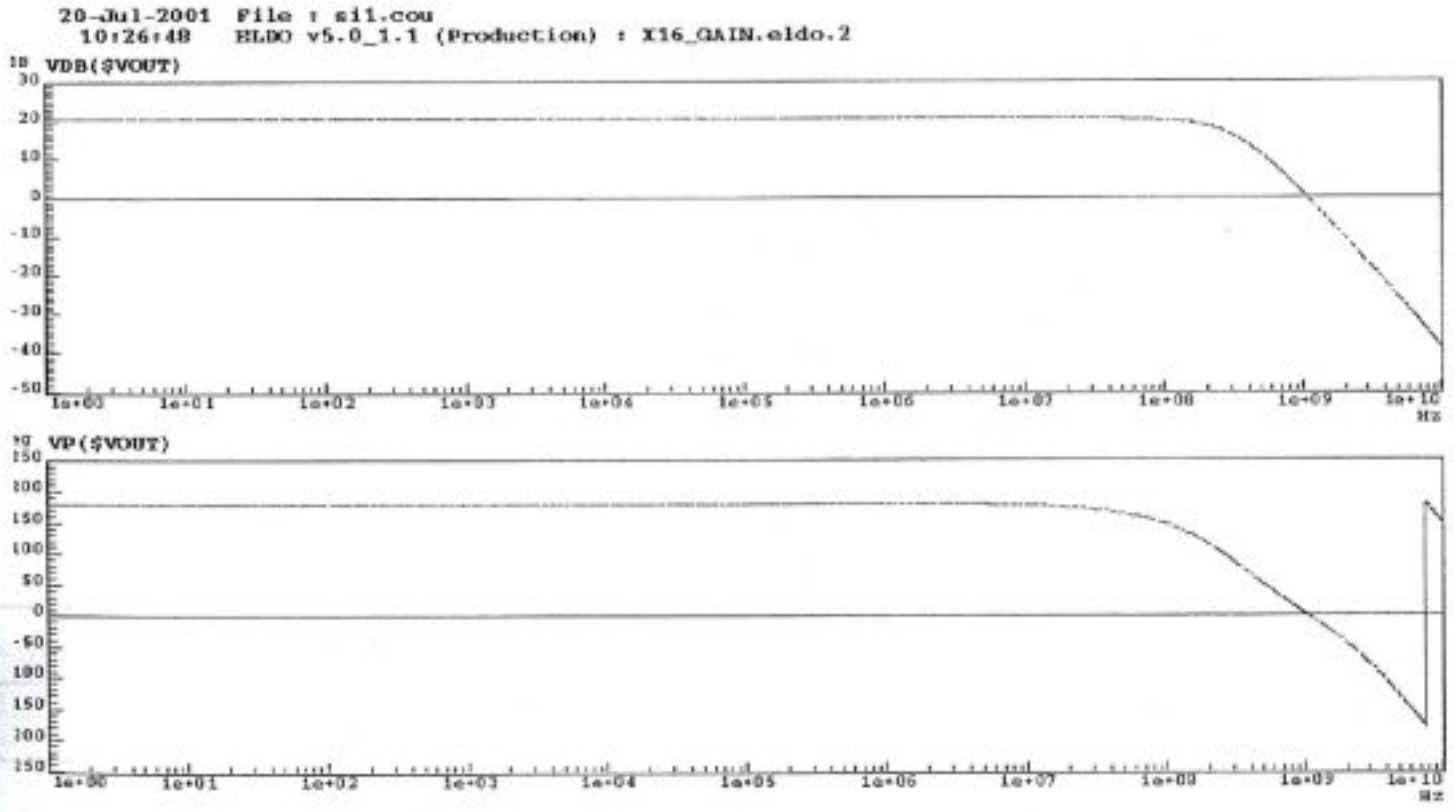


Figure 5.13 Closed loop AC characteristics of high open loop gain OTA based op-amp.

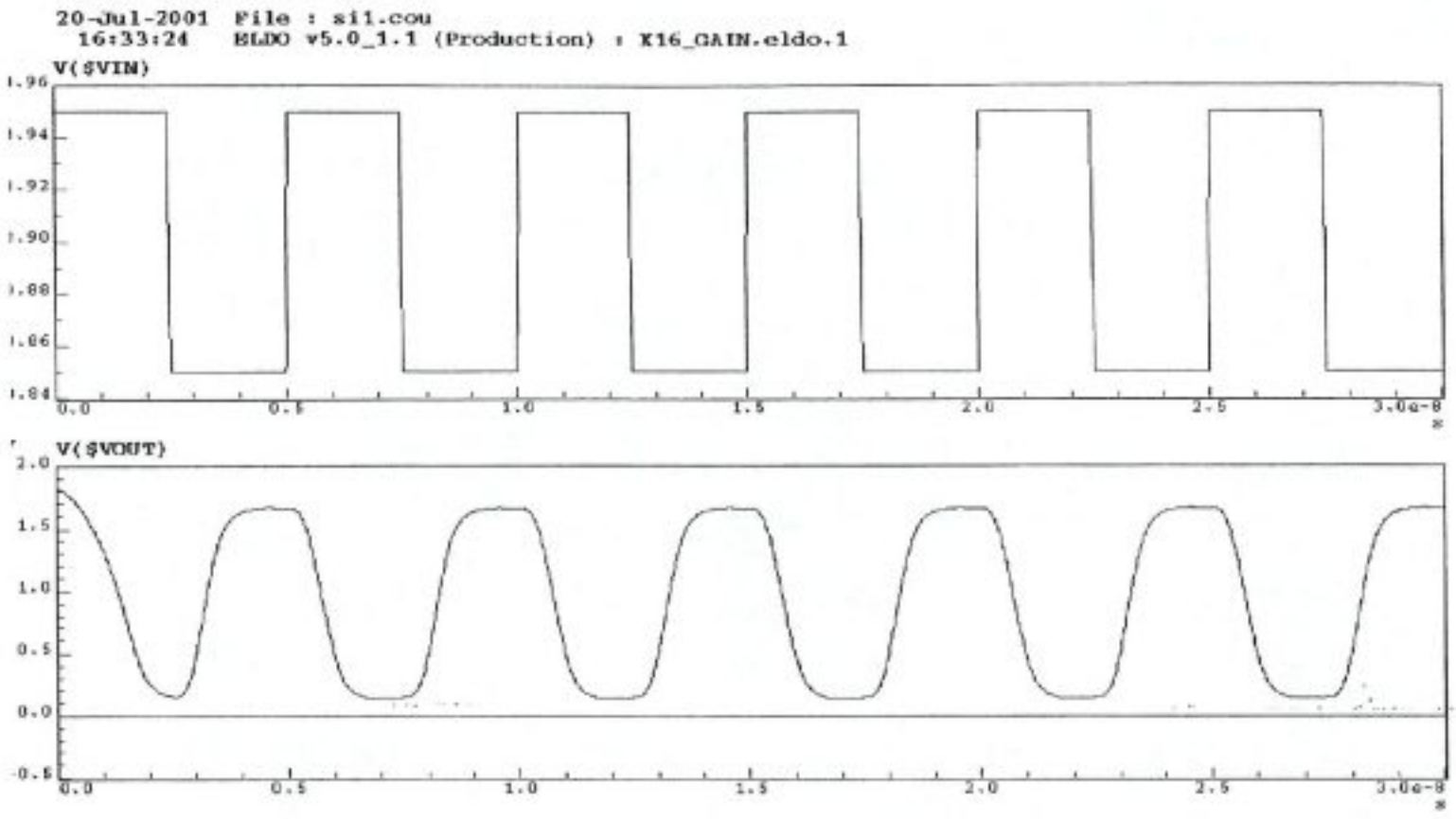


Figure 5.14 Transient characteristics of high open loop gain OTA used in a X16 feedback gain for residue amplifier for a 200MHz 100mV$_{pp}$ input pulse.

Input ofset	1.163 mV
Output ofset	94.67 mV
I_B	50 μA
Open loop gain	50.19496 dB
f_{180}	1.0025GHz
f_0	2.92098 GHz
Closed loop f_{3dB}	2.53 GHz
Slew rate	2.7523 V/ns

Table 5.3-a Simulation results of the most important specifications.

Pole frequency	Simulated	Manually calculated
p_1	50.7355 MHz	53.88729 MHz
p_2	492.689 MHz	795.52 MHz
p_3	551.1578 MHz	3.6377 GHz
p_4	764.5468 MHz	6.59124 GHz
p_5		13.213 GHz
Zero frequency	**Simulated**	**Manually calculated**
z_1	490.7125 MHz	2.8456 GHz
z_2	771.8586 MHz	25.526 GHz

Table 5.3-b Comparison of simulated and manually calculated pole/zero frequencies.

There still exists a severe problem for high open loop gain OTA based op-amp. As shown in Figure 5.14 transient response of the amplifier can not reach the rails of the input analog signal. Thus, there will exist systematic conversion errors, which can be corrected by using a very simple, digital error correction algoritm, named *as bit overlapping* instead of *cascading* the 4-bit outputs of successive pipeline stages. However, this technique requires higher resolution in the comparator chain of the internal successive pipeline stages. In other words analog input voltage swing range for the internal successive stages have to be halved (refer to Chapter 6). Thus, a feedback gain of "8" is required instead of "16". We now have to design an op-amp to be used in negative feedback loop with gain "8".

We have to reduce the feedback gain from "16" to "8", thus we have to design a more stable op-amp than the previous one. Otherwise we could face stability problems in feedback configuration. On the other hand we also need high open loop gain in order to over come any gain error that can arise from low loop gain of the feedback configuration. Thus, we increased the compensation capacitance value from 50 fF to 100 fF, which will in return lower the slew rate of the op-amp. In order to over come some of this side effect we decreased the value of feedback resistor from 75 kΩ to 50 kΩ that will also reduce the parasitic capacitance of the resistor. All other elements of the architecture stayed the same as the high open loop gain op-amp (Table 5.4). Simulation results of X8 op-amp are given in Figure 5.15 to Figure 5.18.

	W (μm)	*L(μm)*
M1	10	0.5
M2	10	0.5
M3	0.36	0.18
M4	0.36	0.18
M5	3.6	0.18
M6	3.6	0.18
M7	2	0.18
M8	2	0.18
M9	7.2	0.18
M10	18	0.18
R_f	50 kΩ	
C_f	100 fF	

Table 5.4 Aspect ratio table for X8 OTA based op-amp configuration.

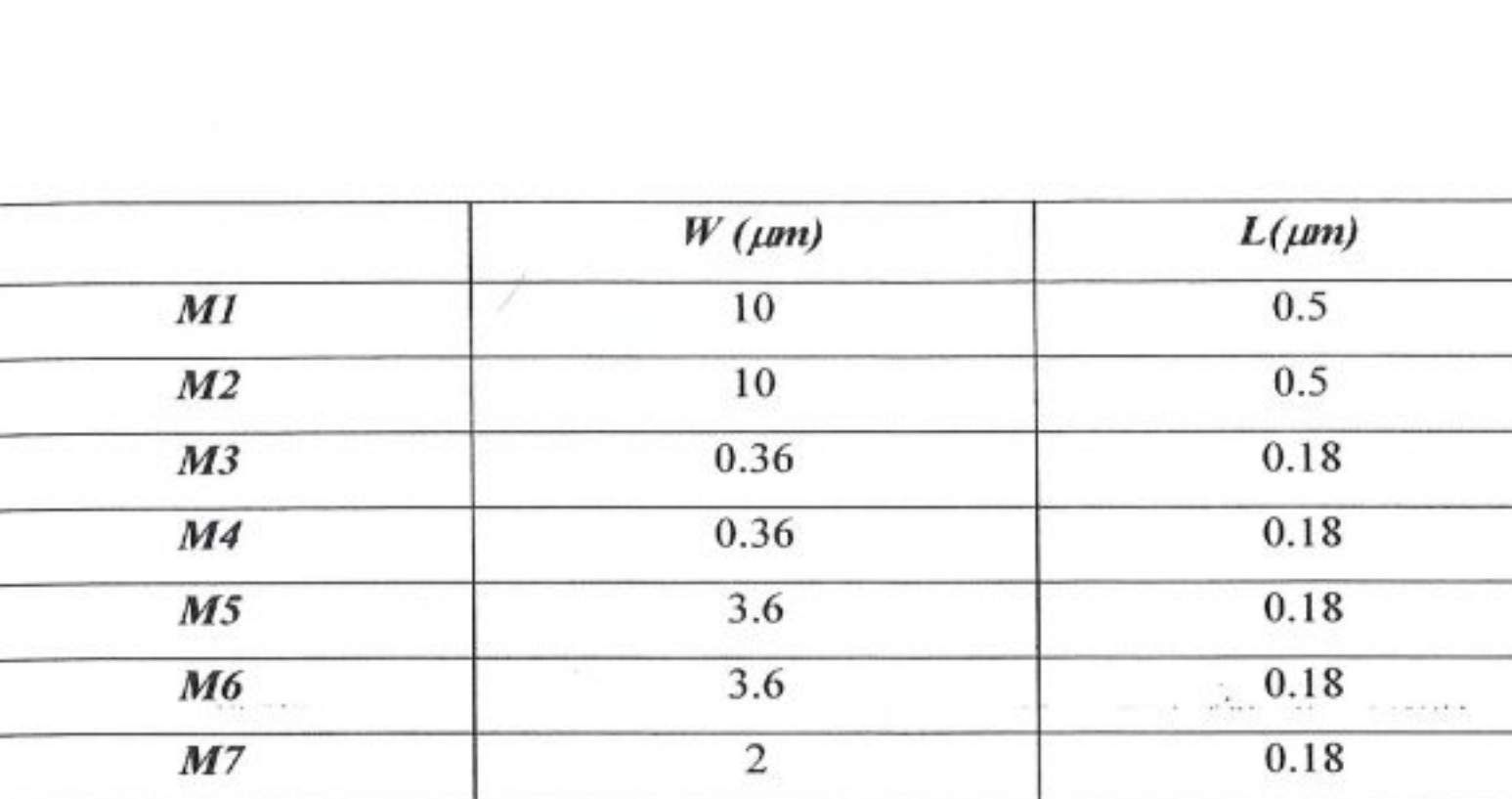


Figure 5.15 DC characteristics of X8 OTA based op-amp.

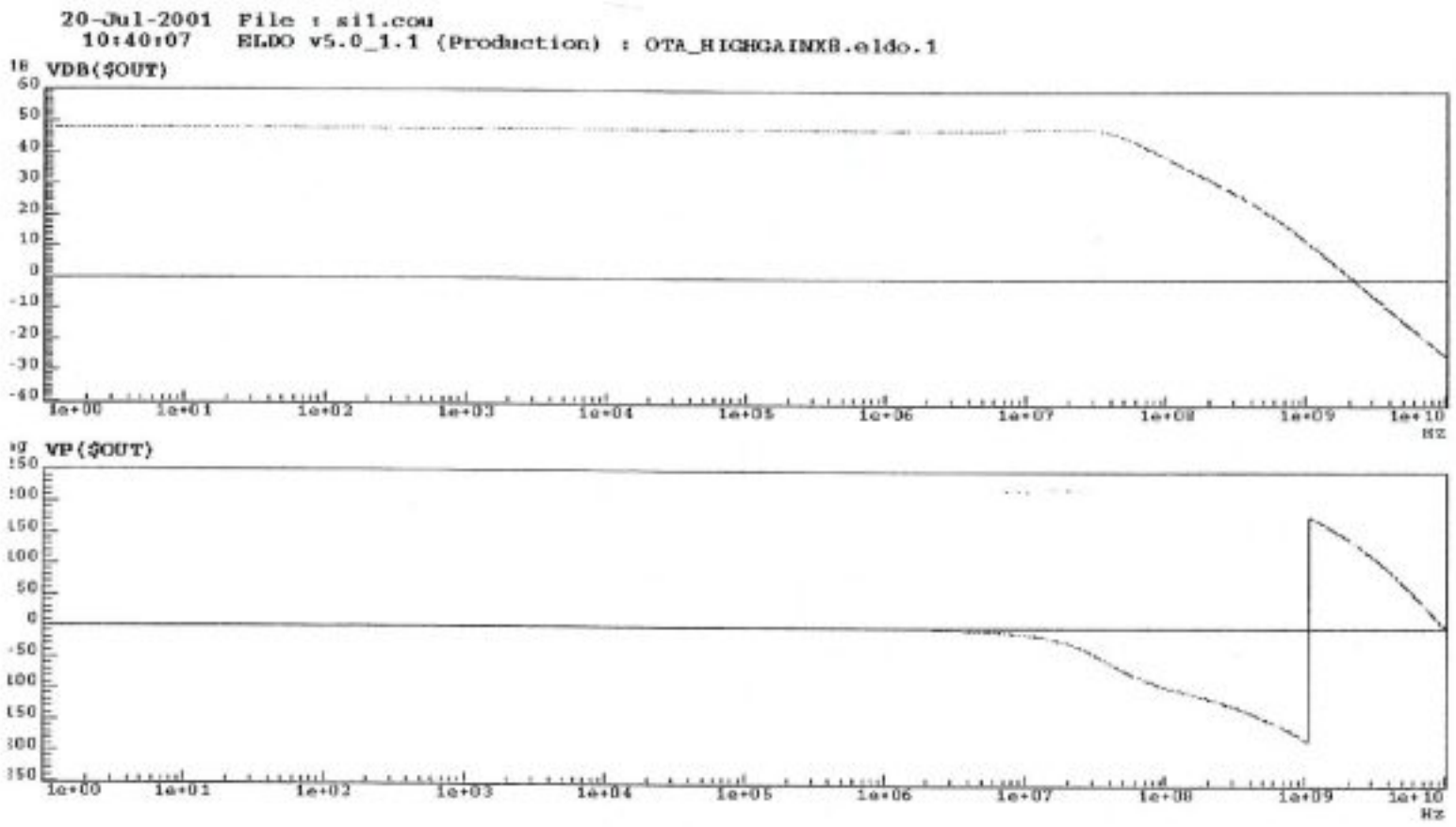


Figure 5.16 Open loop AC characteristics of X8 OTA based op-amp.

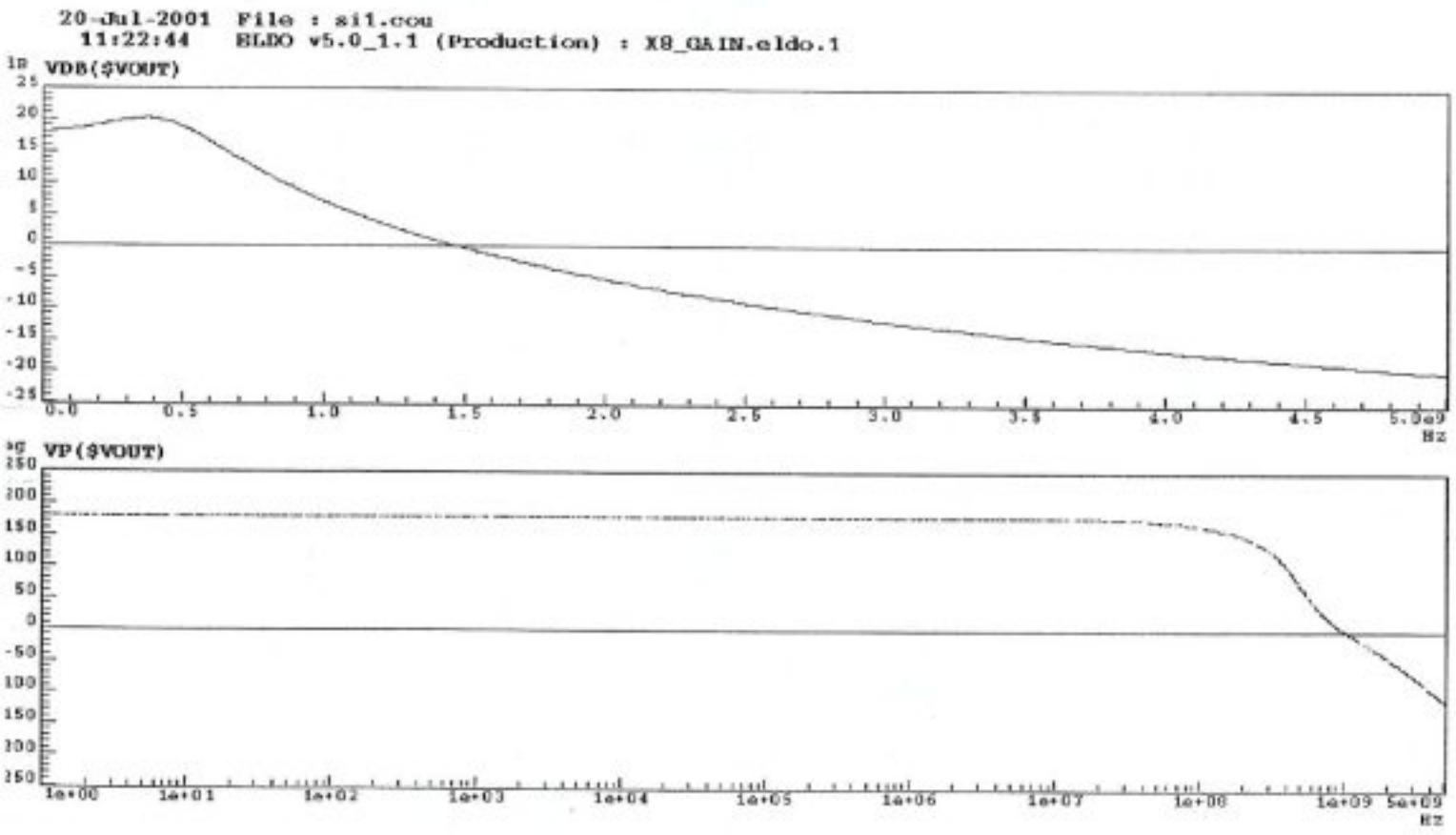


Figure 5.17 Closed loop AC characteristics of X8 OTA based op-amp

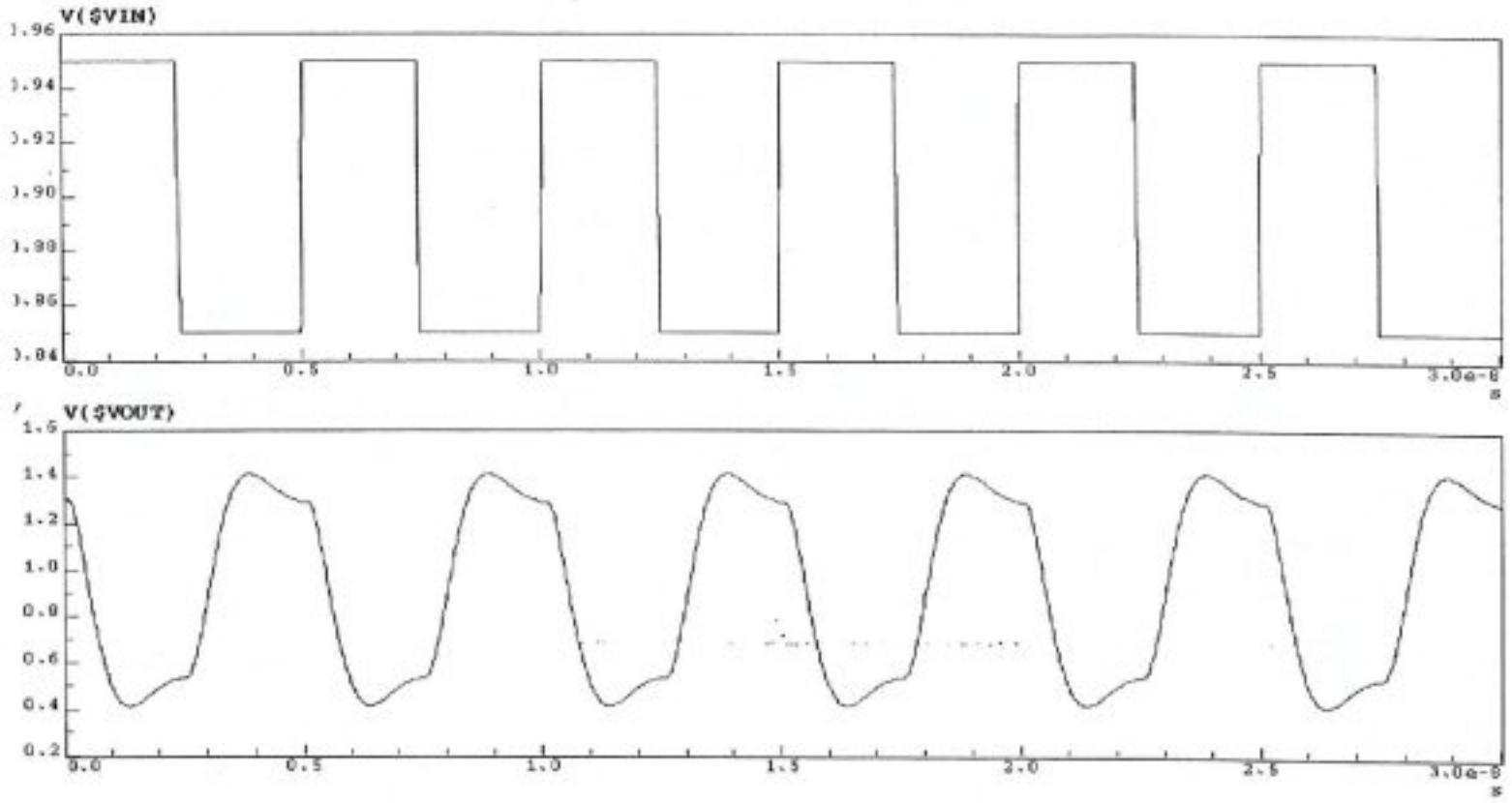


Figure 5.18 Transient response of X8 OTA based op-amp to a 200MHz 100mV_{pp} input pulse.

Input ofset	1.20 mV
Output ofset	144.82 mV
I_B	50 μA
Open loop gain	48.2797 dB
f_{180}	1.0484 GHz
f_0	2.1626 GHz
Closed loop f_{-3dB}	665.154 MHz
Slew rate	1.1209 V/ns

Table 5.5-a Simulation results of the most important specifications.

Pole frequency	Simulated	Manually calculated
p_1	38.21138 MHz	52.28104 MHz
p_2	38.21138 MHz	795.52 MHz
p_3	492.266 MHz	2.0274 GHz
p_4	555.83 MHz	11.4516 GHz
p_5	764.603 MHz	13.213 GHz
Zero frequency	**Simulated**	**Manually calculated**
z_1	42.374 MHz	1.68194 GHz
z_2	490.69 MHz	26.426 GHz
z_3	771.861 MHz	

Table 5.5-b Comparison of simulated and manually calculated pole/zero frequencies.

The only drawback of this op-amp is output offset but still in tolerable limits. Thus, we will keep this architecture for the residue amplifier to be used in each pipeline stage with bit overlapping in the digital pipeline.

5.5 OTA based Low-Gain Op-Amp Design

After finishing the design of residue amplifier we now have to design a stable operational amplifier for the sample-and-hold circuit. This op-amp has to be stable in unity gain feedback configuration, which is named as the worst possible configuration for the stability. For this purpose we have to reduce the open loop gain by reducing the input transistors aspect ratio and also the B factor of the pMOS current mirrors, which will also reduce the parasitic capacitances in return, consequently higher the pole frequencies that could cause instability. We need a real sample-and-hold circuit for our purpose (not a track-and-hold amplifier), because we have to process the analog input during half of the sampling clock period. Thus, we will use two stable op-amps cascaded, operated with a non-overlapping clock consequently, which will realise the hold operation. We designed the OTA based op-amp given in Figure 5.19 the element aspect ratios are given in Table 5.6.

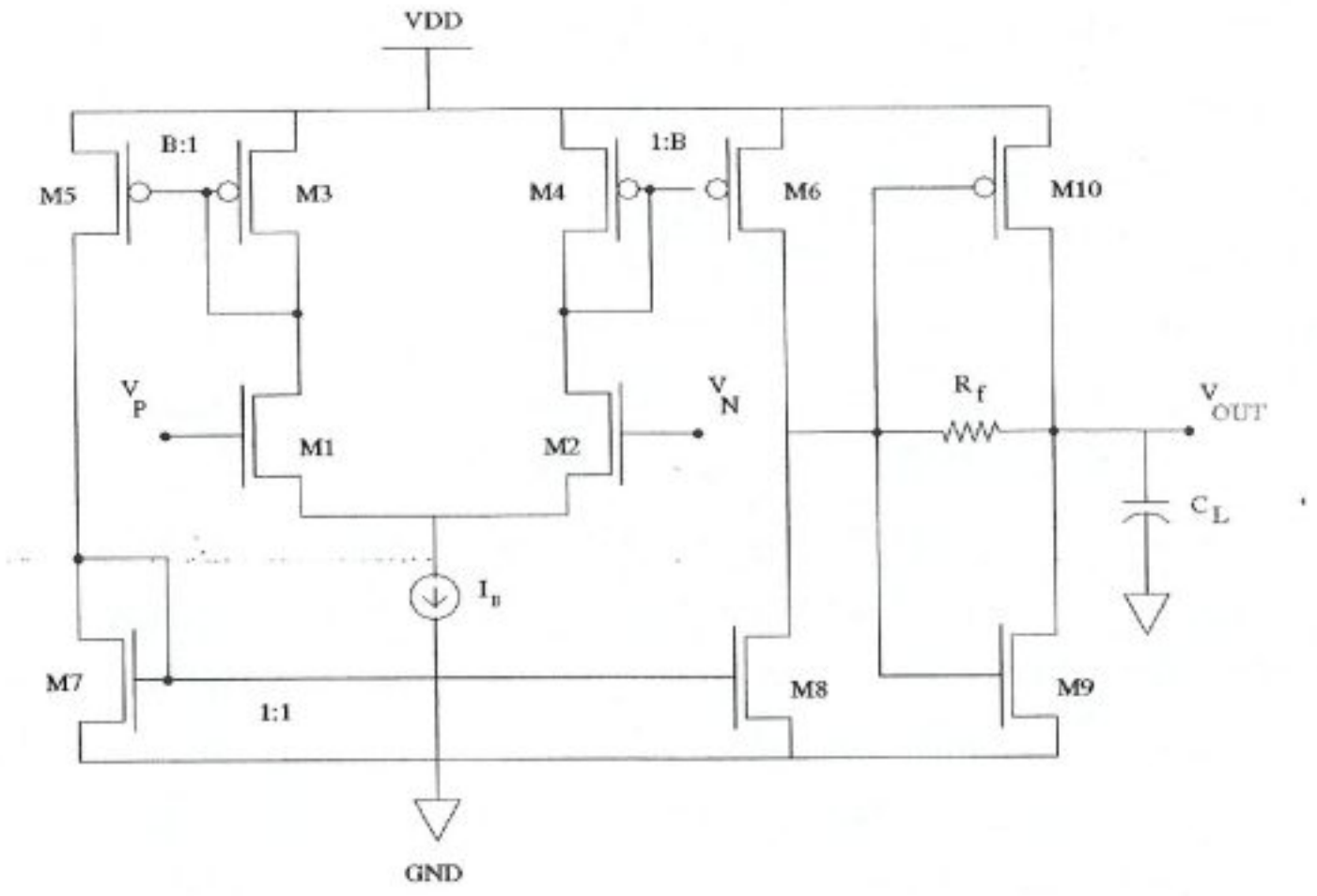


Figure 5.19 Schematic view of low open loop-gain OTA.

	W (μm)	*L(μm)*
M1	2	0.5
M2	2	0.5
M3	0.36	0.18
M4	0.36	0.18
M5	0.72	0.18
M6	0.72	0.18
M7	0.26	0.24
M8	0.26	0.24
M9	14.4	0.18
M10	36	0.18
R_f	75 kΩ	

Table 5.6 Aspect ratio table for low open loop-gain OTA.

After deciding to reduce open loop gain we lowered the pMOS current mirror gain from 10 to 3. In order to satisfy the input offset specification we also lowered the transconductance (g_m) of the input stage and aspect ratio of the nMOS current mirror. We end up with a transistor width of 0.28 μm for nMOS current mirror, which is not feasible. So that we kept the aspect ratio as it was and scaled nMOS current mirror to minimum possible W value. In order to lower the input offset we had to decrease pMOS current gain once more from 3 to 2, which in return lower the open loop gain, higher the phase margin and the output offset. But still very suitable for times two feedback gain configuration to used in sample-and-hold circuit. We inserted this design is a X2 negative feedback configuration having an absolute resistor ratio of two. There we faced gain error because of the low open loop gain of op-amp and also low valued feedback resistors, which steal current from, output stage that results in lower output voltage swing. In order to solve this problem we have to first increase resistor values, resulting in a lower phase margin which will create stability problems. Secondly we have to find a ratio of feedback resistors that will clearly give X2 feedback gain. We used 2kΩ/5kΩ feedback resistors to obtain accurate gain. We also have to do compensation to guarantee stability. After several trials 50fF of compensation capacitance is found out to be the most proper capacitor value. As always this positive improvement has a negative effect on slew rate of the op-amp, which can only be solved by increasing output stage's aspect ratio and thus also increasing the output offset.

Although we used feedback we could not reach input range swing because of two obvious problems.

- Clipping of output voltage swing because of the topological behaviour,
- Having soft corners in DC voltage sweep characteristics, which means having lower gain while the input signal becoming near to both supply ranges.

Clipping of output voltage, is solved by further increasing feedback resistor values while keeping the ratio of these two resistors constant, and also increasing the aspect ratio of the output stage's aspect ratios. But soft corners in the DC characteristics still remain after all these steps have been taken. Soft corners in DC characteristics could only be resolved by increasing the feedback resistor's value from 50 kΩ to 75kΩ. We saw that this solution is not enough to reach the supply rails in feedback configuration.

Simulation results of low open-loop gain OTA based op-amp are given in Figure 5.20 to Figure 5.23.

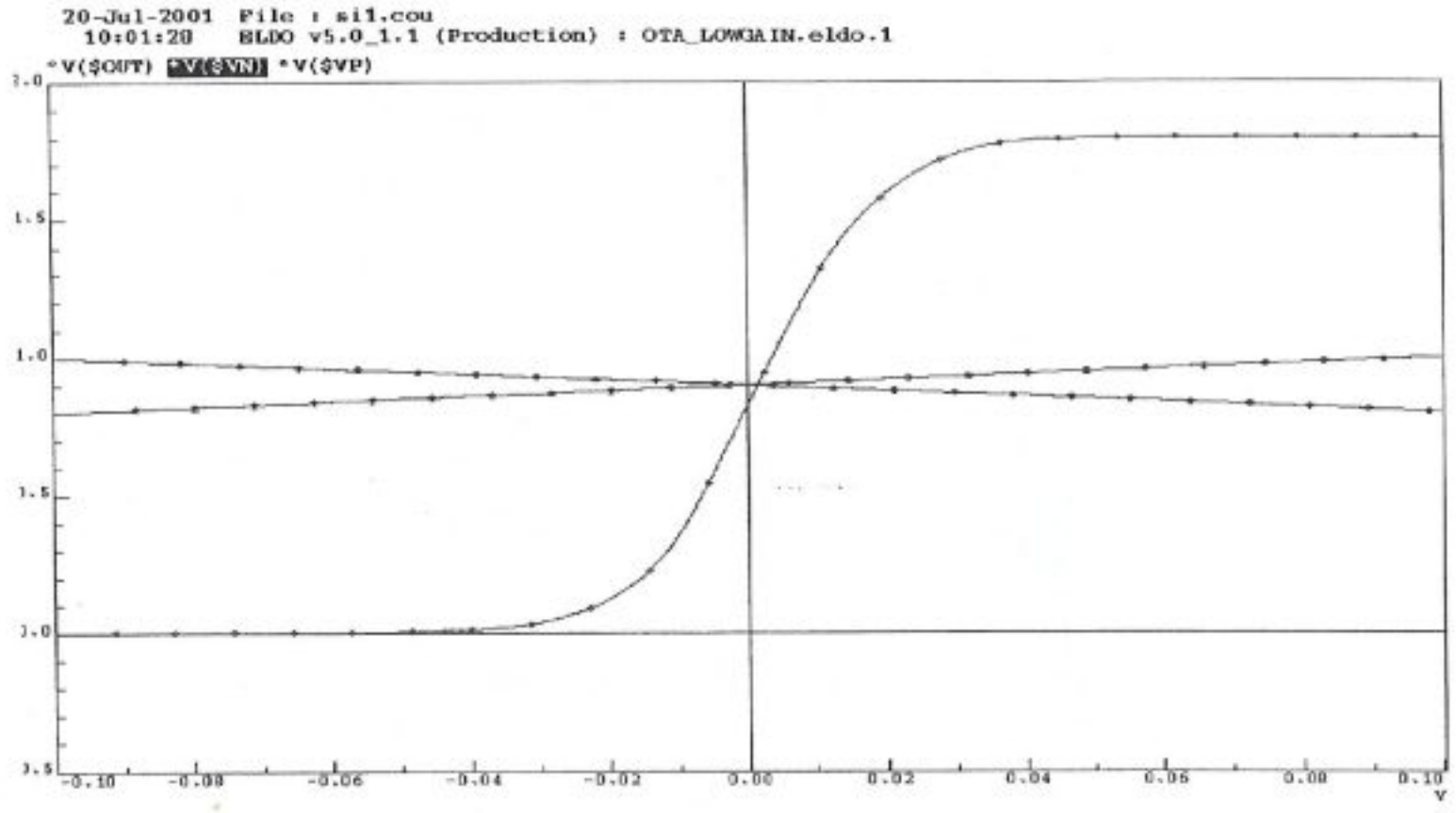


Figure 5.20 DC characteristics of low-open loop gain OTA based op-amp.

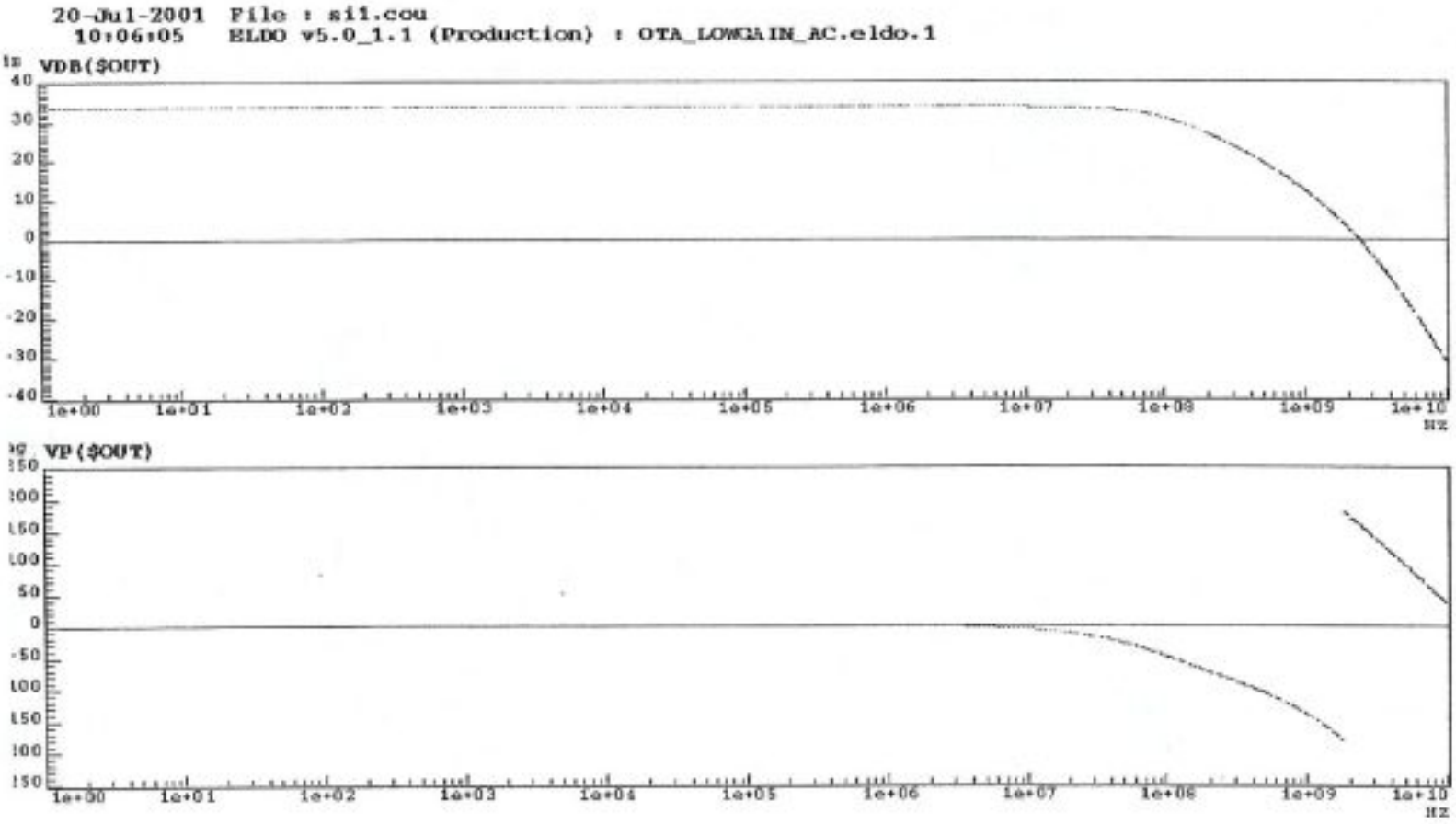


Figure 5.21 Open loop AC characteristics of low-open loop gain OTA based op-amp.

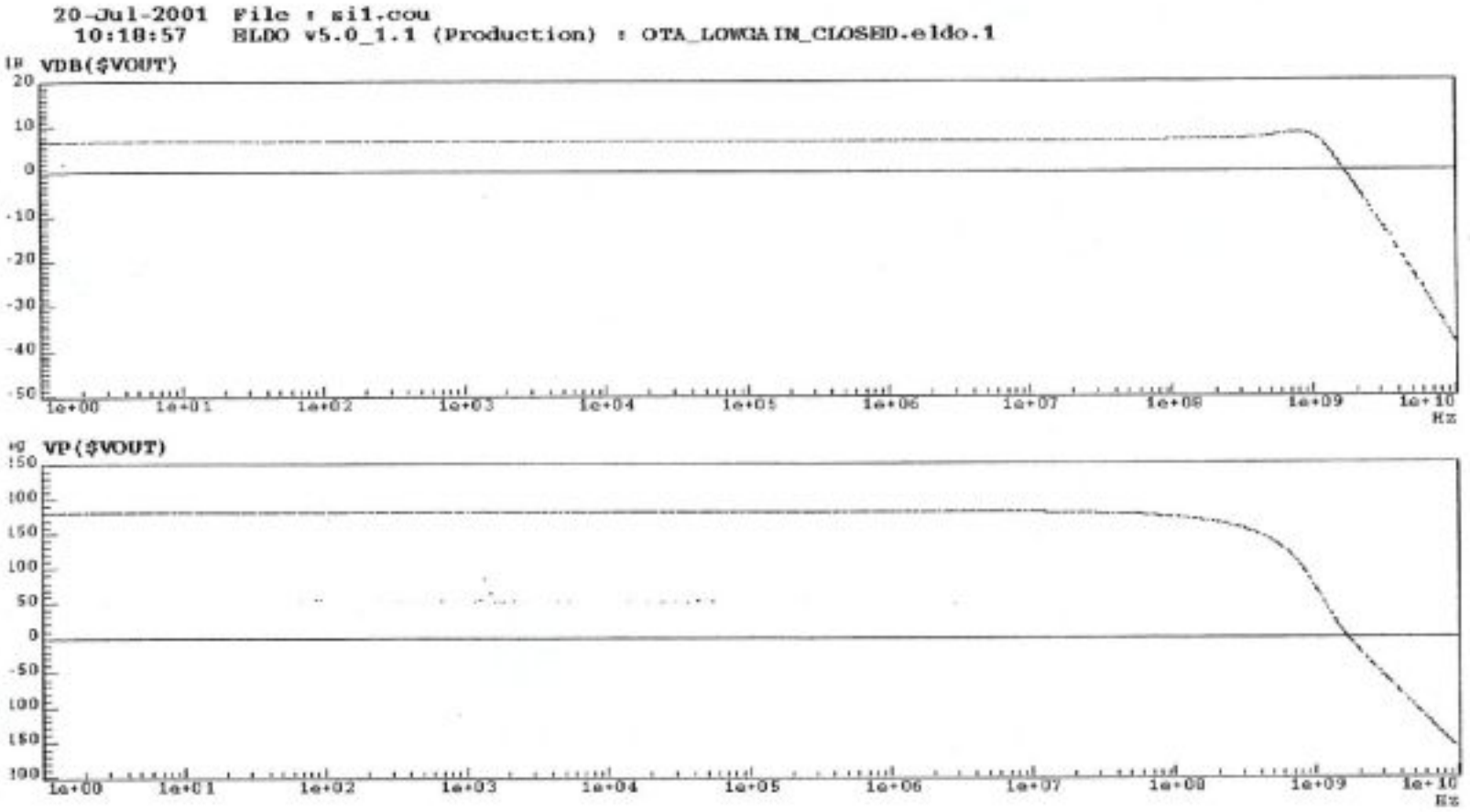


Figure 5.22 Closed loop AC characteristics of low-open loop gain OTA based op-amp.

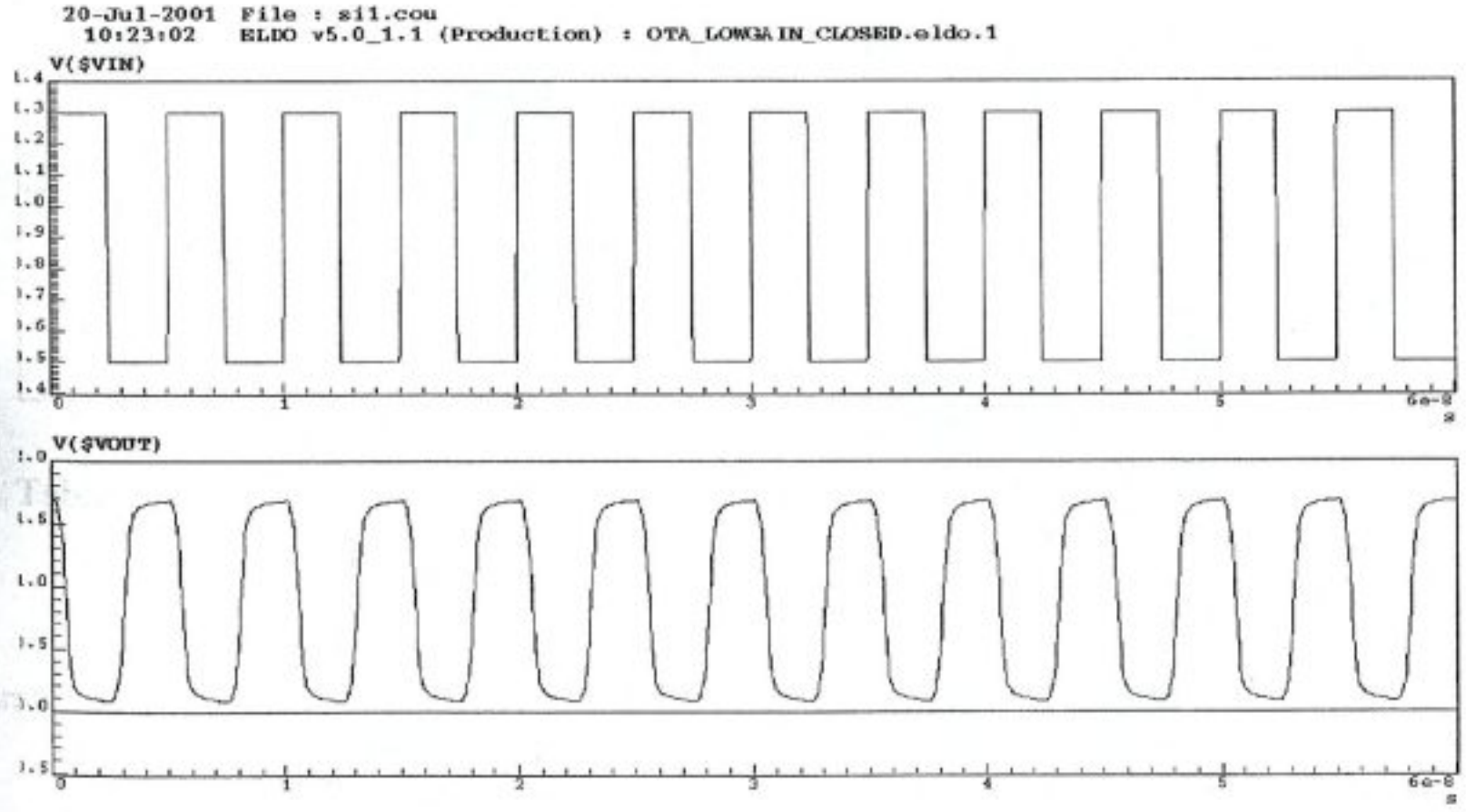


Figure 5.23 Transient response of X2 feedback configuration to a 200 MHz 800 mV_{pp} input pulse signal.

Input ofset	3.80 mV
Output ofset	90.18 mV
I_B	50 μA
Open loop gain	33.4996 dB
f_{180}	1.79369 GHz
f_0	2.4259 GHz
Closed loop f_{-3dB}	2.58 GHz
Slew rate	2.8246 V/ns

Table 5.7-a Simulation results of the most important specifications.

Pole frequency	**Simulated**	**Manually calculated**
p_1	106.307 MHz	108.778387 MHz
p_2	679.404 MHz	2.0274027 GHz
p_3		2.762945 GHz
p_4		5.451627 GHz
p_5		11.4516 GHz
Zero frequency	**Simulated**	**Manually calculated**
z_1	679.3941 MHz	1.681914 GHz
z_2		10.903254 GHz

Table 5.7-b Comparison of simulated and manually calculated pole/zero frequencies

In order to achieve real sample-and-hold operation we now have to design an op-amp, which is stable in negative feedback configuration.

5.6 OTA Based Op-amp Designed for Unity Gain Configuration

	W (μm)	*L(μm)*
M1	2	0.5
M2	2	0.5
M3	0.36	0.18
M4	0.36	0.18
M5	0.72	0.18
M6	0.72	0.18
M7	0.26	0.24
M8	0.26	0.24
M9	7.2	0.18
M10	18	0.18
R_f	75 kΩ	
C_f	50 fF	

Table 5.8 Element aspect ratio's of unity gain stable OTA based op-amp.

When we simulated low open loop gain configuration as a sample-and-hold configuration we faced a severe problem, because we used resistors in negative feedback, in hold mode of the circuit all charged stored on the hold capacitor during the tracking phase discharged through the feedback resistors to load capacitor immediately. Thus, the output voltage discharges to AC ground in hold mode. There exist three possible solutions to this problem:

- Using the op-amp designed for a feedback gain of 2 in a non-inverting configuration instead of inverting configuration,
- Using a simple source follower at the input of the amplifier,
- Designing a unity gain configuration op-amp to be used as an analog buffer.

We decided to use the third solution because we already have a low open loop gain design which is stable in unity gain configuration. The only problem of this solution is the limited output swing of the topology to be used, approximately $1V_{pp}$,

which is already solved by using this configuration in a X2 feedback gain configuration. We only lowered the aspect ratios of both the nMOS and pMOS of the inverter used as the output stage of the op-amp by two, because this op-amp will only have to drive the input stage of the op-amp with low open loop gain, and secondly added a Miller compensation capacitance for a cleaner transient response than the low open loop-gain op-amp. Results are shown in Fig. 5.24 to Fig. 5.26.

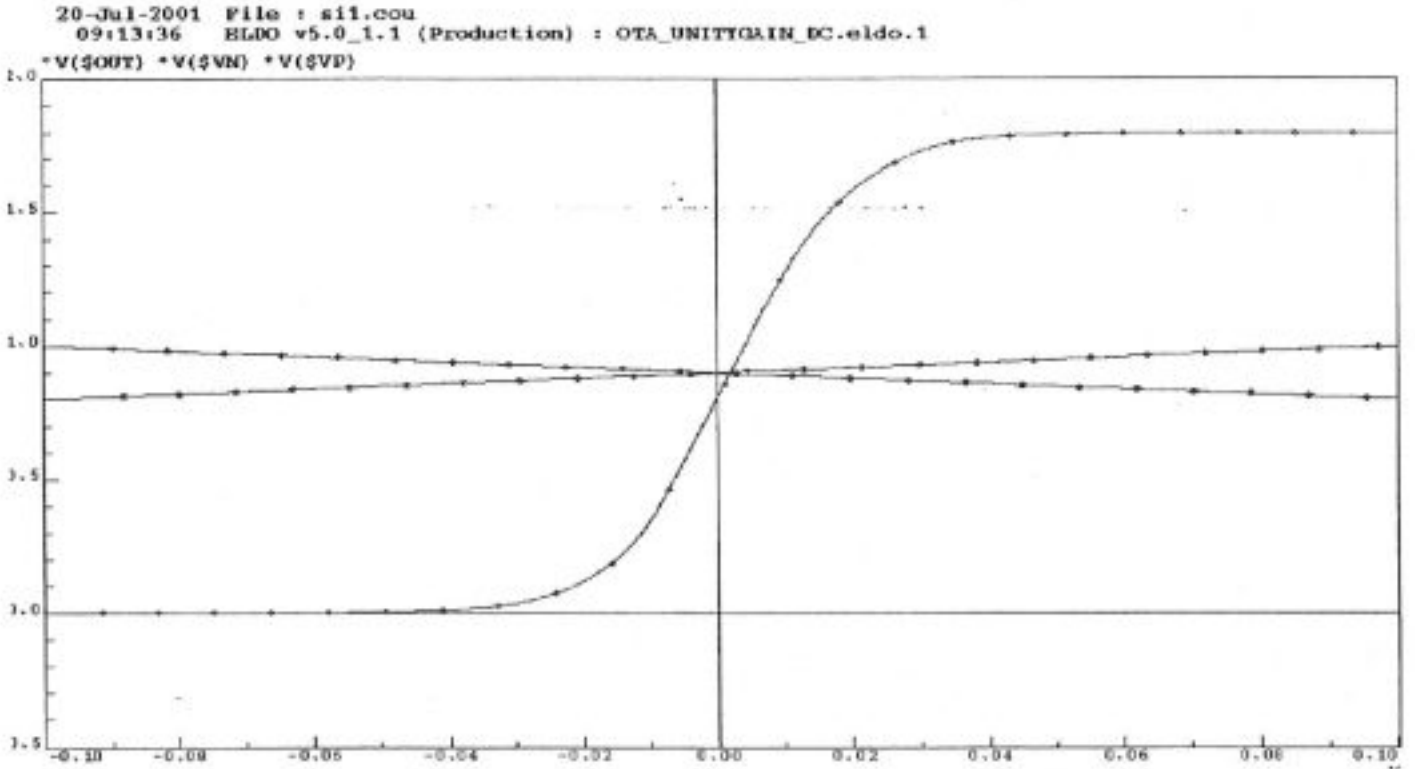


Figure 5.24 DC characteristics of unity gain stable OTA based op-amp.

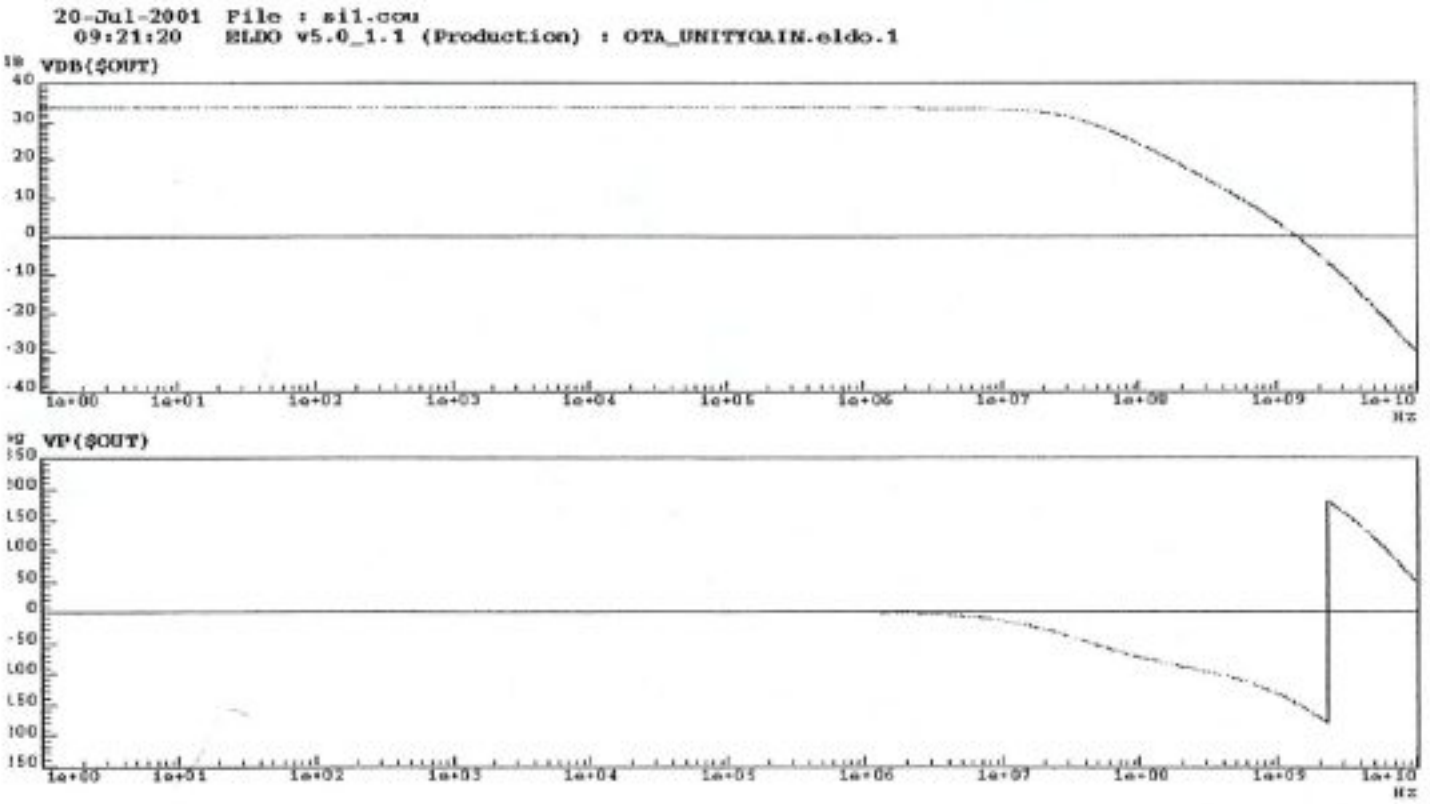


Figure 5.25 Open loop AC characteristics of unity gain stable OTA based op-amp.

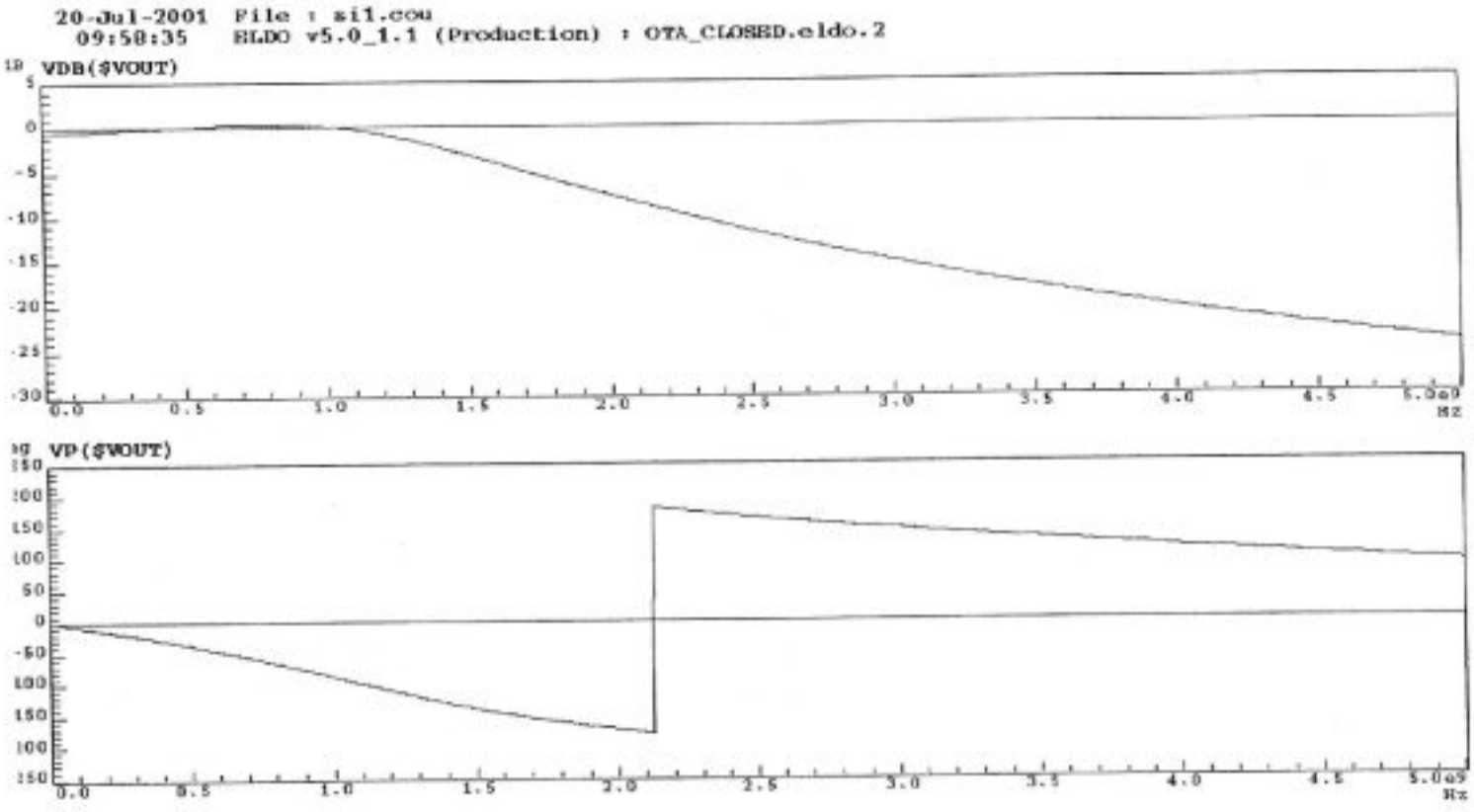


Figure 5.26 Closed-loop AC characteristics of unity gain stable OTA based op-amp.

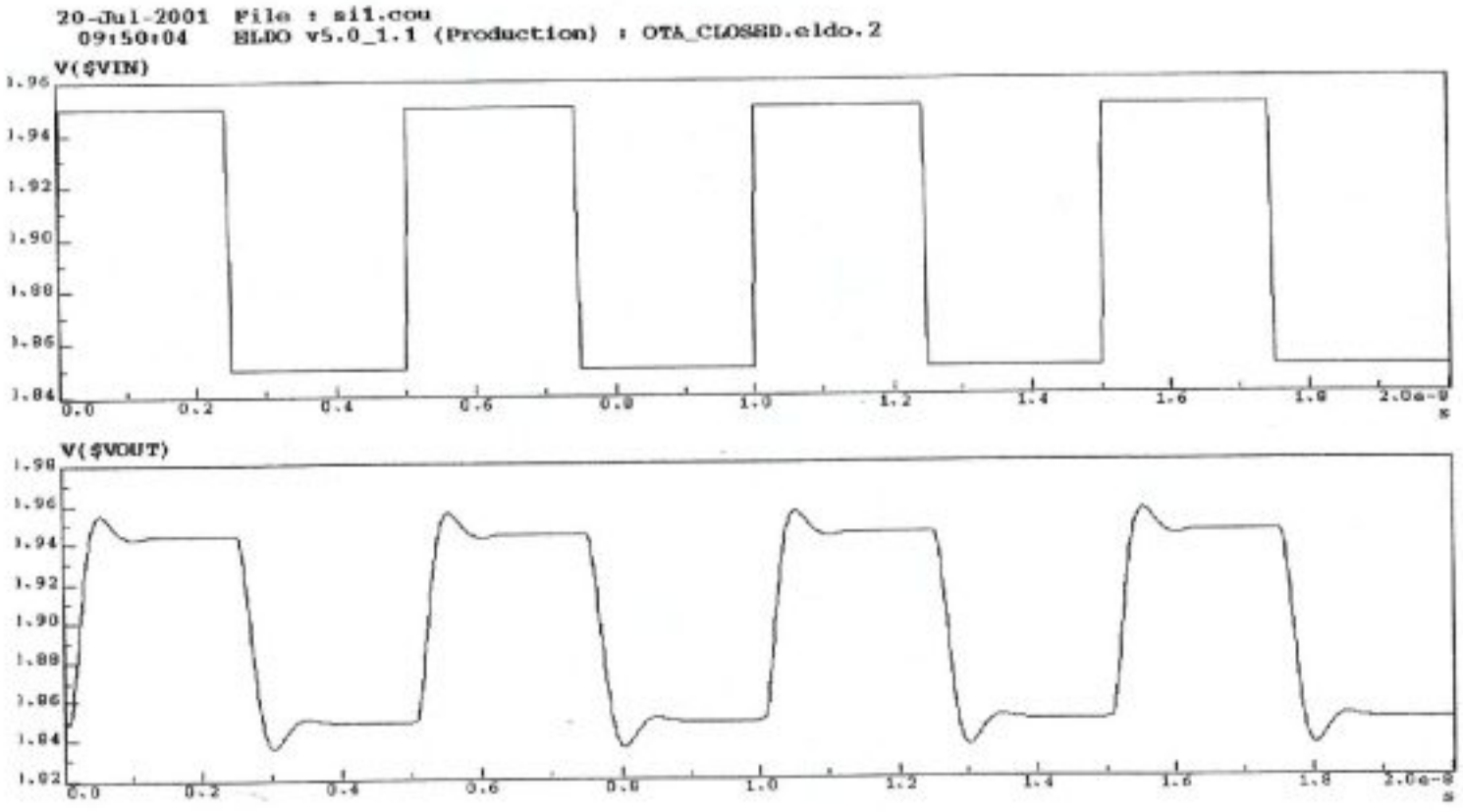


Figure 5.27 Transient response of unity gain stable OTA based op-amp to a 200MHz 10 mV_{pp} input pulse signal.

Input ofset	03.99 mV
Output ofset	94.67 mV
I_B	50 μA
Open loop gain	33.4855dB
f_{180}	2.2597 GHz
f_0	1.4015 GHz
Closed loop f_{-3dB}	1.43 GHz
Slew rate	781.63 V/μs

Table 5.9-a Simulation results of the most important specifications.

Pole frequency	**Simulated**	**Manually calculated**
p_1	37.19636 MHz	37.1877 MHz
p_2	679.4 MHz	2.762944 GHz
p_3		3.6377 GHz
p_4		4.451627 GHz
p_5		6.59124 GHz
Zero frequency	**Simulated**	**Manually calculated**
z_1	679.4 MHz	2.8456 GHz
z_2		10.9032 GHz

Table 5.9-b Comparison of simulated and manually calculated pole/zero frequencies.

Thus the sample-and-hold circuit and also the residue amplifier to be used in the design is now ready and given in Figure 5.28 and Figure 5.29. Simulation results of this sample-and–hold circuit is given in Figure 5.30 to Figure 5.35. Also simulation results of designed residue amplifier given in Figure 5.29, are given from Figure 5.36 to Figure 5.37.

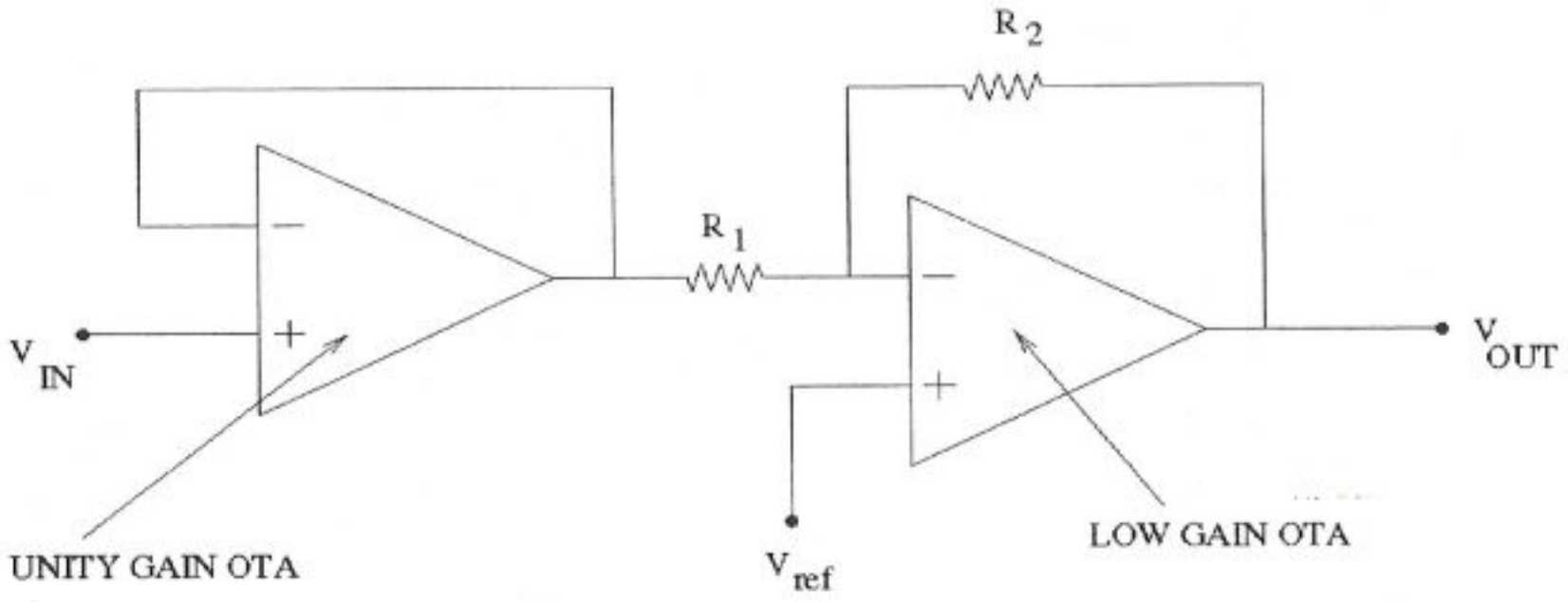


Figure 5.28 Block representation of sample-and-hold circuit.

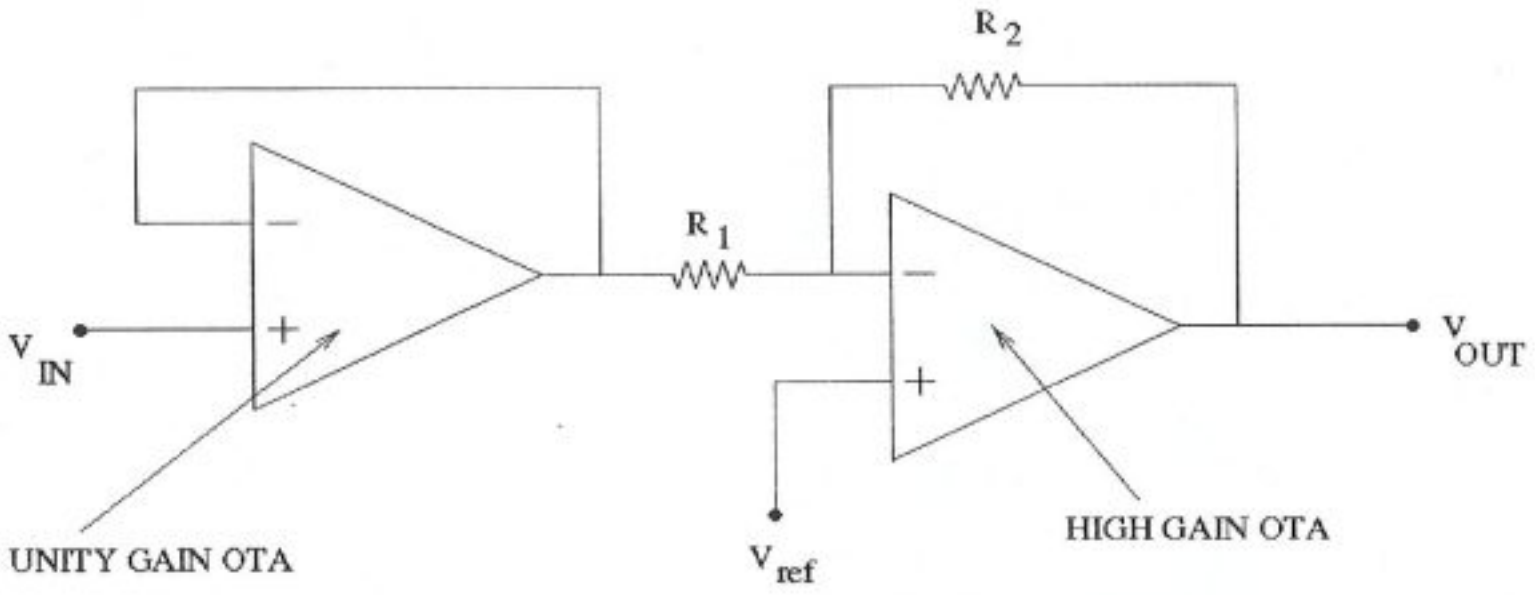


Figure 5.29 Block representation of residue amplifier circuit.

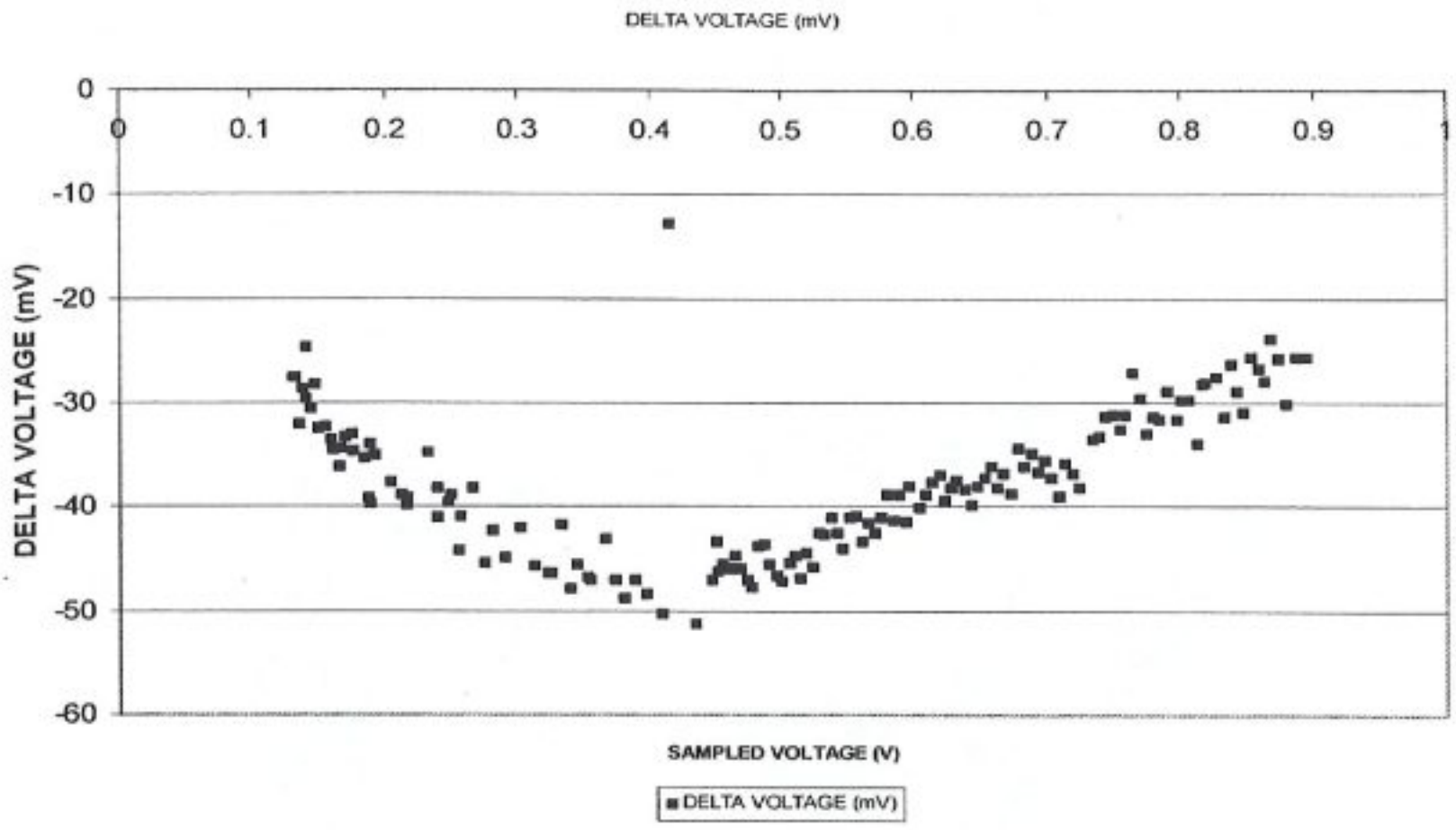


Figure 5.30 Sampled voltage versus sampling pedestal, where input signal frequency is 50 kHz and sampling clock frequency is 200MHz.

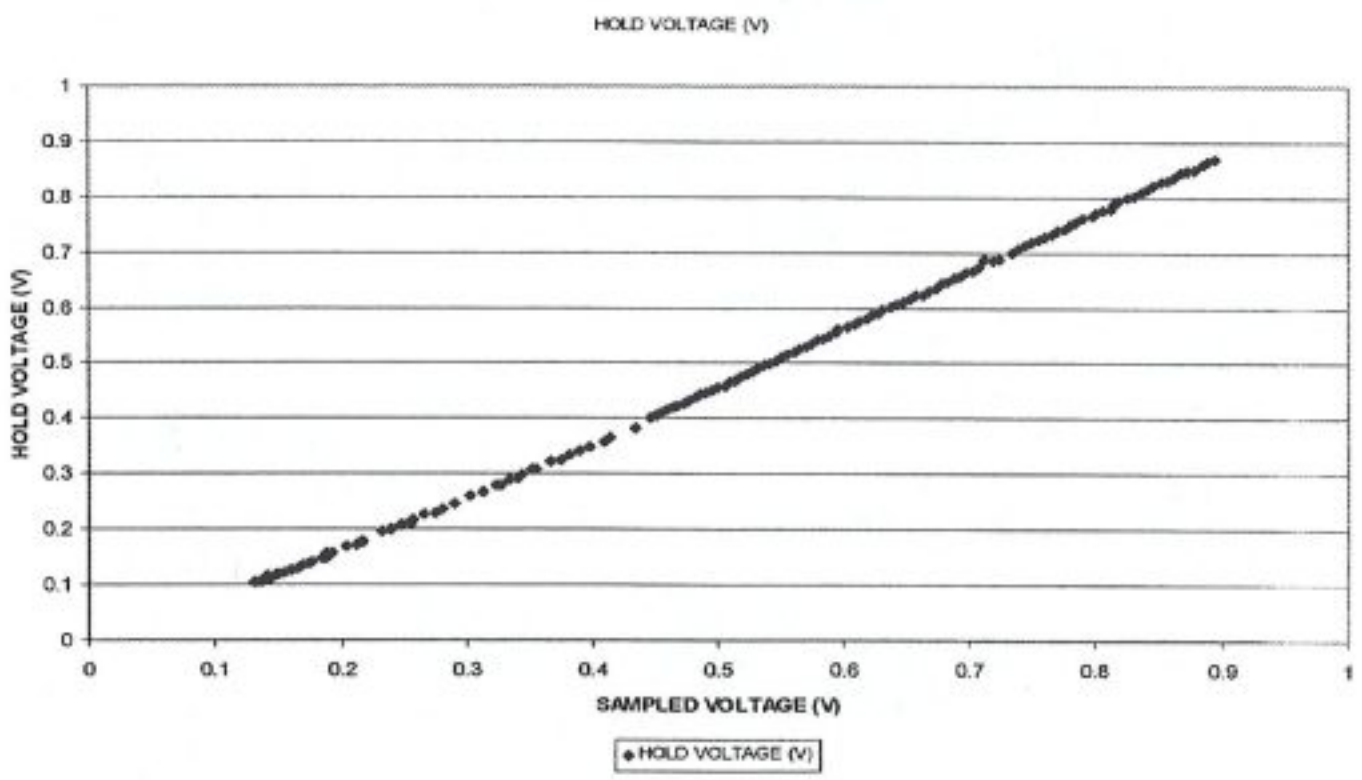


Figure 5.31 Sampled voltage versus held voltage, where input signal frequency is 50 kHz and sampling clock frequency is 200MHz.

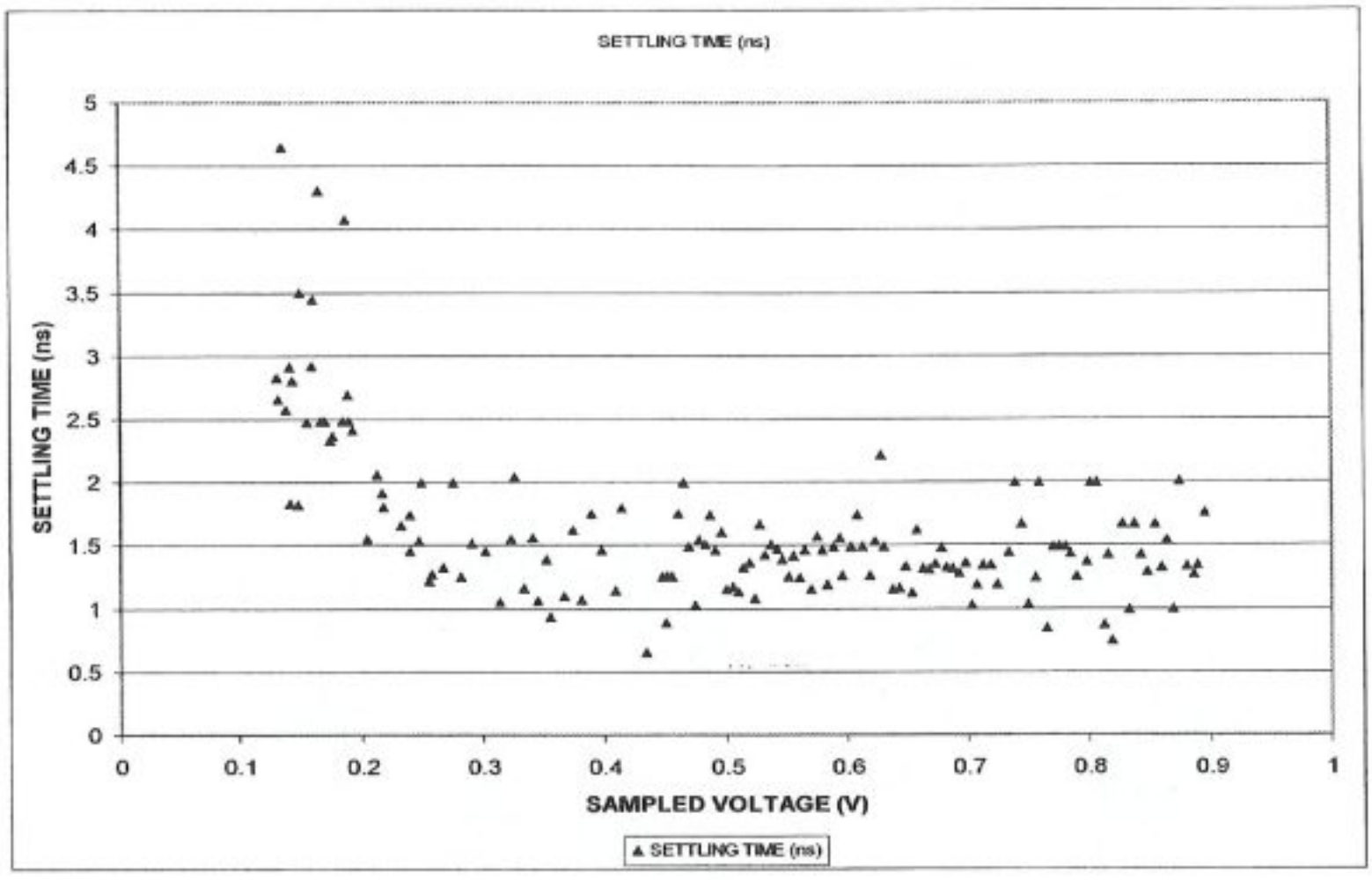


Figure 5.32 Sampled voltage versus settling time, where input signal frequency is 50 kHz and sampling clock frequency is 200MHz.

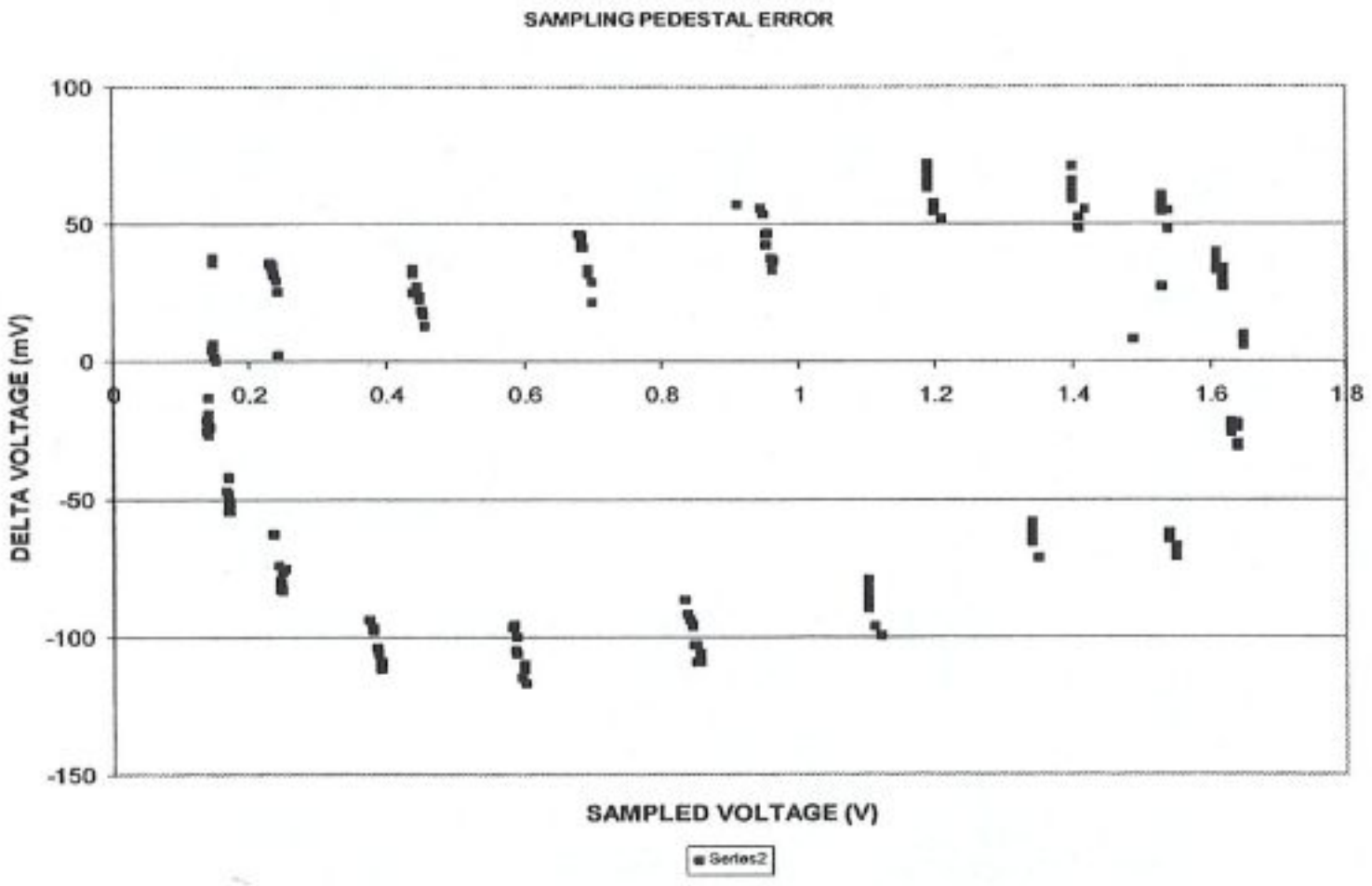


Figure 5.33 Sampled voltage versus sampling pedestal, where input signal frequency is 30 MHz and sampling clock frequency is 200MHz.

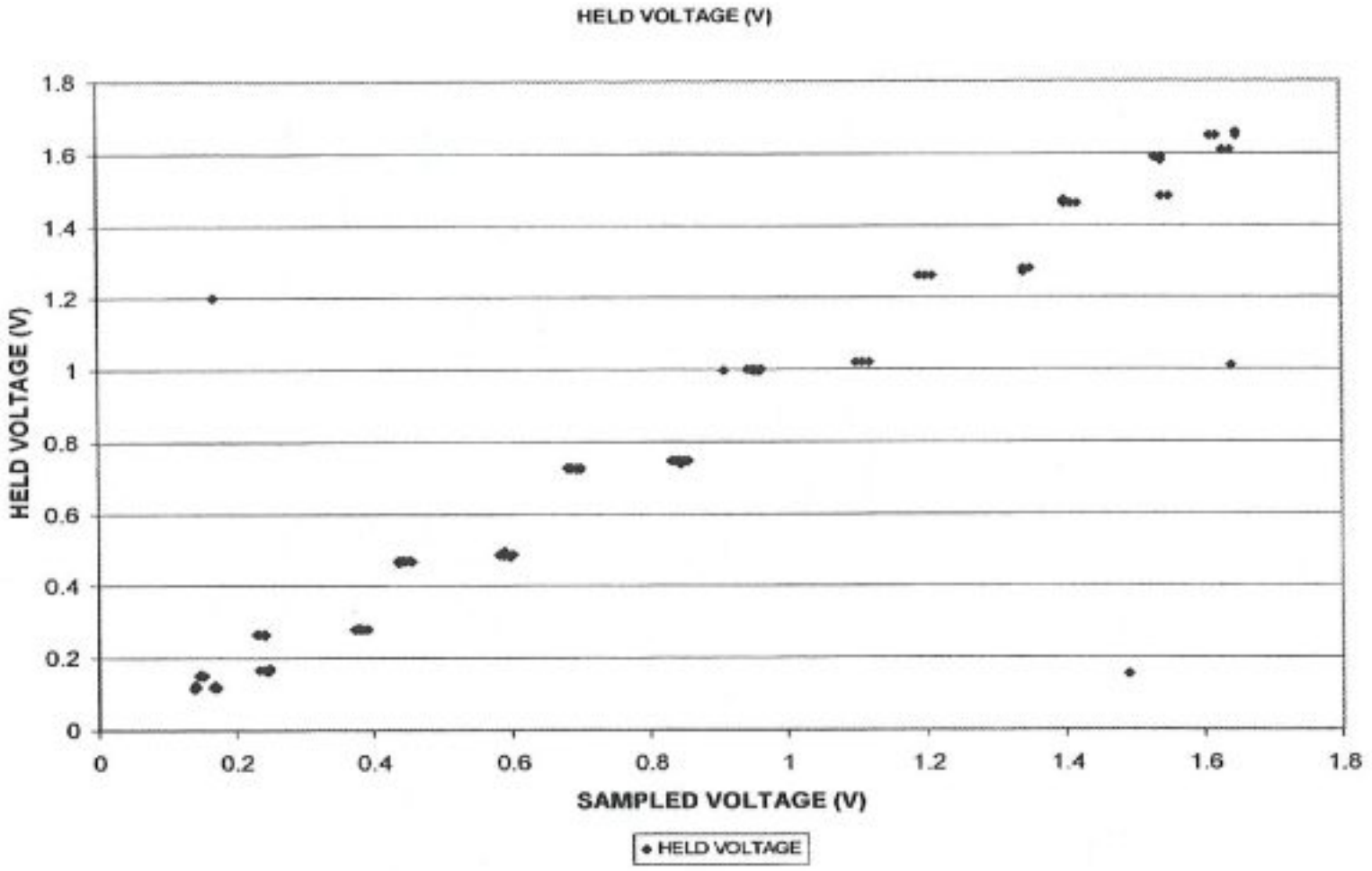


Figure 5.34 Sampled voltage versus held voltage, where input signal frequency is 30 MHz and sampling clock frequency is 200MHz.

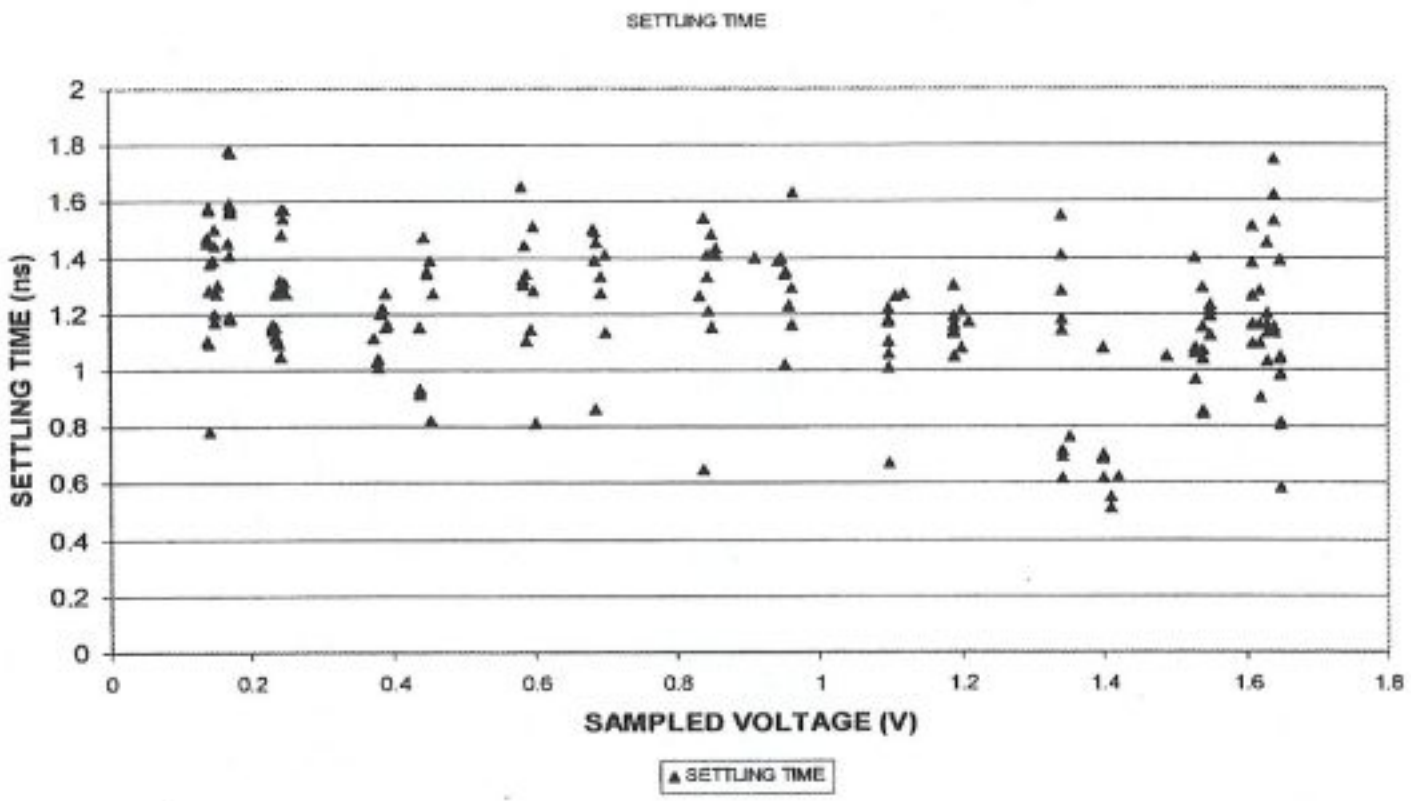


Figure 5.35 Sampled voltage versus settling time, where input signal frequency is 30 MHz and sampling clock frequency is 200MHz.

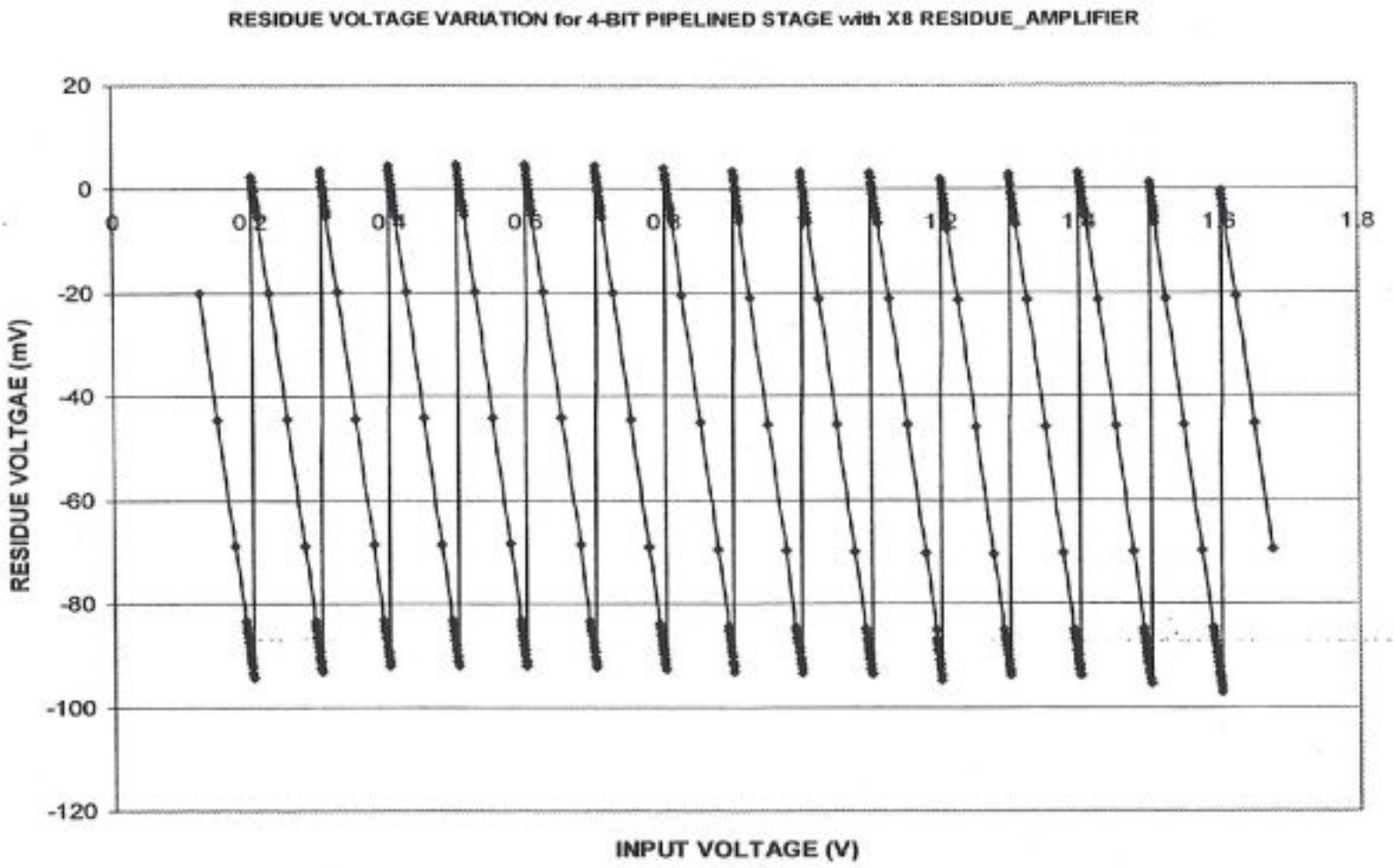


Figure 5.36 Residue voltage obtained versus input voltage for typical simulation corner.

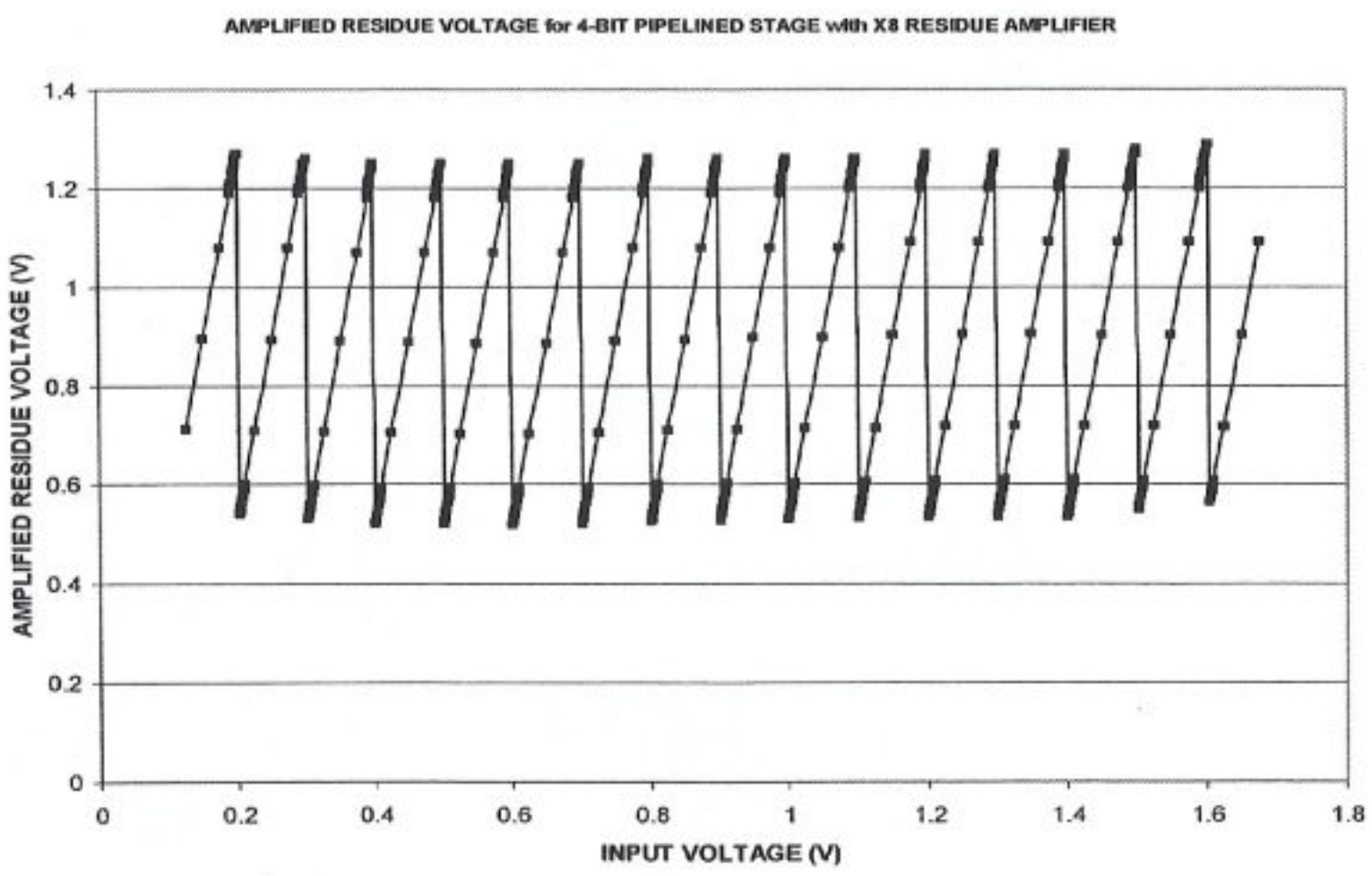


Figure 5.37 Amplified residue voltage by X8 amplification factor in residue amplifier circuit.

Given simulation results for sample-and-hold amplifier clearly states that the designed sample-and-hold amplifier (Fig. 5.28) is not precise enough for a 12bit A/D conversion application because of its sampling pedestal. Thus, an external high-speed, highly precise S&H amplifier has to be used for the characterization of the circuit.

On the other hand simulation results related to residue amplifier circuit are as expected. Thus, configuration given in Figure 5.29 will be used as a X8 feedback amplifier in each analog pipeline stage.

Note that simulated poles/zeros of all op-amps are examined up uo 1 GHz frequency range. Thus, it is normal that the simulated and the manually calculated poles/zeros are not totaly coincide with each other.

6. DESIGN OF ADC/DAC PIPELINE STAGES

Following a detailed study of the specific building blocks (components) in the previous chapters, the design and verification of a complete 4-bit ADC/DAC pipeline stage will be studied in this chapter. The complete schematic view of the 4-bit pipeline stage is shown in Fig. 6.2. It can be seen that the analog components of the proposed pipeline stage architecture consist of a 4-bit flash A/D converter, a 4-bit charge-scaling D/A converter (MDAC) and a residue amplifier, while the digital components include the 4-bit output encoder, the pipeline register banks, and part of the error correction circuitry (binary adder array). Also a simplified schematic view of a 4-stage pipelined Analog-to-Digital converter is given in Figure 6.1. All sub-blocks of the pipeline A/D converter architecture are included in this simplified view. The digital pipeline with error correction algorithm is given detail in Figure 6.1, where DFF and FA stand for a rising edge data flip-flop and 1-bit full adder circuits respectively. Note that the digital building blocks will be examined in detail in Chapter 7. The operation of the encoder sub-block will be explained in detail in this chapter.

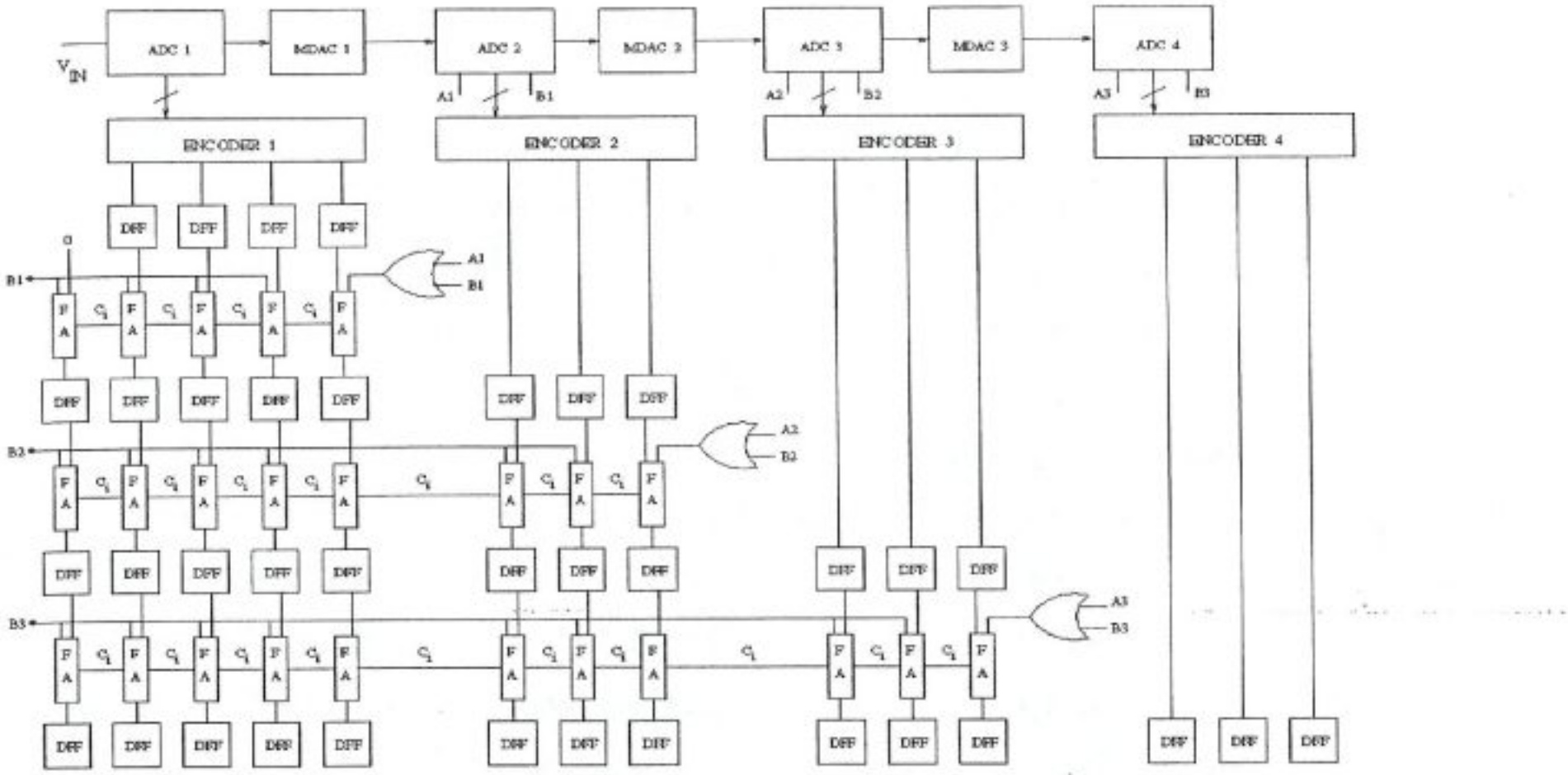


Figure 6.1 Four stage pipelined A/D converter schematic. Ai and Bi bits are overflow and underflow bits respectively. They will be explained in detail later in this chapter.

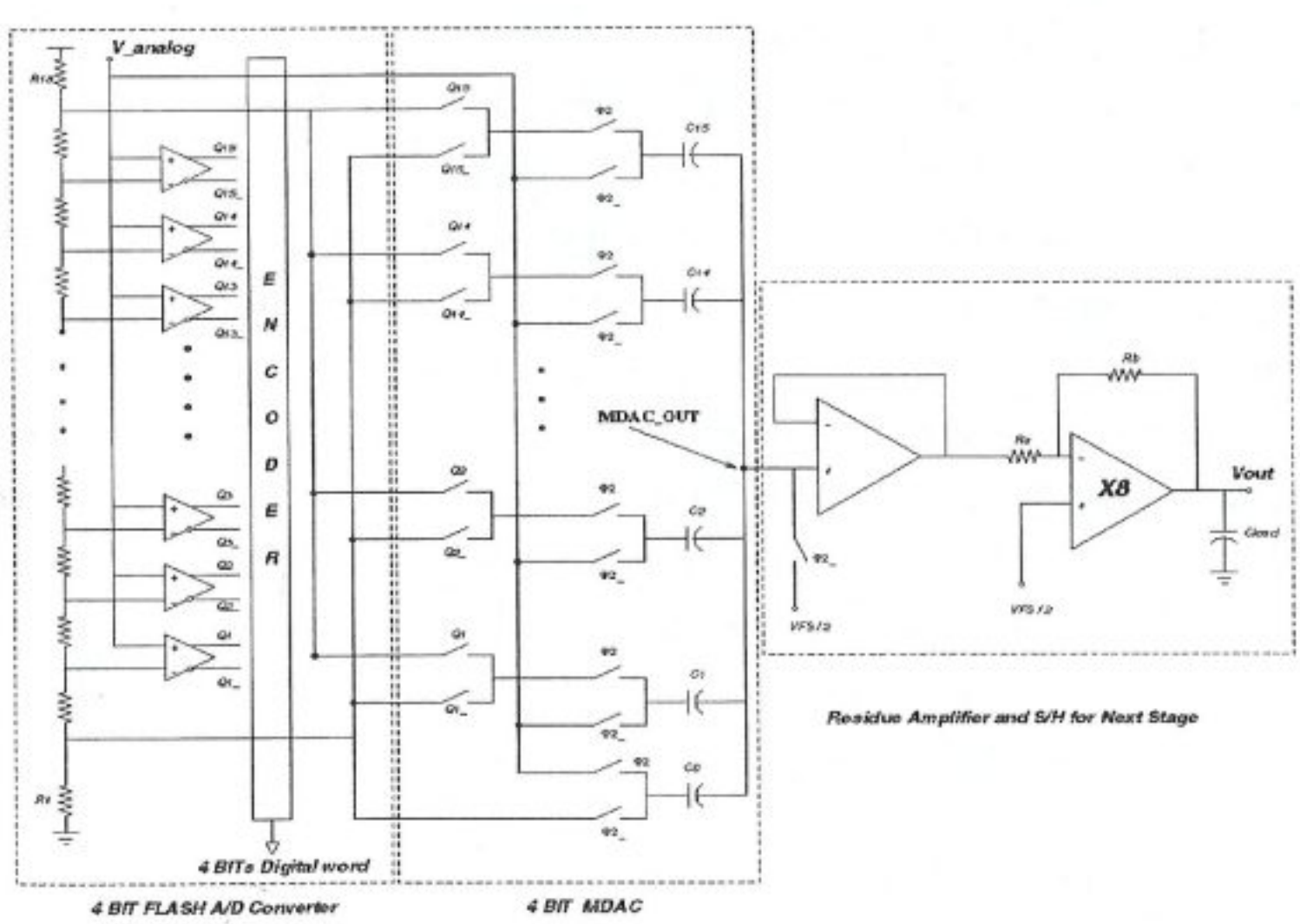


Figure 6.2 Full schematic view of a 4-bit pipeline stage.

6.1 Design of the 4-bit Flash A/D Converter

A resistive voltage divider is used between two reference levels, to generate fifteen voltage references needed for a four bits flash A/D converter. We used two external pins for positive and negative reference voltages, which will provide flexibility on choosing the analog input voltage swing range. Thus, sixteen (2^{N-1}) resistors were used in order to create fifteen voltage references between the input voltage signal rails (Figure 6.2). We used 500 Ω resistors realized as *polyn* resistors for all components of the resistor array. We chose *polyn* resistors because of their relatively high parasitic capacitance to ground, which will work as a filter to any fluctuations on the reference voltages due to clock feedthrough during the sampling (conversion) points. We will also use *salicide* layer in order to increase the sheet resistance of the *polyn* layer in the layout. Creating the layout of these resistors plays a very critical role, because their matching is more important than their absolute value. Thus, dummy resistors were used in the layout in order to prevent any edging effect that can cause mismatch, and also each of the eighteen resistors were drawn in an S-shaped form to save area.

After organizing the reference voltage chain, which is the heart of a flash A/D converter, by a resistive voltage divider we manufactured the comparator chain consisting of fifteen comparators for a four-bit conversion. Improved complementary-input comparators are used as the building block of the pipelined stage. We used thermometer code conversion in our A/D converter, which is the most suitable conversion algorithm in our case due to the available complementary outputs of the comparators. Thus, combining the resistor array, the comparator chain and the thermometer-to-binary encoder completes our 4-bit flash ADC. The simulated DC, time domain transient and frequency domain (AC) characteristics of the 4-bit ADC are presented in the following figures. The DC characteristics (INL and DNL plots) indicate that the comparator chain described above has an effective resolution of at least 10 bits. The operation is highly linear, and the 4-bit ADC is capable of producing a correct output with no missing codes for a very wide input range (between 0.1 V and 1.7 V).

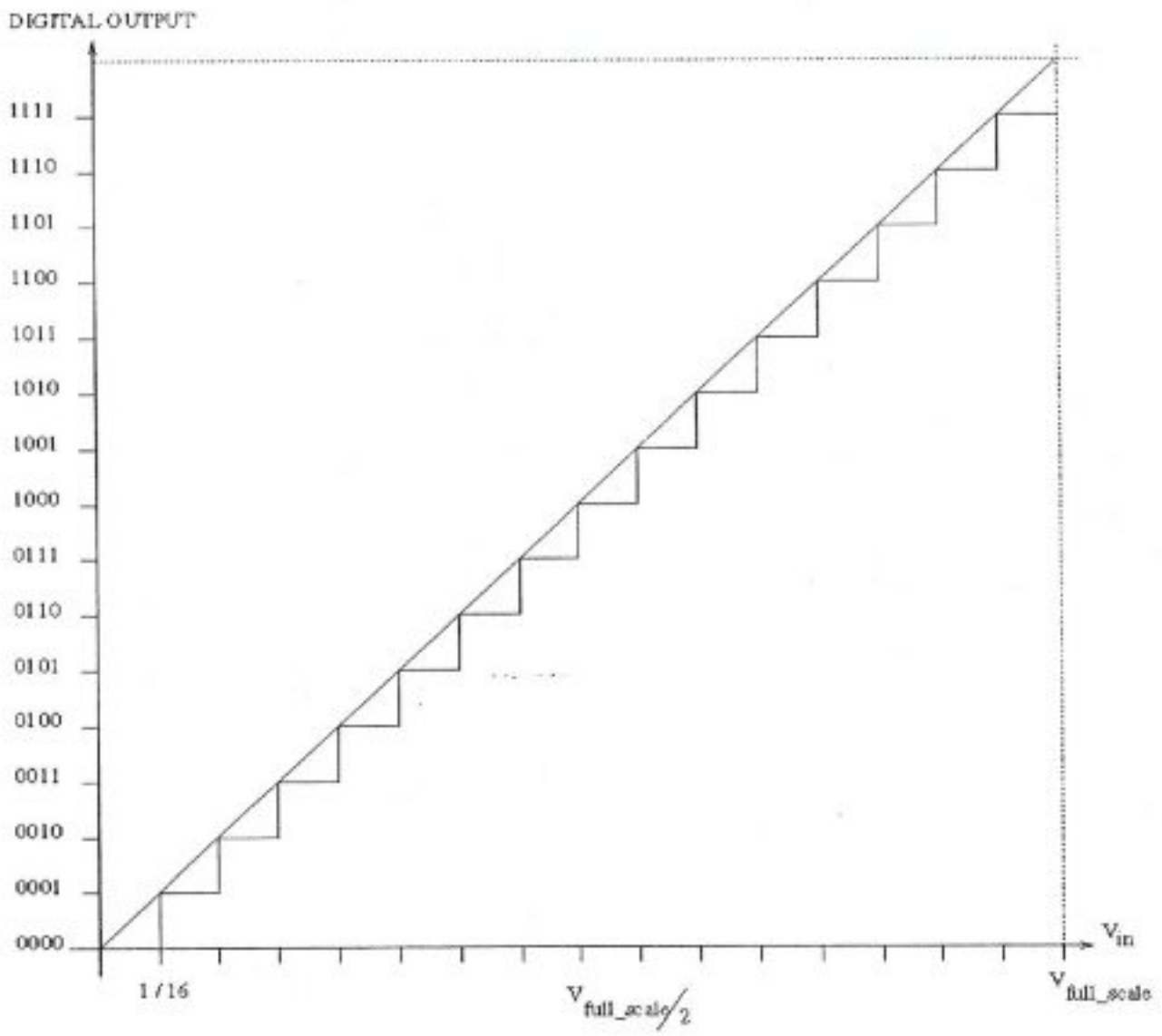


Figure 6.3 DC input-output characteristics of a 4-bit A/D converter.

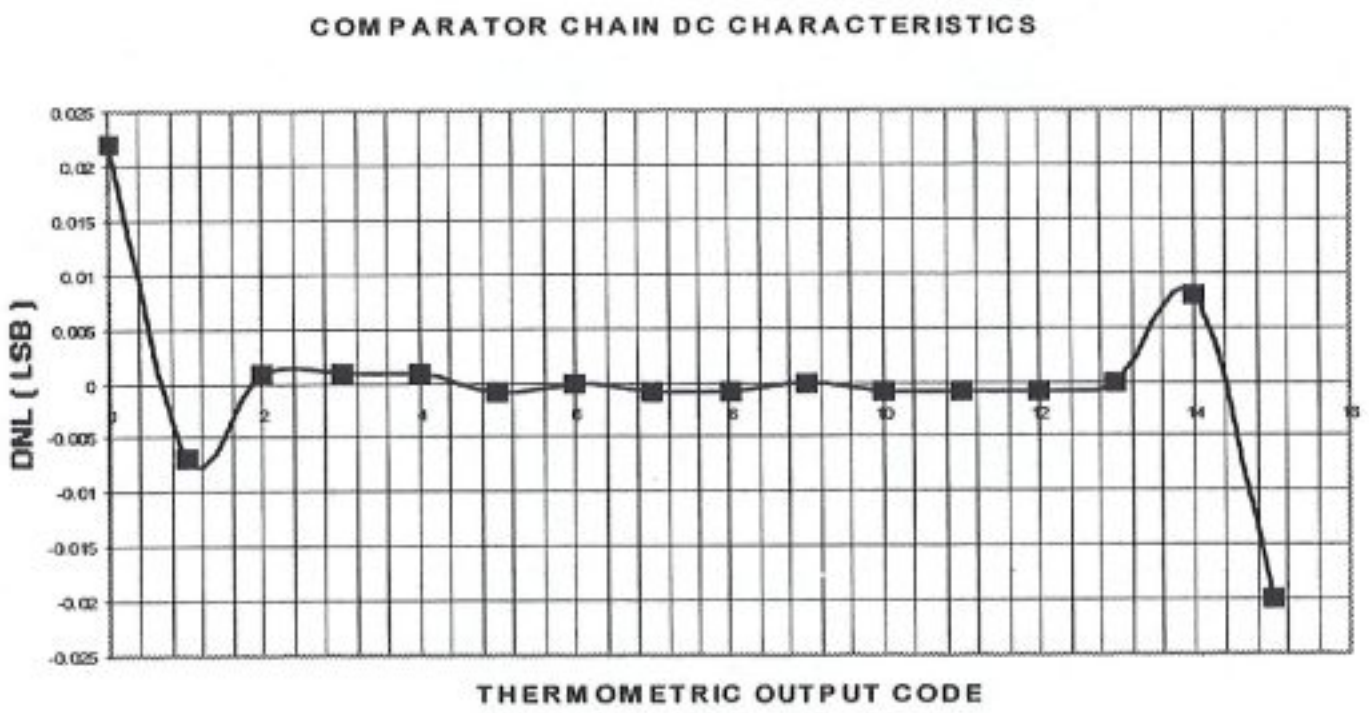


Figure 6.4 Typical corner DNL plot for 4bit A/D converter.

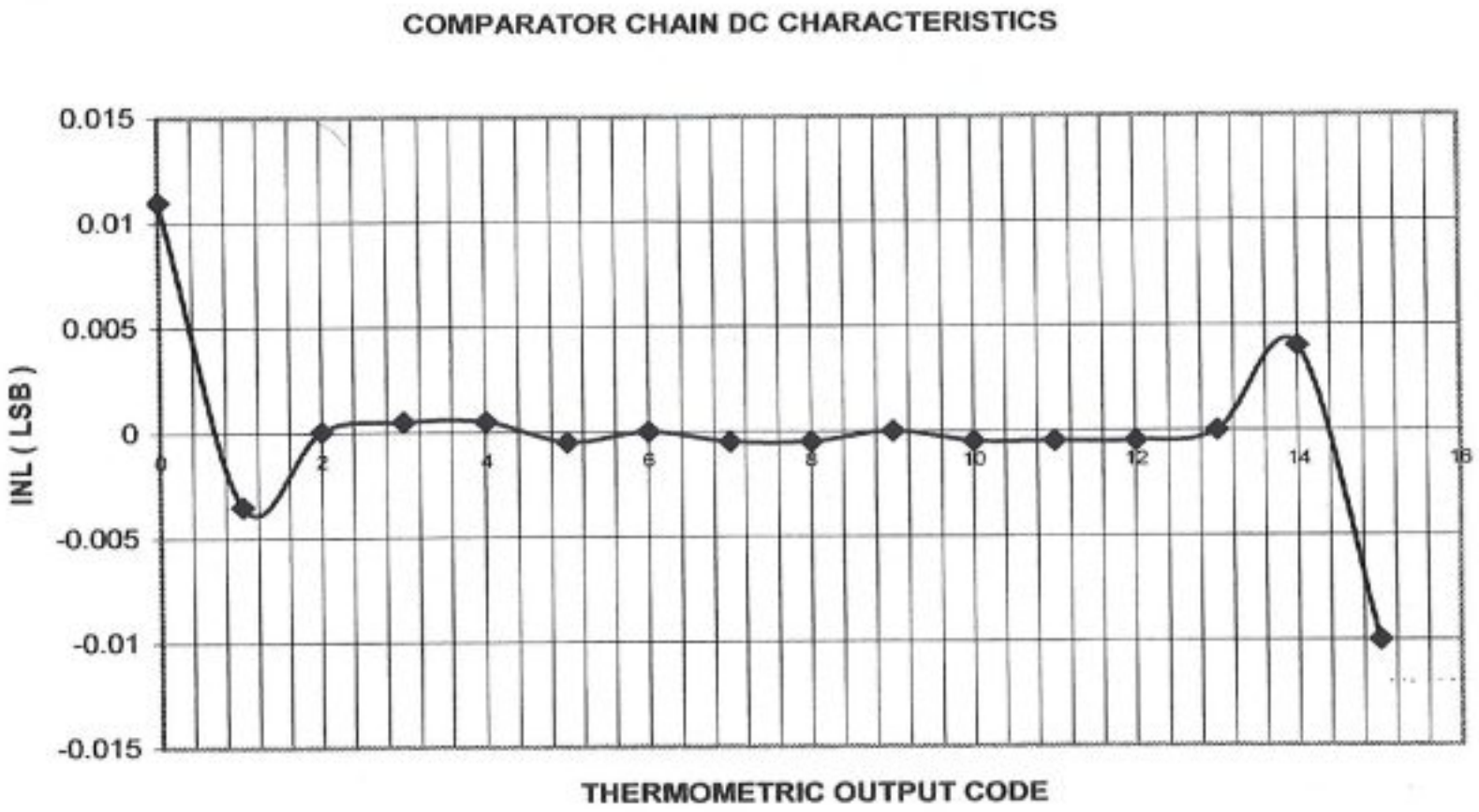


Figure 6.5 Typical corner INL plot for 4bit A/D converter.

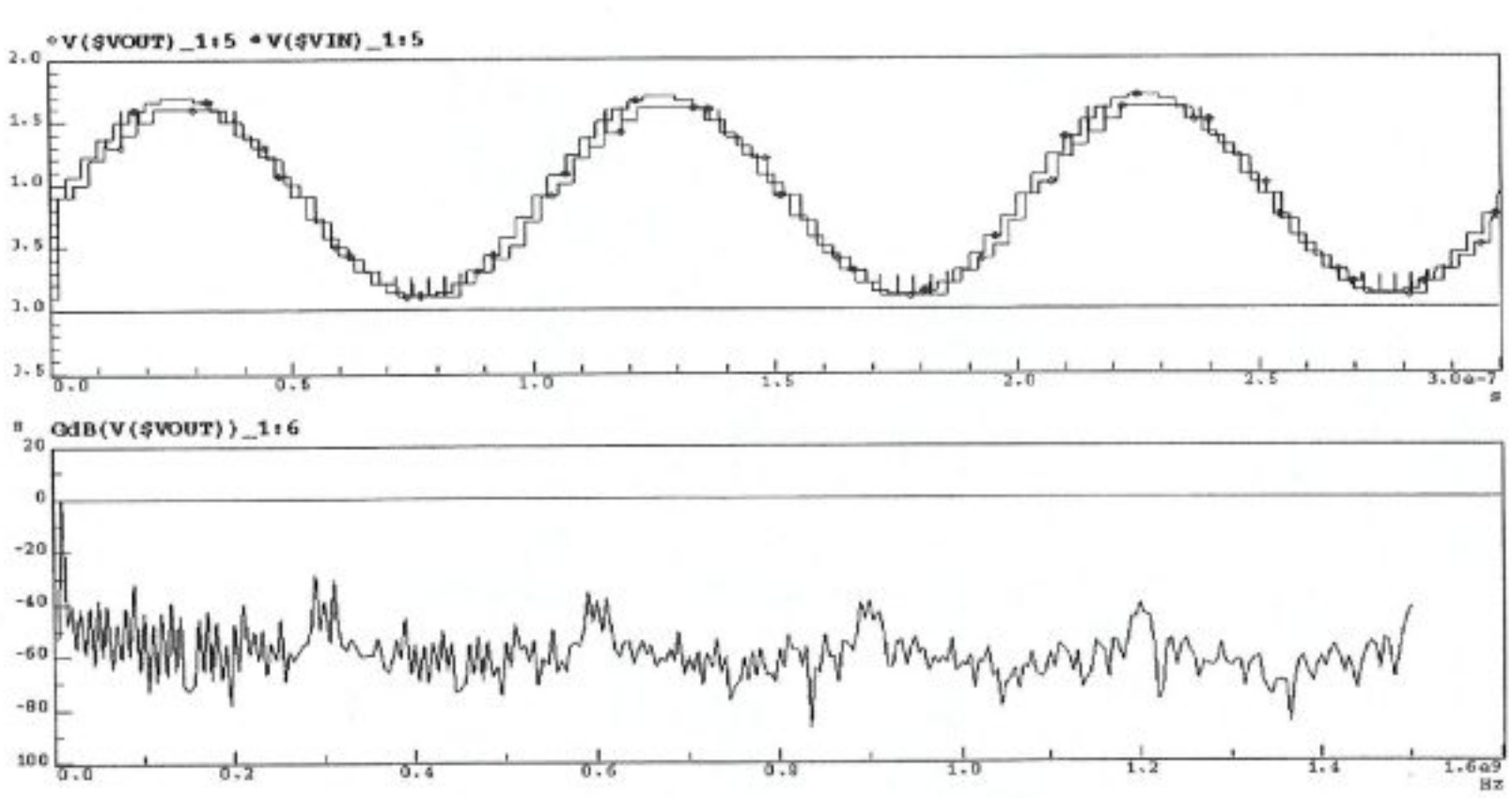


Figure 6.6 Typical FFT plot obtained for a 4-bit A/D converter when the input signal frequency is 10 MHz and the sampling clock frequency is 300 MHz.

To evaluate the dynamic performance of the ADC chain with transistor-level simulation, a sampled sinusoidal signal was applied to the input, and the resulting

thermometer code was converted back into the analog domain for comparison. Note that the sampling of the input signal as well as the digital-to-analog conversion were done using ideal circuit elements, so that the observed differences between the input and the output waveforms can only be attributed to the non-idealities of the 4-bit ADC circuit.

The signal-to-noise ratio (SNR) is calculated from Fourier transformation. The SNR is calculated by measuring the difference between the signal peak and the noise floor. Note that for discrete Fourier transformations, where only a finite number of samples are taken (K samples), the signal energy increases by a factor of K^2 while the noise energy increases by a factor of K. Therefore the SNR has to be calculated as the difference of the signal peak and the noise floor minus a correction term of 10log(K) Eq. 6.1. [25]

$$SNR(dB) = signal\ peak(dB) - noise\ floor(dB) - 10.\log(K) \qquad (6.1)$$

The simulated input and output waveforms, as well as the calculated FFT plot are shown in Figure 6.6 for a signal frequency of 10 MHz and sampling frequency of 300 MHz. Note that the signal peak is at zero "0" dB, the noise floor at –53.405 dB, and number of data samples (K) is 601 in Figure 6.6. Thus the SNR is equal to 25.616 dB, where the theoretical upper limit of the SNR value for a 4-bit A/D converter is 25.84 dB. Figure 6.7 shows the SNR in function of the sampling clock frequency in the case that the input signal frequency is constant at 10 MHz. It can be seen that the signal-to-noise ratio is relatively low for sampling frequencies that are close to the Nyquist limit, and that the SNR approaches the theoretical limit of 25.84 dB as the sampling frequency increases. Figure 6.8 shows the high frequency dynamic performance of the designed 4-bit A/D converter, again with an input signal frequency of 10 MHz. As expected, the SNR decreases gradually for sampling frequency values above 500 MHz, and drops by –3dB at about 1 GHz. Thus, the dynamic operation of the designed 4-bit ADC is verified to remain within acceptable limits, even for sampling frequencies of up to 1 GHz. Figure 6.9 shows the overall variation of the SNR with the sampling clock frequency, i.e., combining the information provided in Fig. 6.7 and Fig. 6.8. Finally, Figure 6.10 shows the SNR as a function of the input signal frequency in the case of sampling clock frequency held constant at 200 MHz. It can be seen that the SNR gradually drops from its near-ideal level of 25.2 dB at 10 MHz to about 22.7 dB at 80 MHz, as the signal frequency approaches the Nyquist limit of 100 MHz.

In order to achieve analog pipelining we still have to build-up a digital-to-analog converter, DAC. We need a high-resolution, high-speed, monotonic DAC in our work. We searched for different D/A converter topologies in the literature to find the most suitable one for our usage. A brief comparison will be given in the following section.

Figure 6.7 SNR of the 4-bit ADC as a function of sampling frequency, with input signal frequency of 10 MHz and the sampling clock frequency is varied from 50 MHz to 300 MHz.

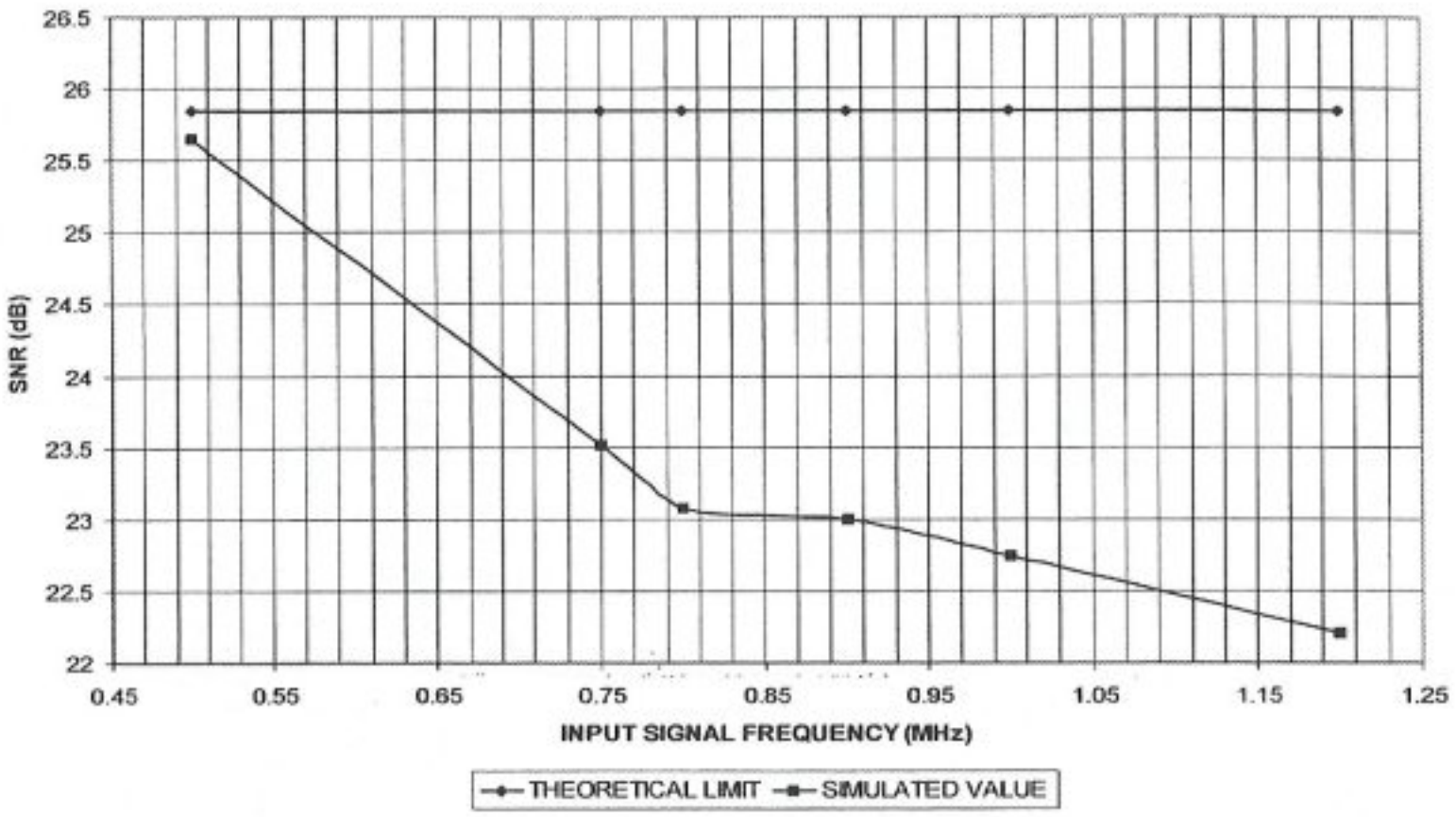


Figure 6.8 SNR of the 4-bit ADC as a function of sampling frequency, with input signal frequency of 10 MHz and the sampling clock frequency is varied from 500 MHz to 1.2 GHz.

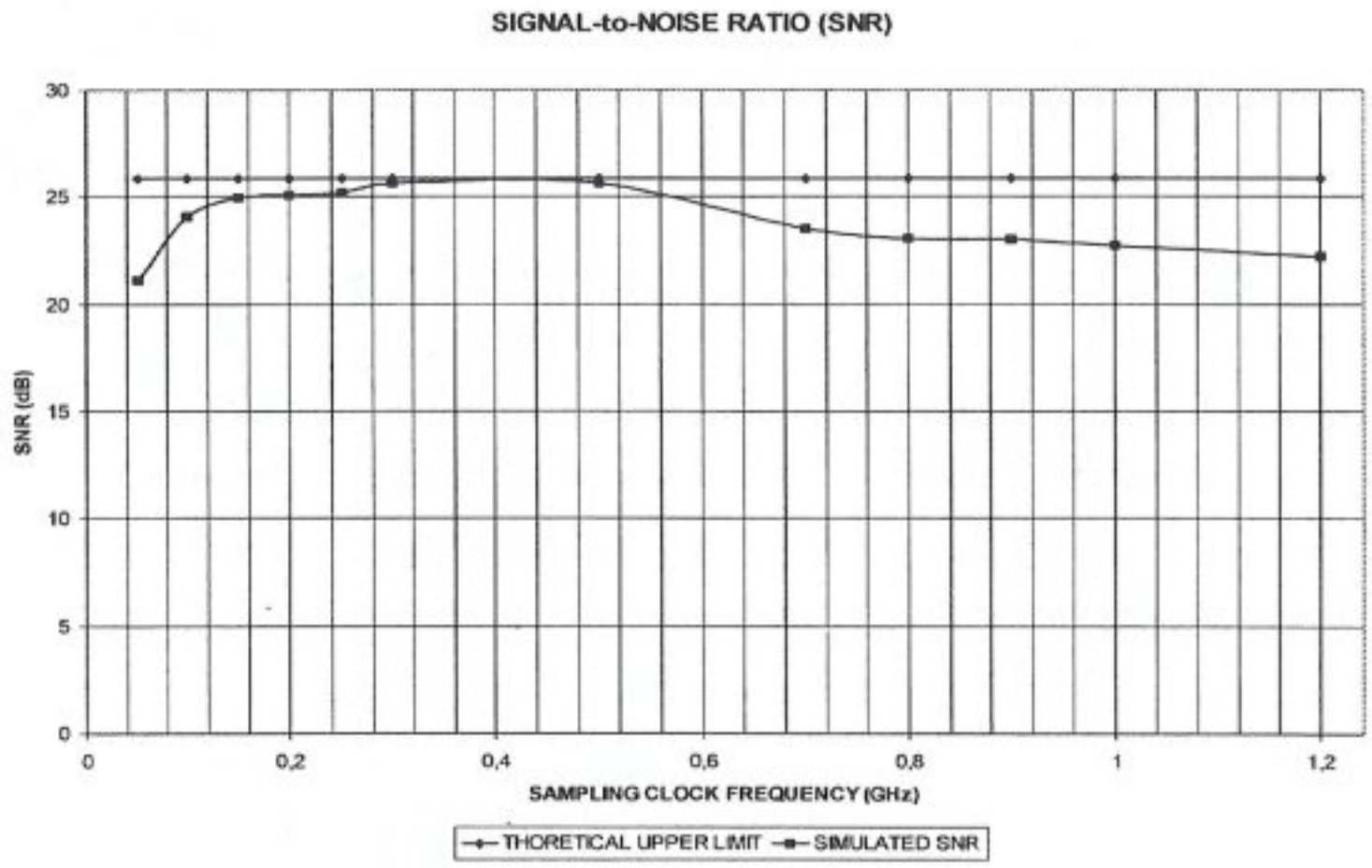


Figure 6.9 Overall variation of SNR as a function of the sampling frequency, with input signal frequency of 10 MHz.

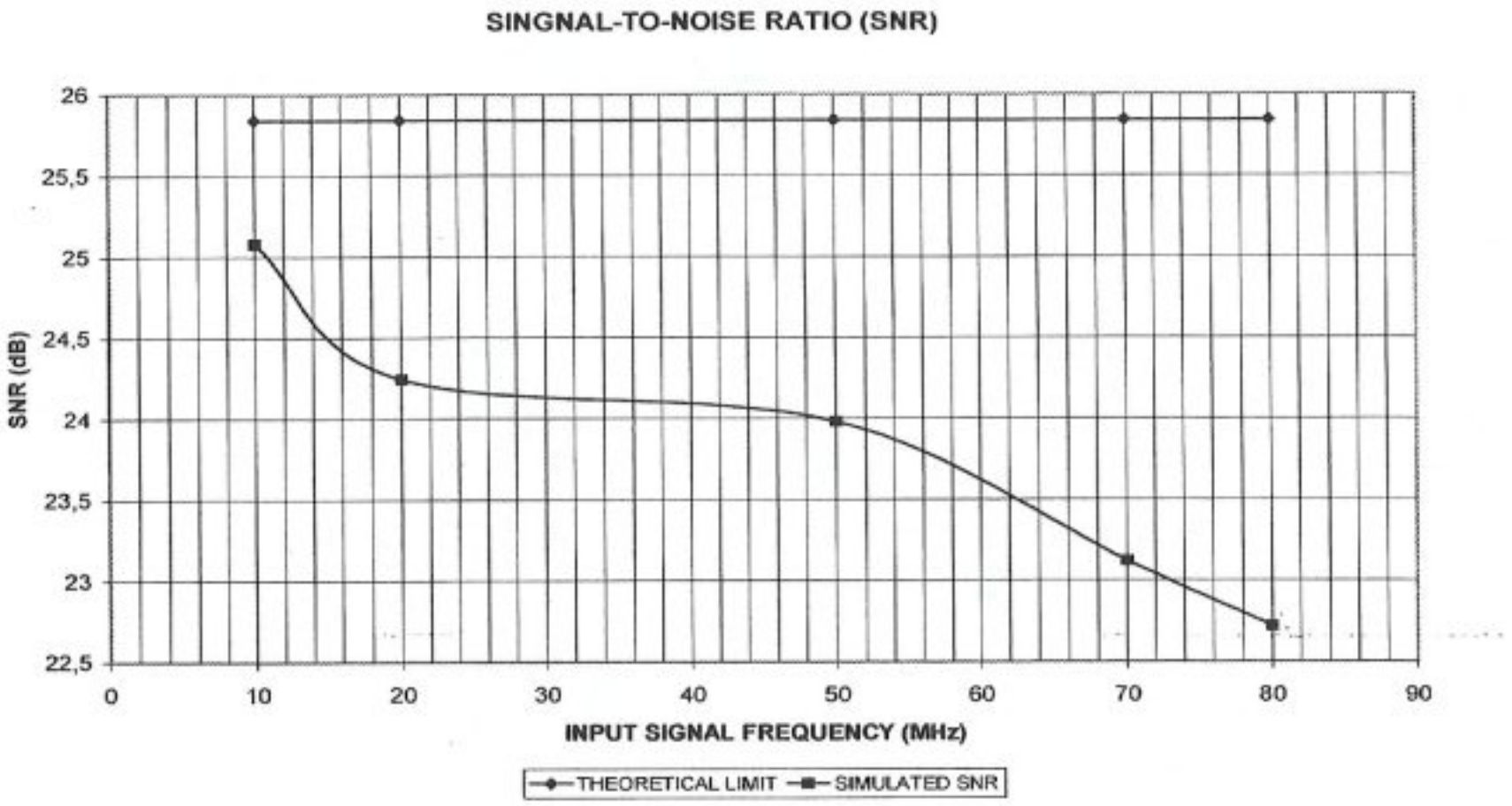


Figure 6.10 SNR of the 4-bit ADC as a function of input signal frequency, with sampling clock frequency of 200 MHz and the input signal frequency is varied from 10 MHz to 80 MHz.

6.2 Digital-to-Analog Converter Design

In general, an A/D conversion process will convert a sampled-and-held analog signal to a digital word that represents the sampled analog signal. The D/A conversion process is essentially the reciprocal of the A/D conversion process. Digital words are applied to the input of the D/A to create from a reference voltage an analog output signal that represents the digital word.

The ideal static behavior of a D/A converter is shown in Figure 6.11. The digital word is on the horizontal axis, which consists of all possible combinations of that word. Figure 6.11 is for a 3-bit digital word. The vertical scale is the analog output of the ideal D/A converter. For each digital word, there should be a unique analog output signal. Any deviations from Figure 6.11 fall into the category of static-conversion errors. These errors can affect the following characteristics: integral linearity, differential linearity, absolute linearity, resolution, zero and full-scale error, and monotonicity. All these

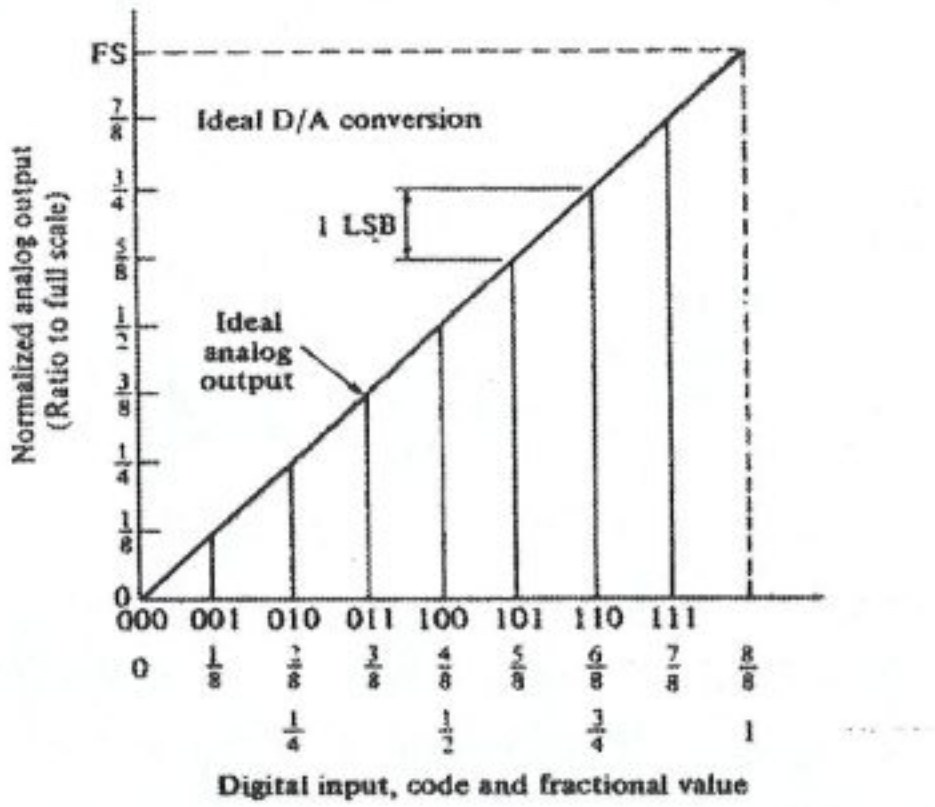


Figure 6.11 Ideal input-output characteristics for a three-bit D/A converter [3].

specifications define the accuracy of the converter, its static and dynamic performances. For detailed information on these specifications, please refer to chapter 2 because all specifications defined above are also the same for an A/D converter.

6.2.1 Current weighting D/A converter using ladder networks

There exist different systems using ladder networks to obtain accurate current weighting in the literature. These ladder networks are simple to implement in the integrated circuits. Furthermore, the very well matched value and thermal tracking of components on the same die improve the overall performance of the system. R-2R ladder network, resistor weighting current network, equal currents output ladder network, two-step current division network, binary weighted current divider and MOS ladder network are several examples for current weighting D/A converters.

Because of weighting used, the largest transistor has a size, which is 2^{N-1} times the size of the transistor in the least significant bit. Such a ratio in transistor sizes requires a large die size. Moreover, the output capacitance of the MSB current source is large due to the parallel connection of 2^{N-1} transistors. Such a large capacitance has a draw back on the latency of switching this current on and off to the output terminal. As a result it is difficult to operate all switches at the same speed, which will result in an output glitch.

Using more elements in parallel to generate the high current values, which simultaneously increase power consumption of the converter, increases the weighting accuracy [6].

6.2.2 Self-calibrating D/A converters

The system consists of a main D/A converter and a sub-D/A converter used to eliminate the errors in the main D/A converter. During calibration cycle an analog ramp is generated using a ramp generator. The output of the main D/A converter is compared with the ramp signal by a comparator. The correction logic generates a digital correction signal that is stored in a RAM unit. The RAM data control the sub-D/A converter to correct the output signal of the total D/A converter function to obtain the full ½ LSB integral nonlinearity. Main disadvantages of this topology are the required number of bits to be stored to correct the main D/A output and the fact that during calibration the D/A converter cannot be used for conversion [6].

6.2.3 Voltage and charge-scaling D/A converters

A very important component of a D/A converter is the accurate scaling of the reference voltage V_{REF}. The analog output is equal to this scaled value, which is determined by the digital word. Scaling is usually accomplished by the use of passive components, e.g., resistors or capacitors. Resistors are used to accomplish voltage scaling whereas capacitors are used to accomplish charge scaling.

Voltage scaling uses series resistors connected between the positive reference voltage, $+V_{REF}$ and negative voltage reference, $-V_{REF,}$ to obtain voltages between these limits. For an N-bit converter, the resistor string would have at least 2^N segments. An op-amp can be used to buffer the resistor string from loading effect of the switches used to control the output voltage level. Each tap is connected to a switching tree whose switches are controlled by the bits of the digital word. If the *ith* bit is "1", then the switches controlled by b_i are closed. If the *ith* bit is "0", then the switches controlled by b_i are opened (Figure 6.12).

It is seen that the voltage scaling D/A structure is very regular and thus well suited for MOS technology. An advantage of this architecture is that it guarantees monotonicity, for the voltage at each tap cannot be less than the tap below. The area

required for the voltage-scaling D/A converter is large if the number of bits is eight or more. Also, the conversion speed of the converter will be sensitive to parasitic capacitances at each of its internal nodes.

Charge-scaling D/A converters operate by binarily dividing the total charge applied to a capacitor array, or by just equally weighting the total charge applied to a capacitor array. It has been proved that the total number of capacitors in both structures will be 2^N (N is the number of bits of the converter). A two-phase nonoverlapping clock is used for this kind of converters. During the ϕ_1 the top and the bottom plates of all capacitors in the array are grounded. Next, during ϕ_2, the capacitors associated with bits that are "1" are connected to $+V_{REF}$ and those with bits that are "0" are connected to $-V_{REF}$. The output of the D/A converter is valid during ϕ_2 (Figure 6.13).

The accuracy of the capacitor and the area required are both factors that limit the number of bits used. The accuracy is seen to depend upon the capacitor ratios in the binary weighting charge-scaling DAC and to capacitor mismatch in equally weighting charge-scaling DAC. The ratio error for capacitor in MOS technology can be as low as

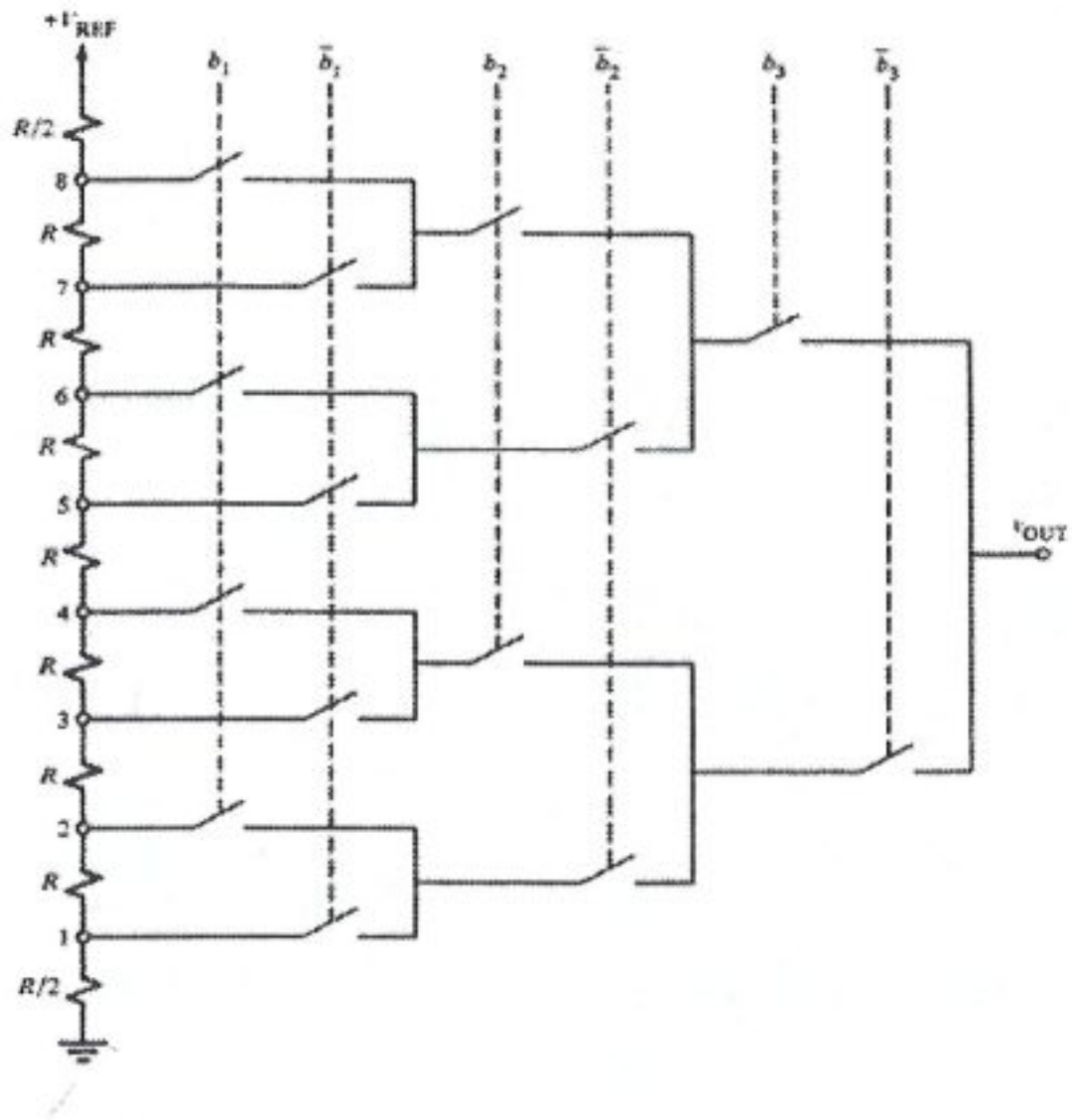


Figure 6.12 Implementation of a 3-bit voltage scaling D/A converter [6].

0.1%. If capacitor ratios were able to have this accuracy, then a D/A converter that is capable of 10-bit resolution could be realizable. However, this implies that the ratio between the MSB and LSB capacitors will be 1024:1 in the extreme case, which is undesirable from an area view point for a binary weighting charge-scaling D/A converter. Also, the 0.1% capacitor ratio accuracy is applicable only for ratios in the neighborhood of unity. As the ratio increases, the capacitor ratio accuracy decreases. But, for an equally weighting charge-scaling D/A converter, the total area can be expressed as $2^N C_{unit}$, which will result in a more desirable chip area. Moreover, response time of an equally weighting charge-scaling DAC is better than the binary weighting one due to the large capacitance appeared on MSB ($C_{unit}2^{N-1}$) because of the binary weighting structure. The working principle of an equally weighting DAC (MDAC) given in Figure 6.13 with only a single clock (ϕ_1) and its inverse (ϕ_2)– two phased working principle – instead of two non-overlapping clocks can be expressed as follows:

$$
\begin{aligned}
Q_{\Pr echarge} &= \sum C_{UNITi}(V_r - V_{in})in\overline{CLK} \\
Q_{Evaluation} &= \sum C_{UNITi}(V_r^{'} - V_{BITi})inCLK \\
where\, V_r^{'} &= V_r + \Delta V_r
\end{aligned}
\tag{6.2}
$$

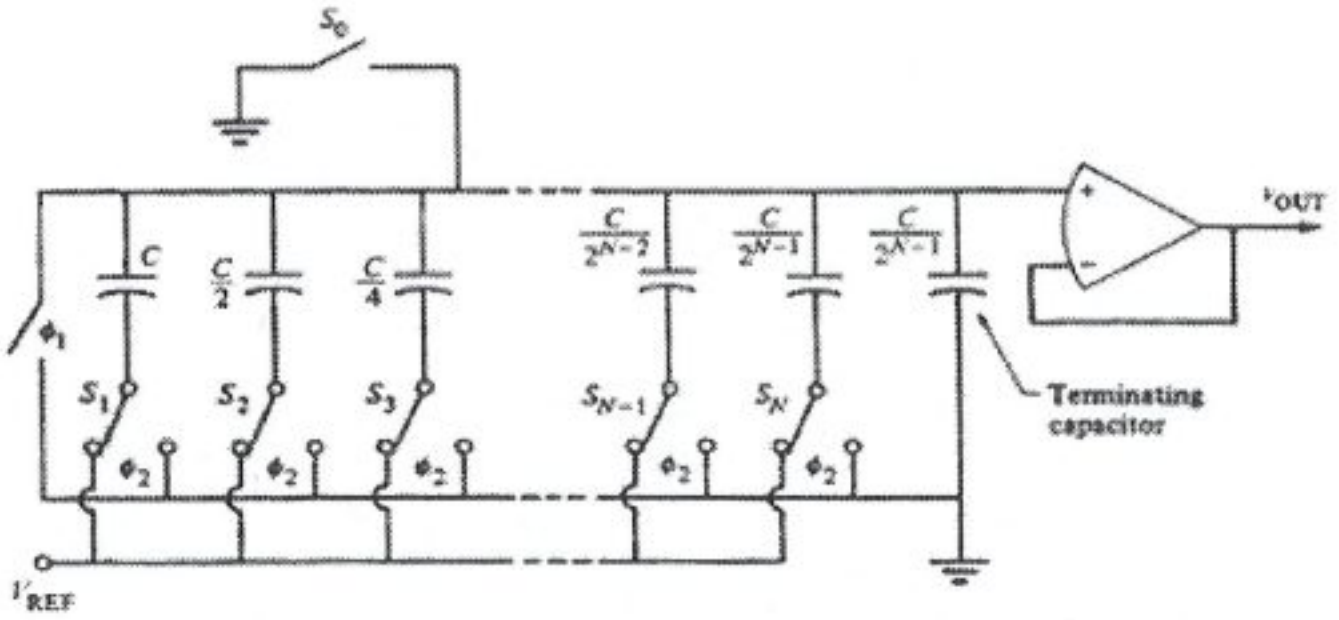


Figure 6.13 N-bit charge-scaling D/A converter schematic [6].

From the charge conservation principle these two charges stored on the MDAC_OUT node (Figure 6.11) should be equal to each other, $Q_{\Pr echarge} = Q_{Evaluation}$. Deriving ΔV_r (residue voltage) from this equality results in

$$\Delta V_r = \frac{1C_{UNIT}}{2^{N-1}C_{UNIT}} \sum V_{BITi} - V_{in} \tag{6.3}$$

The residue voltage formed at the output of MDAC is equal to the difference of the produced analog voltage in DAC and the input analog voltage to the pipeline stage. The value of this voltage is not dependent on the absolute unit capacitor value but on the ratio of the decoder capacitances. The influence of the capacitor ratio accuracy on number of bits of a charge-scaling D/A converter can be shown as follows:

The ideal output voltage of the charge-scaling D/A converter is,

$$V_{OUT}/V_{ref} = C_{equivalent}/NC_{UNIT} \tag{6.4}$$

Now assume that the worst-case output voltage is given as,

$$V'_{OUT}/V_{ref} = \frac{C_{equivalent}(\min)}{[NC_{UNIT} - C_{equivalent}](\max) + C_{equivalent}(\min)} \tag{6.5}$$

Then the difference between the ideal output and the worst-case output can be written as,

$$\left| V_{OUT}/V_{ref} - V'_{OUT}/V_{ref} \right| = \left| \frac{C_{equivalent}/NC_{UNIT} - C_{equivalent}(\min)}{[NC_{UNIT} - C_{equivalent}](\max) + C_{equivalent}(\min)} \right| \tag{6.6}$$

If we assume the worst-case condition occurs at the midscale, then the $E_{quivalent}$ becomes N/2Cunit. Therefore the difference can be expressed as,

$$\left| V_{OUT}/V_{ref} - V'_{OUT}/V_{ref} \right| = \left| \frac{N/4 - N/2\, C_{UNIT}(\min)}{N/2\, C_{UNIT}(\max) + N/2\, C_{UNIT}(\min)} \right| \tag{6.7}$$

Replacing C_{UNIT} (max) by C_{UNIT}+0.5ΔC and C_{UNIT}(min) by C_{UNIT}-0.5ΔC and setting the difference between the ideal and worst-case output voltage equal to +-0.5LSB results in the following equation

$$\left| \Delta C / C_{UNIT} \right| = 1/2^{N} \tag{6.8}$$

Consequently, as a result of this topology survey we decided to use an equal weight "Multiplying Digital-to-Analog Converter" (MDAC) in our pipeline stage. We preferred this topology because it is the most suitable one for our case regarding speed, power consumption, area, and linearity. We preferred using unit capacitors to be used for charge-scaling at the output of each fifteen comparators because we will use directly the thermometer code and its complement created at the falling edge of ϕ_1. Moreover, the subtraction process needed between the held input analog voltage and the reconstructed analog voltage by the DAC to achieve analog pipelining between two consequent pipeline stages can be done without any extra design steps. This voltage difference is named the *residue voltage* of the pipeline stage. This subtraction process is achieved by the help of two extra CMOS switches that simply connect the top plates of all capacitors in the array to analog input voltage instead of ground and bottom plates to a fixed reference voltage in ϕ_1 as given in Figure 6.14 [3].

The most challenging step in the design of an MDAC is to find the appropriate sizes of the complementary MOS switches that will result in low clock feedthrough, low series resistance, and high output driving capability. The later two specifications require wide MOS switches, while the first one requires narrow widths. Thus, simulations were done on the sizing of CMOS switches to identify the acceptable minimum width needed for the switch transistors. Consequently, aspect ratio of 5μm/0.18μm is used for all switches in the design.

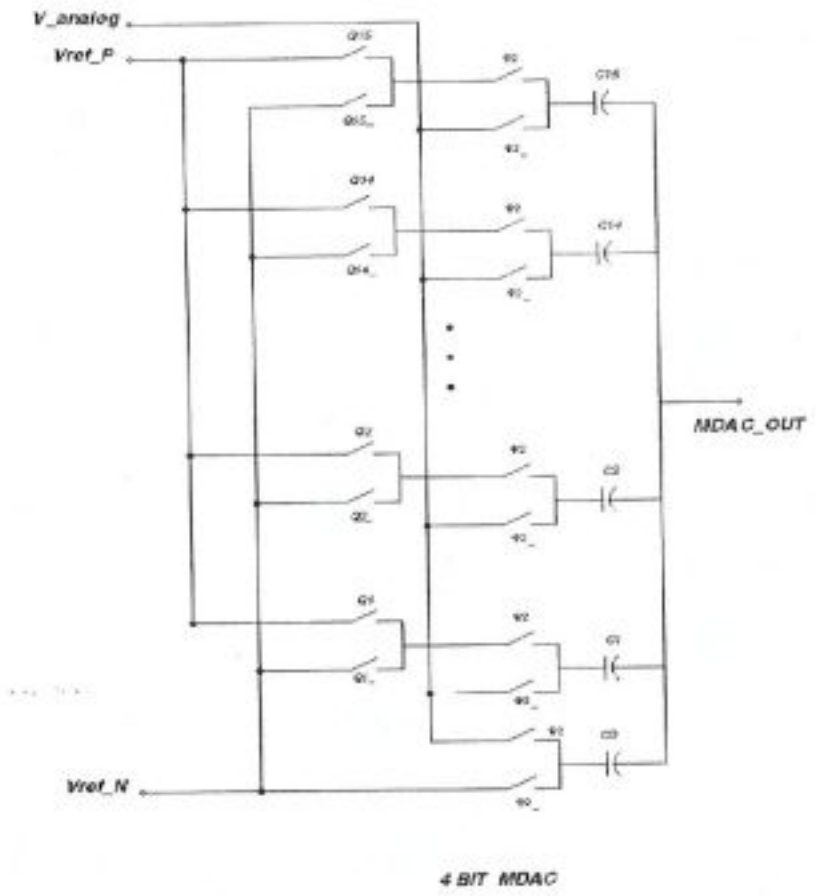


Figure 6.14 Schematic view of a 4bit MDAC.

Another important point in a charge-scaling D/A converter design is the identification of the value of the minimum acceptable unit capacitor. A unit capacitor of 50 fF is used in the design that provides needed speed and linearity specifications. Each unit capacitor can only be implemented as metal-metal capacitors due to the technology limitations. Thus, layouting this capacitance array is a great deal to be achieved. As mentioned before matching of these fifteen capacitors is more critical than their absolute value. Hence, we could say that matched capacitors form the basis of most data conversion products such as analog-to-digital and digital-to-analog converters. We can classify matching in three groups listed as follows:

- Minimal matching: Approximately ± 1% three-sigma mismatch, or 6 to 7 bits of resolution.
- Moderate matching: Approximately ± 0.1% three-sigma mismatch, or 9 to 10 bits of resolution.
- Precise matching: Approximately ± 0.01% three-sigma mismatch, or 13 to 14 bits of resolution. Suitable for precision A/D and D/A converters.

Precisely matched capacitors usually employ a thick oxide dielectric in conjunction with deposited electrodes. Junction capacitors have difficulty maintaining even minimal matching due to their extreme temperature dependence and the effects of out-diffusion. The following hints summarize the most important principles of constructing matched deposited-electrode capacitors.

- Use identical geometries for matched capacitors. Capacitors of different sizes or shapes match poorly; so matched capacitors should always use identical geometries. Unit capacitors should not be connected in series because differences between the parasitic capacitances of the upper and the lower plates will produce systematic mismatch.
- Use square geometries for precisely matched capacitors. Peripheral variations are a major source of random mismatch in capacitors. The smaller the periphery-to-area ratio, the higher the obtainable degree of matching. The square has the lowest periphery-to-area ratio of any rectangular geometry and therefore yields the best matching. Rectangular capacitors with moderate aspect ratios (2:1or 3:1) can be used to construct moderately matched capacitors, but precisely matched capacitors should always be square. In reality, the value of an integrated capacitor is not equal to the product of the specific capacitance ($\varepsilon_o\varepsilon_r / t_{ox}$) of the designed area of the plate. The etching that defines the plate proceeds under the protective mask (undercut effect) and reduces the designed area:

$$A_{eff} = (W - 2x)(L - 2x) \approx WL - 2(W + L)x = A - Px \tag{6.9}$$

where A is the designed area and P is the perimeter. Thus, the effective area is smaller than the designed area by an amount proportional to the perimeter of the plate. Thus, in order to also match the reduction effect due to undercut, it is necessary to keep the area-perimeter ratio as small as possible.

- Make matched capacitors as large as practical. Increasing the size of capacitors reduces random mismatch as well as dividing large capacitors into practical sized parts, which will introduce cross coupling that will minimize gradient effects and improve overall matching.

- Place matched capacitors adjacent to one another. If large number of capacitors is involved, they should be arranged to forma rectangular array having as small an aspect ratio as possible. Adjacent rows of unit capacitors should have equal spacing between them, as should adjacent columns of unit capacitors.
- Place matched capacitors over field oxide. Matched capacitors should always reside over field oxide well away from the edges of moat regions and diffusions.
- Connect the upper electrode of a matched capacitor to the higher-impedance node, because this generally exhibits less parasitic capacitance than the lower electrode. If substrate noise coupling is a concern, consider placing a well under the entire array.
- Place dummy capacitors around the outer edge of the array. Both electrodes of each dummy capacitor must be connected to prevent static charges from accumulating on the dummy electrodes and interfering the operation of adjacent devices.
- Electrostatically shield the capacitor array. Electrostatic shielding provides several benefits. First, it contains fringing fields to the capacitor array, thereby eliminating the need for wide arrays of dummy capacitors. Second, it allows leads to route over the capacitors without causing mismatch or noise injection. Third, it prevents electrostatic fields from adjacent circuitry from interfering with the matched capacitors. Fourth, it reduces the effects packaging stress on the underlying capacitors. All precisely matched capacitors should be electrostatically shielded, and this shielding should extend over the dummies placed around matched capacitor array.
- Cross-coupled array capacitors preferred. Cross coupling minimizes the effects of oxide gradients on capacitor matching and provides protection against stress and thermal gradients.
- Consider the number of the leads connected to the matched capacitor.
- Do not run leads over matched capacitors unless they are electrostatically shielded.
- Use thick-oxide dielectrics in preference to thin-oxide or composite dielectrics.

- If possible, place capacitors in areas of low stress gradients. The stress distribution reaches a broad minimum in the middle of the die.
- Place matched capacitors well away from power devices.
- Place precisely matched capacitors on axes of symmetry of the die [16].

Concerning all the explained properties of the capacitor array that will be used in the multiplying D/A converter and all the hints given above to help the designer to be able to layout matched capacitor arrays we decided to draw the sixteen unit capacitors as square shapes in a common-centroid form, and also in order to be able to reduce the occupied area by each unit capacitor we draw each unit capacitance in fractals. Hence, every fringe capacitor value will also be added to the total capacitance value. What is more, we will place this capacitor array in an N-well in order to be able to shield the array from the substrate noise. We also draw each unit capacitor as a sandwich made up of consequent metal layers (up to metal 5) connected in series (Figure 6.15). Thus, in order to construct 50 fF of unit capacitors we will consume less area than the area of a single sheet capacitor. Reduction in the area will further increase matching between array elements.

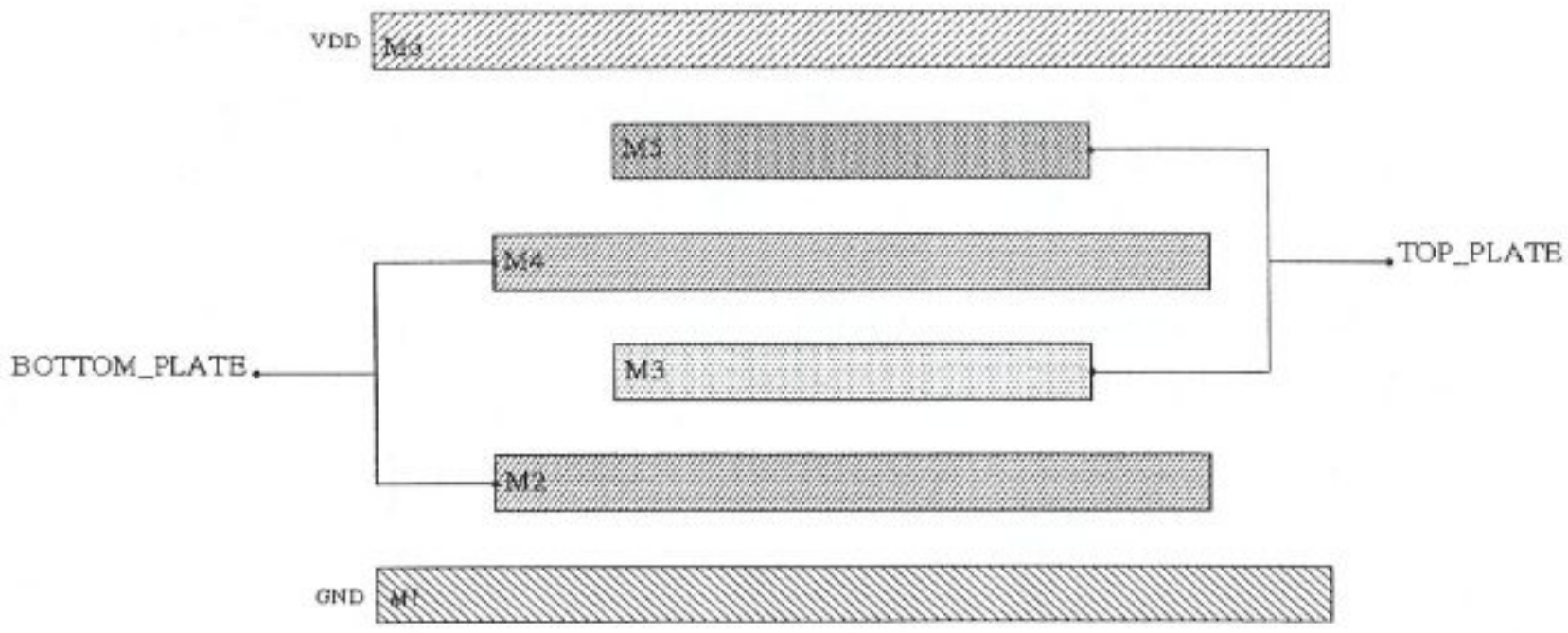


Figure 6.15 Simplified cross-section representation of metal-metal capacitors constructed in N-well. Note that N-well is not shown in figure for simplicity.

The ADC/MDAC structure that was described here takes the held analog input voltage, compares it with the reference voltages created by a resistor divider through the

comparators and reconstructs the digitally represented analog signal via the MDAC into analog format again. Then, we subtract that reconstructed analog signal from the held input voltage. Now the residue voltage is ready at the output of the D/A converter. If not any unpredictable conversion error arises, by definition this residue voltage must not be bigger than |-100mV| in our 4-bit A/D converter. In order to achieve pipelining now we have to amplify this residue voltage to full scale by the help of a residue amplifier. Note that, the full scale for the pipeline stages following the first stage should be half the input swing range of the first stage in the A/D converter. This is needed because we will use bit-overlapping technique in the digital pipeline in order to be able to correct any conversion error that can arise in the preceding stage. Thus, an op-amp with a closed loop gain of X8 is needed as the residue amplifier. The high open loop-gain OTA based op-amp will be used in negative feedback configuration (Figure 5.29). The residue voltage formed on the unit capacitors of the MDAC will be rapidly sinked to ground through the feedback resistors and the output stage of the op-amp, which is the same problem faced with the sample-and-hold amplifier. Thus, the same solution will be applied here. A unity gain OTA based op-amp designed (refer to chapter 5) will be placed in between the DAC output and the series feedback resistor. Consequently only a MOS transistor's gate will be seen by the DAC output thus, no charge will be lost (Figure 5.29). The amplified residue voltage at the output of the residue amplifier will be used as the held input voltage by the proceeding pipeline stage. In order to hold this amplified residue voltage constant during the sensing phase of the comparators of the proceeding stage a sample-and-hold circuit must be introduced. What is more, as explained before, the algorithm used in a MDAC being charge-scaling, any voltage changes on the top plate of the unit capacitor will be reflected directly to the D/A converter's output. In order to prevent this phenomenon and to be able to hold the amplified residue constant during the conversion phase of the proceeding stage, we buffered the comparator outputs of the flash A/D converter via the sampling clock. Thus, the comparators will keep their previous state up to the next decision time. In other words sensing the phase of the comparators will be invisible to MDAC capacitors. Thus, the residue voltage will be constant for a half period of sampling clock, and the same is true for the amplified residue voltage. Simulated residue and amplified residue voltages are given respectively in Figure 6.16 and Figure 6.17 for typical corner silicon Spice parameters. Also, the variation of these two voltages with respect to the analog signal applied at the input of the pipeline stage is provided in Figures 6.18 and 6.19. It

can be seen that the amplified residue signal has the expected saw-tooth shape that corresponds to the difference between the analog input level and the quantized output levels. The transitions are perfectly linear, the amplitude of the signal is 800 mV (with a maximum error of ± 4.7 mV) and the amplified residue signal remains with in (± 10 mV) of the ideal upper and lower boundaries, i.e. 0.5 V and 1.3 V, respectively. With these properties, it can be verified that each pipeline stage is capable of producing the output bits with the desired accuracy.

In Figures 6.20 and Figure 6.21, the time-dependent variation of the residue voltage and the amplified residue voltage are given for a sampling clock frequency of 50 MHz, respectively. Note that the residue voltage and the amplified residue voltage have more time to settle until the next falling edge of the clock signal arrives, and consequently, the accuracy of the pipeline stage response is expected to increase at lower sampling frequencies. The exact variation of the residue voltage as a function of the input voltage level was not produced at 50MHz, since the results obtained for 200 MHz sampling frequency are already quite adequate for the desired bit-precision.

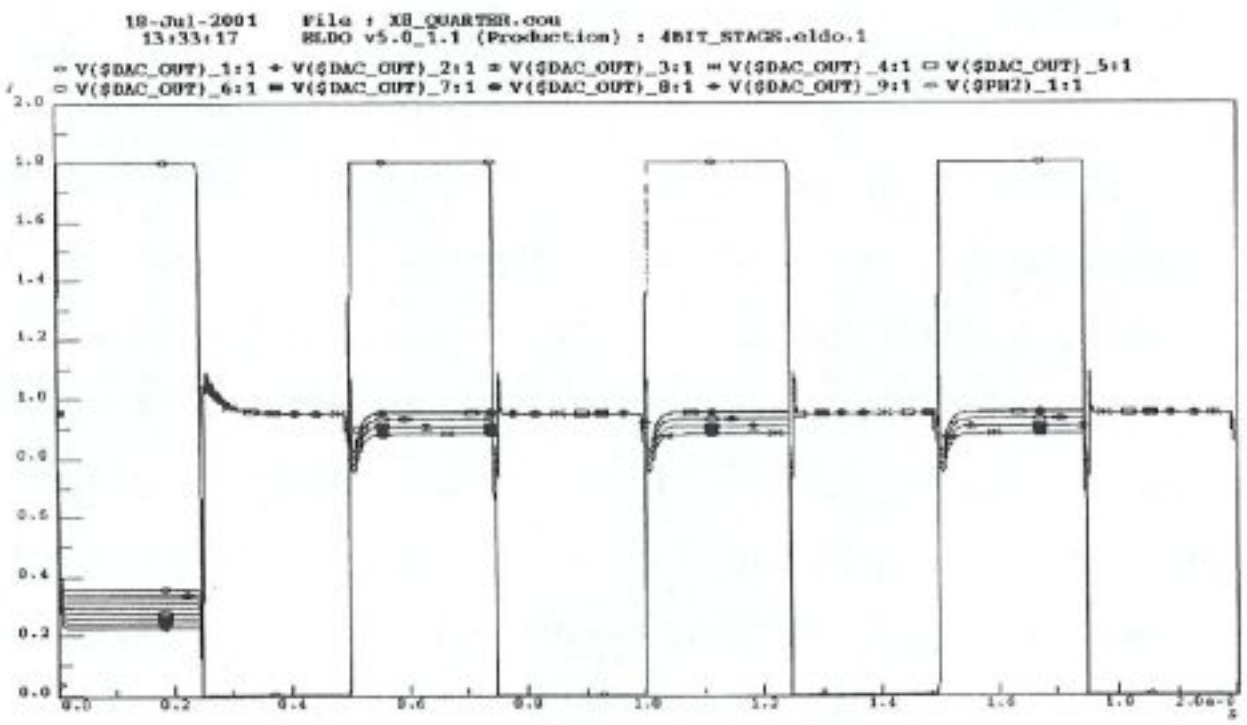


Figure 6.16 Residue voltages obtained for different input voltage levels applied to the input of the 4-bit pipeline stage. The sampling clock frequency is 200 MHz.

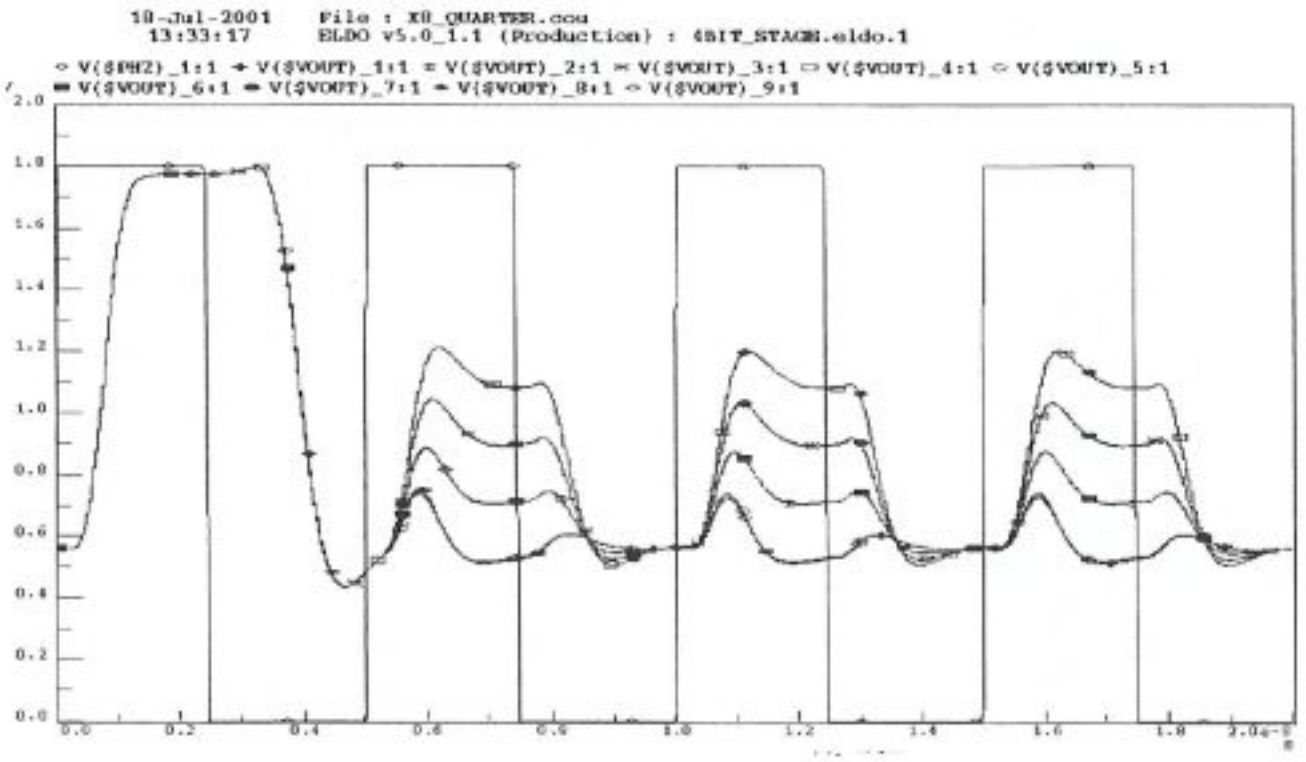


Figure 6.17 Time-dependent variation of the amplified residue voltage, with a sampling clock frequency of 200 MHz.

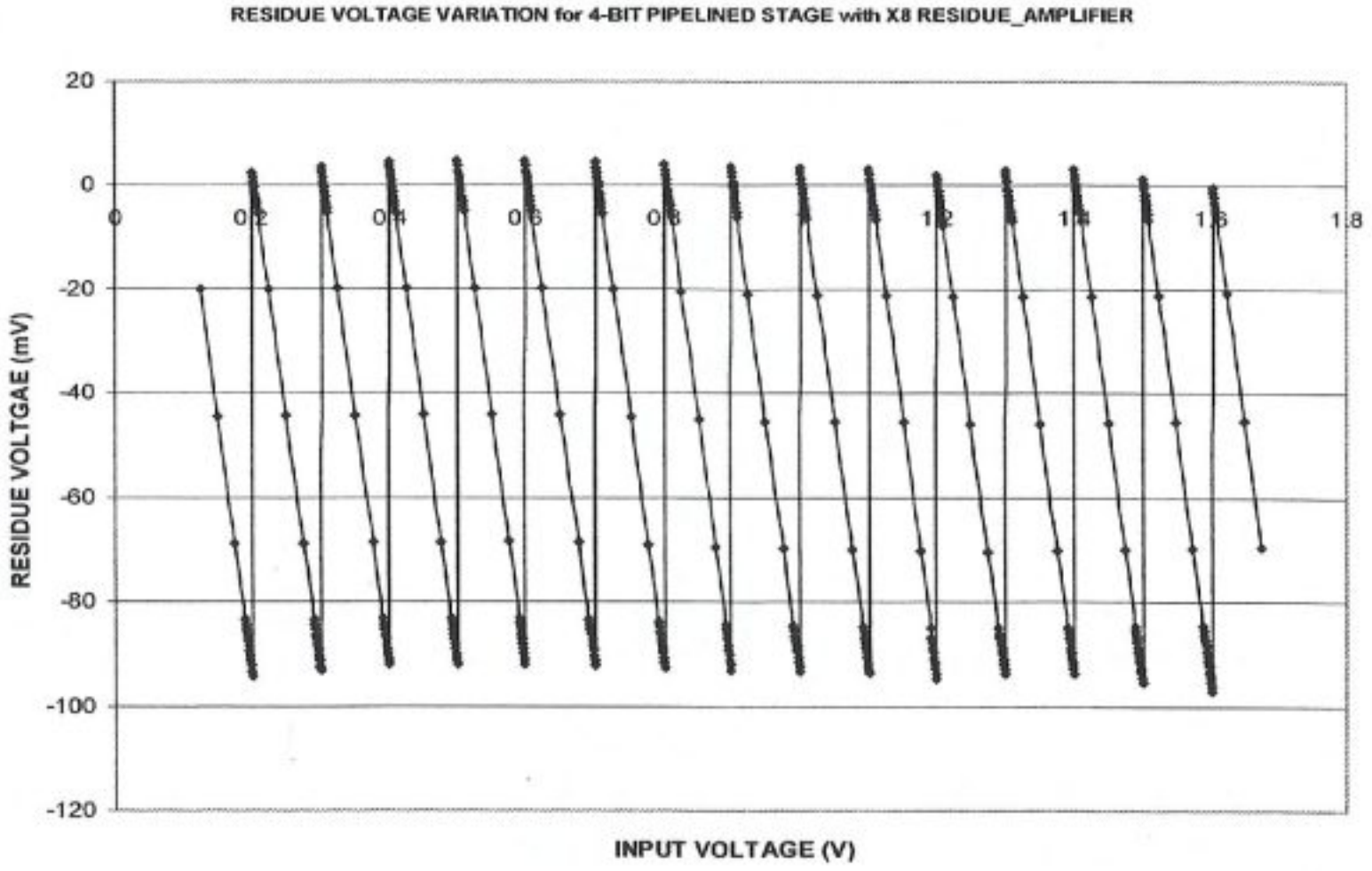


Figure 6.18 Residue voltage obtained versus input voltage for typical simulation corner at 200 MHz sampling rate.

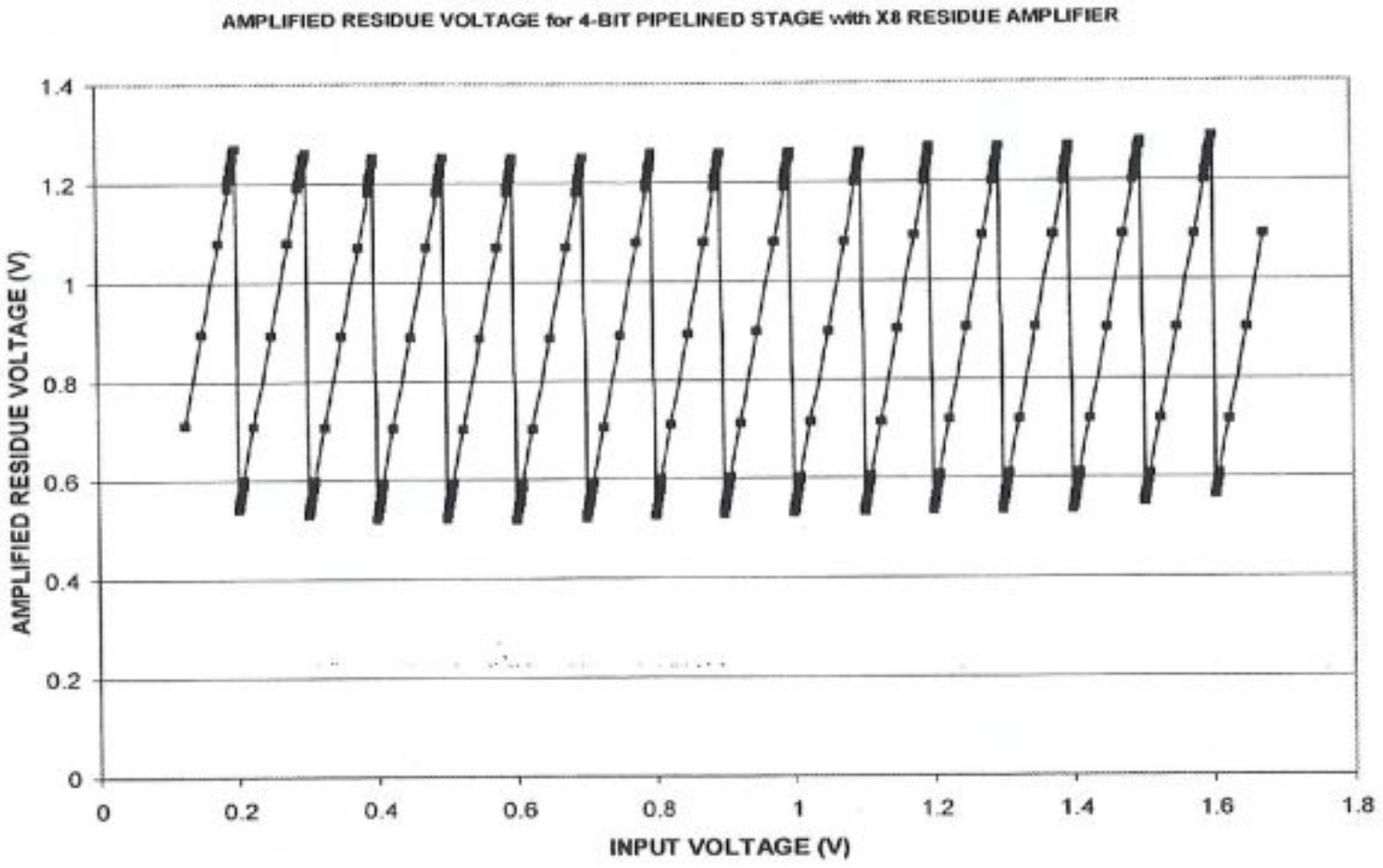


Figure 6.19 Variation of the amplified residue voltage given in Figure 6.19 as a function of the input voltage level, with X8 amplification factor.

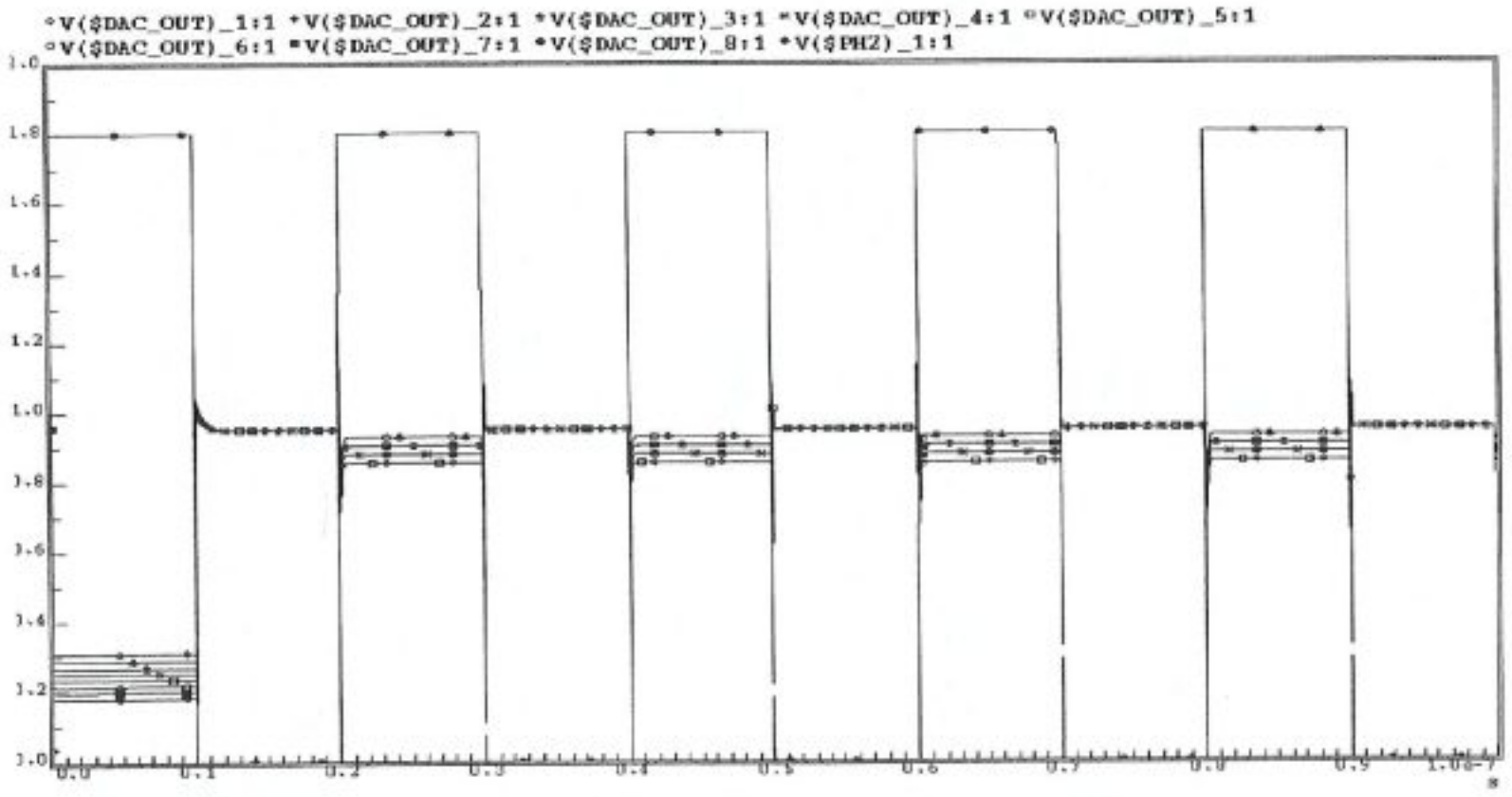


Figure 6.20 Residue voltages obtained for different input voltage levels applied to the input of the 4-bit pipeline stage. The sampling clock frequency is 50 MHz.

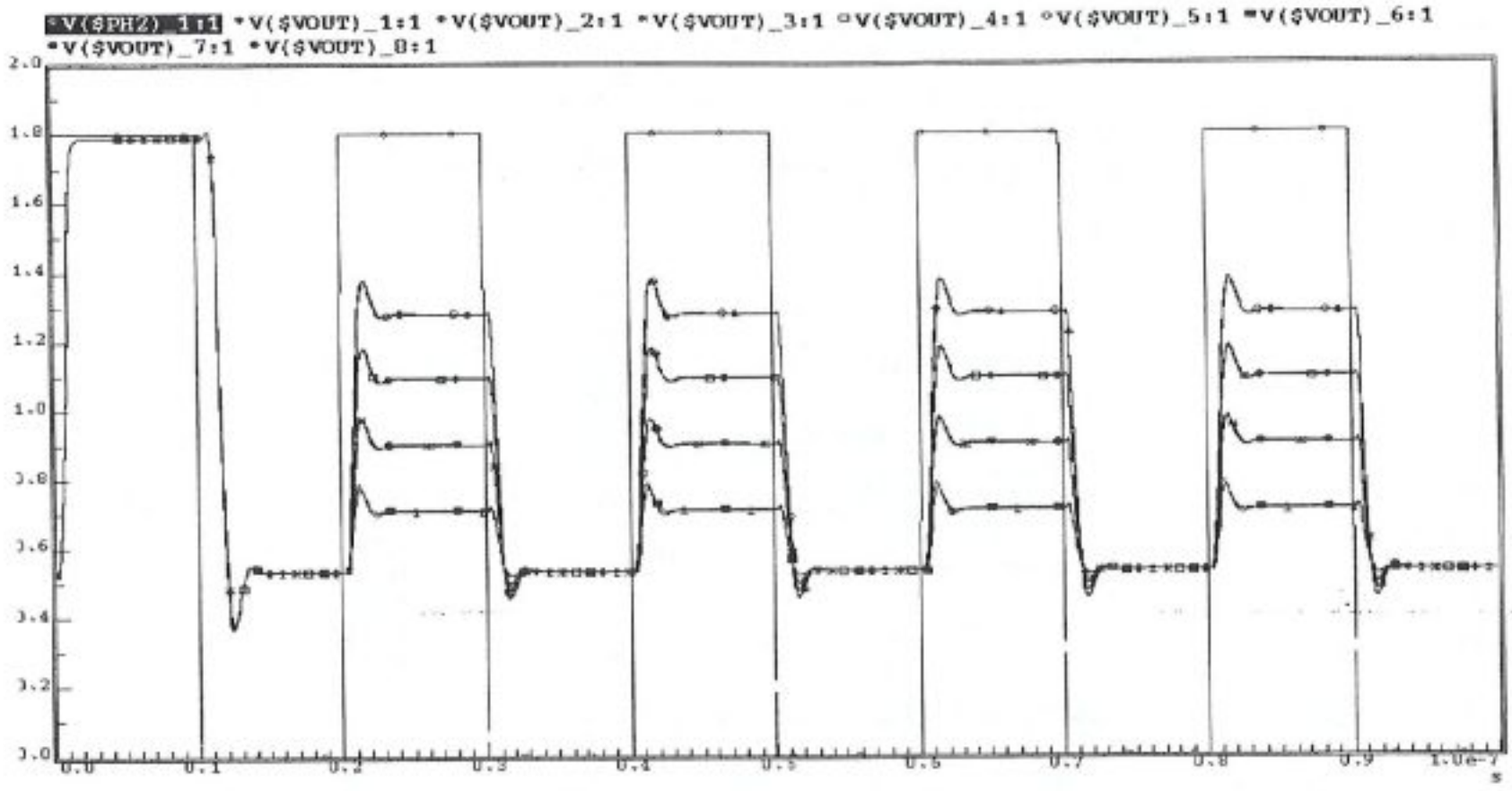


Figure 6.21 Time-dependent variation of the amplified residue voltage, with a sampling clock frequency of 50 MHz.

6.3 Error Correction with Bit-Overlapping

As mentioned before we decided to use "bit-overlapping" technique to achieve error correction. We choose this architecture because of its simplicity. In order to be able to use this technique we have to design more precise comparators to be used in the pipeline stages that follow the first one. We used "single bit-overlapping" technique thus; we had to decrease the input signal swing to one half of its original in the proceeding pipeline stages. This phenomena is established by amplifying the residue voltage produced in the preceding stage by "8", which will result in a halved input signal swing of 800 mV_{pp} where the original input voltage swing is 1.6 V_{pp}. Thus, the amplified residue voltage will be 800 mV_{pp} with a DC offset of 0.9V. Up to this point no error correction is done. Coding errors will arise if the previous stage's residue signal is greater than 1LSB. Causes of this kind of errors were examined in Chapter 2. Error correction is introduced in digital pipeline by designing a clever encoder (Figure 6.22) that can distinguish the possible *over / under flow* states from the decoded 4bits of the

related pipeline stage (pipeline stages 2, 3 and 4). The encoding technique used in these stages is explained in detail in Table 6.1. For example, if the amplified residue of the first stage is greater than 1.3 volts an *over flow* state occurs. The following analog pipeline stage will produce the thermometer code representing this analog input voltage, and an over-flow flag (A = 1) will be produced by the 12th comparator's "Q" output as the 4th MSB bit of the related pipeline stage in the clever encoder circuit. This raised over-flow flag will be added to the preceding pipeline stage's output and the rest of the digital word produced (3bits), will be concatenated to the resulting digital code (Figure 6.23). If the amplified residue of the first stage is less than 0.5 volts an *under flow* state is occurred. The following analog pipeline stage will produce the thermometer code representing this analog input voltage, and an *under flow* flag (B = 1) will be produced by the 4th comparator's "$\overline{Q}$" output as the 4th MSB bit of the related pipeline stage in the clever encoder circuit. This raised under-flow flag will be subtracted from the preceding pipeline stage's output and the rest of the digital word produced (3bits), will be concatenated to the resulting digital code (Figure 6.23). And if the amplified residue of the stage is in between the 0.5V-1.3V range than "0" will be added to the following stage's 4-bit output and produced 3-bits will be concatenated to the resulting digital code (Figure 6.23).

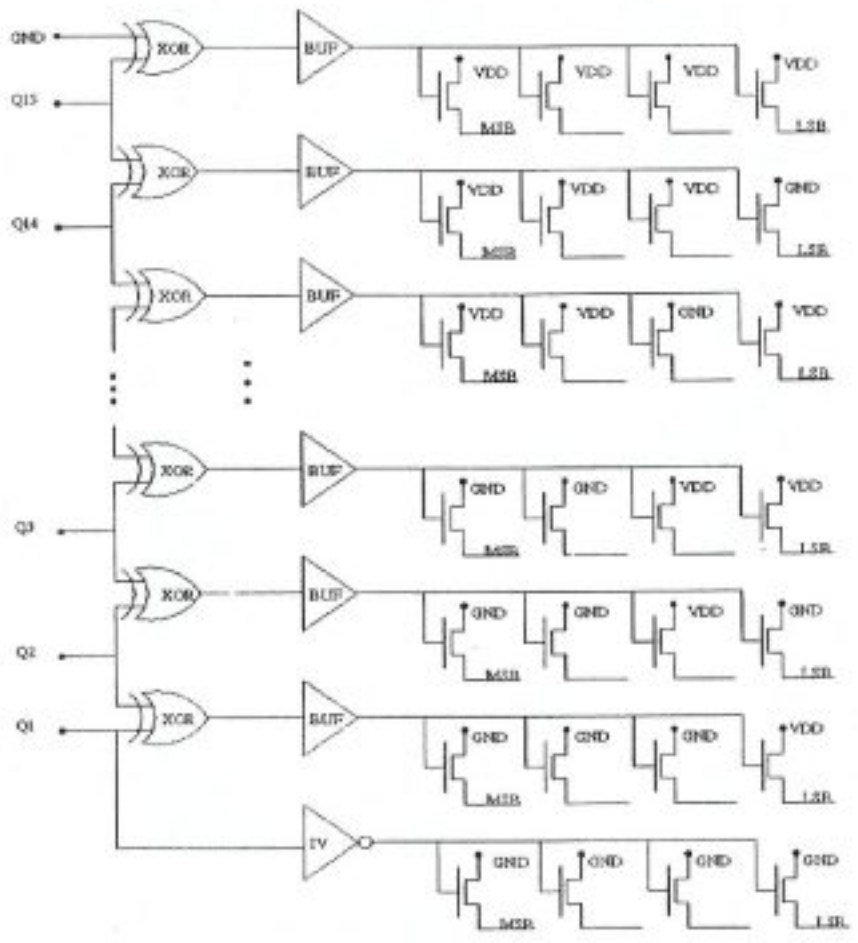
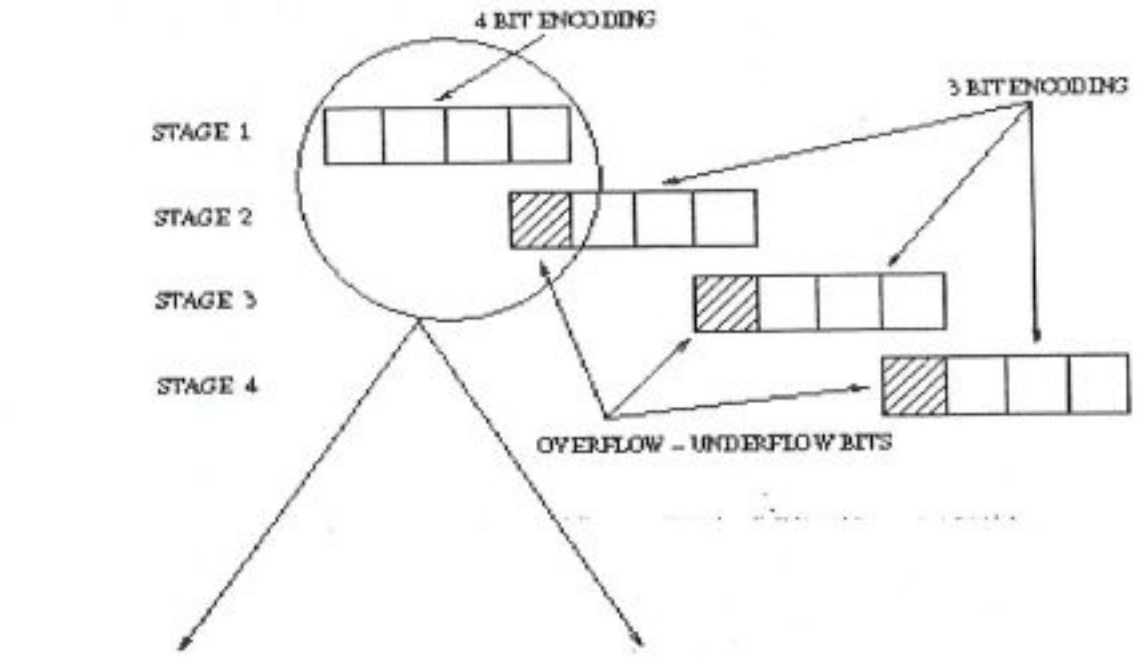
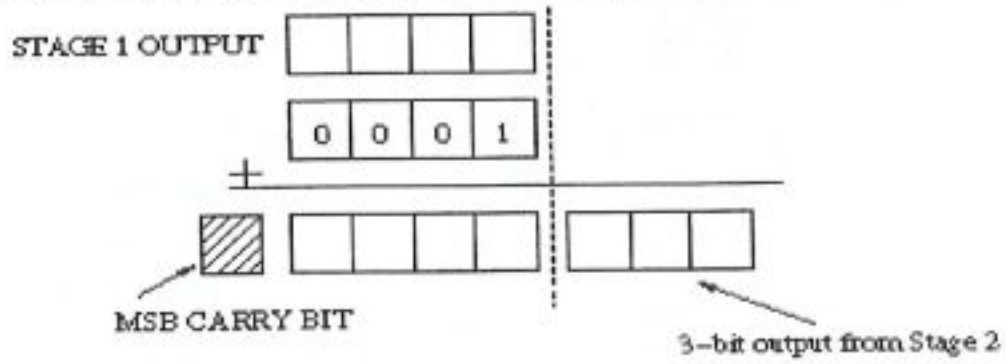


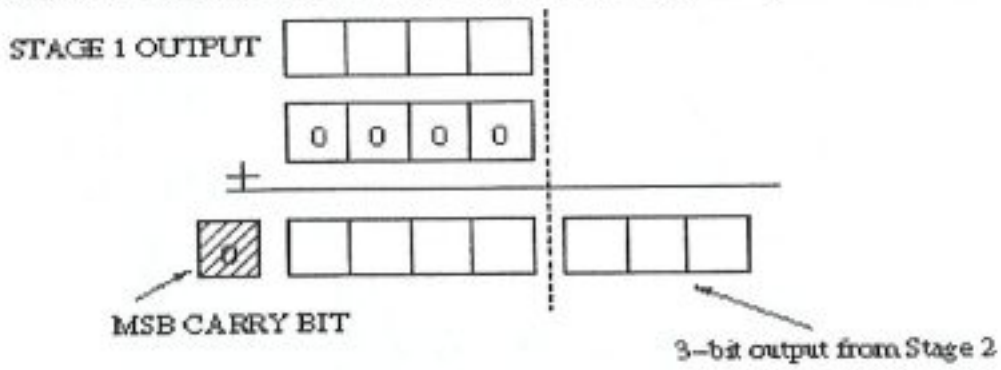
Figure 6.22 Simplified schematic view of a 4-bit encoder block used in stage 1.



1. OVERFLOW CONDITION : Add 0001 to Stage 1 output and concatinate 3–bit output from Satge 2



2. NORMAL RANGE CONDITION : Add 0000 to Stage 1 output and concatinate 3–bit output from Satge 2



3. UNDERFLOW CONDITION : Subtract 0001 from Stage 1 output and concatinate 3–bit output from Satge 2

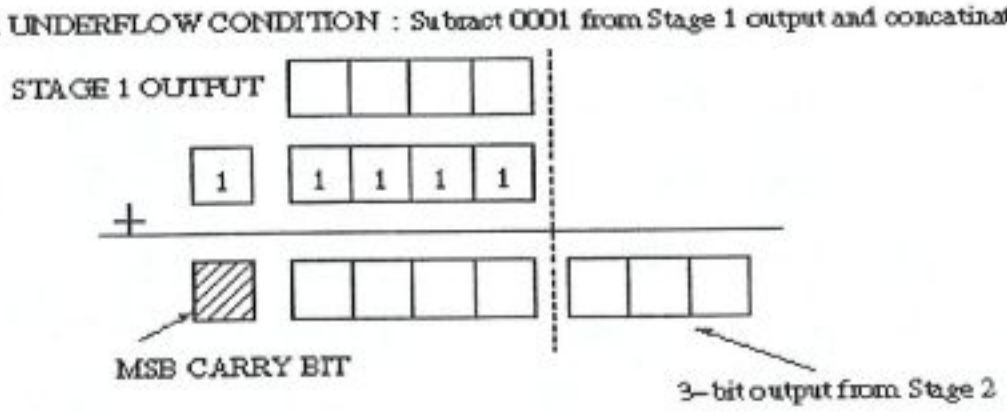


Figure 6.23 *Bit-overlapping* technique that is used in the design of the pipeline stages.

Decimal representation of the thermometer code	Binary code produced in STAGE 1 Encoder	Binary code produced in STAGES 2, 3 and 4 Encoders
15	1111	***011***
14	1110	***010***
13	1101	***001***
12	1100	***000***
11	1011	111
10	1010	110
9	1001	101
8	1000	100
7	0111	011
6	0110	010
5	0101	001
4	0100	000
3	0011	***111***
2	0010	***110***
1	0001	***101***
0	0000	***100***

Table 6.1 Encoding strategy of the related pipeline stage.

Note that over / under flow flags are not given in Table 6.1. They simply correspond to the 4^{th} and the 12^{th} comparator outputs. Also note that 3-bit codes are highlighted for pipeline stages 2, 3 and 4 in over / under flow states.

Design and verification of a full 4bit analog pipeline stage is completed by combining all the building blocks together. In order to achieve 4-stage pipelining we now have to design the digital pipeline's building blocks, such as data flip-flops, full adders, OR and XOR gates and buffers. Design and verification of these digital blocks will be examined in detail in Chapter 7.

7. DESIGN OF DIGITAL BUILDING BLOCKS

Following the design of the analog pipeline components, we now turn our attention to the digital building blocks that are needed to establish full pipeline operation. More specifically, we will have to design the 11-bit adder to construct the output word, the 4-bit thermometer-to-binary encoder that is constructed by XOR gates, buffers, and finally data flip-flops to establish pipelining at the rising edge of the sampling clock. Design and verification of these digital pipeline stage elements will be examined in this chapter.

7.1 Full Adder Design

Addition forms the basis for many important binary operations from counting to multiplication to filtering. As a result, adder circuits that add two binary numbers are of great interest to digital system designs. A wide variety of adder implementations are available to serve different speed/density requirements. Considering the Boolean description of the binary adder circuit, let A and B the two binary input variables (addend bits), and let C the represent the carry_in bit. The binary full adder is a three-input, two-output combinational circuit that satisfies the truth table given in Table 7.1.

A	B	C	sum_out	carry_out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 7.1 Truth table for the full adder circuit.

A and B are the adder inputs, C is the carry input, sum_out is the sum output, and carry_out is the carry output.

7.1.1 Single-bit adders

Probably the simplest approach to design an adder is to implement gates to yield the required majority logic functions. The sum_out and the carry_out signals can be found as the following two combinational Boolean functions of the three input variables, A, B and C. From the truth table these are:

$$\begin{aligned} sum\_out &= A \oplus B \oplus C \\ &= ABC + A\overline{BC} + \overline{AB}C + \overline{AC}B \end{aligned} \tag{7.1}$$

$$carry\_out = AB + AC + BC$$

which may be factored as follows:

$$sum\_out = C\left(AB + \overline{AB}\right) + \overline{C}\left(A\overline{B} + \overline{A}B\right) \tag{7.2}$$

$$carry\_out = AB + C(A + B)$$

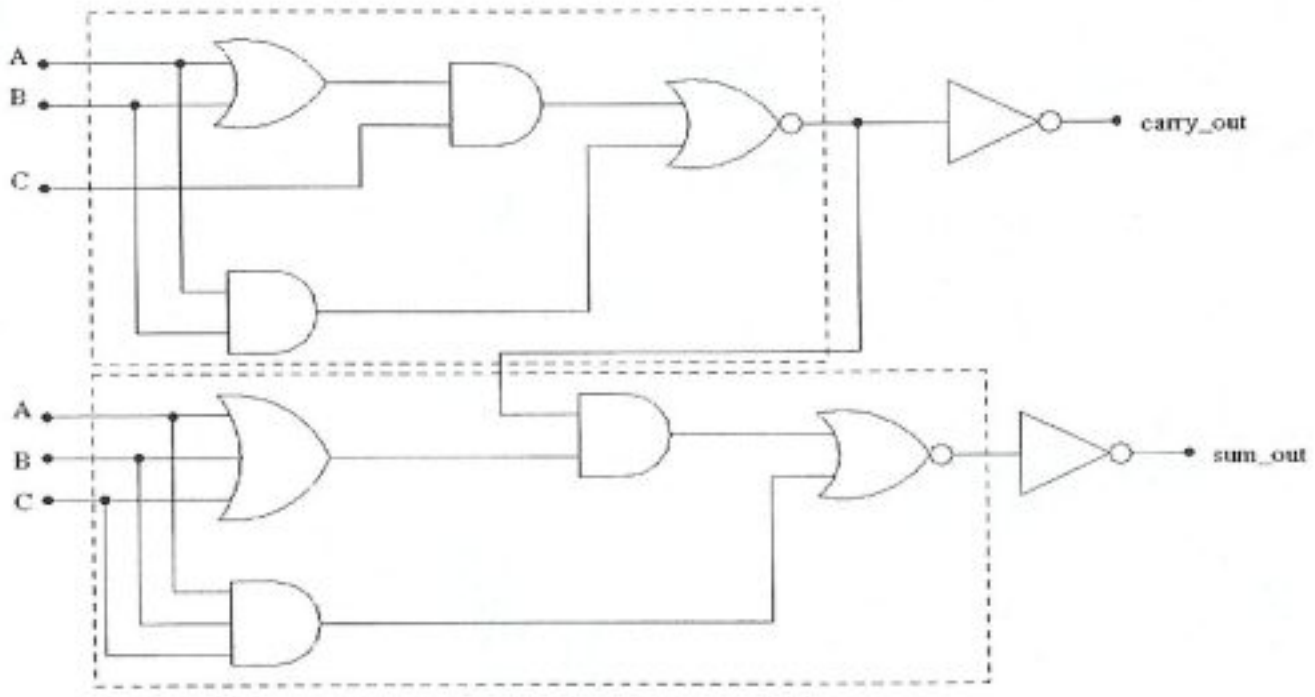


Figure 7.1 Gate-level schematic of the one-bit full-adder circuit [10].

The direct gate level realization of these two functions of Eq. 7.2 is shown in Figure 7.1. Note that instead of realizing the two functions independently, we use the carry_out signal to generate the sum output with an implementation that does not use XOR gates is shown in Figure 7.2. This uses an alternative implementation that is achieved by realising that the carry_out term reused in the sum_out term as a common subexpression. In this implementation, shown in Figure 7.2, sum_out can be expressed as

$$\begin{aligned} sum\_out &= ABC + (A+B+C)\overline{carry\_out} \\ &= ABC + (A+B+C)\overline{(AB + C(A+B))} \end{aligned} \tag{7.3}$$

Note that the circuit implementation shown in Fig. 7.2 also makes use of the fact that both functions are symmetric Boolean functions, resulting in identical nMOS and pMOS network topologies.

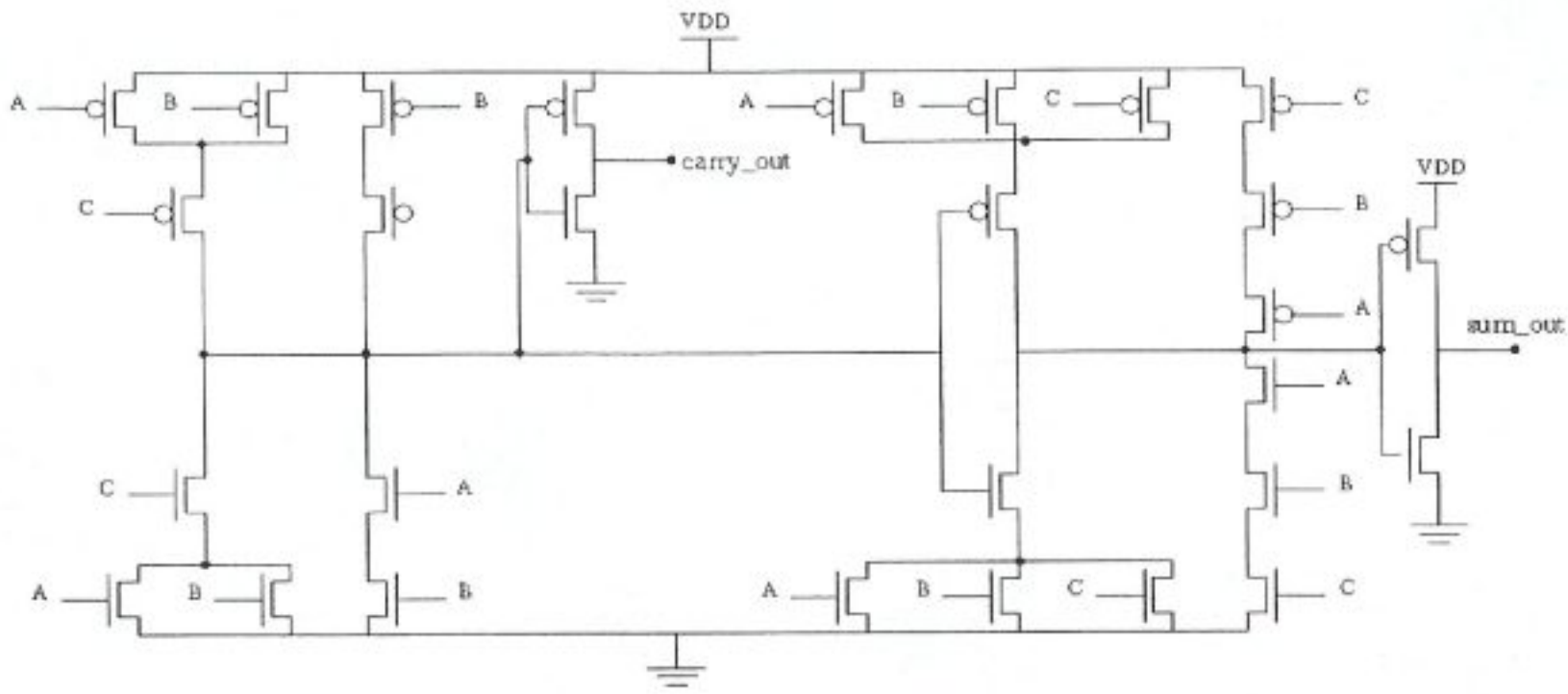


Figure 7.2 Completely symmetric 1-bit full adder cell [10].

The designed full adder circuit is now simulated in order to determine its dynamic performance. Assuming that the outputs of this adder circuit may drive a similar circuit, both output nodes are loaded with capacitors, which represent the typical input capacitance of a full adder. The three input waveforms (A, B and C) are chosen so that all of the eigth possible input combinations are applied consequtively to the full adder circuit. Figure 7.3 shows the simulated input and output waveforms of the full adder circuit.

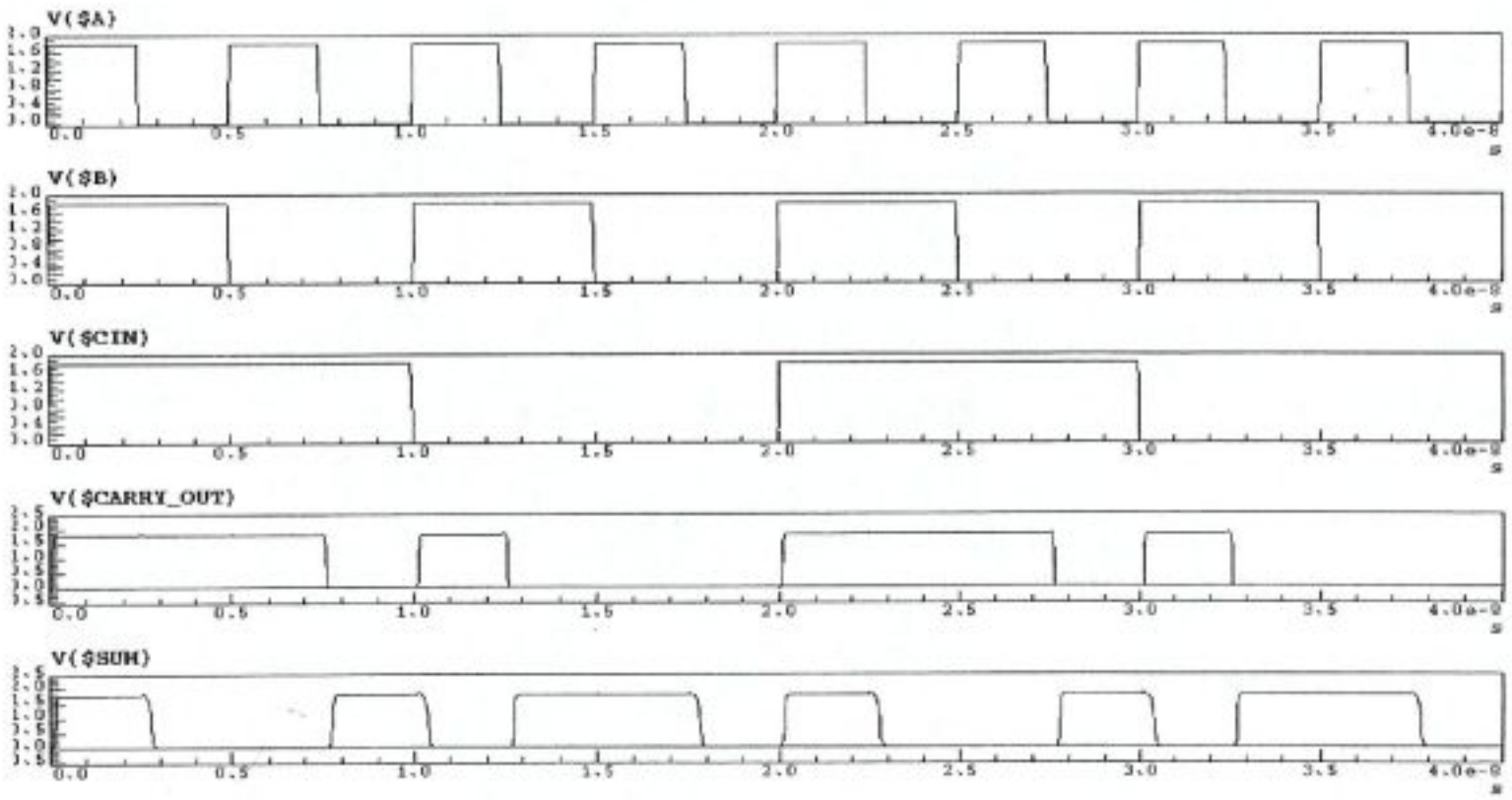


Figure 7.3 Simulated input and output waveforms of the 1-bit full adder circuit.

7.1.2 Bit-parallel adder

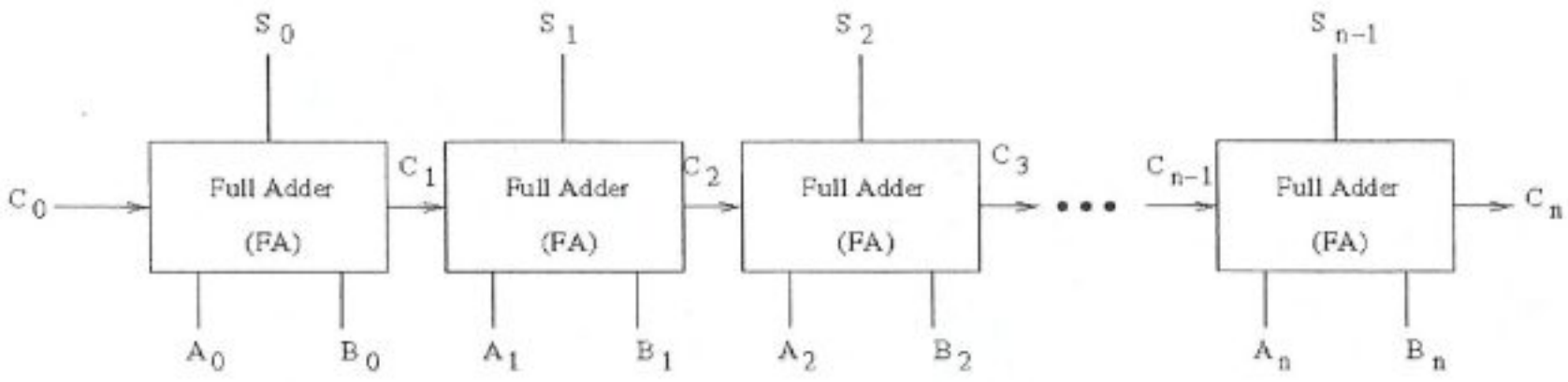


Figure 7.4 Block diagram of a carry ripple adder chain consisting of n 1-bit full adders.

An n-bit adder may be constructed by cascading n 1-bit adders, as shown in Figure 7.4. This implementation is called a Ripple Carry adder. The inputs are n-bit A and B values. The carry_out signal of stage *i* is fed to the C signal of satge *i* + 1 and the sum_out signal forms the n-bit output. The nth bit of the sum_out indicates the sign of the result, while the nth carry_out signal indicates whether an overflow condition has occurred. Because the carry-output signal (caryy_out) is used in the generation of sum_out in the circuit shown in Figure 7.4. sum_out will be delayed with respect to carry_out. In the case of n-bit parallel adder, the carry delay has to be minimized, because the delay associated with the adder is $T_n = nT_C$, where T_n is the total add time, n is the number of stages, and T_C is the delay of one carry stage.

We designed a 10-bit ripple carry adder chain described as in Figure 7.4, and simulated the dynamic performance of the chain at 200 MHz. Related simulation results of 10-bit full adder chain are given in Table 7.2 and Table 7.3. Rise and fall time characteristics of $carry\_out_i$ signal are given with the propagation delay of both rising/falling edge of the same signal due to the in coming carry signal in Table 7.2. Also rise and fall time characteristics of sum_out_i signal are given with the propogation delay of both rising/falling edge of the same signal due to the incoming carry signal in Table 7.3. All results given in these tables are in ps units.

carry_out$_i$	*Rise Time (ps)*	*Fall Time (ps)*	*Rising edge PD (ps)*	*Falling edge PD (ps)*
1	152	117.69	178	175
2	152.93	117.53	372	361
3	152.93	117.52	566	547
4	152.93	117.52	763	733
5	152.93	117.51	957	920
6	152.93	117.52	1150	1110
7	152.93	117.51	1350	1290
8	152.93	117.51	1540	1480
9	152.91	117.51	1740	1660
10	152.91	117.52	1880	1810

Table 7.2 Simulated carry_out dynamic performance results.

sum_out$_i$	*Rise Time (ps)*	*Fall Time (ps)*	*Rising edge PD (ps)*	*Falling edge PD (ps)*
1	109.57	217.63	343.68	419.07
2	109.58	217.68	530.18	613.76
3	109.57	217.68	716.63	808.45
4	109.58	217.69	903.09	1003
5	109.57	217.69	1089	1197
6	109.57	217.7	1275	1392
7	109.57	217.71	1462	1587
8	109.57	217.71	1648	1787
9	109.57	217.72	1835	1976
10	109.1	217.41	2023	2173

Table 7.3 Simulated sum_out dynamic performance results.

Note that, sum_out is delayed with respect to carry_out signal and what is more carry_out delay increases with increasing the number of bits to be added. Hence, these simulated results states that the dynamic performance of the designed 10-bit ripple carry

adder is suitable for applications at 200 MHz signal frequency. Layout of 1-bit full adder circuit is given in Figure 7.5. The silicon area is approximately 107 μm^2.

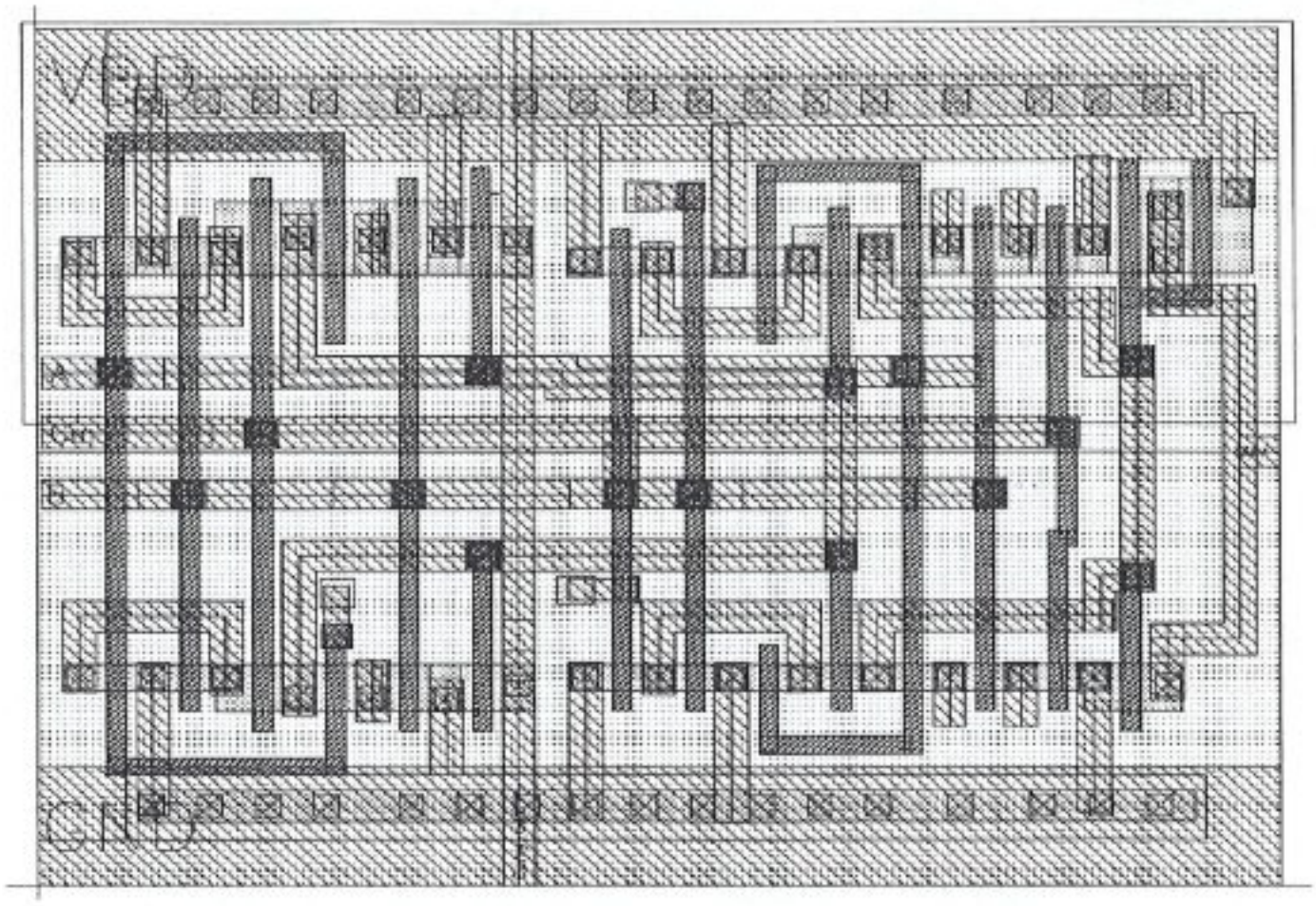


Figure 7.5 Layout view of the designed 1-bit full adder circuit.

7.2 D-type Flip-Flop (DFF) Design

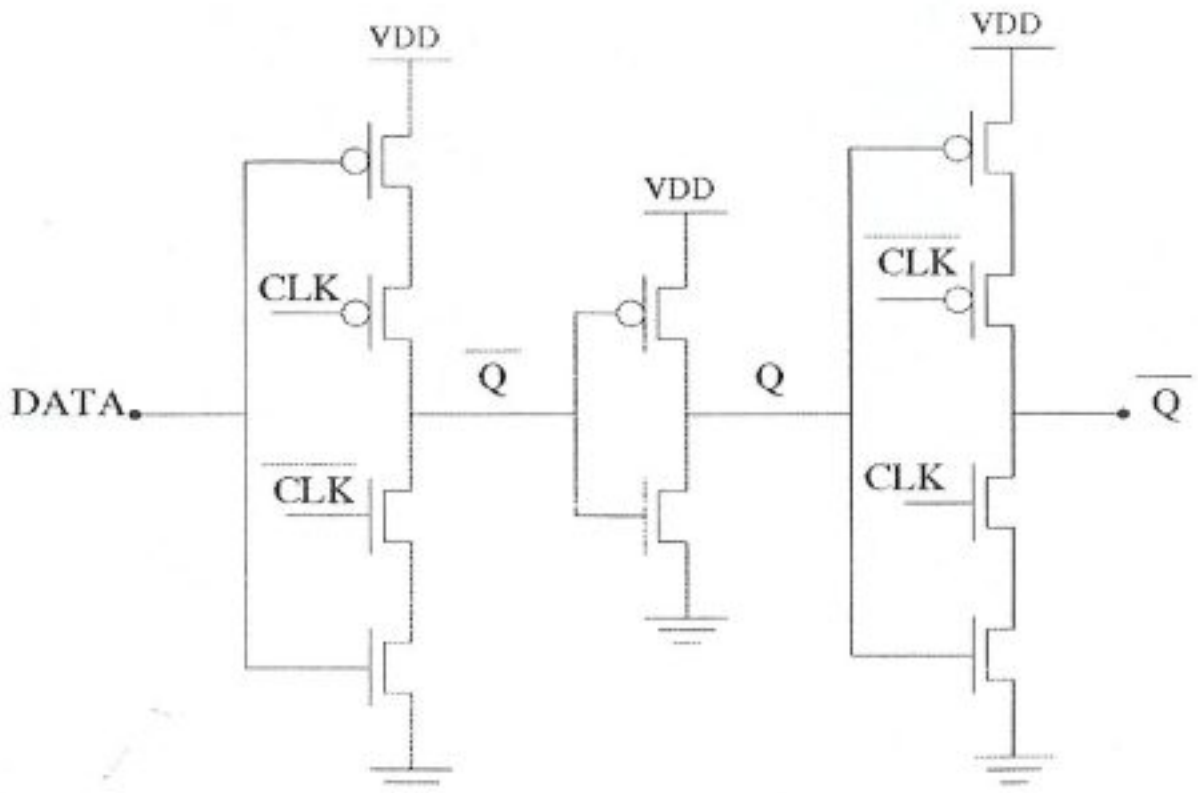


Figure 7.6 CMOS implementation of the D-latch circuit [10].

Figure 7.6 shows the CMOS implementation of D-latch. The circuit contains two tristate inverters, driven by the clock and its inverse. The first tristate inverter acts as the input switch, accepting the input signal when the clock is low. At this time, the second tristate inverter is at its high-impedance state, and the ouput Q is following the input signal. When the clock goes high, the input buffer becomes inactive, and the second tristate inverter completes the two-inverter loop, which preserves its state until the next clock pulse.

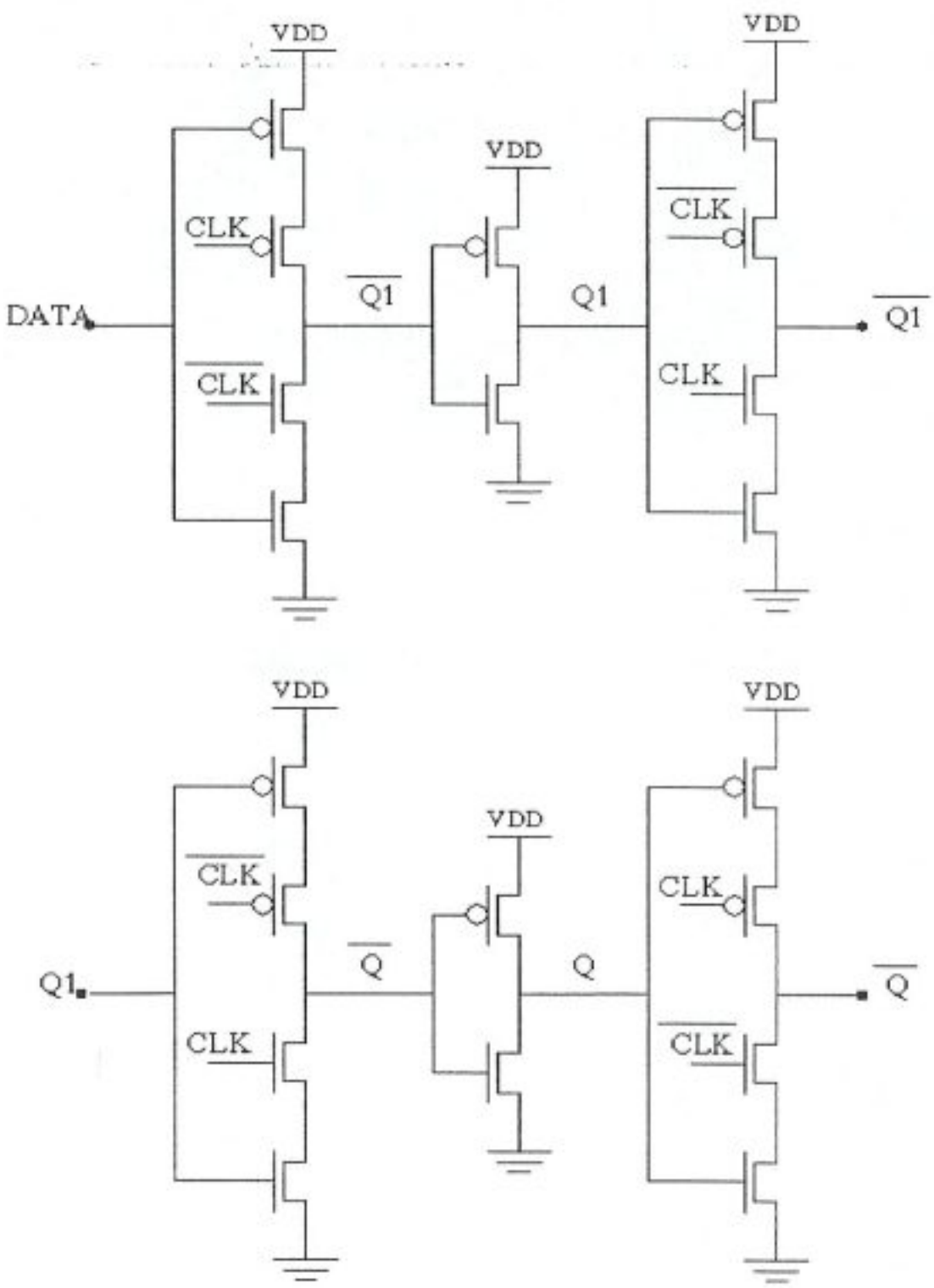


Figure 7.7 CMOS rising edge-triggered master-slave D flip-flop (DFF) [10].

Now, consider the two-stage master-slave flip-flop shown in Figure 7.7, which is constructed by simply cascading two D-latch circuits given in Figure 7.6. The first stage (master) is driven by the inverse of the clock signal, while the second (slave) is driven by the clock signal its self. Thus, the master stage is negative level-sensitive, while the slave stage is positive level-sensitive.

When the clock signal is low, the master stage flows the DATA input while the slave stage holds the previous state. When the clock changes from logic "0" to "1", the master latch ceases to sample the input and stores the DATA value at the time of the clock transition. At the same time, the slave latch becomes transparent, passing the stored master value Q_1 to the output of the slave stage, Q. The input cannot affect the output because the master stage is disconnected from the DATA input. When the clock changes again from "1" to "0", the slave latch locks in the master latch output and the master stage starts sampling the input again. Thus, this circuit is a positive edge-triggered D flip-flop by virtue of the fact that it samples the input at the rising edge of the clock pulse. Finally we added reset signal to the DFF circuit given in Figure 7.7 by simply adding two extra nMOS transistors to the master stage outputs in such a way that Q1 output will be "0" when RESET signal is HIGH. Figure 7.8 shows the simulated input and output waveforms of the two-stage master-slave D flip-flop designed with reset.

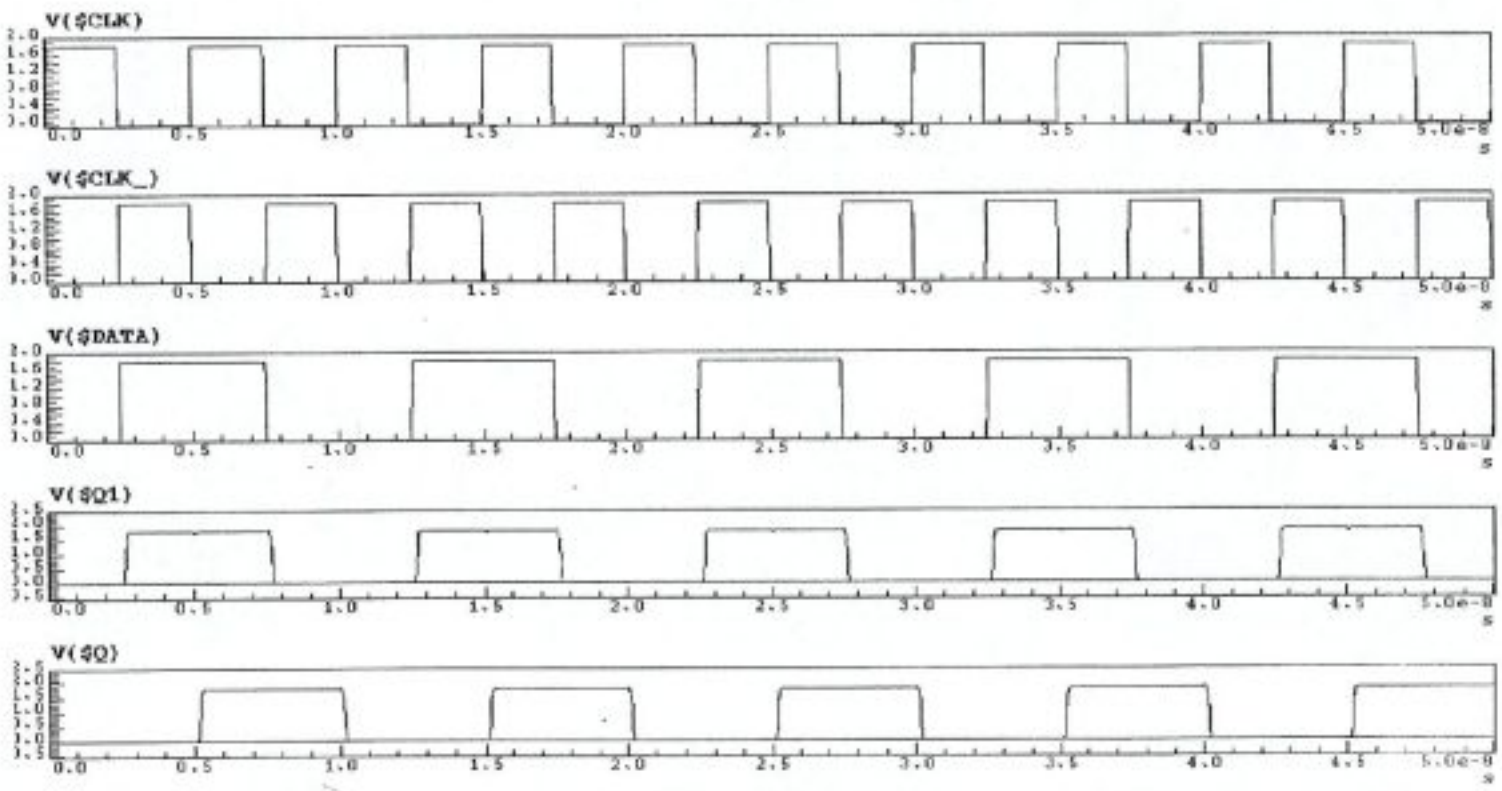


Figure 7.8 Simulated input and output waveforms of the CMOS DFF circuit given in Figure 7.7.

The dynamic performance of the designed two-stage master-slave DFF with reset is characterised in three different conditions. Set-up and hold times, most critical attributes of D-type flip-flops, are simulated at 200 mHZ clock frequency while the delay between clock and its inverse is 50 ps, 100 ps and 150 ps. The outputs of this DFF circuit are loaded with the same circuit itself. Typical corner simulation results obtained are given in Table 7.4 in ps time unit. Layout view of designed DFF is given is Figure 7.9.

Inversion delay (ps)	***Set-up (ps)***	***Rising edge Propagation Delay (ps)***	***Falling edge Propagation Delay (ps)***
50	182.5	172.62 ps	141.89 ps
100	239	177.58 ps	92.179 ps
150	294.5	180.28 ps	42.8 ps

Table 7.4 Simulated dynamic characteristics of two-stage master-slave DFF circuit.

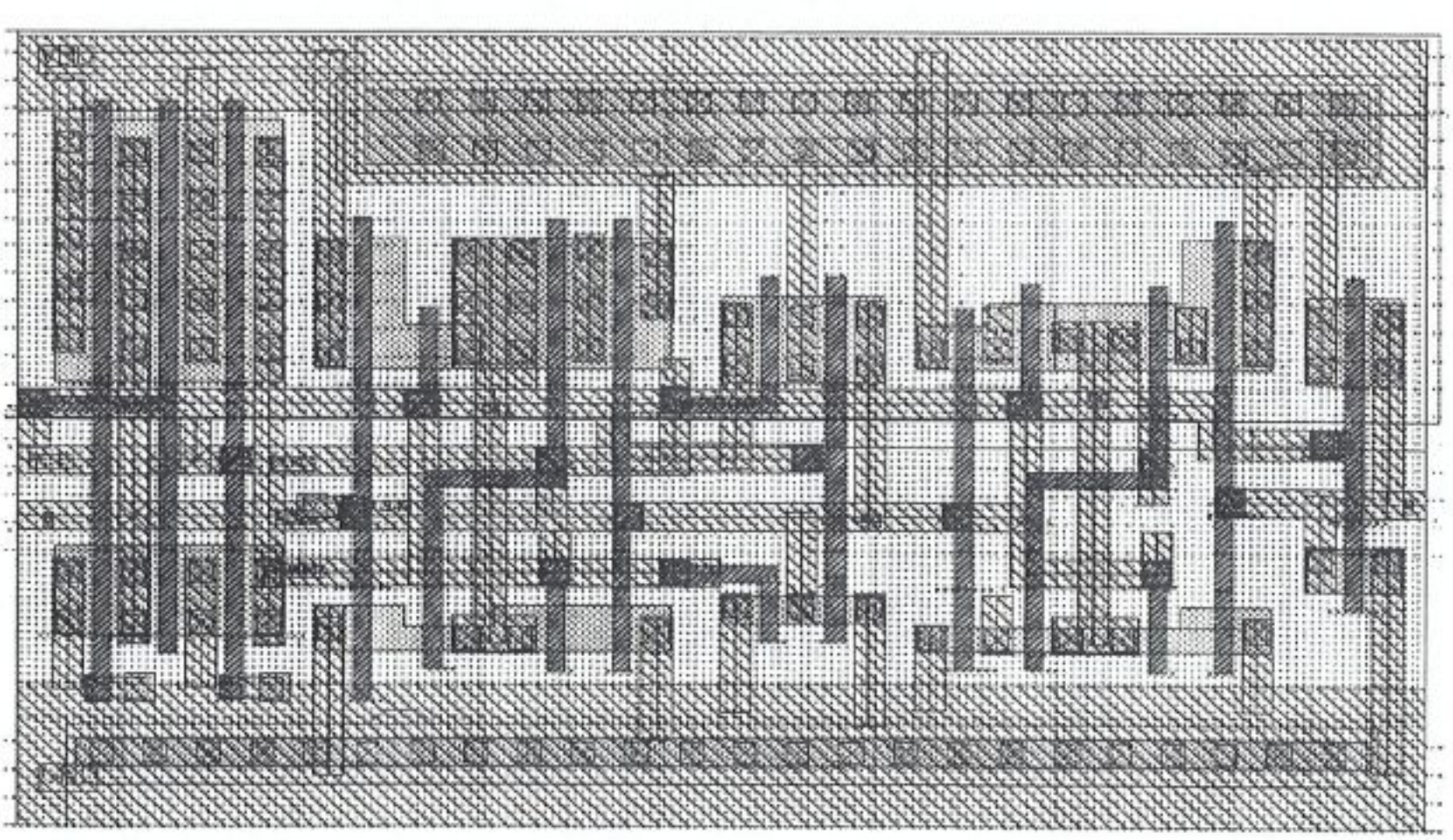


Figure 7.9 Layout view of the designed D-type flip-flop. Area is aproximately 132 μm^2.

7.3 Exclusive OR Gate Design

The truth table of exclusive OR (XOR) function is given in Table 7.5. The Boolean expression obtained from this truth table is given in Eq. 7.5 and gate level, full CMOS implementation of Eq. 7.5 is given in Figure 7.10 and Figure 7.11 respectively. Note that two extra inverters are needed in Figure 7.11.

A	B	Z
0	0	0
1	0	1
0	1	1
1	1	0

Table 7.5 Truth table of exclusive OR function.

$$\begin{aligned} Z &= A \oplus B \\ &= \overline{A}B + A\overline{B} \end{aligned} \tag{7.5}$$

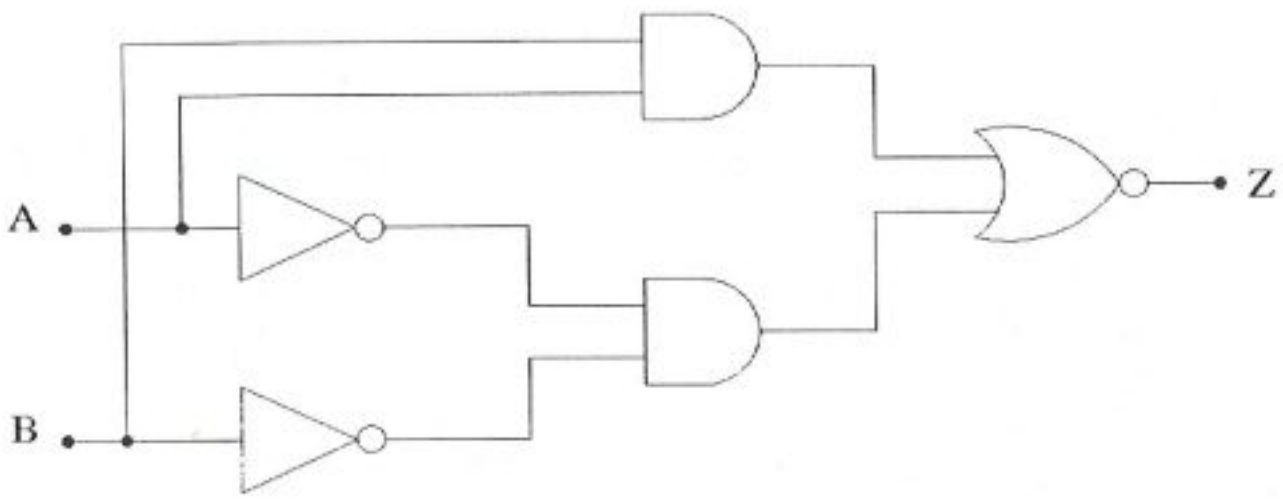


Figure 7.10 Gate level representation of XOR function [8].

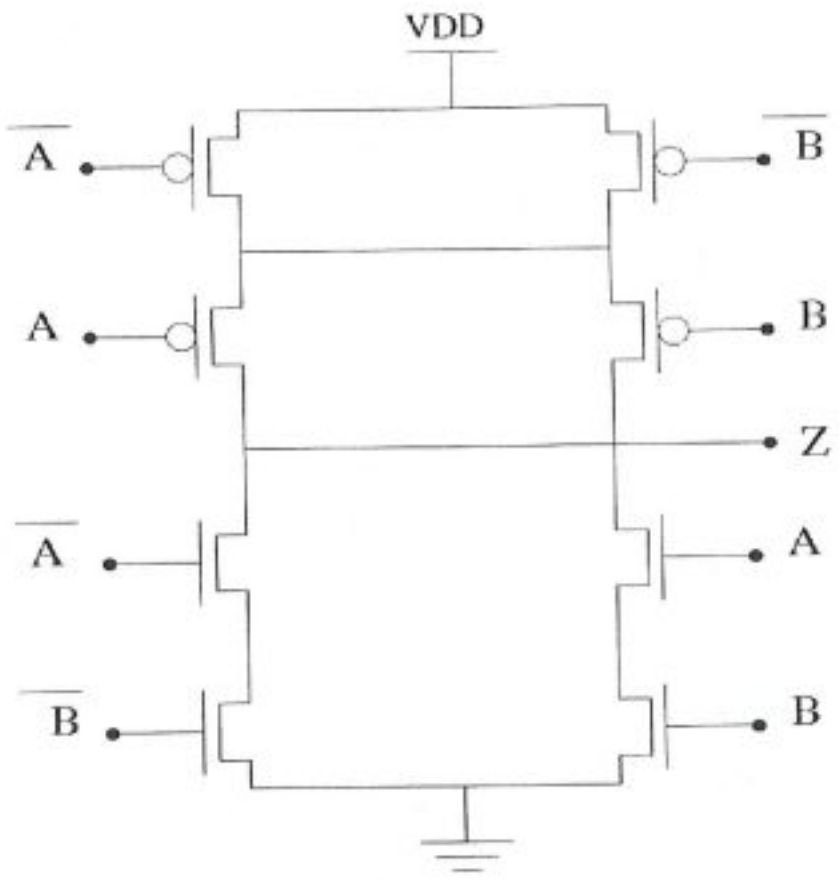


Figure 7.11 Full CMOS implementation of XOR function [8].

Finally, the designed XOR circuit is simulated in order to verify its dynamic performance while loaded with 5 fF capacitance, which is equivalent to the input capacitance of minimum sized buffer. Typical simulation corner results are given is Table 7.6 and layout view of XOR circuit is available in Figure 7.12. Simulated input and output waveforms at 200 MHz signal frequency are given in Figure 7.13.

Rising edge Propagation Delay	51.67 ps
Falling edge Propagation Delay	46.64 ps
Rise Time	137.88 ps
Fall Time	81.48 ps

Table 7.6 Simulated dynamic performance characteristics of XOR circuit.

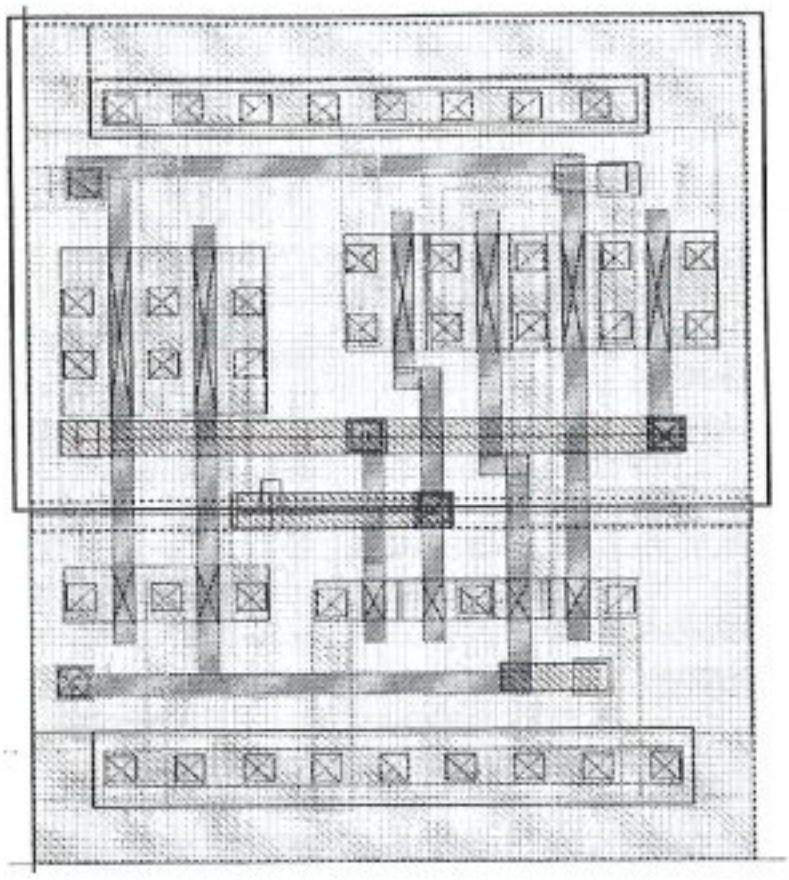


Figure 7.12 Layout view of the designed XOR gate. Area is aproximately 45 μm^2.

Simulated results of the designed 4-bit encoder circuit using XOR gates and buffers (Figure 7.14) are as follows:

- Propagation delay : 443.41 ps
- Rise time : 72.37 ps
- Fall Time 68.94 ps

Note that, these simulation results are for typical simulation corner.

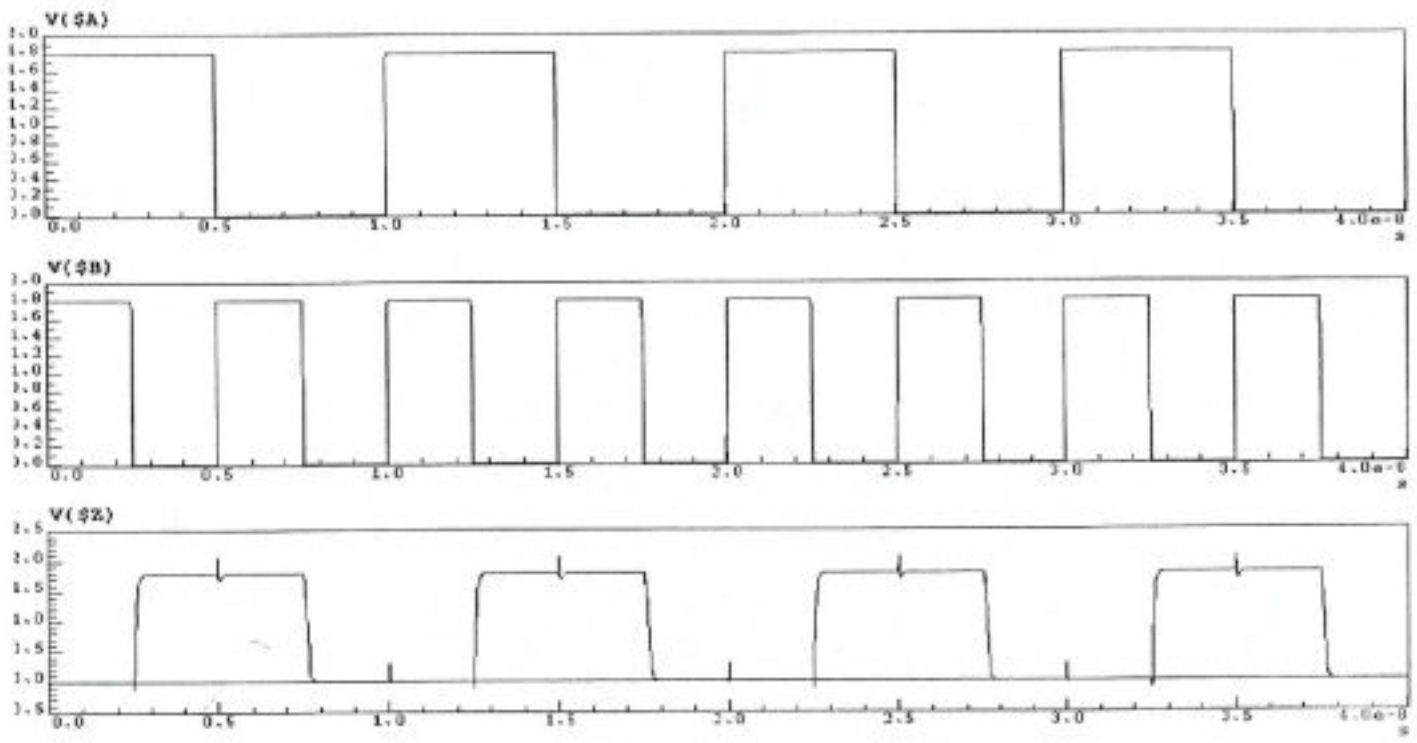


Figure 7.13 Simulated input and output waveforms of the designed XOR circuit.

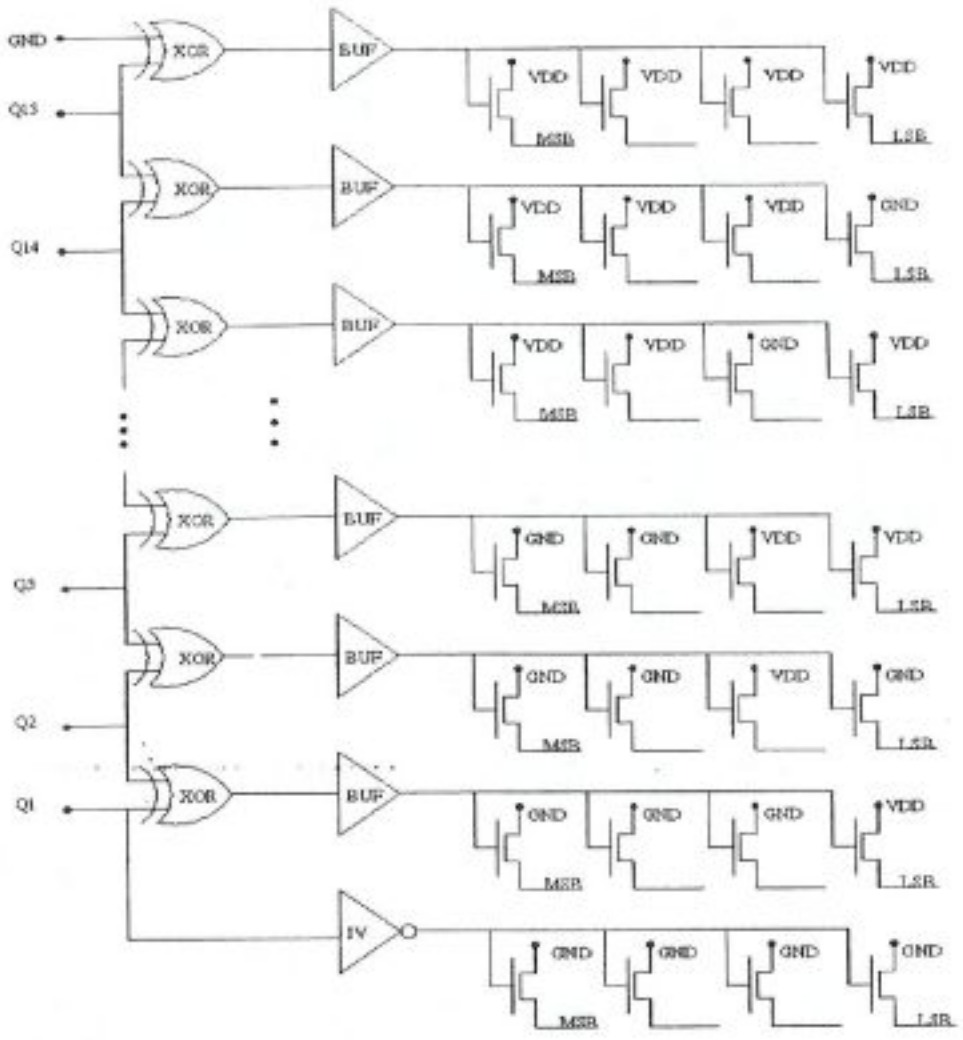


Figure 7.14 Simplified schematic view of a 4-bit encoder block.

Note that, other digital blocks designed for this dissertation, such as OR2 gate, buffers and inverters are not explained in detail because of the simplicity of the structures. Design criteria for these cells were speed and almost symmetrical rise and fall times.

8 . TOP-LEVEL CONSTRUCTION OF THE PIPELINED ADC

The previous chapters have presented the design of all sub-blocks that are used in the pipelined ADC structure, as well as the complete design of the 4-bit analog pipeline stage and the digital pipeline stage elements. The operation and the performance characteristics of these essential components were also verified with extensive simulations. It was demonstrated that the electrical performance of the sub-blocks are well within the expected bounds so that the operation of the overall ADC architecture can be guaranteed to match the initial specifications. At this point, the final task is to combine the designed components into the final 12-bit pipelined ADC structure, using four cascaded pipeline stages.

8.1. Overall Structure of the Pipeline

A simplified view of the overall ADC architecture is shown in Fig. 8.1, where each analog pipeline component and the corresponding digital outputs are highlighted for better description. It can be seen that the structure consist of four 4-bit flash ADCs, three 4-bit multiplying DACs (MDACs) including their respective residue amplifiers, four thermometer-to-binary code encoders, three adder chains to construct the corrected output word at the end of each conversion step, and the DFFs to facilitate the pipeline.

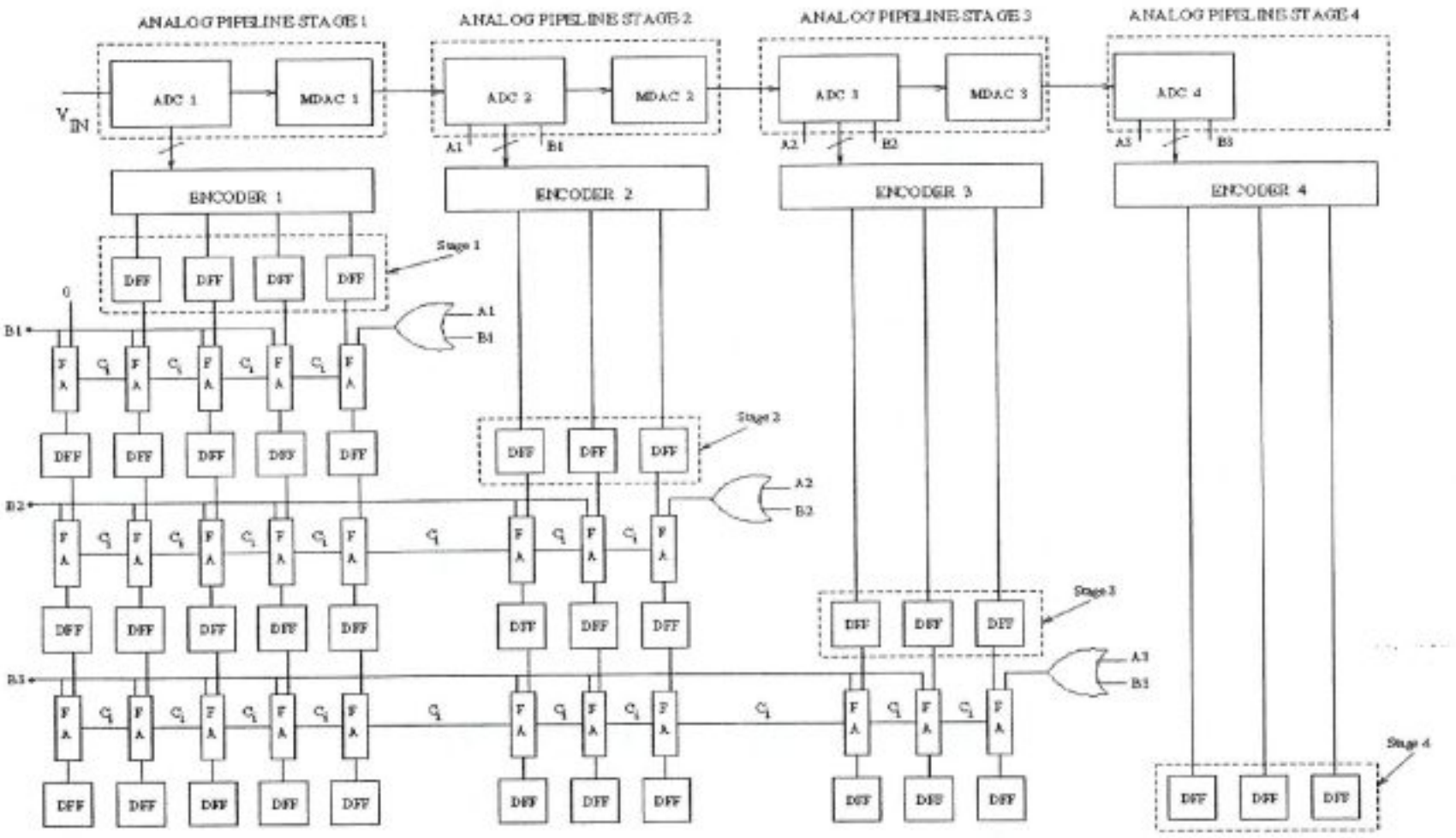


Figure 8.1 Block level representation of four-stage pipelined A/D converter.

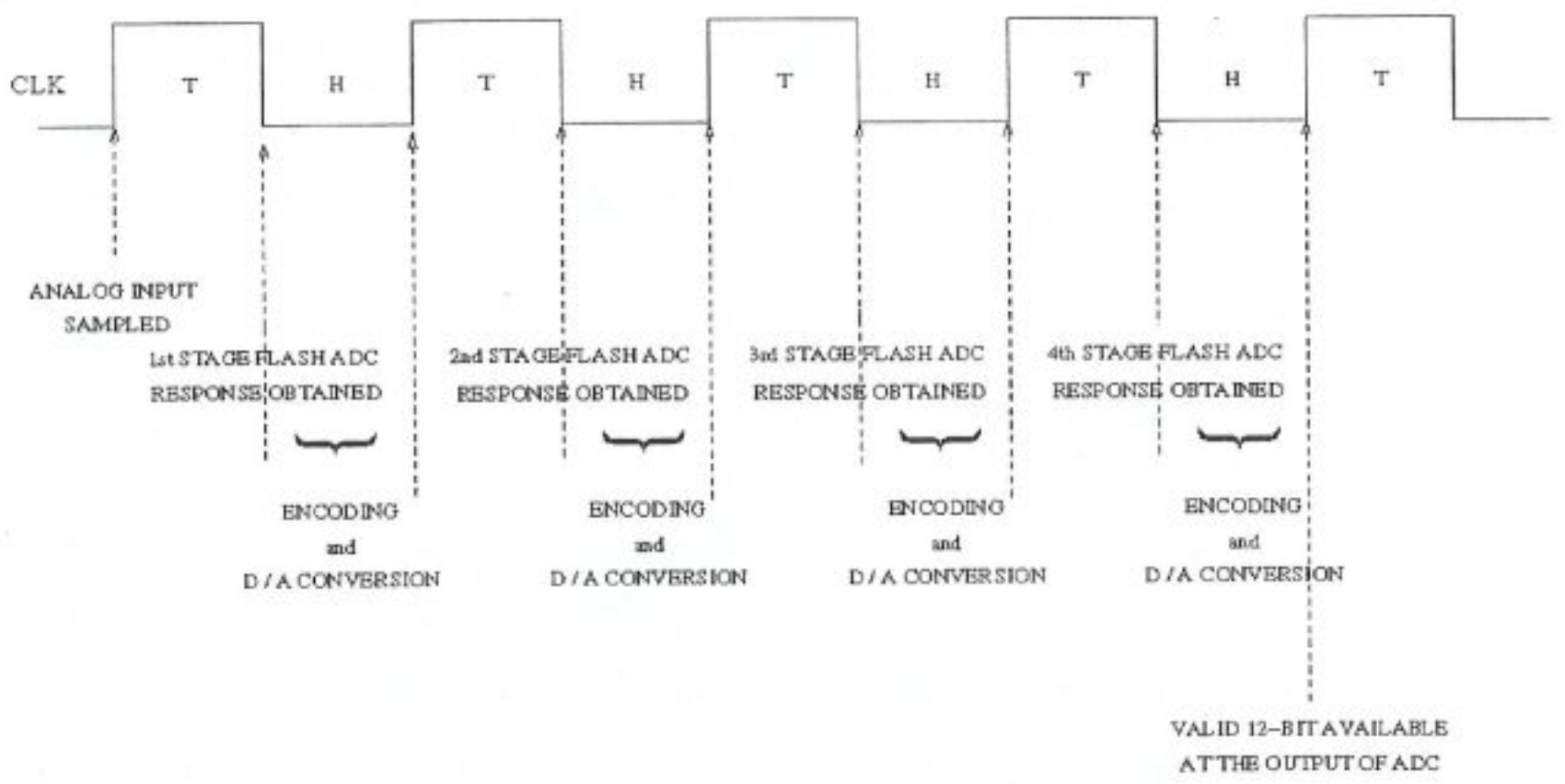


Figure 8.2 Four-stage pipelined ADC clocking scheme.

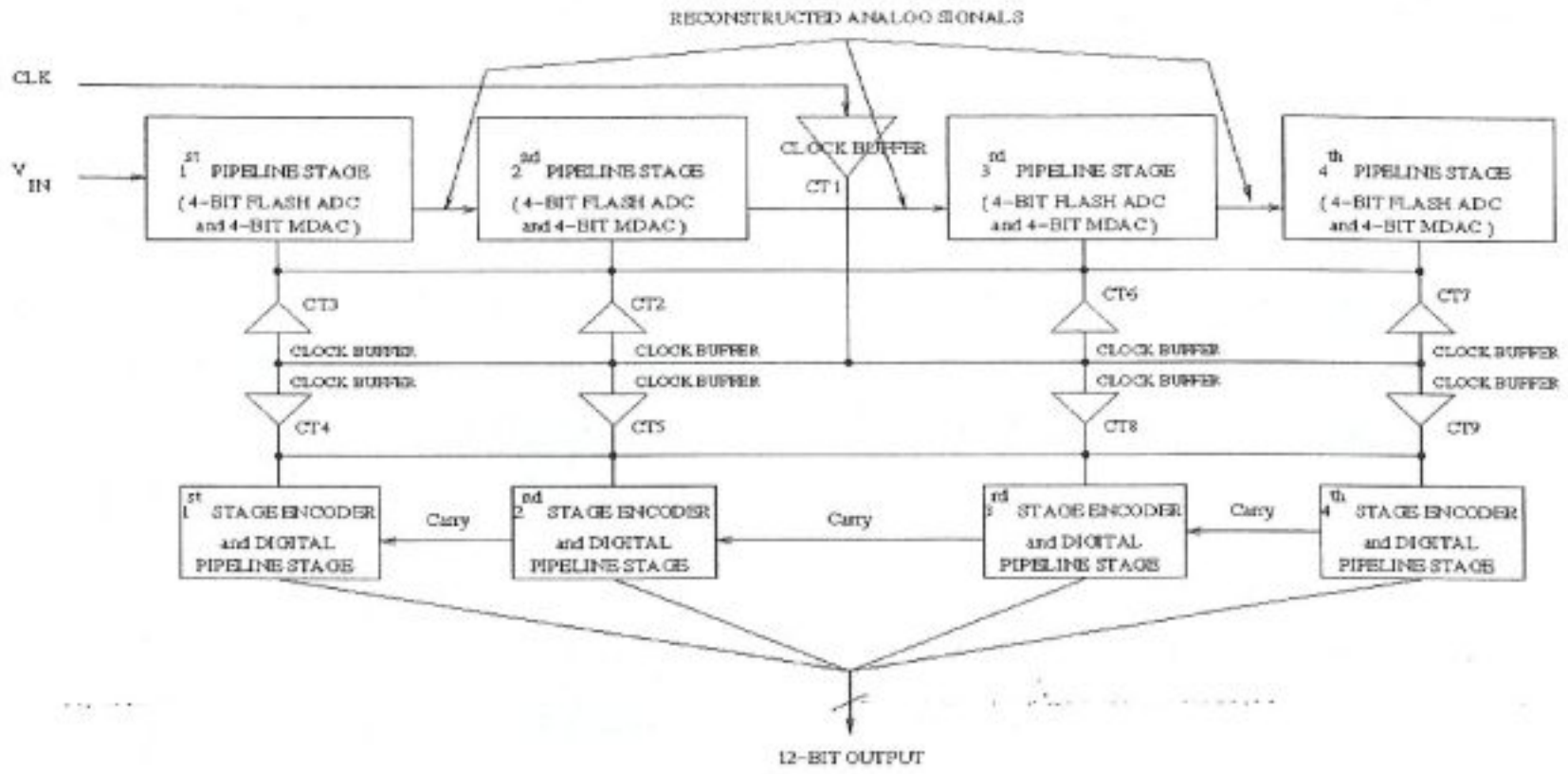


Figure 8.3 Block level representation of the proposed clock distribution between functional modules of the pipelined ADC architecture.

According to the pipelined operation principle of this four-stage structure, each four-bit stage is capable of processing subsequent portions of four different sampled input signals at any given clock cycle. The processed results are passed on to the following pipeline stage in the next clock cycle, so that the final stage produces a complete 12-bit result (13 bits with overflow) at the end of each clock period. The latency of this pipeline structure is four clock cycles; i.e. the complete conversion of any sampled signal is obtained at the end of the fourth clock period following the sampling edge. Assuming that the clock frequency is set to 200 MHz (as proven to be feasible by previous simulation results) the proposed pipelined architecture is thus capable of generating a 12-bit analog-to-digital conversion every 5 ns.

8.2. Timing Considerations

The simplified clocking scheme of the pipeline architecture is shown in Fig. 8.2. Track and hold phases of the clock are indicated as "T" and "H" respectively. The tracked input analog signal is sampled with the falling edge of the clock and the corresponding 4-bit thermometric code is ready at the output of the 1st pipeline stage's output with a small time delay. In other words, the output of 1st stage's flash ADC is

ready at the falling edge of first clock cycle. The encoding process starts right after the thermometric code is generated, during the following half period in the related encoder circuit. Meanwhile, the second stage's input analog signal is constructed by the multiplying DAC. With the rising edge of the CLK, decoded 1st stage's 4-bit code (MSB) by the 1st stage encoder is sampled via the DFFs and held constant until the next rising edge of the sampling clock. Subsequently, the tracking phase of 2nd pipeline stage is entered. Thus, the second stage's flash ADC receives the reconstructed analog signal at the output of the 1st stage's MDAC during the next half period. At the end of this half period (with the falling edge of the clock) the thermometric code representing the reconstructed analog input signal via the 1st stage MDAC is formed at the output of the second stage's flash ADC. Right after the production of the thermometric code by second stage flash A/D converter, the thermometric to binary code encoding starts. At the same time the analog-to-digital conversion process takes place at the second stage MDAC. Meanwhile, a new analog input signal is being processed in the 1st stage, which is the basis of pipeline operation. The 2nd stage DFFs sample the summation of encoded 1st stage encoder output and the over/under flow bit of the 2nd stage with the rising edge of the third clock cycle. Similarly, the third stage flash A/D converter receives the reconstructed analog signal by the second stage MDAC and 15-bit thermometric code representing this analog signal is ready at the falling edge of 3rd clock cycle. This 15-bit thermometric code is encoded into a 4-bit binary code in the 3rd stage encoder and also processed in the 3rd stage MDAC. Summation of the encoded 4-bit binary code and the 2nd stage's DFF outputs are sampled via the 3rd stage DFFs, held constant until the next comming rising edge of the clock. Consequently, 4th (last) pipeline stage's flash A/D converter operates on the finaly reconstructed analog signal. With the falling edge of the 4th clock cycle the thermometric code is formed at the output of the 4th stage's flash ADC. Similarly the 4-bit binary code (LSB) is encoded in the 4th stage encoder during the proceeding half period. Note that no digital-to-analog conversion process takes place in the last stage. Thus, with the rising edge of the fifth clock pulse the valid 12-bit digital word that represents the held analog input signal four clock cycles before is formed at the outpout of pipelined A/D converter. Thus the latency of the designed analog-to-digital converter is four clock cycles (20 ns).

Note that the entire analog and digital pipeline structure is designed to operate with only one clock signal (and its inverse), which is a very significant advantage of the proposed ADC architecture. As opposed to relying on several clock signals hat need to

be generated and distributed with high precision, the sufficiency of a single clock is one of the key factors that make this architecture a very good candidate for modular expansion and simple technology migration. Still, it is highly important to distribute this single clock signal throughout the chip without any clock skew so that the corresponding pipeline stages can operate correctly. Thus, the overall floor planning, layout and clock/signal distribution throughout the system will be important issues that need to be addressed.

8.3. General Floor-planning and Layout Considerations

The totally symmetric appearance of the pipeline ADC makes it easy to repeat the modular building blocks. Hence, as soon as the layout of one pipeline stage is completed, four stage pipeline A/D converter can be constructed very easly and quickly, just by repeating the modules one after another and connecting them in a suitable way.

As already mentioned before, the designed 4-stage 12-bit pipelined A/D converter operates with only one clock and it's inverse. It is essential to distribute this single clock without any skew throughout the pipeline stages in order to be able to process all the stages accordingly. Thus, we will use clock-tree buffers that are placed symmetrically throughout the chip to distribute the system clock to all stages without any skew. We decided to use five clock-tree buffers placed as follows: The system clock is being fed from outside of the chip with a high drive capable clock-tree buffer (CTBUFFX32, numbered as CT1 in Figure 8.3) exactly at the middle of the four pipeline stages, as shown in Figure 8.3. We had to use metal wires as wide as possible in order to reduce the side effects of narrow metal strips such as, high series resistance that can cause voltage drops or fringe capacitors that cause cross-coupling. Thus we decided to route the clock lines throughout the chip using 5 μm wide metal-5 tracks. We chose metal-5 level because of its relatively low parasitic capacitance to substrate that results in considerably low coupling. The disadvantage of this decision is the series resistance of the needed stack "vias" in order to electrically connect the transistors to the clock signal routed on metal-5 tracks. Thus, we used "n×n" via sets all over the chip, where the minimum number of "n" is at least two, which will in return reduce the series resistance, as well as increase the quality of the electrically connectivity. The output of this high drive capable clock-tree buffer (CT1) drives eight clock-tree buffers such as

CTBUFFX16, which have less drive capability than CT1. Each of these second level clock-tree buffers, placed totally symmetrical with respect to the center of the chip drives one of the analog or digital pipeline stages, as shown in Figure 8.3. What is more we *short circuit* the outputs of these second level clock-tree buffers in the hierarchy, in order to be safe from any possible clock skew that could arise because of any unpredictable signal delay. We use local inverter circuits for the inverse of the clock signal, "$(\overline{CLK})$", throughout the chip. We chose this technique because the inverter delays play the dominant role on the efficiency of the sub-blocks rather than the skew. What is more we use a lattice shaped routing for ground (GND), clock (CLK) and supply (VDD) signals on metal levels 4, 5, and 6 respectively as shown in Figure 8.4 throughout the chip. We use 5 μm wide metal tracks for all three level metals and construct a network from this lattice shape as given in Figure 8.5. Thus we use metal-2 or metal-3 (if needed) for lower hierarchy routing between pipeline stages. Note that metal-1 level is used for routing within the sub-block layouts. It is also important to note that we have to reconstruct this latticework over multiplying D/A converter areas because we used all the metal levels in order to construct the unit capacitors and their shielding. Thus, special care must be taken over these areas in the top-level floor planning.

Up to now we finished the design of each sub-block layout, taking special care to make them modular. Also we described the signal routing strategy in detail in the preceding paragraphs. Thus we have to take one more step and design the overall floor plan of the 12-bit A/D converter. An approximate view of the designed floor plan is given in Figure 8.6. As indicated in Figure 8.6 analog and digital pipeline stages are separated from each other in order to prevent analog signal processing from any noise caused by digital signal processing on substrate. That can degrade the overall efficiency of the analog block, hence, the resolution of the overall analog-to-digital converter. In between the analog and digital pipeline stages we placed the clock and

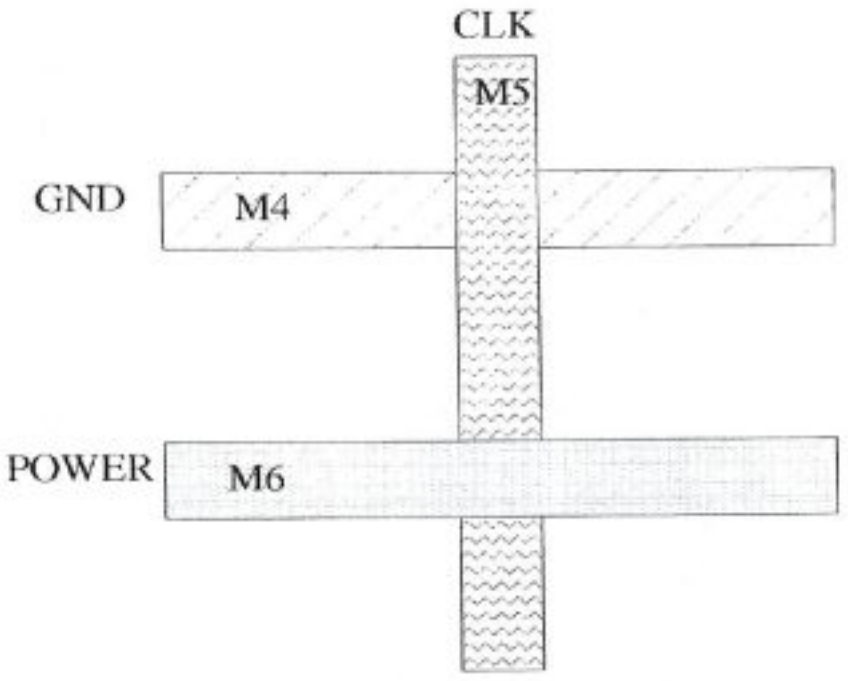


Figure 8.4 Assignment of clock signal / power distribution to different metal layers.

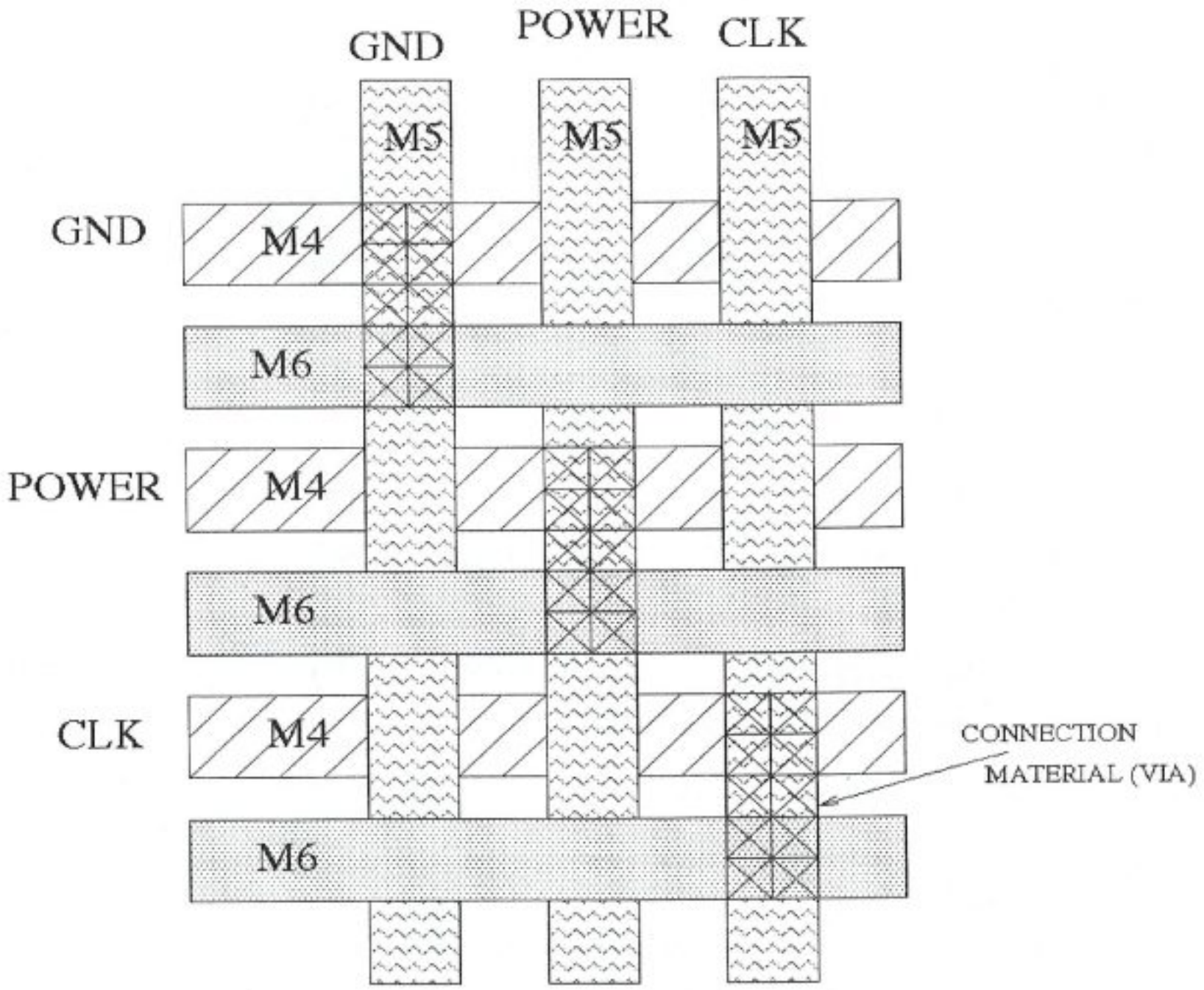


Figure 8.5 Lattice network consisting of clock and power distribution grids.

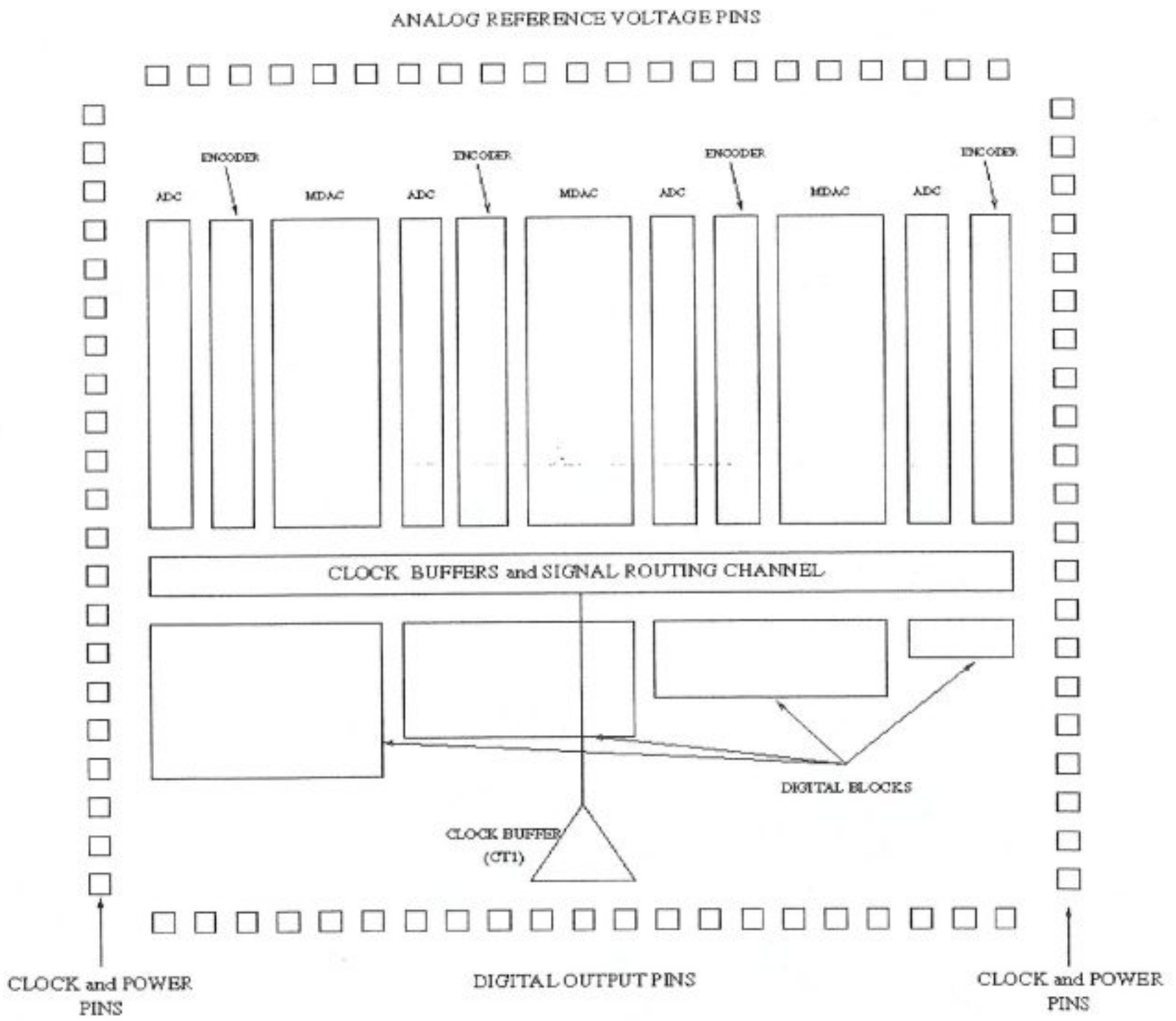


Figure 8.6 Top-level floor plan of the designed 12-bit pipelined A/D converter.

signal routing channels (Figure 8.6). We also separated the analog and digital signal pins as a result of the placement of the pipeline stage's sub-blocks. Figure 8.6 also shows that both the analog and digital pipeline stage blocks are placed in a sequential manner from left to right in order to minimize the routing metal line lengths, thus the capacitive load due to the parasitics on these tracks. Thus, we placed the flash A/D converter, the resistor and comparator chains, at the far left hand side of the sub-block in a vertical line-up. Note that the y-dimension of the flash A/D converter is determined by the y-dimension of the fifteen voltage comparators. Outputs of these comparators drive both the encoder and multiplying DAC inputs. But the output of the MDAC is

processed in the following analog pipeline stage, so that we placed the encoder sub-block next to right hand side of the A/D converter and then the multiplying D/A converter in a horizontal manner. We only repeat this block in order to construct the four pipeline stages. As in the same manner we placed the digital pipeline stages as the analog part. We constructed the digital pipeline stages in the same vertical axis with the related analog pipeline stage (Figure 8.6). Note that size of the digital pipeline stages decreases with the increasing stage number just because of the decreasing digital pipeline depth (four in the first stage and one in the last stage). We designed the digital pipeline stages by vertically repeating two horizontally designed "*rows*" that are formed by D-type flip-flops (DFFs) and full adder circuits (FAs) one after another (Figure 8.1). Consequently the analog signals flow from left to right, while the digital signals flow from top to bottom throughout the chip. Finally we used both the left and right side pins of the package for clock and power signals, which will work in a harmony with the lattice shaped distribution network we designed for these signals.

The overall silicon area that is occupied by these analog and digital pipeline stages is estimated to be about 0.25 mm^2, excluding the I/O pad-ring.

9 . CONCLUSIONS

This thesis has presented the design, verification, system integration and the physical realization of a monolithic high-speed analog-digital converter (ADC) with 12-bit accuracy. The architecture of the ADC has been realized as a pipelined structure consisting of four pipeline stages, each of which is capable of processing the incoming analog signal with 4-bit accuracy. A bit-overlapping technique has been employed for digital error correction between the pipeline stages so that the influence of possible errors that occur during analog signal processing can be minimized. The entire circuit architecture is built with a modular approach, consisting of identical blocks organized into an easily expandable pipeline chain.

To realize the proposed circuit architecture, four basic building blocks were required: (i) high-speed voltage comparators, (ii) very high bandwidth op-amps with low offset, (iii) high-speed multiplying DAC (capacitive MDAC), and (iv) the digital correction circuitry including a 11-bit ripple carry adder. Initially, these key components were designed to meet the desired specifications, and then, the overall physical design of the ADC has been constructed by following a simple modular approach.

The voltage comparator is one of the main components that dictate the resolution of the overall A/D converter as well as the conversion speed of the converter. Several different topologies were studied; all of which were derived from the same basic structure. The full complementary circuit architecture was chosen as the final design, aided with a simple inverter based output stage to further improve the response times. The worst-case input voltage offset of the improved complementary comparator was

found to be less than 10 mV, allowing conversion with 7-bit accuracy at a dynamic input range of 1.6 V_{pp}. The worst-case INL and DNL errors remain within ± 0.1 LSB for this 4-bit application due to the fact that the maximum input offset does not exceed 10 mV. Typical response times obtained for this voltage comparator are less than 450 ps, allowing operation speeds of up to 1 GHz. The circuit occupies a silicon area of about 320 μm^2 and consumes 800 μW at 200 MHz sampling frequency.

Using the designed voltage comparator as the main building block, a 4-bit flash A/D converter was built which is capable of operating at sampling clock frequencies up to 800 MHz with a signal-to-noise ratio of greater than 22.84 dB. It was verified that the designed 4-bit flash A/D converter is capable of processing input signal frequencies up to 80 MHz with 200 MHz sampling clock rate. Typical INL and DNL errors are less than 0.015 LSB and 0.025 LSB respectively.

Two possible implementations have been studied for the residue amplifier, which is one of the most important sub-blocks of a pipelined A/D converter. The single ended OTA-based circuit architecture was preferred in both of the designed versions, using a 1.8 V single power supply. The open-loop unity-gain frequency of the designed high gain op-amp is 2.16 GHz, while its open-loop gain is approximately 48.5 dB. Consequently its closed-loop 3dB frequency is 665 MHz, and input referred offset is 1.2 mV. The second implementation is a unity-gain stable (low gain) op-amp with an open-loop gain of 33.4 dB and 1.4 GHz unity gain frequency. Its closed-loop (unity gain configuration) 3dB frequency is 1.43 GHz. The input referred offset of the second op-amp implementation is less than 4 mV. With these operational characteristics, both of the designed op-amps are suitable for 12-bit data conversion at 200 MHz sampling clock frequency.

D/A converters play a very critical role in pipelined ADC architectures. Resolution and conversion speed mostly depend on how fast and accurate the DAC can generate its response. Based on the residue amplifier blocks described above, the typical response time of the monotonic MDAC (multiplying DAC) that was designed for this architecture is about 400 ps, allowing 200 MHz operation speed in the analog pipeline.

Finally, the performance of the digital pipeline depends critically on the response time of the error correction circuit that includes the 11-bit adder chain. Totally symmetric 1-bit full adder circuits were designed and used in a ripple-carry adder chain to facilitate the required 11-bit addition. Typical response time of the eleventh carry-out signal is about 1.8 ns, which is sufficient for operation at 200 MHz clock frequency.

All analog as well as digital sub-blocks of the ADC architecture presented in this work operate on a single clock signal (and its inverse), which significantly simplifies the design while ensuring a more robust performance. Other important features of this ADC include small area, single power supply, low power consumption, capability to operate at very high sampling clock rates, and the ability to handle a wide range of input signal amplitudes. The analog processing modules were designed using single-ended signals and the single-ended building blocks (as opposed to differential signals and building blocks) for simplicity. The ADC architecture was realized using a conventional 0.18 micron digital CMOS technology (Foundry: UMC), which ensures a lower overall cost and better portability for the design.

The ADC architecture presented in this work is capable of operating at sampling frequencies of up to 200 MHz, and still can achieve the nominal bit-resolution that was intended for 12-bit accuracy. The entire circuit is designed with single 1.8 V power supply. The maximum range of the input signal amplitude that the ADC can handle is 1.6 Vpp, with 1.8 V supply voltage. The input signal range as well as the operating points of critical components can be adjusted externally using dedicated control pins. The overall power consumption is estimated as 67.5 mW at 200 MHz sampling rate. Each 4-bit pipeline stage consists of a 4-bit flash A/D converter, a fully capacitive multiplying DAC (MDAC) and the corresponding digital encoding circuitry. The overall silicon area of the ADC is approximately 0.25 mm^2.

To summarize, the ADC architecture presented in this thesis is intended as a state-of-the-art data converter for very high-speed applications such as digital video transmission or high bandwidth wireless communication needs. It can be used either as a stand-alone single-chip unit, or as an embedded IP block that can be integrated with other modules in various SOI (system-on-chip) applications.

APPENDIX A

LITERATURE SURVEY ON ANALOG-TO-DIGITAL CONVERTERS

Year	Bit	Sampling Rate	Linearity	Power	Architecture	Applications	Die Size
75 Dec.pg 386	12	20kHz	-0.1	300mW	Pipeline	Custom analog procees chip "A High precision Component Tolerant ADC"	90*125mil
75 Dec.pg392	16	200MHz	3%	0.9W	Gray code parallel	Quantizer "A Monolithic voltage comparator array for A\D Converters"	98*104mil
76 June.pg408	11	20S/s	%0.0125	10V	Constant slope	"An All MOS A\D Converter"	
77 Dec.pg 662	6	50S/s	%0.01	30mW	Monolithic charge balancing	Analog meters to digital meters "A Charge-Balancing Monolithic A\D Converter"	131*133 mils
78 Dec.pg 736	10	40kHz	no mising codes	16V	Monolithic I2L LWT Thin film resistor	measurement instrumentation control "A Monolithic 10 Bit A\D Using I2L and LWT Thin Film Resistors"	120*151 mils
78 Dec. pg 779	12	20MHz	%0.1	6mW	C2MOS dual slope integrating	Micro processor systems "Anew single chip c2mos A\Dconverter for miroprocessor Sys..."	4.3*3.9 mils
78 Dec. pg 785	8	1MHz	1 LSB		All MOS monolithic resistor string conver.	CODEC systems "A Single Chip All-MOS 8bit A\D Converter"	14000 mil2
79 June. Pg 547	8	1kHz	0.62 LSB		cascade of several folding amp.stages	Video applications nonlinear version for PCM speech encoding "A high speed 8bit A\D coverter based on a gray-code multiple..."	
79 Dec. pg 912	8	640kHz	1/2 LSB	25mW	Monolithic charge balancing	I/O port to microprocessor or memory "A Monolithic Charge Balancing Successive App. A\D Tech."	210*127 mils
79 Dec. pg 926	6	20MHz	0.5 LSB	50mW	Flash 4um	Video bandwidth comperision radar signature analysis, transient analy. Storage of osci.traces or	2.4*3.2 mm2
						relative data distortion analysis and high speed multiplexed data transition.	
79 Dec. pg 932	8	30MS/s	full 8b linear.	2.5mW	Monolithic fully parall.	High speed data communication,antialising filter commercial video processing radar sig. Processing	6.5*6.7 mm2
80 Feb. pg 38	8	200S/s	1%	400mW	Constant slope with external cap.	Microcomputer peripherial interface unit. "An NMOS Microcomputer *eripherial Interface Unit In.ADC"	3mm2
80	8	100MHz	full 8 bit linearity	850mW	Monolithic comparator arrays in parallel.	High definition radar,particularly radars with moving target indication and in instrumentation,fast digital	2.5*3 mm2
June. Pg 286						storage oscilloscopes and transient recorders. "Monolithic Components for 100MHz Data Conversion"	

Table A.1

Year	Bit	Sampling Rate	Linearity	Power	Architecture	Applications	Die Size
80 June. Pg 295	8	13.2us	pm1/2LSB	100mW	successive aprox.	"A High Speed NMOS A\D Converter with a Cuurent Source Arrary"	4mm2
80 Dec.pg 1040	12	25us	0.2 LSB	40mW	Monolithic	"Circuit Techniques for Achiveing High-Speed - High Resolution A\D Converters"	39000 mil2
80 Dec. pg 949	12	50us	0.1 LSB	100mW	Successive aprox. 3 IC	"A Fast Latching Comparator for 12Bit A\D Applications"	23000 mil2
79 Dec. pg 938	7	50MHz		520mW	2 step parallel lacthing comp.	Radar and video systems. "A High-Speed 7Bit AD Converter"	2.4*2.5 mm2
82 Dec.pg 1088	12	2MHz	0.2 LSB	120mW	Successive aprox. sensing the polarity	"A Fast Latching Current Comparator for 12Bit A\D Applications"	63000 mil2
					of input current.		
82 Dec.pg 1112	14	44.1kHz	pm1/4LSB	450mW	successive aprox. dynamic ele. match	hifi audio coding systems with high overall S/N ratio low distortion,high temp.stability of reference source allows applications of this comp.to industrial & other professional systems.	3.5*4.4 mm2
84 Dec. pg 842	8	100MHz	pm1/3LSB	1.2W	Flash	high definition video sys.,in radar sys.with moving object indication,instrumentation,fast digital oscilloscope and transient recorders. "An 8 Bit 100MS/s Flash ADC"	4.15*5.35 mm2
84 Dec. pg 995	13	12MHz		20mW	İnterpolative pulse density modulator	very critical analog functions that are not feasible with monolithic integration.	2.0*1.45 mm2
82 Dec. pg 723	10	20MHz	pm1/2LSB	2W	Fully parallel	vVideo speed TV sysytems. "A Fully Parallel 10Bit AD Converter.."	9.2*9.8 mm2
83 June.pg 374	14	50kHz	0.2LSB	450mW	Monolithic dual chan. coars-fine integration	PCM audio systems. "A Monolithic 14 Bit 20us/s Dual Channel ADC"	3.35*3.35 mm2
84 Dec. pg 837	8	120MHz	1/4LSB	2W	Flash	high definition TV's or PCM optical transmission sys. instruments in fast wave analyzer&digital storage osc.	
84 June.pg 374	8			520mW	2 step parallel Flash	Video "A Monolithic 8 Bit Video AD Converter"	3*4.2 mm2

Table A.2

Year	Bit	Sampling Rate	Linearity	Power	Architecture	Applications	Die Size
85 June. Pg 775	8	20MHz	pm1/2LSB	350mW	Fully parallel	Video "A CMOS HİGH Speed A\D Converter IC"	4.8*6.3 mm2
85 June. Pg 780	6	200MHz	pm0.1LSB	1.1W	Full Flash	"A 6bit 200MHz Fully Nyquist A\D Converter"	4*2.2 mm2
85 Dec.pg 1138	8	8MHz	0.3LSB	20mW	Subranging 3um	Video,digital siganl processing. "An 8 bit CMOS Subranging ADC"	3.2*2.2 mm2
86 April.pg 318	8	20MHz	<pm0.5LSB	150mW	1st order self calibrat. ΣΔ	Process control,medical,scientific instruments digital audio etc.	3*1.1 mm2
86 June. Pg 446	14	12MHz	approx.14b	60mW	Flash	Video systems, TV's VCR's "A Compatible CMOS-JFET Pulse Density Modulator for ..."	3.08*2.56 mm2
86 Dec.pg 1016	12	2.5MHz	pm1/2LSB		successive approxi. digital error correction	"A 12 bit Successive Approximation Type ADC with Digital Error Correction"	1800 mil2
87 April.pg 157	16		<pm0.6LSB	150uW	Switched capacitor 4u ΣΔ	telemetry,instrumentation measurements require high accuracy,excellent linearity negligible dc offset,speech audio,video.	2.7 mm2
87 April.pg 295	6		<1/6LSB		2 stage Flash monotonic dual ladder	"Monotonic Dual-Ladder AD Conversion"	
87 Dec. pg 921	16	<3MHz		110mW	1st order 2um ΣΔ	High quality audio & high accuracy measurement systems.	2.7*2.7 mm2
87	6	30MHz	<pm1/2LSB	12mW	Flash	video freq.video&measuring equip.,liquid crystal TVs portable measuring equip. Such as digital osc.	1.5 mm2
Dec. pg 939	8	55MHz		300mW	Flash folding&interpolating	video and professional systems. "A 12mW 6 bit Video Frequency A\D Converter"	6 mm2
87 Dec. pg 944	9	5MS/s	<0.6LSB	180mW	Pipelined	Complex high-speed image processing. "An 8 bitVideo ADC Incorporating Folding and Interpolating ..."	8500 mil2
87 Dec. pg 962	6	1GHz	pm0.3LSB	16W	Interleaved	Digitizing oscilloscopes. "A 1 GHz 6 bit ADC Sysytem"	2.2*3.5 mm2
86 June.pg 436	7	30MS/s	pm0.5LSB	350mW	Flash	Digital video signal processing,high speed data conversion.	3.5*3.6 mm2

Table A.3

Year	Bit	Sampling Rate	Linearity	Power	Architecture	Applications	Die Size
88 Dec.pg 1324	12	1MS/s	12bit linearity	400mW	Pipelined cap.array avaraging	High performance medical,industrial and military applications.	14 mm2
88 Dec.pg 1309	14	100kHz	0.5LSB	480mW	Subranging Flash	"A 14bit 10us Subranging A\D Converter with S/H"	260*260 mil
88 Feb. pg 152	8	8kHz	0.5LSB	5V	Cyclic 2um	"A Cyclic A\D Converter that Does not Reguire Ratio-Matched Components"	0.79 mm2
88	15		<0.3LSB	325uW	2nd orderoffset & charge injection comp.	Telecommunication,dedicated to applications which can tolerate offset&gain errors.	4.6 mm2
June. Pg 736					ΣΔ	measurement&instrumentation. "A Second-Order High Resolution Incremental ADC ..."	
88 Dec.pg 1316	13	250kS/s	0.5LSB	15mW	Pipelined	high speed telecommunication sys.,ISDN,applications that require complex signal processing.	3400 mil2
88 June pg 742	4	1GS/s	1LSB	2.4mW	Flash	Video. "A Silicon Bipolar 4bit 1GSample/s Full Nyquist A\D Converter"	1.5*2.9 mm2
88 Aug. pg1017	4	>20GHz			periodic-threshold Josephson	"A New High Speed Periodic Threshold Comparator for ..."	
88 Dec.pg 1334	8	100MHz	0.5LSB	800mW	Folding & interpolating	is used to optimize the speed of converter with respect to technology used.	3.2*3.8 mm2
88 Feb. pg 198	4	1MS/s	<pm0.4LSB	18mW	Flash (SOI)	"A SOI Structure for Flash A\D Converter"	1.25*3.00 mm2
90	10	15MHz	1.1/-0.8LSB	250mW	2 step recycling	video signal procesisng,high quality video reproductioni image recognition(Xray,ultrasonic imaging)digital	1.75 mm2
Dec.pg 1328						instrumentation,radar,digital radio tape,HDTV.	
90 Dec.pg 1339	10	75MS/s	pm1LSB	2W	2 step fully diff. subranging	consumer oriented Tv-digital video signal processing In professional imaging sys.,HDTV	4.8*4.2 mm2
89 Feb. pg 13	10	20MHz	pm0.5LSB	900mW	2 step parllel	high quality video sys.,high definition video sys.,video tape recorde for business,digital video cameras.	25 mm2
89 April pg 241	10	5MS/s	0.6LSB	350mW	2 step fully diff. Flash	image recognition,high defition TV's, digital video. "A 10bit 5MS/s CMOS Two Step Flash ADC"	54000 mil2

Table A.4

Year	Bit	Sampling Rate	Linearity	Power	Architecture	Applications	Die Size
89 Decembre	12	500ns/4b	0.02%	650mW	Subranging		25 mm2
89 April pg 250	12	1MHz	0.5LSB	750mW	2 step Flash	Digital signal processing "A 12bit 1 MHz Two-Step ADC"	9.5*8.4 mm2
89	14	80kHz		75mW	ΣΔ 1.75um	ISDN,U_interface transreceivers,modems,digital audio tape(DAT),compact disc(CD) players,sonar	2 mm2
April pg 256						signal processing.	
90 April pg 431	16	160kHz		76mW	1st order 1.5um ΣΔ	ISDN , digital audio. "A 16bit 160kHz CMOS A\D Converter Using Sigma-Delta..."	3 mm2
90 April pg 562	4	>1GHz	pm0.5LSB	<100mW	Flash	Experimental for FIB. "A Deep-Submicrometer Analog to Digital Converter Using ..."	0.91 mm2
89 June pg 617	pm51/2	7.5 to 15/s	2 counts	50mW	Monolithic 3 step conversion	digital voltmeter,precision measurements recording DC or low freq.quantities (upto 22bits)	5.6*3.8 mm2
90 Dec.pg 1311	20	256kHz		125mW	4th order monolithic ΣΔ	"A Monolithic 20bit Delta-Sigma A\D Converter"	29.25 mm2
90 June pg 880	8	1.3MHz	<1LSB	70mW	Pipelined successive app.	"An 8bit 1.3MHz Successive-Approximation A\D Converter"	3750 mil2
90 Feb. pg 167	8	20MS/s	<pm0.5LSB	50mW	2 stage pipelined subranging	Video systems "An 8bit20MS/s CMOS AD Converter with 50mW Power Consup."	2.09*2.15 mm2
89 Dec. pg1485	8	50MHz		600mW	Pipelined subranging with S/H	Video signal processing "An 8bit 50MHz CMOS Subranging A\D Converter with ..."	3.2*4.3 mm2
92 Mar. pg 351	10	20MS/s	0.2LSB	240mW	9 stage pipelined fully diff.	"A 10b 20MS/s Analog to Digital Converter"	8.7 mm2
92 Dec.pg 1667	12	5MS/s	0.7LSB	200mW	2 step flash fully diff. 1um	avoid the need for opamp with high gain or large voltage swing	2.5*3.7 mm2
91 Dec.pg 1790	12	1.5MHz	pm0.5LSB	600mW	Multiple flash subranging	"A 12b 750ns Subranging A\D Converter with Self_Correcting..."	29.2 mm2
91 April.pg 628	13	2.5MHz	0.4/-0.6LSB	100mW	Pipelined self-calibrated 3um	wide dynamic range imaging,high resolution video. "A 13b 2.5MHz Self_Calibrated Pipelined AD converter ..."	26 mm2

Table A.5

Year	Bit	Sampling Rate	Linearity	Power	Architecture	Applications	Die Size
91 Dec.pg 1781	8	4GHz	pm1/4LSB		sample&filter	high sampling devices,digitizing oscilloscopes "A 4 GHz 8b ADC Sysytem"	
91 Dec.pg 1746	12	2MHz		41mW	cascaded multibit ΣΔ	voice band telecommunications,digital audio ISDN "A 50MHz Multibit Sigma_Delta Modulator for 12b 2MHz A\D Con."	0.65 mm2
92 July.pg 957	13	25kS/s	1/2LSB	45mW	cyclic redundent signed digit	 "A CMOS 13b Cyclic RSD A\D Converter"	2.9 mm2
92 Oct.pg 1313	5	1GS/s	pm0.4LSB	3400mW	Flash	measurement technology,HDTV,digital broadcasting radar technology	3*3 mm2
91 July.pg 910	20		0.25LSB	6.7mW	2um monolithic ratiometric	resistive thermometer, strain gauges "A Monolithic CMOS 20b Analog to Digital Converter"	14 mm2
91 Aug.pg 1103	10	20MS/s	1LSB	1W	Pipelined 2um	ultrasound & infrared imagers "A Wide Band 10b 20MS/s Pipelined ADC Using Current ..."	6.35*7.61 mm2
92 Dec.pg 1662	8	650MHz	<0.5LSB	850mW	Folding	 "An 8b 650MHz Folding ADC"	4.2 mm2
93 Mar.pg 292	10	50MHz	pm0.5LSB pm1LSB INL	900mW	3 stage pipelined 4b flash 0.8um	HDTV,video signal processing,VCRs & encoders "A 10b 50MHz Pipelined CMOS AD Converter With S&H"	6*3 mm2
94 Dec.pg 1531	10	20MS/s	pm0.5LSB pm1LSB INL	135mW	Pipelined multistage subranging 0.8um	HDTV video systems processing "A 10b 20MS/s 3V Supply CMOS AD Converter"	3.5*2.0 mm2
93 Dec.pg 1180	10	100MS/s	pm0.5LSB pm1LSB INL	950mW	pipelined subranging 0.8um	ultra high speed studio equipment for HDTVs "A 10b 100MS/s Pipelined Subranging BICMOS ADC"	3.4*5.6 mm2
93 Dec.pg 1200	10	20MHz	pm0.5LSB	30mW	pipelined interpolating	audio-visual equipment "A 10b 20MS/s 30mW Pipelined Interpolating CMOS ADC"	2.6*2.5 mm2
93 April.pg 516	10	300MHz	pm0.4LSB	4W	interpolating parallel &folding 1um	high speed measuring,medical engineering systems& HDTVsystems	9.0*4.2 mm2
93 Dec.pg 1187	10	75MHz	pm0.5LSB pm0.75LSB	800mW	2 stage pipelined 4b flash	video signal processing, HDTVs "A 10b 75MHz Two_Stage Pipelined Bipolar ADC"	4.4 mm2
94 Aug.pg 866	10	5MS/s	pm0.5LSB pm0.68LSB	18mW	successive approach SA a.2um	"A 10b 5MS/s Successive Approximation ADC Cell Used in a70MS/s ADC Array in 1.2um CMOS"	0.6 mm2
94 Aug.pg 967	10	550kHz	0.8LSB	20mW	pipelined switched current	 "A 10b Pipelined Switched-Current A\D Converter"	2.5 mm2

Table A.6

Year	Bit	Sampling Rate	Linearity	Power	Architecture	Applications	Die Size
93 Dec.pg 1606	6	100MHz		252mW	Fully parllel	PRML magnetic disk read channel interface "A 100MHz AD Interface for PRML Magnetic Disk Read Channel"	256*258 mil2
94 April.pg 509	12	600kS/s	pm0.6LSB pm1LSM	45mW	2 stage pipelined digital. self cal.1.6um	"A 12b 600ks/s Digitally Self-Calibrated Pipelined Algorithmic ADC"	1 mm2
93 Dec.pg 1207	15	1MS/s	pm0.25LSB pm1.25LSB	1.8W	Pipelined digitally self calib.2.4um	"A 15b 1MSample/s Digitally Self-Calibrated Pipelined ADC"	9.3*8.3 mm2
93 June.pg 640	16	320kHz		65mW	3rd order 2 stage ΣΔ	audio applicatlications "A 16b 320kHz CMOS AD Converter Using Two_Stage ..."	1.6 mm2
94 Aug.pg 879	8	25MS/s	0.5LSB DNL 0.5LSB INL	540mW	Full flash 1um	sensors,tuners,display elecronics,power amplifiers,display drivers "A 25MS/s 8b CMOS AD Converter for Embedded App."	2.8 mm2
94 Aug.pg 873	6	80MS/s		400mW	Flash 1um	teelcommunication receivers "A 5V 6b BiCMOS Flash ADC"	2.0*3.0 mm2
94 Aug.pg 857	16	48MHz		180mW	4th order 3 stage ΣΔ	"A High Frequency and High Resolution Fourth_Order Sigma_Delta AD Converter in BiCMOS Technology"	2.9*1.8 mm2
93 July.pg 725	8	13.5MHz	pm1LSB	150mW	Half flash subranging 1um	visiophony , ISDN "A Low Power 8b 13.5MHz Video CMOS ADC for Visiophony..."	2.9 mm2
91 April.pg 455	12	200kHz	pm1/2LSB	10mWw	Fully differential 1um	"A Low Power 12b Analog to Digital Converter with On Chip ..."	15000 mil2
94 Dec.pg 1514		500kHz		180mW 85mW	4th order 3 stage ΣΔ	stereo audio "A Stereo Audio Sigma-Delta Converter"	4.7*5.5 mm2
96 Sep.pg 1336	8	1.2GS/s		460mW	monolithic	digitizing oscilloscopes "a 1.2GS/s 8b Silicon Bipolar Track&Hold IC"	1.45*1.12 mm2
95	10	20MS/s	0.6LSB	35mW	pipelined 1.2um	portable video devices camcorders,personal communi. wireless LAN transreceivers read channels of magnetic	3.2*3.3 mm2
Mar.pg 166						storage devices.	
95 May.pg 514	10	20MS/s	pm0.6LSB	50mW	8 identical unscaled pipelined 1.2um	high definition video reproduction computer graphics X-ray,medical imaging	13 mm2
96 Oct.pg 1507	10	40MS/s	0.3/-0.6LSB 0.6/-0.9LSB	<400mW	Pipelined	advanced digital signal processing "A 10b 40MS/s BiCMOS A\D Converter"	30700 mil2

Table A.7

Year	Bit	Sampling Rate	Linearity	Power	Architecture	Applications	Die Size
96 Jan.pg 70	14	25MS/s	pm0.5LSB	500mW	Pipelined	applications such as high&still imaging CCD,PMT,high data rate digital communication over twisted pair ADSL	5.4*4.4 mm2
96 July.pg 938	6	175MS/s	1/0.8LSB	160mWw	Full flash 0.7um continous time analog	mixed signal processing systems with feedback "A 175MS/s 6b 160mW 3.3V CMOS ADC"	12 mm2
95 Dec.pg 1533	10	20MS/s	pm0.5LSB pm0.5LSB	20mW	subranging mixed mode	video recorders,battery operated portable video systems "A 2V 10b 20MS/s Mixed Mode Subranging CMOS A\D Con."	3.2*3.8 mm2
95 Dec.pg 1326	10	200MHz		15mW	SHA	"A 200MHz 15mW BiCMOS S&H Amplifier Unit 3V Supply"	220*150 um2
96 Oct.pg		5GHz		89mW	Bandpass ΣΔ	digitizing IF signals in wireless radio receiver "A 5GHz SiGe zero Comparator BiCMOS for RF AD Converters"	407*143 um2
95 Oct.pg 1109	6	4HS/s	pm0.5LSB		Folding	digitizing oscilloscope,waveform recorders, radar signal caapture	
95 Dec.pg 1302	8	70MS/s	pm0.2LSB pm0.5LSB	110mW	Folding&interpolating 0.8um	"A 70 MS/s 110mW 8b CMOS Folding and Interpolating ..."	0.7 mm2
96 Nov.pg 1834	6	200MS/s	pm0.3LSB pm0.5LSB	110mW	Flash 0.5um	PRML read channel LSI,partial response max. Likehood "A CMOS 6b 200MS/s 3V Supply AD Converter for PRML ..."	0.8*2 mm2
96 Aug.pg 1201	14	10kHz	<=1LSB	50mW	Switched cap. algorithmic 0.8um	scientific&medical instruments,process control, digital audio "A CMOS Ratio Independent and Gain Insensitive Algorithmic ..."	2.1*0.8 mm2
95 May.pg 522	8	4.5MS/s	pm0.6LSB	16mW	Pipelined current mode	"A CMOS Transistor Only 8b 4.5MS/s Pipelined Analog to Digital..."	0.73 mm2/b
96 July.pg 945	8	15MS/s		350mW	Pipelined SI multistage 0.8um	video applications "A Fully Nyquist 15MS/s 8b Differential Switched Current A\D ..."	2.4 mm2
96 Feb.pg 169	12	1MHz	<1/2LSB	25mW	time interleaved multistep E2PROM	"A Low Power 1MHz 25mW 12b Time Interleaved ADC"	130*176 mil2
96		30MHz		270mW	multiple sampling	radio receivers,mixers,filters	6.4 mm2
96 Mar.pg 294	13	5MS/s	0.3LSB 0.8LSB	166mW	Pipelined 1.2um	medical imaging,high-speed data transmission sys. base stations for wireless	6.9*6.9 mm2
95 Mar.pg 153	10	40MS/s	pm1LSB	85mW	parallel pipelined 0.8um	HDTV MUSE,NTSC,S-VHS,high resolution TVs, ultrasound scanning	1.9*2.1 mm2

Table A.8

Year	Bit	Sampling Rate	Linearity	Power	Architecture	Applications	Die Size
96	8	125MS/s	0.8LSB	225mW	Folding current mode	HDTV,magnetic recording samplingdetectors,medical imager,digital trans.links for telephone,cable&terrestial	4 mm2
Sep.pg 1248						networks "CMOS Folding A\D Converter with Current Mode Interpolation"	
96 Aug.pg 1132	7	80MHz	<1LSB	307.2mW	Flash 1.2um	telecommunication&instrumentation for time-domain analysis "Power Efficent Metastability Error Reduction in CMOS Flash..."	1585*3037 mil2
97 Mar.pg 302	10	100MS/s	0.7/-0.3LSB	1.1W	Parallel pipelined 1um	"A 10b 100MS/s CMOS AD Converter"	50 mm2
97 Dec.pg 1876	12	60MS/s	<0.6LSB <1.5LSB	300mW	cascaded folding & interpolating	digital telecommunication applications "A 12b 60MS/s Cascaded Folding and Interpolating ADC"	7 mm2
97 July.pg 989	3000count		0.0015/100	90mW	Transducer	commercial & industrial weigh scales "A CMOS Soft-Switched Transconductor and its App...."	2.73*4.68 mm2
98	14	5MHz		9.6mW	3rd order 0.6um ΣΔ		1.06 mm2
98	10	200kS/s	<pm0.5LSB	12mW	Pipelined successive approx.	audio	5.12 mm2
97	6	166MS/s	pm0.5LSB	505mW	Flash folded cascode FCDL	PRML	2.5*2.4 mm2
99 Dec.pg 1812	12	125kS/s	pm0.21LSB	16mW	digital back ground calibrated algorithmic	"A 12b Digital Background Calibrated Algorithmic ADC with ..."	5.9 mm2
97 March	10	100MS/s	0.7/-0.3LSB	1.1W	Prallel Pipelined	high end video signal,high performance digital communication, medical imaging	50 mm2
97 Mar.pg 312	8	52MS/s	1LSB	250mW	Prallel Pipelined 0.9um	data communication, storage QAM pR detection	15 mm2
97	24	48kHz	pm10LSB	500mW	ΣΔ 0.7um	audio	25.8 mm2
97 July.pg 933	19	800Hz	10LSB	2.7mW	ΣΔ dataweighted avarag.	Instrumentation and geoseismic survery applications	19 mm2
97 July.pg 959			0.0015per.	140mW	Transducer	Industrial weigh scales "A Low Noise Low Drift Transducer ADC"	2.73*4.68 mm2

Table A.9

Year	Bit	Sampling Rate	Linearity	Power	Architecture	Applications	Die Size
97 July.pg 1122	4	4kHz		100mW	0.5um	telecınference systems,hands free telephone "A 3V 0.5um CMOS AD Audio Processor for a Microphone ..."	50 mm2
97 Sep.pg 1460	6	166MS/s	<pm0.5LSB	505mW	Flash FCDL	PRML read channels "Error Suppressing Encode Logic of FCDL in a 6b Flash ADC"	2.5*2.4 mm2
97 Dec.pg 1866	15	5MS/s	0.75/-0.6LSB 1.77/-1.58	60mW	Pipelined	RF,IF radio filters "A 15b 5MS/s Low-Spurious CMOS ADC"	27 mm2
97 Dec.pg 1876	12	60MS/s	0.25LSB	300mW	cascaded folding interpolating	digital telcommunication "A 12b 60MS/s Cascaded Folding and Interpolating ADC"	7 mm2
97 Dec.pg 1887	10	50MS/s	0.5LSB	240mW	Flash 0.5um	"An Embedded 240mW 10b 50MS/s CMOS ADC in 1mm2"	1.4*1.4 mm2
97 Dec.pg 1896	16	1.25MHz		550mW	ΣΔ Pipelined	wideband digital radio receivers and echo cancelled fuul duplex modems	5.7*6.2 mm2
98	8		pm4LSB	4.3uW	Flash 2 step 4bit	visual dat processing,hard disk controllers, handy dat terminals	0.52*0.36 mm2
98 Aug.pg 1244	10	200kS/s	1LSB	12mW	successive approximation	communication,wireless "Design&Implementation of a Untrimmed MOSfet only 10b ADC ..."	5.12 mm2
98 Dec.pg 1887	16	255MHz	pm0.4LSB	200mW	subranging pipelined	PRML read channels "A 900mW Low Power Delta-Sigma Converter with ..."	2.1*2.6 mm2
98 Dec.pg 1898	12	20MS/s	0.36LSB	250mW	self calibrating pipelined, 0.7um	digital telcommunication digital imaging "A Single Ended 12b 20MS/s Self-Calibrating Pipelined ..."	3.2*3.1 mm2
98 Dec.pg 1920	12	10MS/s	0.2LSB 0.4LSB	335mW	continously calibra. pipelined, 0.5um	DSP(digital signal processing) "A Continously Calibrated 12b 10MS/s 3.3V ADC"	3.71*3.91 mm2
98 Dec.pg 1932	6	400MS/s	0.9LSB	200mW	folding interpolating	LAN,hard disk drive read channels&communication circuits "A 400MS/s 6b CMOS Folding and Interpolating ADC"	0.6 mm2
98	6	400MS/s	0.2LSB	190mW	Flash	HDD's,digital video disks, LAN's "A CMOS 6b 400MS/s ADC with Error Correction"	1.6*0.75 mm2
98 July.pg 1065	15	40MHz		230mW	Nyquist rate ΣΔ	1um Fully differential switched cap. Circuts "A 15b 2MHz Nyquist Rate ΣΔ ADC in 1um CMOS Tech."	2.5*2.1 mm2
99 May.pg 599	10	14.3MS/s	0.5LSB DNL 0.7 LSB INL	36mW	Pipelined 0.6um	video rate, DSP "A 1.5V 10b 14.3MS/s CMOS Pipeline Analog to Digital Con."	2.3*2.5 mm2

Table A.10

Year	Bit	Sampling Rate	Linearity	Power	Architecture	Applications	Die Size
99 July.pg 912	6	500MS/s	0.32LSB DNL 0.2LSB INL	225mW	0.35um Full Flash	disk drive read channels .MHz	0.8 mm2
99 July.pg 927	15	52.8MHz		200mW	ΣΔ 0.5um	ADSL, high speed and resolution "A 3.3V,15b ΣΔ ADC with a Signal Bandwidth of 1.1MHZ ..."	5 mm2
99 Aug.pg 1056	6	75MS/s	< 1 LSB INL, DNL	110mW 3.3V	Folding 0.5um	dat commun.&data storage sys. High speed,medium resolution "Efficent 6bit AD Converter Using a 1bit Folding Front End"	1 mm2
99 Dec.pg 1777	13	18MHz	<.5 LSB	324mW	Pipelined ΣΔ 1.2um Nyquuist Rate	"A Nyquist Rate Pipelined Sampling A\D Converter"	
99 Dec.pg 1788	10	20MS/s	<.4 LSB DNL	75mW	Subranging	"A 75mW 10b 20MS/s CMOS Subranging ADC with 0.5 ..."	1.6 mm2
99 Dec.pg 1796	10	40MS/s	0.3LSB DNL% 1LSB INL	65mW	Nyquist cascode Folding &Interpolating bicmos	digital communication, video signaling "A 65mW,10b 40MS/s BiCMOS Nyquist ADC in 0.8um2"	0.8 mm2
99 Dec.pg 1803	10	25MS/s	0.7LSB DNL 0.9LSB INL	195mW 3.3V	Two step 0.35um	video, quadrature amplifier modulation,digital television "A 3.3V,10b,25MS/s Two_Step ADC in 0.35um CMOS"	
99 Dec.pg 1812	12	125kS/s	0.34 LSB DNL 0.21LSB INL	16mW 5V	Algorithmic 1.5um	imaging "A 12b Digital Background Calibrated Algorithmic ADC with ..."	5.5 mm2

Table A.11

APPENDIX B

COMPLETE CIRCUIT SCHEMATICS and MASK LAYOUTS

1. Complementary-Input Voltage Comparator

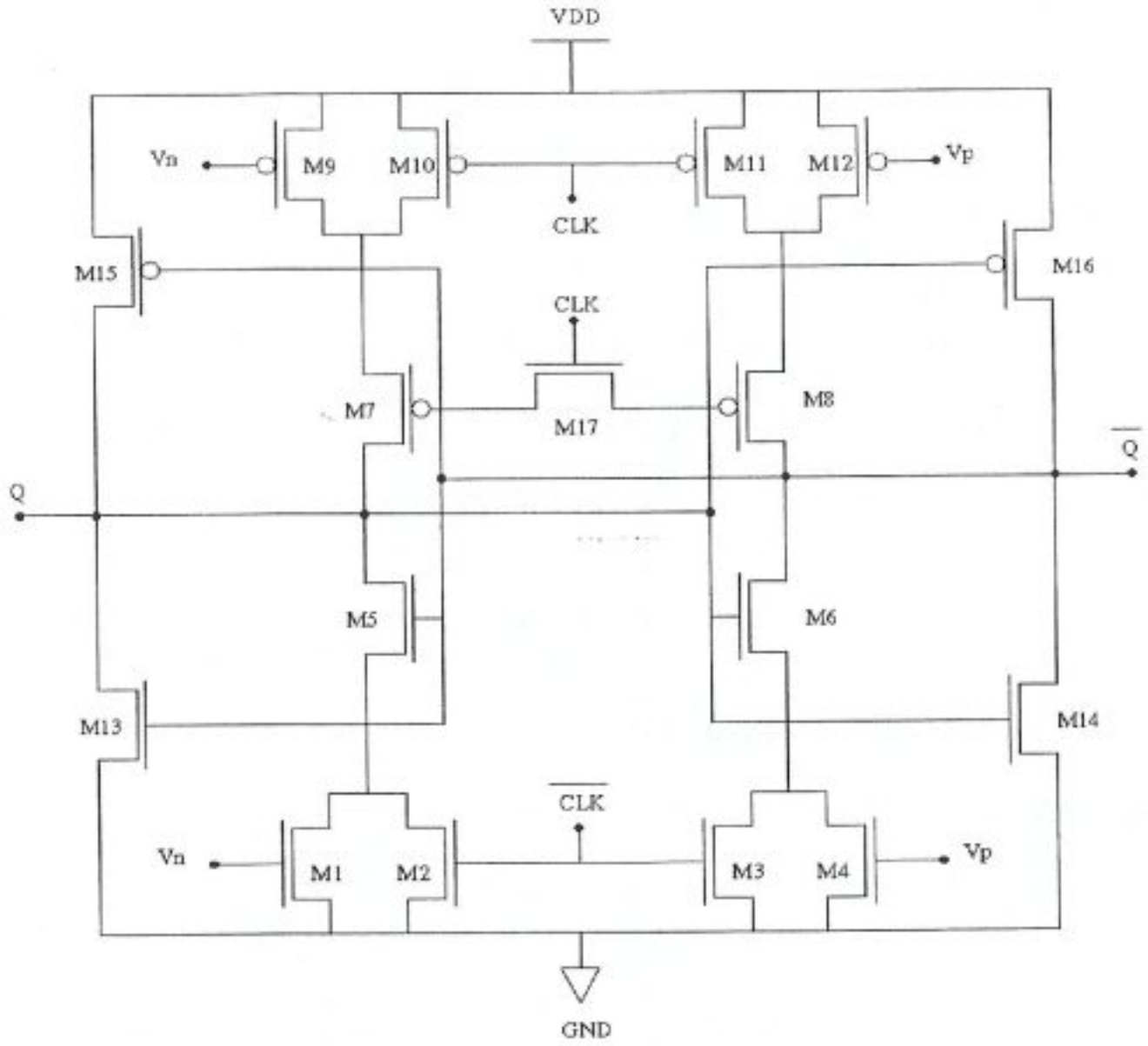


Figure B.1 Voltage comparator circuit schematic.

DEVICE LABEL	ASPECT RATIO (μm / μm)
M1 / M2	1 / 0.18
M3 / M4	1 / 0.18
M5 / M6	2 / 0.18
M7 / M8	5 / 0.18
M9 / M10	3 / 0.18
M11 / M12	3 / 0.18
M13 / M14	2 / 0.18
M15 / M16	5 / 0.18
M17	10 / 0.18

Table B.1 Voltage comparator transistor dimensions.

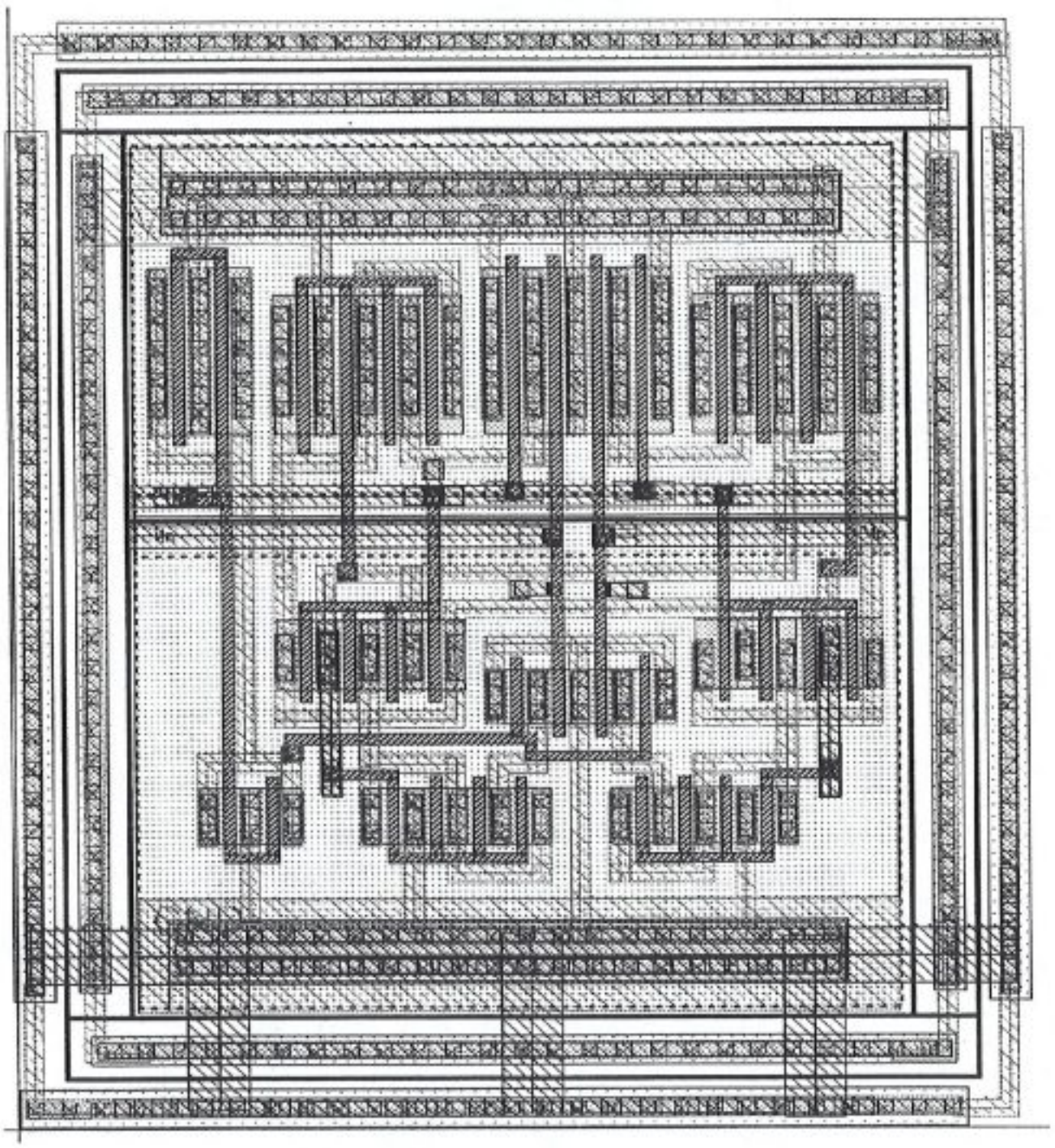


Figure B.2 Mask layout of the improved complementary-in voltahe comparator.
Silicon area is approximately 132 μm^2.

2. OTA-Based Operational Amplifier

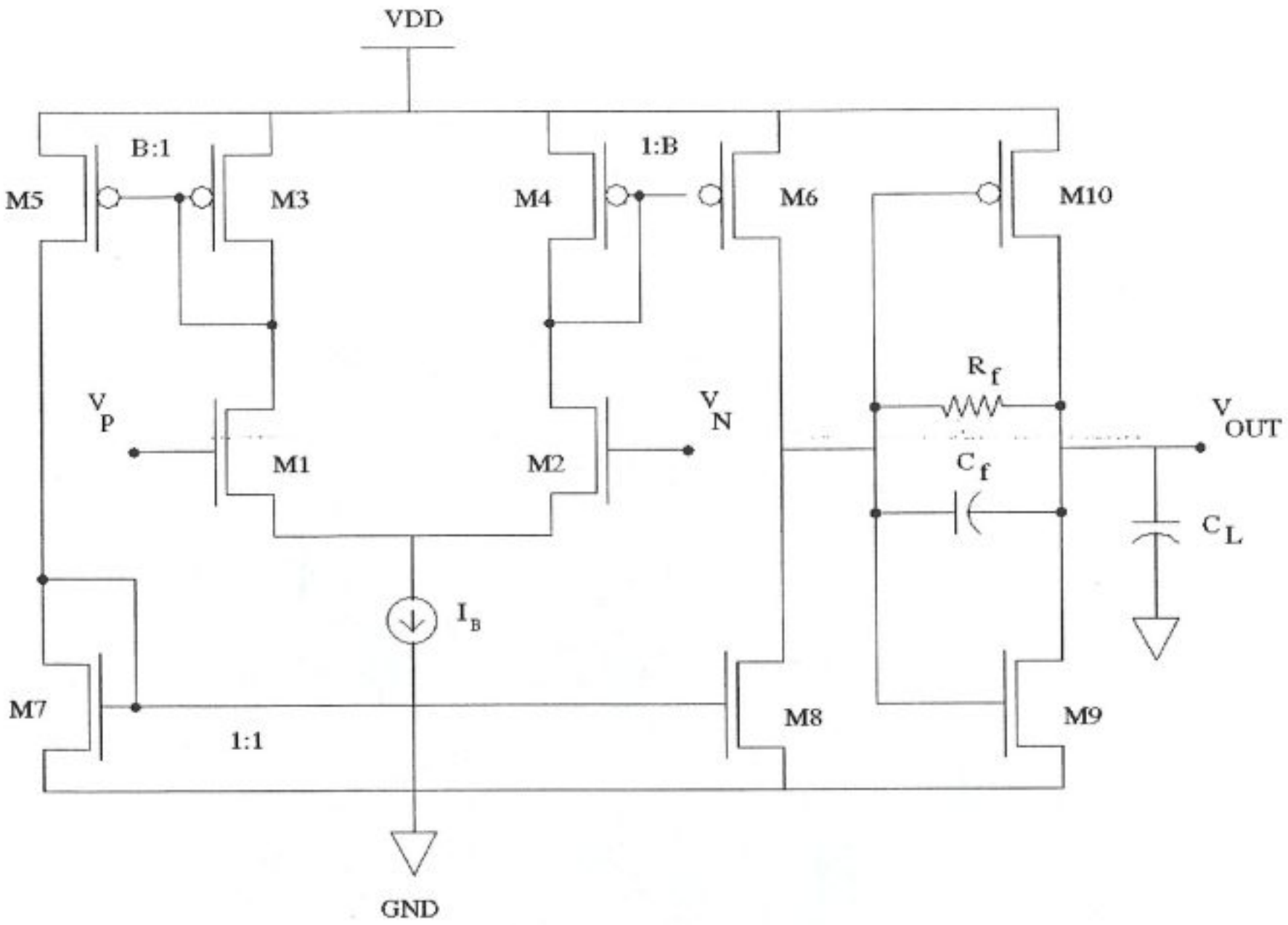


Figure B.3 OTA based op-amp circuit schematic.

DEVICE LABEL	ASPECT RATIO (μm / μm)
M1 / M2	10 / 0.5
M3 / M4	0.36 / 0.18
M5 / M6	3.6 / 0.18
M7 / M8	2 / 0.18
M9	7.2 / 0.18
M10	18 / 0.18
R_f	50 kΩ
C_f	100 fF

Table B.2 Op-amp transitor dimensions.

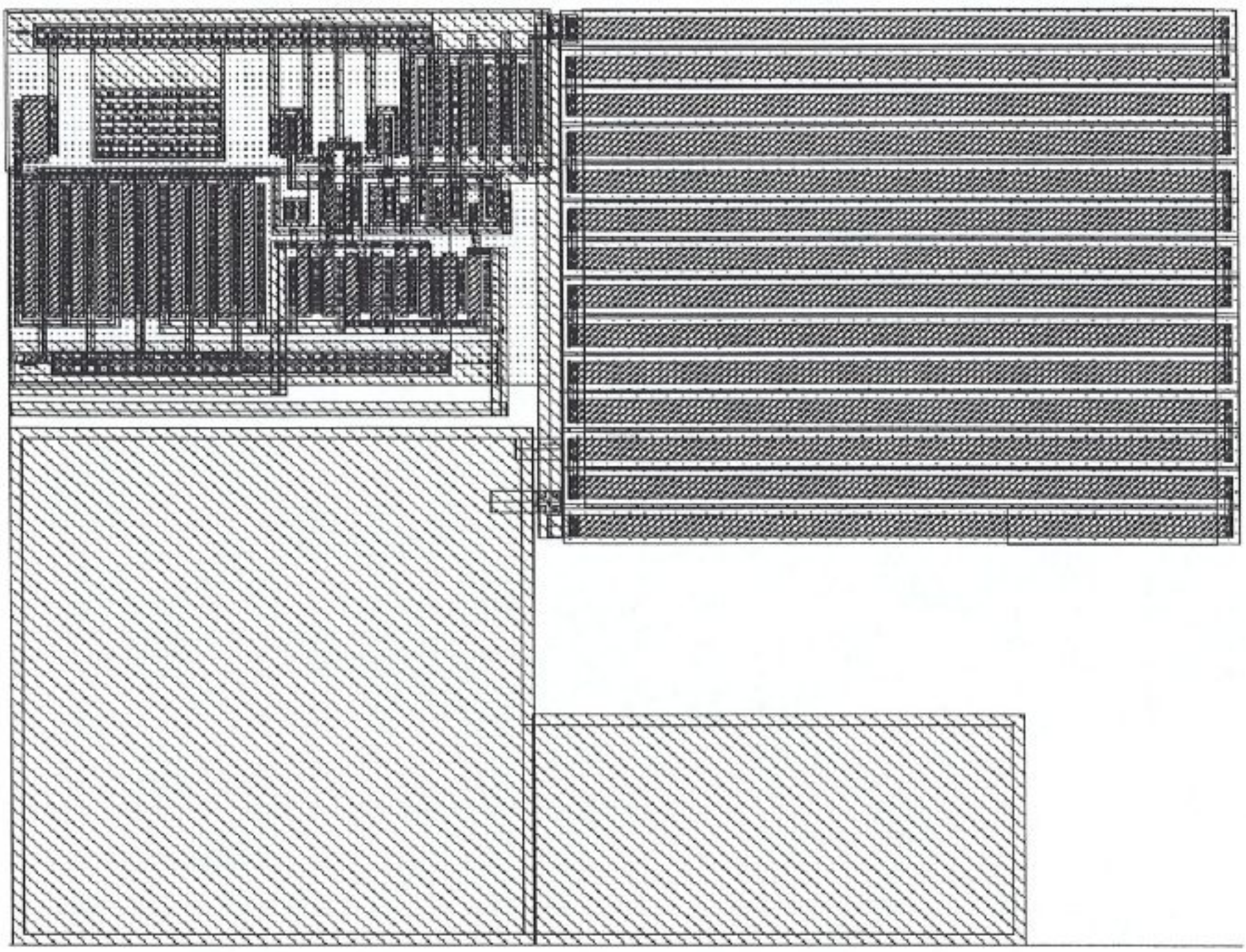


Figure B.4 Mask layout of the OTA based op-amp used as residue amplifier.
Silicon area is approximately 2230 μm^2.

3. D-Type Flip Flop (DFF)

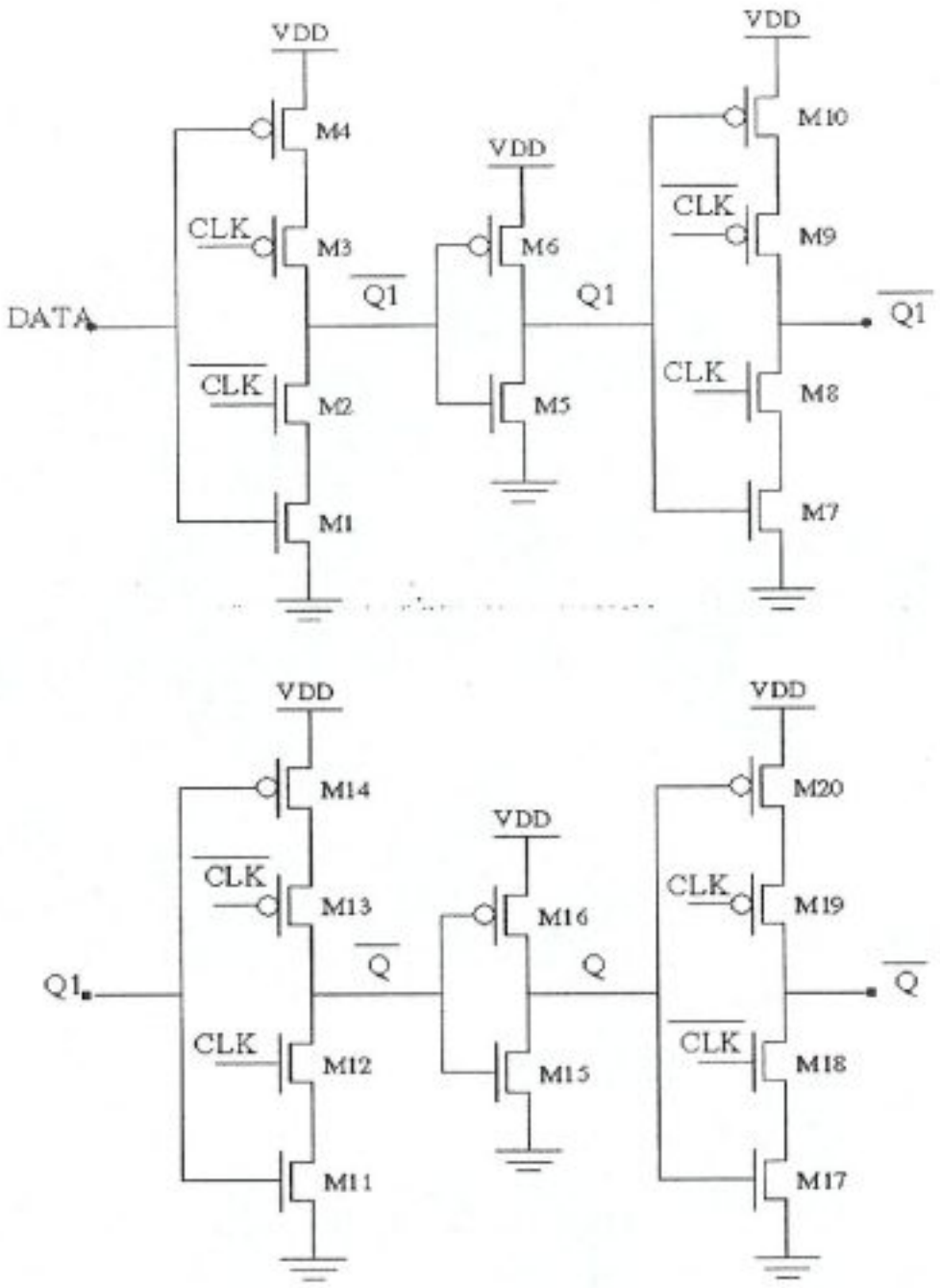


Figure B.5 Schematic of two stage master-slave rising edge triggered D-type flip-floop.

MOS NAME	ASPECT RATIO (μm / μm)
M4 , M9, M10, M20	1.5 / 0.18
M6, M16	1 / 0.18
M13 , M19	0.76 / 0.18
M3, M7, M8, M14,, M15, M17	0.5 / 0.18
M1, M5	0.3 / 0.18
M2, M11, M12, M18	0.28 / 0.18

Table B.3 DFF transistor dimensions.

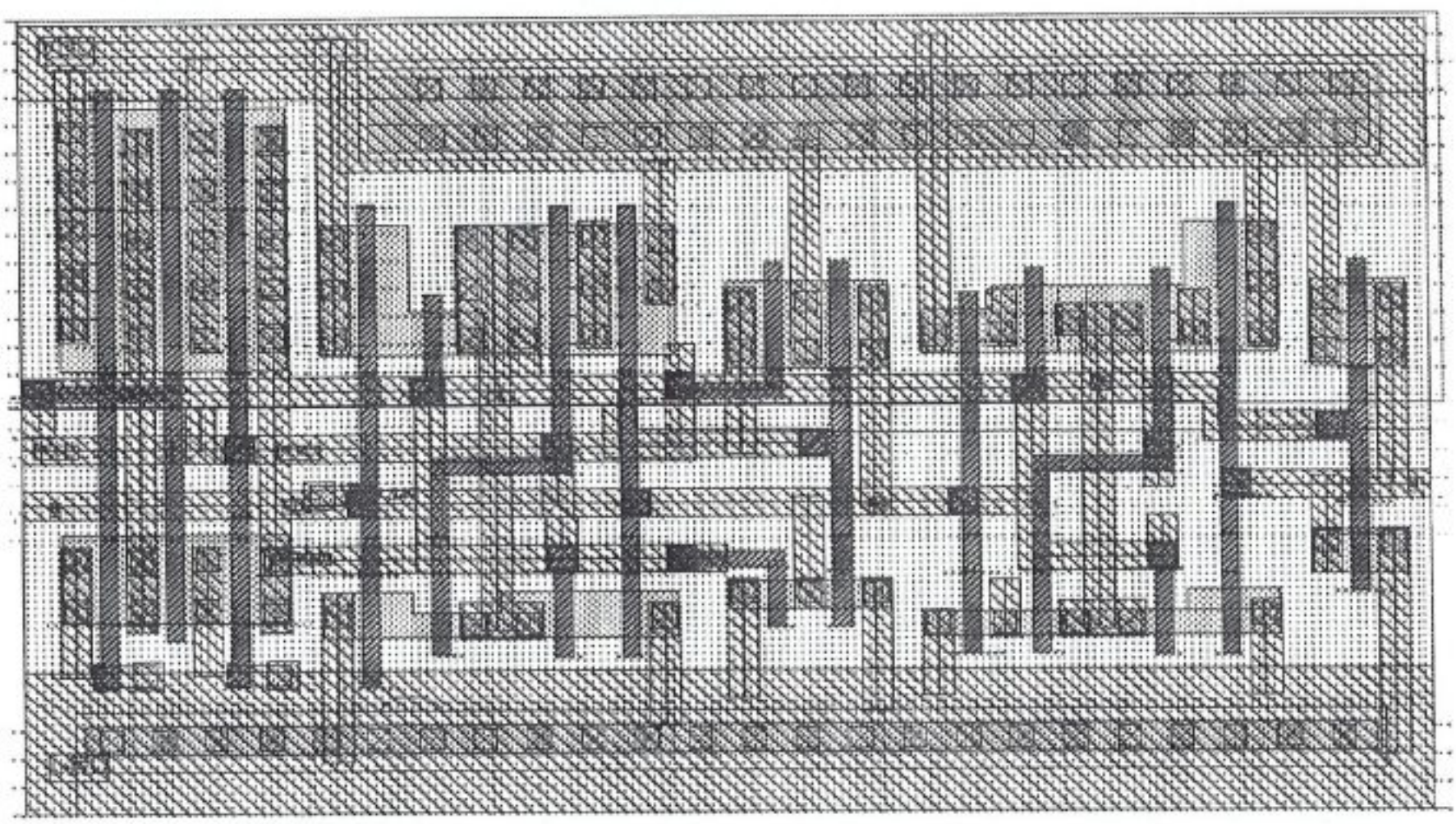


Figure B.6 Layout view of the designed type flip-flop.

Silicon area is aproximately 132 μm^2.

4. One-bit Full Adder

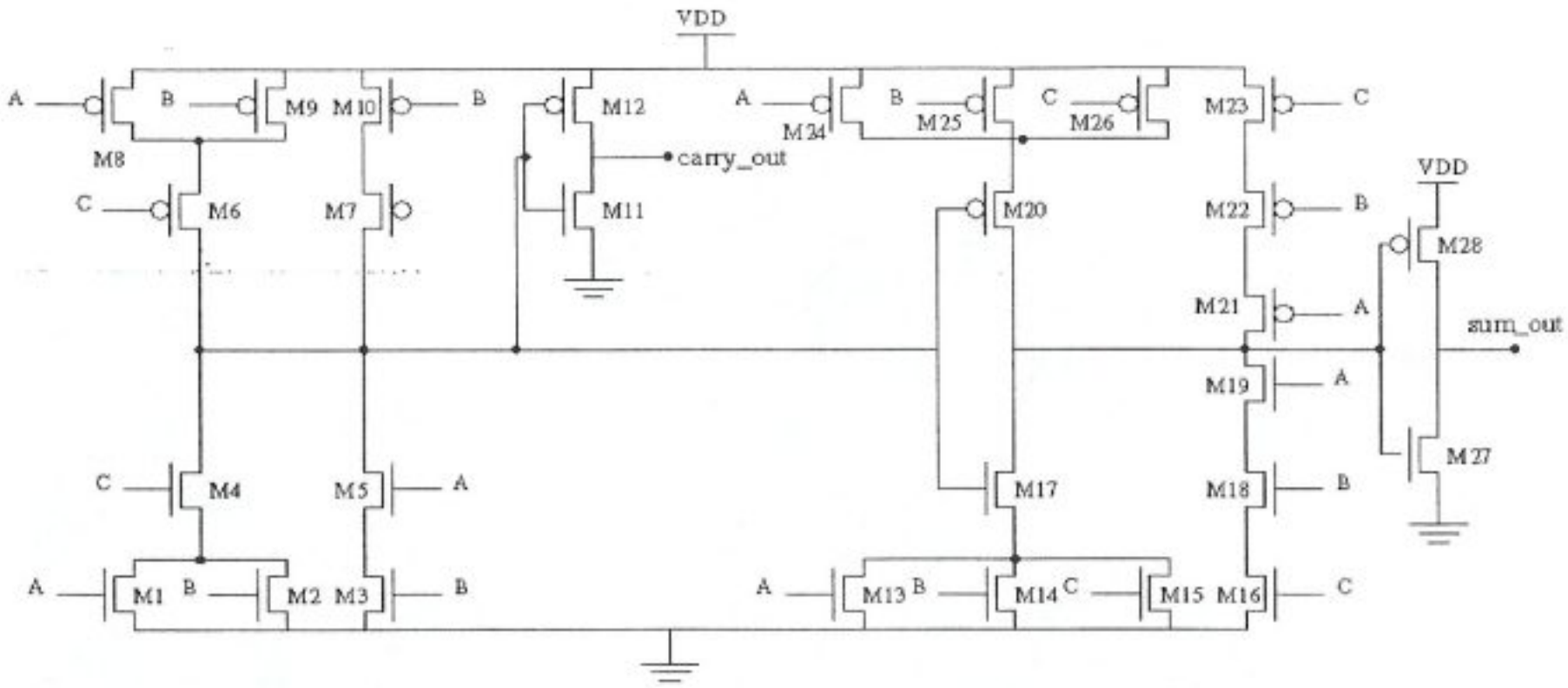


Figure B.7 Schematic view of the designed full adder circuit.

DEVICE LABEL	ASPECT RATIO (μm / μm)
M6, M7, M10	0.76 / 0.18
M3, M4, M5, M11,M12, M20, M21, M22, M23, M24	0.5 / 0.18
M8, M9	0.4 / 0.18
M1,i M2, M13, M14, M15, M16, M17, M18, M19, M24, M25, M26	0.28 / 0.18
M27	/ 0.18
M28	/ 0.18

Table B.4 Full adder transistor dimensions.

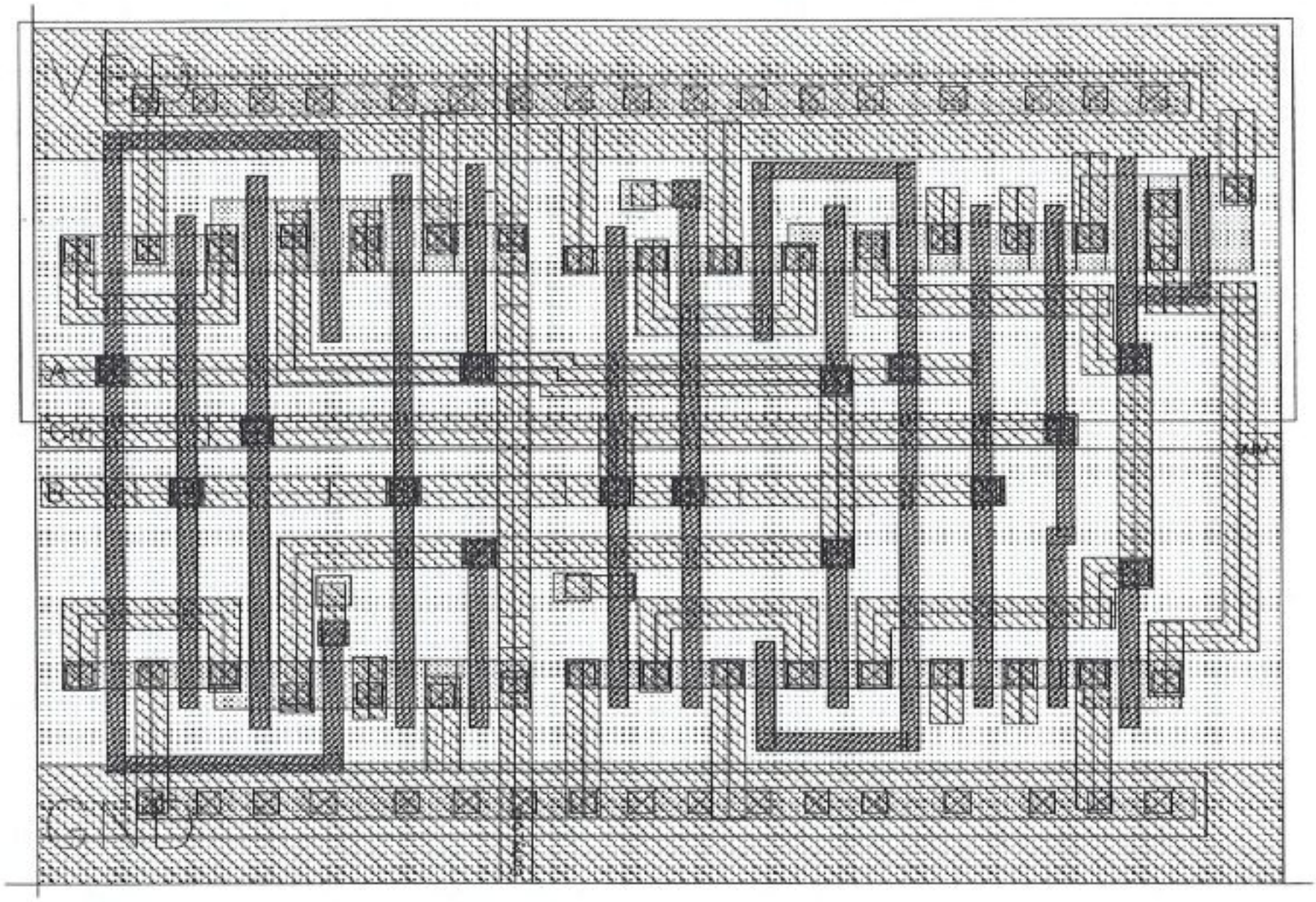


Figure B.8 Layout view of the designed 1-bit full adder circuit.

Silicon area is aproximately 107 μm^2.

5. XOR Gate

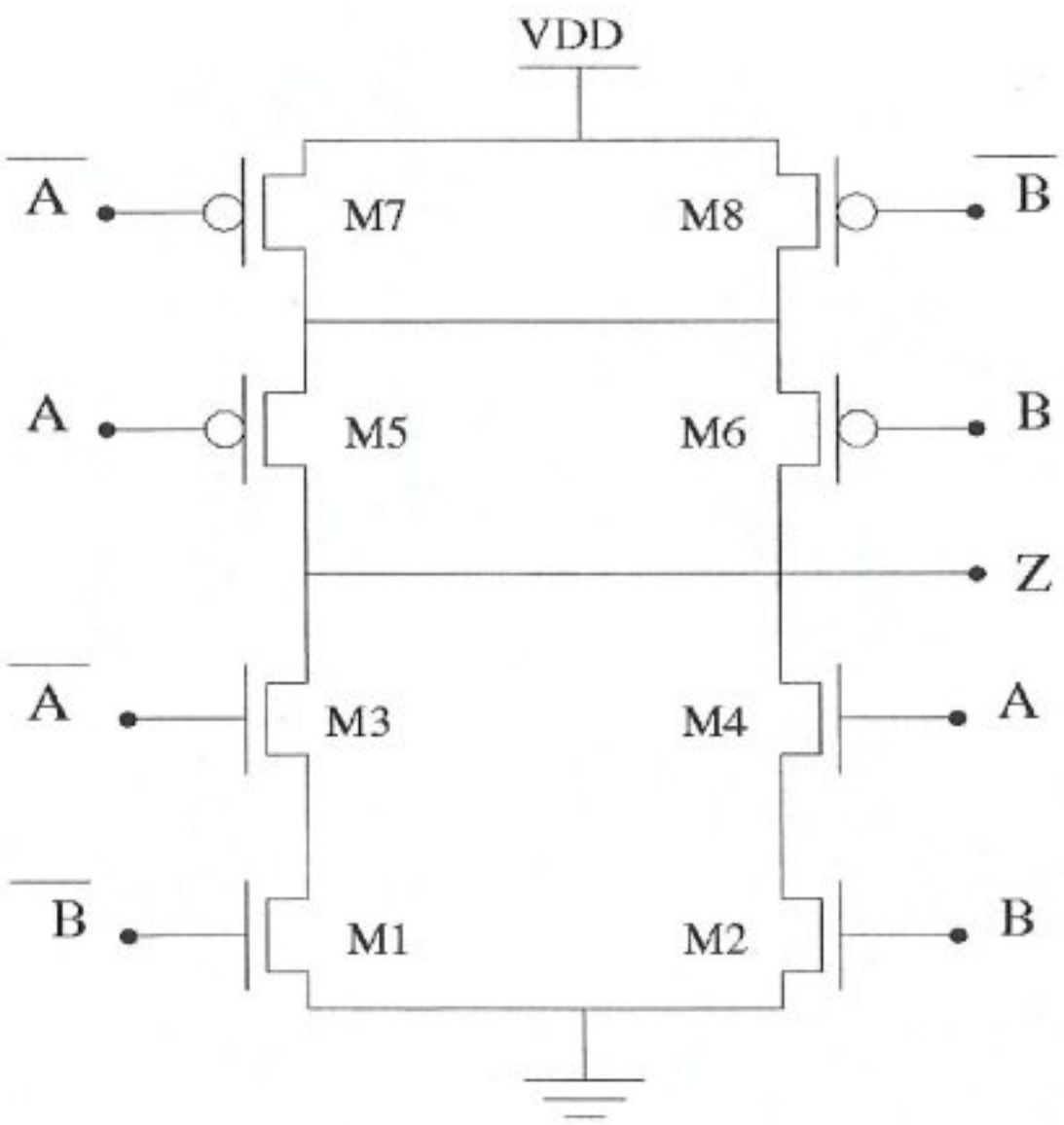


Figure B.9 Schematic view of the designed exclusive-OR (XOR) gate.

MOS NAME	ASPECT RATIO (μm / μm)
M1, M2, M3, M4	0.35 / 0.18
M5, M6, M7, M8	1.05 / 0.18

Table B.5 XOR gate transistor dimensions.

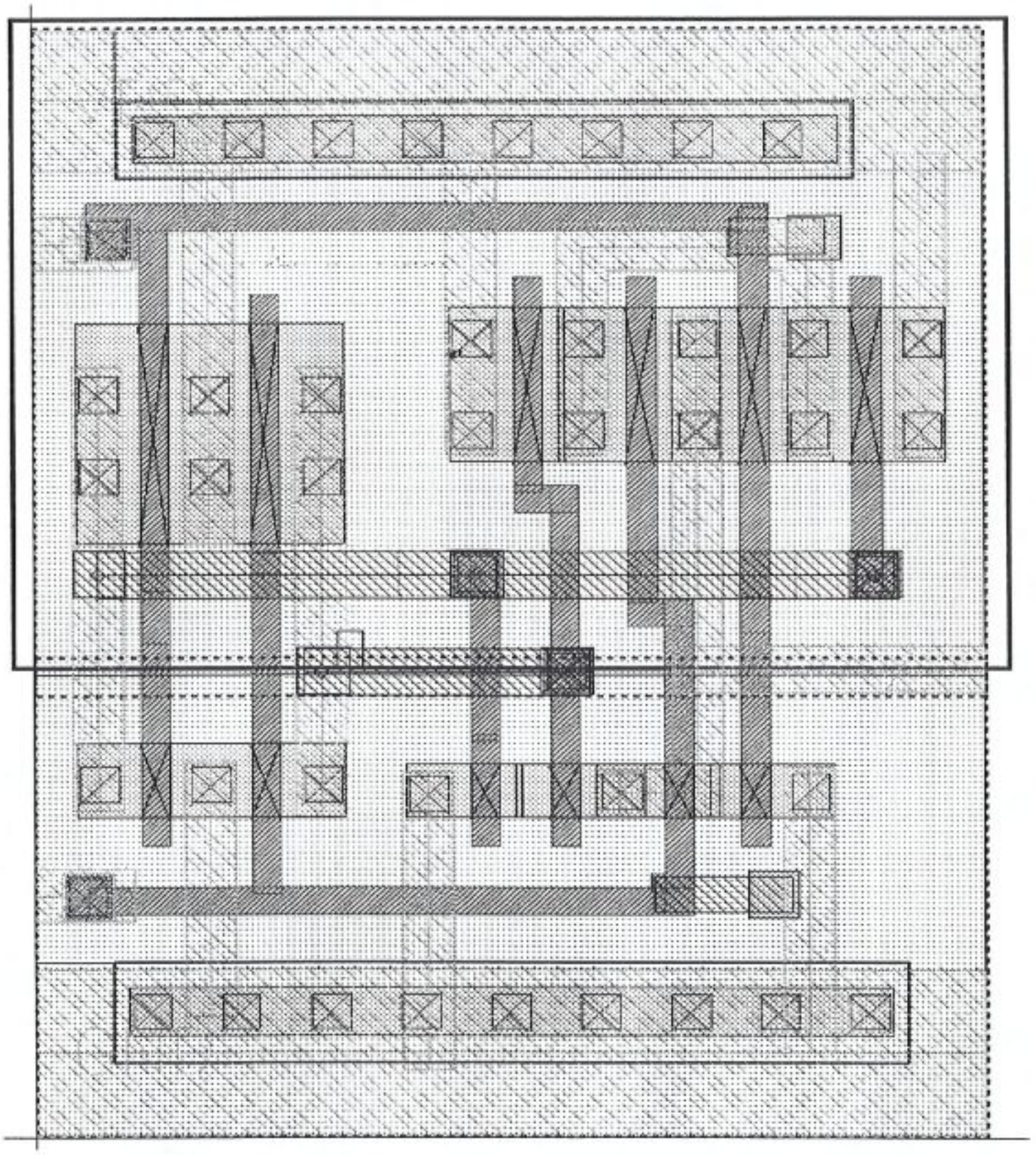


Figure B.10 Layout view of the designed exclusive-OR (XOR) gate.
Silicon area is aproximately 45 μm^2.

6. Thermometer-to Binary Encoder

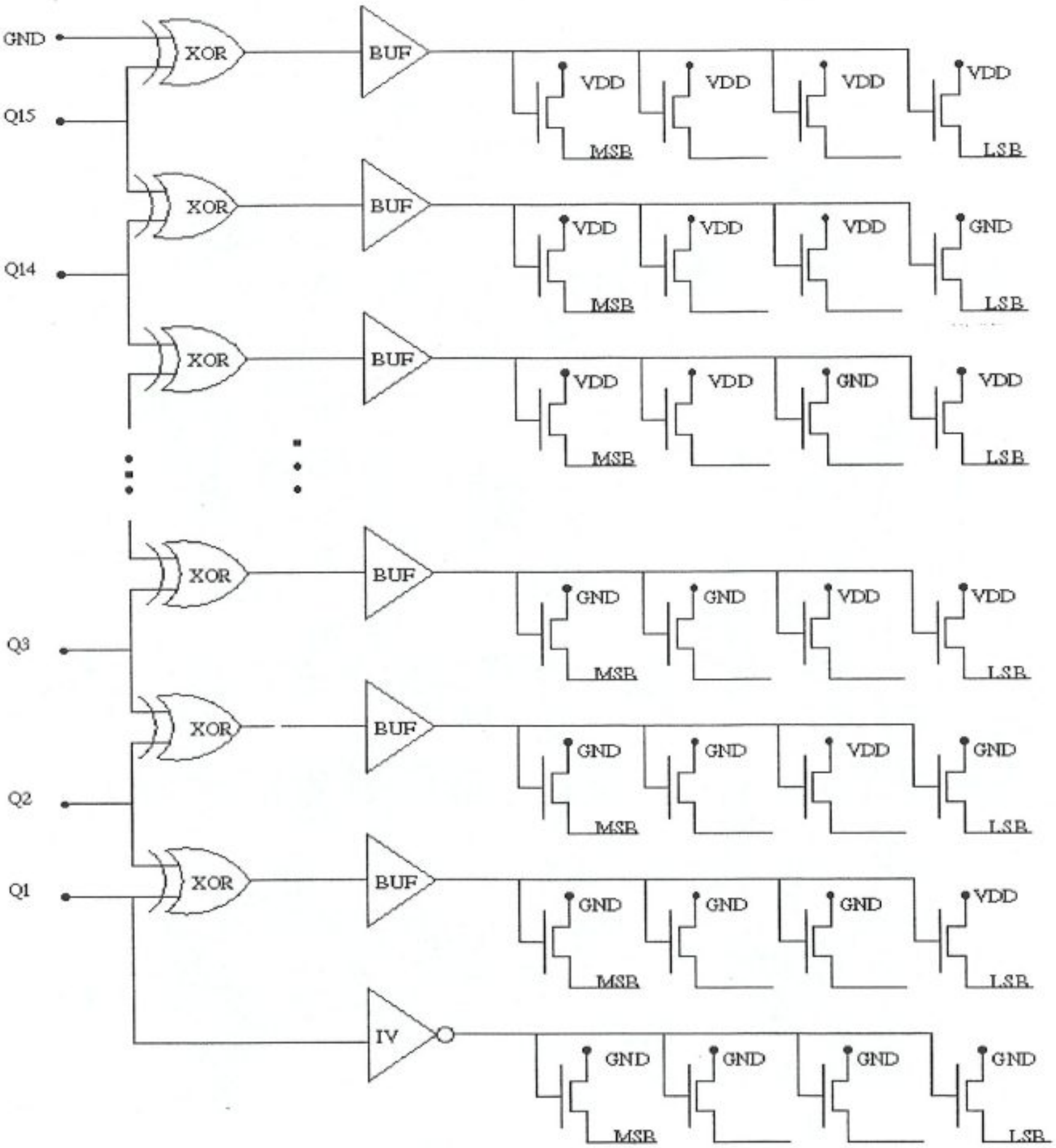


Figure B.11 Symplified schematic view of 4-bit *thermometer-to-binary* encoder.

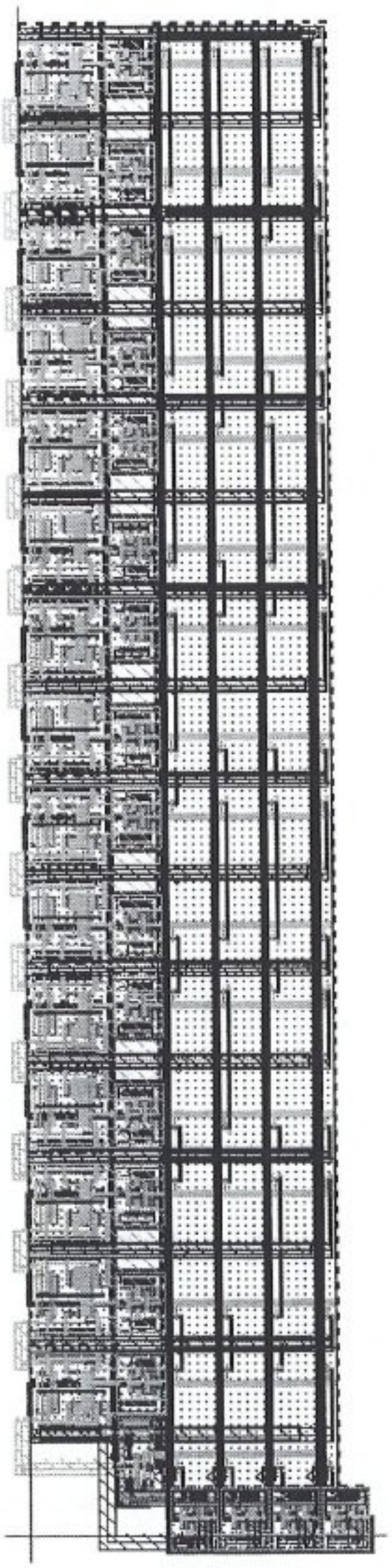


Figure B.12 Layout view of 4-bit thermometer to binary encoder.
Silicon area is approximately 3126 μm^2.

BIBLIOGRAPHY

[1] Laker K.R., Sansen W. *Design of Analog Integrated Circuits ans Systems*, McGraw-Hill, (1994).

[2] Johns D., Martin K. *Analog Integrated Circuit Design*, John Wiley and Sons, Inc., Canada (1997).

[3] Allen P.E., Holberg D.R. *CMOS Analog Circuit Design*, Oxford, New York (1987).

[4] Razavi B. *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, (2000).

[5] Cherry J.A., Snelgrowe W.M. *Continous-Time Delta-Sigma Modulators for High-Speed A/D Conversion Theory, Practice and Fundamental Performance Limits*, Kluwer Academic Publishers (1999).

[6] Van de Plassche R. *Integrated Analog-to-Digital and Digital-to-Analog Converters*, Kluwer Acaademic Publishers, Dordrecht (1994).

[7] Horenstien M.N. *Microelectronic Circuits and Devices*, Prentice Hall, New Jersey (1996).

[8] Weste N.H.E., Eshraghian K. *Principles of CMOS VLSI Design, A System Perspective*, Addison-Weslet Publishing Company (1993).

[9] Leblebici D. *Analog Elektronik Devreleri*, İ.T.U. Rektorlugu, Istanbul (2000).

[10] Kang S., Leblebici Y. *CMOS Digital Integrated Circuits Analysis and Design*, McGraw-Hill (1996).

[11] Cilingiroglu U. *Systematic Analysis of Bipolar and MOS Transistors*, Artech House (1993).

[12] Hoeschele D.F. *Analog-to-Digital and Digital-to-Analog Conversion Techniques*, John Wiley & Sons, Canada (1994).

[13] Sedra A.S., Smith K.C. *Microelectronic Circuits*, Oxford, New York (1998).

[14] Geiger R.R., Allen P.E., Strader N.R. *VLSI Design Techniques for Analog and Digital Circuits*, McGraw-Hill (1990).

[15] Ismail M., Fiez T. *Analog VLSI Signal and Information Processing*, McGraw-Hill, Singapure (1994).

[16] Hastings A. *The Art of Analog Layout*, Prentice Hall, New Jersey (2001).

[17] Geiger R.L., Allen P.E., Strader N.R. *VLSI Techniques for Analog and Digital Design*, Mcgraw-Hill, Singapoure (1990).

[18] Ho J. "An Overview of an 8bit 64msps ADC Design", Centre of Wireless Communications, June 2000.

[19] Razavi B. "Principles of Data Conversion System Design", IEEE press, 1995.

[20] Wooley B.A., Su D. "MOS D/A Converters", Course handout, Colombia Univ., New York, USA (Spring 2000).

[21] Wooley B.A., Su D. "Pipelined A/D Conversion", Course handout, Colombia Univ., New York, USA (Spring 2000).

[22] Wooley B.A., Zargari M., Limotyrakis S. "Folding and Interpolating A/D Conversion", Course handout, Colombia Univ., New York, USA (Spring 2000).

[23] Wooley B.A., Su D. "A/D Converter Architectures", Course handout, Colombia Univ., New York, USA (Spring 2000).

[24] Samavati H., Hajimin A., Shahani A.R., Nasserbaktt G.N., Lee T.H. Fractial Capacitors, Session FP 16, Stanford University, Stanford.

[25] Baumgartner R. Capacitive Circuit Architectures for Realization of Compact Ripple-Flash Analog-Digital Converters, Ph.D. Thesis, Worcester Polytechnic Institute (2001).

[26] Leblebici D. Genis Bandli, OTA Tabanli bir Kuvvetlendirici Uzerine Tartisma, Elektronik ve Haberlesme Muhendisligi Bolumu, İstanbul Teknik Universitesi (2000).

[27] Yotsuyanagi M., Etoh T., Hirata K. "A 10-b 50-MHz Pipelined CMOS A/D Converter with S/H", JSSC, vol.28, no.3, March 1993.

[28] Ahn G., Choi H., Lim S., Lee S.H., Lee C.D. "A 12-b, 10-MHz, 250-mW CMOS A/D Converter", JSSC, vol.31, no.12, Dec. 1996.

[29] Silveria F., Flandre D., Jespers P.G.A. " A g_m/ I_D Based Methodology for the Design of CMOS Analog Circuits and its Application to the Synthesis of a Silicon-on-Insulator Micropower OTA", JSSC, vol.31, no.9, Sept. 1996.

[30] Chen M.J., Gu Y.B., Wu T., Hsu P.C., Lin T.H. "Weak Inversion Charge Injection in Analog MOS Switches", JSSC, vol.30, no.5, May 1995.

[31] Shue B.J., Hu C. "Switch-Induced Error Voltage on a Switched Capacitor", JSSC, vol. SC-19, no.4, Aug. 1984.

[32] Yin M.J., OP't Eynde F., Sansen W. "A High-Speed CMOS Comparator with 8-b Resolution", JSSC, vol.27, no.2, Feb. 1992.

[33] Razavi B., Wooley B.A. "A 12-b 5-Msample/s Two-Step CMOS A/D Converter", JSSC, vol.27, no.12, Dec. 1992.

[34] Shih T., Der L., Lewis S.H., Hurst P. "A Fully Differential Comparator Using a Switched-Cpacitor Differencing Circuit with Common-Mode Rejection", JSSC, vol.32, no.2, Feb. 1997.

[35] Wu J.T., Wooley B.A. "A 100-MHz Pipelined CMOS Comparator", JSSC, vol.23, no.6, Dec. 1988.

[36] McCarroll B.J., Sodini C.G., Lee H.S. "A High-Speed CMOS Comparator for Use in an ADC", JSSC, vol.23, no.1, Feb. 1988.

[37] Dalton D., Spalding G., Rejyhani H., Murphy T., deevy K., Walsh M., Griffin P. "A 200-MSPS 6-Bit Flash ADC in 0.6 μm CMOS", IEEE Trans. On Circuits and Systems, vol.45, no.11, Nov. 1998.

[38] Choe M.J., Song B. S., Bacrania K. "A 13-b 40-Msample/s CMOS Pipelined Folding ADC with Background Offset trimming", JSSC, vol.35, no.12, Dec. 2000.

[39] Wang Y.T., Razavi B. "An 8-bit 150-MHz CMOS A/D Converter", JSSC, vol.35, no.3, March 2000.

[40] Van der Ploeg H., Remmers R. "A 3.3-V, 10-b, 25-Msample/s Two-Step ADC in 0.35 μm CMOS", JSSC, vol.34, no.12, Dec. 1999.

[41] Opris I.E., Wong B.C., Chin S.W. "A Pipeline A/D Converter Architecture with Low DNL", JSSC, vol.35, no.2, Feb. 2000.

[42] Abo A.M., Gray P.R. "A 1.5-V, 10-b, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter", JSSC, vol.34, no.5, My 1999.

[43] Nagaraj K., Martin D.A., Wolfe M., Chattopadhyay R., Pavan S., Cancio J., Viswanathan T.R. "A Dual-Mode 700-Msample/s 6-bit 200-Msamples/s 7-bit A/D Converter in a 0.25-μm Digital CMOS Pocess", JSSC, vol.35, no.12, Dec. 2000.

[44] Nakamura K., Hotta M., Carley L.R., Allstot D.J. "An 85 mW, 10 b, 40 Msample/s CMOS Parallel-Pipelined ADC", JSSC, vol.30, no.3, March 1995.

[45] Hadidi K., Vincent S., Temes G.C. "An 8-b 1.3-MHz Successive-Approximation A/D Converter", JSSC, vol.25, no.3, June 1990.

[46] Tsukamoto S., Schofield W., Endo T. "A CMOS 6-b, 400-Msample/s ADC wirh Error Correction", JSSC, vol.33, no.12, Dec. 1998.

[47] Flynn M.P., Sheahan B. "A 400-Msample/s, 6-b CMOS Folding and Interpolating ADC", JSSC, vol.33, no.12, Dec. 1998.

[48] Mercer D.A: "A 14-b 2.5 MSPS Pipelined ADC with On-Chip EPROM", JSSC, vol.31, no.1, Jan. 1996.

[49] Vorenkamp P., Roovers R. "A 12-b, 60-Msample/s Cascaded Folding and Interpolating ADC", JSSC, vol.32, no.12, Dec. 1997.

[50] Bult K., Buchwald A. "An Embedded 240-mW 10-b 50-MS/s CMOS ADC in 1 mm^2", JSSC, vol.32, no.12, Dec. 1997.

[51] Yotsuyanagi M., Hasegawa H., Yamaguchi M., Ishida M., Sone k. "A 2 V, 10 b, 20 Msample/s, Mixed-Mode Subranging A/D Converter", JSSC, vol.30, no.12, Dec. 1995.

[52] Song W., Choi H., Kwak S., Song B. "A 10-b 20-Msample/s Low-Power CMOS ADC", JSSC, vol.30, no.5, May 1995.

[53] Cho T., Gray P.R. "A 10 b, 20 Msample/s, 35 mW Pipeline A/D Converter", JSSC, vol.30, no.3, March 1995.

[54] Song B., Tompsett M., Lakshmikumar K.R. "A 12-bit 1-Msample/s Capacitor Error-Averaging Pipelined A/D Converter", JSSC, vol.23, no.6, Dec. 1988.

[55] Hosotani S., Miki T., Maeda A., Yazawa N. "An 8-bit 20-MS/s CMOS A/D Converter with 50-mW power Consumption", JSSC, vol.25, no.1, Feb. 1990.

[56] Lin Y., Kim B., Gray P.R. "A 13-b 2.5-MHz Self-Calibrated Pipelined A/D Converter in 3-μm CMOS", JSSC, vol.26, no.4, April 1991.

[57] Kim K.Y., Kusayanagi N., Abidi A.A. "A 10-b, 100-MS/s CMOS A/D Converter", JSSC, vol.32, no.3, March 1997.

[58] Moreland C., Murden F., Elliot M., Young J., Hensley M., Stop H. "A 14-bit 100-Msample/s Subranging ADC", JSSC, vol.35, no.12, Dec. 2000.

[59] Opris I., Wong B., Chin S. "A Pipeline A/D Converter Architecture with Low DNL", JSSC, vol.35, no.2, Feb. 2000.

[60] Lee S.H., Song B.S. "Digital-Domain Calibration of Multistep Analog-to-Digital Converters", JSSC, vol.27, no.12, Dec. 1992.

[61] Yu P.C., Lee H.S. "A 2.5-V, 12 b, 5-Msample/s Pipelined CMOS ADC", JSSC, vol.31, no.12, 1996.

[62] Hammerschmied C., huang Q. "Design and Implementation of an Untrimmed MOSFET-Only 10-Bit A/D Converter with –79-dB THD", JSSC, vol.33, no.8, Aug. 1998.

[63] Ingino J., Wooley B.A. "A Continously Calibrated 12-b, 10-MS/s, 3.3-v A/D Converter", JSSC, vol.33, no.12, Dec. 1998.

[64] Paul S.A., Lee H.S., Goddrich J., Alailima T., Santiago D. "A Nyquist-Rate Pipelined Oversampling A/D Converter", JSSC, vol.34, no.12, Dec. 1999.

[65] Mehr I., Singer L. "A 55-mW, 10 bit, 40-Msample/s Nyquist-Rate CMOS ADC", JSSC, vol.35, no.3, March 2000.

[66] Harjani R., Heineke R., Wang F. "An Integrated Low-Voltage Class AB CMOS OTA", JSSC, vol.34, no.2, feb. 1999.

[67] Palmisano G., Palumbo G., Salerno R. "A 1.5-V High Drive Capability CMOS Op-Amp", JSSC, vol.34, no.2, Feb. 1999.

[68] Reay R.J., Gregory T.A. "An Unconditionally Stable Two-Stage Amplifier", JSSC, vol.30, no.5, May 1995.

[69] Gulati K., Lee H.S. "A High-Swing CMOS Telescopic Operational Amplifier", JSSC, vol.33, no.12, Dec. 1998.

[70] Ferri G., Sansen W. "A Rail-to-Rail Constant-g_m Low-Voltage CMOS Operational Transconductance Amplifier", JSSC, vol.32, no.10, Oct. 1997.

[71] Razavi B. "A 200-MHz 15-mW BiCMOS Sample-and-Hold Amplifier with 3-V Supply", JSSC, vol.30, no.12, Dec. 1995.

BIBLIOGRAPHY

[1] Laker K.R., Sansen W. *Design of Analog Integrated Circuits ans Systems*, McGraw-Hill, (1994).

[2] Johns D., Martin K. *Analog Integrated Circuit Design*, John Wiley and Sons, Inc., Canada (1997).

[3] Allen P.E., Holberg D.R. *CMOS Analog Circuit Design*, Oxford, New York (1987).

[4] Razavi B. *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, (2000).

[5] Cherry J.A., Snelgrowe W.M. *Continous-Time Delta-Sigma Modulators for High-Speed A/D Conversion Theory, Practice and Fundamental Performance Limits*, Kluwer Academic Publishers (1999).

[6] Van de Plassche R. *Integrated Analog-to-Digital and Digital-to-Analog Converters*, Kluwer Acaademic Publishers, Dordrecht (1994).

[7] Horenstien M.N. *Microelectronic Circuits and Devices*, Prentice Hall, New Jersey (1996).

[8] Weste N.H.E., Eshraghian K. *Principles of CMOS VLSI Design, A System Perspective*, Addison-Weslet Publishing Company (1993).

[9] Leblebici D. *Analog Elektronik Devreleri*, İ.T.U. Rektorlugu, Istanbul (2000).

[10] Kang S., Leblebici Y. *CMOS Digital Integrated Circuits Analysis and Design*, McGraw-Hill (1996).

[11] Cilingiroglu U. *Systematic Analysis of Bipolar and MOS Transistors*, Artech House (1993).

[12] Hoeschele D.F. *Analog-to-Digital and Digital-to-Analog Conversion Techniques*, John Wiley & Sons, Canada (1994).

[13] Sedra A.S., Smith K.C. *Microelectronic Circuits*, Oxford, New York (1998).

[14] Geiger R.R., Allen P.E., Strader N.R. *VLSI Design Techniques for Analog and Digital Circuits*, McGraw-Hill (1990).

[15] Ismail M., Fiez T. *Analog VLSI Signal and Information Processing*, McGraw-Hill, Singapure (1994).

[16] Hastings A. *The Art of Analog Layout*, Prentice Hall, New Jersey (2001).

[17] Geiger R.L., Allen P.E., Strader N.R. *VLSI Techniques for Analog and Digital Design*, Mcgraw-Hill, Singapoure (1990).

[18] Ho J. "An Overview of an 8bit 64msps ADC Design", Centre of Wireless Communications, June 2000.

[19] Razavi B. "Principles of Data Conversion System Design", IEEE press, 1995.

[20] Wooley B.A., Su D. "MOS D/A Converters", Course handout, Colombia Univ., New York, USA (Spring 2000).

[21] Wooley B.A., Su D. "Pipelined A/D Conversion", Course handout, Colombia Univ., New York, USA (Spring 2000).

[22] Wooley B.A., Zargari M., Limotyrakis S. "Folding and Interpolating A/D Conversion", Course handout, Colombia Univ., New York, USA (Spring 2000).

[23] Wooley B.A., Su D. "A/D Converter Architectures", Course handout, Colombia Univ., New York, USA (Spring 2000).

[24] Samavati H., Hajimin A., Shahani A.R., Nasserbaktt G.N., Lee T.H. Fractial Capacitors, Session FP 16, Stanford University, Stanford.

[25] Baumgartner R. Capacitive Circuit Architectures for Realization of Compact Ripple-Flash Analog-Digital Converters, Ph.D. Thesis, Worcester Polytechnic Institute (2001).

[26] Leblebici D. Genis Bandli, OTA Tabanli bir Kuvvetlendirici Uzerine Tartisma, Elektronik ve Haberlesme Muhendisligi Bolumu, İstanbul Teknik Universitesi (2000).

[27] Yotsuyanagi M., Etoh T., Hirata K. "A 10-b 50-MHz Pipelined CMOS A/D Converter with S/H", JSSC, vol.28, no.3, March 1993.

[28] Ahn G., Choi H., Lim S., Lee S.H., Lee C.D. "A 12-b, 10-MHz, 250-mW CMOS A/D Converter", JSSC, vol.31, no.12, Dec. 1996.

[29] Silveria F., Flandre D., Jespers P.G.A. " A g_m/ I_D Based Methodology for the Design of CMOS Analog Circuits and its Application to the Synthesis of a Silicon-on-Insulator Micropower OTA", JSSC, vol.31, no.9, Sept. 1996.

[30] Chen M.J., Gu Y.B., Wu T., Hsu P.C., Lin T.H. "Weak Inversion Charge Injection in Analog MOS Switches", JSSC, vol.30, no.5, May 1995.

[31] Shue B.J., Hu C. "Switch-Induced Error Voltage on a Switched Capacitor", JSSC, vol. SC-19, no.4, Aug. 1984.

[32] Yin M.J., OP't Eynde F., Sansen W. "A High-Speed CMOS Comparator with 8-b Resolution", JSSC, vol.27, no.2, Feb. 1992.

[33] Razavi B., Wooley B.A. "A 12-b 5-Msample/s Two-Step CMOS A/D Converter", JSSC, vol.27, no.12, Dec. 1992.

[34] Shih T., Der L., Lewis S.H., Hurst P. "A Fully Differential Comparator Using a Switched-Cpacitor Differencing Circuit with Common-Mode Rejection", JSSC, vol.32, no.2, Feb. 1997.

[35] Wu J.T., Wooley B.A. "A 100-MHz Pipelined CMOS Comparator", JSSC, vol.23, no.6, Dec. 1988.

[36] McCarroll B.J., Sodini C.G., Lee H.S. "A High-Speed CMOS Comparator for Use in an ADC", JSSC, vol.23, no.1, Feb. 1988.

[37] Dalton D., Spalding G., Rejyhani H., Murphy T., deevy K., Walsh M., Griffin P. "A 200-MSPS 6-Bit Flash ADC in 0.6 μm CMOS", IEEE Trans. On Circuits and Systems, vol.45, no.11, Nov. 1998.

[38] Choe M.J., Song B. S., Bacrania K. "A 13-b 40-Msample/s CMOS Pipelined Folding ADC with Background Offset trimming", JSSC, vol.35, no.12, Dec. 2000.

[39] Wang Y.T., Razavi B. "An 8-bit 150-MHz CMOS A/D Converter", JSSC, vol.35, no.3, March 2000.

[40] Van der Ploeg H., Remmers R. "A 3.3-V, 10-b, 25-Msample/s Two-Step ADC in 0.35 μm CMOS", JSSC, vol.34, no.12, Dec. 1999.

[41] Opris I.E., Wong B.C., Chin S.W. "A Pipeline A/D Converter Architecture with Low DNL", JSSC, vol.35, no.2, Feb. 2000.

[42] Abo A.M., Gray P.R. "A 1.5-V, 10-b, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter", JSSC, vol.34, no.5, My 1999.

[43] Nagaraj K., Martin D.A., Wolfe M., Chattopadhyay R., Pavan S., Cancio J., Viswanathan T.R. "A Dual-Mode 700-Msample/s 6-bit 200-Msamples/s 7-bit A/D Converter in a 0.25-μm Digital CMOS Pocess", JSSC, vol.35, no.12, Dec. 2000.

[44] Nakamura K., Hotta M., Carley L.R., Allstot D.J. "An 85 mW, 10 b, 40 Msample/s CMOS Parallel-Pipelined ADC", JSSC, vol.30, no.3, March 1995.

[45] Hadidi K., Vincent S., Temes G.C. "An 8-b 1.3-MHz Successive-Approximation A/D Converter", JSSC, vol.25, no.3, June 1990.

[46] Tsukamoto S., Schofield W., Endo T. "A CMOS 6-b, 400-Msample/s ADC wirh Error Correction", JSSC, vol.33, no.12, Dec. 1998.

[47] Flynn M.P., Sheahan B. "A 400-Msample/s, 6-b CMOS Folding and Interpolating ADC", JSSC, vol.33, no.12, Dec. 1998.

[48] Mercer D.A: "A 14-b 2.5 MSPS Pipelined ADC with On-Chip EPROM", JSSC, vol.31, no.1, Jan. 1996.

[49] Vorenkamp P., Roovers R. "A 12-b, 60-Msample/s Cascaded Folding and Interpolating ADC", JSSC, vol.32, no.12, Dec. 1997.

[50] Bult K., Buchwald A. "An Embedded 240-mW 10-b 50-MS/s CMOS ADC in 1 mm^2", JSSC, vol.32, no.12, Dec. 1997.

[51] Yotsuyanagi M., Hasegawa H., Yamaguchi M., Ishida M., Sone k. "A 2 V, 10 b, 20 Msample/s, Mixed-Mode Subranging A/D Converter", JSSC, vol.30, no.12, Dec. 1995.

[52] Song W., Choi H., Kwak S., Song B. "A 10-b 20-Msample/s Low-Power CMOS ADC", JSSC, vol.30, no.5, May 1995.

[53] Cho T., Gray P.R. "A 10 b, 20 Msample/s, 35 mW Pipeline A/D Converter", JSSC, vol.30, no.3, March 1995.

[54] Song B., Tompsett M., Lakshmikumar K.R. "A 12-bit 1-Msample/s Capacitor Error-Averaging Pipelined A/D Converter", JSSC, vol.23, no.6, Dec. 1988.

[55] Hosotani S., Miki T., Maeda A., Yazawa N. "An 8-bit 20-MS/s CMOS A/D Converter with 50-mW power Consumption", JSSC, vol.25, no.1, Feb. 1990.

[56] Lin Y., Kim B., Gray P.R. "A 13-b 2.5-MHz Self-Calibrated Pipelined A/D Converter in 3-μm CMOS", JSSC, vol.26, no.4, April 1991.

[57] Kim K.Y., Kusayanagi N., Abidi A.A. "A 10-b, 100-MS/s CMOS A/D Converter", JSSC, vol.32, no.3, March 1997.

[58] Moreland C., Murden F., Elliot M., Young J., Hensley M., Stop H. "A 14-bit 100-Msample/s Subranging ADC", JSSC, vol.35, no.12, Dec. 2000.

[59] Opris I., Wong B., Chin S. "A Pipeline A/D Converter Architecture with Low DNL", JSSC, vol.35, no.2, Feb. 2000.

[60] Lee S.H., Song B.S. "Digital-Domain Calibration of Multistep Analog-to-Digital Converters", JSSC, vol.27, no.12, Dec. 1992.

[61] Yu P.C., Lee H.S. "A 2.5-V, 12 b, 5-Msample/s Pipelined CMOS ADC", JSSC, vol.31, no.12, 1996.

[62] Hammerschmied C., huang Q. "Design and Implementation of an Untrimmed MOSFET-Only 10-Bit A/D Converter with –79-dB THD", JSSC, vol.33, no.8, Aug. 1998.

[63] Ingino J., Wooley B.A. "A Continously Calibrated 12-b, 10-MS/s, 3.3-v A/D Converter", JSSC, vol.33, no.12, Dec. 1998.

[64] Paul S.A., Lee H.S., Goddrich J., Alailima T., Santiago D. "A Nyquist-Rate Pipelined Oversampling A/D Converter", JSSC, vol.34, no.12, Dec. 1999.

[65] Mehr I., Singer L. "A 55-mW, 10 bit, 40-Msample/s Nyquist-Rate CMOS ADC", JSSC, vol.35, no.3, March 2000.

[66] Harjani R., Heineke R., Wang F. "An Integrated Low-Voltage Class AB CMOS OTA", JSSC, vol.34, no.2, feb. 1999.

[67] Palmisano G., Palumbo G., Salerno R. "A 1.5-V High Drive Capability CMOS Op-Amp", JSSC, vol.34, no.2, Feb. 1999.

[68] Reay R.J., Gregory T.A. "An Unconditionally Stable Two-Stage Amplifier", JSSC, vol.30, no.5, May 1995.

[69] Gulati K., Lee H.S. "A High-Swing CMOS Telescopic Operational Amplifier", JSSC, vol.33, no.12, Dec. 1998.

[70] Ferri G., Sansen W. "A Rail-to-Rail Constant-g_m Low-Voltage CMOS Operational Transconductance Amplifier", JSSC, vol.32, no.10, Oct. 1997.

[71] Razavi B. "A 200-MHz 15-mW BiCMOS Sample-and-Hold Amplifier with 3-V Supply", JSSC, vol.30, no.12, Dec. 1995.