Design and Simulation of Micro Resonator Oscillator for Communication Circuits

by

Mustafa Parlak

Submitted to the Graduate School of Engineering and Natural Sciences
in partial fulfillment of
the requirements for the degree of
Master of Science

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APPROVED BY

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Abstract

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Integration of MEMS structure with Complementary Metal Oxide Semiconductor (CMOS) electronics is another motivation and driving force of this study. Therefore completely monolithic high-Q micromechanical oscillator integrated with CMOS circuits is aimed and described. As it has high Q (over 80.000) and very stable, laterally driven microresonators can be a good miniaturized replacement of a crystal and surface acoustic wave (SAW) resonator based oscillators used in telecommunication applications. The electrical model of the microresonator is given and used as a frequency selective network in the oscillator design. Different oscillator circuits are designed and simulated to estimate and compare their performance to other mechanical based oscillators (SAW, FBAR, Crystal etc.). Analog CMOS integraated circuits are designed and optimized to achieve highly stable oscillations.

Haberleşme Devreleri için Mikro Rezonatör Osilatörlerin Tasarımı ve Simülasyonu

Özet

Bu tez MikroelektroMekanik sistem (MEMS) bazlı osilatörün tasarımını ve simlasyonunu sunar. Elektrostatik olarak etkileşebilen tarak benzeri (Mikro Rezonatör) bir MEMS yapısı osilatörün yapı taşı olarak kullanıldı. Bu tezin konusu olan mikro rezonatör gibi MEMS bazlı titreşen yapılar işaret işleme uygulamalarında kullanılabilecek aletlerdir. Osilatör yapımında Mikro Rezonatörün kullanılmasının seçimi MEMS bazlı yapıların havasız ortamda yüksek kalite faktörüne (Yüksek-Q) sahip olmasından kaynaklanmaktadır. Yüksek kararlı osilatörler Mikro Rezonatörler kullanılarak yapılabilmekte ve 16 kHz'de çalışan örnekleri gösterilmiştir. Fakat bu osilatörlerin taşınabilir haberleşme devrelerinde kullanılabilmesi için çalışma frekansının en azından IF bandına ($>$ 455 kHz) çıkartılması gerekmektedir. Bu tezde MEMS bazlı osilatörlerin simulasyonu yapıldı ve fiziksel boyutlarında yapılan uygun değişikliklerle istenilen frekans aralığında çalışması sağlandı. Mikro Rezonatörün elektriksel eşdeğer devreleri ve belirleyici matematiksel denklemleri incelendi. Elde edilen bu sonuçlar kullanılarak MEMS bazlı, 500 kHz'de çalışan bir osilatör tasarlandı. Bu calişmalar hem Mikro Rezonatörün eşdeğer devresi hem de matematiksel denklemleri kullanılarak yapıldı.

Bu çalışmanın yapılmasındaki diğer bir amaç MEMS yapılarının kolaylıkla CMOS elektronik devreleriyle entegre olabilme özelliğidir. Dolayısıyla tamamıyla aynı çip üzerinde gerçeklenmiş MEMS tabanlı osilatörler amaç olarak seçilmiştir. Yüksek kalite faktörüne sahip olan MEMS yapıları şu anda haberleşme devrelerinde kullanılan kristal ve yüzey akustik dalga (SAW) rezonatörlerinin yerine kullanabilecek bir kapasiteye sahiptir. Bu tezde Mikro Rezonatörün elektriksel modeli osilatörde frekans belirleyici devre olarak kullanıldı. Değişik osilatörler dizayn edildi ve rezonatör performansları diğer mekanik (SAW, kristal) rezonatörlerle karşılaştırıldı. Osilatör devresi gerçeklenirken daha karalı salınım sağlayabilmesi için çeşitli CMOS analog devreleri tasarlandı ve optimize edildi.

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Chapter 1

Introduction

Oscillator circuits are widely used in communication circuits and instrumentation applications. Oscillators can be broadly classified into two groups: relaxation oscillators and harmonic oscillators. A relaxation oscillator tends to have poor phase noise characteristic and high harmonic content. A harmonic oscillator is capable of producing a near sinusoidal signal with good phase noise and high spectral purity. Harmonic oscillators usually use LC resonant circuits, crystals, or SAW resonators for defining the oscillation frequency.

Most of the high performance oscillators employ discrete components to meet many of the specifications for the functions required for communication technology. Using discrete components brings many disadvantages to communication circuits. First of all they are expensive and need to be integrated. But practically there are presently no integrated transistor- based filters or oscillators that can even match the performance of those based upon SAW resonators and Quartz crystals.

Integration is important not only for economic purposes but also in terms of size and power. These two are actually very much related when considering battery-operated wireless components. Although integration is necessary, product can not be made compact unless it consumes low enough power to allow the use of small batteries. Therefore replacing the off-chip components (quartz, crystals, ceramic filters, SAW resonators) with monolithically integrated versions, fabricated using the planar integrated circuit processing techniques of both CMOS and surface micromachining is crucial for many aspects mentioned above.

Mechanical elements are generally utilized as transducers when used in sensors. For example, an accelerometer uses a mechanical proof mass to sense acceleration

in the mechanical domain and transduce it to voltage or charge in the electrical domain. If the accelerometer in question were a resonant accelerometer, then the quality factor of both the material and design would be a very important parameter. It is well known that the quality factor of mechanical resonators is generally orders of magnitude higher than achievable by discrete or integrated LCR tank circuits. For this reason, many of the high-Q filters and local oscillators required in communication systems are implemented using off-chip macroscopic mechanical components, which interface with the integrated amplifying and discriminating electronics on the board level. The use of off-chip components, although relatively inexpensive, makes production of such communications products cumbersome and prevents the realization of a truly compact product. Many study [2] has been done on this subject to solve the mentioned problems.

there is a great incentive to replace high-Q macroscopic (off-chip) elements with integrated versions, since this could potentially lead to a fully monolithic, batch fabricated transmitter or receiver systems. This theses aims to investigate the possibility of replacing the crystal, ceramic and SAW components currently used in today's communications equipment with equivalent miniaturized and integrable micromechanical versions.

To get an idea of which components are replaceable we refer to Fig 1.1 which presents the simplified block diagram of a heterodyne receiver used in mobile communication systems. As it can be seen from the figure, off-chip components occupies 80% of the cellular phone board.

The target components which can potentially be replaced by micromechanics, then, include all off-chip high-Q components used in the IF amplifier, the local oscillator, and perhaps the RF filter (if micromechanical resonators can reach such frequencies) [5]. Whether such components are replaceable by micromechanics depends upon the specifications of the system and on the material and design properties of the micromechanical elements, in particular the quality factor. For example, poly silicon microresonator has Q in the range of over 30.000 at 30 MHz suggest that the broadcast FM receiver is feasible using micromachining technologies to replace off-chip components.

Once the off-chip components are miniaturized, a technology which then merges

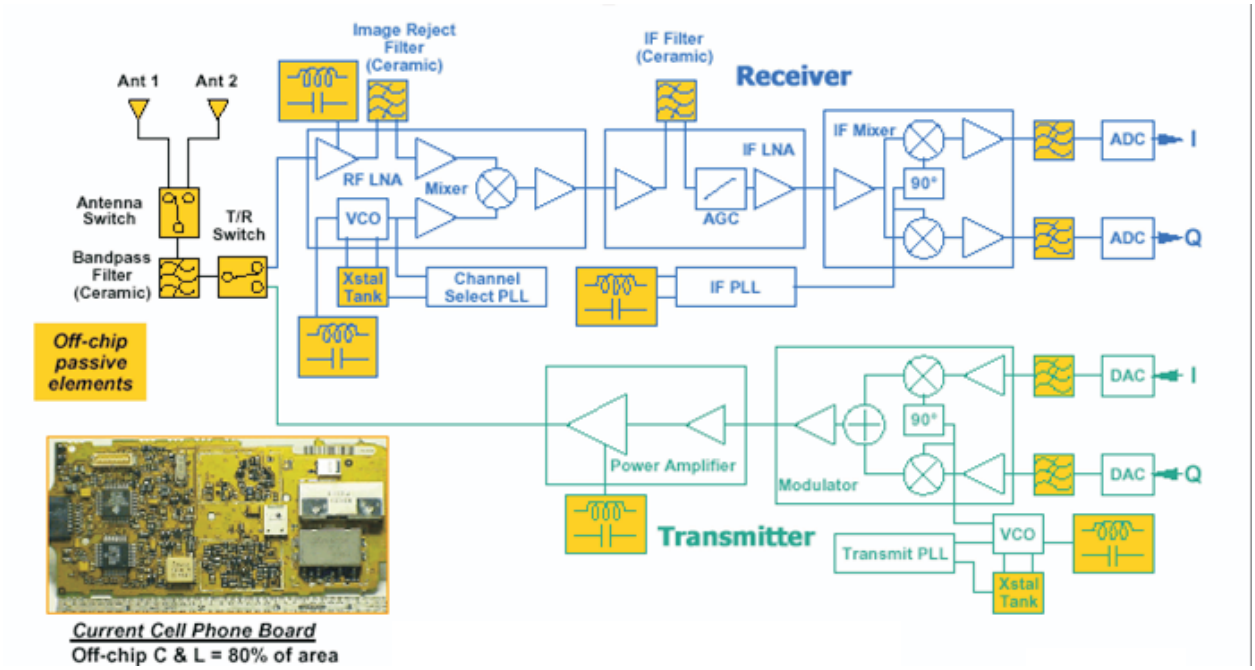


Figure 1.1: Block diagram of a heterodyne receiver used in cellular phones and mobile communication systems

these devices with amplifying and discriminating electronics is all that is required to realize a fully monolithic receiver or transmitter.

1.1 Important Resonator Properties

Macroscopic mechanical resonators are extremely popular in the communications industry due to three basic properties: an extremely high quality factor, low temperature coefficient, and a very low aging rate. They are also quite inexpensive in large quantities. In addition, the electromechanical transduction mechanism and geometric vibration characteristics of quartz crystals make them easy to design with. For example, the low series resistance in the equivalent motional circuit for an AT-cut quartz crystal makes the design of sustaining amplifiers in oscillators much simpler, and it allows the design of crystal or mechanical filters much simpler in terms of filter termination. These are some of the properties that are desirable in the miniaturized integrated circuit mechanical resonators.

1.2 State-of-the-art Resonators

There are number of different types of resonators available to used in communication circuits. The most common ones are, Surface Acoustic Wave (SAW), LC, Crystal, Film Bulk Acoustic Resonator (FBAR) and MEMS resonator. SAW resonators are used in receiver front ends, fiber optic clock recovery, inductorless oscillators, VCOs etc. LC resonators is effective at low frequencies, since they have a great design and simulation flexibility and virtually no frequency limitation. Their sizes are substantially smaller than the other mechanical resonators. They can be integrated with ASICs. But LC resonators has poor quality factor at high frequencies. Crystal resonators are made of piezoelectric crystal, such as quartz, and exhibits electromechanical-resonance characteristics that are very stable (with time and temperature) and highly selective (having very high Q factors). They operate well until several hundred MHz. A basic FBAR device consists of a piezoelectric layer (ZnO) sandwiched between two electrodes above a via in a wafer. When a RF signal is applied across the device it produces a mechanical motion in the piezoelectric layer. The fundamental resonance is observed when the thickness of the film is equivalent to half the wavelength of the input signal. Currently ZnO is used as the piezoelectric material, however other materials such as AlN can also be used [1].

Tabular comparison of resonators is in the Table 1.2 [12].

Table 1.1: Comparison of some of the resonator technologies

	MEMS	SAW	Quartz	FBAR	LC
Operation Principle	Capacitive	Piezoelectric	Piezoelectric	Piezoelectric	Electric
Quality Factor (Q)	500 (air)	1500	100000	1000	30-80
Frequency Range	$<$ 100 MHz	50 MHz - 2 GHz	50 kHz several 100 MHz	10 MHz - 10 GHz	¡ 5 GHz
Typical Size	50 $\mu m\times$ 50 μm	1 cm $\times$ 1 cm	0.13 $\times$ 0.08 $\times$ 0.13 mm^2	100 $\mu m\times$ 50 μm	$\sim$ 100 $\mu m\times$ 50 μm
Integration with IC	$\surd$	$\times$	$\times$	$\surd$	$\surd$
Materials	Silicon, Metals	$LiTaO_3, LiNbO_3$, Quartz	$LiTaO_3$	AlN, ZnO	Silicon

Chapter 2

Design of MEMS resonator and its fabrication

In the past decade, the application of bulk and surface micromachining techniques greatly stimulated research in micromechanical structures and devices. Advancement in this field are motivated by potential applications in batch-fabricated integrated sensors and silicon microactuators.

MicroElctroMechanical (MEM) vibrating structures such as linear drive resonators can be used as driving components in signal processing applications. The applications are targeted for front-end transceivers and include oscillators and filters [4]- [8]. These devices promise new capabilities, as well as improved performance-to-cost ratio over conventional hybrid sensors. Micromachined transducers that can be fabricated compatibly with an integrated circuit process are the building blocks for integrated microsystems. Furthermore, miniaturized transducers are powerful tools for research in the micron-sized domain in the physical, chemical and biomedical fields.

Integrated-sensor research is rigorously pursued because of the broad demand for low-cost, high-precision, and miniature replacements for existing hybrid sensors. In particular, resonant sensors are attractive for precision measurements because of their high sensitivity to physical or chemical parameters. These devices utilize the high sensitivity of the frequency of a mechanical resonator to physical or chemical parameters that affect its potential or kinetic vibrational energy. Electrostatic excitation combined with capacitive (electrostatic) detection is an attractive approach for silicon microstructures because of simplicity and compatibility with micromachining technology [14]. Figure 2 shows the layout of a linear resonant structure which can be driven electrostatically from one side and sensed capacitively at the

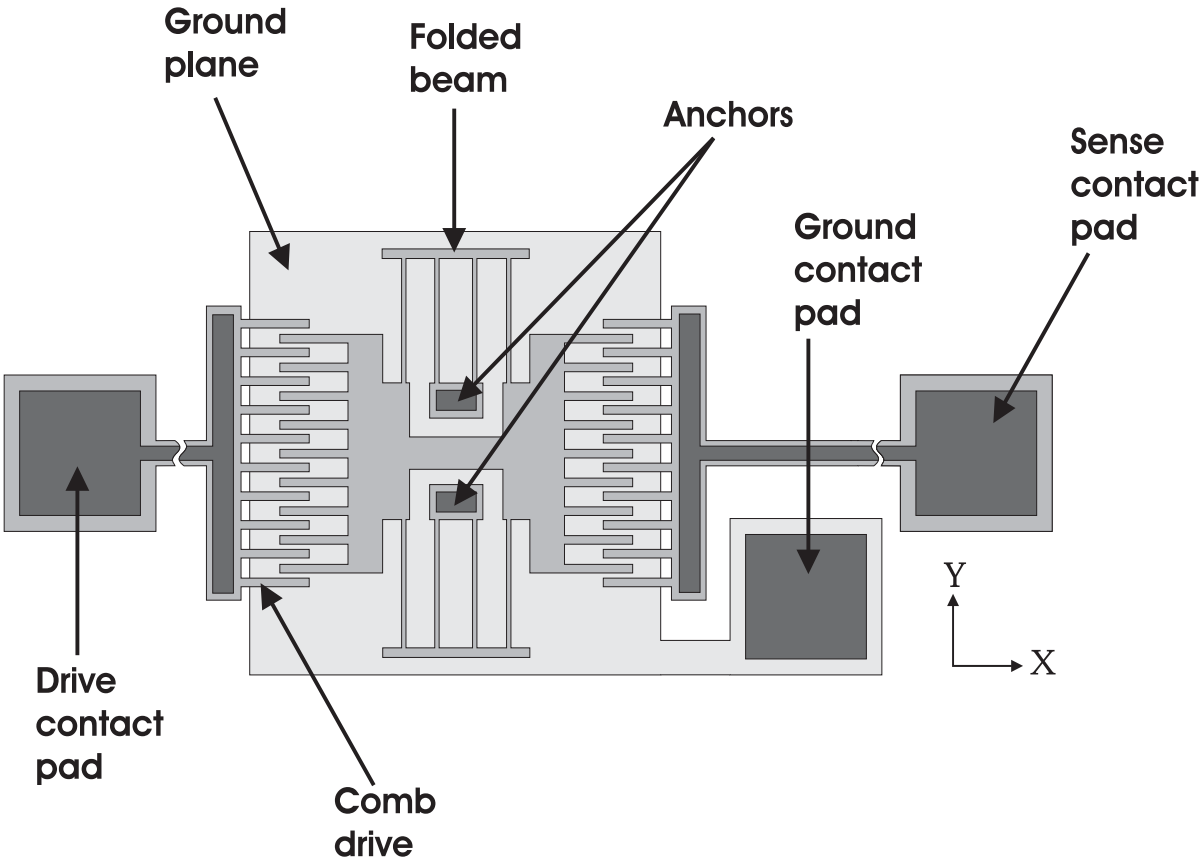


Figure 2.1: Layout of a linear lateral resonator

other side with interdigitated finger (comb) structures. Alternatively, the structure can be driven differentially (push-pull) using the two combs, with the motion sensed by the impedance shift at resonance [14].

The electrostatic comb structure can be used either as a derive or a sense element. The induced driving force and the output sensitivity are both proportional to the variation of the comb capacitance C with the lateral displacement x of the structure, $\partial C/\partial x$. A key feature of the electrostatic comb derive is that $\partial C/\partial x$ is a constant independent of the displacement Δx, as long as Δx is less than the overlap We can model the capacitance between the movable comb fingers and the stationary fingers as a parallel combination of two capacitors, one due to the fringing fields, C_f, and the other due to the normal fields, C_n. By considering the electric filed distribution difference between before and after the displacement of the finger as shown in Figure 2, it becomes obvious that C_f is independent of the displacement, Δx, while C_n is linearly proportional to Δx.

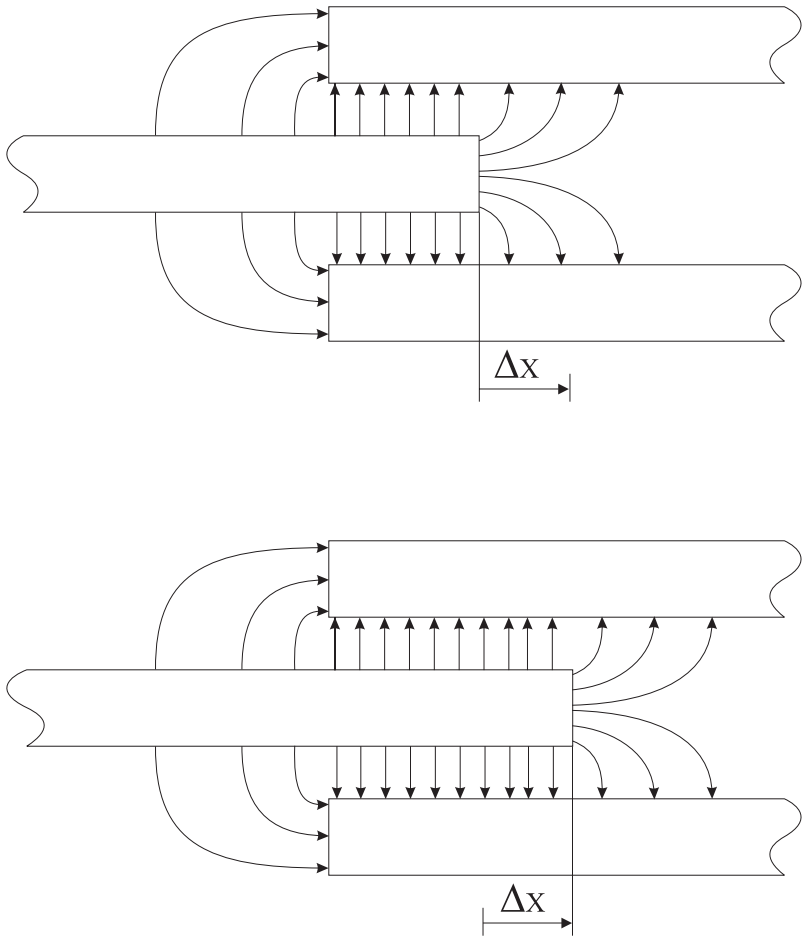


Figure 2.2: Electric Field distribution before and after the movable finger displaces by Δx into the slot

2.1 Transfer Function

In analyzing the electromechanical transfer function, we consider the resonator is driven electrostatically with the comb structure from one side and sensed capacitively at the other side as illustrated in Figure 2.1.

At the drive port, the induced electrostatic force in the x direction, F_x is found by Tang [14] and given by

$$F_x = \frac{1}{2}\frac{\partial C}{\partial x}v_D^2 \tag{2.1}$$

where v_D is the derive voltage across the structure and stationary drive electrode. For a drive voltage $v_D(t) = V_P + v_d sin(\omega t)$, where V_P is the DC bias at the derive port and v_d is the AC drive amplitude, Equation 2.1 becomes

$$F_x = \frac{1}{2}\frac{\partial C}{\partial x}[V_P^2 + \frac{1}{2}v_d^2 + 2V_P v_d sin(\omega t) - \frac{1}{2}v_d^2 cos(2\omega t)] \tag{2.2}$$

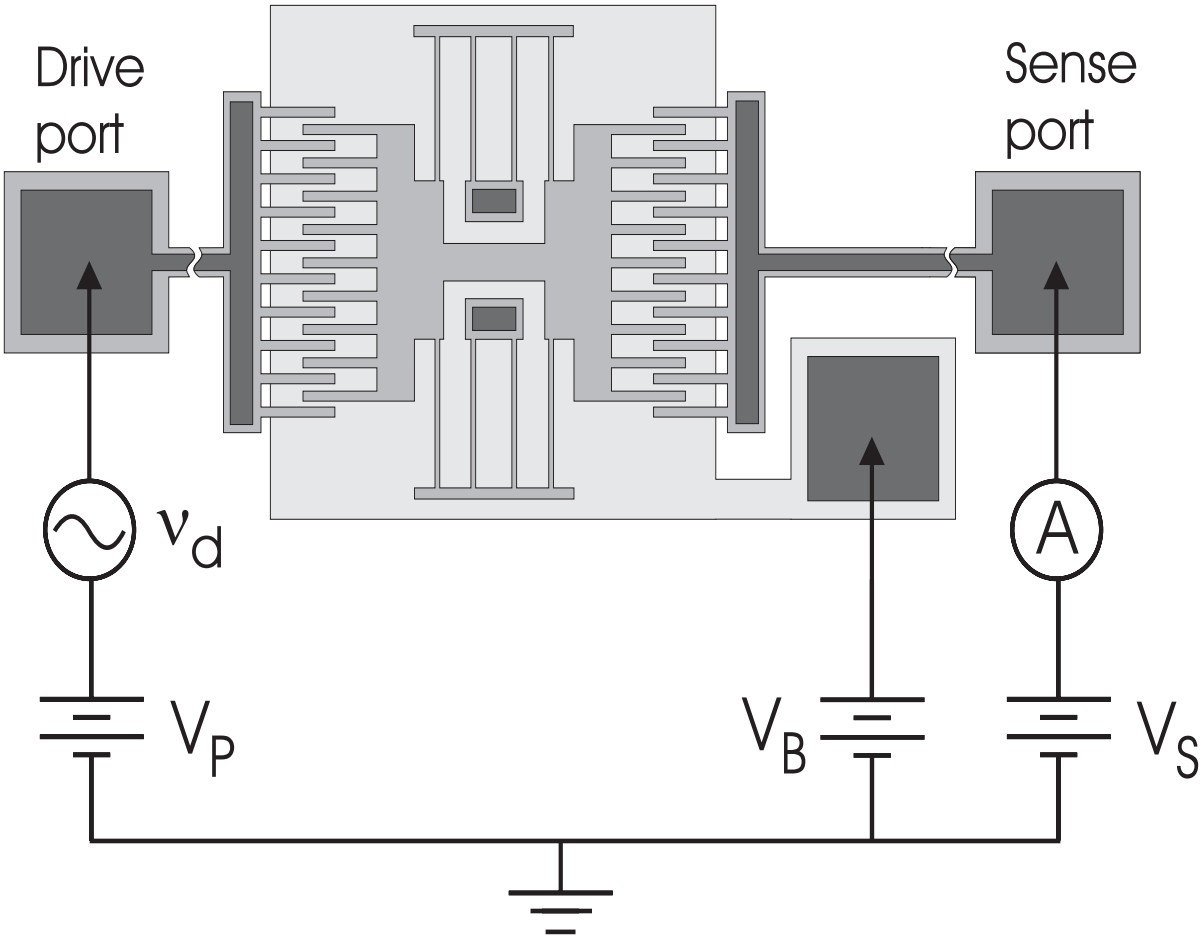


Figure 2.3: A linear resonator electrostatically driven from one side and sensed capacitively at the other side

Given the system spring constant in the x direction, k_x, and a damping factor, c, the equation of the motion is a second-order-differential equation given by

$$Mx'' + cx' + k_x x = F_x(t) \tag{2.3}$$

where M is the effective mass of the structure. Therefore after tedious calculations the steady state response x is a simple harmonic function given by

$$x(t) = \frac{2(\partial C/\partial x)V_P v_d}{\sqrt{(k_x - M\omega^2)^2 + c^2\omega^2}} sin(\omega t - \phi_1) \tag{2.4}$$

the motion is sensed by detecting the short-circuit current through the time varying comb capacitor with a dc bias. At the sense port, harmonic motion of the structure results in a sense current, i_s, which is given by

$$i_s = V_S \frac{\partial C}{\partial x}\frac{\partial x}{\partial t} \tag{2.5}$$

where V_S is the bias voltage between the structure and the stationary sense electrode.

2.2 Mechanical Analysis

The design criteria for lateral resonator are two. First, the suspensions should provide freedom of travel along the direction of the comb-finger motions (x), while restraining the structure from moving sideways (y) to prevent the comb fingers from shorting to the drive electrodes. Therefore, the spring constant along the y direction must be much higher than that along the x direction, i.e., $k_y \gg k_x$. Second, the suspensions should allow for the relief of the built-in stress of the structural poly silicon film as well as axial stress induced by large vibrational amplitudes. Folded beam suspension design fulfills these two criteria. This design allows large deflection in the x direction (perpendicular to the length of the beams) while providing stiffness in the y direction (along the length of the beams). Furthermore, the only anchor points for the whole structure are near the center, thus allowing the parallel beams to expand or contract in the y direction, relieving most of the built-in stress.

Spring constant in the x direction is with the resonant plate is statically displaced by a distance X_0 under an applied force F_x in the positive x direction is given below. Each of the beams has a length L, width w, and thickness h.

$$k_x = \frac{F_x}{X_0} = \frac{24EI_z}{L^3} \tag{2.6}$$

where I_z is the moment of inertia with respect to the z axis and E is Young's modulus. For an ideal beam with rectangular cross section having a width w and a thickness h, the moment of inertia is

$$I_z = \frac{hW^3}{12} \tag{2.7}$$

2.2.1 Lateral Resonant Frequency

Using Rayleigh's energy method

$$K.E._{\cdot max} = P.E._{\cdot max} \tag{2.8}$$

and a mass of calculation as did by tang et all we can reach resonant frequency formula as in Equation 2.9 where $K.E._{\cdot max}$ is the maximum kinetic energy during a

vibration cycle, and $P.E._{max}$ is the maximum potential energy.

$$\omega = (\frac{k_x}{M_p + \frac{1}{4}M_t + \frac{12}{35}M_b})^{\frac{1}{2}} \tag{2.9}$$

The denominator on the right-hand side of this equation can be lumped together as the effective mass of the system, M

$$M = M_p + \frac{1}{4}M_t + \frac{12}{35}M_b \tag{2.10}$$

such that

$$\omega = (\frac{k_x}{M})^{\frac{1}{2}} \tag{2.11}$$

Substituting the Equations 2.7 and 2.6 in the above resonance frequency formula and more elegant and playing a little bit denominator more instructive and useful expression can be obtained as below [11].

$$f_r = \frac{1}{2\pi}[\frac{2Eh(\frac{W}{L})^3}{M_p + 0.3714M}]^{\frac{1}{2}} \tag{2.12}$$

where M_p and M are the masses of the plate and of the supporting beams respectively.

2.2.2 Quality Factor

One of the advantages of laterally driven resonant structures is that the damping in the lateral direction is much lower than in vertical direction. Therefore when operated in air, undesired vertical motions are conveniently damped. There are a number of dissipative processes during lateral motion, all of them affecting the quality factor Q. The dominant influences include Coutte flow underneath the plate, air drag on the top surface, damping in the comb gaps and direct air resistance related to the thickness of the structure [11]. If we consider Coutte flow alone, then we can estimate the quality factor Q as

$$Q = \frac{d}{\mu A_p}\sqrt{Mk_x} \tag{2.13}$$

where $\mu$is the absolute viscosity of air, d is the offset between the plate and the substrate, and M is the effective mass of the resonator. when resonated in vacuum, vibrational energy is mostly dissipated to the substrate through the anchors, or polysilicon structure itself.

2.3 MicroResonator Fabrication

The fabrication process for the electrostatic-comb drives and associated lateral structures is a straightforward application of the surface-micromachining technology. The structures are fabricated with six-mask process illustrated in Figure 2.3. A significant advantage of this technology is that all the critical features are defined with one mask, eliminating errors due mask-to-mask misalignment. The process begins with metal deposition onto silicon wafer using teknoplasma sputter system, which defines DC plane of the microresonator. After this SiO_2 deposited on top of the metal layer. Then contact windows to the metal layer opened using wet etching. The next steps involve the deposition of the second metal layer and patterning with Karl- Suss mask aligner. Sacrificial PSG layer deposited and patterned for dimple formation and anchor openings. Poly silicon structural layer is then deposited on top of the patterned PSG layer. After stripping the PSG layer the final microresonator structure is formed.

2.4 Small Signal Equivalent Circuits for Micromechanical Resonators

The equivalent circuit describing microresonator performance under AC electrostatic excitation can be derived through consideration of the electromechanical transduction mechanism and the details of resonator construction (i.e. geometry and structural material) [2]. For two port microresonator we can think of the whole system as a black box. Its behaviour as seen by its port can be modeled as a series RLC circuit. Nguyen found small signal model of the resonator in his theses [13]. where C_{o1} is the total DC capacitance (i.e. the value of capacitance for a motionless shuttle), Q is the quality factor, k is the system spring constant and V_P is the voltage difference between input comb drive and shuttle. Corresponding C_x, L_x, R_x values

are

$$C_x = \frac{[V_P \frac{\partial C}{\partial x}]^2}{k} \tag{2.14}$$

$$L_x = \frac{k}{\omega_r^2 [V_P \frac{\partial C}{\partial x}]^2} \tag{2.15}$$

$$R_x = \frac{k}{\omega_r^2 Q [V_P \frac{\partial C}{\partial x}]^2} \tag{2.16}$$

$$\frac{\partial C}{\partial x} \approx \frac{\xi N \epsilon_0 h}{d} \tag{2.17}$$

where h is the shuttle finger thickness, d is the gap between electrode and resonator fingers, and N is the number of finger gaps. ξ is a constant that models additional capacitance due to fringing electric fields. As it is seen from the formulas, the model parameters are strictly depend on the dimensions (Beam length/width, DC bias voltage, number of finger overlaps N, gap spacings between fingers etc.) and construction of the resonator. Therefore dimensions of the resonator must be carefully chosen to obtain desired results. Figure 2.4 shows all the critical dimensions of the comb drive that effects the resonance frequency, spring constant, model parameters, etc.

The resonance frequency of this micromechanical resonator is determined largely by W/L ratio of the folded beams. Therefore, by decreasing the length L of the beam and by keeping the other parameters in Equation 2.12 constant, the resonance frequency is tuned to the desired value. The variables as presented in Table 2.4 above, define critical parameters along with their values used in this study. The resonance frequency can be verified by using combined information of Table 2.4 and Equation 2.12.

2.5 Summary

In this chapter we have discussed basic operation principles and electrostatic characteristics of microresonator. Resonance frequency, Quality factor, important device dimensions were given. Small signal equivalent circuit of the microresonator is created in order to model the device and to make it ready for simulation in the electrical domain. Furthermore we have described the poly silicon surface-micromachining techniques for fabricating the laterally-driven microstructures.

Table 2.1: Critical dimensions of 459 kHz microresonator used in the design of oscillator

	Parameter	Value
E	Young's modulus	150 GPa
μ	Absolute viscosity of air	$17.46x10^{-6}Ns/m^2$
H	Structure thickness	2 μm
W	Beam width	2 μm
L	Beam length	$25\mu m$
M	Mass (beam + truss)	1.791110^{-12} Kg
M_P	Shuttle mass	$3.4333x10^{-11}$ Kg
k_{sys}	System spring constant	303.543 N/m
Q	Quality factor	1250.22
f_r	Resonance frequency	459.017 kHz

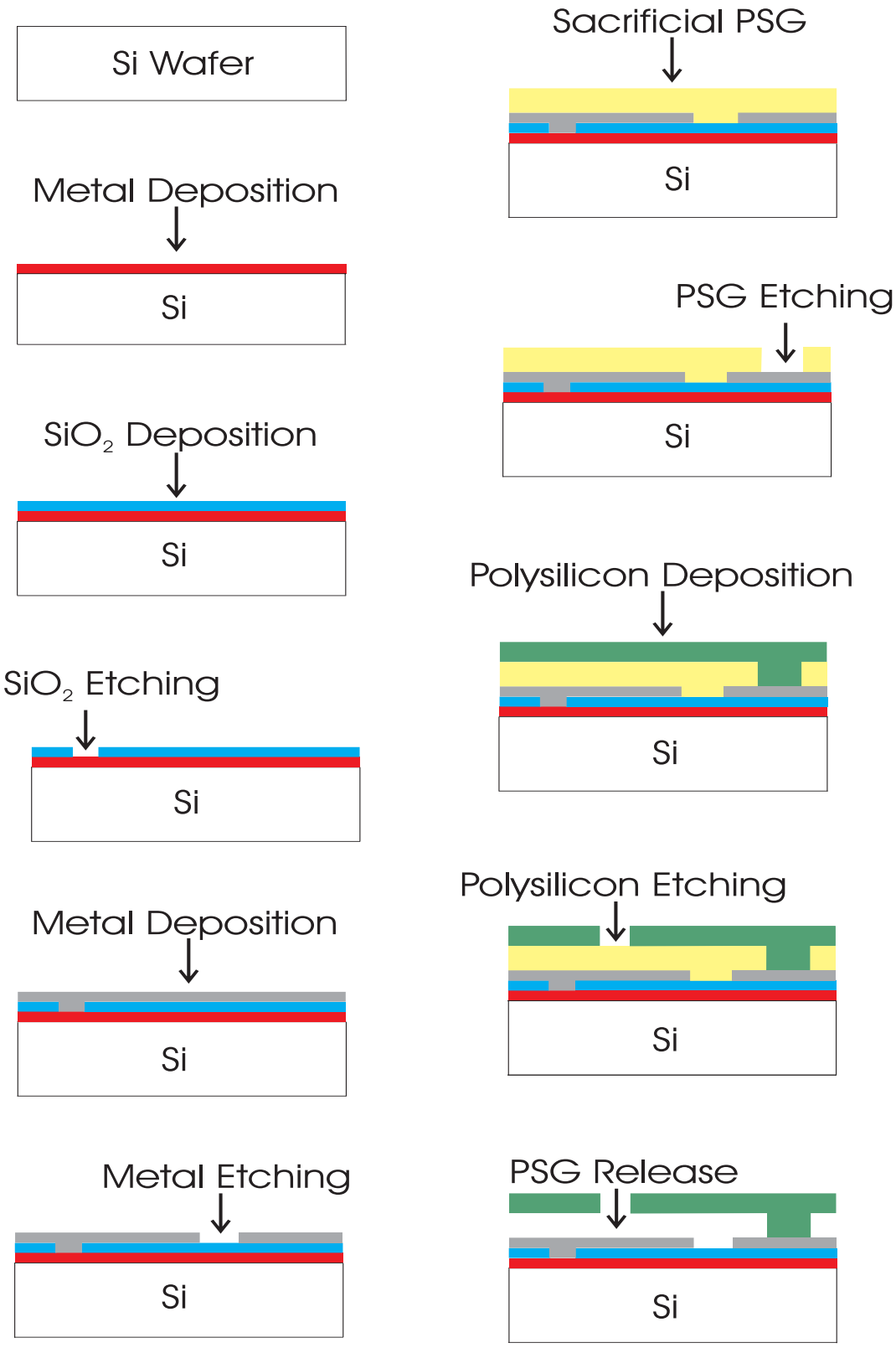


Figure 2.4: Process Sequence of the Micro resonator

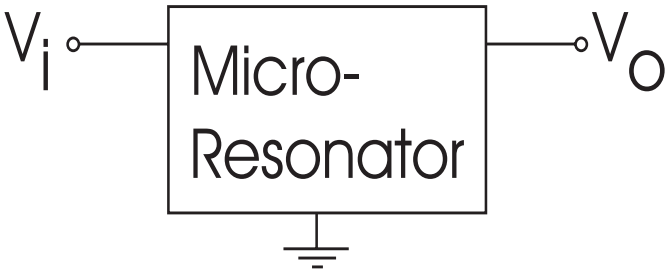


Figure 2.5: Block representation of the microresonator

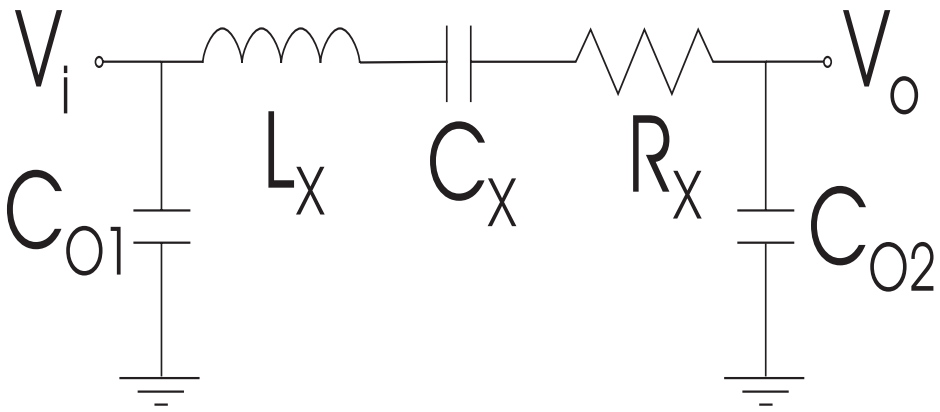


Figure 2.6: Equivalent circuit model of the microresonator

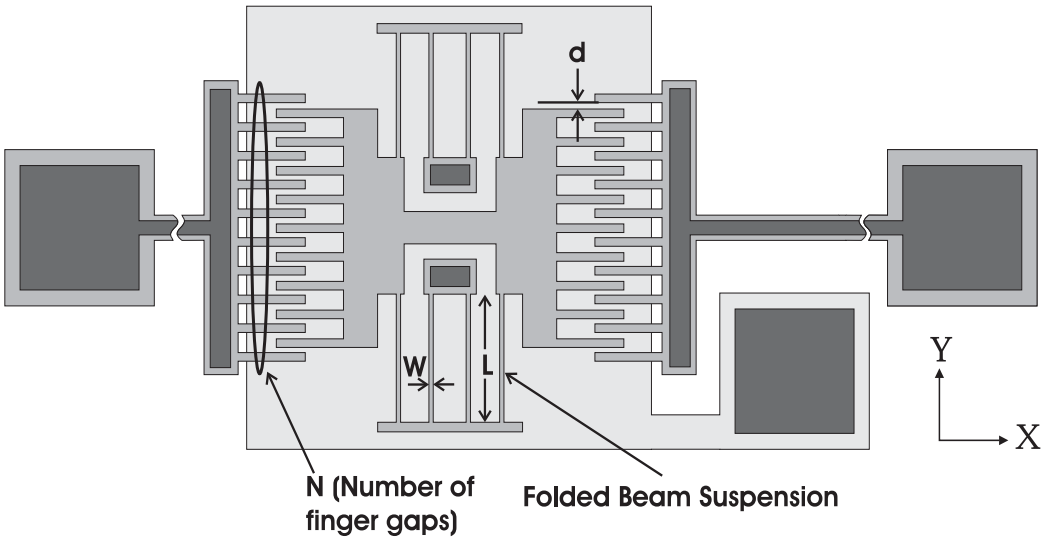


Figure 2.7: Critical Dimensions of a comb drive

Chapter 3

Design of CMOS Analog Integrated Circuits for MEMS Oscillator

This chapter concentrates on the design of analog integrated circuits. Op-amps and their performance characteristics are the main subject of this chapter. ICs are designed using AMS 0.35μ [26] CMOS technology. Two different op-amp architectures are applied namely, 1. Basic two stage op-amp 2. Folded cascode op-amp.

Oscillators need a sustaining amplifier to ensure oscillation. Amplifiers used in oscillators must be stable and broad band. High gain is the another attribute to construct a high quality oscillators. Therefore, amplifier design specifically op-amp design is a key issue when dealing with oscillators. There has been many research done on improving performance of the op-amps. These include increasing gain, broadening bandwidth and constructing more stable op-amps [19]- [23]. Before going to optimizing op-amp characteristics, It is useful to give some details about op-amps.

3.1 Two Stage CMOS Op-amp

Currently, the most widely used circuit approach for implementation of MOS operational amplifiers is the two-stage configuration shown in Figure 3.1. This circuit configuration provides good common mode range, output swing, voltage gain, and CMRR in a simple circuit that can be compensated with a single pole-splitting capacitor [27]. In this section, we will analyze the various performance parameters of the CMOS implementation of this circuit.

First stage of two stage op-amp is simple differential pair, therefore, it is instructive to begin with it. The Differential input stage consists of M_1, M_2, M_3, and M_4,

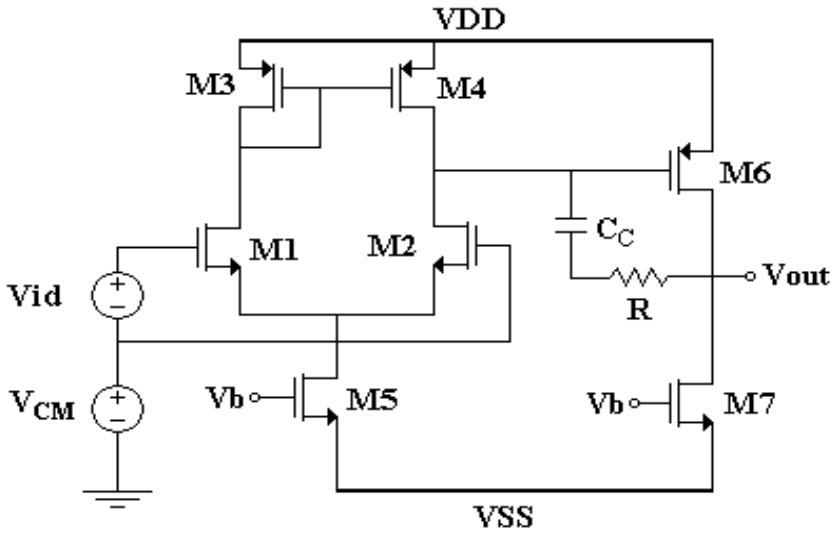


Figure 3.1: Simplified basic two stage Op-amp

with M_1 matching M_2 and M_3 matching M_4 as shown in Figure 3.2. The small signal analysis of the differential input stage can be accomplished with the assistance of the model shown in Figure 3.1 which is only appropriate for differential analysis when both sides of the amplifier are assumed to be perfectly matched. If this condition is satisfied, then the point where the two sources of M_1 and M_2 are connected can be considered at AC ground.

$$C_1 \approx C_{gd1} + C_{gs3} + C_{gs4} \tag{3.1}$$

$$C_2 \approx C_{gd2} \tag{3.2}$$

$$C_3 \approx C_{gd4} \tag{3.3}$$

Therefore, the small signal gain of the differential pair is simply

$$V_{out}/V_{id} = g_m(r_{o2} \parallel r_{o4}) \tag{3.4}$$

$$g_m(r_{o2} \parallel r_{o4}) \approx \frac{1}{\lambda I_{SS}} \tag{3.5}$$

$$g_m = \sqrt{k'(W/L)I_{SS}} \tag{3.6}$$

$$A_v = \frac{V_{out}}{V_{id}} = \sqrt{k'}\sqrt{\frac{W_{1,2}}{L_{1,2}I_{SS}}}(\frac{1}{\lambda}) \tag{3.7}$$

The expression of gain illustrates several key aspects of MOS devices used as analog amplifiers. First, for constant drain current decreasing either the channel length or

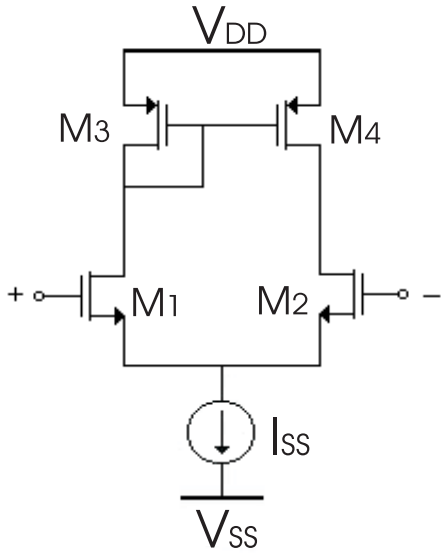


Figure 3.2: MOS differential pair

width results in a decrease in the gain. This fact, along with noise considerations, usually dictates the minimum size of the transistors that must be used in a given high-gain amplifier application. Usually, this is larger than the length and width used for digital circuits in the same technology. Second, if the device geometry is kept constant, the voltage gain is inversely proportional to the square root of the drain current [27]. To summarize, k' is a constant, uncontrollable by the designer and the effect of λ on the gain diminishes as L increases, such that $1/\lambda$ is directly

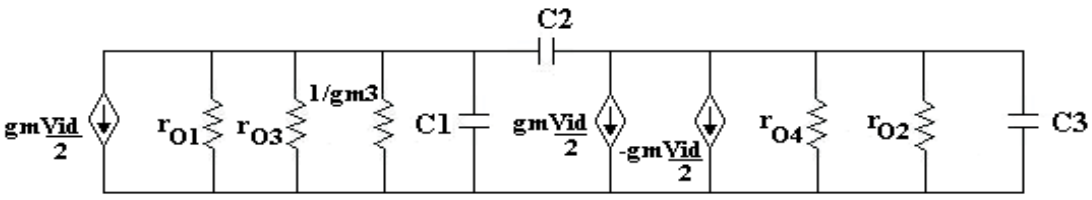


Figure 3.3: The simplified equivalent model of differential pair

proportional to the channel length. Then proportionality can be established between $W_{1,2}/L_{1,2}$ and the drain current versus the small signal gain such that:

$$A_v \propto \sqrt{\frac{W_{1,2}}{L_{1,2} I_{SS}}} \tag{3.8}$$

Conclusions:

- Increasing $W_{1,2}, L_{1,2}$ or both increases the gain
- Decreasing the drain current through M_1 and M_2 increases the gain.

3.1.1 The Frequency Response, Compensation

Operational amplifier architectures are generally of two types: single-stage externally compensated or two stage internally compensated amplifiers, both of which can have a dominant two pole type frequency response [28]. Ignoring higher order poles, the small signal behaviour of the two stage amplifier can be modeled by the general two pole, one zero small signal equivalent circuit shown in Figure 3.7. Referring back to the model of the input stage Figure 3.1, we will work to find poles of the system. We have two poles these are

$$p_1 = \frac{1}{C_1 \dfrac{1}{g_{m3}}} \tag{3.9}$$

$$p_2 = \frac{1}{C_2(r_{o2} \parallel r_{o4})} \tag{3.10}$$

Since $p_1 \gg p_2$ we can approximate gain as

$$A_v = g_m(r_{o2} \parallel r_{o4}) \frac{1}{1 + \dfrac{s}{C_2(r_{o2} \parallel r_{o4})}} \tag{3.11}$$

The compensation of the two stage CMOS amplifier can be carried out using a pole splitting capacitor. The goal of the compensation task is to achieve a phase margin greater than 45°. The circuit can be approximately represented by the small-signal equivalent circuit of Figure 3.7 if the nondominant poles which may exist on the circuit are neglected.

The overall transfer function that results from the addition of C_C is [29].

$$\frac{V_{o(s)}}{V_{in(s)}} = \frac{g_{m1} g_{m2} R_1 R_2 (1 - sC_C/g_{m2})}{1 + s[R_1(C_1 + C_C) + R_2(C_2 + C_C) + g_{m2} R_1 R_2 C_C] + s^2 R_1 R_2 [C_1 C_2 + C_C(C_1 + C_2)]} \tag{3.12}$$

The circuit displays two poles and a right half plane zero, which under the assumption that the poles are widely separated, can be shown to be approximately located at

$$p_1 = \frac{-1}{(1+g_{m2}R_2)C_C R_1} \tag{3.13}$$

$$p_2 = \frac{-g_{m2}C_C}{C_2C_1 + C_2C_C + C_CC_1} \tag{3.14}$$

$$z = \frac{g_{m2}}{C_C} \tag{3.15}$$

Note that the pole due to the capacitive loading of the first stage by the second, p_1, has been pushed down to a very low frequency by the miller effect in the second stage, while the pole due to the capacitance at the output node of the second stage, p_2, has been pushed to a very high frequency due to the shunt feedback. For this reason, the compensation technique is called pole splitting.

Physically, the zero arises because the compensation capacitor provides a path for the signal to propagate directly through the circuit to the output at high frequencies. Since there is no inversion in that signal path as there is in the inverting path dominant at low frequencies, stability degraded. Fortunately two effective means have evolved for eliminating the effect of the right half-plane zero. One approach has been to insert a source follower in the path from the output back through the compensation capacitor. An even simpler approach is to insert a nulling resistor in series with the compensation capacitor as shown in Figure 3.4. Using an analysis

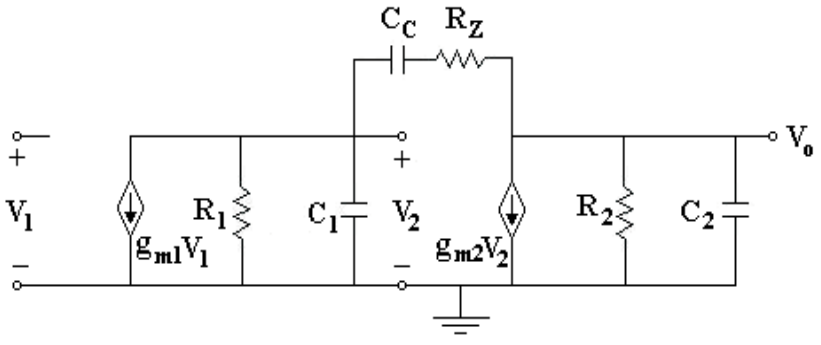


Figure 3.4: Simplified small signal model of the basic two stage Op-amp added with the nulling resistor

similar to that performed for the circuit of Figure 3.7, one obtains pole locations which are close to those for the original circuit, and a zero. This circuit has the

fallowing node-voltage equations.

$$g_{m1}V_{in} + \frac{V_2}{R_1} + sC_1V_2 + (\frac{sC_C}{1+sC_CR_Z})(V_2 - V_O) = 0 \tag{3.16}$$

$$g_{m2}V_2 + \frac{V_O}{R_2} + sC_2V_O + (\frac{sC_C}{1+sC_CR_Z})(V_O - V_2) = 0 \tag{3.17}$$

These equations can be solved to give

$$\frac{V_{o(s)}}{V_{in(s)}} = \frac{a\{1 - s[(C_C/g_{m2}) - R_ZC_C]\}}{1 + bs + cs^2 + ds^3} \tag{3.18}$$

where

$$a = g_{m1}g_{m2}R_1R_2 \tag{3.19}$$

$$b = R_2(C_2 + C_C) + R_1(C_1 + C_C) + g_{m2}R_1R_2C_C + R_ZC_C \tag{3.20}$$

$$c = [R_1R_2(C_1C_2 + C_CC_1 + C_CC_2) + R_ZC_C(R_1C_1 + R_2C_2)] \tag{3.21}$$

$$d = R_1R_2R_ZC_1C_2C_C \tag{3.22}$$

If R_Z is assumed to be less than R_1 or R_2 and the poles are widely spaced, then the roots of the above equation can be approximated as

$$p_1 = \frac{-1}{(1+g_{m2}R_2)C_CR_1} \cong \frac{-1}{g_{m2}R_2R_1C_C} \tag{3.23}$$

$$p_2 = \frac{-g_{m2}C_C}{C_2C_1 + C_2C_C + C_CC_1} \cong \frac{-g_{m2}}{C_2} \tag{3.24}$$

$$p_3 = \frac{-1}{R_ZC_1} \tag{3.25}$$

and

$$z = \frac{-1}{C_C(\frac{1}{g_{m2} - R_Z})} \tag{3.26}$$

The resistor R_Z allows independent control over the placement of the zero. The zero vanishes when R_Z is made equal to $1/g_{m2}$. In fact, the resistor can be further increased to move the zero into the left half-plane and place it on top of p_2 to improve the amplifier phase margin. R_Z can be realized by a MOS transistor in the triode region. The value of R_Z can be found as

$$R_Z = (\frac{C_2 + C_C}{C_C})\frac{1}{g_{m2}} \tag{3.27}$$

3.1.2 Open Circuit Voltage Gain

The voltage gain of the first stage was found (differential pair) in previous section to be given by

$$A_1 = -g_{m1}(r_{o2} \parallel r_{o4}) \tag{3.28}$$

where g_{m1} is the transconductance of each of the first stage that is M_1 and M_2. The second stage is an actively loaded common-source amplifier whose voltage gain is given by

$$A_2 = -g_{m6}(r_{o6} \parallel r_{o7}) \tag{3.29}$$

The dc open loop gain of the op amp is the product of A_1 and A_2.

$$A = g_{m1}g_{m6}(r_{o2} \parallel r_{o4})(r_{o6} \parallel r_{o7}) \tag{3.30}$$

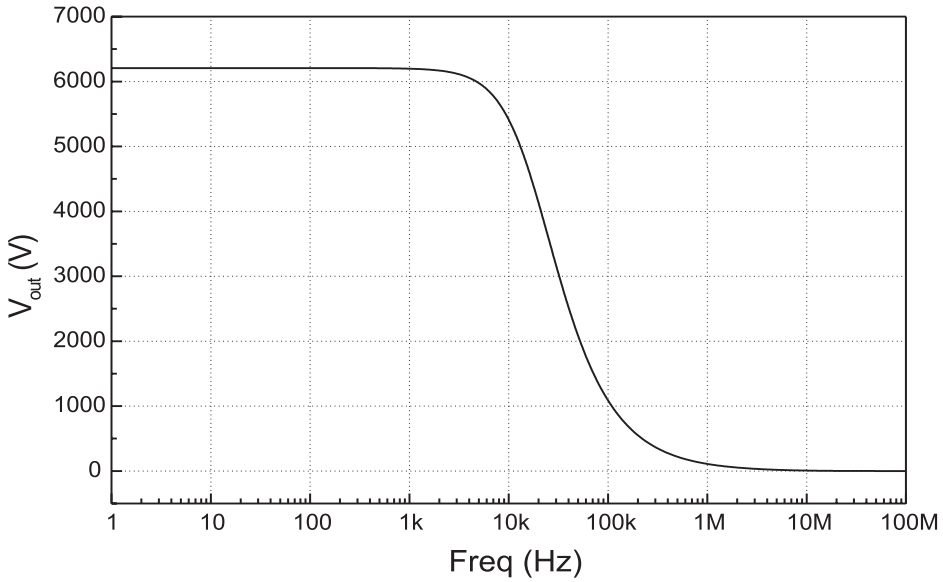


Figure 3.5: AC Frequency Simulation of the Op-Amp. DC gain of this Op-Amp is more than 6000 V/V.

3.1.3 DC Offsets, DC Biasing

In MOS op amps, because of the relatively low gain per stage, the offset voltage of the differential to single-ended converter and the second stage can play an important role. In Figure 3.7, the operational amplifier has been split into two separate stages.

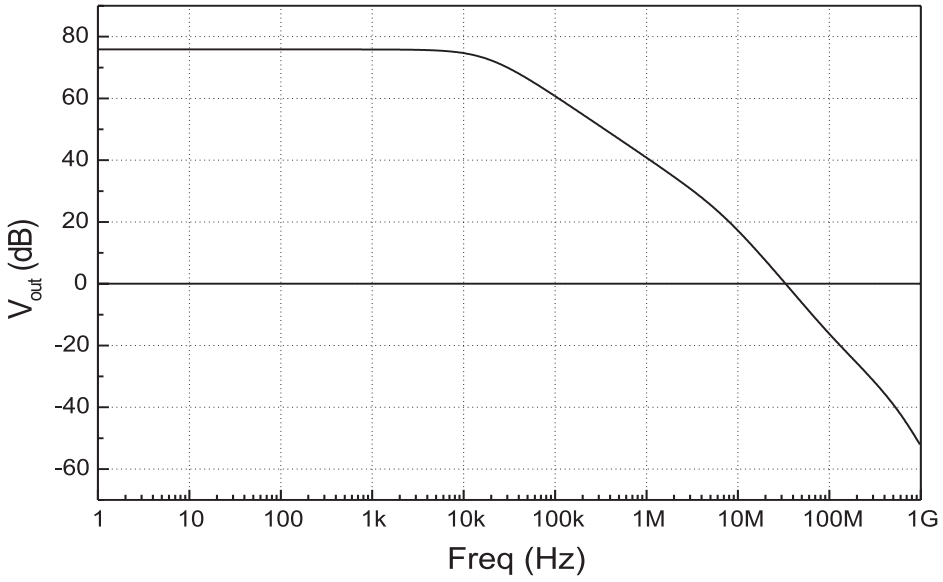


Figure 3.6: AC Frequency Response in terms of dB. DC gain is 75 dB

Assuming perfectly matched devices, if the inputs of the first stage are grounded, then the quiescent output voltage at the drain of M_4 is equal to the voltage at the drain of M_3 (M_3 and M_4 have the same drain current and gate-source voltage, and hence must have the same drain-source voltage). However, the value of the gate voltage of M_6 which is required to force the amplifier output voltage to zero may be different from the quiescent output voltage of the first stage. For a first stage gain of 50, for example, each 50 mV difference in these voltages results in 1 mV of input-referred systematic offset. Thus, the W/L ratios of M_3, M_4, and M_6 must be chosen so that the current densities in these three devices are equal. For the simple circuit of Figure 3.1 this constraint would take the form

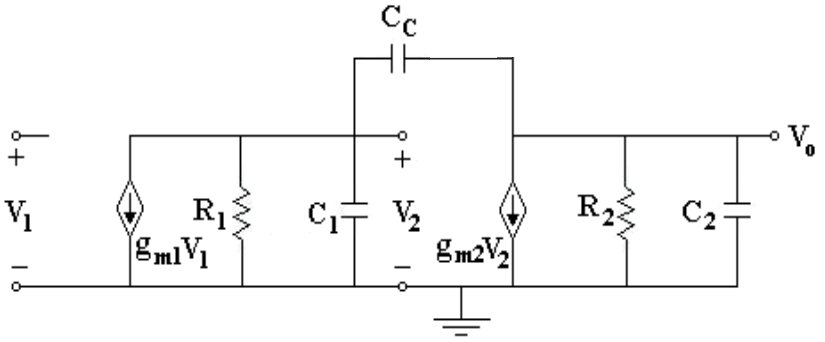


Figure 3.7: Simplified small signal model of the basic two stage Op-amp

$$\frac{(W/L)_3}{(W/L)_6} = \frac{(W/L)_4}{(W/L)_6} = \frac{1}{2}\frac{(W/L)_5}{(W/L)_7} \tag{3.31}$$

Systematic offset voltage is closely correlated with dc power supply rejection ratio. If a systematic offsets exists, it is likely to display dependence on power supply voltage, particularly if the bias reference source is such that the bias currents in the amplifier are not supply independent. Figure 3.8 shows input offset voltage of the basic two stage op-amp of our interest. Figure 3.9 shows input common mode range and output swing of the same circuit.

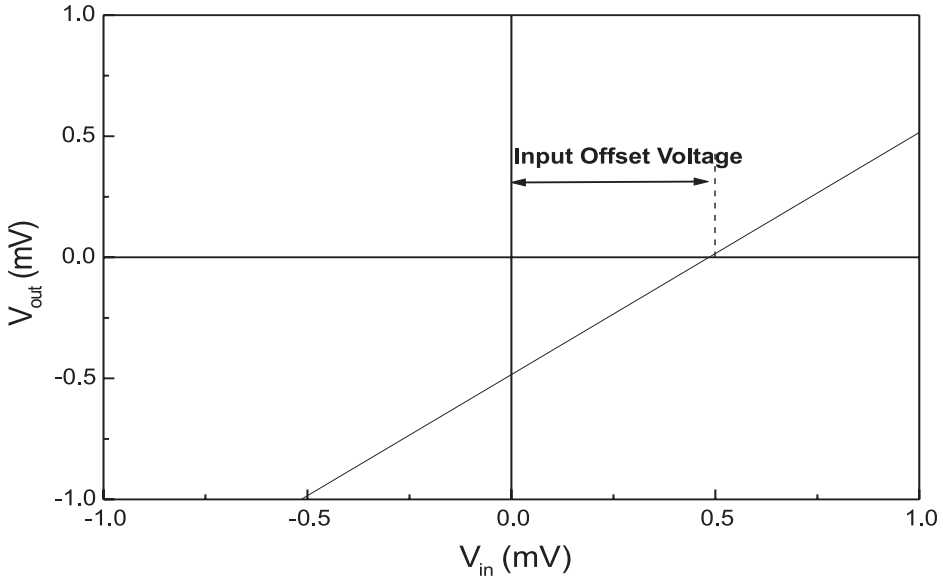


Figure 3.8: Simulation results showing the Input Offset voltage (484.6 μV in this circuit)

3.1.4 Slew Rate

The rate of change of output voltage dVo/dt in response of a large step input is called slew rate and is usually specified in $V/\mu s$. Consider the circuit Figure 3.10and input step for testing the slew-rate performance. At t = 0, the input voltage steps to +5 V, but the output voltage cannot respond instantaneously and is initially zero. Thus the op-amp differential input is $V_{id} = 5V$, which drives the input stage completely out of its linear range of operation. This can be seen by considering a two-stage op-amp, simplified schematics for CMOS op amp used in this analysis shown in Figure 3.11. The Miller compensation capacitor C connects around the

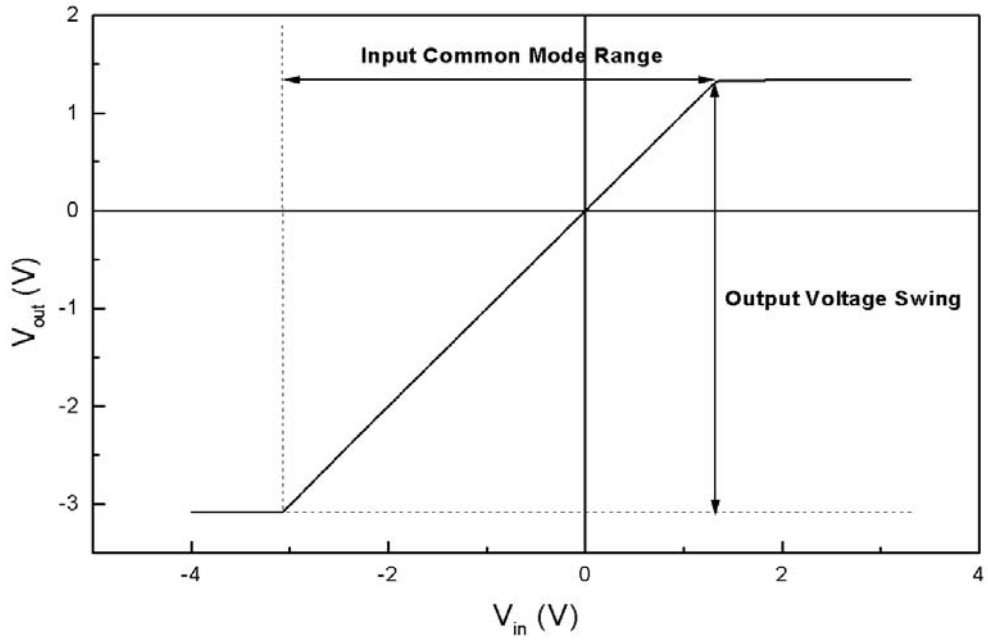


Figure 3.9: Simulation results showing the ICMR and output swing

high-gain second stage and causes this stage to act as an integrator. The large-signal transfer characteristic from the op-amp differential input voltage V_{id} to I_X is that of a differential pair, the maximum current available to charge C is $2I_1$, which is the tail current in the input stage. Consider a large input voltage applied to the circuit of Figure 3.11 so that $I_X = 2I_1$. Then the second stage acts as an integrator with an input current $2I_1$, and output voltage V_O can be written as

$$V_O = \frac{1}{C}\int 2I_1 dt \tag{3.32}$$

and thus

$$\frac{dV_O}{dt} = \frac{2I_1}{C} \tag{3.33}$$

3.1.5 Power Dissipation

wer dissipation is a complex function of the technology used and particular requirements of the application. In sampled data systems such as switched capacitor filters, the requirement is that the amplifier be able to settle in a certain time to a certain frequency with a capacitive load of several Pico farads. In this application, the

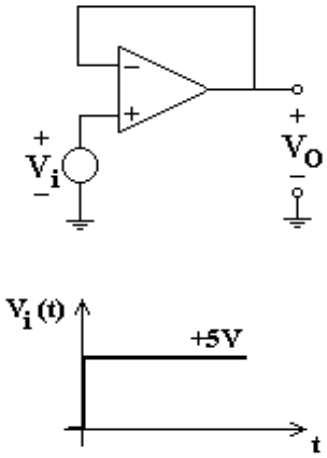


Figure 3.10: Circuit for testing slew-rate performance

factors determining the minimum power dissipation tend to be the fact that there must be enough be standing current in the amplifier class A second stage such that the capacitance can be charged in the allowed time, and the fact that the amplifier must have sufficient phase margin to avoid degradation of the settling time due to the ringing and overshoot. The latter requirement dictates a certain minimum g_m in the transistor M_6 for a given bandwidth and load capacitor. This, in turn usually dictates a certain minimum bias current in M_6 for a reasonable device size. If a class A source follower output stage is added, then the same comment would apply to its bias current since its gm together with the load capacitance, contribute a nondominant pole.

The preceding discussion is predicted on the use of class A circuitry (i.e. circuits whose available output current is not greater than the quiescent bias current). Quiescent power dissipation can be greatly reduced through the use of dynamic circuits and class B circuits.

3.1.6 Noise Performance

Average power of the noise is predictable and can be measured or simulated [30]. It is customary to express average power in V^2 rather than W. In analogy with deterministic signals we can also define a root-mean-square (rms) voltage for noise. The concept of average power proves essential in noise analysis and must be defined carefully. The concept of average power becomes more versatile if defined with

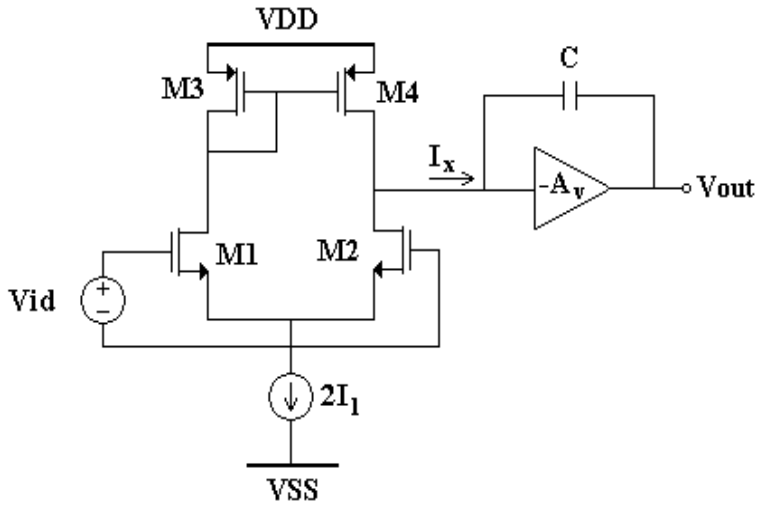


Figure 3.11: Simplified schematic of a two-stage MOS op-amp for slew rate calculations

regard to the frequency content of noise. The spectrum shows how much power the signal carries at each frequency. For example $5nV/\sqrt{Hz}$ at 100 MHz, simply means the average power in a 1Hz bandwidth at 100 MHz is equal to $(5x10^{-9})^2V^2$. Because of the fact that MOS devices display relatively high 1/f noise, the noise performance is an important design consideration in MOS amplifiers. All four transistors in the input stage contribute to the equivalent input noise. By simply calculating the output noise for each circuit and equating them,

$$V_{eqTOT}^2 = V_{eq1}^2 + V_{eq2}^2 + \frac{g_{m3}}{g_{m1}}(V_{eq1}^2 + V_{eq2}^2) \tag{3.34}$$

where it has been assumed that $g_{m1} = g_{m2}$ and that $g_{m3} = g_{m4}$.

Thus, the input transistors contribute to the input noise directly, while the contribution of the loads is reduced by the square of the ratio of their transconductance to that of the input transistors. The significance of this in the design can be further appreciated by considering the input-referred 1/f noise and the input-referred thermal noise separately. Figure 3.12 shows output noise spectrum of basic two stage op-amp of this work.

3.1.7 DC Power Supply Rejection

Power supply rejection ratio (PSSR) is a parameter of considerable importance in MOS amplifier design. One reason for this is that in complex analog-digital systems,

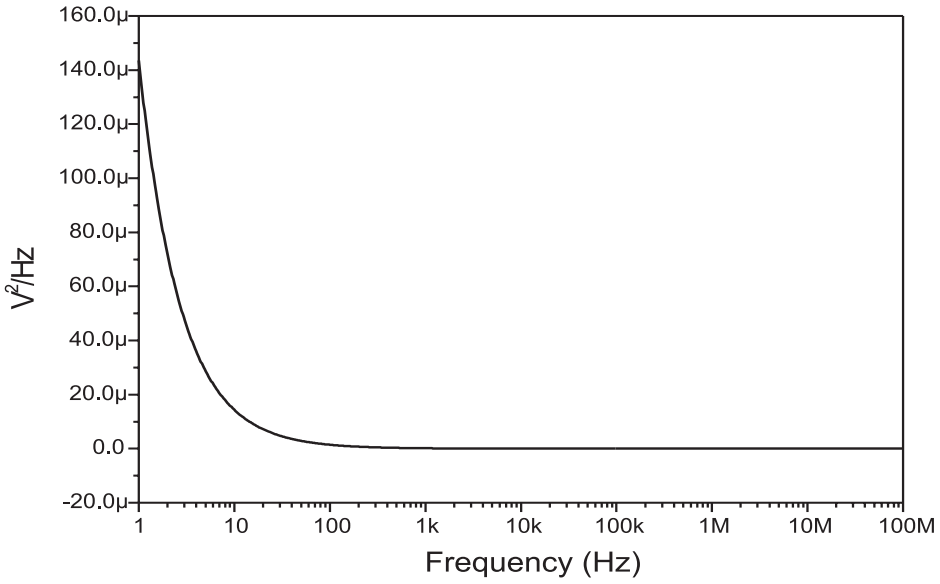


Figure 3.12: Output noise spectrum of the two stage op-amp

the analog circuitry must coexist on the same chip with large amounts of digital circuitry. Even though separate analog and digital supply buses are often run on chip, it is hard to avoid some coupling of digital noise into analog supplies. A second reason is that in many systems, switching regulators are used which introduce power supply noise into the supply voltage lines. If these high-frequency signals couple into the signal path in a sampled data system such as a switched capacitor filter or high speed A/D converter, they can be aliased down into the frequency band where the signal resides and degrades the overall system signal-to-noise ratio. The parameters reflecting susceptibility to this phenomenon in the operational amplifier are the high-frequency PSRR and the supply capacitance.

The PSRR of an operational amplifier is simply the ratio of the voltage gain from the input to the output (open loop) to that from the supply to the output. It can be easily demonstrated that for frequencies less than the unity gain-frequency, if the operational amplifier is connected in a follower configuration and an ac signal is superimposed on one of the power supplies, the signal appearing at the output is equal to applied signal divided by the PSRR for that supply. Figure 3.1.7, 3.1.7 shows the simulated results.

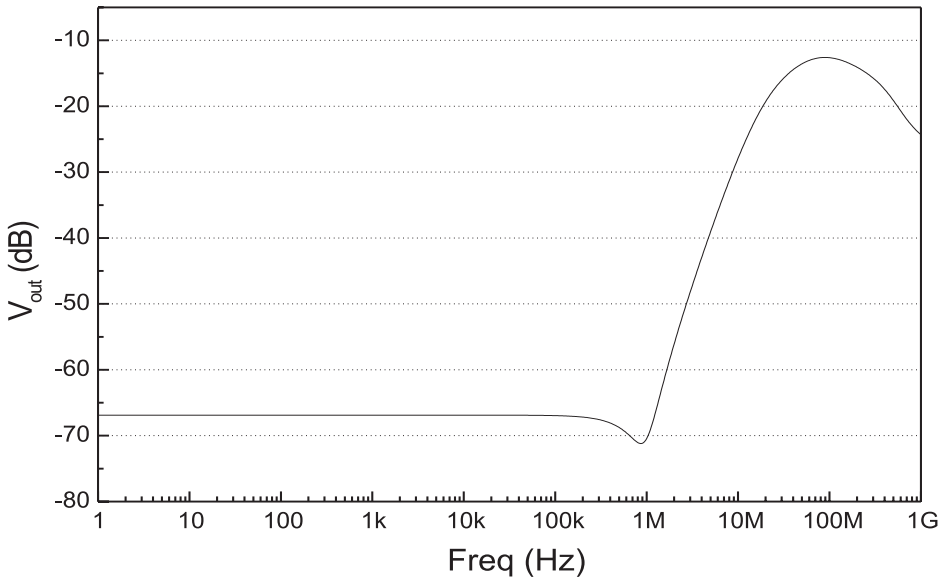


Figure 3.13: Simulation results showing the PSRR- for the circuit shown in Figure 3.22

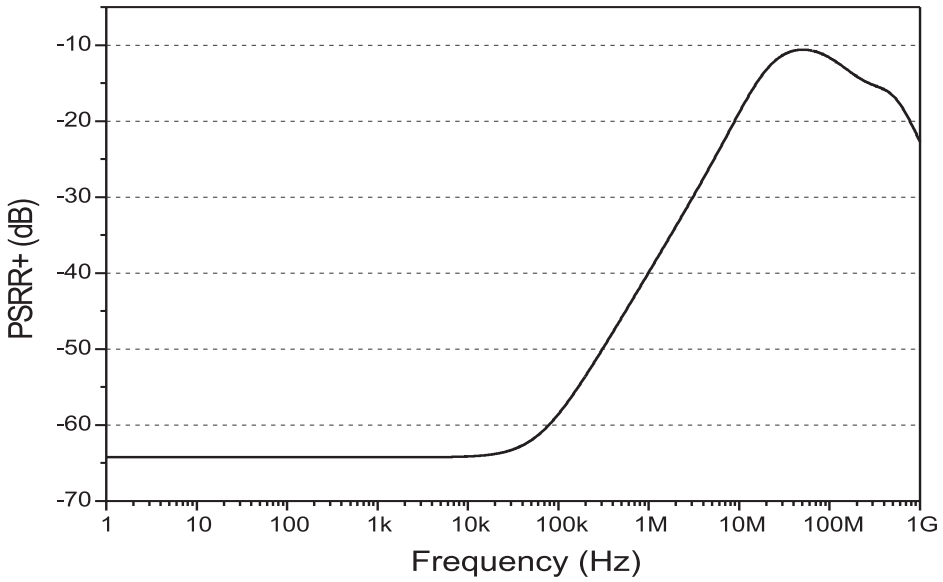


Figure 3.14: Simulation results showing the PSRR+ for the circuit shown in Figure 3.22

3.1.8 Output Stage

One way of constructing an output amplifier is to use the source-follower configuration of the MOS transistor. This configuration has both large current gain and low output resistance. Unfortunately, since the source is the output node, the MOS device becomes dependent on the body effect. The body effect causes threshold voltage V_{TH} increase as the output voltage is increased, creating a situation where the maximum output is substantially lower than V_{DD}. Figure 3.15 shows the general configuration for the CMOS source follower. The gate of the M_2 is connected to the output to form an active resistor. The small signal gain can be found as

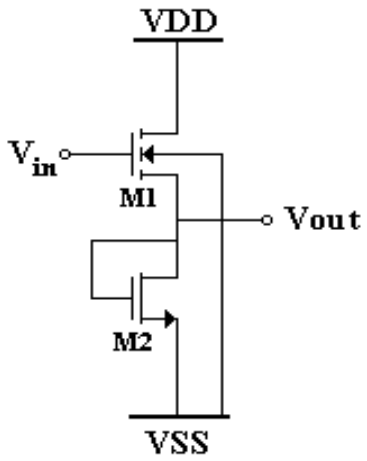


Figure 3.15: Common-drain (Source-follower) output amplifier

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}}{g_{ds1} + g_{ds2} + g_{m1}(1 + g_{mb1}/g_{m1})} \tag{3.35}$$

where the effect of bulk is implemented by the g_{mb1} transconductance.

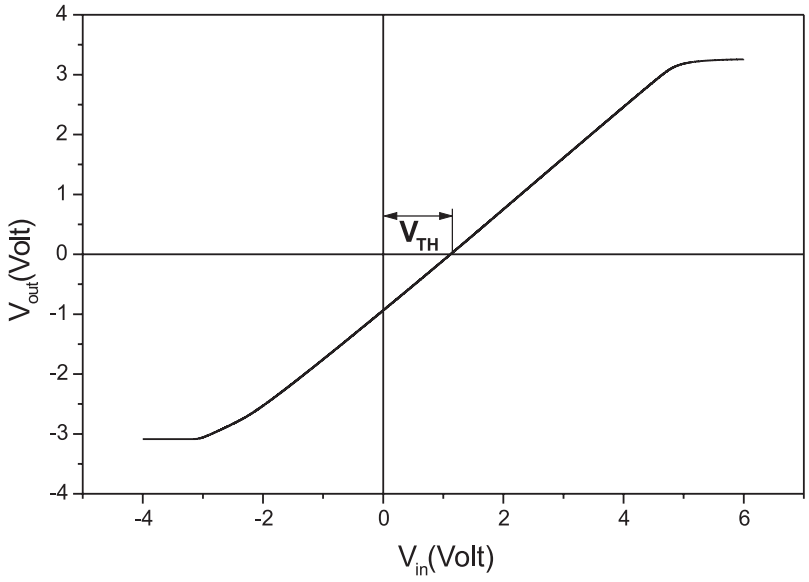


Figure 3.16: Transfer characteristics of the ClassA output stage

3.1.9 Linearity

In electronics, linearity is an important concept. All systems should be designed to be as linear as possible over the expected operating range. There is a good reason for this: nearly all analyses we use to determine system performance and stability assume the system is linear. This section discusses linear systems and their properties, and gives techniques on how to determine linearity in a system. There are several characteristics on what a linear system constitutes.

- In a linear system, the output must resemble the input
- A linear system has only a single input and a single output
- The output must be in the same dimensions as the input. That is, if an input is a continuous voltage, the output must also be a continuous voltage
- A linear system generates no new frequencies. That is, if the input is a single sine wave, the output must also be a sine wave, perhaps shifted in phase and amplitude, but it must be a sine wave of the same frequency as the input and nothing else

The nonlinearity can be quantified by looking at how straight the input and output characteristic is. Figure 3.1.9 shows input and output characteristic of two stage op-

amp without employing negative feedback. The characteristic is linear and exhibits almost straight line behaviour. Figure 3.1.9 shows the same op-amp's linearity result but with use of negative feedback.

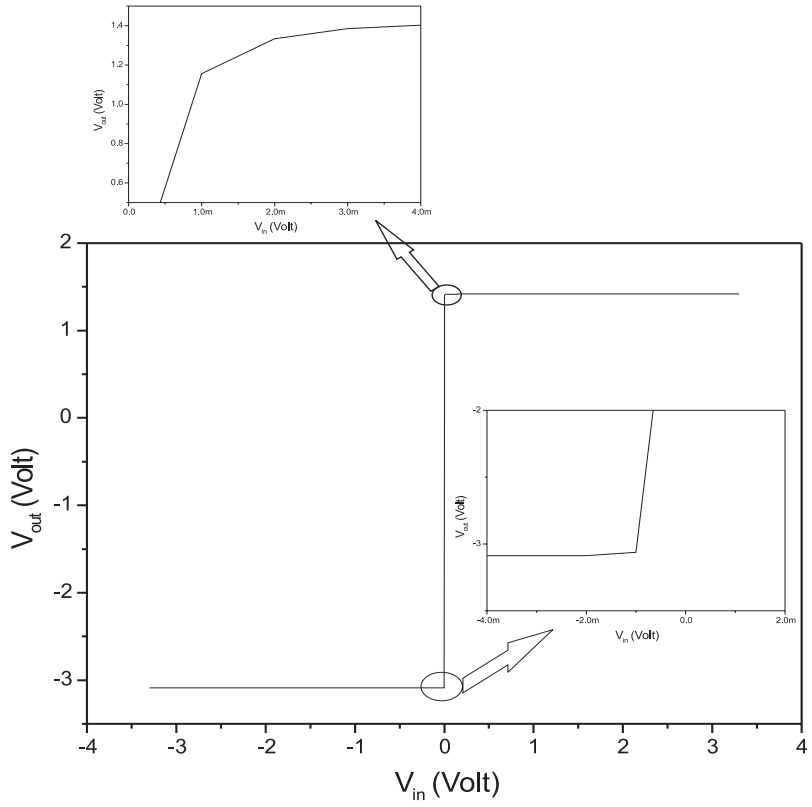


Figure 3.17: Linearity of basic two stage op-amp

The nonlinearity of a circuit can also be characterized by applying a sinusoid at the input and measuring the harmonic content of the output. This analysis gives us an important parameters called Total Harmonic Distortion (THD). THD of a signal is the ratio of the sum of the powers of all harmonic frequencies above the fundamental frequency to the power of the fundamental frequency. The THD is usually expressed in dB and measurements for calculating the THD are made at the output of a device under specified conditions. Figure 3.1.9 shows the thd result of the basic op-amp. 200m is a percentage value that is 0.2 % (- 54 dB) of THD.

3.1.10 Phase Margin

Phase margin is the phase difference between the input and output of an open circuit control loop at a frequency where the loop has unity gain. Phase margin

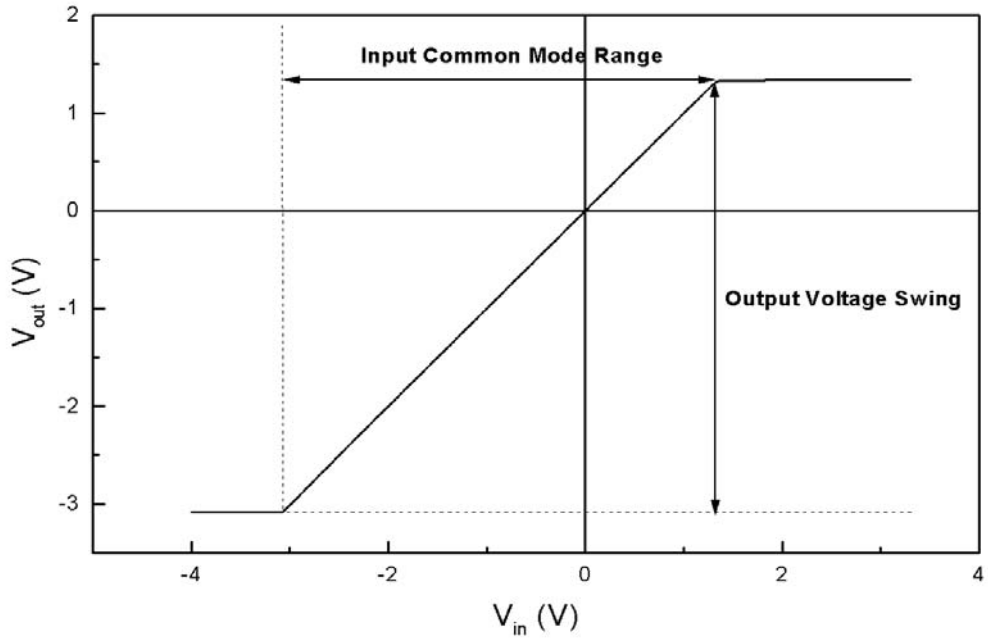


Figure 3.18: Linearity of the two stage op-amp with employing negative feedback

is important and directly related with stability of an op-amp. Therefore it needs special attention. While designing the op-amp phase margin is adjusted through compensation capacitor and nulling resistor. But adjusting these components affects bandwidth. So it presents trade-off between bandwidth and phase margin. Thus the best thing is to simulate the circuit parametrically. Figures 3.20 gives us the dependence between phase margin and nulling resistor.

But at the same time nulling resistor defines bandwidth of the op-amp this effect is shown in Figure 3.21. The phase margin is a function of nulling resistor. The range of nulling resistor for which phase margin and bandwidth changes is shown in Table 3.1.10.

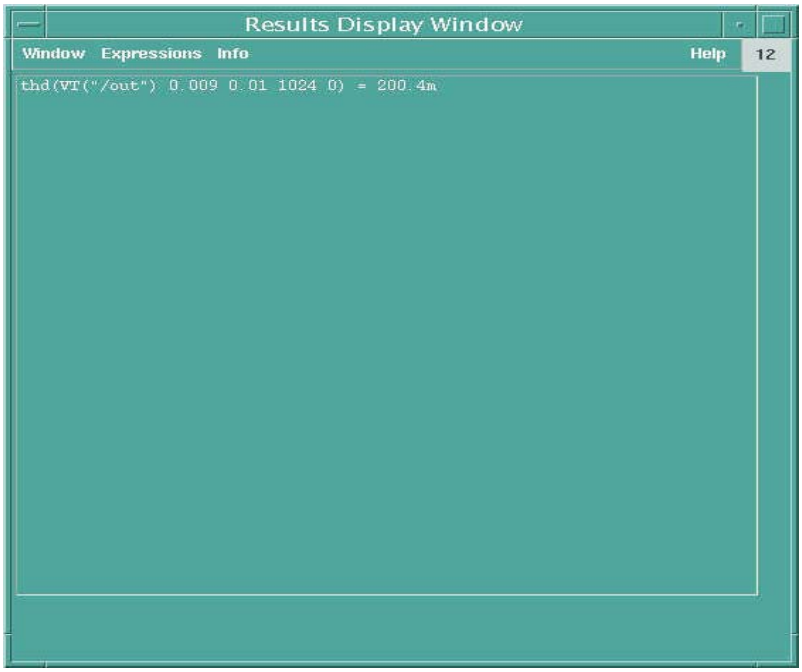


Figure 3.19: THD of the basic op-amp

3.1.11 Two Stage Op-Amp Design and Simulation

The overall structure of the basic two stage op-amp is shown in Figure3.22 Gain: Since there are three stages in this op-amp overall gain is the product of the each stage. Therefore the total small signal gain is

$$A = g_{m1}g_{m6}(r_{O2} \parallel r_{O4})(r_{O4} \parallel r_{O7})\frac{g_{m8}}{\frac{1}{r_{O8}} + \frac{1}{r_{O9}} + g_{m8}(1 + \frac{g_{mb8}}{g_{m8}})} \tag{3.36}$$

Component values for two stage op-amp are given in table 3.1.11. Important performance parameters of the two stage op-amp are given table 3.1.11. Load capacitance

Table 3.1: Nulling Resistor effect on Bandwidth and Phase Margin

Nulling Resistor (kΩ)	Bandwidth (MHz)	Phase Margin
1	76	71.5°
3.5	426	75.8°
6	517	5.3°
8.5	543	172.6°
11	551	166.3°

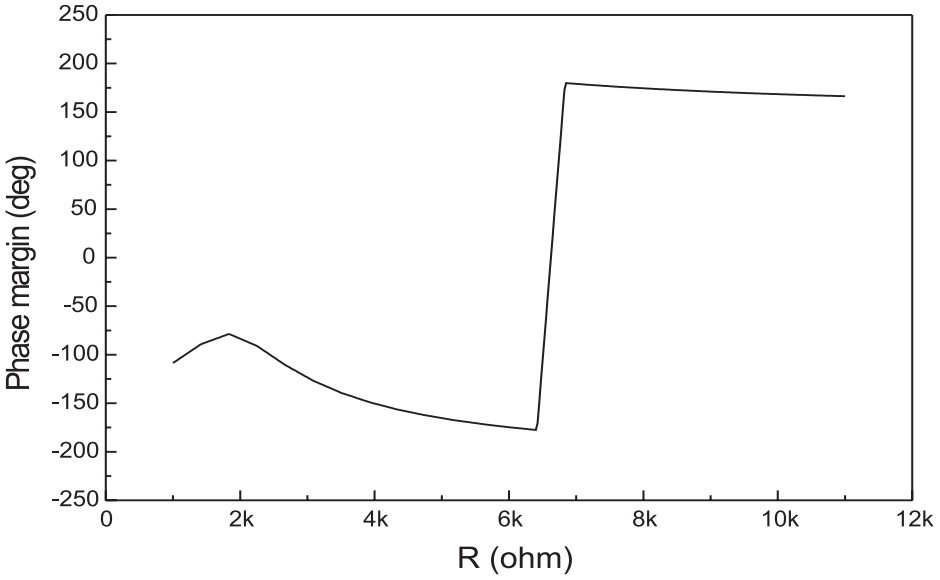


Figure 3.20: Phase margin versus nulling resistor R

C_O is 250 fF.

3.2 Design and small signal analysis of a two-stage folded-cascode CMOS Operational Amplifier

The CMOS folded-cascode operational amplifier (op-amp) provides higher frequency operation and better power supply noise rejection in switched-capacitor (SC) circuits than conventional cascode stage. It has recently been shown that for SC applications there exists a well-defined minimum settling time (MST) versus unity-gain phase margin for two pole op-amps [21]. Since the folded-cascode design is well suited to high frequency applications, it is desirable to design it for the MST response in order to obtain the maximum operating frequency. This section presents design and small-signal analysis of the CMOS single-ended two-stage folded cascode op-amp shown in Figure 3.2. A small signal model of the first stage of the above op-amp is associated with nodes a through e in Figure 3.24. The very high frequency pole associated with the node between M_5 and M_6 is excluded from the model with negligible error. The loading capacitance, C_L is included in C_d and V_{out} is associated with node d. The node equations for the equivalent circuit are

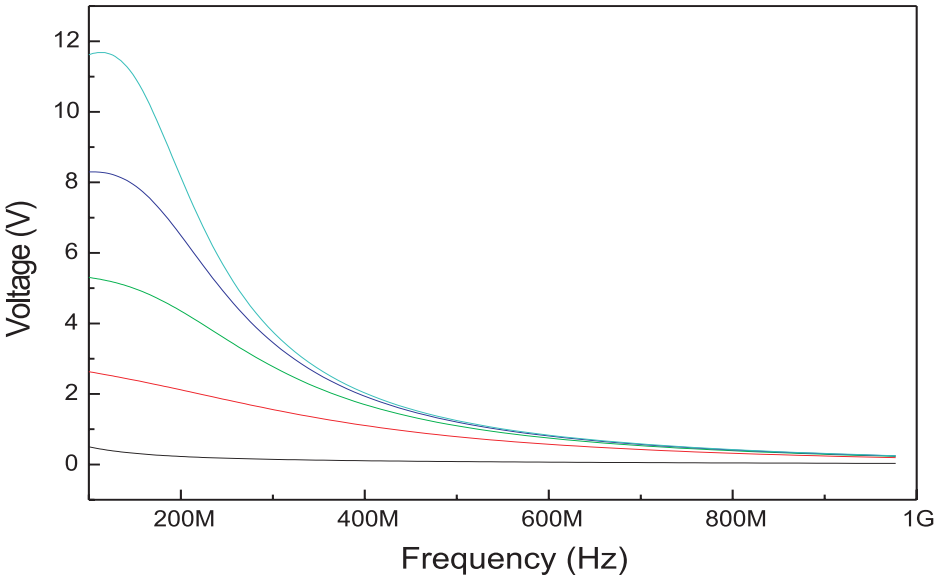


Figure 3.21: Effect of R on op-amp bandwidth

$$g_{m2}(V_{in}/2) + (1/R_a + G_{m4} + g_{ds4} + sC_a)V_a - g_{ds4}V_b = 0 \tag{3.37}$$

$$-(G_{m4} + g_{ds4})V_a + (1/R_b + g_{ds4} + sC_b)V_b = 0 \tag{3.38}$$

$$g_{m10}V_b + (1/R_c + G_{m9} + g_{ds9} + sC_c)V_c - gds9V_{out} = 0 \tag{3.39}$$

$$-(G_{m9} + g_{ds9})V_c - (G_{m8} + g_{ds8})V_e + (g_{ds8} + g_{ds9} + sC_d)V_{out} = 0 \tag{3.40}$$

$$-g_{m1}(V_{in}/2) + (1/R_e + G_{m8} + g_{ds8} + sC_e)V_e - g_{ds8}V_{out} = 0 \tag{3.41}$$

Where $G_m = g_m + g_{mbs}$. Using a dominant-pole approximation, the transfer function for the circuit of Figure **??** is

$$a(s) \approx \frac{(1 + s/s_{z1})(1 + s/s_{z2})}{(1 + s/\omega_b)(1 + s/\omega_c)(1 + s/\omega_d)(1 + s/\omega_e)} \tag{3.42}$$

the dominant pole frequency

$$\omega_d \approx \frac{(g_{ds1} + g_{ds7})(g_{ds8} + G_{m8}) + g_{ds10}(g_{ds9} + G_{m9})}{C_d} \tag{3.43}$$

and the nondominant pole/zero frequencies are

$$\omega_b \approx \frac{g_{m6}}{C_b} \tag{3.44}$$

$$\omega_c \approx \frac{G_{m9}}{C_c} \tag{3.45}$$

$$\omega_e \approx \frac{G_{m8}}{C_e} \tag{3.46}$$

$$s_{z1}, s_{z1} \approx (\omega_b + \omega_c)/2 \pm [(\omega_b^2 + \omega_c^2)/4 - 3\omega_b\omega_c/2]^{1/2} \tag{3.47}$$

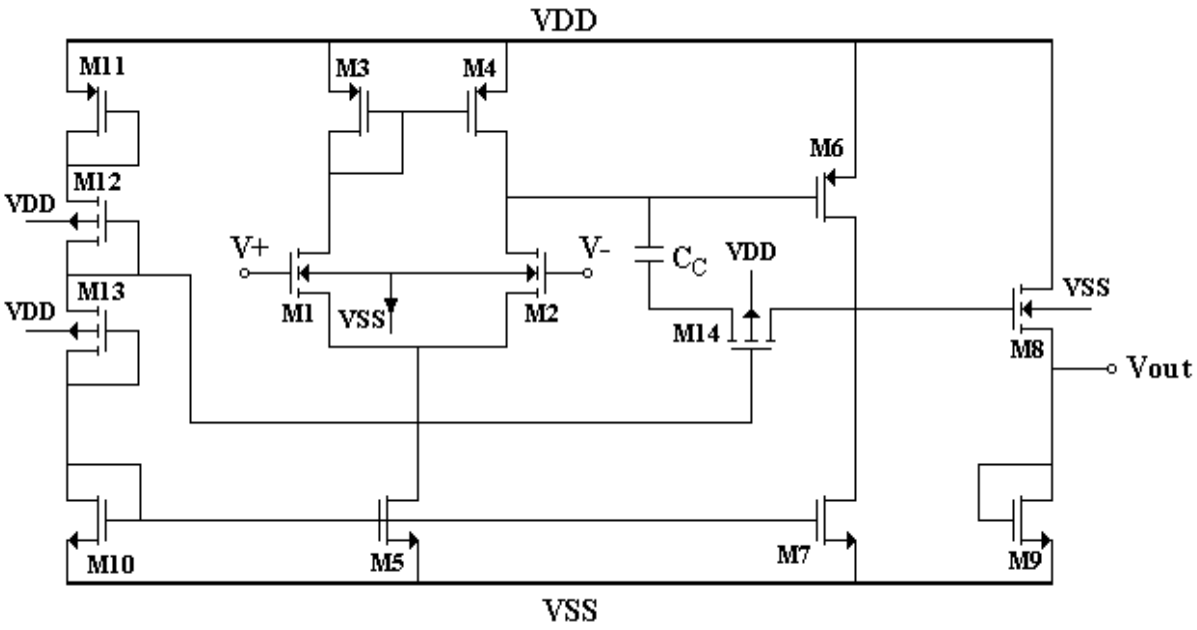


Figure 3.22: Complete schematic of the two stage Op-amp

C_d is approximately equal to the loading capacitance, C_L. Thus the dominant pole $\omega_d \approx \frac{(g_n+g_p)}{C_L}$ is determined by the loading capacitance C_L. Folded Coscode op-amp characteristics are given in appendix B.

Table 3.2: Overall Op-Amp Characteristics.

OP-AMP Specifications	Simulation Results
Gain	$6207V/V(75.85dB)$
Gain-Bandwidth	$60.256MHz$
Settling Time	$< 1\mu sec$
Slew Rate	$6V/\mu sec$
ICMR	$-3.1to1.336V$
Output Swing	$-3.1to1.4V$
Phase Margin	76^o
Offset	$484.3\mu V$
Power Dissipation	$3.151mW$
PSRR+	$139.5dBat1kHz$
PSRR-	$142.7dBat1kHz$
CMRR	$95.5dB$

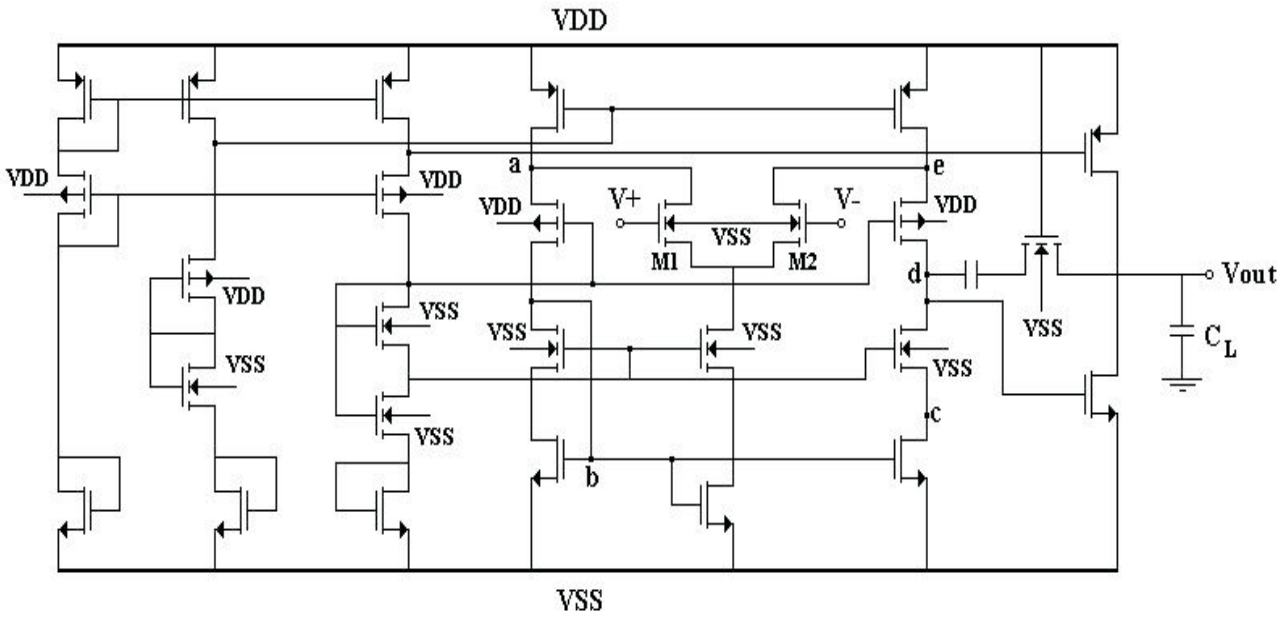


Figure 3.23: Two-stage folded-cascode

Table 3.3: Critical values of the transistors in the op-amp

Transistor	W/L($\mu m/\mu m$)	Function	Typ $V_{GS}/V_{DS}(V)$	g_m(mA/V)
M_1	15/1	Input Diff. Stage	1.125 / 2.932	0.241
M_2	15/1	Input Diff. Stage	1.125 / 2.932	0.241
M_3	10/10	Active Load	-1.494 / -1.494	0.0346
M_4	10/10	Active Load	-1.494 / -1.494	0.0346
M_5	1/0.6	Current Sink	1.127 / 2.174	0.0899
M_6	7/0.3	Common Source	-1.702 / -2.181	0.577
M_7	16/1	Current Sink	1.127 / 4.419	1.070
M_8	10/0.3	Output Stage	1.12 / 3.301	0.594
M_9	1/10	Active Load	3.299 / 3.299	0.0259
M_{10}	1/0.6	Biasing	1.127 / 1.127	0.0882
M_{11}	1/0.6	Biasing	-1.825 / -.1825	0.0462
M_{12}	1/0.3	Biasing	-1.747 / -1.747	0.0625
M_{13}	1/0.3	Biasing	-1.901 / -1.901	0.0631
M_{14}	10/0.3	Active Resistor	1.869 / 191.7 n	2.061E-13

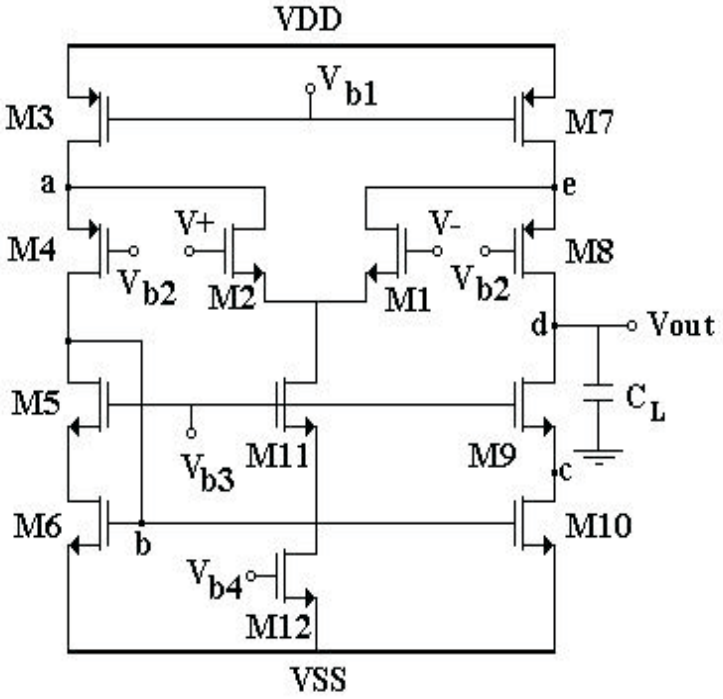


Figure 3.24: One-stage single-ended folded-cascode CMOS operational amplifier

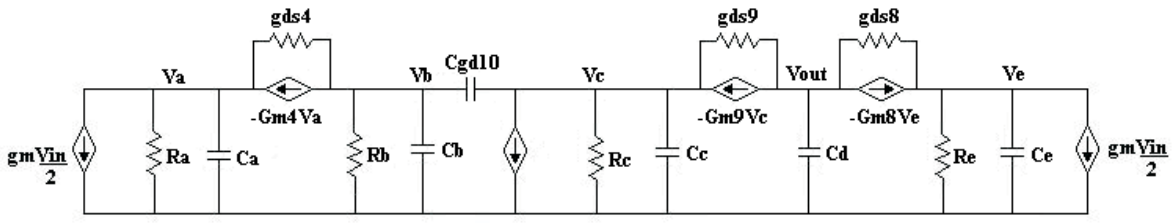


Figure 3.25: A complete small signal model for the op-amp of Figure 3.2. Node voltages $V_a - V_e$ refer to nodes a-e in Figure 3.24, and V_{out} is associated with node d.

Chapter 4

Oscillator

Oscillators are an integral part of many electronic systems. Applications range from clock generation in microprocessors to carrier synthesis in cellular telephones, requiring vastly different oscillator topologies and performance parameters.

The oscillator is an important component of modern communication systems. Integrating this element saves the need for off-chip resonator or discrete inductors and provides important advantages in terms of cost, physical size, pin count, and design flexibility. Although the circuit structure appears very simple, the design of a oscillator compliant with the specifications of modern wireless standards is one of the most complex tasks in the integration of a transceiver. The tuning range and phase noise requirements are usually the tightest specifications; they trade off each other and with power dissipation. Moreover, these circuits are intrinsically time-variant, which makes analysis of their behavior extremely difficult, mainly of their phase noise performance. Research in this field is therefore very active, especially considering the rising of new standards operating in the multi-gigahertz range.

Several recent results have demonstrated the possibility of building fully integrated LC resonators for 1-5 GHz applications. These resonators are based on inductors in the nH range and varactors in the pF range, which have been proven feasible for on-chip fabrication. The drawback of this fully integrated approach is the low quality factors of the resulting resonators compared to discrete devices, increasing the phase noise level and power dissipation required to achieve high oscillation amplitude [31].

A piezoelectric crystal, such as quartz, exhibits electromechnical-resonance characteristics that are very stable (with time and temperature) and highly selective

(having very high Q factors). The extremely stable resonance characteristics and the very high Q factors of quartz crystals result in oscillators with very high accurate and stable frequencies. Crystals are available with resonance frequencies in the range of few kHz to hundreds of MHz. Temperature of ω_0 of 1 or 2 parts per millon (ppm) per ^oC are achievable. Unfortunately, crystal oscillators, being mechanical resonators, are fixed-frequency circuits.

However poly crystalline silicon micromechanical resonators, with Q's over 80,000 under vacuum at audio frequencies and center frequency temperature coefficients in the range of -10 ppm/^oC, can serve reasonably well as miniaturized substitutes for crystals in a variety of high-Q oscillator and filtering applications.

This chapter deals with the analysis and design of CMOS oscillators integrated with MEMS based resonator. Beginning with a general study of oscillation in feedback systems, we introduce LC oscillators along with methods of varying the frequency of oscillation.

4.1 General Consideration

A simple oscillator produces a periodic output, usually in the form of voltage. As such, the circuit has no input while sustaining the output indefinitely. How can a circuit oscillate? An oscillator is a badly-designed feedback amplifier. Consider the unity-gain negative feedback circuit shown in Figure 4.1, where

$$\frac{V_{out}}{V_{in}}(s) = \frac{H(s)}{1 + H(s)} \tag{4.1}$$

If the amplifier itself experiences so much phase shift at high frequencies that the overall feedback becomes positive, then the oscillation may occur. More accurately, if for s = ω_0, H(jω_0) = -1, then the closed-loop gain approaches infinity at ω_0. Under this condition, the circuit amplifies its own noise components at ω_0. For oscillation to begin, a loop gain of unity or greater is necessary. In summary, if a negative-feedback circuit has a loop gain that satisfies two conditions:

$$|H(j\omega_0)| \geq 1 \tag{4.2}$$

$$\angle H(j\omega_0) = 180 \tag{4.3}$$

then the circuit may oscillate at ω_0. Called —Barkhausen criteria—. These conditions are necessary but not sufficient [10]. CMOS oscillators in today's technology

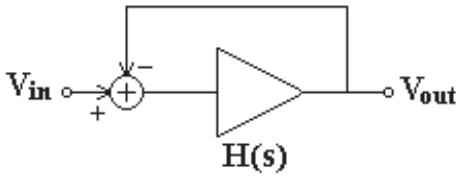


Figure 4.1: Basic structures of a feedback system

are typically implemented as ring oscillators or LC oscillators.

4.2 LC Oscillators

Before delving into such oscillators, it is instructive to review basic properties of RLC circuits. We begin our study of circuit resonance with the parallel structure shown in Figure 4.2. Analytical expression for V_{out} as a function of ω is

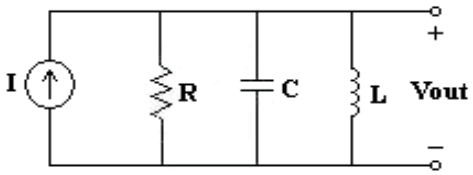


Figure 4.2: The parallel-resonant circuit.

$$V_{out} = \frac{I}{\frac{1}{R} + \frac{1}{j\omega L} + j\omega C} \tag{4.4}$$

Amplitude of V_{out} is

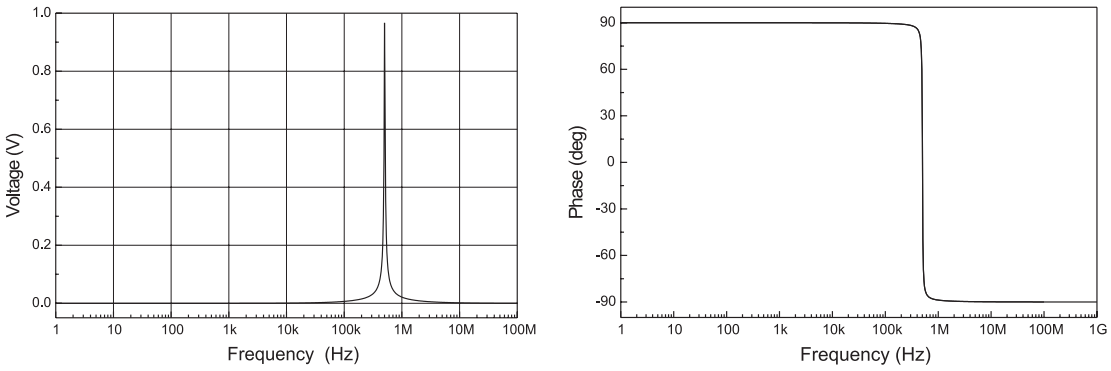
$$|V_{out}| = \frac{|I|}{\sqrt{1/R^2 + [\omega C - (\frac{1}{\omega L})]^2}} \tag{4.5}$$

and the phase angle between I and V is

$$\theta = -\tan^{-1}(\omega C - \frac{1}{\omega L})R \tag{4.6}$$

The resonant frequency for the circuit in Figure 4.2 is defined as the frequency that makes the impedance seen by the current source purely resistive.

$$\omega_0 C = \frac{1}{\omega_0 L} \Rightarrow \omega_0 = \frac{1}{\sqrt{LC}} \tag{4.7}$$



(a) (b)

Figure 4.3: (a) Amplitude and (b) phase versus frequency for the circuit of Figure 4.2

4.3 Bandwidth and Quality Factor

The bandwidth for the parallel-resonant circuit of Figure 4.2 is defined as the range of frequencies in which the amplitude of the output voltage is equal or greater than the maximum value divided by $\sqrt{2}$. The limiting frequencies ω_1 and ω_2, which define the bandwidth, can be found by corresponding to the values of ω that make

$$\sqrt{\frac{1}{R^2} + (\omega C - \frac{1}{\omega L})^2} = \frac{\sqrt{2}}{R} \tag{4.8}$$

or

$$(\omega C - \frac{1}{\omega L})^2 = \frac{1}{R^2} \tag{4.9}$$

$$\omega_1 = -\frac{1}{2RC} + \sqrt{(\frac{1}{2RC})^2 + \frac{1}{LC}} \tag{4.10}$$

$$\omega_2 = \frac{1}{2RC} + \sqrt{(\frac{1}{2RC})^2 + \frac{1}{LC}} \tag{4.11}$$

from which it fallows that the bandwidth of the circuit

$$\beta = \omega_2 - \omega_1 = \frac{1}{RC} \tag{4.12}$$

with above equation in mind, we see that we can use the inductor and capacitor to fix the resonant frequency and then the value of R to adjust the bandwidth. Large values of R correspond to narrow bandwidth, which in turn implies that the circuit is very selective as to which frequencies it transmits. For a circuit that is intended to be frequency-selective, the sharpness of the selectivity is a measure of the quality of the circuit. The quality of the frequency response is described quantitatively in

terms of the ratio of the resonant frequency to the bandwidth. This ratio is called the Q of the circuit; thus

$$Q = \frac{\omega_0}{\beta} \tag{4.13}$$

For the parallel-resonant structure in Figure 4.2 the quality factor can be expressed in several ways, namely

$$Q = \omega_0 RC = \frac{R}{\omega_0 L} = R\sqrt{\frac{C}{L}} \tag{4.14}$$

For applications outside the realm of circuits, we can also define Q in terms of an energy ratio, namely,

$$Q = 2\pi \frac{maximum\ energy\ stored}{total\ energy\ lost\ per\ period} \tag{4.15}$$

The phase angle θ can also be expressed in terms of Q since $\beta = \omega_0/Q$; thus

$$\theta = -\tan^{-1} \frac{(\omega + \omega_0)(\omega - \omega_0)Q}{\omega_0 \omega} \tag{4.16}$$

The effect of Q on the phase-angle characteristic is most easily shown by investigating the slope of the θ versus ω curve at ω_0

$$\frac{d\theta}{d\omega} = -\frac{2Q}{\omega_0} = -2RC \tag{4.17}$$

Thus as Q is increased by increasing R, the slope at ω_0 increases. Note that if R is made infinitely large, the phase angle snaps from $+90^o$ to -90^o at the resonant frequency. The effect of Q on the magnitude is shown in Figure 4.3

4.3.1 The Frequency Response versus the Natural Response of the Parallel RLC Circuit

We are interested in the frequency response of a circuit because it can be used to predict the time-domain behavior of the circuit. Let us show how attributes of the frequency-response behavior relate to attributes of the natural time-domain response. For the under damped case is given by

$$v(t) = K_1 e^{-\alpha t} cos\omega_d t + K_2 e^{-\alpha t} sin\omega_d t \tag{4.18}$$

$$\alpha = \frac{1}{2RC} \tag{4.19}$$

$$\omega_d = \sqrt{\omega_0^2 - \alpha^2} \tag{4.20}$$

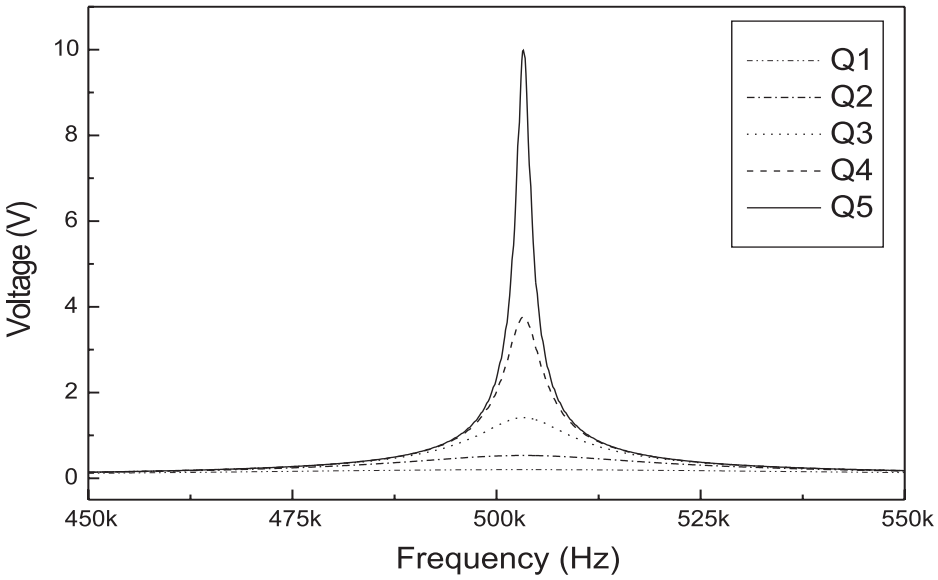


Figure 4.4: Effect of Q on resonant circuit magnitude response($Q5 \geq Q1$)

The coefficients K1 and K2 are determined by the initial conditions. We can relate the damping coefficient α and the damped frequency of oscillation ω_d to the Q of the circuit; thus

$$\alpha = \frac{\beta}{2} = \frac{\omega_0}{2Q} \tag{4.21}$$

$$\omega_d = \omega_0 \sqrt{1 - 1/4Q^2} \tag{4.22}$$

We also note that the transition from overdamped to the underdamped response occurs when $\omega_0^2 = \alpha^2$, or when Q = 1/2. Therefore the natural response will be underdamped whenever the Q of the circuit is greater than 1/2 or, alternatively, whenever the bandwidth is less than $2\omega_0$. From Equation 4.21 we see that in high-Q circuits natural response oscillation persists longer than in low-Q circuits. Equation 4.22 tells us that the frequency of oscillation in the underdamped response approaches the resonant frequency ω_0 as Q increases.

We can summarize our observations by saying that if the frequency response of the parallel RLC structure shows a sharp resonant peak, the natural response will be underdamped, the frequency of oscillation will approximate the resonant frequency, and the oscillations will persists over a relatively long interval of time [25].

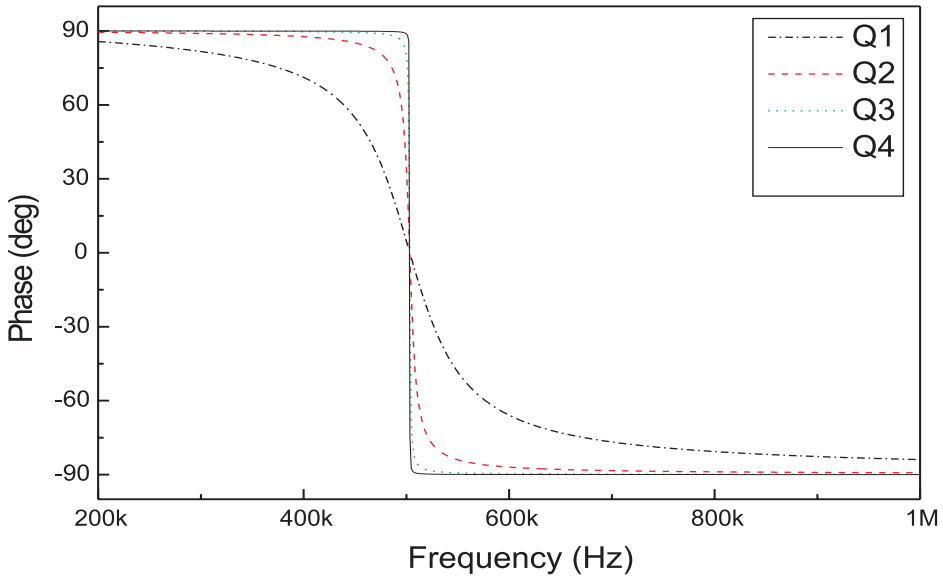


Figure 4.5: Effect of Q on resonant circuit phase response($Q4 \geq Q1$)

4.4 Series Resonance

The basic series resonant circuit is shown in Figure 4.6. Here we are interested in how the amplitude and phase angle of the current vary with the frequency of the sinusoidal voltage source. The analysis of the series-resonant circuit follows very closely the analysis of the parallel-resonant structure shown in Figure 4.2. The current amplitude will peak at V/R when the inductive reactance exactly cancels the capacitive reactance. The frequency at which the reactive impedances cancel is the resonant frequency of the circuit; thus $\omega_0 L = 1/\omega_0 C$, or

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{4.23}$$

The magnitude and the angle of the current (I) are, respectively,

$$|I| = \frac{V}{\sqrt{R^2 + [\omega L - 1/\omega C]^2}} \tag{4.24}$$

$$\theta = -\tan^{-1}\frac{\omega L - (1/\omega C)}{R} \tag{4.25}$$

The bandwidth of the series circuit is defined as the range of frequencies in which the amplitude of the current is equal to or greater than $1/\sqrt{2}$ times the maximum amplitude V/R. Thus the frequencies at the edge of the passband are the frequencies where the magnitude of the impedance equals $1/\sqrt{2}R$. Setting

$$\sqrt{R^2 + (\omega L - 1/\omega C)^2} = \sqrt{2}R \tag{4.26}$$

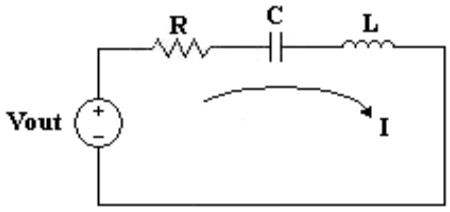


Figure 4.6: Series-resonant circuit

and solving for the two positive values yields

$$\omega_1 = -\frac{R}{2L} + \sqrt{(\frac{R}{2L})^2 + \frac{1}{LC}} \tag{4.27}$$

$$\omega_2 = \frac{R}{2L} + \sqrt{(\frac{R}{2L})^2 + \frac{1}{LC}} \tag{4.28}$$

Since by definition Q is the ratio of the resonant frequency to the bandwidth, the Q of the series circuit is

$$Q = \frac{\omega_0}{\beta} = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 CR} = \frac{1}{R}\sqrt{\frac{L}{C}} \tag{4.29}$$

The phase angle between the source voltage and the current can be expressed in terms of ω_0 and Q as

$$\theta = -\tan^{-1}\frac{(\omega + \omega_0)(\omega - \omega_0)Q}{\omega_0 \omega} \tag{4.30}$$

4.5 Analysis of a Practical Parallel Resonant Circuit

The parallel-resonant structure in Figure 4.7 is a more practical model because it accounts for the losses in the inductor. The inductor losses are represented by the resistor R. The resonance frequency for this circuit is

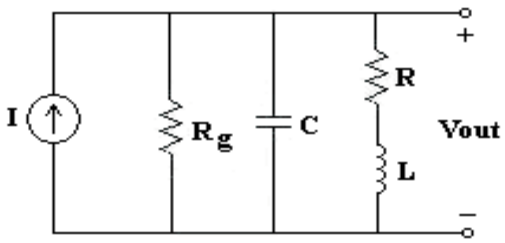


Figure 4.7: A parallel-resonant circuit containing a low loss inductor.

$$\omega_0 = \sqrt{\frac{1}{LC} - (\frac{R}{L})^2} \tag{4.31}$$

The circuit of Figure 4.7 can be transferred to an equivalent topology that more easily lends itself to analysis and design.

4.6 Parallel Crossed-Coupled Oscillator

Suppose we place two tuned gain stage in a cascade, as depicted in Figure 4.8 This configuration has two parallel resonance circuit and does not latch up because its low frequency gain is very small. Furthermore, at resonance, the total phase shift around the loop is zero because each stage contributes zero frequency-dependent phase shift. That is, if $g_{m1}Rg_{m2}R \geq 1$, then the loop oscillates. The circuit of Figure 4.8 serves as the core of many LC oscillators.

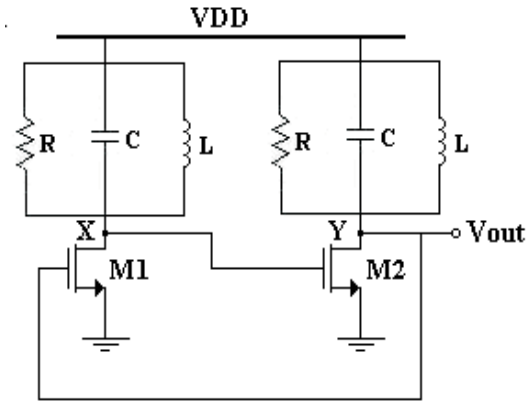


Figure 4.8: Two tuned stages placed in a feedback loop.

4.7 Series Crossed-Coupled Oscillator

The series crossed-coupled oscillator is analogous of the parallel counterpart except that parallel resonance circuit is replaced by series resonance circuit and is shown in Figure 4.9.

In this configuration frequency of oscillation is determined by the series-resonant circuit. Since the resonant circuit has high Q, the resultant oscillator achieves a reliable oscillation buildup and has a single predictable frequency of oscillation in the

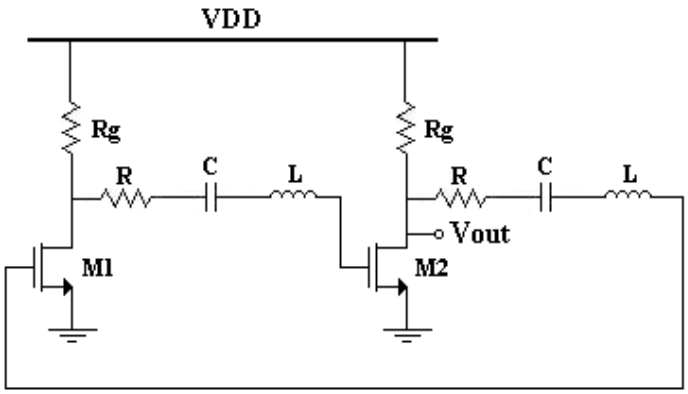


Figure 4.9: Series cross-coupled oscillator.

steady state. As oscillation grow in amplitude, the transistor's nonlinear characteristics reduce the effective value of g_m and, correspondingly, reduce the loop gain to unity, thus sustaining the oscillations. For sustained oscillations, the magnitude of the gain from the gate to drain must be greater than unity at resonance. Because the total phase shift around the loop is zero. Thus

$$g_m R_g \geq 1 \tag{4.32}$$

Unlike the op-amp oscillators that incorporate special amplitude-control circuitry, LC-tuned oscillators utilize the nonlinear $i_D - v_{GS}$ characteristics of the MOS for amplitude control. Thus these LC-tuned oscillators are known as self-limiting oscillators. Specifically, as the oscillations grow in amplitude, the effective gain of the transistor is reduced below its small-signal value. Eventually, an amplitude is reached at which the effective gain is reduced to the point that the Barkhausen criterion is satisfied exactly. The amplitude then remains constant at this value [24]. Figure 4.7 shows the implementation of the oscillator given in Figure 4.9. R_g's are replaced by the transistors operating in sat. Other transistor are for the biasing. A sample oscillation for the Figure 4.7 is given in Figure 4.7. In this figure a series resonant of circuit is used for selecting 5 KHz noise component. In the Figure 4.12 the resonator values are taken directly from the equivalent model of microresonator.

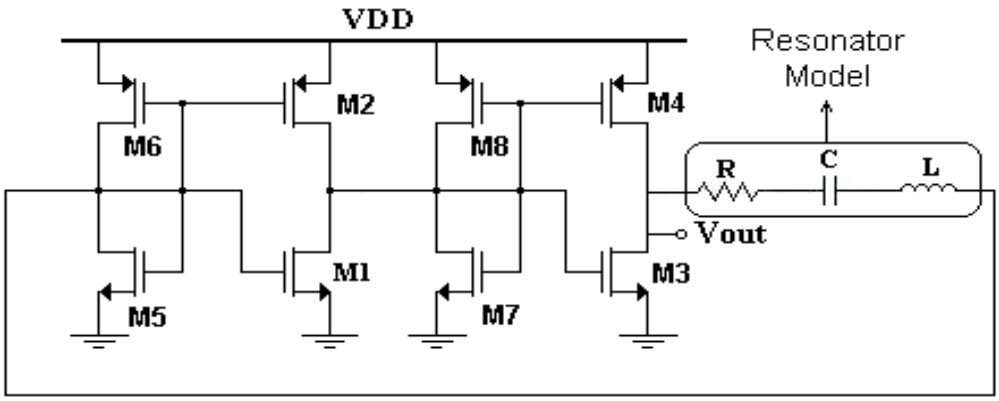


Figure 4.10: Complete circuit for the oscillator shown in Figure 4.9

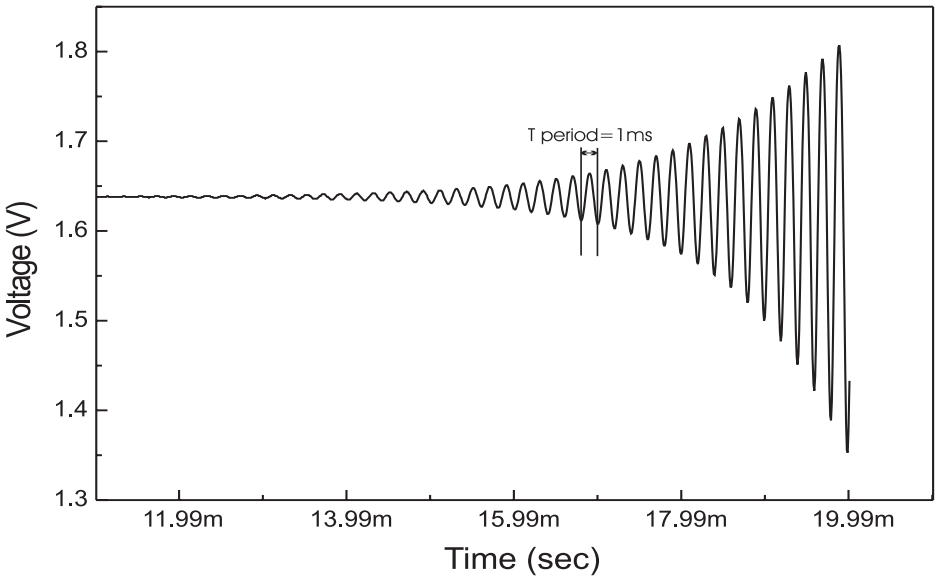


Figure 4.11: Oscillation at 5 KHz

4.8 Microelectromechanical Resonator Oscillator Design

MEM vibrating structures such as linear drive resonators can be used to realize integrated high-Q tanks. These structures have high-Q values (as high as 80.000 [15], [16]) and relatively small sizes (as small as 1000 times [17]). For high frequency applications, resonators operating at 733MHz have also been demonstrated [3]. Having these attributes and advances in micromachining technologies make MEM resonator a preferred candidate as miniaturized substitutes for the off-chip components in verity of oscillator and filter applications. Many micromechanical resonators are integrated with conventional integrated circuits to form a fully monolithic oscillators

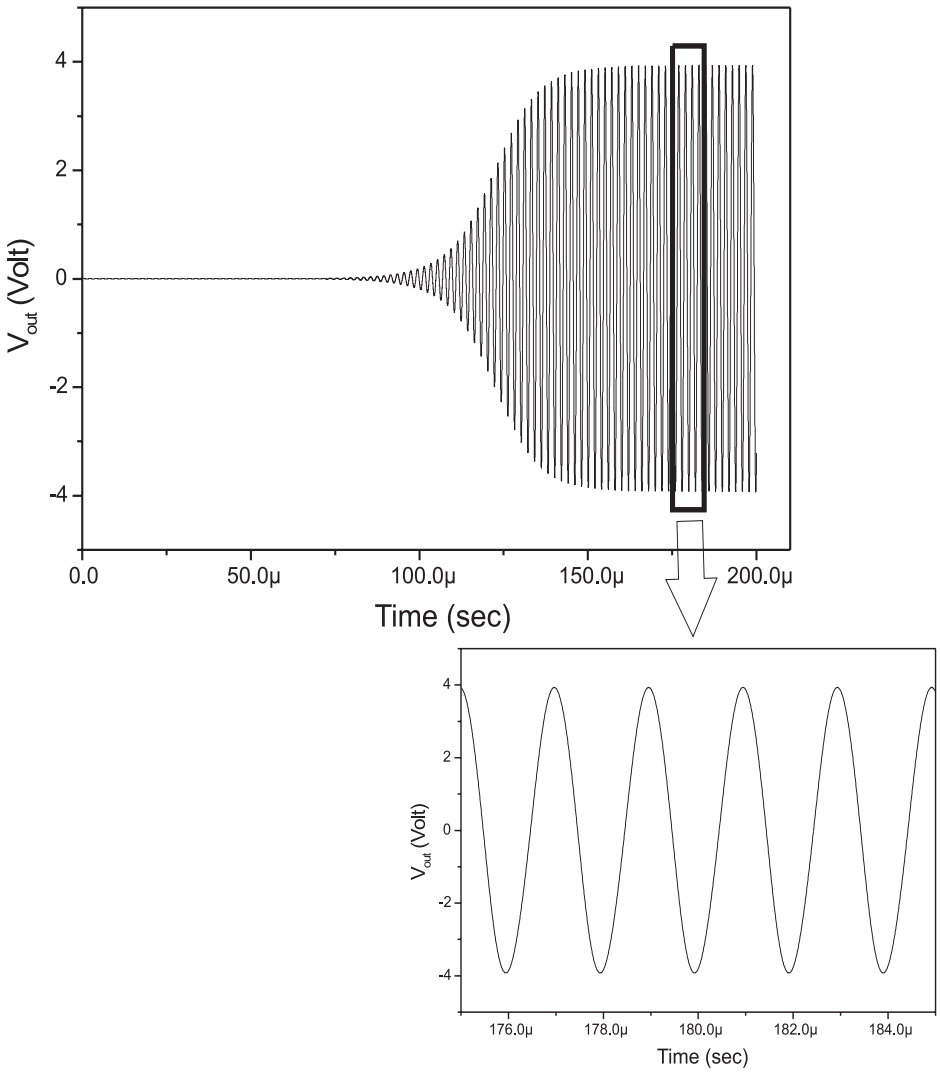


Figure 4.12: Oscillation at 500 KHz

and working samples are demonstrated at 14MHz [18].

The design of the MEM oscillator is done by using the equivalent circuit of the MEM resonator given in the Figure 4.13. Design of a high Q oscillator often requires specific attention to preservation of the quality factor of the high-Q element. In this respect, the best high-Q oscillator designs are those for which degradation of resonator Q by the sustaining electronics is minimized. With this in mind, oscillator architectures may be subdivided into two broad categories: series resonant or parallel resonant. Schematic examples are presented in Figures 4.14 and 4.15. Where for both cases, the two resonator is represented by an equivalent LCR circuit. In the series resonant architecture of Figure 4.15, the input impedance of the sustaining (transresistance) amplifier is in series with the resonator's motional resistance,

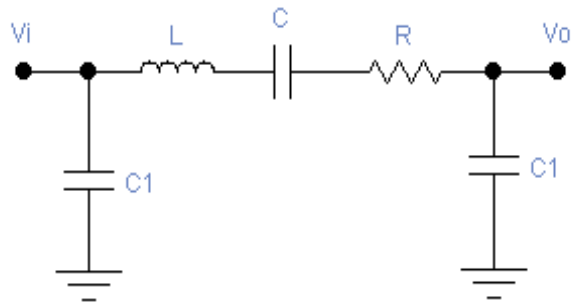


Figure 4.13: Equivalent circuit for a two-port capacitively transduced resonator. It is basically a series resonant circuit

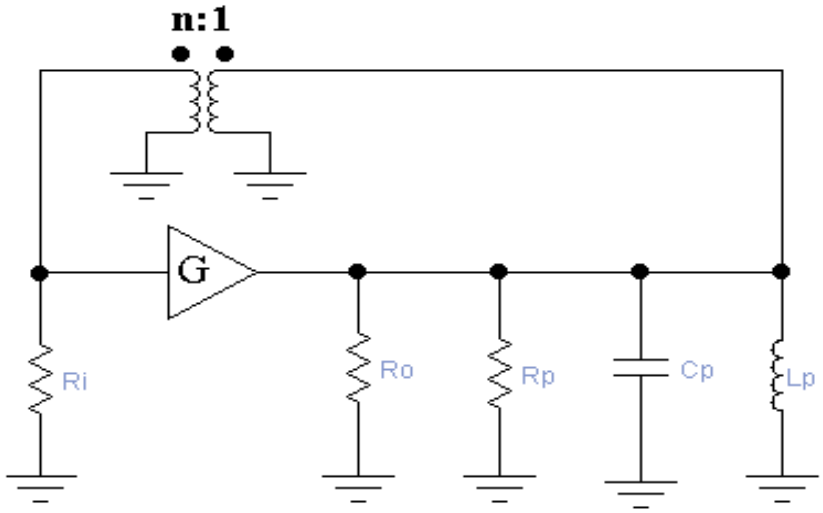


Figure 4.14: Schematic example of parallel resonant oscillator architecture

resulting in an effective oscillator Q given by

$$Q = \frac{\omega L_x}{(R_x + R_i + R_o)} = \frac{Q_{ul}}{1 + ((R_i + R_o)/R_x)} \tag{4.33}$$

where R_i and R_o are the input and output resistances of the sustaining amplifier, respectively, and $Q_{ul} = \omega L_x / R_x$ is the unloaded resonator quality factor. Eq. 4.33 indicates that a series resonant oscillator architecture offers minimum Q-loading of the resonator when the series motional resistance of the resonator R_x is much larger than the sum of the input and output resistance of the sustaining amplifier, i.e., where $R_x \gg R_i + R_o$.

For the parallel resonant architecture of Figure 4.14, the transformed input impedance and the output impedance of the sustaining (transconductance) ampli-

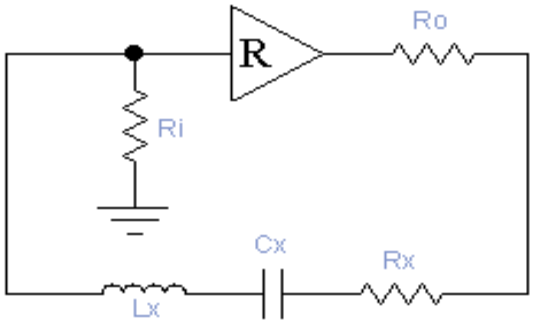


Figure 4.15: Schematic example of series resonant oscillator architecture

fier are in parallel with that of the parallel motional resistance R_p of the resonator, yielding an effective oscillator Q given by

$$Q = \frac{Q_{ul}}{1 + (R_p/(n^2 R_i \parallel R_o))} \tag{4.34}$$

Here, loading of the resonator Q is minimized when $R_p \ll R_i + R_o$. The motional resistance of a micromechanical resonator is usually quite large for typical values of resonator dc-bias voltage. Thus, for the prototype micromechanical resonator oscillator of this work, a series resonant oscillator architecture will be used. However it should be understood that parallel architectures, such as the popular Pierce design, could be advantageous for low series resistance resonator design.

Figure 4.8 shows a system level schematic describing the basic architecture used for this oscillator. It could be wiser to choose series resonant oscillator architecture to minimize Q-loading because motional series resistance of the resonator is large. As shown in the figure the system composed of a microresonator and an amplifier (it could be an op-amp or simple amplification stage). The microresonator is used as a resonator and defines the frequency of oscillation and amplifier sustains that oscillation properly.

Conceptually, the sustaining amplifier and micromechanical resonator comprise negative and positive resistances, respectively. During start up, the negative resistance of the amplifier, R_{amp} is larger in magnitude than positive resistance of the resonator, R_x and oscillation starts. Oscillation builds up until either some form of nonlinearity or a designed automatic-level control circuit alters either or both resistors so that, $R_{amp} = R_x$, at which point the oscillation amplitude limits.

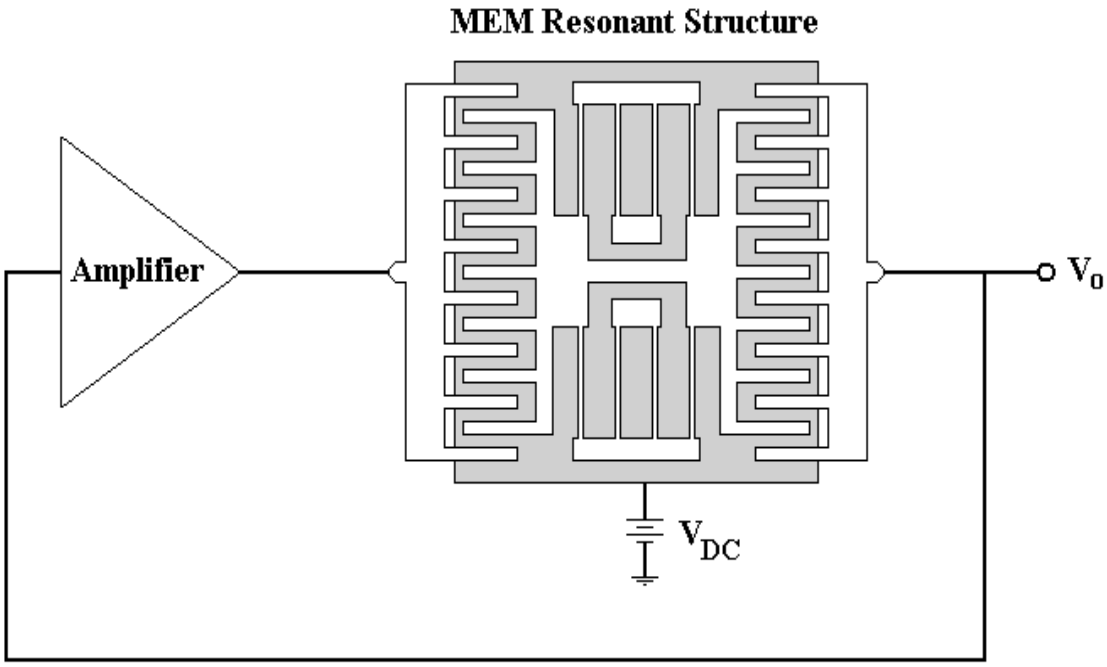


Figure 4.16: System level schematic showing the basic series resonant architecture used for the CMOS micromechanical reso nator oscillator of this work.

MEM Oscillator can also be designed using op-amp then using series RLC as the frequency defining circuit in the feedback path, Figure 4.8 can be obtained. Here op-amp is the key element because it must have large unity gain bandwidth, high gain and stable around the oscillation frequency, so phase margin should have a reasonable $(60-75^{o})$ value. Details of the op-amp to be used as sustaining amplifier is given in chapter 4.

4.9 Phase Noise in Oscillators

Oscillators exhibit a natural tendency to amplify any noise present near the oscillation frequency. The closer the frequency of the noise is to the oscillation frequency, the greater the amplification. Noise amplified by the oscillator in this manner is referred to as phase noise. Phase noise is extremely important because it is the most significant source of noise in oscillators. In addition, since the phase noise is centered about the oscillation frequency, it can never completely be removed by filtering.

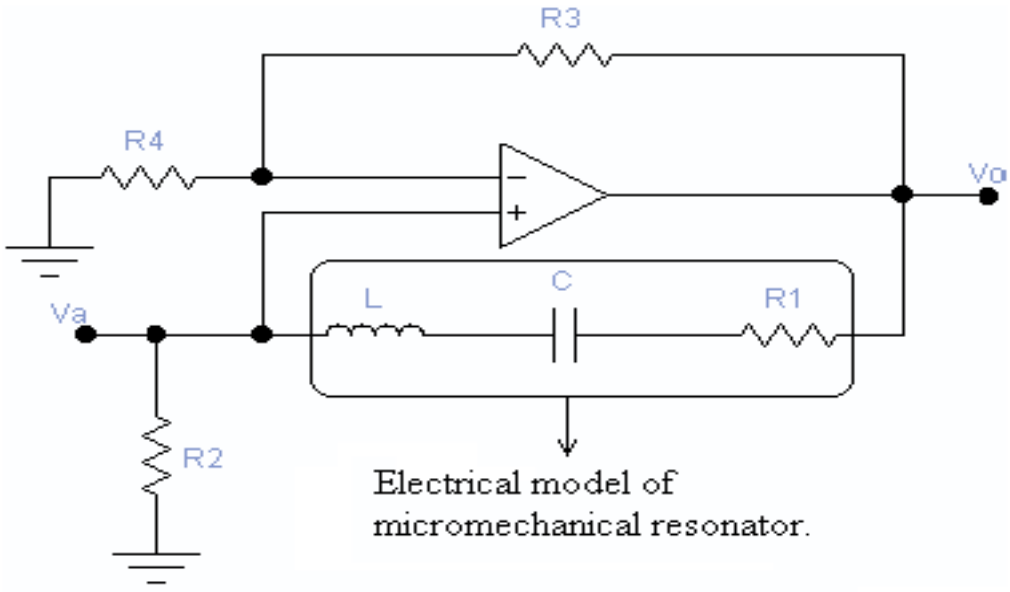


Figure 4.17: System level schematic using op-amp as a sustaining amplifier.

Phase noise can be understood by recognizing that the phase of an oscillator is arbitrary simply because there is no drive signal present to lock to. Any waveform that is a solution to an oscillator can be shifted in time and still be a solution. If a perturbation causes the phase to be disturbed, there is nothing that acts to restore the phase, so it is free to drift without bound. If the perturbation is random noise, the drift takes the form of a random walk. Furthermore, the closer the frequency of perturbation is to the oscillation frequency, the better it couples to the phase and the greater the magnitude of the drift. The perturbation need not come from random noise. It might also couple into the oscillator from other sources, such as the power supplies.

In particular, RF oscillators employed in wireless transceivers must meet stringent phase noise requirements, typically mandating the use of passive LC tanks with a high quality factor (Q). However, the trend toward large-scale integration and low cost makes it desirable to implement oscillators monolithically. Phase noise is usually characterized in the frequency domain. For an ideal oscillator operating at ω_0, the spectrum assumes the shape of an impulse, whereas for an actual oscillator, the spectrum exhibits "skirts" around the center or "carrier" frequency (Figure 4.9). To quantify phase noise, we consider a unit bandwidth at an offset $\Delta\omega$ with respect to

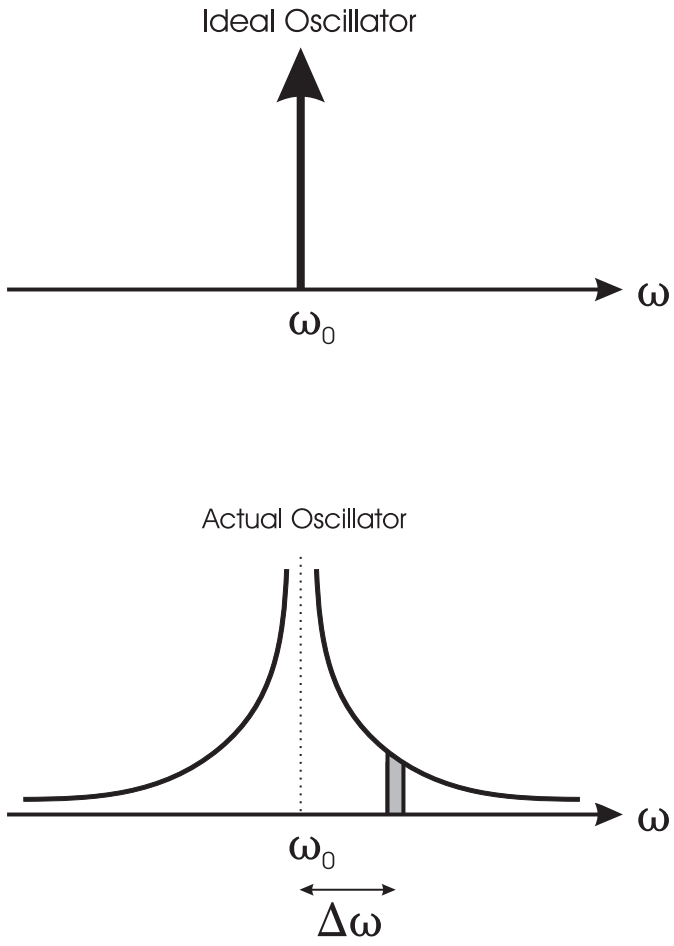


Figure 4.18: Spectrum of an ideal and actual oscillator showing phase noise in oscillators.

ω_0, calculate the noise power in this bandwidth, and divide the result by the carrier power [32].

To understand the importance of phase noise in wireless communications, consider a generic transceiver as depicted in Figure 4.9. The local oscillator (LO) providing the carrier signal both mixers is embedded in a frequency synthesizer. If the LO oscillator output contains phase noise, both the down converted and up converted signals are corrupted. This is illustrated in Figure 4.9 for the receive path.

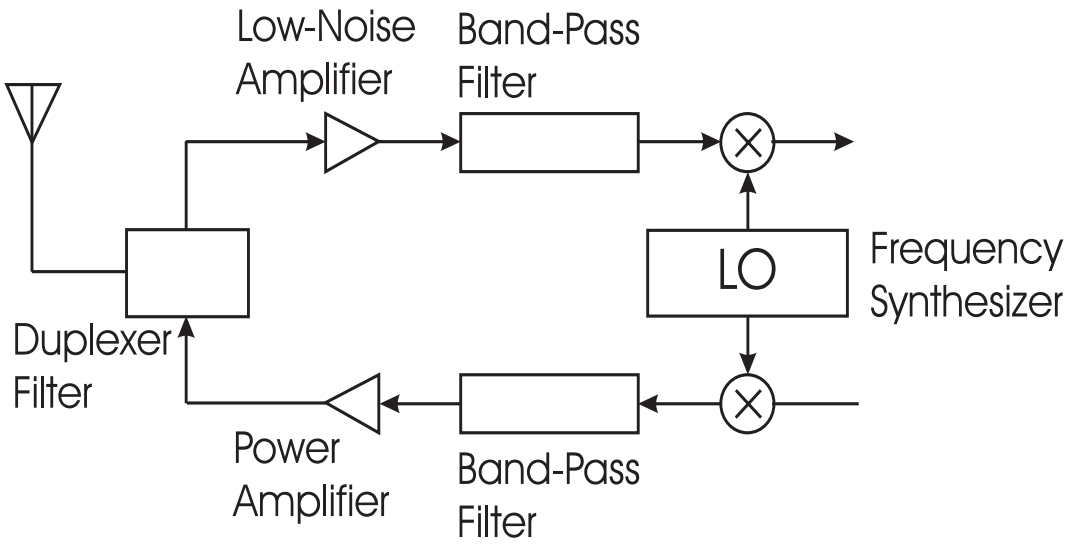


Figure 4.19: Generic wireless transceiver.

Referring to Figure 4.9 we note that in the ideal case, the signal band of interest is convolved with an impulse and thus translated to a lower (and a higher) frequency with no change in its shape. In reality however, the wanted signal may be accompanied by a large interferer in an adjacent channel, and the local oscillator exhibits finite phase noise. when the two signals are mixed with the LO output, the down converted band consists of two overlapping spectra, with the wanted signal suffering from significant noise due to tail of the interferer. This effect is called "reciprocal mixing."

Shown in Figure 4.9 the effect of phase noise on the transmit path is slightly different. Suppose a noiseless receiver is to detect a weak signal at ω_2 while a powerful, nearby transmitter generates a signal at ω_1 with substantial phase noise. Then the wanted signal is corrupted by the phase noise tail of the transmitter.

The effect of phase noise on the transmit path is slightly different (Figure 4.9). Suppose a noiseless receiver is to detect a weak signal at ω_2 while a powerful, nearby transmitter generates a signal at ω_1 with substantial phase noise. Then, the wanted signal is corrupted by the phase noise tail of the transmitter [9].

The important here is that the difference between ω_1 and ω_2 can be as small as few tens of kilohertz while each of these frequencies is around 900 Mhz or 1.9 GHz. Therefore, the output spectrum of the LO must be extremely sharp. In the North American Digital Cellular (NADC) IS54 system, the phase noise power per

unit bandwidth must be about 115 dB below the carrier power (i.e.,-115 dBc/Hz) at an offset of 60 kHz. MEMS oscillator has a phase noise characteristics as shown in Figure 4.22. As it can be seen from the graph simulation results gives a -117.6 dBc/Hz of phase noise which shows that the oscillator requires the standard set by NADC.

Oscillators were designed for a center frequency of approximately 500 kHz which is the resonance frequency of the micro resonator. Each circuit were simulated in the time domain and the output was processed in MATLAB to obtain its power and angle spectrum. Figure 4.23 and 4.24 show frequency spectrum of the oscillator.

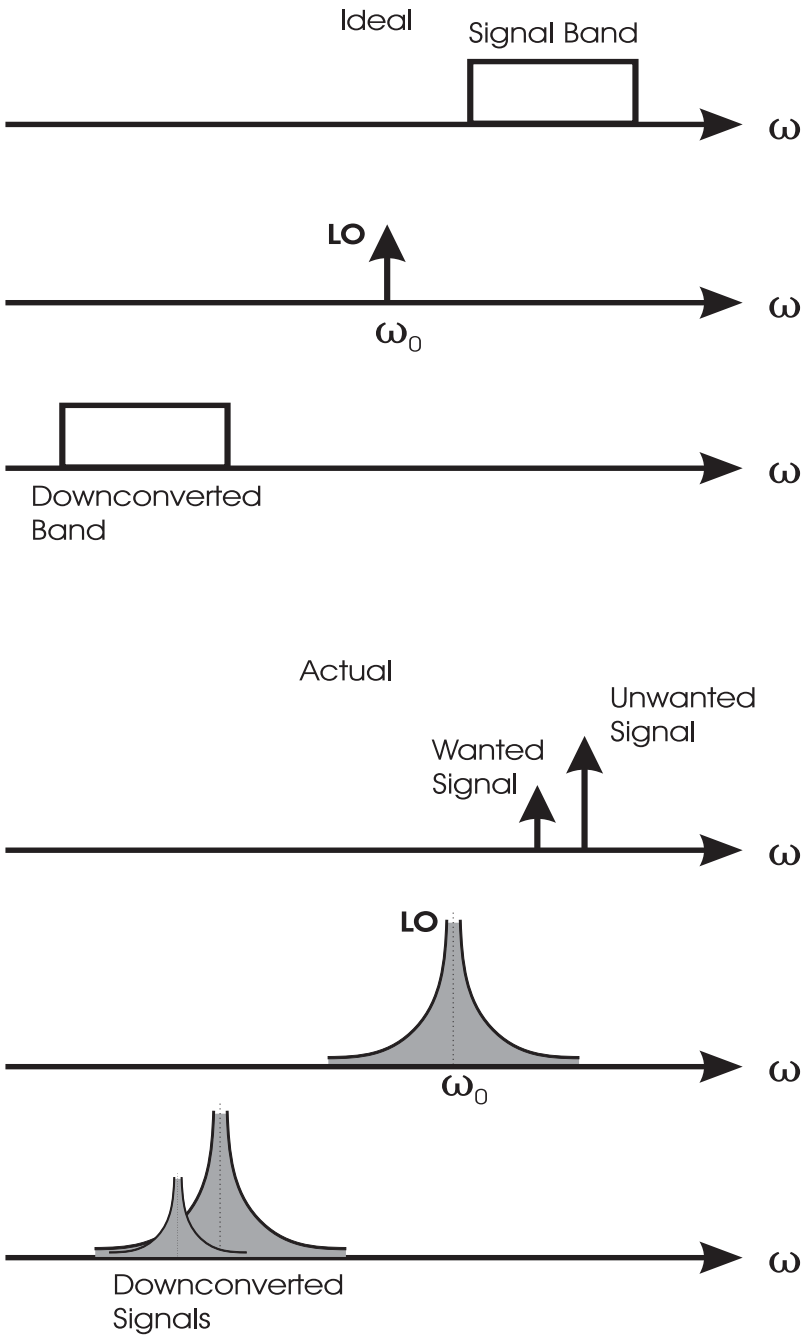


Figure 4.20: Effect of phase noise on receive path.

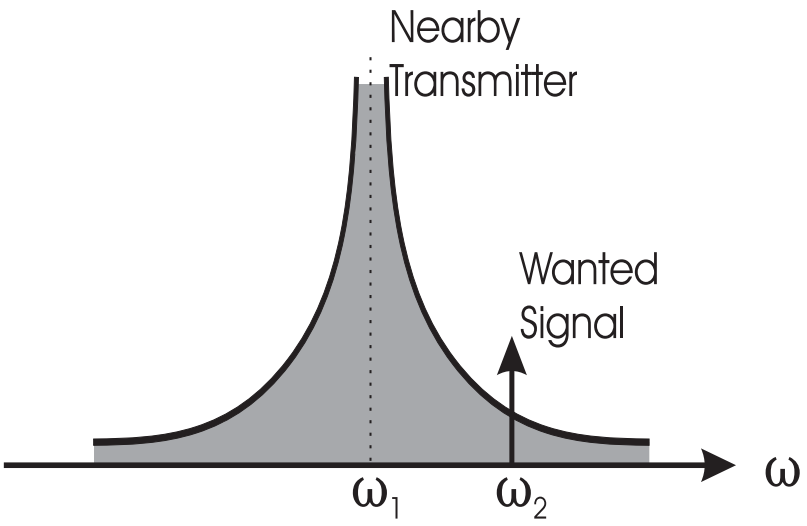


Figure 4.21: Effect of phase noise on transmit path.

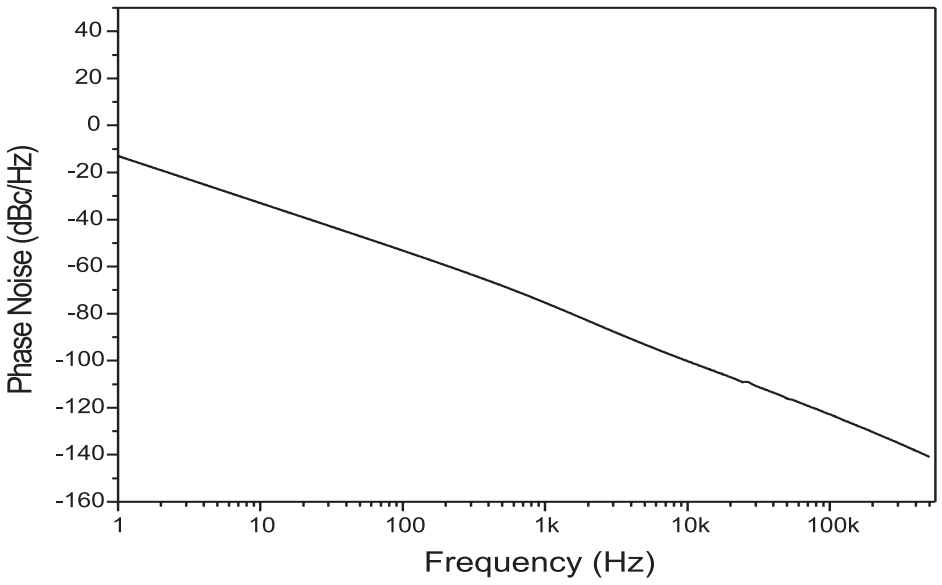


Figure 4.22: Phase noise for the circuit shown in Figure 4.7

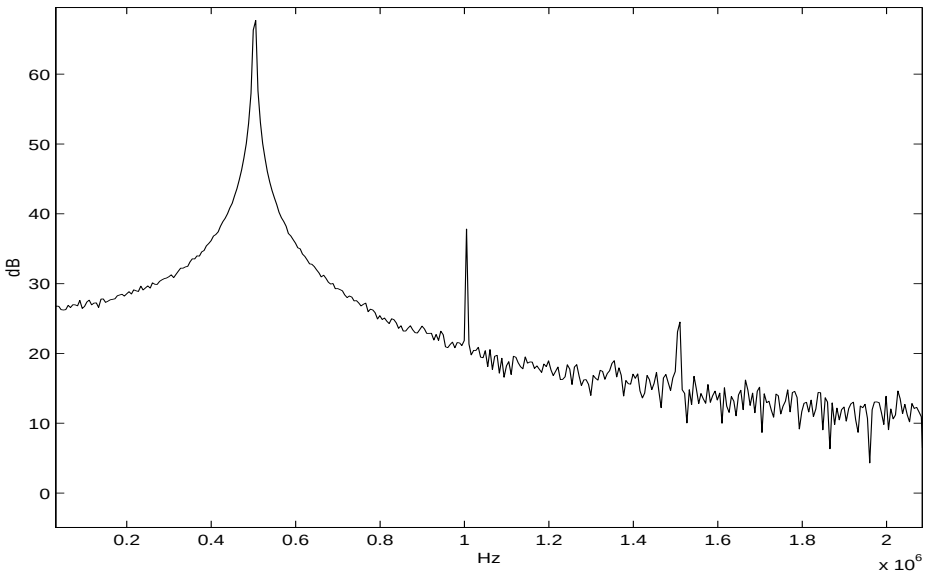


Figure 4.23: Power spectrum of the oscillator output operating at 500 kHz

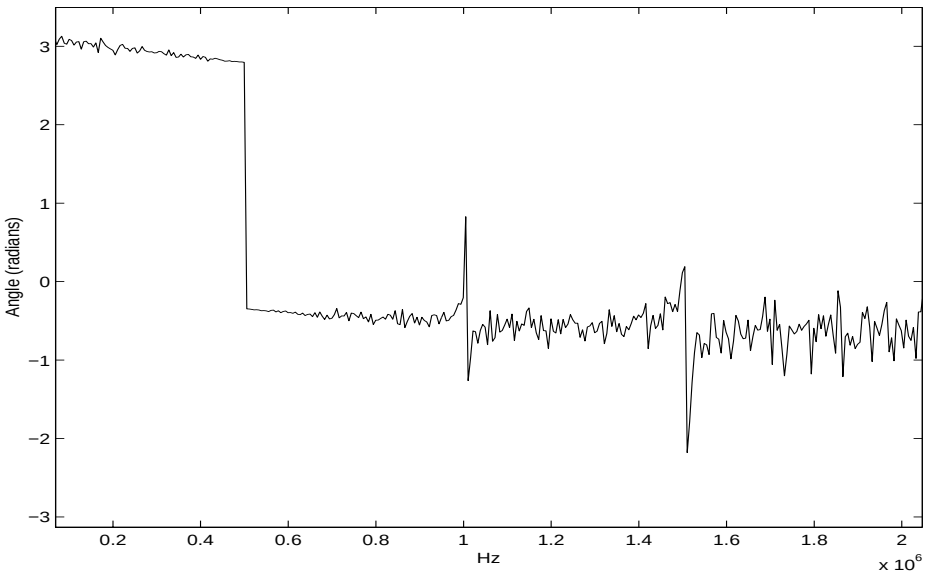


Figure 4.24: Angle spectrum of the oscillator output operating at 500 kHz

Chapter 5

Conclusions

This theses presents design and simulation of MEM resonator based oscillator. A fully monolithic high-Q oscillator, with oscillation frequency referenced to a micro mechanical resonator, and with oscillation sustained by active CMOS electronics is investigated. The operating frequency is dependent upon the constituent resonators which can be replaced with alternative designs for higher frequencies. The central issue of phase noise and oscillation stability is addressed for 500kHz oscillator. However, for higher central frequencies, the noise figure of sustaining amplifier will require minimization.

Such oscillators' performances are good enough for low frequencies. But are they still show good performances at higher frequencies? What the micro mechanical performance will be at higher frequencies is still unclear and is certainly a question ripe for further research. Other problems for MEM based oscillators are phase noise and packaging. Because resonator has high-Q in vacuum. Packaging of MEMS resonator to create vacuum ambient is important. Phase noise is second problematic issue and caused by mass loading noise of MEM resonator and flicker, thermal noise of the CMOS electronics. Phase noise performance can be improved by low noise design of op-amps and less mass loading noise of the resonators. All of these problems need further research in the future.

Since oscillator requires a sustaining amplifier, three different sustaining amplifier designed. Op-amps as a sustaining amplifier are analyzed in terms of their characteristics. They optimized to obtain better oscillations. Important op-amp characteristics are bandwidth, gain and phase margin. All of the mentioned parameters present trade off. Therefore the design needs careful attention.

To summarize a micro mechanical resonator based oscillator is presented. Design of sustaining electronics is also given. Fabricating MEM based resonator and sustaining electronics will enable us to build an oscillator on a single chip. This technology show much promise for one day being one of the component of compact, inexpensive, high performance communication devices.

Appendix A

Layouts

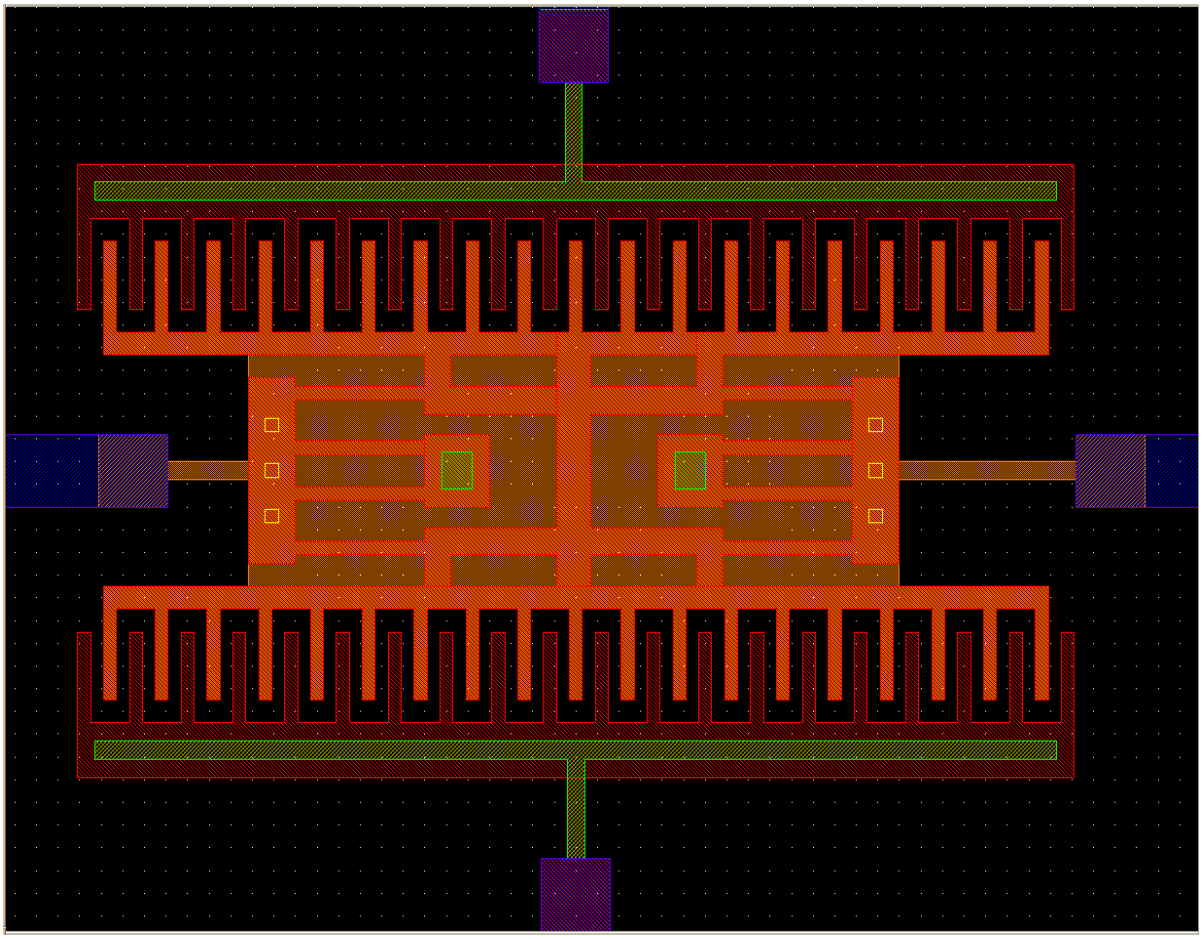


Figure A.1: Mask layout of the electrostatic comb drive

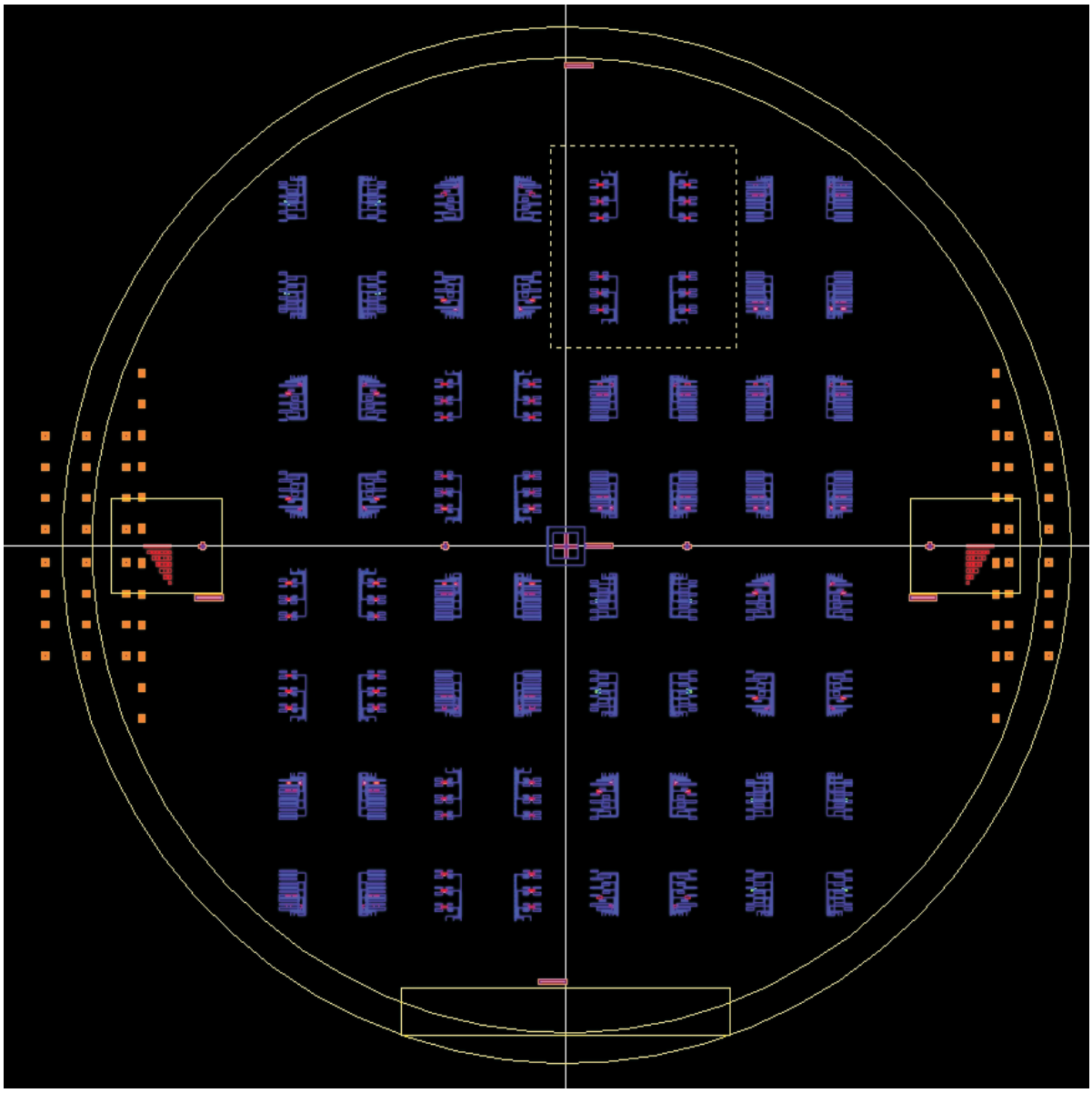


Figure A.2: Complete Mask layout of the electrostatic comb drives and Filters

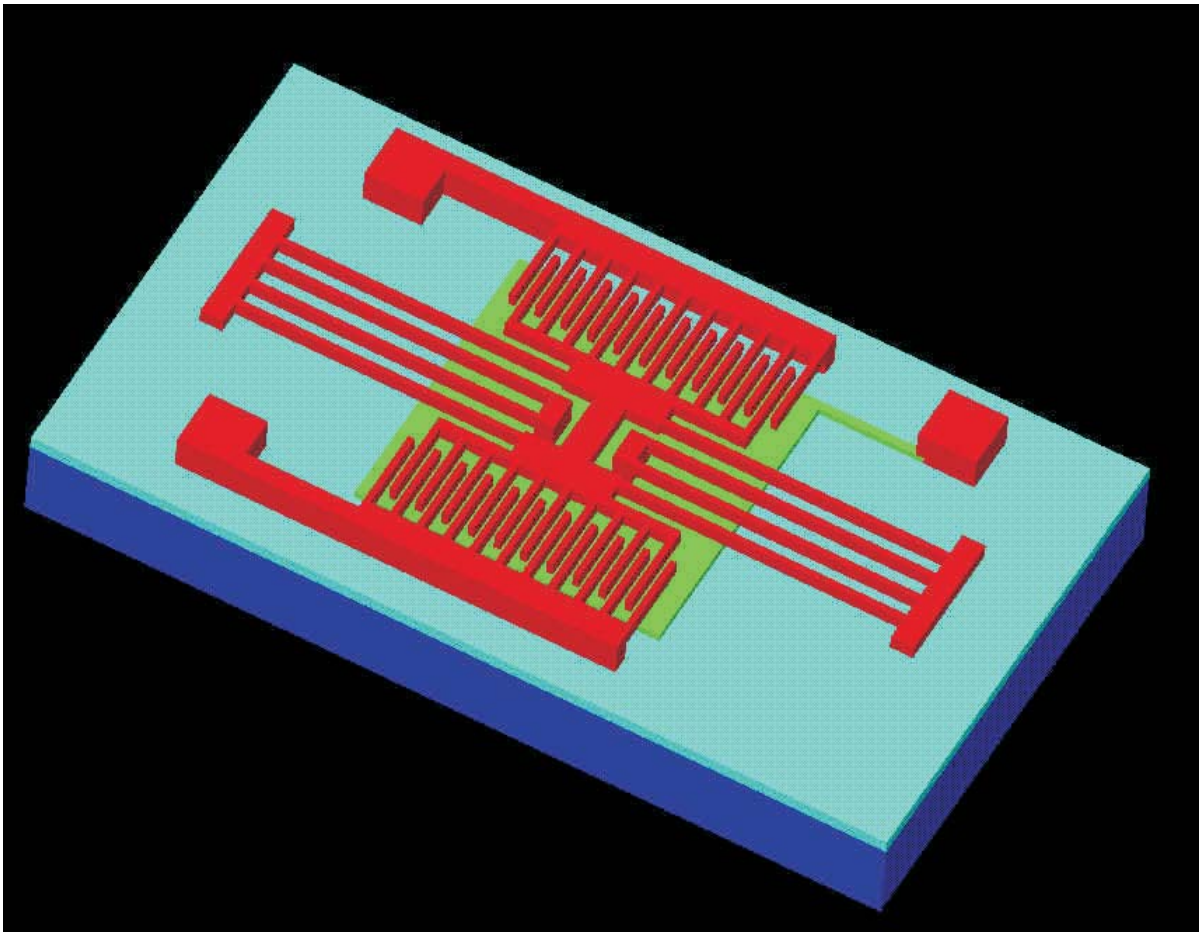


Figure A.3: 3-D view of the electrostatic comb resonator. 3-D view is produced by MEMCAD®

Appendix B

Opamp characteristics

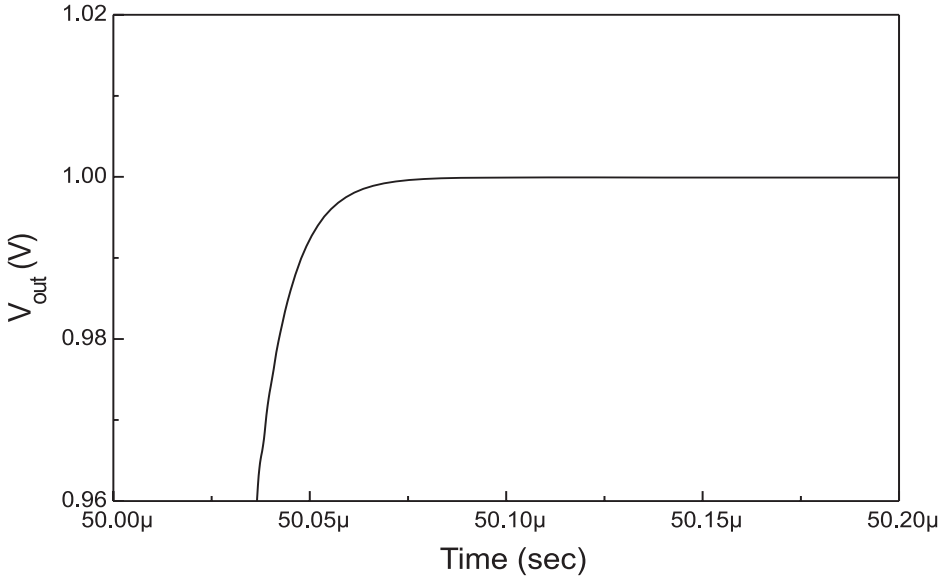


Figure B.1: Settling for R=4kΩ phase margin = 29.7

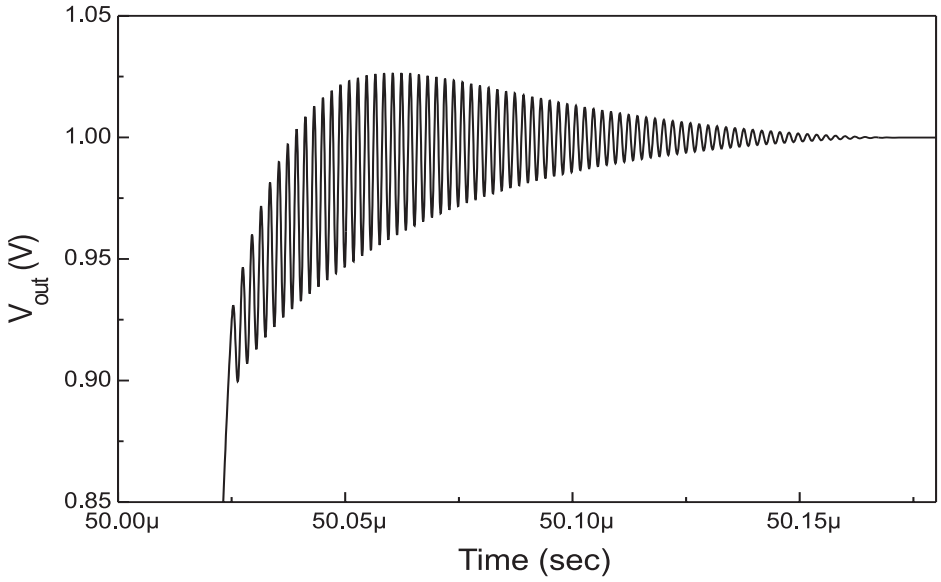


Figure B.2: Settling for R=7kΩ phase margin =179

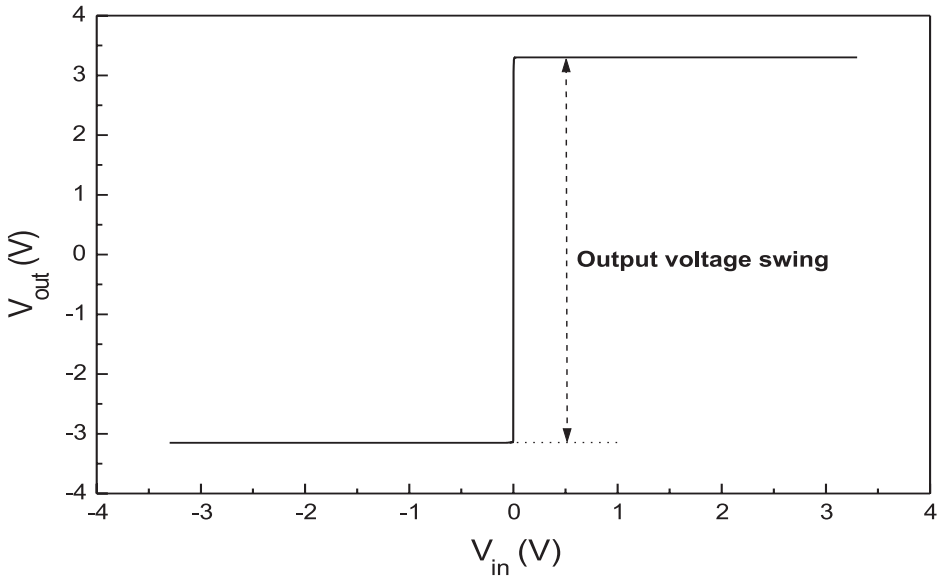


Figure B.3: Output voltage swing of the folded cascode op-amp

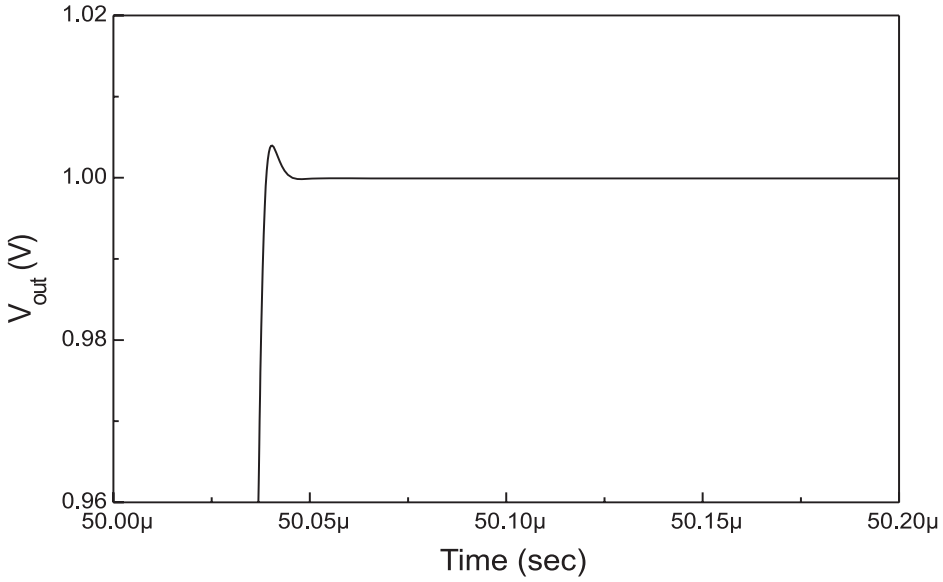


Figure B.4: Settling for R=1kΩ phase margin = 72

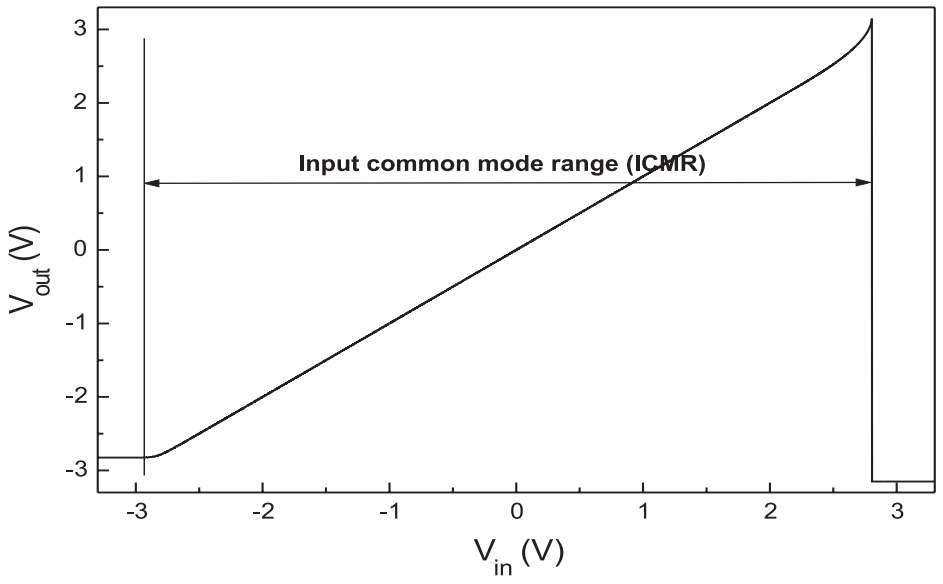


Figure B.5: Input Common Mode Range

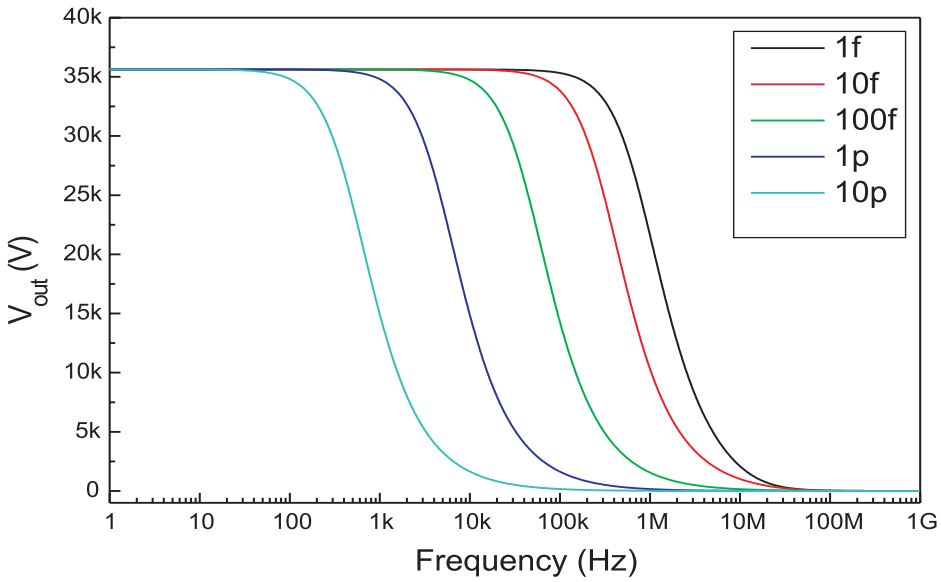


Figure B.6: Effect of compensation C on magnitude response of the folded cascode opamp

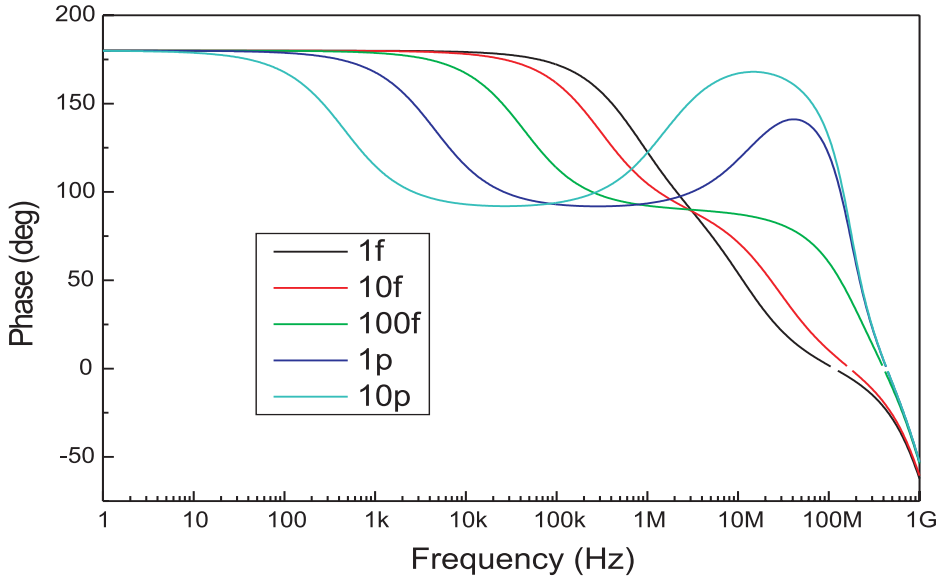


Figure B.7: Effect of compensation capacitor on the phase response of the folded cascode op-amp

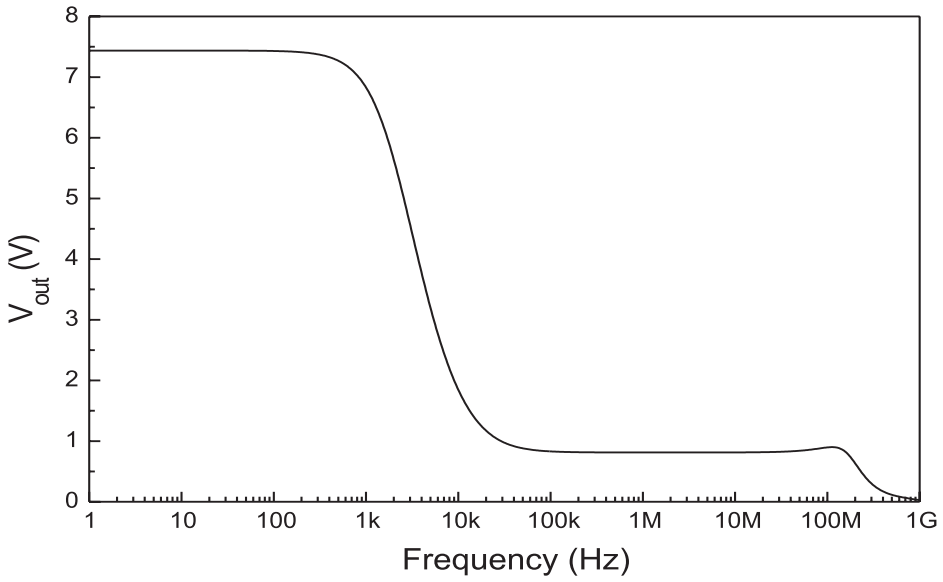


Figure B.8: Negative power supply rejection ratio PSRR-

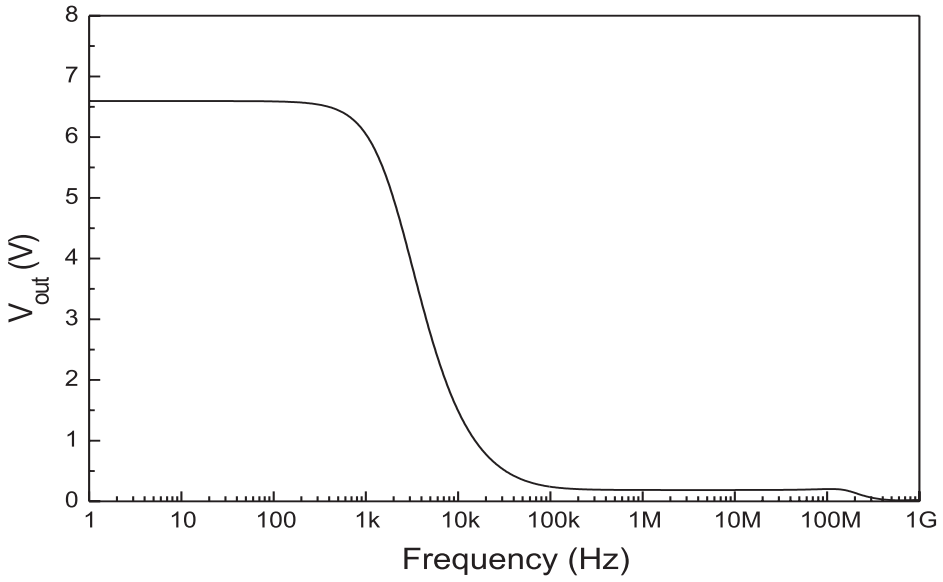


Figure B.9: Positive power supply rejection ratio PSRR+

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