

A Coplanar Waveguide On-chip RF Choke for WLAN RF Circuits

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Abstract — A novel on-chip RF choke at 5 GHz is designed and measured for a class A operating Wireless LAN RF power amplifier (PA). The coplanar waveguide (CPW) based on-chip RF choke is implemented as an alternative component to inductors provided by the 0.35 μm SiGe BiCMOS technology. The CPW RF choke is designed at 5 GHz, and has a length of 1600 μm and loaded with a capacitance of 0.95 pF. The measured impedance of the RF choke at 5 GHz is around 104 ohms.

Index Terms — **On-chip RF choke, Transmission Line, Coplanar Waveguide.**

I. INTRODUCTION

In any class of RF power amplifier (PA) circuit, an RF choke is used to separate DC and RF parts of the circuit. The spiral inductors provided by the RFIC technologies are employed as mainly RF chokes in typical PA circuits [1-4]. Traditionally, quarter wave transmission lines are used as off-chip RF choke inductors; however, the size is a concern for these inductors to be placed on-chip [5-6]. In this paper, capacitively loaded CPW based RF chokes are presented as on-chip components, and the performance of these RF chokes are investigated in terms of impedance level, quality factor and chip area occupied. Recently, SiGe HBT power amplifiers are emerging as a contender for RF power amplifier applications at higher frequencies. However, SiGe devices capable of operating at 5 GHz have a low collector-emitter breakdown voltage, making it difficult to extract high output power from a single transistor. An RF choke with a large value of inductance is connected at the collector of the transistors and is used to feed DC power to the collector. In this study, the RF choke inductor is replaced by an on-chip CPW based RF choke. RF choke must have a comparatively large inductance in order to act as an open circuit at high frequencies (by showing high impedance at RF), thus isolating the RF signals from DC.

The organization of the rest of the paper will be as follows: in Section II, the theory of using short circuited transmission line will be presented, followed by a design example of a capacitively loaded CPW RF choke in Section III. Simulation and measurement results will be presented in section IV, and finally the paper will be concluded.

II. SHORT CIRCUITED TRANSMISSION LINE

The impedance of an inductor based RF choke can be easily calculated as

$$Z_L = j2\pi fL \quad (1)$$

where f is the frequency of operation and L is the inductance in Henries. Thus, if the operating frequency is 5 GHz, the impedance of an RF choke of 5 nH is calculated to be $j157 \Omega$ using Eqn. (1). For a

reference impedance of 50 Ohms, an impedance value of 100-150 Ohms will be large enough to be used as an RF choke. Instead of an inductor based RF choke, one can also use a transmission line section terminated with a short circuit as a high impedance component. For a transmission line of length l , terminated with Z_l , the input impedance seen at the source terminal is given by

$$Z_{in} = Z_0 \frac{Z_l + jZ_0 \tan(\beta l)}{Z_0 + jZ_l \tan(\beta l)} \quad (2)$$

where Z_0 is the characteristic impedance of the transmission line and β is the propagation constant, $\beta = 2\pi / \lambda_g = \omega / v_p$. If the transmission line is terminated with a short circuit, i.e., $Z_l = 0$, then (2) can be simplified to

$$Z_{in} = jZ_0 \tan(\beta l) \quad (3)$$

In order to use a short circuited transmission line section as an RF choke, Z_0 should be high and βl should be close to $\pi / 2$. Usually, in RF circuits, a high valued inductor is used as an RF choke, which has a very small resistance at DC and very high impedance at the desired RF frequency, and hence the inductor is called RF choke, [3-5]. However, it is not always necessary for an RF choke to be an inductor. Different components can provide the same characteristic as the RF choke as long as the component has small impedance at DC, and very high impedance at the desired RF frequency. The impedance of the short circuited transmission line is very small at DC since βl has diminishing values, and if βl is set to $\pi / 2$, then Z_{in} , the input impedance, will reach high values.

As seen in Fig. 1, the normalized input impedance is plotted versus the electrical length where one can see that if the βl is chosen around $\pi / 2$, the normalized impedance reaches very high values. Actually, for an RF choke to be used in an RF circuit, it should be at least larger than Z_0 , and in Fig. 1, these points correspond to $\beta l = \pi / 4, 3\pi / 4$ which also defines the operation bandwidth of the RF choke. The transmission line RF choke bandwidth is given by the difference between the two end points, which is

$\pi/2$. Since βl is close to $\pi/2$, this means the RF choke has 100 % fractional bandwidth. In other words, if the center frequency of the RF choke design is 5 GHz, a bandwidth of 5 GHz around the 5 GHz center frequency will be accessible for the RF choke.

III. CPW RF CHOKE DESIGN EXAMPLE

Due to size limitations, most of the RF chokes in RF circuits are implemented as off-chip components. When we look at our example of a transmission line based RF choke at 5 GHz, the main concern is the size of the transmission line. If we use a coplanar waveguide (CPW) as the transmission line, CPW line can be simulated as transmission line via Advanced Design System (ADS) tool in order to find out the required length. Note that back of the envelope calculations is possible for the transmission line length; however, this will not be as precise as the simulation results. (One can simply take the line length $\lambda_g / 4$ as a rough approximation). Assume that a 3-5 nH valued RF choke inductor will have considerably high impedance at 5 GHz, we can find out what the required length of the CPW transmission line is. Since we are designing with a specific technology, SiGe BiCMOS, the process parameters dictate our CPW line parameters as follows: Substrate thickness (total oxide thickness) is set to 6.5 μm , ϵ_r (relative dielectric constant) is set to 4.1, T (conductor thickness) is set to 3 μm and TanD (dielectric loss tangent) is set to 0.001. We assume no conductor losses for this part of the simulation (conductivity is set to $1\text{e}15$). The length and the width of the coplanar waveguide sections are set to 6000 μm and 10 μm , respectively. The gap, which is the spacing between the center and the ground plane conductors, is set to 35 μm . The short circuited CPW line input impedance is calculated as $j146\Omega$, which corresponds to an inductance value of 4.66 nH, which is shown in Figure 2. Note that the simulated impedance is obtained as the impedance of the short circuited CPW whose characteristic impedance and the phase velocity is determined via a model given in ADS tool.

The required length of the CPW line is 6 mm, rather long for an on-chip placement. One of the ways to make the CPW line shorter without sacrificing from its performance is to load the CPW with discrete

capacitances. Keeping in mind that the transmission line lumped element model is the combination of distributed series inductors and parallel capacitors, by loading the CPW transmission line with additional discrete parallel capacitances, one can increase the total capacitance of the transmission line. The varactor loaded transmission line is called nonlinear transmission line and it is used for ultra wide band pulse generation and pulse shaping circuits [7-9]. The additional capacitances will increase the propagation constant and decrease the phase velocity of the wave propagating on the CPW line. In this way, the length of the transmission line can be shortened to obtain the desired phase shift/time delay. As illustrated in Figure 3, the CPW line is loaded with parallel discrete capacitances at three different points. The same layered structure is used for the coplanar waveguide substrate; however, the total CPW length for the capacitively loaded line is shortened to 400 μm from 6 mm. For this case, an impedance of $j147\ \Omega$, which corresponds to an inductance of 4.67 nH is obtained with a much shorter CPW line.

One possible drawback of using capacitive loading may be to worsen the quality factor of the short-circuited CPW line. We can investigate the Q factor of the CPW line by introducing realistic losses for the signal and ground conductors of the CPW and re-simulate with more realistic coplanar waveguide conductor characteristics. Using SiGe BiCMOS technologies, CPW structure was realized using thick upper layer (MET4) for the signal and ground lines of the CPW and typical electrical conductivities (available for this technology) for the top conductor is used in our simulations. We modified the capacitive loaded CPW model example which is given in Figure 4. The new version of this model with more realistic conductor conductivity is simulated and the input impedance of the short-circuited line is calculated to be $50*(1.12 + j*0.436)$. The magnitude of the impedance dropped to 60 Ω and the quality factor which is the ratio of imaginary part of the impedance to real part of the impedance is around 0.39. As a result, adding capacitance shrinks not only the size of the CPW RF choke, but also lowers the impedance level, which is the trade-off between the impedance level and the size of the CPW RF choke. However, the high value of the impedance should still make the short-circuited CPW line be used as an RF choke in RF circuits.

IV. EXPERIMENTAL RESULTS

For simulations, Agilent Design Systems ADS2006A and Cadence Hit-Kit 3.71 are used. The layouts are implemented using 0.35 μm SiGe BiCMOS technology. The impedance measurements are performed using Agilent 8720 ES Network Analyzer, with Carl Suss probe station. To be used as an RF choke, a short circuited CPW line loaded with only one capacitor is simulated and tested. In Figure 4, a modified CPW with a length of 1600 μm , gap of 15 μm and width of 10 μm connected in parallel with a capacitor of 1.19 pF is shown. A magnitude of impedance of 140 Ω ($50*(2.11+j*1.85)$) is obtained by using a single capacitor and extending the length of the CPW. Instead of having multi section CPW line loaded with multiple capacitors, one section CPW line with only one capacitor is first simulated and the results are obtained.

As given in Figure 5, this CPW structure provides an inductance of about 3 nH at 5 GHz. However, the quality factor is not exceeding 1. To explain the role of RF choke one can look at a theoretical component which has a zero resistance at DC and a very large pure resistance (1 K Ω) at the desired RF frequency. This component has a quality factor of zero, but it can be used as an RF choke since it represent very large impedance at the RF. Keeping all parameters the same except the Gap (G) width of the coplanar waveguide and the shunt capacitance, higher inductance values can be obtained while trading off the quality factor. This is possible by increasing the Gap width from 15 μm to 30 μm and reducing the capacitance from 1.19 pF to 0.95 pF. The simulation results of this structure are given in Figure 6. An impedance of $50*(3.0+j*3.2)$ is obtained, which corresponds to an inductance of 5 nH.

The layout of the CPW RF choke is given in Figure 7. In the layout, the CPW line has a 10 μm wide signal line and a gap length of 30 μm from the ground lines, the ground lines have a width of 60 μm and connected by the bridges at 8 points. The capacitance of 0.95 pF was realized as metal/insulator/metal (MIM) capacitors. The die size is 300*300 μm^2 including the bias pads. In Figure 8, the impedance of the RF choke is plotted on a Smith Chart. The locus of the RF choke impedance for both simulation and

measurements are very similar, Figure 6.a and Figure 8. The simulations resulted in an impedance of 150 ohms, and measured input impedance is around 104 ohms at a frequency around 5 GHz. From these impedances at Smith chart, it is seen that these two impedances are very close to each other. The difference may be the schematic simulations of the CPW structures as well as the finite width of the ground lines (in simulations, these lines are assumed to be infinite). In simulations, the CPW line is taken as one straight transmission line, however, in the layout, the CPW line is bent in the shape of U to save layout space.

V. CONCLUSION

In this paper, we presented the design of a CPW based RF choke as an alternative to the inductors provided by the 0.35 μm SiGe RFIC technology. As a design example, a 1600 μm length CPW loaded with a 0.95 pF capacitance is given as equivalent impedance to a 5 nH inductor. This CPW based RF choke is implemented using 0.35 μm SiGe BiCMOS technology and 104 Ohms impedance is measured at 5 GHz. The capacitively loaded CPW line has a high impedance at RF and very low impedance at DC and can be used as an RF choke in RF circuits.

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FIGURES

Fig. 1. Normalized impedance of a short circuited line versus the electrical length βl

Fig. 2. a) CPW line simulation set-up b) Input impedance on Smith Chart

Fig. 3. Capacitively loaded coplanar waveguide model

Fig. 4. Modified CPW structure

Fig. 5. a) Impedance on Smith Chart b) Inductance of the CPW structure vs. frequency

Fig. 6. a) Impedance on Smith Chart b) Inductance of the CPW loaded with Capacitance

Fig. 7 Coplanar waveguide based capacitively loaded RF choke

Fig. 8. Input impedance of coplanar waveguide based capacitively loaded RF choke

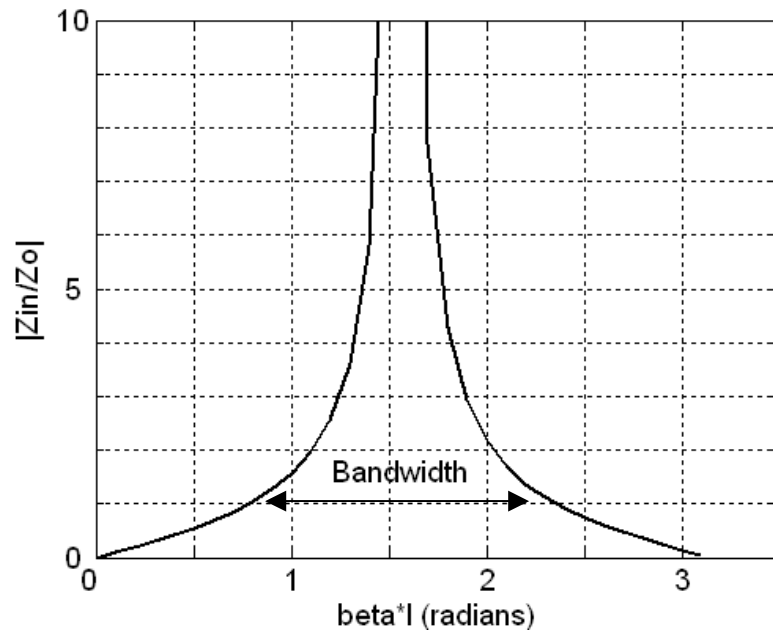
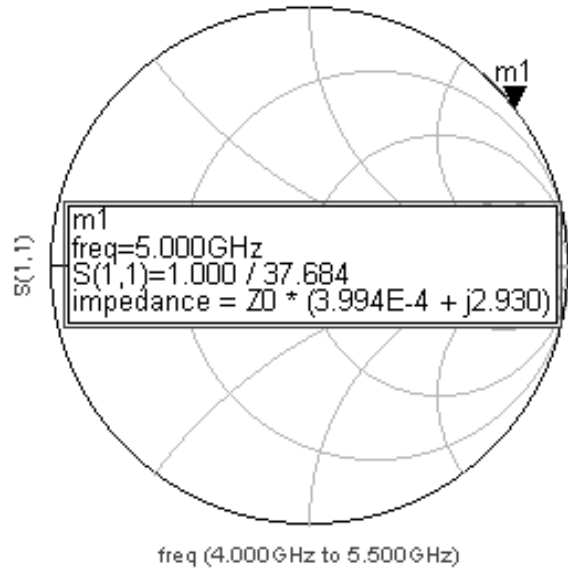
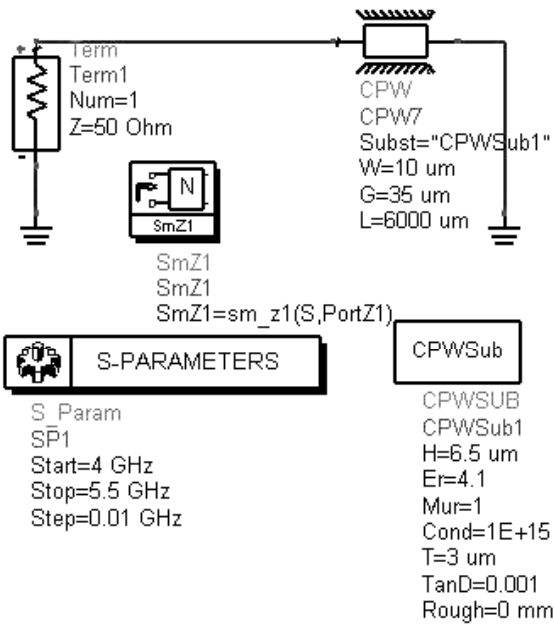


Fig. 1. Normalized impedance of a short circuited line versus the electrical length βl



(a)

(b)

Fig. 2. a) CPW line simulation set-up b) Input impedance on Smith Chart

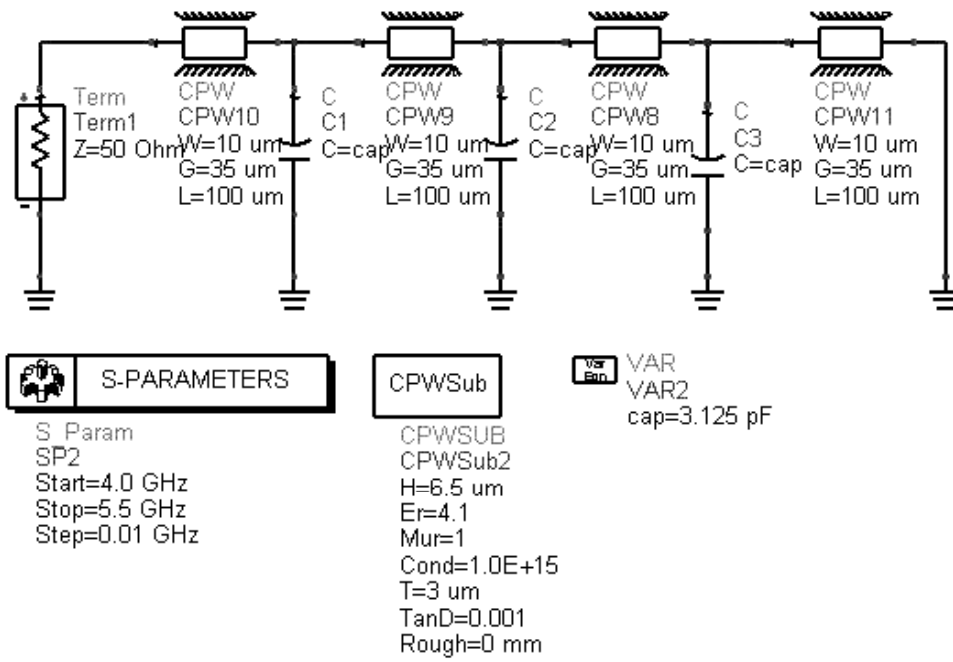


Fig. 3. Capacitively loaded coplanar waveguide model

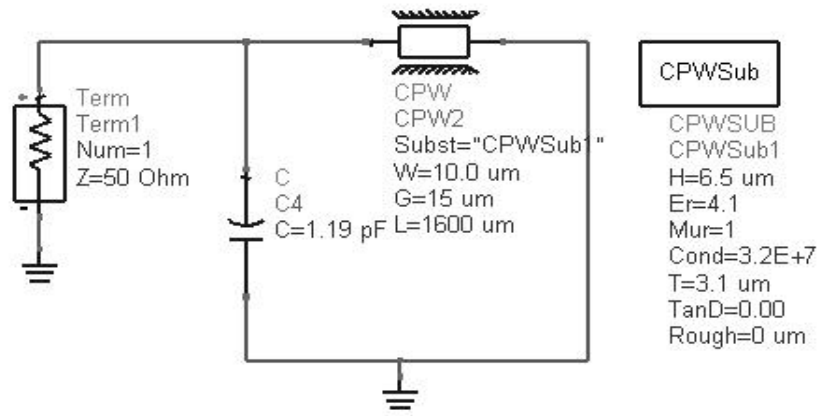
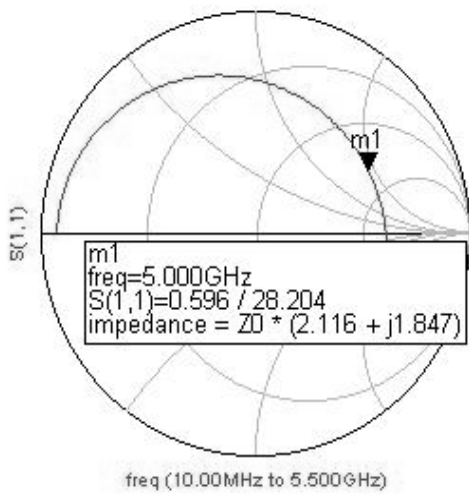
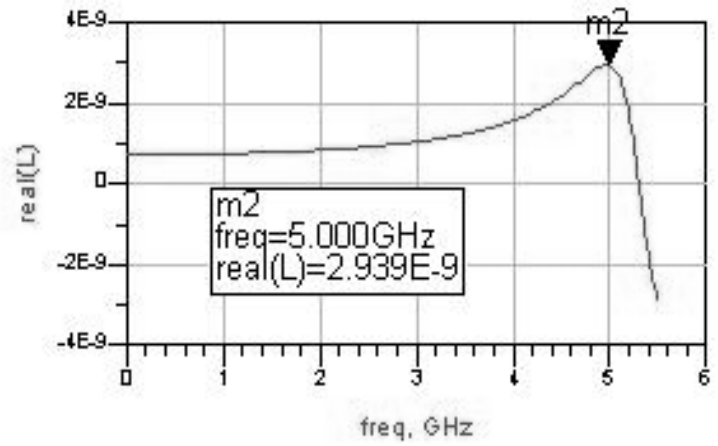


Fig. 4. Modified CPW structure

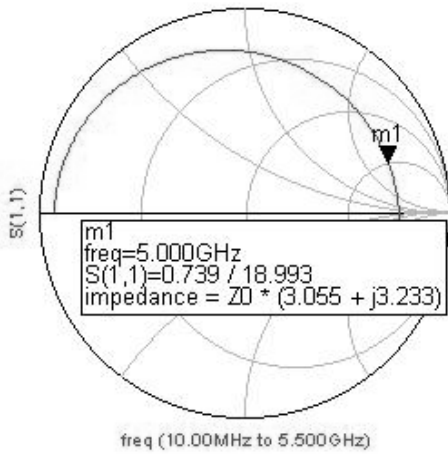


(a)

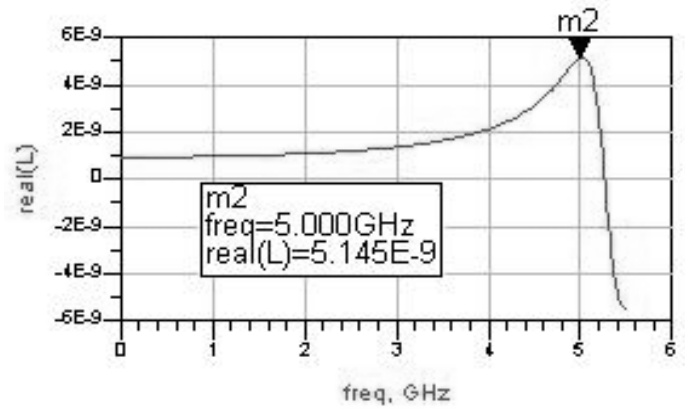


(b)

Fig. 5. a) Impedance on Smith Chart b) Inductance of the CPW structure vs. frequency



(a)



(b)

Fig. 6. a) Impedance on Smith Chart b) Inductance of the CPW loaded with Capacitance

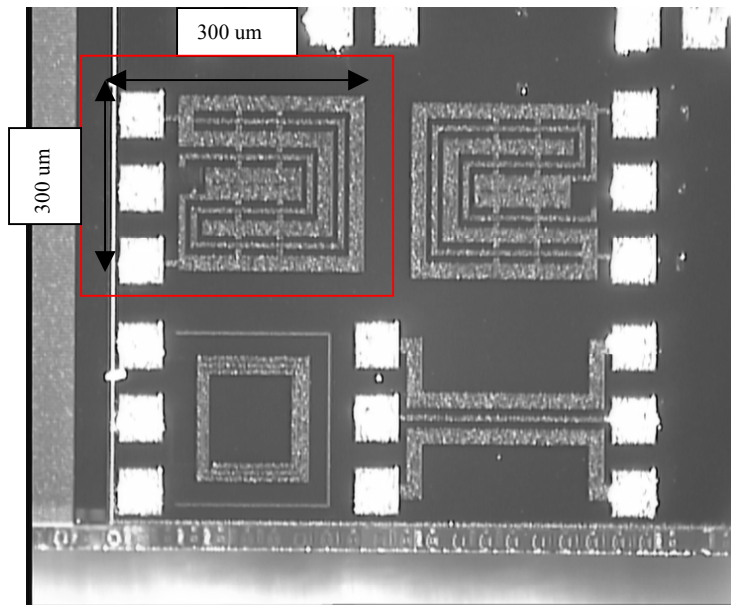


Fig. 7 Coplanar waveguide based capacitively loaded RF choke

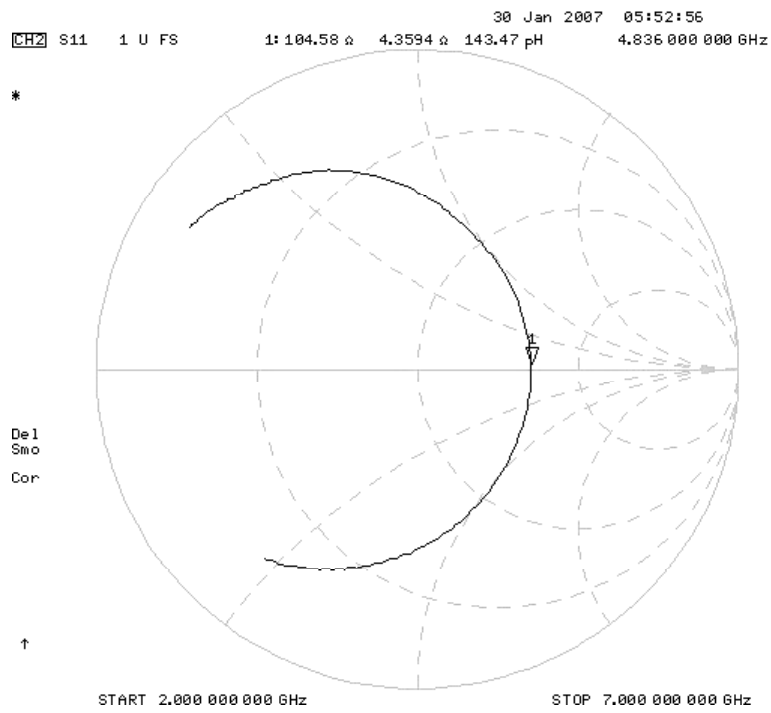


Fig. 8. Input impedance of coplanar waveguide based capacitively loaded RF choke