REDEFINING PASSIVE ELECTRONICS ON RFICS VIA STRESS-INDUCED RESTRUCTURING OF PATTERNED THIN FILMS

by
RAYAN BAJWA

Submitted to the Faculty of Engineering and Natural Sciences
in partial fulfilment of
the requirements for the degree of Doctor of Philosophy

Sabanci University
July 2023

ABSTRACT

REDEFINING PASSIVE ELECTRONICS ON RFICS VIA STRESS-INDUCED RESTRUCTURING OF PATTERNED THIN FILMS

RAYAN BAJWA

Ph.D. Thesis, July 2023

Thesis Supervisor: Prof. Dr. Murat Kaya Yapıcı

Keywords: Electrostatic actuator, RF-MEMS switch, thin film, residual stress, bending, bilayer, 3D wavy cantilevers, Microfabrication, Polymer encapsulation, Wafer-level packaging, Microelectromechanical devices, RF-MEMS, Inductor, Q-factor

Manufacturing three dimensional (3D) structures at microscale has been a major challenge in semiconductor fabrication, which heavily relies on planar layer by layer processing of materials. This essentially restricts the geometry of any electronic component to be built on-chip to two dimensions, often at the expense of extreme performance degradation. For instance, passive elements such as inductors or transformers when fabricated monolithically on integrated circuit (IC) chips need to be shape-modified from conventional 3D solenoidal shape to planar two-dimensional spiral shape. While this approach allows easy integration, passive elements built on-chip often suffer from significant reduction in performance compared to their 3D, mm-scale, discrete counterparts.

Aiming to overcome these issues, this thesis herein puts forward a novel IC-compatible technological platform to fabricate complex 3D shapes monolithically on IC chips, thereby opening up new opportunities for the semiconductor industry to explore. We show that residual stresses that are commonly observed in metal thin films used in IC fabrication can be indeed leveraged to achieve controllable out-of-plane bending, thus indicating a pathway to build complex 3D shapes at microscale. Fundamentally, stacking two thin film layers with different residual stress values can lead to bending in either upward or downward direction, once the film stack is released from the substrate. By utilizing this fundamental concept, we have built the 3D variants of two types of electronic components commonly used in radio-frequency circuits i.e., inductors and electromechanical switches. We show that shape modification via stress engineering allows maneuvering the device geometry in three dimensions, hence liberating an additional degree of freedom in the device design process and allowing a better performance optimization, as opposed to traditional 2D-restricted designs. Specifically, our 3D inductors show approximately 300% performance improvement (quantified using quality factor) compared to planar coils. Similarly, RF switches fabricated using the proposed methodology operate at 4 times lower actuation voltage and exhibit 5x better isolation, in comparison with devices available in market. In general, the devices we fabricated outperform the commercial state-of-the-art by a large margin, and these performance improvements are crucial for realizing future high data-rate wireless networks.

In addition, while we have shown the application of proposed technology to only two types of electronic components, the platform is highly scalable and can easily accommodate other components such as capacitors or transformers etc. As such, we believe our efforts indicate an important landmark towards the implementation of high-performance on-chip RF passive devices that are essential for next generation communication systems.

ÖZET

PASİF RFIC ELEKTRONİĞİNE İNCE FİLMLERİN GERİNİM KONTROLLÜ ŞEKİLLENDİRİLMESİYLE YENİ BİR BAKIŞ

RAYAN BAJWA

Doktora Tezi, Temmuz 2023

Tez Danışmanı: Prof. Dr. Murat Kaya Yapıcı

Anahtar Kelimeler: Elektrostatik eyleyiciler, RF-MEMS anahtar, İnce film, Kalıntı gerinim, Eğilme, Çift tabaka, 3B dalgalı kirişler, Mikrofabrikasyon, Polimer enkapsülasyonu, Altlık seviyesinde paketleme, Mikroelektromekanik aygıtlar, RF-MEMS, İndüktör, Q-faktörü

Üç boyutlu yapıların (3B) mikro ölçekte fabrikasyonu, malzemelerin genellikle katman katman işlendiği yarı iletken teknolojisi için hep bir zorluk oluşturmuştur. Çip üstü elektronik bileşenlerin geometrisini iki boyutlu bir düzlemde kısıtlayan bu durumun, performans üzerinde ciddi bir etkisi olabilmektedir. Entegre devre (IC) çipleri üzerinde monolitik olarak üretilen indüktör veya transformatör gibi bobin elemanlarının klasik üç boyutlu selenoid şeklinden düzlemsel iki boyutlu spirallere dönüştürülmesi gerekliliği buna bir örnektir. Tümleşimleri daha kolay olsa da, bu yaklaşımla üretilen pasif bileşenler üç boyutlu (3B), milimetre üstü, muadillerine kıyasla performanslarında önemli eksiklik gösterir.

Bu sorunun üstesinden gelmek amacıyla, bu çalışmamızda, karmaşık 3B şekillerin entegre devre uyumlu monolitik üretimleri için yeni bir teknolojik platform

geliştirilmiştir. Entegre devre üretimindeki metal ince filmlerin üzerinde yaygın olarak gözlemlenen gerinimlerin, düzlem dışı bükülme elde etmek için kontrol edilebilir şekilde kullanılabileceği ve böylece mikro ölçekte karmaşık 3B şekiller oluşturulabileceği gösterilmektedir. Temel yaklaşımımız, farklı kalıntı gerinim değerlerinde üst üste getirilen iki ince film katmanının altlık yüzeyinden ayrıldıktan sonra yukarı veya aşağı yönde bükülmesine dayanmaktadır. Buradan hareketle, radyo frekans devrelerinde yaygın olarak kullanılan iki tür elektronik bileşenin, indüktörlerin ve elektromekanik anahtarların 3B varyantları oluşturulmuştur. Gerinim kontrolü sayesinde aygıt geometrisiyle üç boyutta oynayabilmenin, tasarım sürecinde ek bir serbestlik derecesi getirdiğini ve geleneksel tasarımlara göre daha iyi bir performans optimizasyonunu mümkün kıldığı gözlenmiştir. Özellikle, üretilen 3B indüktörler düzlemsel muadillerine karşı neredeyse 3 kat daha yüksek Q-faktörü göstermiştir. Ayrıca önerdiğimiz metodla üretilen RF anahtarlar, ticari ürünlere kıyasla 4 kat daha az çalıştırma voltajı ve 5 kat daha iyi izolasyon sergilemektedir. Mevcut ticari ürünlere kıyasla gösterilen bu önemli performans farkları, geliştirilen sensörlerin yüksek hızlı kablosuz ağ uygulamaları için kullanılabilirliğine işaret etmektedir.

Önerilen teknoloji iki farklı türde elektronik bileşene uygulanmış olmakla birlikte, oldukça ölçeklenebilir olan bu yaklaşımın kapasitörler veya transformatörler gibi başka temel bileşenler için de kolayca uygulanabileceği öngörülmektedir. Bu sayede, çalışmalarımızın yansıması olarak yeni nesil yüksek hızlı iletişim sistemleri için kritik olan yüksek performanslı RF bileşenlerin üretimine yönelik mihenk taşı oluşturan kazanımların elde edildiği değerlendirilmektedir.

ACKNOWLEDGEMENT

I am immensely grateful to my supervisor, Dr. Murat Kaya Yapici, for his unwavering guidance, mentorship, and belief in my abilities. His exceptional expertise, dedication, and patience have been instrumental in shaping the direction of my research. His insightful feedback, constant encouragement, and high expectations have motivated me to explore new frontiers and strive for excellence. I am truly fortunate to have had the privilege of working under his guidance, and I am grateful for the trust he placed in me throughout this endeavor.

I would also like to extend my heartfelt appreciation to the members of my thesis committee, Prof. Ibrahim Tekin and Prof. Serhat Yesilyurt, for their valuable insights and thoughtful suggestions that have significantly enriched my research. Additionally, I would like to express my deepest gratitude to my lab mates, whose support made this journey not only intellectually stimulating but also immensely enjoyable. Their insightful discussions, constructive feedback, and shared experiences have been invaluable in shaping my research and personal growth. I am indebted to their friendship, encouragement, and willingness to collaborate, which fostered a vibrant research environment that continuously pushed me to excel.

Last but certainly not least, I owe an immeasurable debt of gratitude to my family. Their unwavering love, unwavering support, and unwavering belief in me have been the foundation upon which I have built my academic journey. Their sacrifices, encouragement, and constant motivation have been the driving force behind my perseverance and success. I am forever grateful for their presence in my life and for the countless ways in which they have nurtured and inspired me.

DEDICATION

Dedicated to my wife for her love and support.

TABLE OF CONTENTs

LIST OF FIGURES

LIST OF TABLES

1. INTRODUCTION

Integrated circuits (ICs) are fabricated using planar processing techniques, where thin material layers are stacked and patterned one by one on top of each other to realize circuitry on semiconductor substrates. While such approach has proven to be highly effective in fabricating densely packed active circuitry (transistors) and achieving extreme miniaturization, this near-2D fabrication flow is not ideal to make passive electronic components such as inductors, transformers, which inherently possess a three-dimensional (3D) shape e.g., solenoid. However, these passive electronic components are an integral part of integrated circuit chips particularly those working at radio frequencies, having applications such as in portable wireless devices, military radars, test and measurement equipment etc. To address this integration issue, researchers over the years have modified the shapes of passive components to better fit them in the conventional 2D IC fabrication flow; for instance, RF coils nowadays have planar spiral shapes. By doing so, though these passive components can be easily integrated with transistors on the same chip, they suffer from a large reduction in their performance. In view of this, there has been a plethora of attempts over the span of past 20-25 years, aiming to develop fully IC-compatible processes that could allow us to build three-dimensional electronic components on the same chip as that of transistors, without affecting the standard IC manufacturing flow. While many interesting results have been published in past [1-4], this 3D component integration problem has not been fully solved, since monolithic integration of 3D components comes with a lot of challenges ranging from compatibility issues to device reliability [5].

Among many strategies that have been explored in the past to monolithically fabricate 3D components on ICs, one viable solution could be on-chip strain-induced shape morphing of patterned thin films by controllably leveraging their intrinsic/residual

stresses. ICs are fabricated by stacking thin films one on top of the other, and by nature, each of these thin films has some stress in it. Though this stress is undesirable in any semiconductor fabrication facility, it is indeed unavoidable. However, we realized that this unwanted stress can in fact become useful, if engineered properly. That is, stacking multiple thin film layers with different amounts of stress can in turn induce out-of-plane bending in the thin film stack in either upward or downward direction. Compared to other approaches for manufacturing out-of-plane structures at microscale such as magnetic field-driven assembly or thick photoresist processing etc., one key benefit of stress-induced bending is that it requires no external stimuli and has relatively simple fabrication [5, 6]. Nevertheless, to effectively utilize this concept in creating 3D shapes on IC chips, it is crucial to first identify IC-compatible thin film materials that also have a large mismatch of intrinsic stress.

In this work, we have demonstrated the use of patterned thin film stacks made of copper and chromium layers that inherently possess a large residual stress mismatch in creating complex 3D shapes [7], where both materials are fully IC-compatible and quite commonly find use in IC fabrication. Through experiments, we observed that evaporated chromium thin films, by nature, possess a large tensile stress at thicknesses below 50 nm, whereas evaporated copper films have a minimal residual stress for thicknesses up to 1 µm. In the early stages, we utilized this residual stress mismatch to fabricate complex out-of-plane shapes, as elaborated in Fig. 1.1, to illustrate the potential of proposed stress-induced restructuring technique (more details are available in Chapter 2). Later, we applied this technique to develop various types of on-chip passive components with 3D shapes for radio frequency applications. In particular, we have extended our stress-engineering concept to accommodate two types of electronic components used in RFICs i.e., inductors and microelectromechanical switches, while it should be noted that the methodology can be easily adjusted to fit other components as well such as transformers and capacitors etc. We show that the devices manufactured using stress-engineering can significantly outperform their standard 2D-shaped counterparts, primarily because of their 3D shape that extends the overall degree of freedom in the device design process.

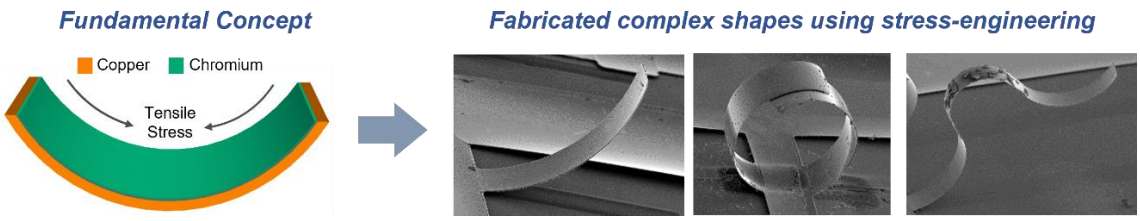

Figure 1.1. Concept of residual stress-induced restructuring technique.

As another contribution of this work, we have introduced the use of machine learning (ML) in optimizing MEMS-based RF electronic components (RF-MEMS), such as the ones fabricated in this work using stress-engineering. Despite the dramatic advent of learning algorithms in almost every engineering domain, their use in aiding the design process of RF-MEMS devices has not been given much importance. To bridge this gap, we have put forward a generic methodology to optimize RF-MEMS devices by leveraging ML techniques. More details on the contributions of this work are provided in the following section.

1.1. Summary of Contributions

1.1.1. Fabrication of High-Performance RF Inductors via Stress-Engineering (Chapter 3)

Planar radio-frequency (RF) on-chip inductors suffer from large electromagnetic losses, stemming from the low resistivity silicon substrate. Though it is well-known that 3-dimensional (3D) MEMS-based RF inductors offer significant performance enhancement by reducing the substrate proximity effects, they are prone to mechanical failures and often come without any appropriate packaging, leading to reliability issues. Herein, we report an approach to fabricate highly robust packaged 3D RF inductors (Fig. 1.2), while relying on the concept of stress-induced self-assembly. By leveraging the large residual stresses in evaporated chromium thin films at low thicknesses (below 50 nm), we assemble the planar copper coils coated with chromium nano-layers into out-of-plane folded RF inductors, directly improving their Q-factor. Through measurements, we show

more than three-fold (~300%) improvement in the inductor Q-factor after the bending. Considering the inherent fragility of suspended inductors, we then add a dedicated wafer-level polymer packaging to our inductors, to improve their mechanical robustness. Specifically, we coat a thick SU-8 layer using a quasi-static volumetric dispensing process, to embed the inductors without deforming them. Upon baking, the polymer layer solidifies, making the buried inductors extremely rigid. We show that though our inductors have Q-factors similar to existing MEMS inductors, their low design complexity and high strength gained via polymer packaging make them stand out among the others. This packaging technique essentially paves the way for the widespread commercialization of suspended inductors, which has been hindered in the past by their poor mechanical reliability.

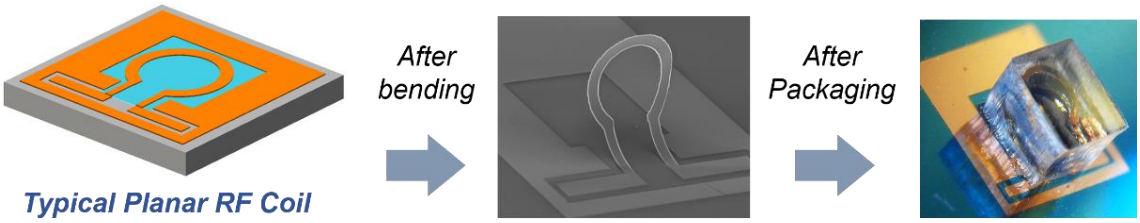

Figure 1.2. Transforming traditional planar RF coils into out-of-plane wafer-level packaged inductors.

1.1.2. Development of High-Performance RF-MEMS Switches via Stress-Engineering (Chapter 4)

Electrostatic microelectromechanical (MEMS) switches are the basic building blocks for various radio-frequency (RF) transceivers. However, conventional cantilever-based designs of MEMS switches require a large actuation voltage, exhibit limited RF performance, and suffer from many performance tradeoffs due to their flat geometries restricted in 2 dimensions (2D). Here, by leveraging the residual stress in thin films, we report a novel development of 3-dimensional (3D) wavy microstructures, which offer the potential to serve as high-performance RF switches. Relying on standard IC-compatible metallic materials, we devise a simple fabrication process to repeatedly manufacture out-of-plane wavy beams with controllable bending profiles and yields reaching 100%. We

then demonstrate the utility of such metallic wavy beams as RF switches achieving both extremely low actuation voltage and improved RF performance owing to their unique geometry, which is tunable in three dimensions and exceeds the capabilities of current state-of-the-art flat cantilever switches with 2D-restricted topology (Fig. 1.3). As such, the wavy cantilever switch presented in this work actuates at voltages as low as 24 V while simultaneously exhibiting RF isolation and insertion loss of 20 dB and 0.75 dB, respectively, for frequencies up to 40 GHz. Wavy switch designs with 3D geometries break through the design limits set by traditional flat cantilevers and provide an additional degree of freedom or control knob in the switch design process, which could enable further optimization of switching networks used in current 5G and upcoming 6G communication scenarios.

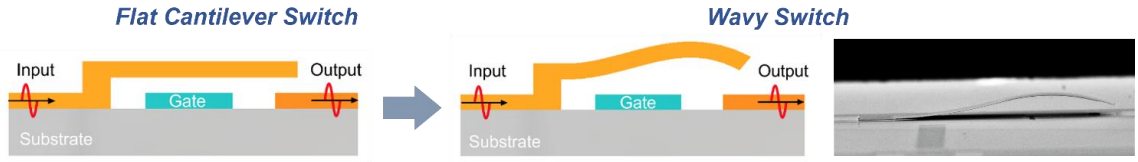

Figure 1.3. Schematic illustration of proposed wavy switch and its geometrical differences compared to traditional flat-cantilever switch.

1.1.3. Machine Learning-Based Design and Optimization of RF-MEMS Components (Chapter 5)

RF-MEMS technology has evolved significantly over the years where various attempts have been made to tailor such devices for extreme performance by leveraging novel designs and fabrication processes as well as integrating unique materials; however, their design optimization aspect has remained less explored. In this work, we report a computationally efficient generic design optimization methodology for RF-MEMS passive devices based on multi-objective heuristic optimization techniques, which to our best knowledge stands out as the first approach offering applicability to different RF-MEMS passives as opposed to being customized for a single, specific component [8] (Fig. 1.4). To comprehensively optimize the design, both electrical and mechanical aspects of RF-MEMS device design are modeled carefully using coupled finite element analysis (FEA). The proposed approach first generates a dataset, efficiently spanning the entire

design space, based on FEA models. By coupling this dataset with machine learning based regression tools, we then generate surrogate models describing the output behavior of RF-MEMS device for a given set of input variables. Finally, the developed surrogate models are subjected to genetic algorithm-based optimizer, to extract the optimized device parameters. The proposed approach is validated for two case studies including RF-MEMS inductors and electrostatic switches, where the multiple design objectives are optimized simultaneously. Moreover, the degree of conflict between various design objectives of the selected devices is studied, and corresponding sets of optimal trade-offs (pareto fronts) are extracted successfully.

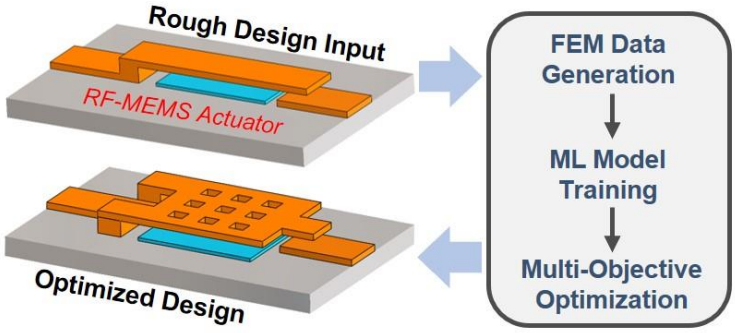

Figure 1.4. ML-based design and optimization methodology for RF-MEMS components.

2. CONTROLLABLE RESTRUCTURING OF THIN FILMS BASED ON INTRINSIC STRESS[1]

2.1. Concept of Intrinsic Stress-Induced Self-Assembly

When a layer of thin metal film is deposited on a substrate, tensile or compressive residual stresses are likely to develop in the deposited film which can cause the film to either contract or expand when released from the supporting substrate [9-11]. The type of intrinsic stress in the film, depends largely on the material properties, as well as the deposition technique (i.e. sputtering, evaporation etc.) and the actual deposition conditions (i.e. temperature, pressure, ambient gas etc.). By engineering stress gradients in multi-layer structures such that differing magnitudes and/or modes of residual stress (i.e. tensile or compressive) exist in each layer, effective transverse bending of the entire structure in either upward or downward direction can be achieved (Fig. 2.1). Accordingly, increasing tensile stress gradients from the sacrificial layer to the top surface of the thin-film stack will cause upward bending of the film upon release (Fig. 2.1(*a*)); and, tensile stress gradients increasing towards the sacrificial layer will result in downward bending (Fig. 2.1(*b*)). Opposite behaviour is observed for compressive stress gradients, where increasing stress towards the sacrificial layer cause upward bending (Fig. 2.1(*c*)); and increasing stress away from the sacrificial layer cause downward bending (Fig. 2.1(*d*)).

Amount of bending in patterned bi-layer films depends on several factors including thickness of the film, substrate type and deposition temperature, to name a few. The

[1] Reprinted with permission from "Intrinsic stress-induced bending as a platform technology for controlled self-assembly of high-Q on-chip RF inductors" by R. Bajwa and M. K. Yapici, Journal of Micromechanics and Microengineering, 29, 064002, 2019. Copyright [2019] by IOP Publishing.

Stoney's equation, which governs the amount of stresses on metal films deposited on a substrate with respect to given conditions is given as follows:

$$\sigma = \frac{E t_1^2 K}{6 t_2 (1-v_s)} \tag{2.1}$$

where σ is the amount of stress, K is the radius of curvature, t_1 and t_2 are the thicknesses of substrate and film, E is the elastic modulus of the substrate, and v_s is the Poisson's ratio. Following Stoney's approach, there have been other efforts to model stress in thin-films [12-15].

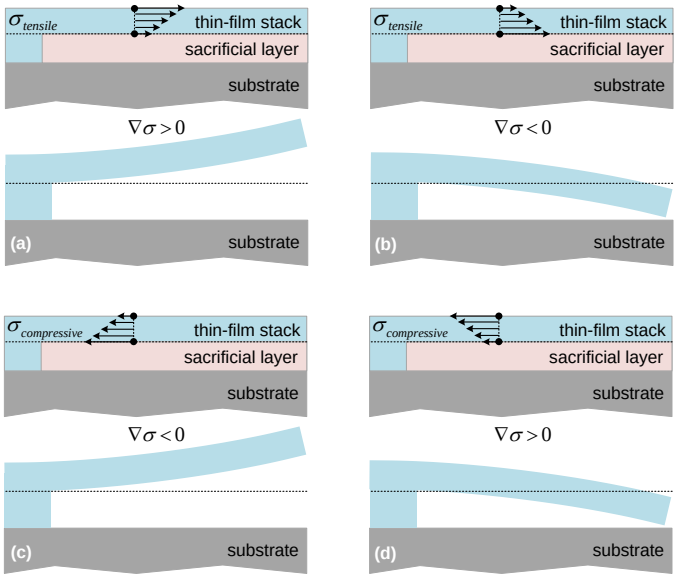

Figure 2.1 Intrinsic stress-induced post-release bending in multi-layer thin film stacks due to tensile and compressive stress gradients.

In addition to the magnitude of stress in thin-films, it is also critical to quantify the amount of bending when patterned thin-film structures are released from an underlying layer. For this purpose, optical and/or electron microscopy imaging can be used to readily quantify and compare the degree of bending in microfabricated thin-film structures with varying geometries and/or fabricated using different deposition techniques or conditions. To evaluate bending, in this work, angular displacement was used as a measure of comparison and bending angle θ was estimated both from simulation and fabrication results. Considering a fixed-free, thin-film cantilever (Fig. 2.2) anchored at point *a* with

its distal end located at position *b*, and assuming that intrinsic stresses exist in the thin-film cantilever structure, upon release from the substrate the cantilever tip will traverse to position *c*. The displacement covered by the tip of the cantilever can be used as a parameter to evaluate the amount of bending achieved; however, to normalize the variation with respect to cantilever length, "angular displacement" was used and bending angle θ was estimated as shown in Fig. 2.2. This approach provided a sound and practical basis to compare transverse bending of different cantilever geometries.

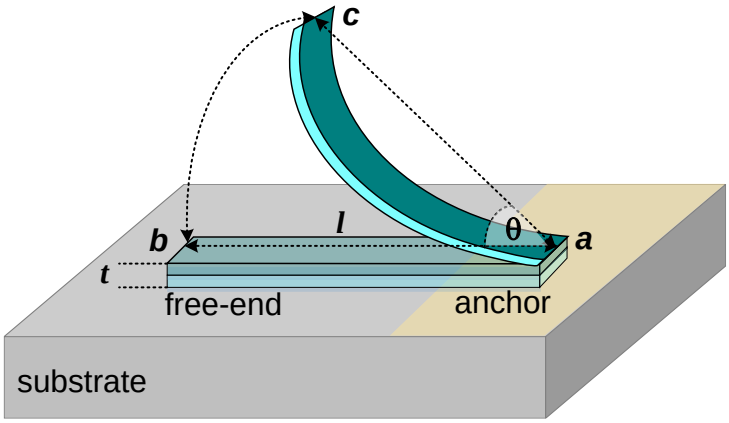

Figure 2.2**.** Concept of bending angle (θ) based on angular displacement.

2.2. Design and Mechanical Modelling

To characterize the bending angle θ with respect to geometrical specifications of patterned thin films, various sets of bi-layer cantilever structures with different dimensions were designed containing copper (Cu) and chromium (Cr) as stacked metal layers. Evaporated chromium thin films have been reported to possess large tensile stress values of around 1.3 GPa at a thickness of 100nm; whereas, copper films possess smaller tensile stress, usually less than 0.1 GPa, over a large span of thicknesses [15]. Since the actual magnitude of intrinsic stress in metallic thin-films is highly dependent on the film thickness and deposition conditions, by fixing the deposition parameters and varying the thicknesses of Cr and Cu, it is possible to control the stress gradients along the thickness of a metallic multi-layer stack to control their bending. As such, cantilevers made up of

stacked layers of Cu/Cr are expected to show upward bending, while reverse stress gradients in Cr/Cu cantilevers are expected to cause downward bending.

Cantilevers assuming different lengths ranging from 90 µm to 290 µm at three different values for the total bi-layer thickness (300 nm, 500 nm and 700 nm) were designed and modelled in CoventorWare®. To create model geometries of desired cantilever structures, a fabrication process flow was first designed in the process editor of CoventorWare®. The Process Editor of CoventorWare® software makes use of foundry MEMS processes (e.g. CVD, metal evaporation and deep etching etc.) to create process flows and hence perform more accurate MEMS simulations. Subsequently, suitable mask layouts defining length and width of the cantilevers were developed and eventually, integrating mask layouts with appropriate fabrication process flow resulted in 3D model geometries of cantilevers. The thickness of the Cr layer was fixed at 100 nm, and Cu layer was varied at 200 nm, 400 nm and 600 nm; respectively. Following the construction of the model geometry, reference values for intrinsic stresses [15] were defined in material library for both copper and chromium metals as a parameter of their material properties. However, other material properties such as elastic constants and density. were kept at pre-defined default values. Progressively, boundary conditions i.e., anchor points for cantilevers etc. were defined and automatic meshing was performed. Finally, the mechanical solver of CoventorWare® software *MemMech* was used to simulate the designs and observe mechanical deformation in the cantilever structures. Finite element analysis (FEA) results revealed out-of-plane bending of cantilever structures away from the substrate with the bending angle (θ) as a function of cantilever thickness (t) and cantilever length (l). Since cantilever width (w) does not significantly affect bending in the low width/length (w/l) regime of less than 1 [9], w was fixed at 50 µm to yield w/l ratios of ~ 0.5 or less, and achieve bending primarily as a function of l and t.

Analysis results display an increase in the bending angles with increasing cantilever length, while bending angles decreased with increasing cantilever thicknesses (from 300 nm to 700 nm), as reported in Fig. 2.3(a-c). To highlight the effect of film thickness, a 280-µm-long cantilever was simulated for various thicknesses and results indicated decreasing bending angles of 128°, 71° and 50° with increasing film thicknesses of 300 nm, 500 nm and 700 nm, respectively (Fig. 2.3(d-f)). The complete trend of bending

angles for all simulated cantilever lengths and thicknesses are plotted and compared in Fig. 2.3(g).

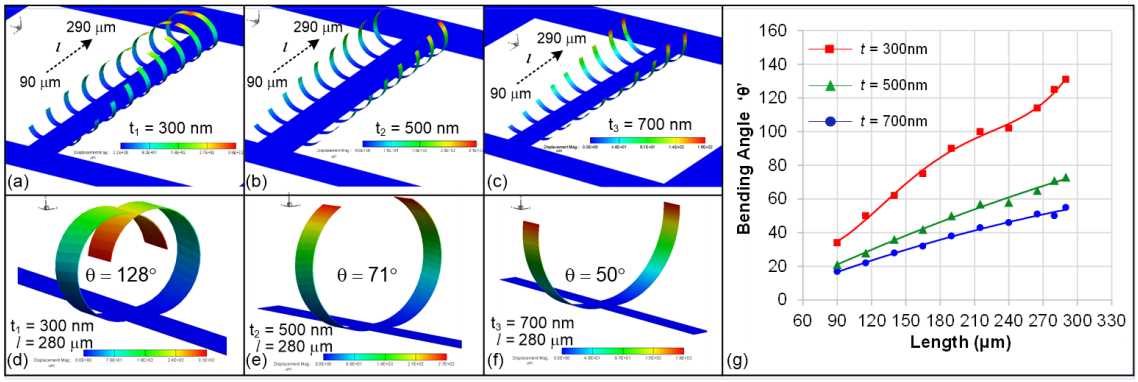

Figure 2.3. FEA results indicating intrinsic stress induced bending for a set of cantilevers with lengths "*l*" varying from 90 µm to 290 µm and thickness of: (a) t_1 = 300 nm; (b) t_2 = 500 nm; and (c) t_3 = 700 nm; (d-g) zoom-in views of 280 µm-long, two-sided cantilevers for the same thicknesses t_1, t_2, t_3, respectively; and (g) trend of simulated bending angles (θ) with respect to the length of cantilevers for varying thicknesses.

2.3. Fabrication and Characterization

To verify the bending results obtained from mechanical modelling, identical structures were developed using standard MEMS fabrication processes. First, a sacrificial layer of silicon dioxide (SiO_2) was deposited on a silicon substrate using plasma enhanced chemical vapor deposition (PECVD). The sacrificial oxide was lithographically patterned by spin- coating and exposing a layer of AZ 5214E photoresist, and wet etching the oxide with buffered oxide etchant (BOE). As a result, contact holes in the SiO_2 layer were created, through which cantilever structural layers were anchored to silicon and mechanical connection was ensured. To realize multi-layer metallic films, chromium and copper of varying thicknesses were deposited on SiO_2 using e-beam evaporation technique with substrate rotation. First, a thin layer (10 nm) of chromium was deposited to serve as an adhesion layer, followed by deposition of a copper layer, and finally by a top chromium layer. The stacked thin-film metallic layers were patterned by

photolithography to form cantilever structures, and selectively wet-etched with commercial Cr and Cu etchants. Etching of the sacrificial oxide layer resulted in free standing cantilevers with some finite amount of intrinsic stress.

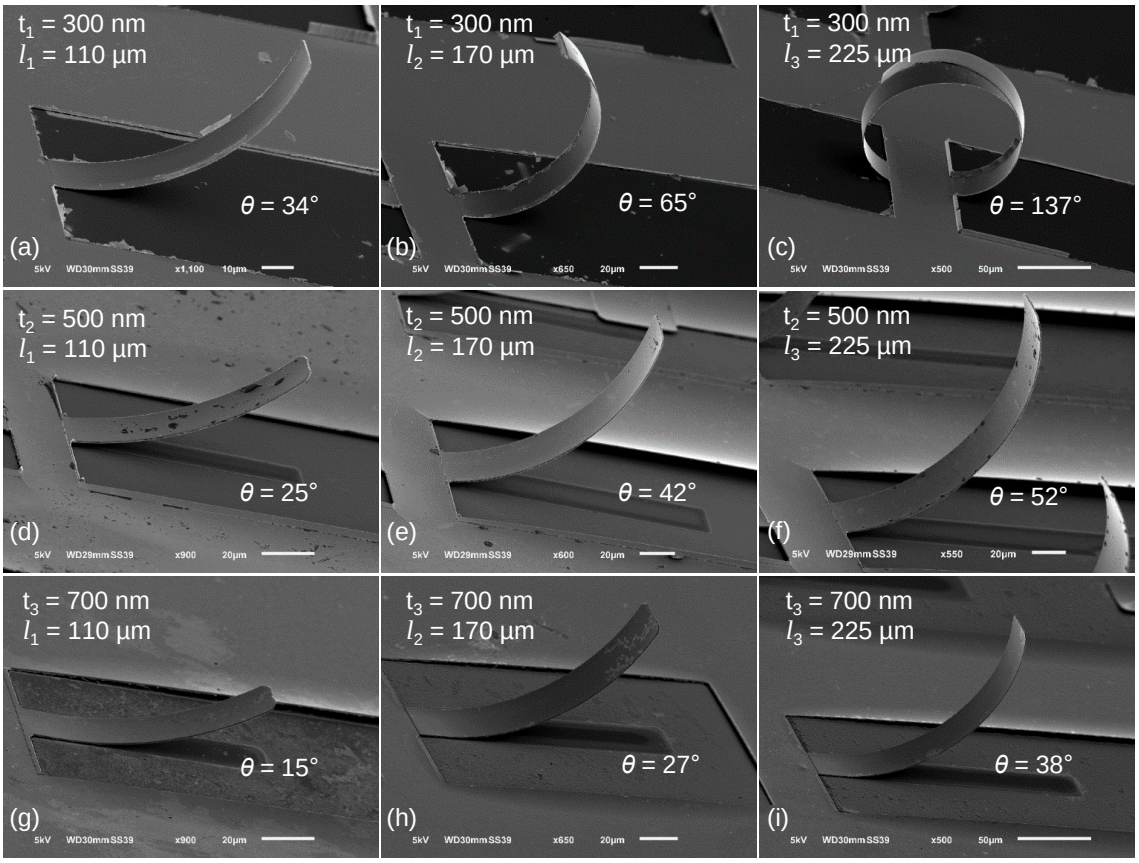

Figure 2.4. Side-view SEM images of released cantilevers with corresponding bending angles (θ) for three different lengths (l_1 = 110 µm, l_2 = 170 µm, l_3= 225 µm) and thicknesses t_1 = 300 nm (a-c); t_2 = 500 nm (d-f); t_3 = 700 nm (g-i).

Thin-films of chromium have large intrinsic stress and act as the primary stressor layer in the bi-metallic cantilever structure. Additionally, the magnitude of stress in Cr is highly dependent on film thickness. Therefore, to ensure the same magnitude of stress in Cr layers for all fabricated designs, the thickness of Cr was kept constant at 100 nm. Instead, thickness of the Cu layer whose stress is relatively invariant of film thickness was adjusted at 3 different values (200 nm, 400 nm and 600 nm) to achieve of Cr/Cu thickness ratios (t_{CR}/t_{CU}) of 1/2, 1/4, and 1/6, respectively. This approach allowed a more controllable modulation of the total stress gradient in the multi-layer stack and provided tuning of the

degree of bending in fabricated microstructures upon sacrificial layer release. Following fabrication, stress-induced bending in cantilevers was observed under a scanning electron microscope (SEM) and bending angles were experimentally quantified. SEM images of cantilevers for three fixed lengths (l) and for three film thicknesses (t) are shown in figure 6, which indicate upward bending where θ decreases with t, and increases with l in much similarity to modelling results. Specifically, θ rises from 34° to a maximum of 137° as l increases from 110 µm to 225 µm for t_1 of 300 nm (Fig. 2.4(a-c)), similarly for t_2 of 500 nm θ varies from 25° to 52° (Fig. 2.4(d-f)), and from 15° to a minimum of 38° at t_3 of 700 nm and l of 225 µm (Fig. 2.4(g-i)).

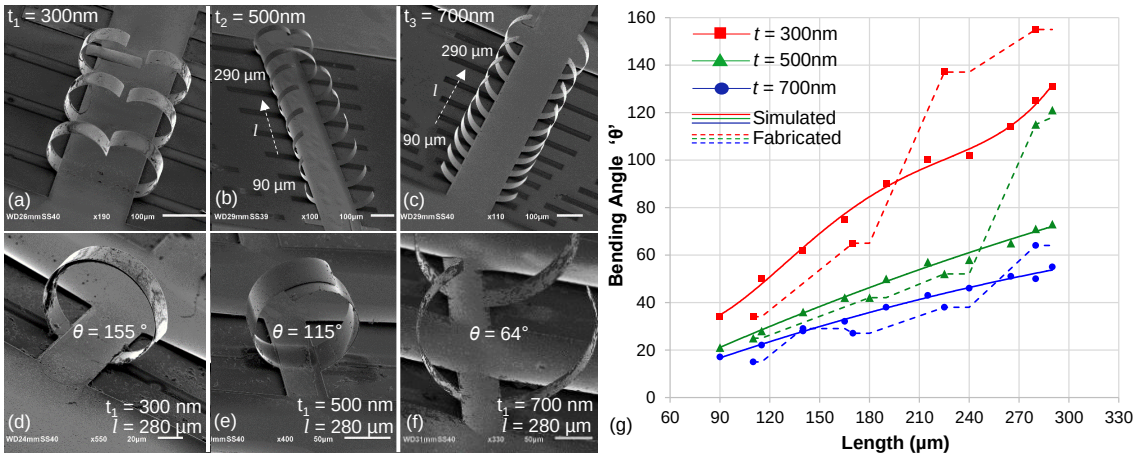

Figure 2.5. (a) SEM images of two-sided Cu/Cr cantilever arrays consisting of varying cantilever lengths and fabricated at three different film thicknesses; (b) SEM images of 280 µm long cantilevers fabricated at thicknesses of 700 nm, 500 nm and 300 nm; and (c) comparison of bending data obtained from simulations and fabrication results for cantilevers.

In coherence with the modelling results, 300-nm-thick structures exhibit the highest, whereas 700-nm-thick structures show the lowest bending for all cantilever designs (Fig. 2.5(a-c)). The comparison between simulated and experimental results shows high consistency especially at lower values of length (l); however, at larger lengths the bending angles of fabricated structures tend to increase more rapidly than simulated bending angles. For instance, bending angles for a cantilever of length 280 µm at film thicknesses of 300 nm, 500 nm and 700 nm were observed to be 155°, 115°, and 64°, respectively (Fig. 2.5(d-f)); whereas modelled cantilevers with similar l of 300 µm displayed θ of 131°,

77°, and 59°, respectively. Complete bending data from both simulation and fabrication results are plotted and compared in Fig. 2.5(g).

As suggested by the theory, direction of cantilever bending can be adjusted by controlling the sign of the stress gradient or the loading mode. Since stress in evaporated thin-film metals is usually tensile; we have chosen to control the sign of the stress gradient (i.e., considering increase of tensile stress away from the sacrificial layer-thin film interface to yield positive stress gradients and increasing tensile stress gradients towards the sacrificial layer to be negative) rather than the loading mode (tensile vs. compressive). Thus, it can be hypothesized that by modulating the stress gradient along the length of a cantilever, it can be possible to realize complex wavy structures upon post-release self-assembly which are otherwise difficult, if not impossible, to fabricate with conventional microfabrication.

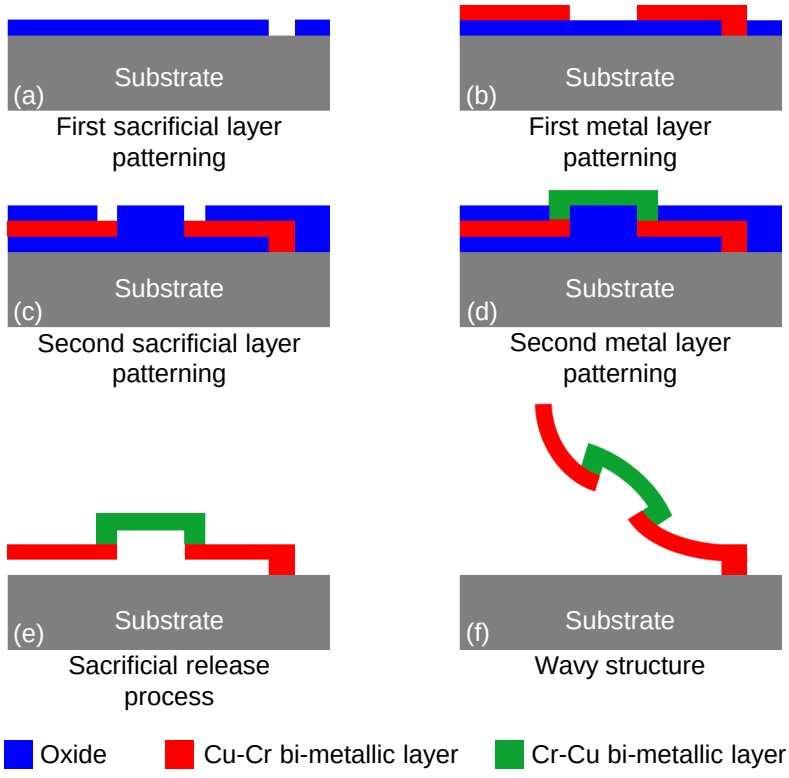

Figure 2.6. Fabrication process flow of a three-segment cantilever showing opposing stress gradients engineered in each segment for realization of wavy structure.

To elaborate on the concept, cantilevers with sections of alternating stress conditions were designed and fabricated. A fabrication process flow diagram for such a cantilever with three segments is shown in Fig. 2.6. Initially, a sacrificial layer of SiO_2

layer was deposited on a silicon substrate using PECVD technique and patterned using standard photolithography step followed by a subsequent wet etching step to create sub-micron deep via holes (Fig. 2.6(a)). Next, a bi-layer thin film metal stack consisting of a chromium metal layer on top of a copper metal layer was deposited and patterned using a combination of e-beam metal evaporation, photolithography and selective wet etching. The patterned metal-1 layer (Cu/Cr) formed the first and last sections of the three-segment cantilever (Fig. 2.6(b)). Afterwards, a second SiO_2 sacrificial layer was deposited and patterned on top of metal-1 layer to create mechanical junctions (vias) between metal-1 and a subsequent metal-2 layer (Fig. 2.6(c)). Lastly, metal-2 layer stack (Cr/Cu) was deposited and patterned with the intention to serve as the middle section of the three-segment cantilever (Fig. 2.6(d)). First and last sections of the cantilever (metal-1 layer) are comprised of Cu/Cr metal stack resulting in upward bending, whereas the middle section is made up of Cr/Cu stack (metal-2 layer) and have opposite stress gradients causing this section to bend downwards. Sacrificial release of such a cantilever results in controllable fabrication of wavy shaped structure (Fig. 2.6(f)) which also demonstrates the potential of intrinsic-stress induced self-assembly technology in 3D microfabrication. Fig. 2.7 shows a scanning electron microscope image of a three-segment, wavy structure fabricated using the described process flow.

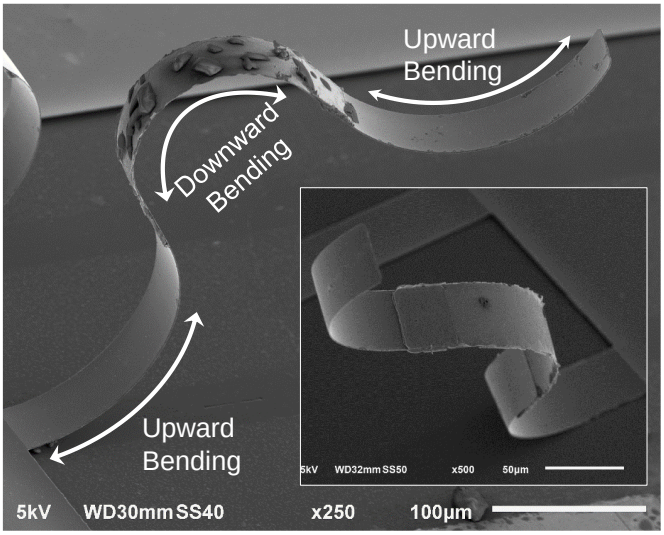

Figure 2.7. SEM images of a segmented cantilever showing opposing stress gradients engineered in each segment to controllably realize upward and downward deflections and form a complex wavy-shaped structure.

3. ORIGAMI-INSPIRED FABRICATION OF HIGH-PERFORMANCE WAFER-LEVEL PACKAGED THREE-DIMENSIONAL RADIO-FREQUENCY INDUCTORS[2]

3.1. Introduction

On-chip inductors are among the key elements of various radio-frequency (RF) transceiver blocks such as low-noise amplifiers, matching networks, voltage-controlled oscillators and filters, and their efficiency directly affects the overall performance of an RF system [16]. Conventional on-chip inductors have planar spiral-shaped geometries, which are easy to design and fabricate; however, such geometries are linked with large RF losses, most of which originate due to strong magnetic coupling between flat spiral inductor coils and underlying silicon substrate with finite resistivity. To quantify inductor losses, a unitless metric known as "*Q*-factor" is often utilized, which is an indicator of the inductor efficiency, where larger *Q*-factor implies a more efficient inductor.

Fundamentally, improvement in *Q*-factor or reduction in losses can be achieved by decreasing the proximity of inductors from lossy silicon substrate, which is practically impossible with flat spiral designs as they are mechanically adhered to substrate. Considering these performance limitations, various efforts have been made to realize more advanced 3-dimensional (3D) inductor geometries, also referred to as MEMS inductors, with better immunity against the substrate effects [16, 17]. This was achieved by either lifting the coils away from the substrate, removing the bulk silicon from

[2] Reprinted with permission from "Origami-Inspired Fabrication of High-Performance Wafer-Level Packaged Three-Dimensional Radio-Frequency Inductors" by R. Bajwa and M. K. Yapici, IEEE Journal of Microelectromechanical Systems, 2023. Copyright [2023] by IEEE.

underneath the inductors, or designing complex 3-dimensional structures with low magnetic leakage into the substrate [2, 4, 7, 18-21].

With 3D designs, on-chip inductors have demonstrated *Q*-factors much larger than the conventional planar spiral designs [2, 4, 7, 18-21]. However, compared to planar designs, out-of-plane topologies are inherently linked with high fabrication complexity, more susceptible to mechanical stresses, and require robust packaging solutions to ensure sufficient device reliability [22]. Though there have been attempts where researchers focused on lowering the manufacturing complexity [23], adding wafer-level cap to inductors [24] or strengthening them mechanically with improved designs [25], all these aspects that are essential for overall device development were scarcely addressed simultaneously. In particular, wafer-level packaging of 3D inductors has been widely overlooked over the years, which is in fact critical for realizing resilient integrated out-of-plane inductors capable of withstanding subsequent die packaging and other assembly procedures. Bare 3D on-chip inductors are by nature incompatible with the die packaging process, due to their suspended shape resulting in high fragility [26, 27]. Therefore, from a practical standpoint, a 3D inductor with performance no matter how much larger than its flat-spiral counterpart, is meaningless without the sufficient mechanical stability and appropriate packaging.

Addressing the above concerns, we here report the development of self-assembled out-of-plane RF inductors with wafer-level polymer encapsulation. Our inductors not only exhibit large *Q*-factors but also have low design and fabrication complexity as well as extremely high mechanical robustness gained via polymer packaging, compared to other free-standing inductors. To fabricate 3D inductors, we have leveraged the concept of intrinsic/residual stress in thin films, where we carefully adjust the stress mismatch between the layers of patterned thin film stack to induce controllable out-of-plane bending [7]. As opposed to other fabrication methodologies for MEMS inductors such as substrate transfer, post-fabrication magnetic assembly, and thick photoresist-based processes that are lengthy and complex, stress-induced self-folding is relatively simple involving only one typical 3-step surface micromachining process. We show that by bending the inductors away from the substrate, their *Q*-factor exhibits a three-fold improvement compared to similar geometries in flat 2D configuration.

Furthermore, thin film suspended inductors have thickness of less than a micron, while their designed footprints can be as large as 1 mm^2 or even more depending on the amount of required inductance. Such large-aspect ratio suspended devices are thus naturally very fragile [28], and their packaging is certainly not straightforward. In view of these challenges, we have developed a quasi-static polymer encapsulation process for 3D bent-up inductors, to realize their on-wafer packaging without mechanically damaging them. Instead of standard spin-coating, we use volumetric dispensing at a low flow rate to quasi-statically immerse the inductors in a commercially available polymer (SU-8) while preserving their shape. Thick films can also be achieved easily using this method by simply controlling the dispensed volume, which is required for encapsulating tall bent-up inductors, while producing thick films is challenging with spin-coating. Upon baking, the dispensed polymer film solidifies with suspended inductors buried inside it, thereby providing a solid mechanical support. Afterwards, we also pattern the SU-8 layer to remove the unwanted polymer material and realize a localized on-wafer packaging for inductors.

It should be noted that SU-8 encapsulation slightly degrades the performance of bent-up inductors due to its large loss tangent value compared to air, however the amount of degradation is quite low. To summarize, we herein highlight a great potential of suspended inductors that has not been fully utilized in past due to their limited reliability. In response, we then propose a multi-faceted development strategy for high-performance out-of-plane RF inductors, in which we address various unanswered practical issues.

3.2. Design Concept

Inherently, thin films deposited on a substrate have residual stresses inside them, which depend on many factors including deposition type, film material, film thickness and deposition conditions etc. A mismatch between the residual stress values of different layers in a multi-layer thin film stack generates a stress gradient along the film thickness. By adjusting the direction and amount of this stress gradient, a controllable out-of-plane bending can be induced in thin films, as they are released from the substrate [7, 15].

Relying on this idea, we have identified two standard IC thin film materials with large residual stress mismatch i.e., copper and chromium (Fig. 3.1(a)), to fabricate bent-up inductors with large bending angles, which helps reduce the substrate proximity losses.

Evaporated copper thin films are known to have low stress while chromium thin films possess a significantly high intrinsic stress, particularly at low thicknesses [15, 29]. We have verified this behavior by characterizing the film stress with respect to thickness, through surface profilometry experiments and utilizing Stoney's equation. We observed that residual stress of copper (Cu) stays between 60-80 MPa (tensile) for thicknesses up to 1 µm. In contrast, stress in chromium thin films is more than 1 GPa at thicknesses below 40 nm, reaching a maximum of 2.7 GPa (tensile) at 20 nm (Fig. 3.1(b)). It is worthwhile to note that both copper and chromium are highly IC-compatible and are widely used as IC interconnects and adhesion layers for metallic films, respectively. Using these materials thus simplifies the fabrication by alleviating any additional costs linked with some special materials, which are often required for fabricating 3D inductors.

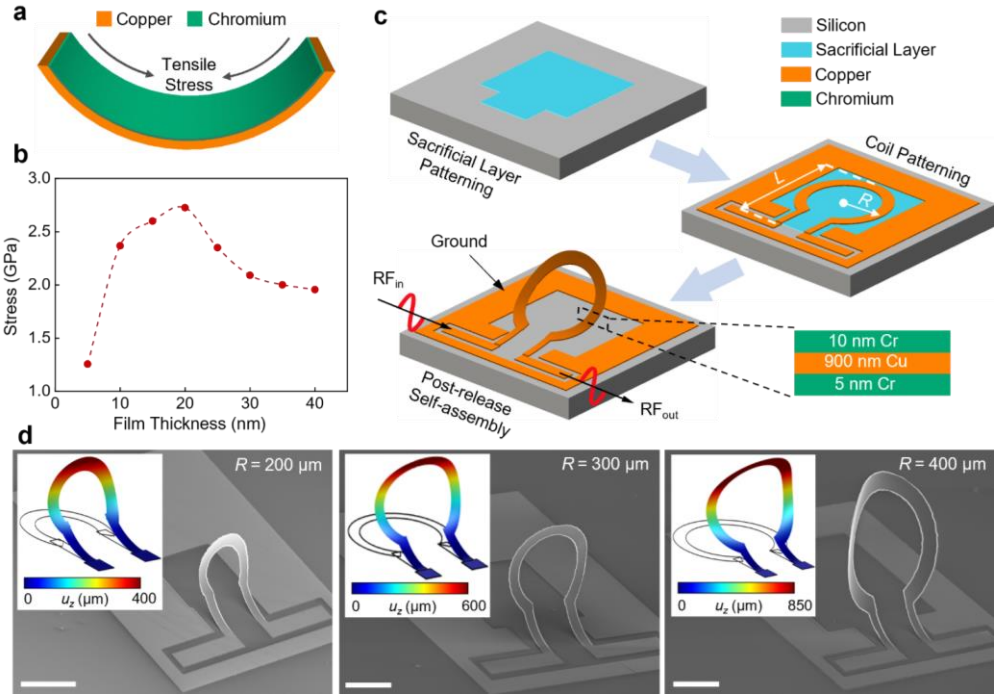

Figure 3.1. Schematic demonstration of the development of stress-induced self-assembled ring inductors: (a) illustration of bending in copper-chromium thin film stacks; (b) characterized residual stress in evaporated chromium thin film for thickness up to 40 nm. As a convention, tensile stress is represented with positive values; (c) fabrication

process for self-assembled inductors; (d) simulation results and SEM images of the designed ring inductors, with ring radius varying from 200-400 µm. Scale bar = 300 µm.

3.3. Modeling and Fabrication of Self-folded Inductors

To validate our approach, we have designed single-turn ring inductors with varying footprints (Fig. 3.1(c)). Though more advanced inductor layouts (e.g., multi-turn structures) can lead to improved performance, these layout optimizations are already well-studied in literature and are beyond the scope of this work [30, 31]. Instead, we here aim to explore and quantify the improvement in inductor performance achieved by mitigating the substrate proximity losses via bending, irrespective of the inductor layout. Therefore, we have chosen basic ring structures, as opposed to other complex layout types available for on-chip inductors. The inductors were designed to have inductance values in a range from 1 to 5 nH, which is typical in RFICs. Accordingly, the designed ring inner radius (R) range was from 200 µm to 400 µm, resulting in a footprint of 0.2-0.6 mm^2.

The structural layer of inductors was assumed with a three-layer thin film stack, containing one copper layer sandwiched between two thin chromium layers (Cr-Cu-Cr). In this configuration, bottom Cr layer served as an adhesion layer, while the top Cr layer was the ‘stressor layer’, responsible for bending. Aiming to develop a systematic design approach, we first estimated the inductor bending angles for different thin film layer thicknesses prior to actual device fabrication, by carrying out a finite element method (FEM) based static-structural analysis in COMSOL [32]. In doing so, we used experimentally extracted residual stress values of thin films as the boundary conditions. Notably, an upward bending can be induced in inductors when the stress in top Cr layer is larger than that in bottom adhesion Cr layer. Therefore, in simulations, we fixed the thickness of bottom Cr layer to a value that results in lowest residual stress i.e., 5nm (Fig. 3.1(b)), while the copper layer thickness was fixed to 900 nm. The thickness of top Cr layer was however varied from 5 nm to 20 nm, to tune the inductor bending angle. We observed that with top Cr layer thickness of 10 nm or more, the inductor bending angles for all designs remain well above 45°, sufficient enough to decouple the substrate

influence, as also demonstrated in earlier works [7]. Hence, we chose the thin film configuration ‘Cr-Cu-Cr’ with thickness of 5-900-10 nm for the inductor fabrication.

The designed inductors were fabricated on a 525 μm thick silicon substrate (resistivity ~10 Ω.cm), with a 500 nm silicon dioxide passivation layer coated via plasma enhanced chemical vapor deposition (PECVD). To fabricate suspended inductors, we employed a typical three-step surface micromachining process with one sacrificial layer (Fig. 3.1(c)). First, we deposited and patterned a 500 nm thick photoresist layer (diluted AZ5214E), serving as the sacrificial layer. The photoresist (PR) layer was then hard-baked at 180°C for 45 min, to ensure its stability in the subsequent fabrication steps [33]. Next, the three-layer thin film stack (Cr-Cu-Cr) was deposited using thermal evaporation and patterned using standard ultraviolet (UV) lithography, to define the inductor geometry. Finally, the hard-baked PR was removed in a photoresist remover at 80°C, in about 20 min, which yielded free-standing bent-up ring inductors. To avoid the stiction of suspended inductors, the samples were rinsed multiple times in methanol, and then dried at room temperature.

Fig. 3.1(d) shows the SEM images of three fabricated inductor designs having ring diameter of 400 μm, 600 μm, and 800 μm, respectively, which agree well with the bending profiles predicted by FEM simulations. It is worthwhile to note that accurate thin film stress characterization is indispensable to enable a precise control over bending angles. However, this is a one-time investment, and the pre-recorded stress data can be used repeatedly in our FEM-guided design strategy, to achieve different degrees of bending.

3.4. Wafer-level Packaging of Self-folded Inductors

As can be seen from Fig. 3.1(d), fabricated inductors have a large clearance from the lossy silicon substrate, with near-vertical post-bending profile and tip deflection of up to ~800 μm. From the performance point-of-view, high isolation from the substrate is conducive to achieving a high *Q*-factor. Nevertheless, such tall high-aspect ratio structures are associated with high fragility, which limits their application in practical

scenarios. Hence, to benefit from the bent-up high-performance inductors, ensuring their mechanical robustness is very crucial. To address these reliability concerns, we propose to add wafer-level packaging to inductors, by encapsulating them in SU-8 polymer, which has also been used in earlier studies as IC-compatible packaging material [34, 35]. The details of the packaging method are reported in the following subsections.

3.4.1. Thick SU-8 Film Process Development

To fully cover suspended tall inductors, thick polymer coating is required i.e., up to 1 mm for designs fabricated in this work. While there are methods, such spin-coating multiple layers that could be used to achieve such large thicknesses [36], these are inapplicable to encapsulate fragile microstructures. That is, strong polymer flow under the centrifugal forces during spin coating can easily damage or deform the inductors. Delicate suspended microstructures instead require a more static encapsulation process, e.g., polymer casting. Therefore, we have utilized the 'constant-volume-injection' method toquasi-statically bury our inductors inside the SU-8 polymer layer [37].

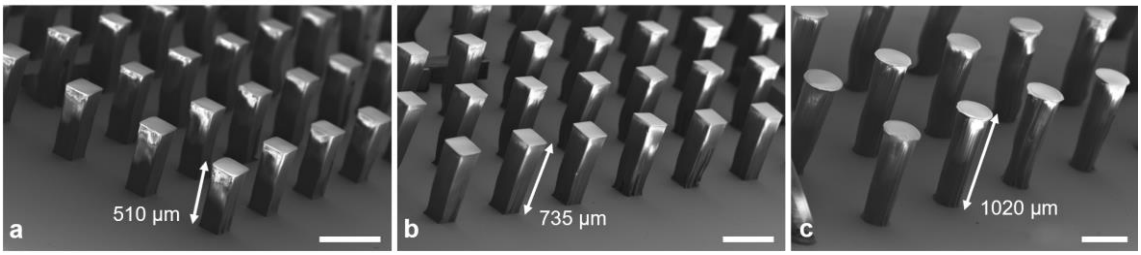

Figure 3.2. SEM images of SU-8 micro-towers fabricated using volmetric dispensing method: (a) film thickness = 500 µm; (a) film thickness = 750 µm; (c) film thickness = 1000 µm. Scale bar = 500 µm.

Before encapsulating the inductors, we first optimized the thick SU-8 patterning process on a silicon substrate. Briefly, we calculated the SU-8 volume according to sample size (4 cm x 4 cm) and required coating thickness, and dispensed it on the sample center using a syringe with resolution of 0.1 mL. The samples were then soft-baked at 110°C on a flat hot-plate surface; we tested three different layer thicknesses i.e., 0.5 mm,

0.75 mm and 1 mm, and their soft-bake times were calibrated to be 2 h, 2.75 h and 3.25 h, respectively. It should be noted that SU-8 shrinks around 20% in the baking process, due to solvent evaporation. We estimated this reduction and compensated it in our calculation of the SU-8 volume to be dispensed. During soft-bake, polymer spreads evenly over the sample, without overflowing from the edges due to surface tension. This results in a highly uniform film, with thickness variation less than 5 %. Afterwards, the baked SU-8 layers were exposed using an arbitrary mask with UV energy dose of 3.5 mJ cm^{-2} μm^{-1}. A post exposure bake was then carried out at 60°C for 30 min, following which the samples were developed in propylene-glycol-methyl-ether-acetate (PGMEA). The development time varied between 3-5 h depending on the layer thickness, where larger thickness required longer development time. Although cross-linked SU-8 layer is quite stable and resistant to many standard organic solvents (e.g., acetone), a hardbake at 200ºC can be carried out to further enhance the stability of SU-8 and ensure its survival in a monolithic fabrication cycle [38].

The SEM images of fabricated SU-8 micro-towers, with thicknesses up to 1 mm, are shown in Fig. 3.2. As seen from the figure, the sidewalls are near-vertical, and thickness errors are under 2 %. This thick SU-8 coating and patterning process served as the basis for realizing robust wafer-level packaging for our suspended inductors.

3.4.2. Quasi-static Encapsulation of Self-folded Inductors

Due to low mechanical robustness of suspended thin film inductors, any kind of postprocessing on them is highly challenging, which in turn also limits their available packaging options. Polymer encapsulation of inductors via volumetric dispensing can be a viable packaging solution [22, 26], only if the polymer flow is controlled carefully. Free-standing inductors can deform under a dynamic fluid flow, which consequently can change their intrinsic properties such as inductance. Hence, in order to keep the inductor geometry unaltered, the system should be in a quasi-static mode during the encapsulation process.

With these considerations, we used the above-described volumetric dispensing method to immerse our inductors in a thick SU-8 layer. A schematic diagram elaborating

the key steps involved in our wafer-level inductor packaging method is provided in Fig. 3.3(a). Specifically, we calculated the SU-8 volume to be dispensed and injected it on the sample center with a syringe (resolution 0.1 ml). Here, we manually controlled the dispense rate μ to be at low values i.e., $\mu < 2$mL min^{-1}, to avoid any mechanical damage to suspended inductors. Since the highest tip deflection in our fabricated inductors is below 1 mm (up to 800 µm), the dispensed volume was calculated with the target polymer film thickness of 1 mm. Next, we put the samples on a flat hotplate surface for soft baking, during which the SU-polymer gradually flows towards the sample edges, leading to a uniform film. Upon cooling after the soft-bake, the SU-8 film solidified with inductors buried inside. At this point, the inductors became mechanically robust, requiring no additional care in the remaining polymer patterning steps. We then performed standard lithography on samples, with UV exposure and PGMEA development, to realize a localized polymer encapsulation of inductors.

Fig. 3.3(b) shows the optical microscope images of a bent-up ring inductor (radius = 300 µm) at different stages of the encapsulation process. From initial polymer immersion to final development stage, no physical changes in the inductor geometry were observed, which essentially validates the effectiveness of proposed technique in packaging thin fragile microstructures. These promising results in fact indicate that our technique is not only limited to inductors and can also be used to package other monolithic fragile 3D electronic components e.g., non-tunable transformers and capacitors [39, 40]. Furthermore, Fig. 3.3(c) shows a fabricated die with 16 fully packaged inductors, demonstrating a high fabrication yield. In addition, a close-up camera image is also provided in Fig. 3.3(c), clearly showing that the ring inductor is perfectly embedded inside the polymer.

Since carefully controlling dispense rate (μ) is the only critical factor in achieving a high yield packaging, we experimented our technique at different values of μ, to identify the process limits. As can be seen from the results given in Fig. 3.3(d), at a dispense rate of 1 ml min^{-1}, the inductor experienced no deformation during the packaging process. However, as the dispense rate increased, the polymer flow on the sample surface also increased, which started affecting the inductor geometry. In particular, at $\mu = 2$ ml min^{-1}, a mild deformation occurred in inductors, which intensified significantly as the dispense

rate reached 4 ml min^{-1} (Fig. 3.3(d)). To put it simply, it is critical to restrict the dispense rate below a certain threshold i.e., where flow field is weak enough to not affect the device geometry. This threshold strongly depends on the type and thickness of the structure to be packaged, and for our designs, we observed this to be near the dispense rate of 2 ml min^{-1}.

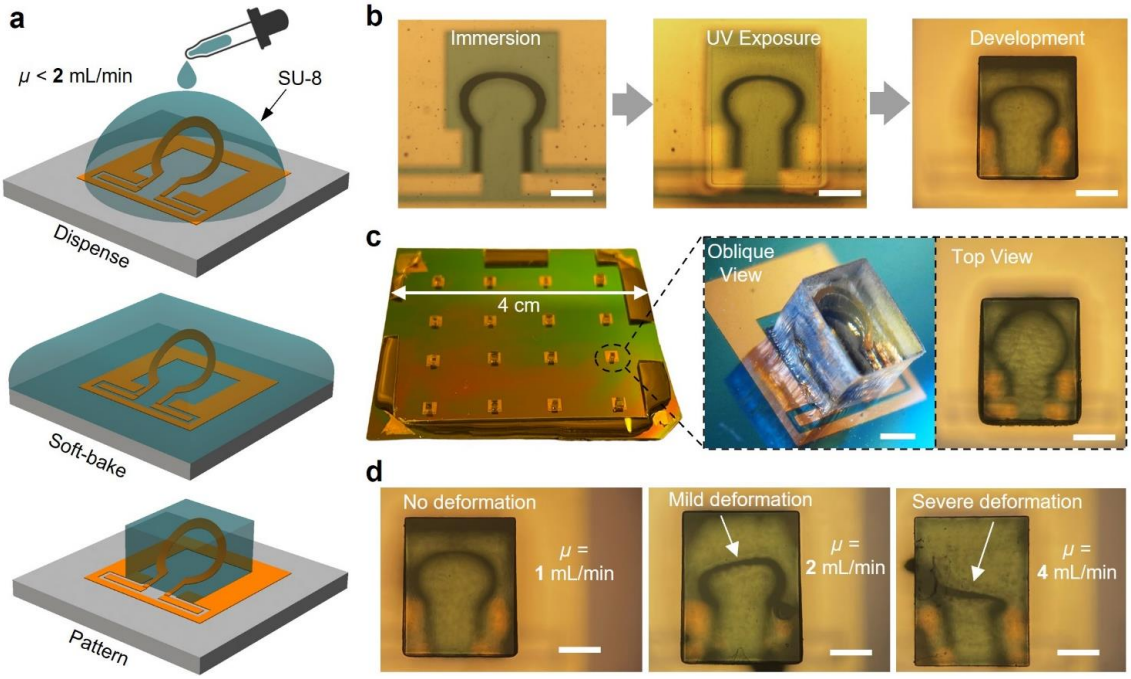

Figure 3.3. Polymer packaging process for the suspended ring inductors: (a) schematic illustration of the encapsulation process; (b) optical microscope images of 300 μm ring inductor during different stages of the encapsulation process; (c) a fabricated sample (4x4 cm^2) with 16 packaged bent-up inductors; (d) influence of SU-8 dispense rate on the inductor shape. At dispense rates of 2 mL min^{-1} and beyond, deformation in the inductors was observed. Scale bar = 300 μm.

3.5. High-frequency Characterization of Inductors

Since majority of inductor electromagnetic losses in planar state are due to its strong magnetic coupling with the nearby semiconductor substrate (e.g., Si), bending the inductor away from the substrate directly improves its *Q*-factor. To more

comprehensively analyze this phenomenon, we performed electromagnetic simulations in COMSOL (frequency = 2 GHz) and quantified the magnetic coupling between inductor and underlying silicon substrate at different bending angles. The corresponding results are reported in Fig. 3.4, where it can be seen that when the bending angle (Θ) is 0°, a significant portion of inductor *B*-field region overlaps the substrate, which in turn will induce Eddy current losses. However, as the bending angle increases from 0° to 60° (similar to our fabricated ring inductors), the *B*-field lines gradually move away from the substrate, making the inductors immune to substrate effects.

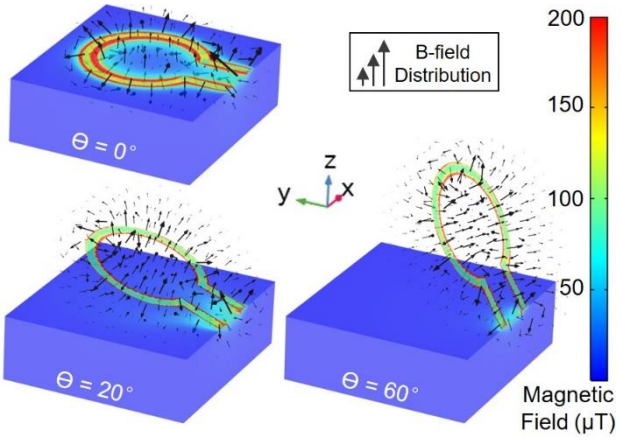

Figure 3.4. Variation in the *B*-field region of inductor with bending angle. *B*-field region shifts away from the substrate with increasing Θ.

To validate the post-bending *Q*-factor improvement and assess the overall RF-performance of developed inductors, their S-parameters were acquired using a 0-50 GHz vector network analyzer and a set of ground-signal-ground (GSG) probes. For comparison, we recorded the inductor S-parameters at three different stages of the overall design process i.e., prior to bending, post-bending, and after the packaging. We also performed 'open-thru' de-embedding on the measured data, to remove the signal pad losses. Finally, the S-parameters were converted to Y-parameters, following which the *Q*-factor and inductance values were derived using the following expressions:

$$Q = \frac{\mathrm{Im}\,(Y_{11})^{-1}}{\mathrm{Re}\,(Y_{11})^{-1}} \qquad (1)$$

$$L = \frac{\mathrm{Im}\,(Y_{11})^{-1}}{\omega} \qquad (2)$$

Fig. 3.5(a) provides a comparison between the inductor *Q*-factor values before and after the stress-induced bending. Evident from the data, *Q*-factor of inductors increased significantly as they bent away from the lossy substrate, exhibiting an almost three-fold improvement. In particular, the maximum *Q*-factor of a 400 µm diameter ring inductor increased from ~3 to 10.5, following the self-assembly. Additionally, owing to reduced capacitive coupling of bent-up inductors with the substrate, their self-resonance frequency also improved. For instance, the self-resonance frequency of a ring inductor with *R* of 400 µm increased from around 2 GHz to a value beyond 8 GHz after bending (Fig. 3.5(a)). The inductance on the other hand, is an intrinsic property of inductor solely depending on its geometry; therefore, it remained the same before and after the bending. The inductance values of all three designs are plotted in Fig. 3.5(b).

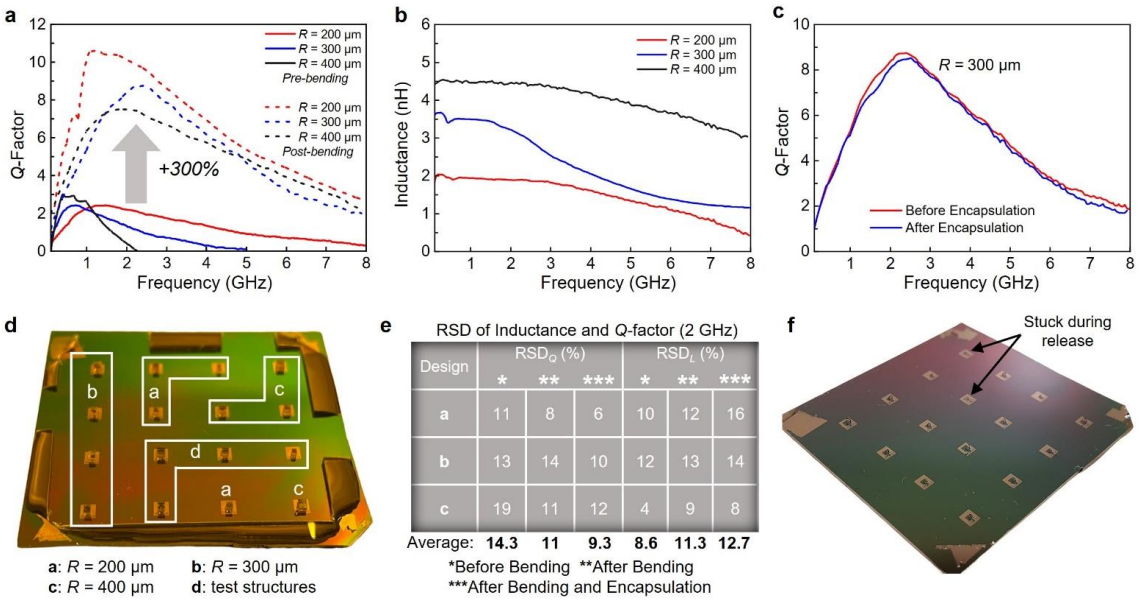

Figure 3.5. Performance characterization of fabricated inductors: (a) measured *Q*-factor of the fabricated inductors, before and after the bending; (b) measured inductance of the fabricated inductors; (c) *Q*-factor of the 300 µm ring inductor before and after the SU-8 encapsulation; (d) distribution of different ring inductor designs on a 4x4 cm^2 silicon substrate; (e) relative standard deviation of inductance and *Q*-factor for different

ring inductors before bending, after bending, and after bending and encapsulation; (f) stiction problem, which occurred in some samples during the drying process.

The role of device packaging is to improve the overall robustness, while keeping the electrical properties unaltered. To verify this, we compared the *Q*-factor values of inductors before and after the encapsulation. Fig. 3.5(c) shows the *Q*-factor variation in a 300 µm diameter ring inductor, where it can be seen *Q*-factor decreases slightly after the encapsulation. However, this reduction is very small, less than 5 %, while the reliability-related benefits of added packaging are quite substantial. In addition, we also characterized the variability of inductor's performance metrics (*L* and *Q*) across the wafer before and after bending and encapsulation. According to designed mask layouts, each of our fabricated samples contained 3 types of inductor designs (a, b and c) and some test structures, as can be seen from Fig. 3.5(d). For these three designs, we calculated the relative standard deviation (RSD) of inductance and *Q*-factor before bending, after bending, and after bending and encapsulation. Evident from Fig. 3.5(e), the ranges of RSD values of *Q*-factor and inductance are similar at all three stages of the inductor fabrication. On average, the RSD values of *Q*-factor (RSD_Q) for all designs before bending, after bending, and after the encapsulation are 14.3, 11 and 9.3, respectively. Similarly, the respective RSD values of inductance (RSD_L) are 8.6, 11.3, and 12.7. This essentially illustrates that our stress-induced bending strategy that modifies inductor profile from planar to vertical and the subsequent packaging methodology have negligible influence on the variability characteristics of on-chip components.

To further assess the effectiveness of the proposed fabrication method, we also analyzed the manufacturing yield in our samples. We observed that using optimized process parameters, the inductor fabrication has high repeatability with yields reaching unity. However, some processed samples encountered stiction issue during drying after the wet sacrificial release process, as can be seen from Fig. 3.5(f). We observed this stiction during sample drying to be the primary factor affecting the manufacturing yield. Since stiction is a well-known problem in MEMS fabrication, there exist mature techniques, such as CO_2 critical point drying, which can be used to mitigate this issue.

Finally, we have benchmarked our inductors against the other self-assembled MEMS inductors reported in literature (Table 3.1). Self-assembled RF inductors offer extreme performance and often times an easier fabrication compared to other MEMS inductors; however, all such previous designs lack packaging, and also very limited attention has been paid to enhance their mechanical robustness. In contrast, our inductors, even with their simple ring geometries, not only offer high *Q*-factors comparable to existing suspended RF inductors, but also have a significantly higher mechanical robustness achieved by polymer encapsulation.

Table 3.1. Comparison with literature.

Ref.	L (nH)	*Q*-Factor	Required Special Processing/Material	Footprint* (mm^2)	Packaged
[21]	4	7	None	~0.1	No
[19]	7	13	Non-metallic inductor material	~0.18	No
[4]	10	70	Use of Non-standard alloy (MoCr)	-	No
[18]	2	20	Lengthy fabrication process	~0.12	No
This work	3-5	11	None	0.2-0.6	Yes

*Footprint is outer coil dimension prior to bending.

4. WAVY-SHAPED ELECTROSTATIC MICROACTUATORS AS HIGH-PERFORMANCE RADIO-FREQUENCY SWITCHES[3]

4.1. Introduction

High-performance switching elements are crucial to realize efficient wireless communication networks, where they are extensively used to route radio-frequency (RF) signals via transmission lines[41-44]. Conventionally, solid-state devices (e.g., transistors and diodes) are utilized as RF switches; however, they suffer from high DC power consumption and RF losses[43]. Meanwhile, with the current high data rate 5G communication standards, the allowable margins for losses originating from the switches are becoming increasingly narrow. In such scenarios, the traditional solid-state switches can no longer meet emerging performance requirements[41].

Therefore, in an attempt to achieve ideal RF switching, many solutions have been proposed, including microelectromechanical system (MEMS) electrostatic switches and 2D material-based atomic scale switches[45-57]. Atomic-scale memristive switches show excellent potential for RF applications due to their high bandwidth, low power consumption, and fast response[58]. However, the power handling capability of memristive switches is limited, and their development is still in its infancy, with many bottlenecks in the way of wafer-scale production needing to be resolved[58, 59].

Alternatively, MEMS-based passive switching technology is quite mature, offering high linearity and extreme RF performance[43]. Among the various available

[3] Reprinted with permission from "Nonlinear restructuring of patterned thin films by residual stress engineering into out-of-plane wavy-shaped electrostatic microactuators for high-performance radio-frequency switches" by R. Bajwa *et al.*, Microsystems and Nanoengineering, 9, 74, 2023. Copyright [2023] by Springer Nature.

design topologies of MEMS switches, fixed-free cantilever switches offer simple design, compact size, and fast switching speed[41]. Nevertheless, the voltages required to actuate such microrelays are generally large compared to solid-state switches[43]. In addition, due to a basic cantilever-based structure, a gap between the suspended switch beam and the underlying fixed actuation electrode and RF line defines both RF transmission and the required actuation voltage, which results in an inherent tradeoff between the actuation voltage and RF performance. To elaborate further, although a reduced gap directly reduces the required actuation voltage, it simultaneously degrades the RF performance by reducing the RF isolation in the up-state (i.e., the unactuated state). To minimize this fundamental tradeoff, a straightforward approach is to structurally modify and optimize the switch beam for a low spring constant, which results in lower actuation voltage but also lowers the beam strength and affects the reliability[41]. Correspondingly, many strategies exploiting various electrical configurations have been reported to overcome intrinsic switch performance tradeoffs, including series-shunt configuration and a series combination of multiple switches[43, 51]. However, they all come at an expense of either increased design complexity or increased insertion losses (IL)[41, 43].

Another promising approach for improving switch performance is to convert traditional in-plane switch geometries into out-of-plane 3-dimensional (3D) switches, which could allow us to break through the performance limitations set forth by existing flat cantilever designs[46, 47]. In one related study, bent up cantilever switch beams with a low gap near the anchor point were reported to overcome the tradeoff between RF isolation and actuation voltage[46]. Although making the gap near the anchor point small and placing the DC electrode near the anchor might help actuate the switches at low voltage in a “zipping” motion[60], the free end of such cantilever switches is prone to having weaker contact with the underlying RF line due to its curled-up topology (Fig. 1). This consequently increases the on-state resistance. To alleviate this problem, additional electrostatic forces are generally required that fully flatten the switch beam and tighten its contact with the RF line[47]. Hence, when used in actual circuits, these switches typically require voltage overdrive and thus demonstrate a large “effective” pull-in voltage. This phenomenon has been well demonstrated in another work, where a bent-up switch was fabricated with an aim of improving RF isolation, which exhibited electromechanical actuation at 35 V. However, it was observed that a voltage overdrive

of up to 80 V was required to fully flatten the bent-up free end of the beam and enable sufficient contact with the RF output line[47]. Therefore, despite the potential of stress-induced bending technology that allows maneuvering the switch geometry in 3 dimensions to maximize switch performance in ways not possible with 2D flat cantilever switches, existing 3D cantilever switches were unable to fully utilize the concept as they mostly restrict their bending to only one direction (upward), thus limiting the overall degree of freedom.

Here, attempting to fully harness the potential of the intrinsic stress-induced bending concept in designing 3D cantilever switches, we report a development route for a new class of MEMS switches, which we term "wavy switch", by controllably leveraging the intrinsic stresses in the metallic structural layers of the cantilever and achieving out-of-plane bending in multiple directions (upward and downward). The switches utilize a combination of chromium and copper metals, which are widely employed in the IC industry, to realize for the first time, cantilevers with predictable wavy profiles through a simple high-yield fabrication process. We show that by using such wavy beams as RF switches, the conflicting relationship between RF isolation and actuation voltage can be effectively eliminated (which is not achievable with existing flat cantilever switches). In addition, these wavy actuators also achieve stable contact with the underlying RF line upon actuation and are free from any voltage overdrive requirements, overcoming limits of existing 3D cantilever switches[47] (Fig. 4.1). Furthermore, compared with state-of-the-art MEMS switches for mm-wave applications, we experimentally validated that our switches demonstrate excellent RF isolation and offer significantly lower actuation voltages.

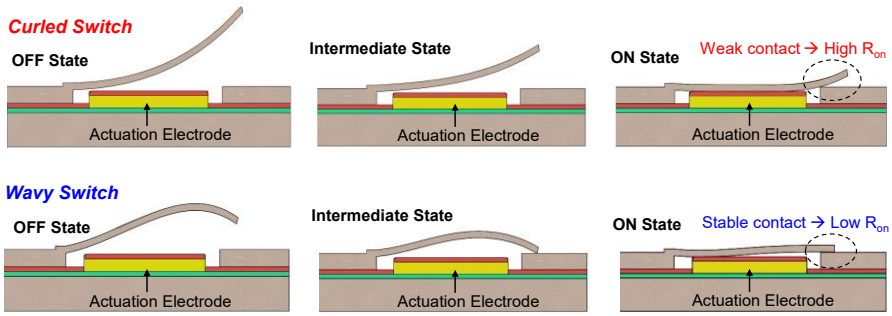

Figure 4.1. Schematic diagram elaborating the operation of the proposed wavy switches and other curled 3D cantilever switches available in the literature.

4.2. Controllable Fabrication of Wavy Cantilevers

Metallic thin films, when deposited on a substrate, often develop residual stresses that depend on the type of deposition technique as well as the deposition parameters[7]. By stacking multiple thin films with different residual stresses, a stress gradient can be created along the thickness, through which out-of-plane bending can be induced in thin films upon their release from the substrate. Relying on this concept, various bending profiles can be achieved using evaporated copper (Cu) and chromium (Cr) thin films by carefully managing their stress values and thicknesses (Fig. 4.2(a)). This occurs because these materials naturally exhibit a large stress gradient, i.e., the tensile stress in Cr is larger than that in Cu[15].

Accordingly, we used evaporated copper and chromium thin films to fabricate wavy cantilevers. In addition to providing a large stress mismatch, Cu and Cr films are also highly compatible with standard IC fabrication, thus allowing for monolithic integration. To achieve controllable bending, we first characterized the stresses in Cr and Cu films based on Stoney's equation, (detailed in section 4.11.1). Evaporated chromium has been shown to possess a large tensile stress at low thicknesses (below 50 nm), while the tensile stress in Cu is generally low over a broad range of thicknesses[7, 15]. Consistent with the literature[15], we observed a large stress variation in the Cr thin film with thickness (Fig. 4.2(b)), whereas the stress in the Cu film remained stable between 60-80 MPa for thicknesses up to 1 μm.

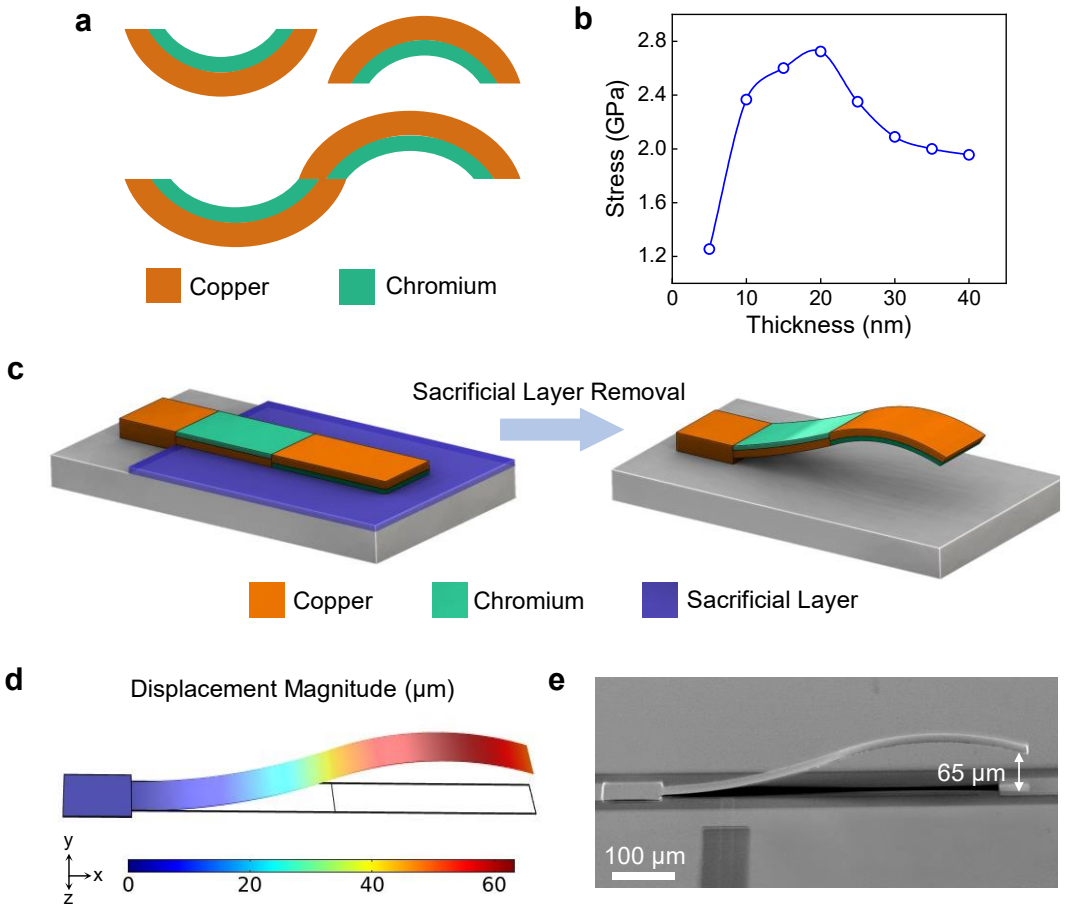

Figure 4.2. (a) Stress-induced bending in Cu and Cr thin film stacks; (b) characterized variation of residual stress in evaporated Cr with film thickness (as a convention, tensile nature of stress in indicated by positive stress values); (c) assembly of flat cantilever into a wavy beam through a combination of Cu and Cr thin films; (d-e) simulated bending profile and SEM image of a 600 μm long wavy cantilever achieved by modulating the stress in Cu-Cr thin film stack.

Considering its low stress and high conductivity suitable for electronic applications, Cu was utilized as the main structural layer of the cantilever beam, while high-stress Cr nanolayers were deposited atop and below the Cu layer to modulate the bending along the beam length and achieve a wavy profile. In particular, the thicknesses of the Cu and Cr films were adjusted to induce an upward bending moment in the first half of the cantilever beam close to its fixed end while inducing a downward bending moment in the other half near the free end, thereby allowing the assembly of initially flat cantilever (adhered to the substrate via a sacrificial layer) into a wavy-shaped beam, as

shown in Fig. 4.2(c). A cross-sectional view of the proposed wavy cantilever is shown in Fig. 4.10 given in section 4.11.2, in which the thicknesses of the Cu layer, bottom Cr layer and top Cr layer are labeled t_{Cu}, t_{Cr_bottom} and t_{Cr_top}, *respectively*. Additionally, to accurately predict the bending profiles of the cantilevers, we established a finite element method (FEM) simulation setup based on quasistatic structural modeling [32] (detailed 4.11.3). The bending simulation result and SEM image of a 600 µm long beam fabricated using the proposed strategy are provided in Fig. 4.2 (d-e), where a clear waviness in the beam shape can be observed with a tip deflection (TD) of ~65 µm.

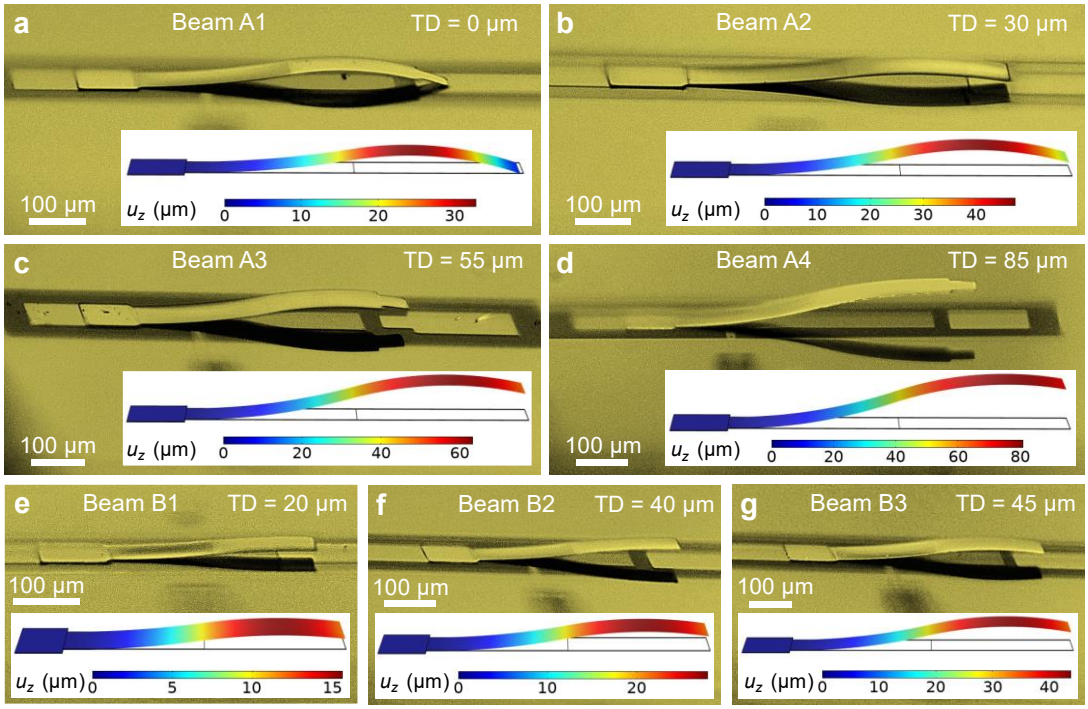

Figure 4.3. Simulated and measured variations in wavy beam shape with (a) different stress conditions and (b) different beam lengths.

To effectively utilize stress-induced bending, ensuring controllability over bending profiles is very critical. To achieve this, we designed cantilevers with varying geometries, which allowed us to comprehensively validate the accuracy of simulations and controllability of fabrication. In total, 7 types of beams were designed (A1-A4 and B1-B3), among which A-type beams have the same length and width but different Cu and Cr layer thicknesses (t_{Cu}, t_{Cr_bottom} and t_{Cr_top}) and thus different stress conditions. In contrast, the B-type beams possess the same stress conditions; however, they differ in

length. The geometrical parameters of all 7 beam designs are listed in Table. 4.2 given in section 4.11.7. The corresponding fabrication and simulation results are reported in Fig. 4.3. As shown in Fig. 4.3 (a-d), a large variation in the overall wavy profile is achieved by slightly adjusting the thicknesses of the top and bottom Cr nanolayers (exact layer thicknesses are provided in Table. 4.2 given in section 4.11.7). Specifically, 600 μm long A-type cantilever beams with varying stress conditions exhibited tip deflections ranging from 0 μm to 85 μm. Furthermore, the fabrication and simulation results for B-type beams are given in Fig. 4.3 (e-g), which illustrate a significant influence of beam length on the bending profile. This length-based curvature tuning is of particular importance since it provides an easy way to tailor the bending profile, as opposed to modifying the thicknesses and corresponding residual stresses, which always brings up a certain degree of uncertainty due to the inevitable nonuniformity of the fabrication process and equipment. These well-matched simulation and fabrication results verify the accuracy of the simulation setup and demonstrate a controllable platform for the fabrication of wavy structures, which allowed us to precisely control the profile of wavy switches reported in subsequent sections.

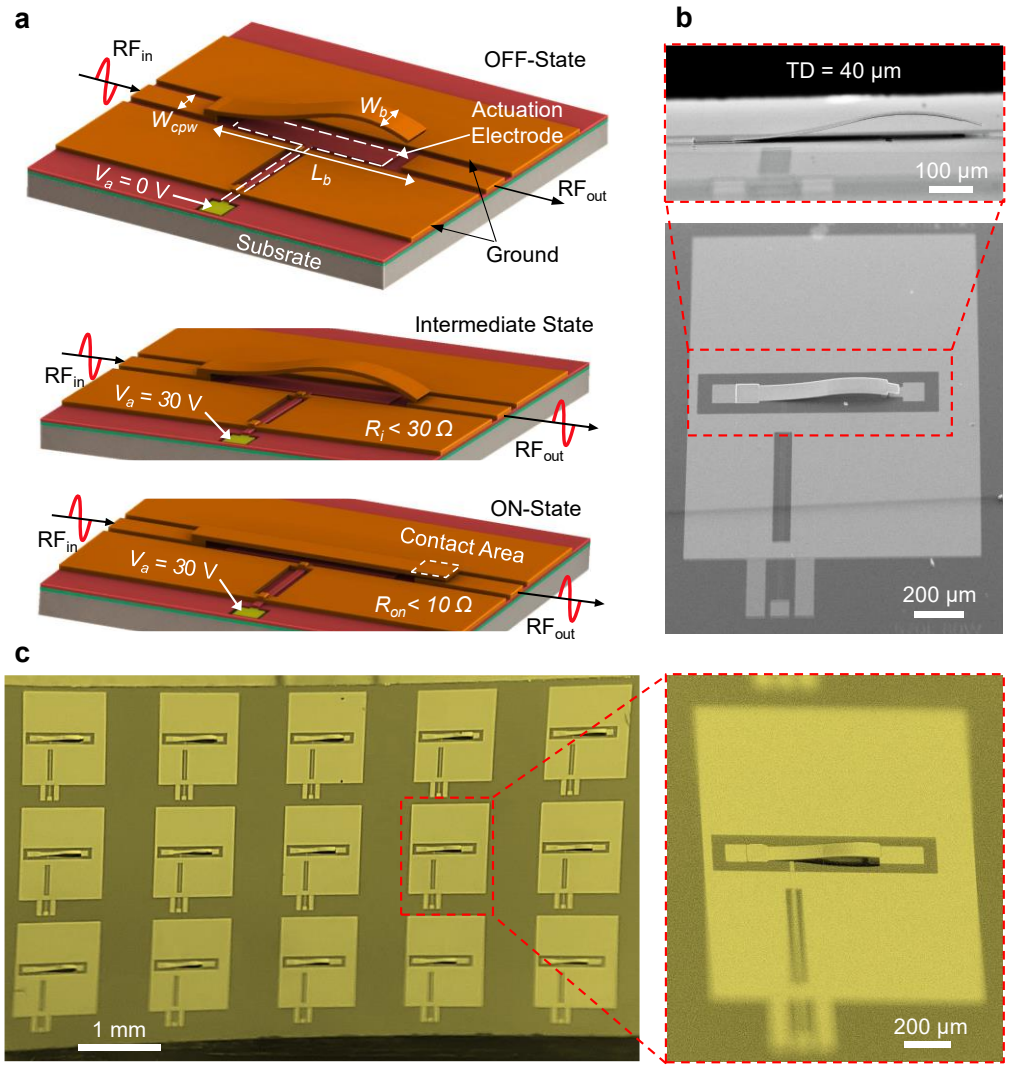

Figure 4.4. (a) Design and operating principle of the proposed wavy switches; (b) SEM image of the proposed wavy switch with a TD of 40 µm; (c) a sample with a high fabrication yield containing 15 fully functional RF switches.

4.3. Wavy Cantilevers as High-Performance RF switches

The structural design and ON/OFF operation of the proposed wavy RF switches are depicted in Fig. 4.4(a). The wavy cantilevers were embedded in a coplanar waveguide (CPW) configuration to realize in-line series RF switches, and L_b, W_b and W_{cpw} represent the length of the switch, width of the switch, and width of the CPW signal line,

respectively. Notably, both upward and downward curvatures in the wavy switch beam play important roles. The upward bending elevates the beam and provides a large air gap from the RF output line, resulting in high OFF-state RF isolation. At the same time, the gap between the switch beam and underlying actuation electrode is small near the anchor point, which in turn triggers electrostatic pull-in at lower values of actuation voltage (V_a). Although pull-in can be triggered at a low voltage in such a configuration, a large additional voltage beyond pull-in is required to fully flatten the bent-up distal end of the beam and enable stable contact with the underlying RF line[47]. To address this issue, we induced a downward curvature at the distal end of the beam to ensure sufficient contact with the RF output line without the need for any voltage overdrive. We verified this behavior via experiments where our proposed switches resulted in very low on-state resistances ($R_{on} < 10\ \Omega$) at the pull-in point. Meanwhile, no significant improvement in the resistance was observed when the actuation voltage was increased up to double the original pull-in voltage (V_{pi}), as shown in Fig. 4.12 given in section 4.11.8. This essentially validates the existence of a stable contact at the pull-in point, which is achieved by downward bending in the beam. Furthermore, the proposed wavy switch establishes contact with the RF output line prior to fully snapping to the underlying actuation electrode due to a downward curvature at its free end (as shown in the "intermediate state" of Fig. 4.4(a)), which further illustrates the natural ability of wavy switches to achieve strong contact with the underlying output line upon actuation. With this principle of operation, the wavy beams reported herein overcome the inherent performance tradeoff between RF isolation and actuation voltage by offering their simultaneous optimization.

Relying on the above concept, we designed a total of 8 wavy switches (X1-X4 and Y1-Y4) with varying lengths and widths to thoroughly investigate the effectiveness of the wavy switch design. However, the beam thickness and corresponding stress conditions were kept constant, with the aim of obtaining tip deflections above 30 µm in all designs to achieve sufficient RF isolation. Details on the structural parameters of all 8 wavy switch designs are provided in Table. 4.3 given in section 4.11.7. Following their design, wavy switches were fabricated using a simple high-yield fabrication process. Fig. 4.4(b) shows an SEM image of the fabricated wavy switch with a length, width and TD of 600 µm, 80 µm and 40 µm, respectively. Moreover, a diced sample containing 15 fully functional wavy switches is shown in Fig. 4.4(c), demonstrating 100% fabrication yield.

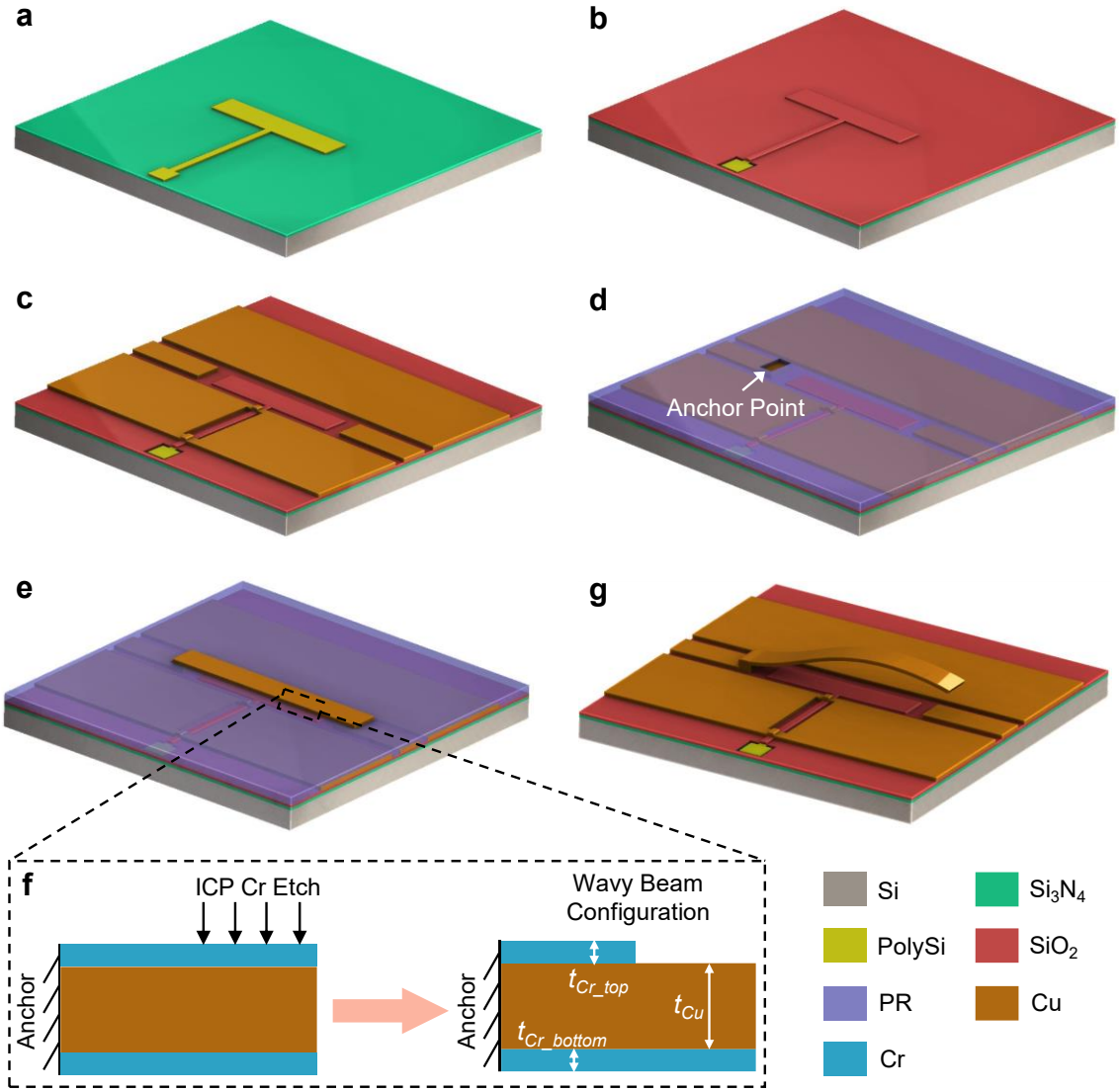

Figure 4.5. Fabrication of wavy RF switches: (a) coating HR-Si substrate with Si_3N_4 passivation layer and pattering of polysilicon DC actuation electrode; (b) SiO_2 insulation layer for DC actuation electrode; (c) pattering CPW structure using copper layer; (d) photoresist sacrificial layer patterning; (e) pattering of thin film stack made of Cu and Cr layers to define the beam; (f) side-view of wavy beam prior to its release shows patterning of top Cr layer using ICP etching, to modulate the stress gradient along beam length; (g) sacrificial layer removal, yielding a wavy-shaped switch beam.

4.4. Fabrication of Wavy Switches

A stepwise fabrication process for the proposed wavy switches is shown in Fig. 4.5. Compared with the fabrication of conventional MEMS switches, our fabrication requires only one additional lithography step (photoresist patterning and etching) to achieve complex and controllable wavy profiles. Briefly, we used high-resistivity silicon (HR-Si) as a substrate to minimize the RF losses. A doped polysilicon (PolySi) layer was used to define the DC actuation electrode (Fig. 4.5(a)), which was then insulated with a SiO_2 layer (Fig. 4.5(b)). Subsequently, a copper layer was deposited and patterned to specify the ground and signal lines of CPW (Fig. 4.5(c)), followed by pattering of the photoresist (PR) sacrificial layer to define the anchor points (Fig. 4.5(d)). Next, a thin film stack containing three layers (Cu layer, bottom Cr layer and top Cr layer) was deposited and patterned to specify the beam shape (Fig. 4.5(e)). At this stage, the top Cr layer of the beam was patterned again to modulate the stress conditions along the beam length, as shown in Fig. 4.5(f). It is worthwhile to note that top Cr layer pattering is the only additional step required to convert traditional flat cantilever switches into wavy-shaped switches. In addition, the proposed fabrication scheme does not require any special processing or materials; instead, we utilize common Cu and Cr metals along with typical surface micromachining techniques to achieve a wavy profile, and therefore, the proposed fabrication process is fully IC compatible. Finally, the beam was released by etching away the underlying sacrificial layer, which resulted in a wavy cantilever (Fig. 4.5(g)). The remaining details regarding the fabrication are provided in the Materials and Methods section.

4.5. Electromechanical Response of Wavy Switches

Fig. 4.6(a) displays the characterized ON-OFF operation of the fabricated X3-type wavy switch, indicating turn-on and turn-off times of 140 μs and 180 μs, respectively. The switching time measurements were performed at actuation voltages slightly higher than the actual pull-in voltages of the switches. In addition, Fig. 4.6(b) shows the evolution of switch resistance during switching, where first a relatively high resistance

value was observed (~20 Ω), which then converged to a stable lower value (below 10 Ω) after a few tens of microseconds. This observation validates the existence of an 'intermediate state' in which only the tip of the switch contacts the output line prior to full flattening of the switch beam. It should be noted that the measured switch resistance includes the resistance of the metallic switch beam (< 0.1 Ω), probe resistance (2-3 Ω), and switch contact resistance.

Fabricated wavy switches with varying geometries were investigated via both simulations and experiments to systematically analyze their electromechanical response (details on the simulation setup are given in sections 4.11.3 to 4.11.6). In addition, the measured and simulated switching times and actuation voltages for all types of fabricated switches are provided in Fig. 4.6(c-d), which shows that the actuation voltage is limited well below 40 V for all designs and reaches the minimum value (23 V) for switch type X4. Progressing from switch type X1 to X4, the beam length increases from 300 µm to 600 µm while the other geometrical parameters remain constant. Despite the large tip deflections of beams with larger lengths (Table. 4.3 given in section 4.11.7), which could severely weaken the impact of the electrostatic actuation force, an increase in the beam length still lowered the required actuation voltage (Fig. 4.6(c)), through utility of the proposed wavy-shaped designs, i.e., the actuation voltage decreased from 37 V to 23 V as the length increased from 300 µm to 600 µm. However, an increased switch length resulted in a slower switching speed (Fig. 4.6(d)) since a longer switch beam inherently exhibits a lower mechanical resonance frequency, which increases the switching time[44]. In particular, the switching time increased from 120 µs to 220 µs as the length increased from 300 µm to 600 µm. On the other hand, the lengths of all B-type designs are the same, and thus, they exhibit similar switching times of ~140 µs (Fig. 4.6(d)). As seen from Table. 4.3 given in section 4.11.7, the designed B-type switches differ in their widths, and varying width results in a varying overlapping area between the switch beam and underlying actuation electrode. Therefore, as the beam width increased from 50 µm to 80 µm, the corresponding actuation voltage decreased from 36 V to 25 V due to the increased overlapping area.

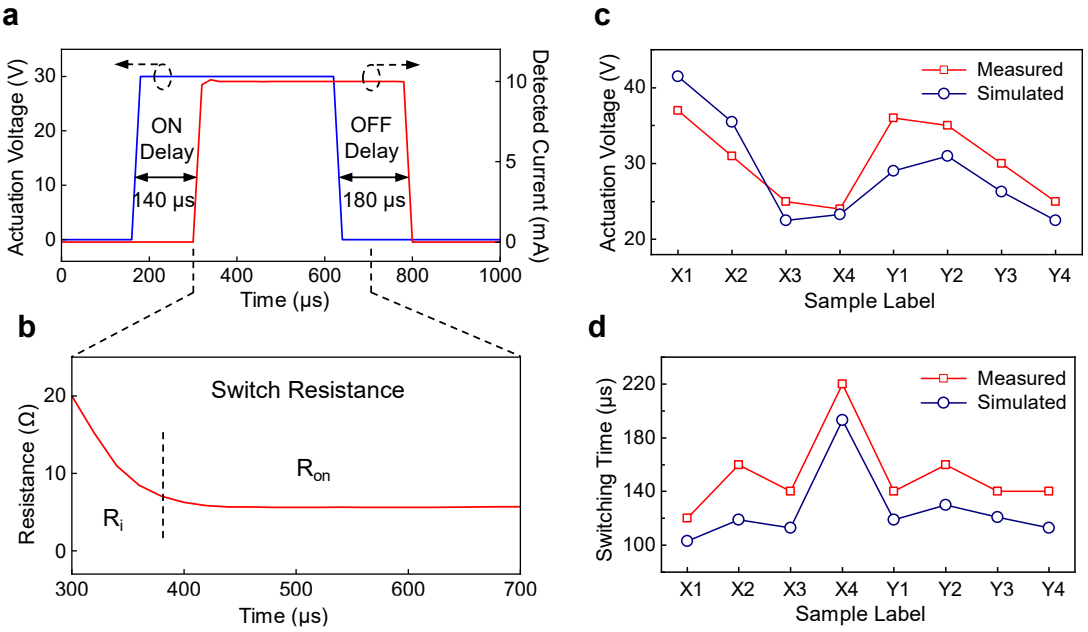

Figure 4.6. Characterized ON-OFF operation of the fabricated X3-type wavy switch; (b) switch resistance during the switching ON period; (c) measured and simulated actuation voltages of all 8 types of fabricated switches; (d) measured and simulated switching times of all 8 types of fabricated switches.

4.6. High-Frequency Performance of Wavy Switches

Simulated and measured high-frequency scattering parameters (S-parameters) of the X3-type fabricated switch in the ON and OFF states are shown in Fig. 4.7(a) and Fig. 4.7(b), respectively. These results show that the switch exhibits very high isolation ($S_{21\text{-}OFF}$ > 20 dB), with an insertion loss ($S_{21\text{-}ON}$) of approximately 1 dB and a return loss ($S_{11\text{-}ON}$) better than 10 dB for frequencies up to 40 GHz. Similar trends were also observed in the measured and simulated RF characteristics of the rest of the fabricated switches, as shown in Fig. 16 given in section 4.11.10. It is worthwhile to note that there is a certain discrepancy between the measured and simulated results, which we attribute to nonidealities in material properties, fabrication conditions, and measurement environment. In addition, the switch contact was also considered ideal in simulations, while during actual operation, losses at the contact region contribute greatly to the overall switch insertion loss and are highly sensitive to ambient factors such as humidity; thus,

unavoidable mismatches were observed[43, 61]. Next, we characterized the linearity of the proposed switches by analyzing their two-tone third-order intermodulation distortion (IMD3) at 2.4 GHz, which revealed the input third-order intercept point (IIP3) beyond 48 dBm (see section 4.10 and Figs. 4.17 and 4.18 given in section 4.11.10).

To better analyze the effectiveness of wavy designs, we studied the variation trends of RF isolation (at 30 GHz) and actuation voltage among various fabricated switches with varying lengths (Fig. 4.7(c)). As seen from the figure, by simply increasing the length of wavy switches (from switch type X1 to X4), simultaneous optimization of RF isolation and actuation voltage is achieved, which is nearly impossible with conventional flat cantilever switch designs. To verify the measurement repeatability, we measured multiple devices with the same geometry and quantified the performance variation using the standard deviation (σ, indicated by error bars in Fig. 4.7(c-d)). We observed the variation in actuation voltages of identical switches to be less than 5%, while that in isolation values was below 1 dB (Fig. 4.7(c)). These variations may be attributed to the variability in the measurement environment and processing conditions during device fabrication.

Another key parameter for RF-MEMS switches is the insertion loss (IL) in the ON state, which primarily depends on the contact resistance of the switch[44]. A key factor affecting the contact resistance is the contact area, where a larger contact area yields a lower contact resistance[44]. Relying on this principle, we varied the beam width among our Y-type samples, which resulted in varying contact areas (from 50 µm x 50 µm to 50 µm x 80 µm for switches Y1-Y4). We observed an improvement in contact resistance, i.e., R_{on} – probe resistance (2 Ω), and corresponding insertion loss with increasing contact area (Fig. 4.7(d)), where contact resistance reached the minimum (~3 Ω) for the Y4-type switch with an associated insertion loss of ~1 dB at 30 GHz, owing to its largest contact area. Moreover, to verify the repeatability of the measurements, we measured the inconsistency between the results obtained from the same type of switches, as shown by the σ error bars drawn in Fig. 4.7(d), which indicate a performance variation of less than 5%. It should also be noted that since insertion losses depend heavily on the contact region and its resistance, the effect of wavy topology on insertion losses is insignificant.

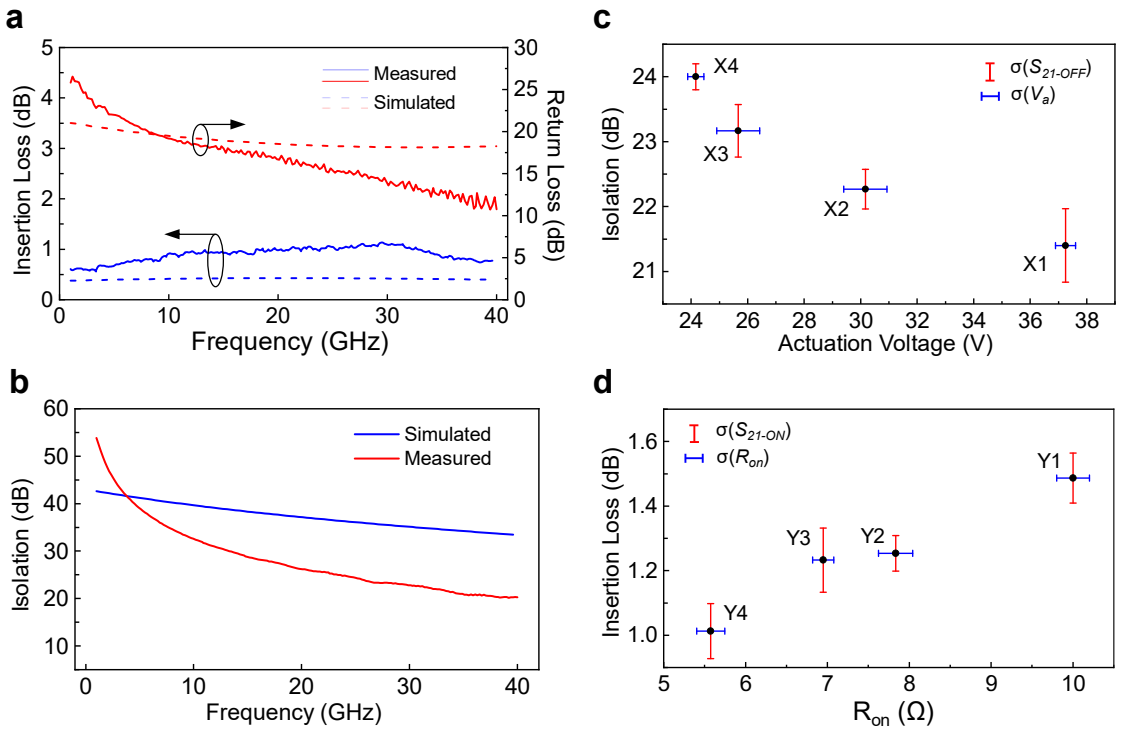

Figure 4.7. (a) Measured and simulated insertion loss and return loss of X3-type switch; (b) measured and simulated RF isolation of X3-type switch; (c) variation of actuation voltage (V_a) and RF isolation ($S_{21\text{-}OFF}$ @30 GHz) among X1-X4-type switches; (d) variation of ON-state switch resistance and insertion losses (@30 GHz) among Y1-Y4-type switches. Standard deviations are calculated by measuring each switch design three times from three different samples.

4.7. Reliability and Power Handling of Wavy Switches

The reliability of RF-MEMS switches is often a concern due to their mechanical nature, which causes wear at the contact region under long-term usage for various reasons, such as microwelding, material transfer, and contact hardening[43, 62]. Therefore, assessing the reliability and power handling ability of the proposed wavy actuators is crucial to demonstrate their feasibility for practical applications. First, we characterized the lifetime of our switches under hot-switching conditions (i.e., keeping the power on while turning the switches on and off), where we used switch X3 for experiments. We

hot-switched the actuator with 0.3 W of RF power (frequency = 2.4 GHz) for 10 million cycles (in alignment with typical test durations [51, 52, 54, 63, 64]) at a switching frequency of 2 kHz and simultaneously measured its on-state resistance at different intervals. These switch cycling results are provided in Fig. 4.8(a) and show that the switch resistance remained stable (between 5-7 Ω) for up to 4 million cycles, after which it increased to approximately 10 Ω at 10 million cycles. The test was stopped at 10 million cycles, when the resistance reached the failure criteria (R_{on} >10 Ω).

To further test the switch's robustness to hot-switching conditions, we cycled our X3 switch at higher power (1 W of DC power). These results are given in Fig. 4.8(b). In principle, DC power degrades the switch contact faster than RF power, primarily because it causes a larger amount of material transfer at the contact region[65]. As shown in Fig. 4.8(b), our switch cycled with a stable ON-state resistance for up to 0.3 million cycles. After this point, the resistance started increasing sharply and ultimately exceeded the failure criteria (R_{on} >10 Ω) after 0.5 million cycles, which is similar to that of the other reported switches with acclaimed high reliability under DC hot switching conditions[66].

It should be noted that all the testing is performed with unpackaged switches in an open-air environment, and the switch lifetime can be improved by adding a hermetic seal[67]. Considering that contact degradation is the most typical cause of switch failure, the use of harder materials (e.g., Ru) at the contact region can also improve the switch lifetime[68], as opposed to softer materials e.g., Au or Cu (used in this work), which are commonly preferred due to their lower resistivity. Furthermore, the use of multiple switch contacts that result in a "zipping" actuation has also been reported in the literature[66] to simultaneously achieve high reliability and low contact resistance.

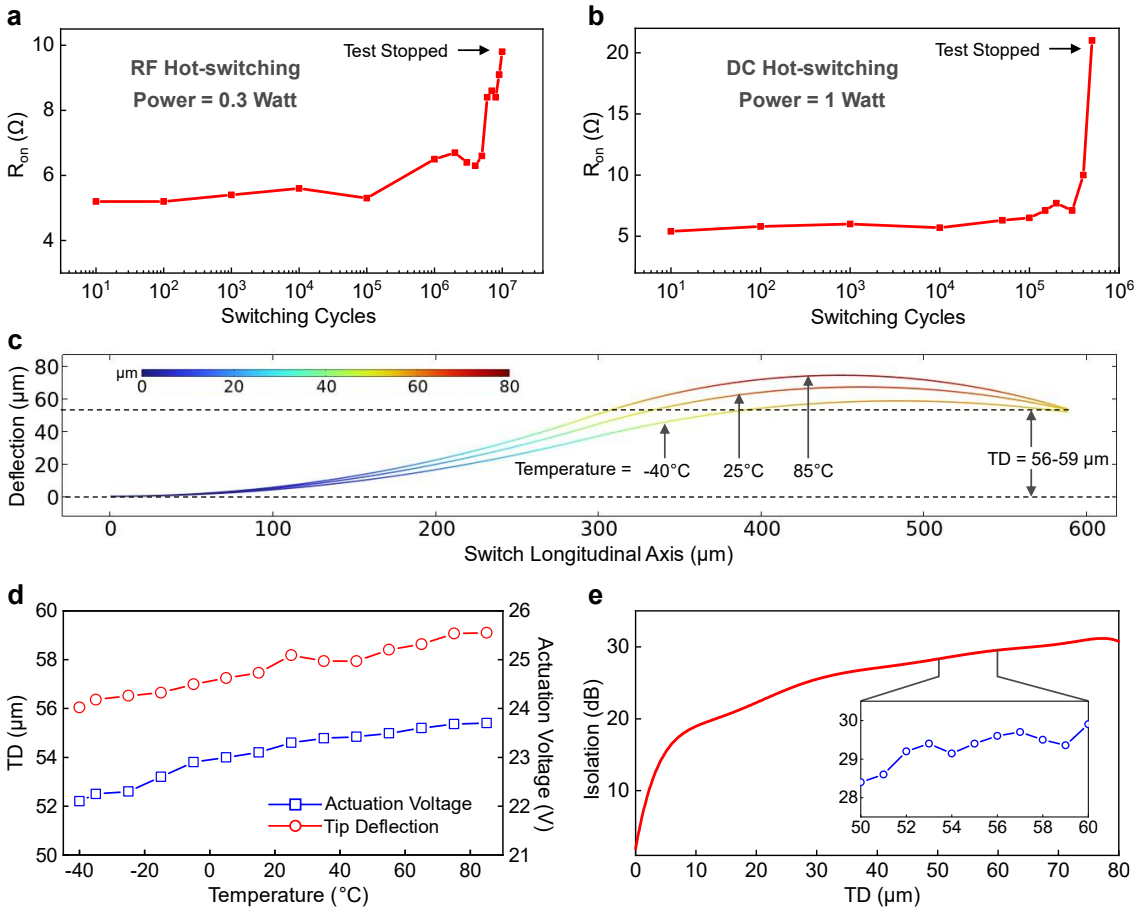

Figure 4.8. Reliability of the proposed wavy switches: lifetime characterization (a) under an RF power of 0.3 W; (b) under a DC power of 1 W. Tests were stopped when the ON-state resistance (R_{on}) crossed 10 Ω; (c) sensitivity of the wavy profile of switch X4 to temperature (under the industrial temperature range, i.e., -40 °C to 85 °C); (d) variation in tip deflection (TD) of switch X4 for temperatures ranging from -40 °C to 85 °C; (e) simulated RF isolation of switch X4 at different degrees of tip deflection at a frequency of 30 GHz.

The power handling capability of RF MEMS switches is yet another figure-of-merit that is interrelated with the switch lifetime and reliability. Two major criteria that limit the power handling of RF MEMS switches are self-actuation and RF latching failures[69]. Self-actuation refers to unwanted actuation of the switch under large RF power, which creates a large potential difference between the hanging switch beam and underlying output RF line. Self-actuation primarily depends on the overlap area and the gap between the switch beam and RF line and hence is typically more pronounced in

membrane-type shunt switches than in series switches[44]. The proposed wavy beams are series switches with a small overlap area with the underlying RF line. In addition, owing to the out-of-plane geometry, the gap between the RF line and wavy switch beams is also relatively large (> 20 μm) compared to conventional flat-cantilever series switches, which indicates the built-in immunity of the proposed switches to self-actuation. To validate this, we applied up to 70 V DC between the switch beam and the RF line; however, no detectable deformation was observed in the switch geometry. Notably, 70 V peak-to-peak voltage translates to approximately 40 dBm or 10 W of RF power in a 50 Ω system, which is quite high. The other factor that limits the power handling of MEMS switches is unintentional RF latching or stiction, which occurs after application of high RF power even though the DC actuation voltage is removed. However, this failure is observed more in capacitive switches that have a dielectric layer at the contact between the RF line and switch beam, which creates an electrostatic potential difference holding the switch in contact[44]. In our testing with power up to 1 W, no undesired latching issues were observed.

We also studied the sensitivity of the proposed switches to temperature since multilayer wavy cantilevers can exhibit a significant temperature-induced strain due to the thermal expansion coefficient mismatch between different layers (Cu and Cr) in a thin film stack that constitutes the wavy shape. A deformed wavy shape under thermal stress can essentially modify the RF isolation and actuation voltage of the switch. Therefore, to verify the resilience of the wavy switch performance against thermal stresses, we analyzed the variations in RF isolation and actuation voltage over the industrial temperature range, i.e., -40 °C to 85 °C. For analysis, we considered the X4-type switch because this device has the greatest length and hence will exhibit the maximum strain among all switch designs (subject to the same thermal conditions). We established a thermomechanical simulation environment (described in 4.11.6), where we varied the temperature and recorded the corresponding changes in the wavy profile (Fig. 4.8(c)). We observed that an increase in temperature slightly increases the degree of waviness and vice versa for the case of decreasing temperature; however, the variation in tip deflection (TD) is negligible. In particular, TD increased from 56 μm to 59 μm as the temperature increased from -40 °C to 85 °C (Fig. 4.8(d)). For deformed wavy profiles, we then extracted the actuation voltage using electromechanical simulations (detailed in 4.11.4),

which reveal that the required actuation voltage varies less than 5% from its value at room temperature (25 °C) to its value at -40 °C and at 85 °C (Fig. 4.8(d)).

Fundamentally, the RF isolation of the switch is mainly defined by the overlap area between the switch beam and the underlying RF line. Therefore, to understand the influence of temperature on the RF isolation of switches, we first simulated the isolation (at 30 GHz) of switch X4 under different amounts of tip deflection. As seen from the results given in Fig. 4.8(e), RF isolation degrades sharply with TD only when TD is below 10 µm; however, in all our wavy switches, TD is maintained above 20 µm. This in turn illustrates that the variation in the TD of the proposed switches due to thermomechanical deformation will not have a significant effect on RF isolation. For instance, considering switch X4 with TD varying from 56 µm to 59 µm over the temperature range -40 °C to 85 °C, the corresponding change in RF isolation is less than 1.5 dB (Fig. 4.8(e) inset). Based on these results, we conclude that although wavy switches can be more prone to unwanted thermally induced strains, their performance remains virtually invariable over a wide range of temperatures.

4.8. Comparison with the State-of-the-art

To evaluate the performance improvement, we compared two of our best performing switches (X3 and X4) with the existing state-of-the-art for in-line series MEMS switches operating at mm-wave frequencies, as shown in Table 4.1. All compared designs require larger actuation voltages (> 50 V) than the proposed wavy switches, which operate at only 24 V. At the same time, our wavy switches also exhibit a relatively large RF isolation (at 40 GHz) when compared to the other designs, thus offering simultaneous optimization of isolation and actuation voltage that cannot be guaranteed with existing flat-cantilever type geometries. To further highlight the effectiveness of wavy switches in optimizing the isolation-voltage tradeoff, we benchmarked our switches against the existing designs through a new performance index parameter (k) that we formulated, which incorporates both RF isolation ($S_{21\text{-}OFF}$) and actuation voltage (V_a) into a simple ratio of $|S_{21\text{-}OFF}|/V_a$. This means that better or higher isolation (a larger absolute value of $S_{21\text{-}OFF}$) and lower actuation voltage (a smaller value for the DC pull-in voltage)

yield a larger *k* parameter. In view of the current 5G communication scenario, we calculated the performance index (*k*) for all compared designs at 40 GHz, as reported in Table 4.1. Due to the unique wavy geometry, the proposed switches outperform all the other compared designs in terms of the performance index (*k*) by a large margin. In addition, as seen from Table 4.1, the insertion loss of wavy switches is in a reasonable range; however, it is not the lowest among the compared designs. This is because the insertion losses primarily depend on contact resistance, which is slightly higher in our switches since we employ a Cr/Cu bilayer contact material, as opposed to conventional gold contacts that inherently provide a lower contact resistance due to their better conductivity and low hardness. Therefore, by simply adding the gold contacts to our wavy designs, the lowest achievable insertion losses can certainly be reached. The only drawback of wavy topology is the large switching time compared to existing designs, which can be attributed to its relatively long length.

Table 4.1. Performance comparison of the proposed switches with existing works.

Ref.	Actuation Voltage	Isolation (dB)		IL (dB)		Switching Time (μs)	Hot-switched Lifetime (millions—MM)	Performance Index (*k*)	
		20 GHz	40 GHz	20 GHz	40 GHz			20 GHz	40 GHz
[48]	50 V	24	15	0.7	1	-	-	0.48	0.3
[54]	80 V	20	14	0.6	0.6	10.6	100 MM @ 0.1 W	0.25	0.18
[51]	50 V	50	36	0.35	0.43	30.4	100 MM @ 1 W	1	0.72
[47]	60 V	18	14	0.3	0.7	3	-	0.3	0.23
[57]	60 V	25	17.5	0.9	0.9	2.2	-	0.41	0.29
[70]	80 V	30	24	0.25	0.4	-	-	0.37	0.3
[52]	60 V	10	-	1.1	-	103	3 MM @ 0.1 W	0.16	-
[63]	89 V	20	-	1	-	10	100 MM @ 0.3 W*	0.22	-
[64]	80 V	21	-	0.9	-	200	4 MM @ 30 mW*	0.26	-
[45]	15 V	21	-	0.8	-	1.8	725 MM @ 1 mW	1.4	-
Switch X3	25 V	27	20.4	0.9	0.75	140	10 MM @ 0.3 W	1.08	0.82
Switch X4	24 V	29	20.2	0.7	0.94	220 μs	-	1.20	0.84

*device is hermetically packaged.

4.9. Material and Methods

4.9.1. Wavy Switch Fabrication

We first deposited a 1 µm thick silicon nitride (Si_3N_4) layer on a 500 µm thick high-resistivity silicon substrate for passivation. To define the actuation electrode and pad, a polysilicon layer was then sputtered and lithographically patterned (etched using SF_6 gas). Next, to electrically insulate the actuation electrode, we deposited a 400 nm thick silicon dioxide layer and patterned it using a commercial etchant (buffered oxide etchant) to uncover the underlying actuation pads. We then used the lift-off technique along with thermal evaporation to pattern a thin-film stack containing a 300 nm copper layer with a 5 nm chromium adhesion layer to define the CPW structures. Afterward, photoresist (AZ5214E) was spin-coated as the sacrificial layer with a thickness of 500 nm (photoresist was diluted with an appropriate solvent to achieve such a thickness). The patterned photoresist layer was then hardened at 170 °C on a hotplate for 45 minutes to improve its chemical resistance to other materials used in the subsequent processes (e.g., acetone). We then deposited and patterned the switch beam layer containing Cu and Cr thin films (layer thicknesses vary as listed in Table. 4.3 given in section 4.11.7) using the thermal evaporation and lift-off technique. Next, the top Cr layer was patterned using photolithography and reactive ion etching (with Cl_2 gas) to modulate its thickness and corresponding stress conditions along the beam length. Finally, we removed the hard-baked photoresist layer in a photoresist remover at 80 °C to release the wavy switch beams. The released samples were rinsed thoroughly first in water and then in isopropyl alcohol (IPA) and dried at room temperature to avoid any stiction issues.

4.9.2. Electromechanical Characterization

The experimental characterization was performed using a Keysight source measurement unit (SMU) with two channels, as shown in Fig. 4.13 given in section 4.11.9. The actuation voltage was provided to the switch through channel 1, while with channel 2, a voltage (100 mV) was applied to two terminals of the signal line with the

switch connected in series between them. Upon actuation under the action of applied voltage from channel 1, the current passing through the switch was sensed from channel 2 (current was limited to 10 mA), from which both transient and steady-state characteristics of the switch were extracted.

4.9.3. High-Frequency Characterization

The radio-frequency response of the switches was analyzed with a 0-50 GHz vector network analyzer, where the two-port S-parameters of switches in both the ON and OFF states were recorded. The switches were designed to have a ground-signal-ground (GSG) configuration at both ports, and thus, GSG RF probes were used for measurements (Fig. 4.14 given in section 4.11.9). Prior to measurements, GSG probes were calibrated using the short-open-load-thru method (SOLT) with a commercial calibration substrate. During high-frequency measurements, a DC actuation signal was also applied to switches using the SMU to control the switch actuation, and to avoid interference from any unwanted DC signal, DC blocks were used at both ports. Last, the power from the VNA was varied from -5 dBm to 10 dBm in the experiments, but no obvious change in the results was observed since MEMS switches inherently have a high linearity.

4.9.4. Lifetime and Linearity Experiments

The measurement setup for characterizing the switch lifetime and linearity is shown in Fig. 4.15 given in section 4.11.9, which consists of two signal generators, a coupler, GSG/DC probes, a 20 dB attenuator, a two-channel SMU, and a spectrum analyzer. To perform IMD3 tests for analyzing device linearity, we actuated the switch using DC voltage supplied by SMU (channel 1) and DC probes, supplied two RF signals with power 13 dBm from two signal generators to the switch via a coupler, and recorded the output spectrum with the spectrum analyzer. The output power was attenuated by 20 dB with an attenuator to ensure that the spectrum analyzer operated in the linear region, and the total loss from input to output was 23 dB. Moreover, the RF signals were set 20 MHz apart with a center frequency of 2.4 GHz. As shown in Fig. 4.17 given in section

4.11.10, no third-order harmonic in the output was observed at 13 dBm of input power, at which the difference between the output peaks and base signal level was 70 dB. Since increasing the input power further beyond 13 dBm was not possible due to equipment limits, we considered the output signal base level (-80 dBm, as shown in 4.17 given in section 4.11.10) as the third-order component amplitude. With this assumption, we then estimated OIP3 and IIP3, as illustrated by the third-order intercept chart given in 4.18 given in section 4.11.10.

For lifetime measurements under RF hot-switching conditions, we used a signal generator with GSG probes to supply 25 dBm (~0.3 W) RF power to switches and SMU (channel 1) for generating an actuation signal at a cycling frequency of 2 kHz. To measure switch resistance during testing, we occasionally turned off the RF source and used the SMU (channel 2) for resistance readings. For DC hot-switching experiments, we removed the RF source and GSG probes and supplied DC power to switch from the SMU (channel 2), while the rest of the measurement setup remained the same as that of the RF hot-switching tests.

4.10. Supplementary Data

4.10.1. Stress Characterization

For residual stress measurements, we first measured the radius of curvature of bare silicon substrate using KLA-TENCOR P6 surface profiler. Next, we deposited the desired film thickness on the substrate and again measured its radius of curvature. Using these substrate radii of curvature before and after the thin film deposition, we estimated the residual stress in deposited thin film according to Stoney's equation, expressed as:

$$\sigma = \frac{Et_1^2}{6t_2(1\text{-}v_s)}\left[\frac{1}{R_f} - \frac{1}{R_s}\right] \quad (1)$$

where σ is the amount of stress, R_f is the radius of curvature after film deposition, R_s is the radius of curvature of bare substrate, t_1 and t_2 are the thicknesses of substrate and film, E is the elastic modulus of the substrate, and v_s is the Poisson's ratio. Using this strategy, we characterized the residual stresses in evaporated copper and chromium films at thicknesses ranging up to 50 nm and 1 μm, respectively, as shown in Fig. 4.9.

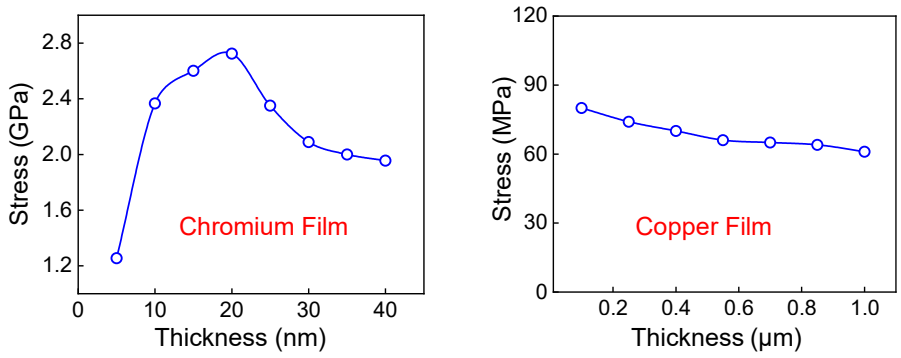

Figure 4.9. Characterized stresses in evaporated copper and chromium thin films.

4.10.2. Wavy Beam Configuration

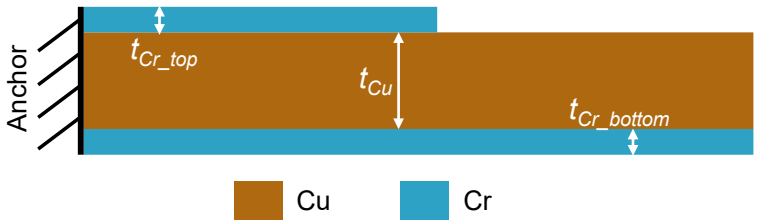

Figure 4.10. Cross-sectional view of wavy beam structure.

4.10.3. Bending Simulation

To estimate the bending profiles, a simulation setup up was established in COMSOL Multiphysics 5.6 using its Structural Mechanics module. First, the 3D geometries were built with configuration shown in Fig. 4.10, and relevant materials were assigned to the

layers. The materials were assumed to be linearly elastic, however, the geometric nonlinearities were considered as the beams were expected to undergo a large deformation. Following the material assignment, a fixed boundary condition was assigned to anchor point, while the residual stresses measured with profiler (shown in Fig. 4.9) were assigned to corresponding layers. To mimic the sacrificial release process, a moving boundary condition was assigned at the bottom edge of the beam, to deform the beam in a quasi-static manner[32]. For meshing, we use a 2D mesh at the top surface of the beam and then sweep it across the thickness to mesh to whole geometry. As recommended by COMSOL, such type of meshing reduces the computation time for beams with large aspect ratio, compared to the standard tetrahedral mesh. Finally, the stationary solver of COMSOL was used to compute the bending profiles.

4.10.4. Electromechanical Simulation of Wavy Switches

Electromechanical behavior of wavy switches was predicted using COMSOL Multiphysics 5.6 with physics type set to “Electromechanical”. Owing to its high computation cost, we performed the electromechanical simulation in 2D. Therefore, the above structural simulations were first repeated in a 2D environment to extract the 2D bending profiles of all switches listed in Table 4.3. In actual scenarios, stresses are isotropic and therefore the bending is uniform along both length and width of the beam. However, by restricting the simulations to 2 dimensions, we in fact ignored the bending effect along the beam width, since in beams where width is significantly smaller than the length, the bending profile is primarily defined by beam length[7]. Next, the deformed geometry was imported as the initial geometry in the electromechanical simulation setup where necessary materials and boundary conditions were assigned. The developed electromechanical simulation setup was dedicated to extract both stationary and transient responses of the switches under the applied actuation voltage (electrostatic force), which allowed us to obtain pull-in voltages and switching times, respectively. The pull-in study was performed using the stationary solver where applied voltage was increased in small increments (0.1 V) until the pull-in point was reached. On the other hand, the transient behavior was studied by using a time-dependent solver of COMSOL. To consider the fringing field effect, the gap between switch beam and actuation electrode was modeled

as air with “moving mesh” condition. To model the contact of switch beam with insulated underlying actuation electrode, a combination of adhesion-repulsion (Lennard-Jones model of intermolecular forces) with the penetration penalty method for the beams was employed by defining the variables implemented as boundary load in solid mechanics physics[71]. The mesh type for the beam was set as “mapped” and that for the surrounding air was set as “triangular”. Since the gap between beam and underlying stationary electrode was large, the deformation of mesh elements in the gap increased dramatically as the beam moved towards the substrate. In such scenario, the software experienced an ill-posed condition labelled as “inverted mesh”. To address this problem, automatic remeshing was considered in the transient study, to maintain the mesh quality.

To ensure a reliable operation, it is crucial to study the stresses in switch beam during actuation. Therefore, in our simulations, we also recorded the maximum stress in switch beams during an actuation cycle, which generally occurs at the anchor point when the beam is fully actuated and flattened. In our switches, copper thin film acts as the main structural layer and for a reliable operation, the maximum stress in switches should be well-below the yield strength of copper. Fig. 4.11 shows the simulated variation of maximum stress with time in switch type X4, which exhibited the largest maximum stress during actuation among all switch types due to its large tip deflection. It can be seen from the figure that the maximum stress is contained below 130 MPa, which is significantly lower than the yield strength of copper i.e., around 400 MPa at thickness of 1 µm.

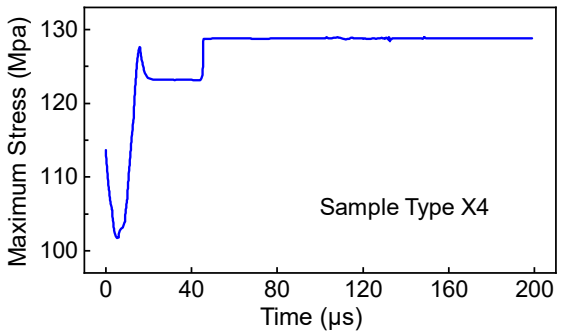

Figure 4.11. Maximum stress in Switch X4 during actuation.

4.10.5. High-Frequency Simulations of Wavy Switches

Following the electromechanical analysis, switch geometries in ON and OFF states were imported to HFSS for high-frequency analysis, where first the appropriate material properties were assigned. In addition, we enclosed the switch geometry in an air box which enables a consistent distribution of electromagnetic (EM) fields around the device to be simulated, thus artificially replicating the practical measurement environment. Moreover, we chose “Driven Modal” as the model type while the excitation type was selected as “Lumped Port”. Next, we configured a frequency sweep from 0-40 GHz, a range similar to that of our measurement system (vector network analyzer and RF probes). Lastly, the EM fields are solved by the built-in solver of HFSS relying on Maxwell’s equations over the specified frequency range, which yielded the final S-parameters of the switch.

4.10.6. Thermomechanical Simulation

To estimate the bending profile variation under thermal load, a simulation setup up was established in COMSOL Multiphysics 5.6 using its Structural Mechanics module. The bending profiles estimated with bending simulations (described in section 4.11.3) were imported to software and materials were assigned to the layers. Then, we added thermal coefficient of expansion to Cu and Cr layers, which is necessary to simulate the thermomechanical behavior of beams. Moreover, the materials were assumed to be linearly elastic; however, the geometric nonlinearities were considered, as the beams were expected to undergo a large deformation under the thermal stress. After the material assignment, a fixed boundary condition was assigned to anchor point, and the temperature was introduced in the system as a boundary condition. Finally, tetrahedral meshing was used and the bending variation is simulated using the software’s stationary solver, where temperature was increased from -40°C to 85°C.

4.10.7. Parameters of Fabricated Wavy Test Structures and Switches

Table 4.2. Geometrical parameters of various fabricated wavy beams.

Beam Type	Length (μm)	Width (μm)	t_{Cr_top} (nm)	t_{Cr_bottom} (nm)	t_{Cu} (nm)	Tip Deflection (μm)
A1	600	80	13	10	850	0
A2	600	80	17	13	850	30
A3	600	80	19	13	850	55
A4	600	80	21	13	850	85
B1	300	70	19	13	850	20
B2	400	70	19	13	850	40
B3	500	70	19	13	850	45

Table 4.3. Parameters of fabricated 8 types of switch samples.

Sample Label	L_b (μm)	W_b (μm)	W_{cpw} (μm)	t_{Cr_top} (nm)	t_{Cr_bottom} (nm)	t_{Cu} (nm)	Tip Deflection (μm)
X1	300	80	100	19	13	850	20
X2	400	80	100	19	13	850	35
X3	500	80	100	19	13	850	40
X4	600	80	100	19	13	850	55
Y1	500	50	100	19	13	850	40
Y2	500	60	100	19	13	850	40
Y3	500	70	100	19	13	850	45
Y4	500	80	100	19	13	850	40

4.10.8. ON-state Switch Resistance at Various Voltage Levels

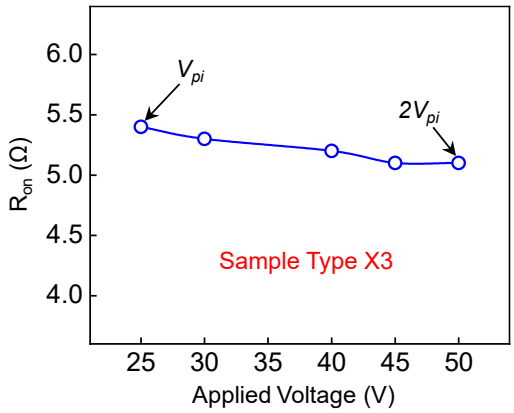

Figure 4.12. Variation of ON-state switch resistance with increasing actuation voltage.

4.10.9. Measurement Setup

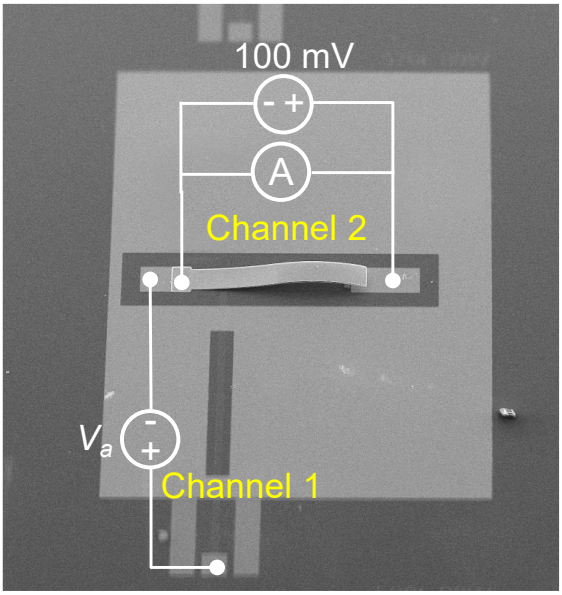

Figure 4.13. Electromechanical characterization setup using source measurement unit with 2 channels.

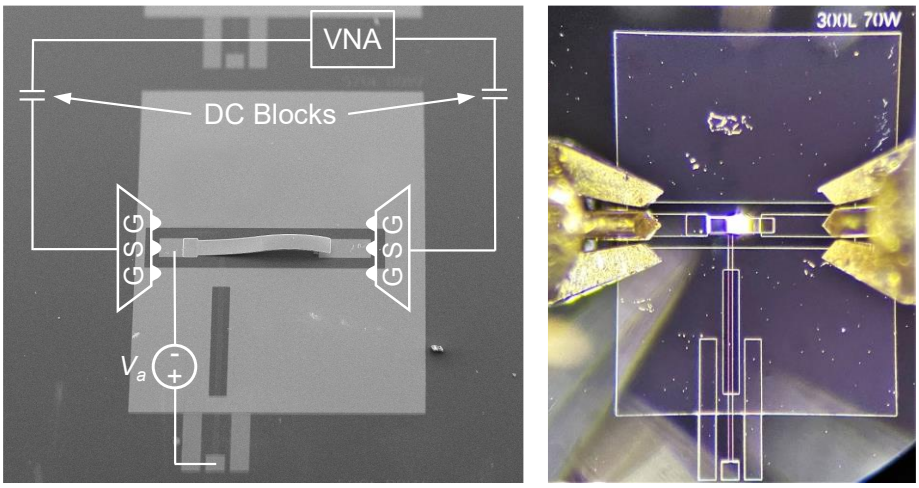

Figure 4.14. High-frequency characterization setup for the wavy switches.

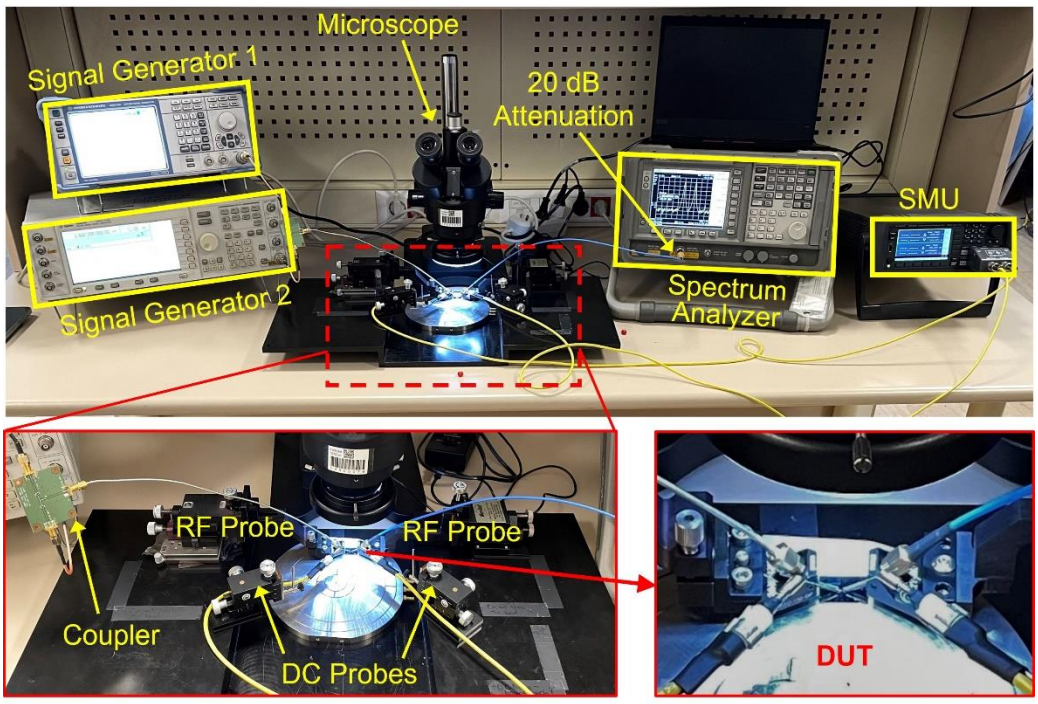

Figure 4.15. Experimental setup for characterization of switch lifetime and linearity.

4.10.10. Supplementary High-Frequency Measurement Results

All the measured and simulated s-parameters for all 8 types of designs are plotted in Fig. 4.16. As can be seen from the figure, we also observed some discrepancies between the measured and simulated results. For instance, the insertion losses of Switch X3 and X4 are lower than that of Switch X1 and X2. However, since we embedded all of our switches in the transmission line of same length, the length of switch itself should have a minimal effect on the measured insertion loss (from one GSG probe to the other). That is, all X type switches X1-X4 should ideally have a very similar insertion loss as their contact area is the same, as can be verified from the measurement results. We would like to highlight that in series DC contact RF MEMS switches, contact resistance is the main factor controlling the insertion losses and it dominates the line losses[44]. This contact resistance is highly sensitive to environmental conditions, and without hermetic seal to switches, contact resistance can vary largely during measurements [43, 61]. That is to say, as we measured the switches unpackaged in open-air lab environment, although being minor, there are unavoidable/unpredictable differences in the measurement compared to simulations.

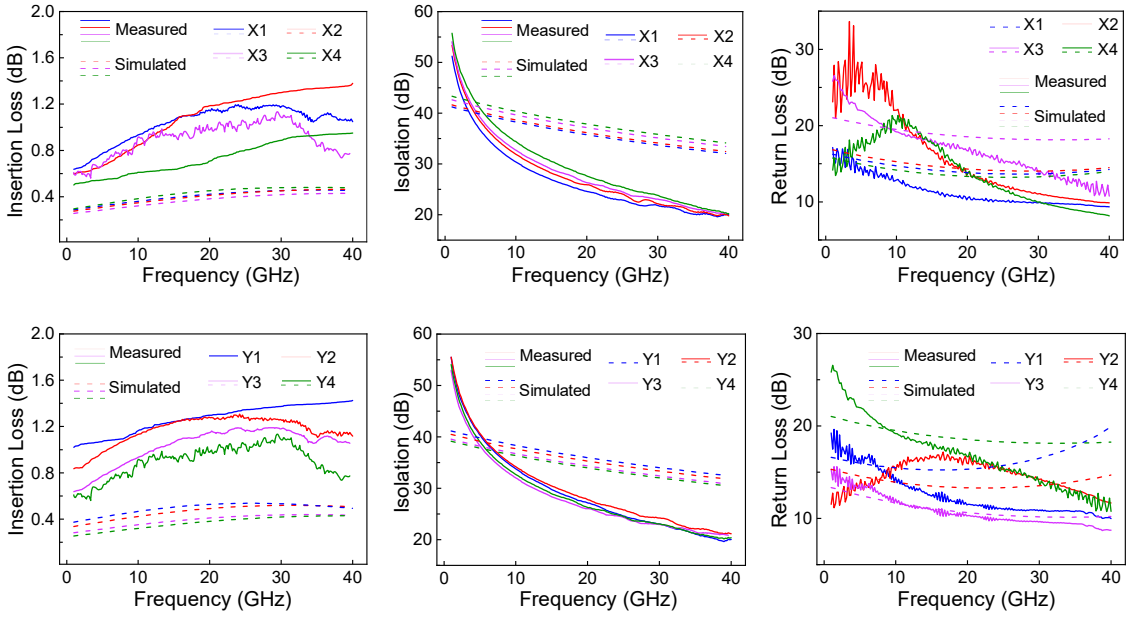

Figure 4.16. Measured high-frequency responses of all 8 types of fabricated wavy switches. Return loss corresponds to the on-state.

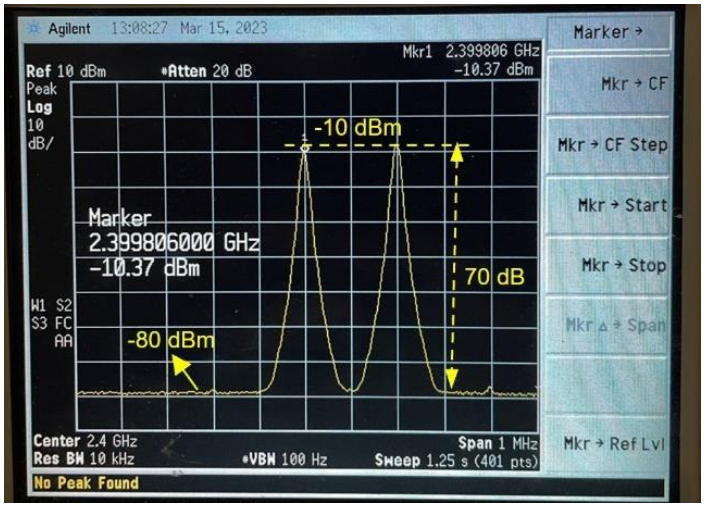

Figure 4.17. Output at spectrum analyzer during two tone IMD3 experiments for linearity characterization under an input power of 13 dBm.

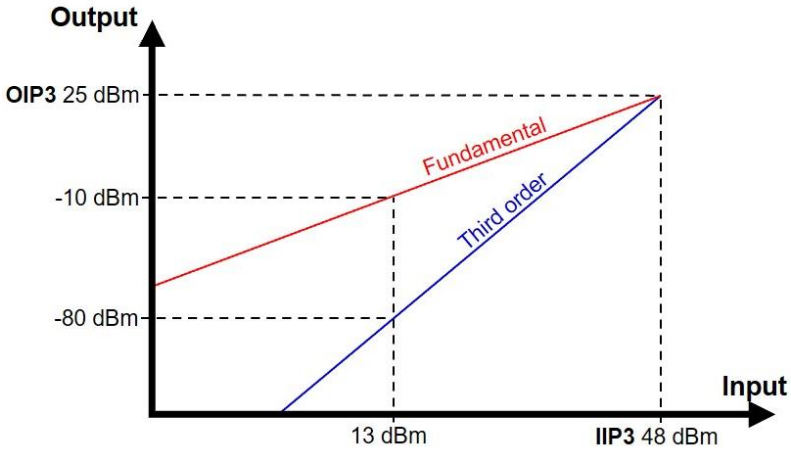

Figure 4.18. Characterized linearity of proposed wavy switches.

5. MACHINE LEARNING BASED MODELING AND OPTIMZATION OF RADIO-FREQUENCY ELECTROMECHANCIAL DEVICES[4]

5.1. Introduction

Ever-growing demands for high-speed wireless communication systems have put a more stringent constraint on the performance of radio frequency integrated circuits (RFICs), to keep up with the upcoming 5G standards. Therefore, along with better performing active circuitry, high performance RF passive components have also become a key to realize any modern-day RFIC transceiver. Unfortunately, owing to inherent technological limitations, RF passive devices based on standard IC fabrication techniques face a large number of losses (e.g., substrate proximity loss), and hence restrict the overall performance of RFICs [72, 73]. On the other hand, the field of MEMS (microelectromechanical systems) has surfaced as a potential substitute to fabricate integrated high performance on-chip RF passive components using advanced micromachining techniques[3, 72, 73]. MEMS based RF passives (i.e., inductors, tunable capacitors, switches, transformers, and phase shifters etc.), also referred to as RF-MEMS, exhibit high linearity, lower losses, high quality factors and better power handling abilities over larger bandwidths [7, 48, 74].

Nevertheless, the design of monolithic RF-MEMS passive components poses a primary technical challenge against the development of integrated RFICs. The coupled electromechanical nature of RF-MEMS components requires careful design and modeling of such devices in two different physical domains, thus formulating a typical

[4] Reprinted with permission from "Machine learning-based modeling and generic design optimization methodology for radio-frequency microelectromechanical devices" by R. Bajwa and M. K. Yapici, Sensors, 23, 4001, 2023. Copyright [2023] by MDPI.

multi-physics problem [75]. Hence, to achieve optimal performance metrics, a robust design optimization approach for RF-MEMS components is essential.

Generally, the design optimization techniques for RF-MEMS passive devices are based on intuitive approaches where designers focus on optimizing one or two most critical performance parameters (design objectives) while keeping others within pre-defined limits [76-78]. This approach, however being time-efficient, does not lead to an optimal design since it relies entirely on designers' very own expertise and experience. Therefore, to alleviate these design challenges, a more advanced optimization approach must be followed. Although, formal design optimization techniques exist and are quite common in the design of RFIC components [79-82] or typical MEMS devices [83, 84], such approaches have been overlooked for RF-MEMS devices which combine the two domains. For instance, an earlier work utilized metaheuristic optimization techniques to obtain optimal sets of design variables for planar CMOS RF inductors [80]. Similarly, in another work, a yield-aware multi-objective optimization strategy was introduced to optimize the accelerometer performance [83].

Undoubtedly, like any other conventional RF device, the performance of RF-MEMS devices largely depends on their geometry, and the design procedures may appear similar. However, their design process is certainly not the same and the optimization methods reported for conventional on-chip RF devices (optimized within a single domain, i.e. electromagnetic) cannot be directly applied to RF-MEMS type passive components. Unlike conventional RF devices, RF-MEMS components exhibit a non-traditional structure and operation along with a more involved design procedure spanning multiple physical domains where mechanical, electrical and electromagnetic performance trade-offs need to be carefully optimized [85]. This intertwined design process spanning various physical domains induces a need to address the design optimization aspect for RF-MEMS devices. However, for RF-MEMS devices, there exist only a handful of attempts, which address the design optimization issues [86-88]. Moreover, these efforts only focus on some specific RF application (e.g., RF switches) and mostly restrict their discussions to a single physical domain [86]. Consequently, current literature lacks in providing a generic multidisciplinary design optimization methodology for RF-MEMS.

Accordingly, to bridge the current gap in RF-MEMS device design process, this work demonstrates a comprehensive design optimization methodology for monolithic RF-MEMS passive devices using an automated multi-physics FEM (finite-element method) framework coupled with heuristic multi-objective optimization techniques through machine learning based surrogate models. For a certain design space, the FEM framework generates a data set describing the relation between input variables and corresponding device performance. Using this dataset, surrogate models are constructed that replace the extensive FEM simulations required in a typical iterative optimization process, thereby minimizing the computation cost overhead [82]. It is worthwhile to note that the computational cost of generating the dataset and corresponding surrogate models is essentially one-time investment, and these surrogate models can be used repeatedly to quickly optimize various design scenarios while by-passing the time-consuming FEM simulations.

Like many other real-life engineering optimization problems, optimization of RF-MEMS devices is also a multi-objective problem i.e., simultaneous optimization of many conflicting design objectives is needed. Likewise, a genetic algorithm-based multi-objective optimization algorithm (NSGA-II) is used in this work to optimize RF-MEMS devices [89]. The algorithm, NSGA-II, is capable of generating a set of optimal trade-offs (also called pareto front or non-dominated solution set) between conflicting design objectives within a single run, which makes it an ideal candidate to solve multi-objective design problems e.g., RF-MEMS. Both FEM and optimization simulations are performed using commercially available software i.e., COMSOL Multiphysics® (COMSOL, Inc., Burlington, MA) and MATLAB® (MathWorks, Inc., Portola Valley, CA). The remainder of this paper is organized in four different sections as follows: section II elaborates on the complete optimization methodology; sections III and IV present two optimization case studies i.e., RF-MEMS inductors and electrostatic switches; and lastly in section V, conclusions and future directions are given. To the authors' best knowledge, this is the first work that illustrates a generic optimization strategy for on-chip RF-MEMS devices.

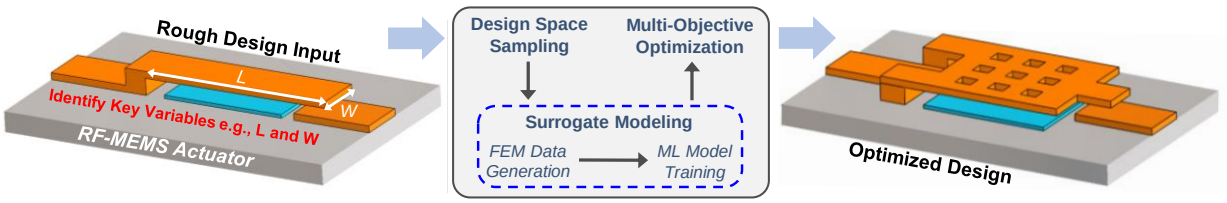

Figure 5.1. Schematic diagram demonstrating the generic design optimization methodology for RF-MEMS devices switching.

5.2. Proposed Multi-Objective Optimization Methodology

This section explains the proposed optimization methodology for RF-MEMS devices by providing details on the main steps involved in the process. A schematic illustration of the proposed optimization method is presented in Fig. 5.1.

5.2.1. Problem Definition

First step for the overall optimization approach is to formulate the target problem appropriately. To do so, critical performance parameters (design objectives), which need to be maximized or minimized for the intended device (e.g., capacitor, inductor etc.) are identified. Next, the relevant design variables (which serve as an input to optimization problem) are defined within the feasible upper and lower bounds. Lastly, linear/non-linear design constraints and the fixed design parameters are added to problem, which conclude the problem definition.

To elaborate further, consider the optimization problem of an RF-MEMS device labeled as '*A*', where the design objectives to be optimized are given by a vector $\boldsymbol{J_A}$. Meanwhile, the input variables are represented by $\boldsymbol{x_A}$, and the design constraints and fixed parameters are $\boldsymbol{G_A}$ and $\boldsymbol{P_A}$, respectively. The design problem can then be mathematically expressed as:

Design variables	:	$\boldsymbol{x_A} = \{x_{A1}, \ldots\ldots, x_{An}\}$
Optimize $\boldsymbol{J_A}$	:	$\boldsymbol{J_A} = \{J_{A1}, \ldots\ldots, J_{Am}\}$
Subject to $\boldsymbol{G_A} \leq 0$	:	$\boldsymbol{G_A} = \{G_{A1}, \ldots\ldots, G_{Ap}\}$
Fixed parameters	:	$\boldsymbol{P_A} = \{P_{A1}, \ldots\ldots, P_{Aq}\}$

where *n, m, p,* and *q* are the numbers of input design variables, design objectives, design constraints, and fixed parameters, respectively.

5.2.2. Finite Element Modeling Framework

To accurately model the electromechanical behavior of RF-MEMS devices, a sequentially-coupled simulation routine consisting of structural analysis and high-frequency analysis is established. Corresponding to the values of the given design variables, first, structural modeling is performed, and the relevant results are recorded. Results from structural simulations are then fed to the high frequency simulation setup, where RF performance parameters are extracted. In this way, the effects of design variables on both structural and high-frequency performance parameters/objectives of the RF-MEMS devices are analyzed. The simulation setup is automated by means of MATLAB scripts to ensure automatic exploration of the whole design space, which is essential to locate the optimal points when FEM codes are subjected to optimization algorithms.

5.2.3. Surrogate Modeling

Ideally, for multi-objective design problems, FEM codes are directly linked with heuristic optimizers, where they are iteratively executed tens of thousands of times in search for optimal solution space or a pareto front [82]. However, FEM simulations are computationally expensive, and hence drastically increase the time and computational costs for the overall optimization process. Alternatively, machine learning techniques can be used to map the FEM simulation data over the desired design space, into intelligent yet computationally cheap surrogate models capable of performing accurate predictions

during optimization iterations. This technique, although being less accurate, can drag down the computational costs into reasonable limits [81, 82].

Similarly, to limit the computational costs, machine learning enabled surrogate modeling approach is employed in this work. First, the design space chosen in problem definition (i.e., range of design variables) is sampled. To effectively explore the whole design space, Latin Hypercube sampling technique is chosen. For this work, the sampling size is restricted to 5^n, where n corresponds to the number of design variables present in the problem. It should be noted that the sampling of 5^n size has been chosen carefully to minimize the time required for data generation with FEM simulations, while efficiently covering the whole design space. However, the number of samples can be increased if one needs to cover a complex design space. Next, FEM simulations are carried out for the entire sampled design space and corresponding values of the design objectives are recorded.

Later, this FEM-driven dataset is utilized to train the decision-tree-based regression models using the "Statistics and Machine Learning Toolbox" of MATLAB®, which directly reflect the input-output relationship between design variables and objectives. Initially, various model presets (including support vector machines, regression trees and linear regression models) offered by MATLAB 'Regression Learner' module are used to fit the data generated through FEM simulations. Among them, regression trees are selected for this work, since they have high interpretability, low computational cost, high prediction accuracy, and can well capture non-linear relationship in data [90-92]. However, it must be noted that no ML model can serve as the "universal" model or fit to all types of datasets, and therefore the optimal model type may vary among different datasets. For our dataset, we observed that regression trees offer fastest training time and highest accuracy among all compared models.

Regression trees are a variant of decision trees, which fit real-valued numerical data. Regression trees work on the principle of binary recursive splitting, which corresponds to an iterative process of successively splitting data into two branches, mimicking a tree-like structure, where the split location is decided based on the mean square error ("split rule": data is split at the location which results in minimum mean squared error). In

particular, the algorithm starts by grouping all the data records in one partition, which is called the “root node”. Next, the splitting process starts and continues in each branch, until the partition size falls below a certain threshold, or the mean squared error within the partition falls to zero, representing the “leaf nodes”. Moreover, *k*-fold validation scheme is adopted during the training of regression tree models, where $k = 5$. The accuracy of these metamodels is ensured by tracking commonly used accuracy metrics including root mean square error (RMSE), relative RMSE, and coefficient of determination (R^2).

5.2.4. Multi-Objective Optimization

The trained surrogate models, along with the information on design variables and constraints, are then subjected to a multi-objective optimizer that reveals pareto optimal points for conflicting design objectives. In the proposed approach, a variant of non-dominated sorting genetic algorithm (NSGA-II) is utilized to solve the RF-MEMS optimization problem [89]. The terms non-dominated solution set and pareto front are interchangeably used, and defined as the points where no further improvement in one objective is possible without degrading at least one of the other objectives.

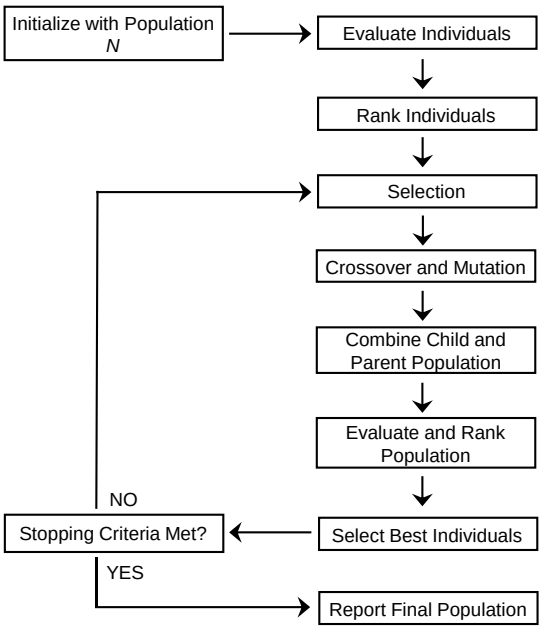

Figure 5.2. NSGA-II algorithm flowchart [89].

The algorithm starts with an initial design variables' population of size *N*. To ensure a thorough exploration of whole design space, population size was set to 200 in this work. Next, initial population is evaluated to get the respective objective functions' values (fitness values). Evaluated population is then ranked based on their fitness values and the best individuals among them are selected as a parent population. In this work, the best half (50%) of the whole population is selected as parent population, while the other half is discarded. By means of genetic operators (crossover and mutation), a child population is then created from parent population and both child/parent populations are merged to make a single extended population. For this work, crossover fraction and mutation rate are set to 0.8 and 0.05, respectively. At this point, all the individuals of the extended population are evaluated to get the corresponding objective functions' values associated with them. Lastly, the individuals of extended population are ranked and sorted on the basis of their non-dominance level. The best individuals from sorted individuals' set are selected as the parent population for the next iteration and fed back to genetic operators. This iterative cycle continues until the stopping criteria is met i.e., when the average relative difference between non-dominated sets of two consecutive iterations falls below a certain value ($1e^{-4}$ is used as a threshold value). A complete flowchart of NSGA-II algorithm can be viewed in Fig. 5.2.

5.3. Case Study: RF-MEMS Suspended Inductor Optimization

On-chip inductors are widely used in many RF transceiver blocks such as low noise amplifiers, voltage-controlled oscillators, DC-DC converters, matching circuits and passive filters etc. [7]. Critical performance parameters for monolithic inductors are inductance (L), Q-factor (Q) and required footprint area. Conventional planar spiral geometries of RF inductors lying on a semiconductor substrate suffer from large substrate losses, and hence offer low Q-factor values [7]. Alternatively, to minimize substrate proximity losses, MEMS technologies offer many techniques to develop out-of-plane RF inductors with improved Q-factors. Some common techniques to develop 3D high-Q on-chip inductors are plastic deformation magnetic assembly to achieve vertical inductors

[1], thick photoresist processing to fabricate elevated suspended inductors [93], and stress-induced self-assembled thin film inductors [7] etc.

For this case study, MEMS-based stress-induced self-assembled on-chip loop inductors were considered to demonstrate the functionality of the proposed design optimization methodology. To maximize inductor performance while minimizing the footprint area, three design objectives were chosen i.e., *Q*-factor, inductance (nH) and area (mm^2). Furthermore, the geometrical parameters of inductor coil i.e., radius (*r*), conductor width (*w*) and metal thickness (*t*), and the operating frequency (*f*) were taken as design variables (Table 5.1).

Table 5.1. Design variables for RF-MEMS inductor.

Design variables	**Lower bound**	**Upper bound**
Thickness (*t*)	1 µm	5 µm
Coil radius (*r*)	300 µm	600 µm
Width (*w*)	60 µm	100 µm
Frequency (*f*)	1 GHz	5 GHz

Although RF-MEMS inductors offer excellent RF performance, their mechanical reliability is limited, primarily due to their suspended structure [28], which inherently complicates the design process and makes the manual design optimization even more challenging. To address this issue in our case study, we constrained the maximum stress value (*S*) in inductor structure below the yield strength of material (205 MPa for gold, which is used as a structural material in simulations), to ensure a mechanically reliable design. A simplified 2D top view of inductor layout is provided in Fig. 5.3(a).

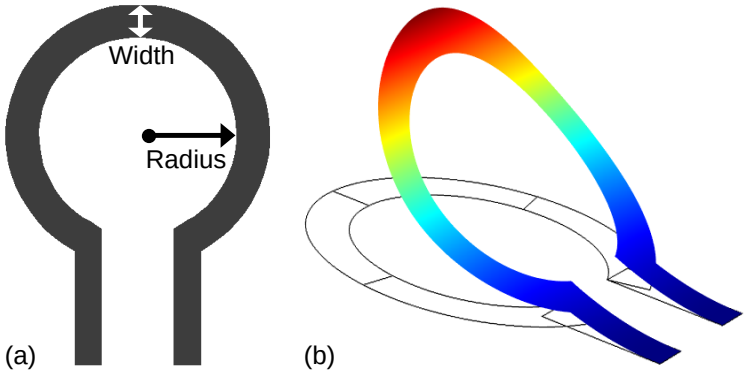

Figure 5.3. Self-assembled RF-MEMS ring inductor: (a) Top view of the planar ring inductor geometry prior to out-of-plane self-assembly; and (b) post self-assembly view of the deformed ring inductor.

5.3.1. Finite Element Modeling of RF-MEMS Loop Inductors

Stress induced self-assembly of patterned thin films into out-of-plane loop inductors was studied using a static structural analysis where self-assembly process was artificially replicated using quasi-static FEM simulations [32]. Modeling results for the structural deformation of a typical ring inductor are shown in in Fig. 5.3(b).

The deformed inductor geometries obtained from mechanical analysis were then imported to the next FEM code where high-frequency AC analysis was performed. The inductors were treated as two-port RF networks and relevant z-parameters were extracted at the target frequencies. The z-parameters for inductors were then converted to *Q*-factor and inductance values through the following relationships:

$$Q = \frac{\mathrm{Im}(Z_{11})}{\mathrm{Re}(Z_{11})} \tag{1}$$

$$L = \frac{\mathrm{Im}(Z_{11})}{\omega} \tag{2}$$

5.3.2. Multi-Objective Optimization

Prior to solving the optimization problem, the defined design space for inductors was sampled with a sampling size of 5^3(125), to fully cover the entire design space. Next, the FEM code (containing mechanical and EM simulations, as described above) was run in an automated loop for all 125 samples to acquire the corresponding values for design objectives (*Q, L* and area), which took 31 h using an Intel core i5 computer. This FEM data was then used to train the regression trees, where the training time was 0.5 s. The accuracy of the developed metamodels of inductance and *Q*-factor was validated using the metrics listed in Table 5.2.

Table 5.2. Accuracy metrics for meta-models of L and *Q*.

Objective	**R^2**	**RMSE**	**Relative RMSE**
Inductance (*L*)	0.91	0.14	8%
Q-factor (*Q*)	0.92	0.75	4%

To comprehensively model the trade-offs between the performance parameters of MEMS inductors, various combinations of design objectives were exploited. Initially, only two design objectives (inductance and area) were considered to trace the optimal inductance density points at a frequency of 5GHz. In this particular case, the inductor optimization problem can be mathematically expressed as:

Design variables	*:*	$x = \{r, w, t\}$
Optimize J	*:*	$J = \{L, area\}$
Subject to G	*:*	$G = \{Q \geq 10, S \leq 205\ MPa\}$
Fixed parameters	*:*	$P = \{f = 5\ GHz\}$

With these conditions, the developed surrogate models were subjected to optimizer, and the extracted non-dominated solution set for inductance and footprint area is presented in Figure 4a. Interestingly, coil's inductance and footprint area exhibit strong conflicting nature; in other words, the inductance of a coil is directly proportional to the coil diameter, whereas the footprint area increases with the increasing diameter [94]. A similar trend was observed for the inductance-area pareto plot (Fig. 5.4(a)), where the inductance first increased sharply with an increasing area. However, for area above 0.3mm^2, the inductance followed a near-linear trend.

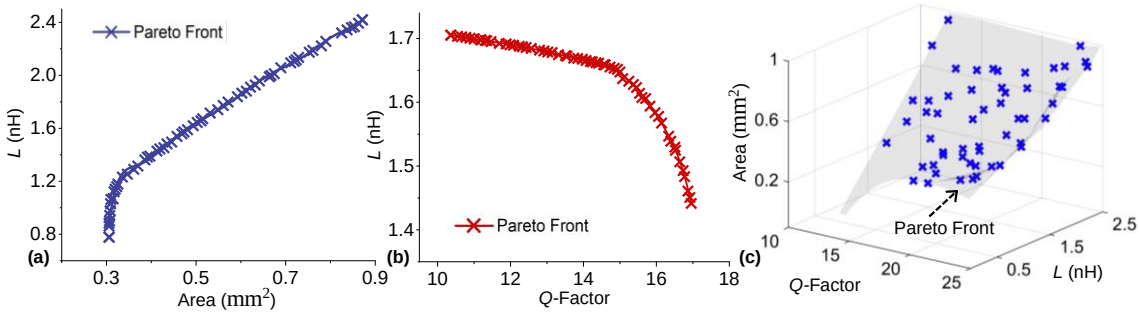

Figure 5.4. Non-dominated solution sets for RF-MEMS inductor optimization problem: (a) inductance vs. area; (b) *Q*-factor vs. inductance; and (c) *Q*-factor vs. inductance vs. area.

Another noticeable trade-off in the inductor design process is displayed by the correlation between inductor's quality factor and inductance. For instance, an increased coil diameter promises an increased coil inductance, but on the other hand, reduces the coil *Q*-factor simultaneously due to increased series resistance [31]. Likewise, for the selected design space, a search for pareto front between inductor's inductance and *Q*-factor was performed, indicating the below formulated optimization problem.

Design variables	:	$x = \{r, w, t\}$
Optimize J	:	$J = \{Q, L\}$
Subject to G	:	$G = \{Area \leq 1\ mm2, S \leq 205\ MPa\}$
Fixed parameters	:	$P = \{f = 5\ GHz\}$

The obtained pareto front plotted in Fig. 5.4(b) illustrates the complex conflicting relationship between *Q*-factor and inductance, where inductance initially decreases slowly with an increase in *Q*-factor, and then suddenly starts to drop near *Q*-factor of 15.

To demonstrate the applicability of proposed methodology to a higher number of design objectives, a search for pareto optimal points between all three design objectives (*Q*, *L* and area) was performed, which revealed a three-dimensional pareto front shown in Figure 4c. The optimization problem in such case can be expressed as:

Design variables	*:*	$x = \{r, w, t\}$
Optimize J	*:*	$J = \{Area, Q, L\}$
Subject to G	*:*	$G = \{S \leq 205\ MPa\}$
Fixed parameters	*:*	$P = \{f = 5\ GHz\}$

In above-described optimization scenarios, the frequency was fixed to 5 GHz. Nevertheless, the proposed methodology can easily be tailored to achieve the broadband optimization of RF-MEMS devices. Since the frequency is taken as an input variable in this case study (Table 5.1), the developed surrogate models essentially describe the frequency-dependent input-output behavior of RF-MEMS inductors. That is to say, following the development of frequency-dependent surrogate models, the inductors can be quickly optimized for various operating frequencies by directly using these frequency-dependent surrogate models. To further illustrate this idea, we optimized the inductor surrogate models at 4 different frequencies (1, 2, 3 and 4 GHz) and extracted the corresponding pareto optimal points, as plotted in Fig. 5.5. These intrinsic trade-off curves, related to the inductor geometry and relevant performance parameters, are difficult to extract and optimize, manually. Hence, information on the optimality of such trade-offs is highly valuable to RF designers.

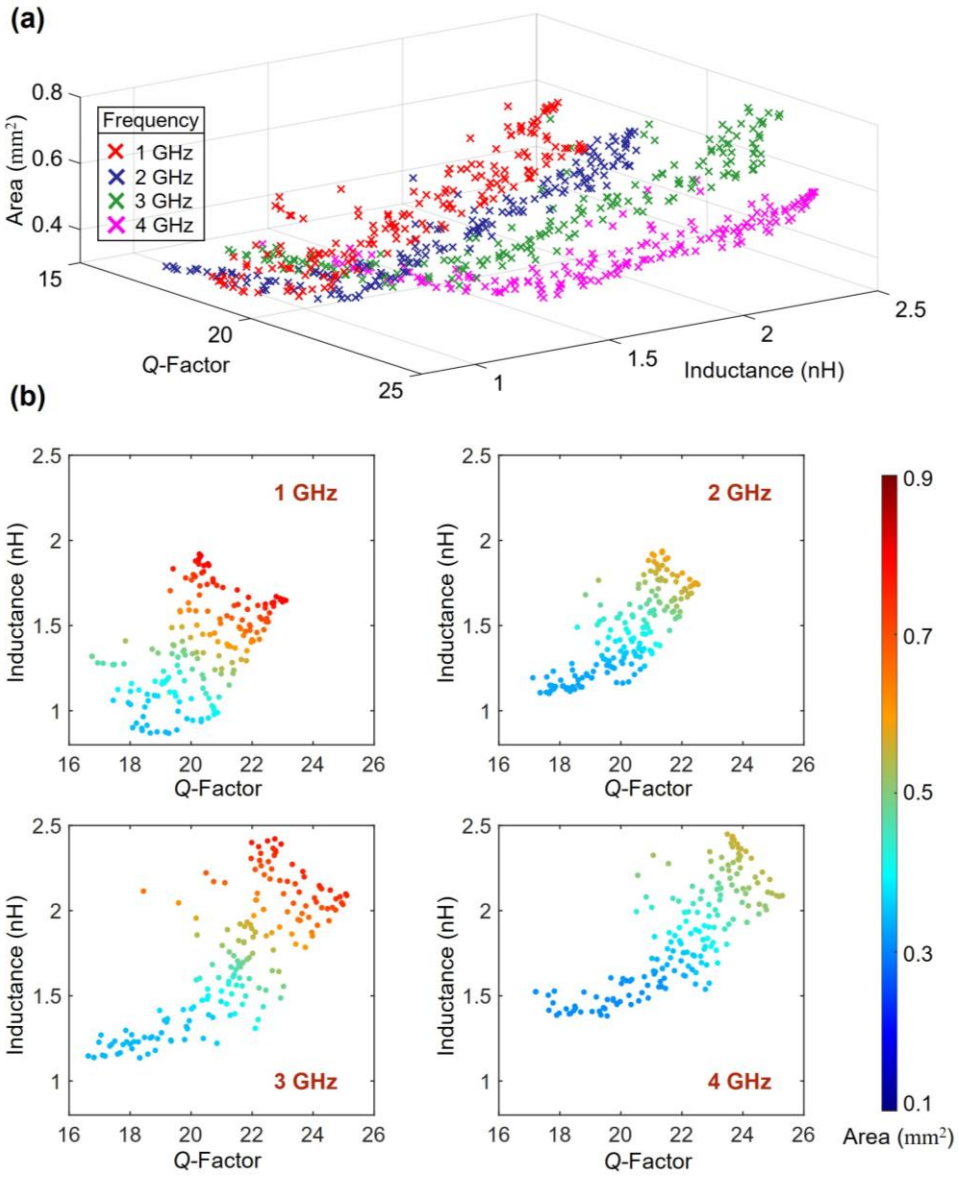

Figure 5.5. Pareto fronts for RF-MEMS inductor at 4 different frequencies between 1-5 GHz: (a) combined pareto plot for all frequencies; and (b) individual pareto plots at different frequencies.

5.4. Case Study: RF-MEMS Switch Optimization

MEMS switches play a key role in many RF circuitries for routing signals through transmission lines. Compared to their active counterparts (i.e., transistor switches),

MEMS switches are highly linear, offer lower ON-state losses, higher OFF-state isolation over a wide bandwidth [74]. Among many actuation principles, electrostatic actuation is most commonly used in RF switches because of its simple operation and ease of integration with standard IC fabrication processes [41, 95]. Correspondingly, cantilever-based series RF-MEMS switches were selected as a second demonstrator to further highlight the significance and validate the adaptability of the formal design optimization method reported herein.

Electrostatic RF-MEMS switches are characterized by three major performance parameters including: the actuation voltage or pull-in voltage (V_P), ON-state insertion loss ($S_{21\text{-}ON}$), and OFF-state signal isolation ($S_{21\text{-}OFF}$), which were considered as the design objectives for this study. Since RF-MEMS switches indicate a complex electromechanical system and are prone to reliability issues such as stiction [44], this case study also considers two highly critical reliability-related design constraints i.e., maximum stress at anchors during actuation (S) and beam stiffness (k), thereby demonstrating a more practical optimization route via proposed optimization methodology. Moreover, the design variables considered for electrostatic series switch were length (l), width (w), thickness (t) of the cantilever beam and the air gap (g) between beam and underlying actuation electrode. Lower and upper limits on the values that can be assumed by the target design variables are summarized in Table 5.3, while the topology of the series MEMS switch subject to the optimization workflow described in this work is shown in Fig. 5.6.

Table 5.3. Design variables for RF-MEMS switch.

Design variables	**Lower bound**	**Upper bound**
Thickness (t)	1 µm	5 µm
Gap (g)	2 µm	8 µm
Width (w)	50 µm	80 µm
Length (l)	300 µm	600 µm

5.4.1. FEM Modeling of RF-MEMS Switches

To extract information on actuation voltages, MEMS switches are first modeled as electromechanical structures representing a multi-physics problem. Following the definition of necessary boundary conditions, the voltage between the cantilever switch and underlying DC electrode is increased gradually, which induces a proportional deflection in the fixed-free cantilever switch. At this point, the electrostatic forces are balanced by the elastic restoring force of the cantilever. However, with increasing voltage, when the electrostatic forces outrun the spring restoring forces, the system gets unstable and the moveable cantilever beam collapses down to the fixed DC electrode (pull-in point, Fig. 5.6(c)).

From FEA perspective, no stable static solution exists for electrostatic actuators at voltage values greater than or equal to pull-in voltage, and hence the solution diverges. Consequently, locating the exact pull-in value directly is not possible with FEM solvers and solution divergence is usually treated as an indicator to estimate the pull-in voltage [96]. Thus, to achieve a more precise estimation on the pull-in voltages for specified MEMS switches in an automatic fashion, an iterative algorithm was established that could locate the pull-in voltage values with a maximum error of less than 0.1 V. The key steps for the automatic detection of pull-in voltage are listed below:

1. Apply the initial voltage $V_0 = 0$ volts.
2. Solve for electromechanical forces. If the solution converges, go to step 3, else reduce the increment voltage V_1 by half i.e., $V_1 = 0.5V_1$, to gradually converge to a solution and go to step 4.
3. Increase the applied voltage with an increment of V_1 (volts) i.e., $V_0 = V_0 + V_1$. Go back to step 2.
4. If $V_1 < 0.05$V (tolerance for stopping criteria), go to step 7, else decrease the applied voltage i.e., $V_0 = V_0 - V_1$, and go to next step.
5. Solve for electromechanical forces. Replace $V_1 = 0.5V_1$. If solution converges go to step 6, else go back to step 4.
6. If $V_1 < 0.05$V (tolerance for stopping criteria), go to step 7, else increase the applied voltage with an increment of V_1 (volts) i.e., $V_0 = V_0 + V_1$. Go back to step 5.
7. Stop the code. Pull-in voltage (V_P) = current value of V_0.

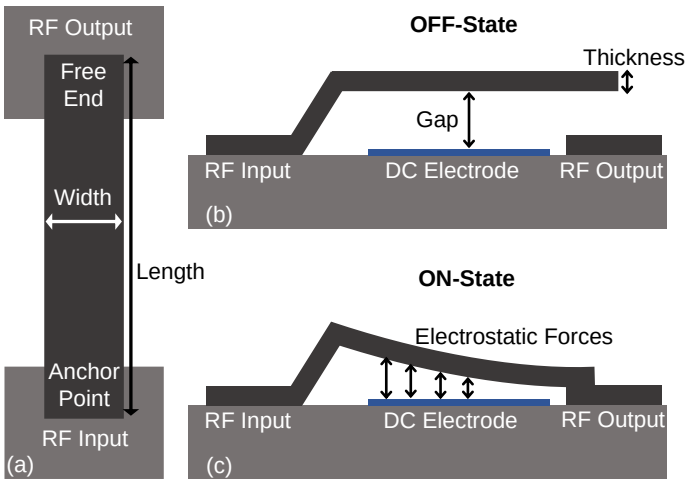

Figure 5.6. Cantilever-based series RF-MEMS switch: (a) top view; (b) side view in OFF-state; and (c) side view in ON-state.

Once the pull-in study was concluded, switch geometries for both ON-state and OFF-state were analyzed for their high-frequency responses. Considering the sizeable contribution of MEMS switches for mm-wave band circuits, the operating frequency for this study was fixed at 28 GHz. The high-frequency models for switches were solved for two-port network s-parameters, specifically S_{21}, which represents the insertion losses and signal isolation for the switch in ON-state and OFF-state, respectively.

1.1.1. Multi-Objective Optimization

Initially, the design space for RF-MEMS switches was sampled into 5^4 (625) samples and the corresponding values for design objectives (insertion loss, isolation, and actuation voltage) were obtained using an automated FEM code, accounting for approximately 104 hours of computation time on an Intel core i5 computer. Subsequently, this dataset of size 625 was used for regression model training, with training time of ~1.6 s. The accuracy of trained metamodels for the objective functions of RF-MEMS switch is illustrated in Table 5.4.

Table 5.4. Accuracy of meta-models of switch's objective functions

Objective	R^2	RMSE	Relative RMSE

Pull-in voltage	0.94	0.69	5%
Insertion Loss	0.96	0.09	2%
Isolation	0.90	0.78	7%

At this stage, the equivalent surrogate models acquired for the design objectives of the switch were subjected to the optimizer and multi-objective optimization was performed. Essentially, the effects of geometrical parameters of switch on the corresponding RF isolation and actuation voltage values are contradictory to each other, which originates a non-trivial trade-off in electrostatic MEMS switch design process [72]. For example, an increased air gap between the switch beam and the underlying electrode improves the RF-isolation, but at a cost of higher actuation voltage [72]. Accordingly, we first identified the pareto optimal points for RF isolation and actuation voltage for the considered electrostatic series MEMS switch using a non-dominated sorting algorithm, and this optimization scenario can be formulated as:

Design variables	*:*	$x = \{l, w, t, g\}$
Optimize J	*:*	$J = \{V_P, S_{21\text{-}OFF}\}$
Subject to G	*:*	$G = \{k \geq 10\ N/m,\ S \leq 205\ MPa\}$
Fixed parameters	*:*	$P = \{f = 28\ GHz\}$

Notably, to ensure a mechanically robust design, the maximum stress at switch anchors was constrained below the yield strength of switch material (gold). Meanwhile, the beam stiffness was restricted above 10 N/m, as suggested in [44]. The extracted optimal solution set shown in Fig. 5.7 validates the contrasting behavior of pull-in voltage and RF isolation, where for the chosen design space, the optimal isolation and pull-in values vary from 3 V to 30 V and 15.5 dB to 24.2 dB, respectively. Furthermore, identification of these variations in an optimal solution set enables designers to explore the design space, effectively.

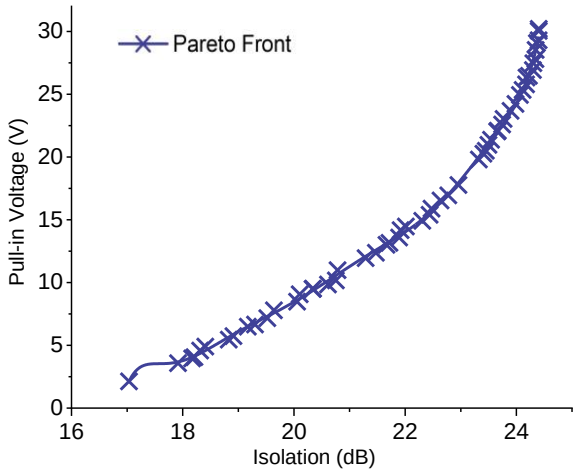

Figure 5.7. Set of optimal trade-offs between the RF-isolation and pull-in voltage of the cantilever-based series RF-MEMS switch.

Lastly, to fully optimize the overall performance of the switch, a multi-objective pareto search with all the design objectives was carried out and the corresponding three-dimensional pareto front shown in Fig. 5.8 was obtained. The relevant mathematical formulation for this optimization case is given as:

Design variables	:	$\boldsymbol{x} = \{l, w, t, g\}$
Optimize J	:	$\boldsymbol{J} = \{V_P, S_{21\text{-}ON}, S_{21\text{-}OFF}\}$
Subject to G	:	$\boldsymbol{G} = \{k \geq 10\ N/m,\ S \leq 205\ MPa\}$
Fixed parameters	:	$\boldsymbol{P} = \{f = 28\ GHz\}$

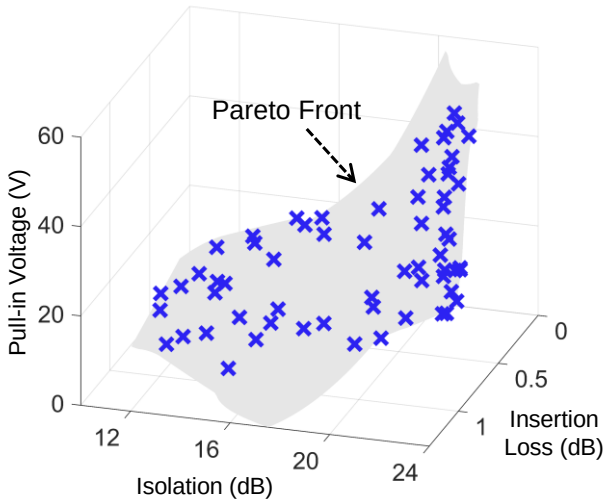

Figure 5.8. Three-dimensional pareto front demonstrating trade-off between actuation voltage, RF isolation and insertion loses for the RF-MEMS series switch.

For a fixed design space, the 3D plot comprehensively displays the relationships among various design objectives and can be used as a tool to handle various design scenarios. For instance, considering a design problem where low pull-in voltage is the prime requirement, a pareto optimal design with lowest pull-in voltage can be readily identified and selected from the plot.

2. CONCLUSIONS

This work attempts to solve a well-known yet complex issue relating to the limited performance of passive devices manufactured on radio-frequency integrated circuits with traditional methods. We show that stress-engineering can be a viable alternative to traditional IC fabrication techniques, when fabricating RF passive devices. Our results reveal that RF passive devices fabricated using stress-engineering beat the current state-of-the-art based on conventional technologies by a large margin, while this newly proposed methodology stays fully IC-compatible. In addition, we also illustrate the benefits of employing machine learning-driven modeling techniques in optimizing MEMS-based RF devices for extreme performance. More detailed conclusions on the findings of this thesis are listed below.

1. In this work, we have presented the fabrication and packaging of self-assembled 3D ring inductors for RF applications. We have demonstrated the use of two standard IC thin film materials, copper and chromium, in creating 3D inductor geometries, simply by adjusting the film thickness and stress. The 3D ring inductors exhibit a 300% increase in the *Q*-factor compared to their flat counterparts, which verifies the potential of our stress-induced self-assembly technique. We have then put forward a new packaging technique for suspended inductors, in which we coat them with a polymer by using the volumetric dispensing method. We have shown that volumetric dispensing enables a quasi-static coating process, which is essential for preserving the inductor shape during packaging. This polymer encapsulation successfully alleviates various reliability issues commonly linked with suspended inductors, thereby illustrating the practical significance of proposed packaging method. Furthermore, our encapsulation technique is generic and can be extended to package other on-chip non-moveable 3D passive components as well.

2. We have introduced a new class of radio-frequency MEMS switches based on wavy-shaped microactuators fabricated through a simple and fully IC compatible process. We characterized our devices in detail, including their electromechanical and high-frequency responses. Our in-line series wavy switches actuate at voltages as low as 24 V while maintaining large RF isolation and low insertion loss for frequencies up to 40 GHz, demonstrating a significant improvement over current state-of-the-art devices and indicating a massive potential for application in emerging high-data-rate communication systems. Through the application of a wavy bending profile in originally flat cantilever switches, a strict fundamental performance tradeoff between RF isolation and actuation voltage can be successfully omitted, thus liberating an additional degree of freedom in the design process. Furthermore, we embedded our wavy microactuators within the simplest topology of MEMS switches (in-line series configuration) to better demonstrate the proposed concept, while our switches can be easily integrated into any other switch configuration to achieve even further improvement in the performance. In the future, this capability may be shown by integrating wavy switches in shunt configuration, a topology that is known to provide better RF performance at higher frequencies.

3. While recent studies attempt to satisfy the needs for RF-MEMS mainly by adding in more efficient novel designs to literature, the discussions in design optimization division are somewhat limited. The design optimization aspect, if modeled properly, not only improves the performance for any particular RF-MEMS device, but also provides a better insight of device's behavior to the RF designers. Accordingly, this study aims to highlight the significance of design optimization for RF-MEMS devices by presenting a machine learning based generic optimization approach. The overall optimization process is flexible and can easily be customized to fit any RF-MEMS device. The proposed strategy is validated for two common RF-MEMS devices (inductors and switches) using NSGA-II multi-objective optimization algorithm and corresponding results in the form of optimal design trade-offs (pareto fronts) are reported. The accuracy of reported results can be further verified with physical device realizations in future studies.

BIBLIOGRAPHY

[1] J. H. Chen, J. Zou, C. Liu *et al.*, "Design and modeling of a micromachined high-Q tunable capacitor with large tuning range and a vertical planar spiral inductor," *Ieee Transactions on Electron Devices,* vol. 50, no. 3, pp. 730-739, 2003.

[2] J. M. López-Villegas, J. Samitier, J. Bausells *et al.*, "Study of integrated RF passive components performed using CMOS and Si micromachining technologies," *Journal of Micromechanics and Microengineering,* vol. 7, no. 3, pp. 162, 1997.

[3] X. Yu, W. Huang, M. Y. Li *et al.*, "Ultra-Small, High-Frequency, and Substrate-Immune Microtube Inductors Transformed from 2D to 3D," *Scientific Reports,* vol. 5, 2015.

[4] C. L. Chua, D. K. Fork, K. V. Schuylenbergh *et al.*, "Out-of-plane high-Q inductors on low-resistance silicon," *Journal of Microelectromechanical Systems,* vol. 12, no. 6, pp. 989-995, 2003.

[5] R. Bajwa, and M. K. Yapici, "Origami-Inspired Fabrication of High-Performance Wafer-Level Packaged Three-Dimensional Radio-Frequency Inductors," *Journal of Microelectromechanical Systems,* 2023.

[6] R. Bajwa, H. Saleh, M. Shojaeian *et al.*, "Nonlinear restructuring of patterned thin films by residual stress engineering into out-of-plane wavy-shaped electrostatic microactuators for high-performance radio-frequency switches," *Microsystems & Nanoengineering,* vol. 9, no. 1, 2023.

[7] R. Bajwa, and M. K. Yapici, "Intrinsic stress-induced bending as a platform technology for controlled self-assembly of high-Q on-chip RF inductors," *Journal of Micromechanics and Microengineering,* vol. 29, no. 6, pp. 064002, 2019.

[8] R. Bajwa, and M. K. Yapici, "Machine Learning-Based Modeling and Generic Design Optimization Methodology for Radio-Frequency Microelectromechanical Devices," *Sensors,* vol. 23, no. 8, 2023.

[9] M. T. K. Hou, and R. S. Chen, "Effect of width on the stress-induced bending of micromachined bilayer cantilevers," *Journal of Micromechanics and Microengineering,* vol. 13, no. 1, pp. 141-148, 2003.

[10] J. P. Raskin, F. Iker, N. Andre *et al.*, “Bulk and surface micromachined MEMS in thin film SOI technology,” *Electrochimica Acta,* vol. 52, no. 8, pp. 2850-2861, 2007.

[11] R. Majumdar, and I. Paprotny, “Configurable Post-Release Stress-Engineering of Surface Micro-Machined MEMS Structures,” *Journal of Microelectromechanical Systems,* vol. 26, no. 3, pp. 671-678, 2017.

[12] S. S. Huang, and X. Zhang, “Extension of the Stoney formula for film-substrate systems with gradient stress for MEMS applications,” *Journal of Micromechanics and Microengineering,* vol. 16, no. 2, pp. 382-389, 2006.

[13] S. Shiri, P. Ashtijoo, A. Odeshi *et al.*, “Evaluation of Stoney equation for determining the internal stress of DLC thin films using an optical profiler,” *Surface & Coatings Technology,* vol. 308, pp. 98-100, 2016.

[14] J. Schicker, W. A. Khan, T. Arnold *et al.*, “Simulating the warping of thin coated Si wafers using Ansys layered shell elements,” *Composite Structures,* vol. 140, pp. 668-674, 2016.

[15] P. Tyagi, N. Bassik, T. G. Leong *et al.*, “Self-Assembly Based on Chromium/Copper Bilayers,” *Journal of Microelectromechanical Systems,* vol. 18, no. 4, pp. 784-791, 2009.

[16] O. F. Hikmat, and M. S. M. Ali, “RF MEMS Inductors and Their Applications—A Review,” *Journal of Microelectromechanical Systems,* vol. 26, no. 1, pp. 17-44, 2017.

[17] H. T. Le, R. I. Haque, Z. Ouyang *et al.*, “MEMS inductor fabrication and emerging applications in power electronics and neurotechnologies,” *Microsystems & Nanoengineering,* vol. 7, no. 1, pp. 59, 2021.

[18] G. W. Dahlmann, E. M. Yeatman, P. Young *et al.*, “Fabrication, RF characteristics and mechanical stability of self-assembled 3D microwave inductors,” *Sensors and Actuators A: Physical,* vol. 97-98, pp. 215-220, 2002.

[19] V. M. Lubecke, B. Barber, E. Chan *et al.*, “Self-assembling MEMS variable and fixed RF inductors,” *IEEE Transactions on Microwave Theory and Techniques,* vol. 49, no. 11, pp. 2093-2098, 2001.

[20] M. K. Yapici, J. M. Hong, J. Zou *et al.,* "Post-CMOS on-chip integration of 3D MEMS inductors using a novel chip embedding technique." *Transducers &*

Eurosensors XXVII: The 17th International Conference on Solid-State Sensors, Actuators and Microsystems, Barcelona, Spain, 2013, pp. 128-131.

[21] X. Yu, W. Huang, M. Li *et al.*, “Ultra-Small, High-Frequency and Substrate-Immune Microtube Inductors Transformed from 2D to 3D,” *Scientific Reports*, vol. 5, no. 1, pp. 9661, 2015.

[22] C. Yun-Seok, Y. Euisik, and Y. Jun-Bo, "Encapsulation of the micromachined air-suspended inductors." *IEEE MTT-S International Microwave Symposium Digest*, Philadelphia, PA, USA, 2003, pp. 1637-1640 vol.3.

[23] Y. Jun-Bo, K. Bon-Kee, H. Chul-Hi *et al.*, "High-performance electroplated solenoid-type integrated inductor (SI/sup 2/) for RF applications using simple 3D surface micromachining technology." *International Electron Devices Meeting*, San Francisco, CA, USA, 1998 pp. 544-547.

[24] M. Rais-Zadeh, P. A. Kohl, and F. Ayazi, “MEMS Switched Tunable Inductors,” *Journal of Microelectromechanical Systems*, vol. 17, no. 1, pp. 78-84, 2008.

[25] W. Xi-Ning, Z. Xiao-Lin, Z. Yong *et al.*, “Fabrication and performance of a novel suspended RF spiral inductor,” *IEEE Transactions on Electron Devices*, vol. 51, no. 5, pp. 814-816, 2004.

[26] Y. Jun-Bo, K. Byeong-Il, C. Yun-Seok *et al.*, “3-D construction of monolithic passive components for RF and microwave ICs using thick-metal surface micromachining technology,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 1, pp. 279-288, 2003.

[27] M. Rais-Zadeh, J. Laskar, and F. Ayazi, “High Performance Inductors on CMOS-Grade Trenched Silicon Substrate,” *IEEE Transactions on Components and Packaging Technologies*, vol. 31, no. 1, pp. 126-134, 2008.

[28] Y. Li, J. Li, and L. Xu, “Failure mode analysis of MEMS suspended inductors under mechanical shock,” *Microelectronics Reliability*, vol. 85, pp. 38-48, 2018.

[29] R. Abermann, and H. P. Martinz, “Internal stress and structure of evaporated chromium and MgF2 films and their dependence on substrate temperature,” *Thin Solid Films*, vol. 115, no. 3, pp. 185-194, 1984.

[30] J. M. Lopez-Villegas, J. Samitier, C. Cane *et al.*, “Improvement of the quality factor of RF integrated inductors by layout optimization,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, no. 1, pp. 76-83, 2000.

[31] A. M. Niknejad, and R. G. Meyer, “Analysis, design, and optimization of spiral inductors and transformers for Si RF ICs,” *IEEE Journal of Solid-State Circuits,* vol. 33, no. 10, pp. 1470-1481, 1998.

[32] W. Huang, S. Koric, X. Yu *et al.*, “Precision Structural Engineering of Self-Rolled-up 3D Nanomembranes Guided by Transient Quasi-Static FEM Modeling,” *Nano Letters,* vol. 14, no. 11, pp. 6293-6297, 2014.

[33] H. H. Tawfik, M. Y. Elsayed, F. Nabki *et al.*, "Hard-Baked Photoresist as a Sacrificial Layer for Sub-180 °C Surface Micromachining Processes," *Micromachines,* 9, 2018.

[34] G. Murillo, Z. J. Davis, S. Keller *et al.*, “Novel SU-8 based vacuum wafer-level packaging for MEMS devices,” *Microelectronic Engineering,* vol. 87, no. 5, pp. 1173-1176, 2010.

[35] I. Zine-El-Abidine, and M. Okoniewski, “A Low-Temperature SU-8 Based Wafer-Level Hermetic Packaging for MEMS Devices,” *IEEE Transactions on Advanced Packaging,* vol. 32, no. 2, pp. 448-452, 2009.

[36] A. Mata, A. J. Fleischman, and S. Roy, “Fabrication of multi-layer SU-8 microstructures,” *Journal of Micromechanics and Microengineering,* vol. 16, no. 2, pp. 276, 2006.

[37] L. Che-Hsin, L. Gwo-Bin, C. Bao-Wen *et al.*, “A new fabrication process for ultra-thick microfluidic microstructures utilizing SU-8 photoresist,” *Journal of Micromechanics and Microengineering,* vol. 12, no. 5, pp. 590, 2002.

[38] H. Lorenz, M. Despont, N. Fahrni *et al.*, “SU-8: a low-cost negative resist for MEMS,” *Journal of Micromechanics and Microengineering,* vol. 7, no. 3, pp. 121, 1997.

[39] W. Huang, J. Zhou, P. J. Froeter *et al.*, “Three-dimensional radio-frequency transformers based on a self-rolled-up membrane platform,” *Nature Electronics,* vol. 1, no. 5, pp. 305-313, 2018.

[40] Z. Yang, M. D. Kraman, Z. Zheng *et al.*, “Monolithic Heterogeneous Integration of 3D Radio Frequency L−C Elements by Self-Rolled-Up Membrane Nanotechnology,” *Advanced Functional Materials,* vol. 30, no. 40, pp. 2004034, 2020.

[41] L. Y. Ma, N. Soin, M. H. M. Daut *et al.*, “Comprehensive Study on RF-MEMS Switches Used for 5G Scenario,” *IEEE Access,* vol. 7, pp. 107506-107522, 2019.

[42] G. M. Rebeiz, K. Entesari, I. C. Reines *et al.*, “Tuning in to RF MEMS,” *IEEE Microwave Magazine,* vol. 10, no. 6, pp. 55-72, 2009.

[43] G. M. Rebeiz, and J. B. Muldavin, “RF MEMS switches and switch circuits,” *IEEE Microwave Magazine,* vol. 2, no. 4, pp. 59-71, 2001.

[44] G. M. Rebeiz, *RF MEMS: Theory, Design, and Technology*, New York, USA: Wiley, 2003.

[45] D. Bansal, A. Bajpai, K. Mehta *et al.*, “Improved Design of Ohmic RF MEMS Switch for Reduced Fabrication Steps,” *IEEE Transactions on Electron Devices,* vol. 66, no. 10, pp. 4361-4366, 2019.

[46] C.-H. Chu, W.-P. Shih, S.-Y. Chung *et al.*, “A low actuation voltage electrostatic actuator for RF MEMS switch applications,” *Journal of Micromechanics and Microengineering,* vol. 17, no. 8, pp. 1649, 2007.

[47] S. Duffy, C. Bozler, S. Rabe *et al.*, “MEMS microswitches for reconfigurable microwave circuitry,” *IEEE Microwave and Wireless Components Letters,* vol. 11, no. 3, pp. 106-108, 2001.

[48] J. Iannacci, “RF-MEMS technology as an enabler of 5G: Low-loss ohmic switch tested up to 110 GHz,” *Sensors and Actuators A: Physical,* vol. 279, pp. 624-629, 2018.

[49] M. Kim, R. Ge, X. Wu *et al.*, “Zero-static power radio-frequency switches based on MoS2 atomristors,” *Nature Communications,* vol. 9, no. 1, pp. 2524, 2018.

[50] M. Kim, E. Pallecchi, R. Ge *et al.*, “Analogue switches made from boron nitride monolayers for application in 5G and terahertz communication systems,” *Nature Electronics,* vol. 3, no. 8, pp. 479-485, 2020.

[51] Y. Liu, Y. Bey, and X. Liu, “High-Power High-Isolation RF-MEMS Switches With Enhanced Hot-Switching Reliability Using a Shunt Protection Technique,” *IEEE Transactions on Microwave Theory and Techniques,* vol. 65, no. 9, pp. 3188-3199, 2017.

[52] Y. Liu, J. Liu, B. Yu *et al.*, “A Compact Single-Cantilever Multicontact RF-MEMS Switch With Enhanced Reliability,” *IEEE Microwave and Wireless Components Letters,* vol. 28, no. 3, pp. 191-193, 2018.

[53] C. D. Patel, and G. M. Rebeiz, “A Compact RF MEMS Metal-Contact Switch and Switching Networks,” *IEEE Microwave and Wireless Components Letters,* vol. 22, no. 12, pp. 642-644, 2012.

[54] C. D. Patel, and G. M. Rebeiz, “A High-Reliability High-Linearity High-Power RF MEMS Metal-Contact Switch for DC–40-GHz Applications,” *IEEE Transactions on Microwave Theory and Techniques,* vol. 60, no. 10, pp. 3096-3112, 2012.

[55] S. Pi, M. Ghadiri-Sadrabadi, J. C. Bardin *et al.*, “Nanoscale memristive radiofrequency switches,” *Nature Communications,* vol. 6, no. 1, pp. 7519, 2015.

[56] H. Saleh, M. Shojaeian, R. Bajwa *et al.*, “Low actuation voltage cantilever-type RF-MEMS shunt switches for 5G applications,” *Microelectronics Reliability,* vol. 136, pp. 114645, 2022.

[57] R. Stefanini, M. Chatras, P. Blondy *et al.*, “Miniature MEMS Switches for RF Applications,” *Journal of Microelectromechanical Systems,* vol. 20, no. 6, pp. 1324-1335, 2011.

[58] K. Zhu, C. Wen, A. A. Aljarb *et al.*, “The development of integrated circuits based on two-dimensional materials,” *Nature Electronics,* vol. 4, no. 11, pp. 775-785, 2021.

[59] M. Dragoman, M. Aldrigo, and D. Dragoman, "Perspectives on Atomic-Scale Switches for High-Frequency Applications Based on Nanomaterials," *Nanomaterials,* 11, 2021.

[60] S. H. Pu, A. S. Holmes, E. M. Yeatman *et al.*, “Stable zipping RF MEMS varactors,” *Journal of Micromechanics and Microengineering,* vol. 20, no. 3, pp. 035030, 2010.

[61] M. Qing, T. Quan, A. C. Tsung-Kuan *et al.*, "Metal contact reliability of RF MEMS switches." *Proc. SPIE, Reliability, Packaging, Testing, and Characterization of MEMS/MOEMS VI*, 2007, p. 646305.

[62] Y. Liu, Y. Bey, and X. Liu, “Extension of the Hot-Switching Reliability of RF-MEMS Switches Using a Series Contact Protection Technique,” *IEEE Transactions on Microwave Theory and Techniques,* vol. 64, no. 10, pp. 3151-3162, 2016.

[63] "Menlo Micro, MM5130 DC to 26 GHz High Power RF Switch," https://menlomicro.com/products/rf.

[64] "Analog Devices, ADGM1001, 0 Hz/DC to 34 GHz, SPDT MEMS Switches," https://www.analog.com/en/products/adgm1001.html.

[65] A. Basu, R. P. Hennessy, G. G. Adams *et al.*, “Hot switching damage mechanisms in MEMS contacts—evidence and understanding,” *Journal of Micromechanics and Microengineering,* vol. 24, no. 10, pp. 105004, 2014.

[66] Y. H. Song, M. W. Kim, M. H. Seo *et al.*, “A Complementary Dual-Contact MEMS Switch Using a “Zipping” Technique,” *Journal of Microelectromechanical Systems,* vol. 23, no. 3, pp. 710-718, 2014.

[67] O. Wunnicke, H. Kwinten, L. v. Leuken-Peters *et al.*, "Small, low-ohmic RF MEMS switches with thin-film package." *IEEE 24th International Conference on Micro Electro Mechanical Systems*, Cancun, Mexico, 2011, pp. 793-796.

[68] F. Ke, J. Miao, and J. Oberhammer, “A Ruthenium-Based Multimetal-Contact RF MEMS Switch With a Corrugated Diaphragm,” *Journal of Microelectromechanical Systems,* vol. 17, no. 6, pp. 1447-1459, 2008.

[69] D. Peroulis, S. P. Pacheco, and L. P. B. Katehi, “RF MEMS switches with enhanced power-handling capabilities,” *IEEE Transactions on Microwave Theory and Techniques,* vol. 52, no. 1, pp. 59-68, 2004.

[70] S. Gong, H. Shen, and N. S. Barker, “Study of Broadband Cryogenic DC-Contact RF MEMS Switches,” *IEEE Transactions on Microwave Theory and Techniques,* vol. 57, no. 12, pp. 3442-3449, 2009.

[71] K. Sylves, K. Maute, and M. L. Dunn, “Adhesive surface design using topology optimization,” *Structural and Multidisciplinary Optimization,* vol. 38, no. 5, pp. 455-468, 2009.

[72] H. Saleh, R. Bajwa, I. Tekin *et al.*, “Wavy Cantilever RF-MEMS Switch based on Bidirectional Control of Intrinsic Stress,” *2020 21st International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (Eurosime),* 2020.

[73] R. Bajwa, and M. K. Yapici, “Integrated On-Chip Transformers: Recent Progress in the Design, Layout, Modeling and Fabrication,” *Sensors,* vol. 19, no. 16, 2019.

[74] W. C. Tian, P. Li, and L. X. Yuan, “Research and Analysis of MEMS Switches in Different Frequency Bands,” *Micromachines,* vol. 9, no. 4, 2018.

[75] D. Peroulis, S. P. Pacheco, K. Sarabandi *et al.*, “Electromechanical considerations in developing low-voltage RF MEMS switches,” *IEEE Transactions on Microwave Theory and Techniques,* vol. 51, no. 1, pp. 259-270, 2003.

[76] Z. A. Yang, R. Q. Zhang, and D. Peroulis, "Design and Optimization of Bidirectional Tunable MEMS All-Silicon Evanescent-Mode Cavity Filter," *IEEE Transactions on Microwave Theory and Techniques,* vol. 68, no. 6, pp. 2398-2408, 2020.

[77] F. Domingue, S. Fouladi, A. B. Kouki *et al.*, "Design Methodology and Optimization of Distributed MEMS Matching Networks for Low-Microwave-Frequency Applications," *IEEE Transactions on Microwave Theory and Techniques,* vol. 57, no. 12, pp. 3030-3041, 2009.

[78] A. Stehle, G. Georgiev, V. Ziegler *et al.*, "RF-MEMS Switch and Phase Shifter Optimized for W-Band," *2008 European Microwave Conference, Vols 1-3,* pp. 870-+, 2008.

[79] R. Gonzalez-Echevarria, E. Roca, R. Castro-Lopez *et al.*, "An Automated Design Methodology of RF Circuits by Using Pareto-Optimal Fronts of EM-Simulated Inductors," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 36, no. 1, pp. 15-26, 2017.

[80] R. Gonzalez-Echevarria, R. Castro-Lopez, E. Roca *et al.*, "Automated Generation of the Optimal Performance Trade-Offs of Integrated Inductors," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 33, no. 8, pp. 1269-1273, 2014.

[81] S. Koziel, and P. Kurgan, "Expedited EM-driven generation of Pareto-optimal trade-off curves for variable-turn on-chip inductors," *IET Microwaves Antennas & Propagation,* vol. 12, no. 7, pp. 1205-1210, 2018.

[82] J. E. Rayas-Sánchez, S. Koziel, and J. W. Bandler, "Advanced RF and Microwave Design Optimization: A Journey and a Vision of Future Trends," *IEEE Journal of Microwaves,* vol. 1, no. 1, pp. 481-493, 2021.

[83] M. Pak, F. V. Fernandez, and G. Dundar, "Yield-aware multi-objective optimization of a MEMS accelerometer system using QMC-based methodologies," *Microelectronics Journal,* vol. 103, 2020.

[84] P. Di Barba, and S. Wiak, "Evolutionary Computing and Optimal Design of MEMS," *IEEE-ASME Transactions on Mechatronics,* vol. 20, no. 4, pp. 1660-1667, 2015.

[85] J. Iannacci, G. Tagliapietra, and A. Bucciarelli, "Exploitation of response surface method for the optimization of RF-MEMS reconfigurable devices in view of

future beyond-5G, 6G and super-IoT applications," *Scientific Reports,* vol. 12, no. 1, 2022.

[86] S. Younis, M. M. Saleem, M. Zubair *et al.*, "Multiphysics design optimization of RF-MEMS switch using response surface methodology," *Microelectronics Journal,* vol. 71, pp. 47-60, 2018.

[87] M. A. Philippine, O. Sigmund, G. M. Rebeiz *et al.*, "Topology Optimization of Stressed Capacitive RF MEMS Switches," *Journal of Microelectromechanical Systems,* vol. 22, no. 1, pp. 206-215, 2013.

[88] M. M. Shalaby, Z. D. Wang, L. L. W. Chow *et al.*, "Robust Design of RF-MEMS Cantilever Switches Using Contact Physics Modeling," *IEEE Transactions on Industrial Electronics,* vol. 56, no. 4, pp. 1012-1021, 2009.

[89] K. Deb, A. Pratap, S. Agarwal *et al.*, "A fast and elitist multiobjective genetic algorithm: NSGA-II," *IEEE Transactions on Evolutionary Computation,* vol. 6, no. 2, pp. 182-197, 2002.

[90] X. Liu, C. E. Athanasiou, N. P. Padture *et al.*, "A machine learning approach to fracture mechanics problems," *Acta Materialia,* vol. 190, pp. 105-112, 2020.

[91] Q. Feng, W. Maier, T. Stehle *et al.*, "Optimization of a clamping concept based on machine learning," *Production Engineering-Research and Development,* vol. 16, no. 1, pp. 9-22, 2022.

[92] S. B. Kotsiantis, "Decision trees: a recent overview," *Artificial Intelligence Review,* vol. 39, no. 4, pp. 261-283, 2013.

[93] J. B. Yoon, Y. S. Choi, B. I. Kim *et al.*, "CMOS-compatible surface-micromachined suspended-spiral inductors for multi-GHz silicon RF ICs," *IEEE Electron Device Letters,* vol. 23, no. 10, pp. 591-593, 2002.

[94] S. S. Mohan, M. D. Hershenson, S. P. Boyd *et al.*, "Simple accurate expressions for planar spiral inductances," *IEEE Journal of Solid-State Circuits,* vol. 34, no. 10, pp. 1419-1424, 1999.

[95] T. T. Cao, T. J. Hu, and Y. L. Zhao, "Research Status and Development Trend of MEMS Switches: A Review," *Micromachines,* vol. 11, no. 7, 2020.

[96] W. Zhang, H. Zhang, F. Du *et al.*, "Pull-In Analysis of the Flat Circular CMUT Cell Featuring Sealed Cavity," *Mathematical Problems in Engineering,* vol. 2015, 2015.