DIGITAL SELF-INTERFERENCE CANCELLATION IN IN-BAND FULL DUPLEX RADIOS: FPGA IMPLEMENTATION AND EXTENSION TO MULTIPLE INPUT MULTIPLE OUTPUT SYSTEMS

by
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ABSTRACT

DIGITAL SELF-INTERFERENCE CANCELLATION IN IN-BAND FULL DUPLEX RADIOS: FPGA IMPLEMENTATION AND EXTENSION TO MULTIPLE INPUT MULTIPLE OUTPUT SYSTEMS

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Keywords: full duplex communication, nonlinear digital cancellation, self-interference, memory polynomial,FPGA,OFDM

With the use of in-band full-duplex (IBFD) radios, spectral efficiency is potentially doubled by allowing communicating transceivers to work at the same time and in the same frequency band. The main problem with implementing IBFD systems is the self-interference of the devices due to their transmission at the same time together. For IBFD radios to operate, self-interference must be suppressed with various techniques such as antenna suppression, analogue cancellation or linear cancellation algorithms. In this thesis, different digital self-interference cancellation (DSIC) techniques are implemented. First, the linear self-interference cancellation algorithm is projected into digital circuitry and embedded into the receiver chain of a software-defined radio(SDR) which includes a Virtex 6 field programmable gate array(FPGA) chip. Self-interference cancellation algorithm is tested in real-time using slot-coupled patch antennas along with the SDR board. The performance of the real-time operation is measured by using the simplest medium access control mechanism which implements no control over medium access. Data frames are sent to the medium when the local traffic generator of the SDR board starts. Secondly, the nonlinear DSIC algorithm is implemented for MIMO radio. The non-linear effects of multiple transmitters are estimated by switched radio configuration. In the first mode of the switch, a loop-back cable is connected between each node's transmitter and receiver. For estimation of the hardware effects, the Memory Polynomial model is used. After training and estimation of the non-linear hardware effects in the first mode, the second mode is activated. In the second mode, non-linearities are applied

to the baseband signal which is to be transmitted. Then, the reconstructed signal is fed to the linear cancellation algorithm as a reference signal. The performance of the switched MIMO setup is measured and compared with conventional DSIC algorithms.

ÖZET

BANT İÇİ TAM ÇİFT YÖNLÜ RADYOLARDA SAYISAL ÖZGİRİŞİM GİDERİMİ:FPGA GERÇEKLEMESİ VE ÇOK GİRİŞLİ ÇOK ÇIKIŞLI SİSTEMLERE UYARLAMASI

DORUK CAN ALTINTAŞ

ELEKTRONİK MÜHENDİSLİĞİ YÜKSEK LİSANS TEZİ, 2023

Tez Danışmanı: Prof. Dr. ÖZGÜR GÜRBÜZ

Anahtar Kelimeler: Tam çift yönlü haberleşme,Doğrusal olmayan giderim,Sayısal özgirişim giderimi, FPGA, OFDM

Bant içi tam çift yönlü (IBFD) radyoların kullanımıyla, iletişim kuran alıcı-vericilerin aynı anda ve aynı frekans bandında çalışmasına izin verilerek spektral verimlilik potansiyel olarak iki katına çıkarılabilmektedir. IBFD sistemlerinin uygulanmasındaki temel sorun, cihazların aynı anda birlikte iletim yapmasından dolayı özgirişim etkilerinin yüksek olmasıdır. IBFD raydolarının çalışabilmesi için anten bastırma, analog giderim veya doğrusal giderim algoritmaları gibi çeşitli tekniklerle özgirişimin bastırılması gerekmektedir. Bu tezde, farklı dijital özgirişim giderim teknikleri uygulanmaktadır. İlk olarak, doğrusal özgirişim giderim algoritması dijital devreye yansıtılmmış ve bir Virtex 6 alanda programlanabilir kapı dizisi (FPGA) çipi içeren yazılım tanımlı radyonun (SDR) alıcı zincirine gömülür. Özgirişim giderme algoritması, SDR kartıyla birlikte yuvaya etkileşimli yama antenleri kullanılarak gerçek zamanlı olarak test edilmiştir. Gerçek zamanlı işlemin performansı, ortam erişimi üzerinde kontrol uygulamayan en basit ortam erişim kontrol mekanizması kullanılarak ölçülmüştür. Veri çerçeveleri, SDR kartının yerel trafik oluşturucusu başladığında ortama gönderilir.Tezin ikinci kısmında, MIMO radyo için doğrusal olmayan DSIC algoritması uygulanmıştır. Birden fazla vericinin doğrusal olmayan etkileri, anahtarlamalı radyo konfigürasyonu ile kestirilir. Anahtarın birinci modunda, her düğümün vericisi ve alıcısı arasına bir geri döngü kablosu bağlanır. Donanım etkilerinin kestirimi için Bellek Polinom modeli kullanılmaktadır. Birinci modda doğrusal olmayan donanım etkilerinin eğitimi ve kestiriminden sonra, ikinci mod etkinleştirilir. İkinci modda, iletilecek olan tabanbant sinyaline doğrusal ol-

mayan etkiler uygulanır. Ardından, yeniden oluşturulan sinyal, doğrusal giderim algoritmasına bir referans sinyali olarak verilir. Anahtarlamalı MIMO kurulumunun performansı ölçülüp ve yaygın DSIC algoritmalarıyla karşılaştırılmıştır.

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To all my teachers..

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List of Abbreviations

DSIC digital self-interference cancellation. 4, 7

FD full duplex. xii, 19, 20

IEEE The Institute of Electrical and Electronic Engineers. 19

LS least squares. 4

LTS Long Training Sequence. 6

MP memory polynomial. 4

SDR software defined radio. 19, 21

SI self-interference. xii, 5–7, 9

WARP Wireless Open Access Research Platform. 19, 21

Chapter 1

INTRODUCTION

Full duplex (FD) communication, which allows simultaneous transmission and reception of data over the same channel, is becoming increasingly important for meeting the growing demand for high-speed wireless communication. By doubling the capacity of existing networks and reducing latency, FD communication offers significant advantages over half-duplex communication [1], [2], [3].

However, a major challenge in FD communication is self-interference, which occurs when the transmitted signal leaks into the receiver, resulting in significant signal degradation and reduced system performance. Self-interference cancellation (SIC) techniques have emerged to mitigate this challenge and enhance the performance of FD systems. The principles of SIC are based on the idea of cancelling the self-interference signal using an estimate of the transmitted signal, which is obtained through a variety of analog or digital signal processing techniques. Analog cancellation methods involve using analog components to cancel out the self-interference signal, while digital cancellation methods use signal processing algorithms to subtract the self-interference signal from the received signal. Hybrid cancellation techniques combine both analog and digital methods to achieve the best performance [4], [5], [6], [7].

Broadband wireless systems commonly use orthogonal frequency division multiplexing (OFDM) due to its high data rates and resiliency to multipath, making it a popular choice for 4G cellular networks, WLANs, and WiMAX [8], [9], [10], [11]. Consequently, self-interference cancellation (DSIC) techniques for full-duplex (FD) communication are primarily designed for OFDM-based physical layers. In [12], [13] various DSIC techniques have been evaluated, including minimum mean square error and least squares approaches in time-domain estimation or frequency-domain estimation of the self-interference channel, followed by time-domain reconstruction

of the self-interference signal. The authors have also integrated time-domain DSIC with different monostatic antennas on their software-defined radio (SDR) based test-bed to obtain performance limits and characterization of the proposed FD radio architecture.

There has been significant research in the field of DSIC in recent years, and a number of techniques have been proposed and evaluated for various applications. These include wireless networks, cognitive radio, vehicular networks, and satellite communication, among others. The choice of self-interference cancellation (SIC) technique depends on the specific requirements of the application, such as the desired level of cancellation, system complexity, power consumption, and implementation cost. Self-interference cancellation is a critical component of FD communication systems that can significantly improve network performance and capacity. The choice of self-interference cancellation technique depends on the specific requirements of the application, and there is ongoing research in the development of new and improved techniques. The work presented in this thesis contributes to the understanding of the principles and limitations of DSIC in FD communication and its potential applications in various domains. The contributions of this thesis can be listed as follows:

- Linear DSIC is implemented in real-time and integrated by digital circuit blocks for transmitter and receiver chains on the field programmable gate array (FPGA) system on the wireless open-access research platform (WARP) SDR board [14]. The circuitry is modified to match the frame structure 802.11g IEEE standard.

- Both simulation and measurement results are given, and the results show that the real-time performance is similar to that of MATLAB simulations. The measurement and simulation shows total suppression of 85 dB, enabling (FD) communication.

- Following adaptation of linear DSIC to MIMO systems, the non-linearity problem in FD MIMO radios is considered by applying the switched FD radio solution [14] with memory polynomial algorithm. The switched radio architecture is extended to a 2X2 MIMO system where both streams are trained for their non-linearity effects that is caused by their transmitter and receiver chains during the training phase. In the cancellation phase, the non-linear SI signal is fed to the linear cancellation algorithm. Measurements are performed on the WARP SDR board set-up.

- Performance of the proposed FD MIMO solution is evaluated via extensive

tests on the WARP SDR set-up. It is shown that linear only DSIC is improved by 5-6 dB, and integrated residual linear and non-linear cancellation technique [15] is improved by 2-3 dB.

- The training overhead of the suggested non-linear algorithm is calculated. The results demonstrate that our solution imposes minimal training cost when compared to the existing integrated DSIC methods. The training overhead can be considered as negligible due to single training sequence just at the beginning of the operation, resulting increased data rate, unlike existing integrated linear and non-linear DSIC methods. The calculations and the comparison between different techniques are presented.

The rest of the thesis is organized as follows. In Chapter 2, background on linear and non-linear DSIC techniques is provided. In Chapter 3, FPGA implementation of linear DSIC and its integration with digital transceiver blocks is presented, together with performance results. In Chapter 4, MIMO extension of DSIC, in particular, application of switched FD solution for non-linear DSIC is explained, along with overhead and throughput analysis as well as detailed performance tests on the WARD SDR set-up. In Chapter 5, our conclusions are provided.

Chapter 2

BACKGROUND

In this chapter, first, well-known and widely applied DSIC techniques are explained with equations. These techniques are least squares (LS) based linear DSIC, the MP model algorithm as nonlinear DSIC. Then, nonlinear DSIC solutions in the literature are reviewed.

2.1 Baseband System Model and Linear Digital Cancellation

In this section, the OFDM system model and linear DSIC algorithm are explained. Figure 2.1 summarizes the system model of the FD radio which is implementing linear digital SI cancellation.

As shown in the figure 2.1, the transmitter chain is the same as the one in a typical OFDM half duplex radio. To have a reference signal for reconstruction of the received signal, generated baseband OFDM signal is fed to the receiver chain. This reference signal is taken before IFFT operation in the transmitter chain.

Received baseband signal vector $\underline{y}$ can be expressed as

$$\underline{y} = \underline{x} * \underline{h} + \underline{w}, \tag{2.1}$$

where $*$ denotes the convolution operation, $\underline{h}$ denotes the channel impulse response which includes the discrepancies of the environment, and $\underline{w}$ expresses additive white Gaussian noise per sample. The channel $\underline{h}$ accommodates the non-linear effects of the radio transceiver hardware in addition to the SI channel. $\underline{x}'$ is the interpolated version of $\underline{x}$ and $\underline{y}$ decimated to acquire $\underline{y}'$. The relationship between the channel

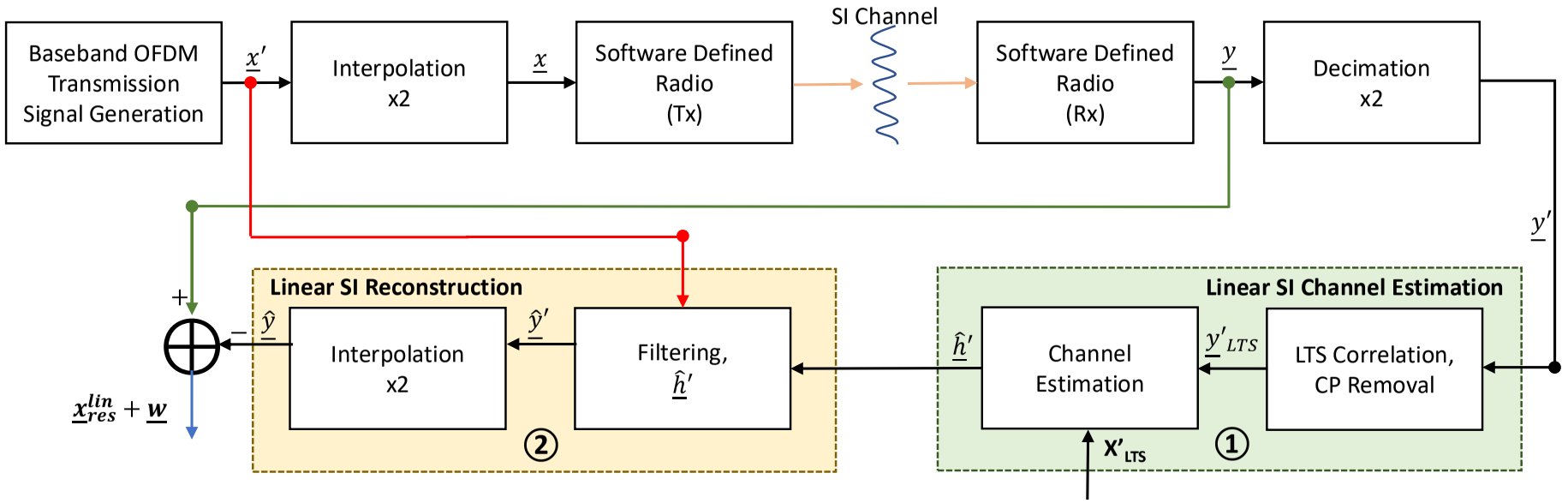

Figure 2.1 Block diagram of the baseband system model and linear digital SI cancellation[13]

in (2.1), the received signal and the broadcast samples can be stated as below.

$$\underline{y}' = \underline{x}' * \underline{h}' + \underline{w}. \tag{2.2}$$

In packet start detection and channel estimation operations, Long Training Sequence(LTS) symbols are used. LTS symbols are inserted in the preamble section of the OFDM frame structure. Four repetitions of LTS symbols are inserted. On the receiver side, packet start is detected using LTS symbols and then they are averaged. For the preamble section, convolution operation in the time domain can be expressed as

$$\underline{y}'_{LTS} = \mathbf{X}'_{\mathbf{LTS}}\underline{h}' + \underline{w}, \tag{2.3}$$

$$\mathbf{X}'_{\mathbf{LTS}} = \begin{bmatrix} l'^{1}_{LTS} & l'^{K}_{LTS} & l'^{K-1}_{LTS} & \cdots & l'^{K-K_{CP}+2}_{LTS} \\ l'^{2}_{LTS} & l'^{1}_{LTS} & l'^{K}_{LTS} & \cdots & l'^{K-K_{CP}+3}_{LTS} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ l'^{K}_{LTS} & l'^{K-1}_{LTS} & l'^{K-2}_{LTS} & \cdots & l'^{K-K_{CP}+1}_{LTS} \end{bmatrix}, \tag{2.4}$$

where $\underline{h}'$ is the channel impulse response vector and $\mathbf{X}'_{\mathbf{LTS}}$ denotes the Toeplitz matrix formed by inserting circularly shifted known transmitted LTS samples denoted by $\underline{l}'_{LTS}$ [16].

The channel impulse response estimation is done by the following expression [16]:

$$\hat{\underline{h}}' = {\mathbf{X}'_{\mathbf{LTS}}}^{\dagger}\underline{y}'_{LTS}, \tag{2.5}$$

where ${\mathbf{X}'_{\mathbf{LTS}}}^{\dagger}$ denotes the pseudo inverse of $\mathbf{X}'_{\mathbf{LTS}}$. The reconstructed SI samples $\hat{\underline{y}}'$ can be calculated as [3, 17–19]

$$\hat{\underline{y}}' = \underline{x}' * \hat{\underline{h}}', \tag{2.6}$$

To be transmitted samples $\underline{x}'$ are obtained before the interpolation filter stage of the transmitter chain. After the convolution, the output $\hat{\underline{y}}'$ is interpolated to get the final reconstructed signal $\hat{\underline{y}}$. After the subtraction of the reconstructed signal from the received signal, the system yields

$$\underline{y} - \hat{\underline{y}} = \underline{r} = \underline{w} + \underline{x}^{\text{lin}}_{\text{res}}, \tag{2.7}$$

where $\underline{r}$ expresses the residual SI signal. $\underline{x}_{\text{res}}^{\text{lin}}$ and $\underline{w}$ determine the noise floor level.

The tests have been conducted for linear only DSIC along with the other techniques to provide a comparison between different approaches. At high power levels, it can be seen that the performance of the linear-only cancellation approach is decreasing significantly. After a certain transmission power level, non-linear DSIC methods are needed to be performed to achieve FD operation.

2.1.1 Frequency Domain Channel Estimation

The frequency domain channel estimation technique for self-interference cancellation works by estimating the self-interference channel in the frequency domain using a known reference signal. The reference signal can be a known training sequence or a tone, and it is transmitted by the transmitter and received by the receiver without any interference. The receiver then uses the received reference signal to estimate the self-interference channel in the frequency domain.

Let the received reference signal be denoted as $y[n]$, and the transmitted reference signal be denoted as $x[n]$. The received reference signal can be expressed as:

$$y[n] = h[n] * x[n] + w[n] \tag{2.8}$$

where $h[n]$ is the self-interference channel impulse response, $*$ denotes convolution, and $w[n]$ is the noise in the received signal.

In the frequency domain, the received reference signal can be expressed as:

$$Y[k] = H[k]X[k] + W[k] \tag{2.9}$$

where $Y[k]$, $H[k]$, $X[k]$, and $W[k]$ are the Discrete Fourier Transforms (DFTs) of $y[n]$, $h[n]$, $x[n]$, and $w[n]$, respectively.

The self-interference channel frequency response can be estimated as:

$$H_{est}[k] = Y[k]/X[k] \tag{2.10}$$

where $H_est[k]$ is the estimated frequency response of the self-interference channel.

Finally, the estimated self-interference channel impulse response can be obtained by taking the Inverse Discrete Fourier Transform (IDFT) of $H_{est}[k]$:

$$h_{est}[n] = IDFT(H_{est}[k]) \tag{2.11}$$

where $h_est[n]$ is the estimated impulse response of the self-interference channel.

Once the self-interference channel is estimated, the receiver can reconstruct the self-interference signal in the frequency domain by multiplying the received signal by the estimated self-interference channel. This effectively removes the self-interference signal from the received signal, leaving only the desired signal.

The reconstructed signal can then be converted back to the time domain using an inverse Fourier transform. The resulting time-domain signal is the received signal with the self-interference cancelled.

2.2 Memory Polynomial Model for Nonlinear DSIC

In an FD communication system, self-interference must be estimated and cancelled from the received signal. Since there are non-linear disturbances in the self-interference signal, the estimation process becomes more complex. To estimate the non-linearity effects of the hardware, the memory polynomial model is used extensively in literature [20, 21]. The memory polynomial model can be formulated as [22]

$$y[n] = \sum_{k=1}^{D} \sum_{p=0}^{M} a_{kp} x[n-p] \left|x[n-p]\right|^{k-1}. \tag{2.12}$$

where $y[n]$ and $x[n]$ represent time domain with complex values as input and output discrete time signals of the memory polynomial model, k denotes the degree of the polynomial, p is the memory length. The memory length is the number of previous samples that are considered for calculation. a_{kp}'s are the weights for the model.

To apply this model to OFDM FD systems, only odd degrees are considered because even non-linear components fall out of the signal band.

Afterwards, a non-linear estimation technique is utilized to analyze a specific portion of $\underline{y}$ during the training process. The training phase involves estimating the coefficients, denoted as a_{kp}. These coefficients are subsequently employed to assess all the data samples of $\underline{y}$ received during the testing phase.

To be able to use the model in SI cancellation, coefficients a_{kp} shall be extracted

from the inputs. First, a matrix of $\mathbf{X}^{\mathrm{MP}}$ is formed based on the terms in (2.12) as shown below. Please note that L represents the number of observations. It is important to mention that $L+M$ should not exceed the length of $\underline{x}$ and the size of $\mathbf{X}^{\mathrm{MP}}$ is denoted as $L \times ((2D-1)+M)$.

Let $\forall\,\{i,\,l\} : \alpha_i^l = \; x_i|x_i|^{l-1} \quad \cdots \quad x_{i+M-1}|x_{i+M-1}|^{l-1}$, then the observation matrix $\mathbf{X}^{\mathrm{MP}}$ can be structured as

$$\mathbf{X}^{\mathrm{MP}} = \begin{bmatrix} \alpha_1^1 & \alpha_1^3 & \cdots & \alpha_1^d \\ \alpha_2^1 & \alpha_2^3 & \cdots & \alpha_2^d \\ \vdots & \vdots & \ddots & \vdots \\ \alpha_L^1 & \alpha_L^3 & \cdots & \alpha_L^d \end{bmatrix}, \tag{2.13}$$

Then, the coefficients can be estimated as (2.14).

$$\underline{a} = \left((\mathbf{X}^{\mathrm{MP}})^{\mathrm{T}}\mathbf{X}^{\mathrm{MP}} + \lambda\mathbf{I}\right)^{-1}(\mathbf{X}_{\mathrm{tr}}^{\mathrm{MP}})^{\mathrm{T}}\underline{y}. \tag{2.14}$$

For the estimation of the coefficients, one full OFDM data frame is used since this operation only takes place at the power-up of the device. After estimation, calculated coefficients are stored and used for the subsequent transmissions.

In the second phase, the coefficients a_{kp} are applied to the baseband signal to reconstruct the received signal as

$$\underline{\hat{y}} = \mathbf{X}^{\mathrm{MP}}\underline{a}. \tag{2.15}$$

Finally, the reconstructed signal $\underline{\hat{y}}$ is subtracted from the received signal $\underline{y}$ to obtain the residual SI signal as in (2.7).

2.3 Switched FD Radio Architecture

With switched radio setup [14], both linear and non-linear effects of the system can be examined and processed one by one. Non-linear interference caused by the hardware components, especially PA, is retrieved and estimated. Then estimated Non-linearity can be fed to the linear SI cancellation algorithm as a reference so that both linear and non-linear effects are considered.

Switched FD architecture operates in two modes. In estimation mode, the output port of the transmitter is connected to the receiver with a coaxial cable to create

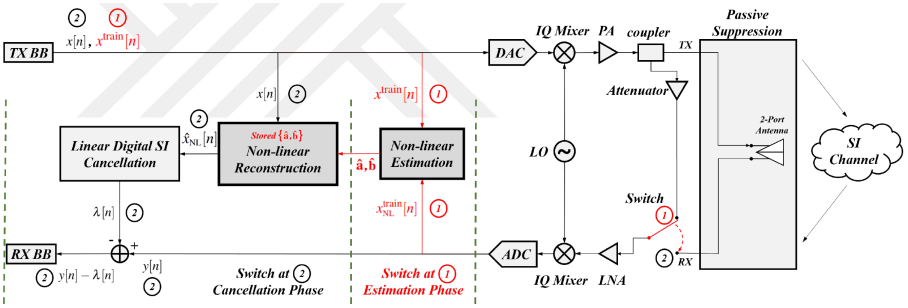

Figure 2.2 Switched FD architecture [14]

a loop-back. After analog to digital conversion of the received signal, it is fed to the estimation block. Baseband transmit signal is also provided to the estimation block so that based on the transmitted signal, coefficients for the non-linear effects of the board can be estimated and stored. Stored coefficients can be used consecutively for later transmissions. After the training session, architecture switches into reconstruction mode. In this mode, transmitter and receiver ports are connected with antennas. Stored coefficients are used to reconstruct a reference signal to be used linear cancellation algorithm [3]. Using the LTS field on the received signal and estimated nonlinear baseband signal, SI channel approximation is done. After channel approximation is made, it is applied to the reference baseband signal to reconstruct the received signal. The resulting reconstructed signal is subtracted from the received signal so that SI cancellation is performed.

Chapter 3

REAL-TIME IMPLEMENTATION OF LINEAR DIGITAL SELF-INTERFERENCE CANCELLATION

In this chapter, the software-defined radio(SDR) environment is briefly introduced. Integration of the linear cancellation algorithm and real-time OFDM system that is based on IEE 802.11g is explained and performance analysis of the system is presented.

3.1 WARP Environment

The WARP is a hardware and software framework designed to enable experimentation and prototyping of advanced wireless communication systems. It is developed by Rice University and is open-source, allowing for collaboration and contributions from the research community.

WARP provides a modular hardware platform that can be configured to support a wide range of wireless communication protocols, from simple point-to-point links to complex multi-user MIMO systems. The hardware platform consists of a baseband processor board and a radio frequency (RF) front-end board, which can be easily swapped out to accommodate different wireless standards and frequency bands.

The baseband processor board is built around a field-programmable gate array

(FPGA), which provides the computational power needed for real-time signal processing and control. The FPGA can be programmed using the open-source MATLAB-based WARP software framework, which includes a comprehensive set of signal-processing tools and communication protocols.

The RF front-end board includes one or more transceivers, which can be configured for different frequency bands and modulation schemes. The front-end board can also be customized to include additional hardware, such as power amplifiers and filters, to support specific applications.

The WARP software framework provides a high-level programming interface that allows researchers to quickly prototype and test new wireless communication algorithms and protocols. The framework includes support for popular communication standards, such as Wi-Fi and LTE, as well as custom protocols.

3.2 FPGA Implementation of Linear DSIC

In the implementation provided by MANGO, the signal received from the RF interface on the WARP v3 card is directly sent to the memory. Since AGC was not used in the MATLAB implementation of the algorithm, the digital interference cancellation algorithm was implemented directly between the ADC in the RF layer and the acquisition memory, in addition to MANGO's implementation. Therefore, the AGC inputs are left blank. The remaining signals obtained at the output (res_i_out, res_q_out) are written to the acquisition memory (Rx Buffer) to be given to the acquisition chain. The intermediate steps were implemented in the Xilinx System Generator tool in a manner compatible with the LS-FDE and TD-R algorithms in Figure 1.3. Detailed information on the input and output signals of the high-level implementation is given in Table 1.1.

The Chipscope module used in the implementation enables real-time observation of intermediate signals. After the design is synthesized and placed in the FPGA, the connected signals to the Chipscope module can be controlled for extraction (debug) purposes. At the same time, these signals can be recorded and transferred to the MATLAB workspace. After the received signals are selected via adc_i_in and adc_q_in the adc_agc_sel block, they are processed in order through the LTS correlation (lts_correlator), carrier frequency offset correction (cfo_correction), and channel estimation (channel_estimator) blocks. After the channel estimation is obtained, the transmission signals tx_i_in and tx_q_in coming from the transmission chain are taken to the time domain restructure (td_r) block and applied to the estimated channel transmission signal. The restructured transmission signal

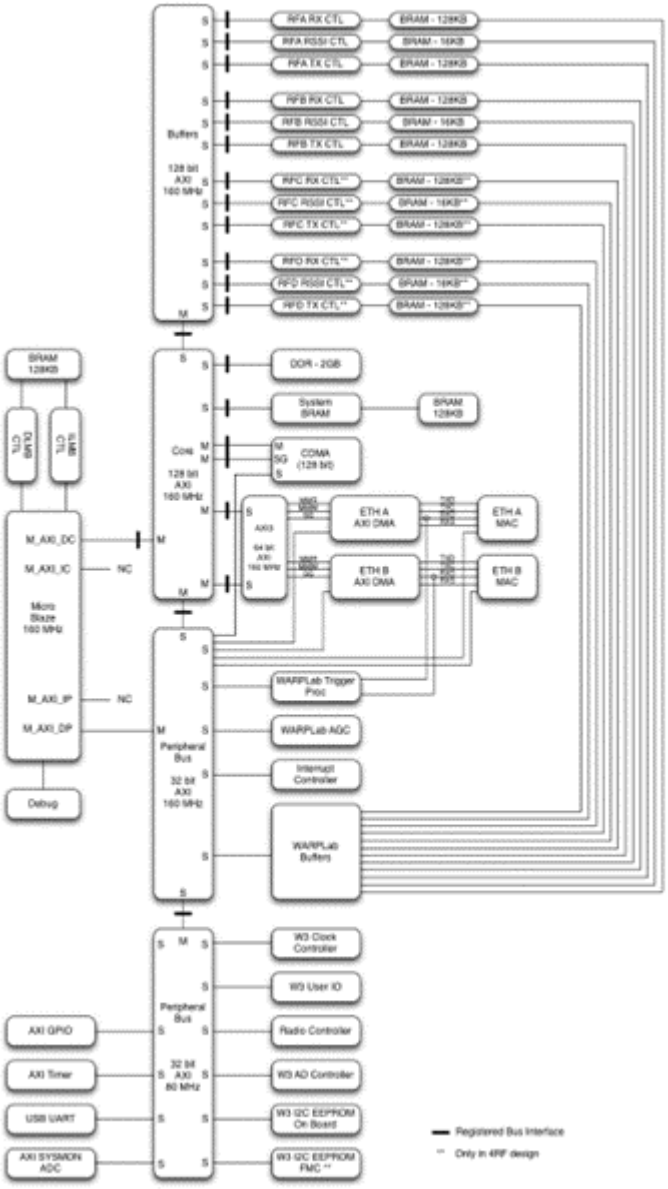

Figure 3.1 FPGA Architecture of WARP Board

according to the channel represents the self-interference signal. When the restructured signal representing the self-interference is subtracted from the received signal, the self-interference is eliminated. For this purpose, the received signal is written to the acquisition memory in the cancellation block from the first trigger (trigger_in). When the restructured signal is ready, the subtraction operation is performed by aligning and scaling the received signal. Thus, self-interference is suppressed and the remaining res_i_out and res_q_out signals are sent to the acquisition memory (Rx Buffer). The details of the blocks are given in the following sections.

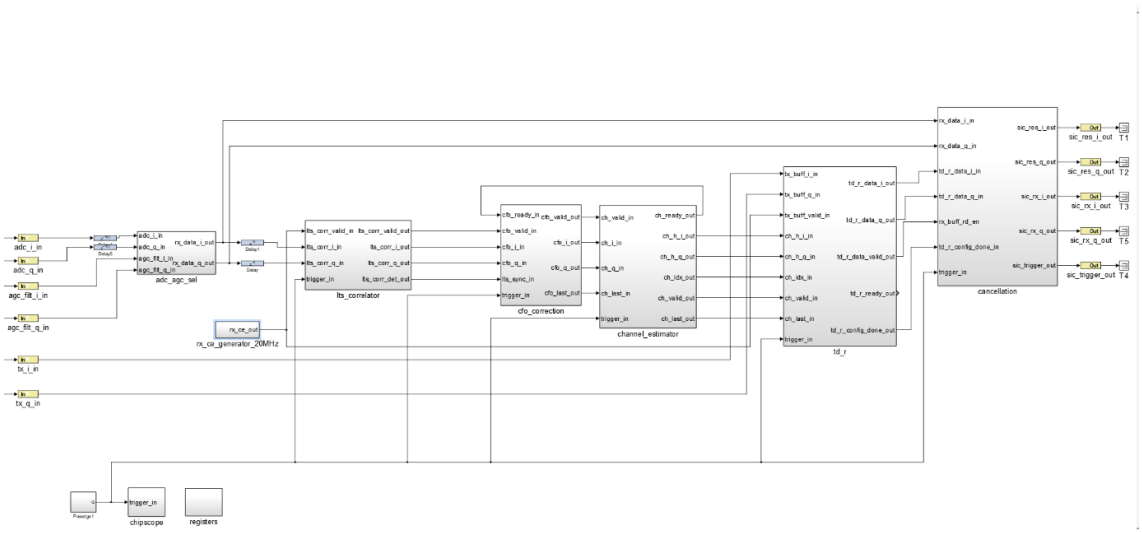

Figure 3.2 Top view of SI cancellation module

Table 3.1 Input and output signals for the SI Cancellation block

Name	In/Out	HDL Type	type	Function
axi_arestn	Input	std_logic	reset	Asynchronous reset signal
clk	Input	std_logic	Clock	160 Mhz clock signal
tx_i_in	Input	std_logic_vector	Data	Real signal generated from Tx chain
tx_q_in	Input	std_logic_vector	Data	Imaginary signal generated from Tx chain
adc_i_in	Input	std_logic_vector	Data	Real signal from ADC block
adc_q_in	Input	std_logic_vector	Data	Imaginary signal from ADC block
trigger	Input	std_logic	Data	Triggers the SI block, Taken from TX chain
res_i_out	Output	std_logic_vector	Data	Real residual signal after cancellation
res_q_out	Output	std_logic_vector	Data	Imaginary residual signal after cancellation

3.2.1 LTS Correlator Block

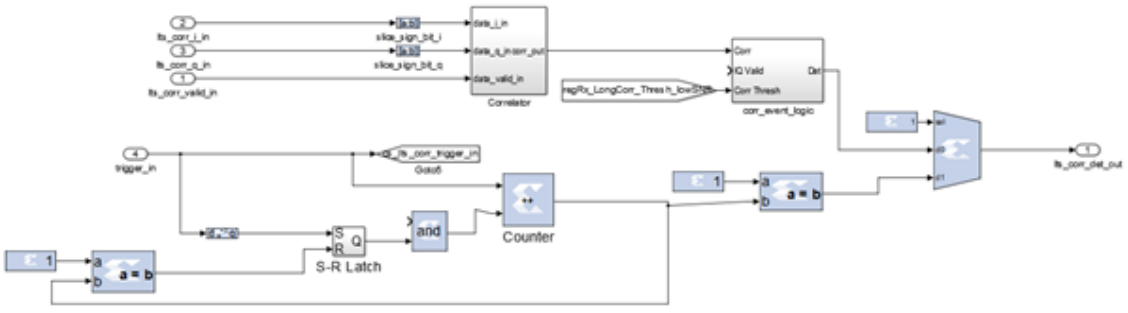

Figure 3.3 Correlator Block

This block works to find two and a half LTS symbols placed in the preamble during transmission in the received signal. The correlator sub-block in the LTS correlator block shown in Figure 1.4 produces the correlated corr_out signal by correlating the LTS symbols. The Corr_event_logic block looks for the two and a half LTS symbols and when the last data for the two and a half LTS symbols comes, the

block produces the detection signal lts_corr_det_out after the last peak. Thus, the beginning of the frame is detected. The simulation graph of this block can be seen in Figure 1.5.

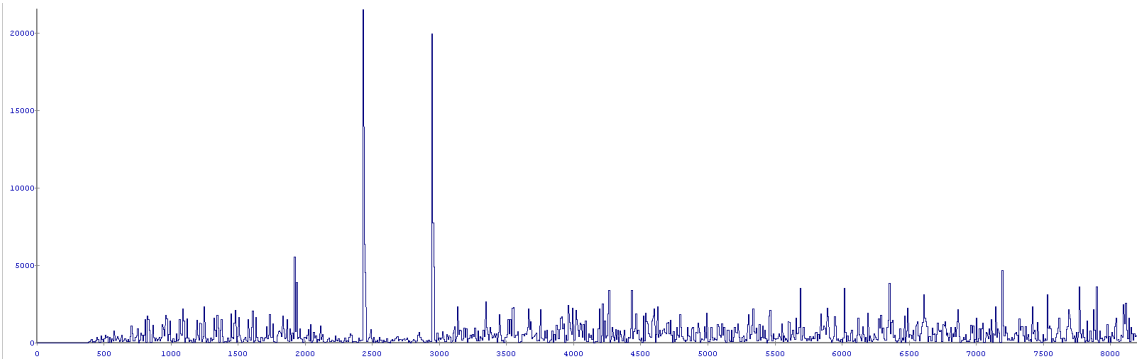

Figure 3.4 Chipscope output of LTS correlation block

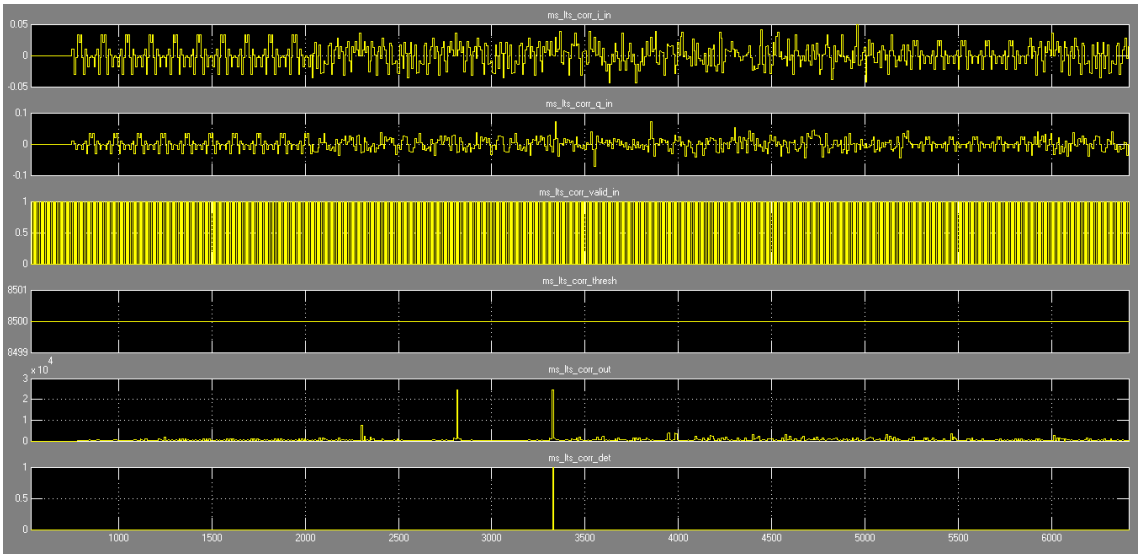

Figure 3.5 Simulation result of the correlation block

3.2.2 Carrier Frequency Correction Block

In the previous section, the LTS correlator block, while performing its task of detecting the packet start, also records the received signals into the Samp Buffer memory inside the cfo_correction block, as shown in Figure 1.6. The memory setting is set for a depth large enough to hold the two and a half LTS symbols of the packet. After the packet start is determined by the LTS correlator block using the lts_sync_in signal, the addressing of the Samp Buffer memory is set to read two LTS symbols from the end and then it is addressed forward one by one to read two LTS symbols. These symbols are then corrected for carrier frequency offset (CFO) and

written to the FIFO memory output. Thus, the LTS symbols are ready for channel estimation. As shown in Figure 1.7, as the channel estimation block becomes ready (cfo_ready_in), each LTS symbol of 64 samples in length is transferred to the channel estimation block. After each LTS symbol, the cfo_last_out signal is generated.

3.2.3 Channel Estimation Block

The channel estimation block uses LTS symbols to estimate channel coefficients. As shown in Figure 1.8, LTS symbols (ch_i_in, ch_q_in) in the time domain with CFO correction are transformed into frequency domain signals using the FFT module to enable LS_FDE. Channel estimation is performed by taking LTS signals in the frequency domain and passing them to the mult_by_LTS sub-block. In this sub-block, known LTS symbols are stored in a ROM. The received LTS symbols are compared with the known LTS symbols, and the coefficients are determined. Two estimation values are added on top of each other and kept in the estimate buffers sub-block in memory. After two channel estimations are completed, the result is divided by two to take the average, and channel estimation is completed. The channel estimation in the frequency domain is transformed back to the time domain using the IFFT operation to enable reconstruction in the time domain (td_r). As a result, the next block can use the impulse response of the channel that has been generated by the channel estimation block (td_r). In the simulation shown in Figure 1.9, the channel impulse response of 64 samples is observed. The end of the channel impulse response is indicated by the ms_ch_h_last_out signal.

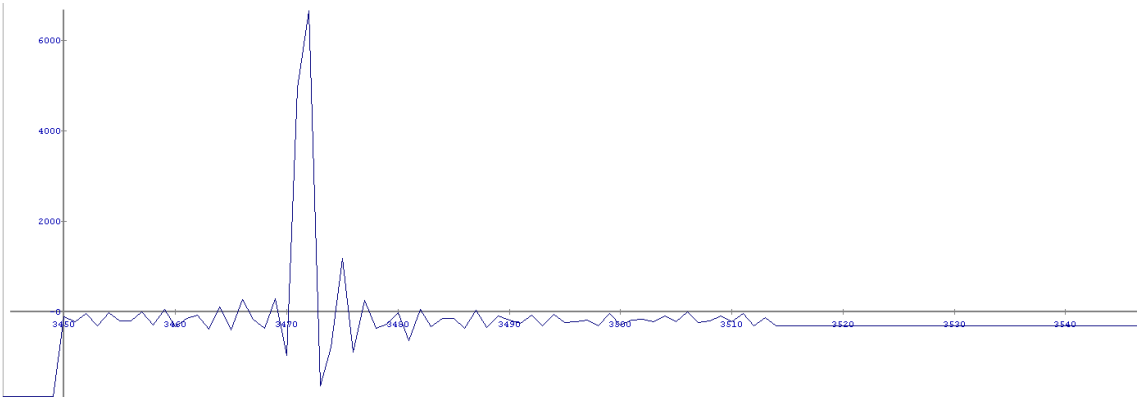

Figure 3.6 Chipscope output of estimation block in frequency domain

3.2.4 Time Domain Reconstruction Block

The received transmission signals from the transmitter are simulated by convolving them with the time-domain channel impulse response obtained from channel

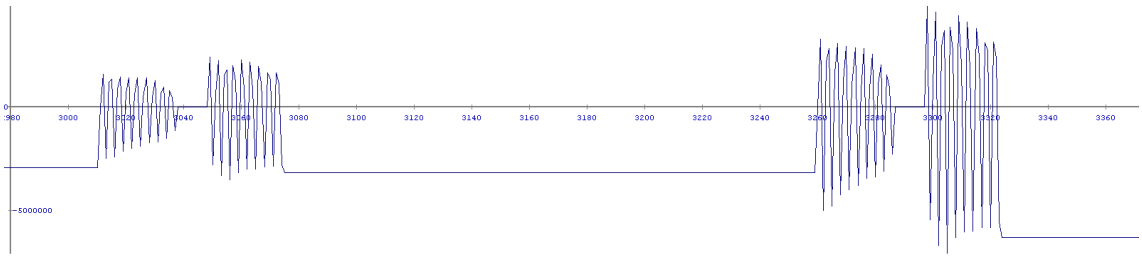

Figure 3.7 Chipscope output of estimation block in time domain

estimation. For this purpose, the coefficients of the convolution filters (FIR) in the td_r block shown in Figure 1.10 are loaded with the channel impulse response (ch_i_in, ch_q_in). The coeff_reload block performs this operation. After loading the channel impulse response coefficients in reverse order addressing to FIR filters, the td_r_config_done_out signal is generated. Thus, FIR filters are ready to perform convolution. The signals obtained by convolution are reconstructed to resemble the received signal by passing through the interpolation filter (FIR filter at the end). The signals' amplitudes at the interpolation filter's output are adjusted using re-scaling and then sent to the cancellation block. The simulation graphs for the time-domain reconstructed ms_td_r_data_i_out and ms_td_r_data_q_out signals sent to the cancellation block are given in Figure 1.11.

3.2.5 Cancellation Block

The received signals from the transmitter are aligned (aligned) in the ADC output by being stored in the memories (dual port RAM) in the cancellation block shown in Figure 1.12. The cancellation block is triggered by the td_r_config_done_out signal that has been generated in the td_r block, the cancellation block starts reading the received signals from the dual port RAMs by generating a read address. The reconstructed signals (td_r_data_i_in, td_r_data_q_in) from the td_r block are then subtracted from the received signals read from the RAMs to perform the cancellation process. The simulation graph in Figure 1.13 shows the received signals and the reconstructed signals are displayed one above the other. The remaining ms_res_data_i_out and ms_res_data_q_out signals after cancellation represent the suppressed signal.

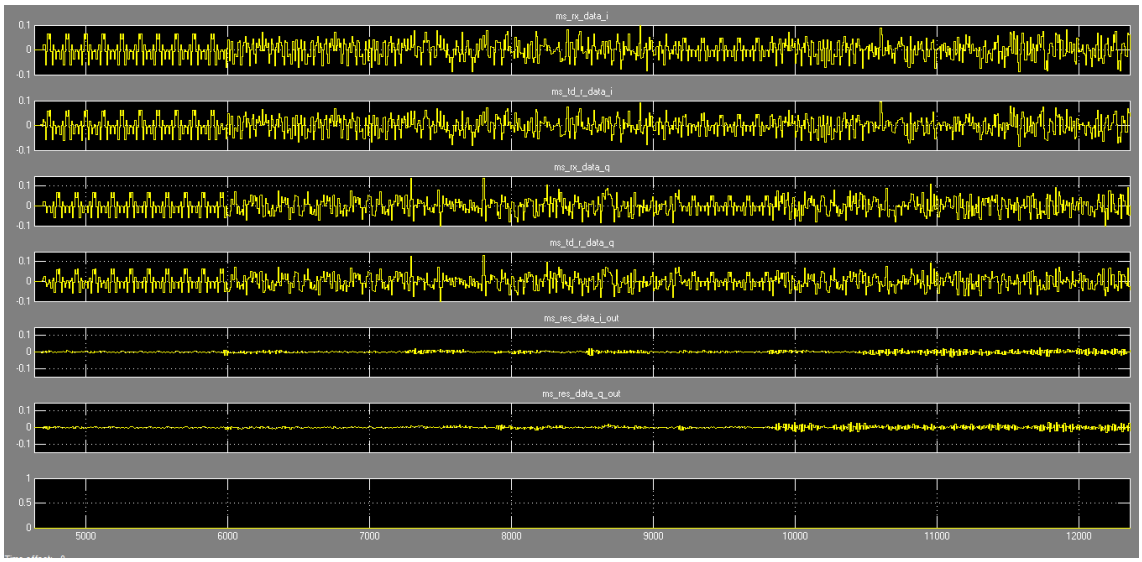

Figure 3.8 Simulation result of the cancellation block

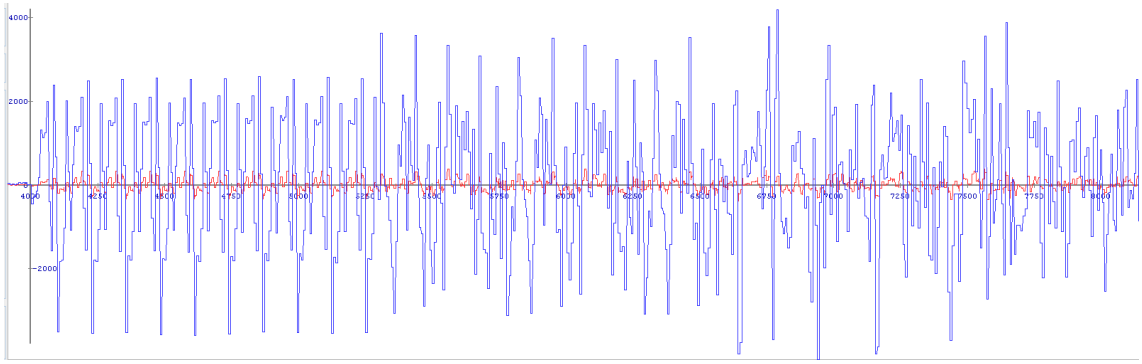

Figure 3.9 Output of the cancellation block

3.2.6 Integration of the Self-Interference Cancellation Module with the 802.11 Reference Design in XPS Environment

After the design of the blocks using the System Generator program, all the blocks were combined into a single block and named with input-output signals. The self-interference cancellation module was transferred to the XPS environment and the necessary input-output connections were made. The tx_start signal, which indicates the start of transmission from the transmission chain, was generated and connected to the start input (Figure 1.15), which will start the cancellation module. The adc_i_in and adc_q_in signals were connected to the output of the ADC module inside the FPGA board. The tx_i_in and tx_q_in signals were taken from the output of the DAC module, as shown in Figure 1.16, from the last stage of the reference design's transmission chain before being fed to the antenna. After the necessary connections were made, a bit file was created to program the entire design

into the FPGA board. This file was later combined with C codes obtained in the SDK environment to program the FPGA board with .elf files.

After the design of the blocks was done with the System Generator program, all the blocks were made into a single block and the input and output signals were named. The self-interference cancellation module was transferred to the XPS environment and the necessary input-output connections were made. The tx_start signal is generated from the transmitter chain, which informs the module when the transmission starts. This signal is connected to the start input, which will start the cancellation module. The adc_i_in and adc_q_in signals are connected to the output of the ADC module inside the FPGA board. The signals tx_i_in and tx_q_in are taken from the output of the DAC module, from the last link of the transmit chain of the reference design before being fed to the antenna. After making the necessary connections, a bit file was created to program the whole design into the FPGA card. This file was then combined with the .elf files obtained with C codes in the SDK environment and programmed into the FPGA card.

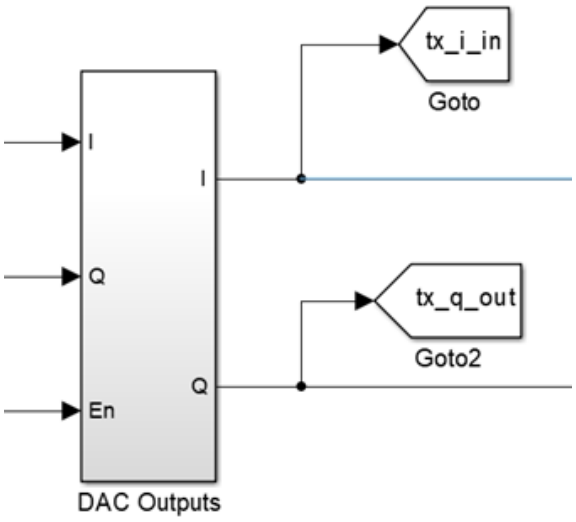

Figure 3.10 Output signals from TX chain

3.3 Integration of Linear DSIC with Transmit and Receive Blocks

The FD radio set-up on which the linear cancellation algorithm has been implemented is given in Figure 3.14. The linear cancellation algorithm which has been integrated with the FD radio is executed in real-time on the WARP v3 SDR board [23], which supports IEEE 802.11a/g physical layer, operating at 2.4 GHz and 5 GHz

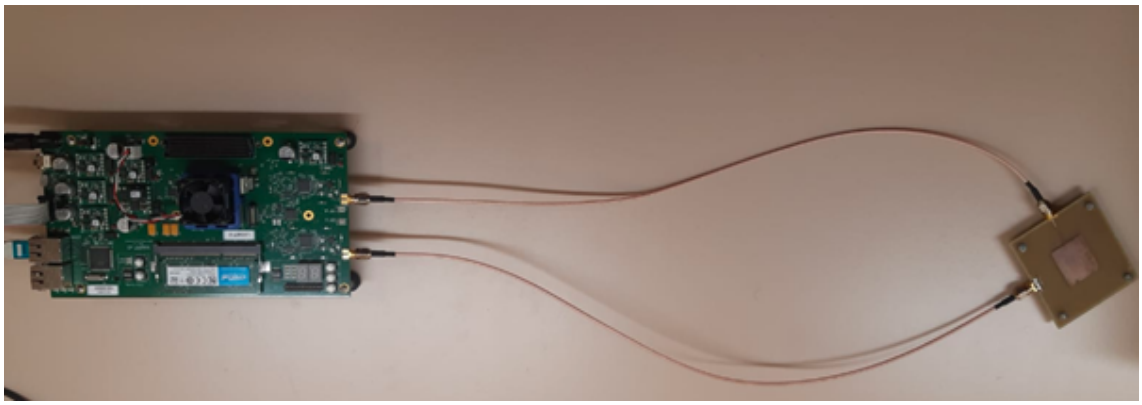

Figure 3.11 FD radio set-up

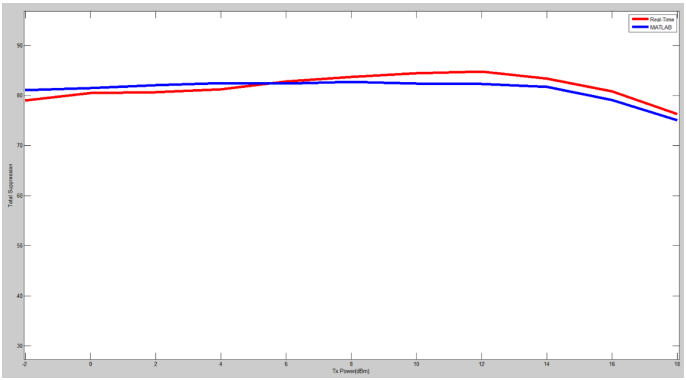

Figure 3.12 Total suppression performance of the SI module

wireless bands with 20 MHz bandwidth.

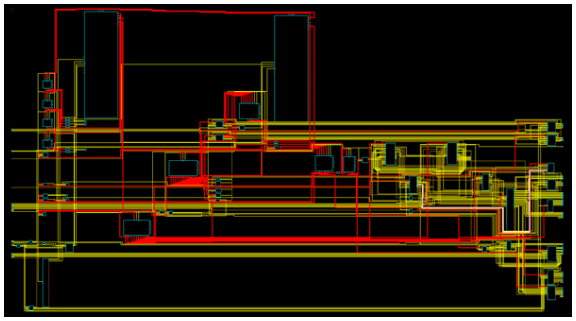

Figure 3.13 SIC Module connections in XPS environment

Table 3.2 FPGA resource usage of different researches

	Flip Flops	LUTs	Digital Cancellation
2019 [25]	37778	67632	48 dB @14 dB Tx power
2022 [26]	38718	85663	46 dB @8 dB Tx power
2018 [27]	66627	56776	48 dB @8 dB Tx power
This work	3606	2445	20 dB @8 dB Tx power

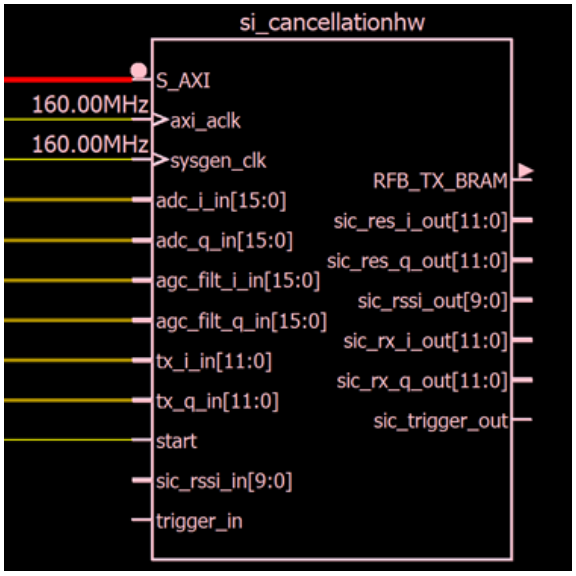

Figure 3.14 SIC Module XPS environment

The set-up consists of a WARP v3 SDR board [23], a dual polarized slot coupled antenna [24], and a laptop that is used for programming and reading ChipScope data from the board through JTAG cable. The transmission signal is generated by the local traffic generator which has been implemented in WARP boards.

The SDR board has a noise floor of -85 dBm and is configured to operate at a frequency of 2.45 GHz. The dual polarized slot coupled antenna, mentioned in references [3] and [24], offers the highest level of isolation at this frequency. During cancellation experiments, the fabricated antenna exhibited an inter-port isolation of more than 55 dB for a 20 MHz bandwidth. Each transmission includes a total of 700 OFDM symbols.

The comparison between recent work and this work is presented in Table 3.2. The implemented linear DSIC algorithm has lower complexity as compared to the non-linear algorithms considered in [25], [26], [27]. As seen in the table, the resources used in the FPGA board in this work are significantly lower than existing research with the trade-off of digital cancellation performance.

3.4 Implementation of Physical Layer Full-Duplex Communication Protocol

For the integration of the SI cancellation module to the physical layer, the NoMAC protocol is used. NoMAC protocol is implemented in the WARP board and this protocol does not perform any medium access control. According to the NoMAC protocol, packets are sent with a certain interval without receiving any acknowledgement. This basic protocol is used because the performance of the SI cancellation

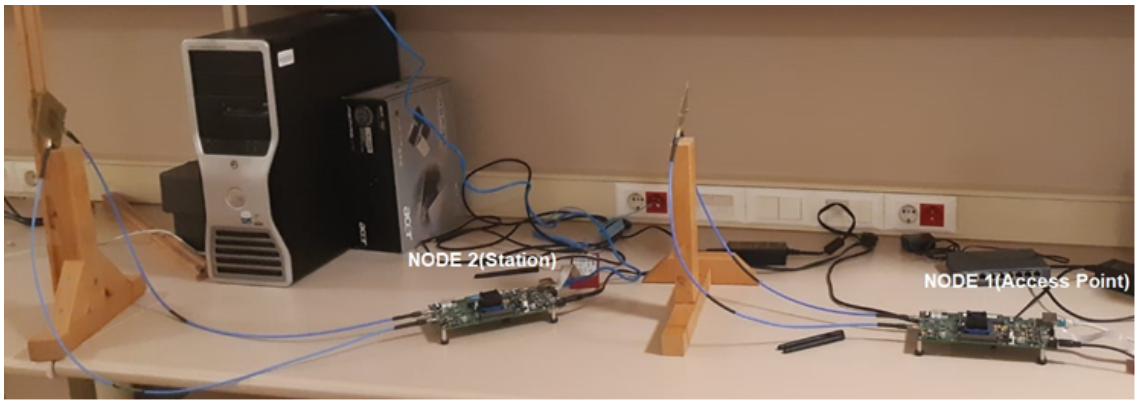

Figure 3.15 Test bed for full duplex communication

block is expected to be the same for the other protocols as long as the LTS part of the frame is received without any interference. Since the LTS part of the frame needs to be received without any interference, the frame structure is changed in accordance with[[15]]. When the two-way transmission begins, the first STS and LTS part of the self-interference signal should be received without the transmitted signal from the second node. For this purpose silent space is created as seen in figure 3.17

Silent space is created by making changes in the reference design transmission chain provided by the WARP board. After the preamble is generated, the preamble done signal is given to a FIFO memory to start the data part of the frame. This preamble done signal is delayed for the desired time to create silent space. The system generator blocks are shown in figure 3.18 For test purposes, silent space is kept larger than needed. Ideally, this space should be exactly the length of the preamble of the frames. In figure 3.15, the set up for full duplex communication is given.

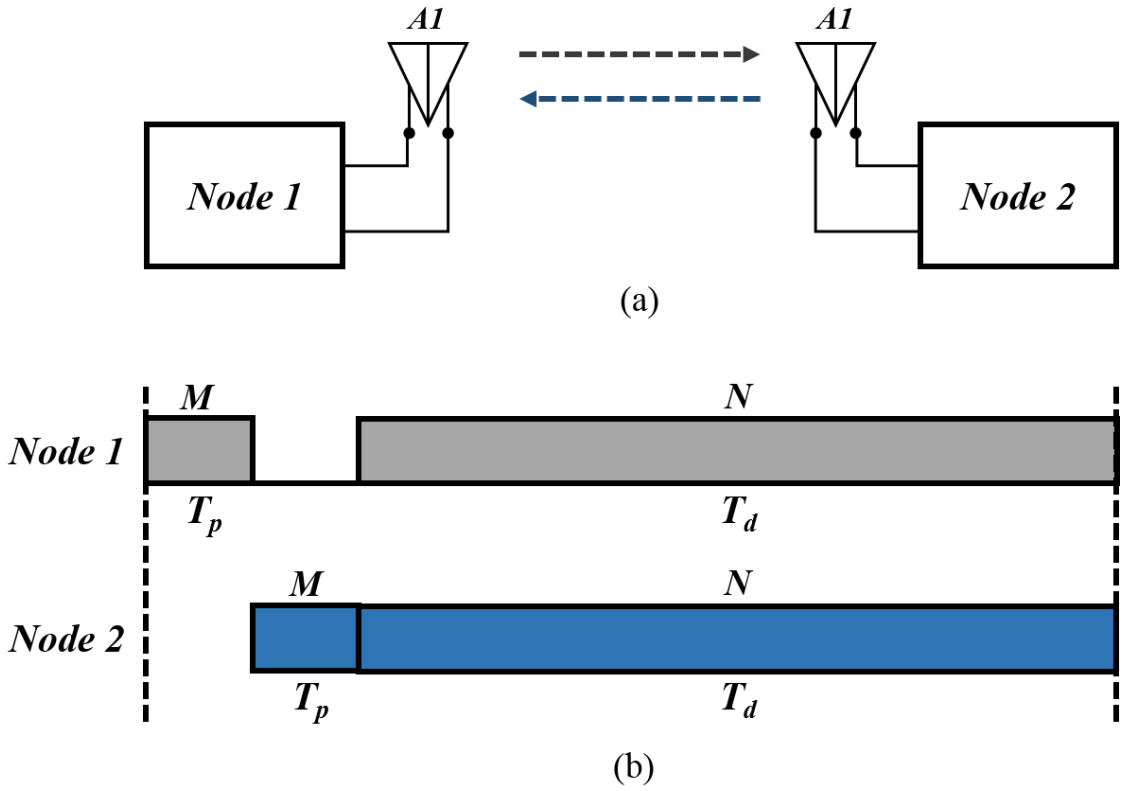

Figure 3.16 (a) Bidirectional FD communication (b) Frame timings for Node 1 and Node 2 [15]

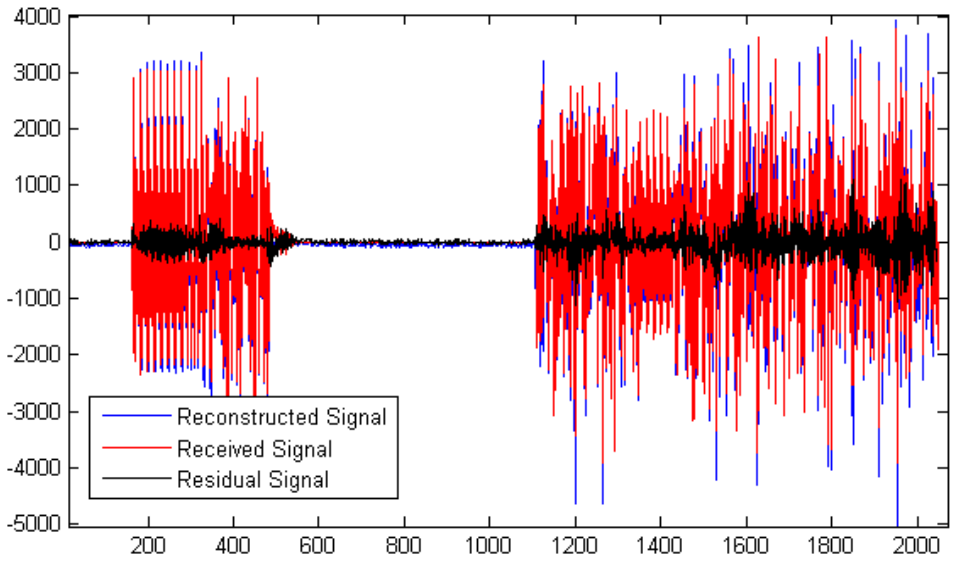

Figure 3.17 Time-Domain signals for cancellation block

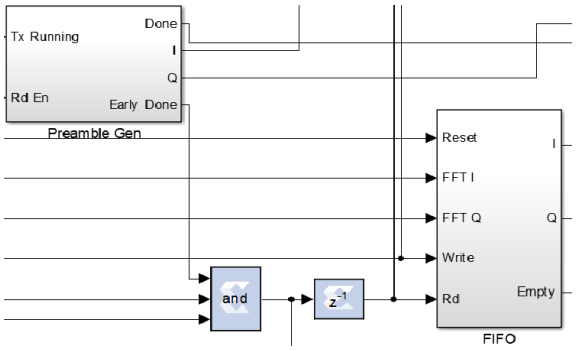

Figure 3.18 System generator block that is responsible for silent space

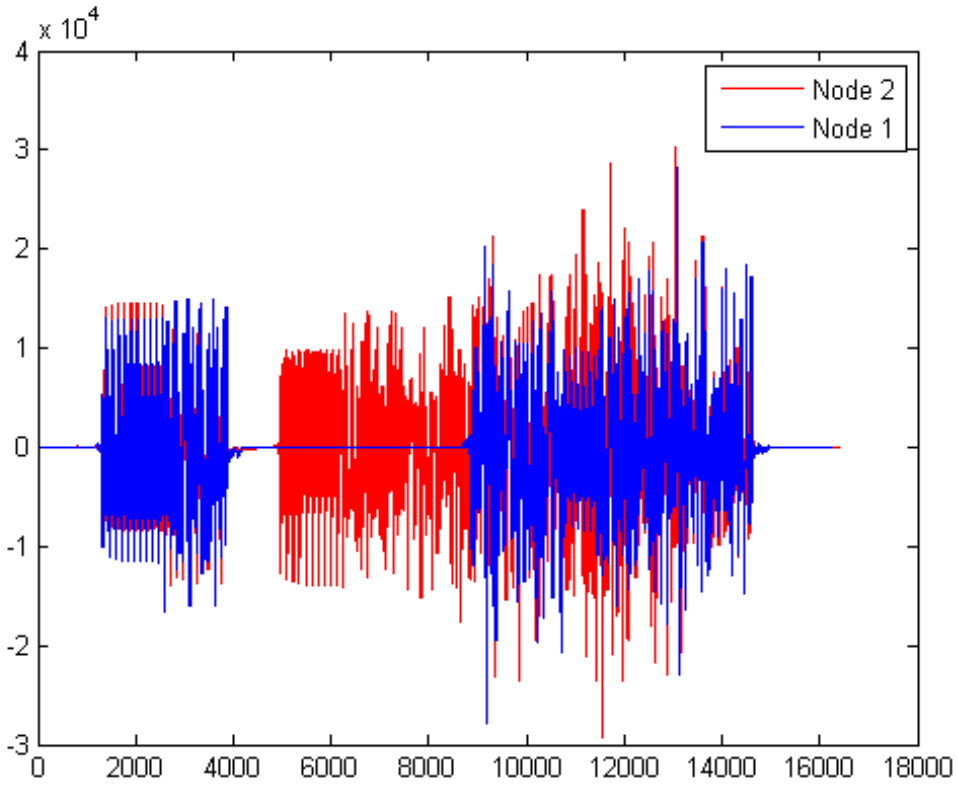

Figure 3.19 Received signal in Node 1 while full duplex communication

Chapter 4

FULL DUPLEX MULTIPLE INPUT MULTIPLE OUTPUT COMMUNICATION (FD-MIMO)

4.1 Linear and Non-linear DSIC for FD-MIMO

In this chapter, we propose to apply the FD-switched (FD-SW) radio architecture in [14] and extend it for MIMO systems. FD-SW radio architecture addresses non-linearity effects separately for MIMO systems. The architecture is given in figure 4.1. The architecture allows for the approximation, reconstruction, and provision of a realistic reference signal for linear DSIC with high accuracy, effectively estimating the non-linear effects of the power amplifier in the transmitter chain and the low noise amplifier in the receiver chain. The proposed FD-SW architecture is comprised of two modes: the estimation (training) phase and the cancellation phase. During the estimation phase, the switch is set to the first position (as shown in red in 4.1), forming a loop-back from the transmitter port to the receiver port of the radio board for each stream. The ADC output serves as the SI signal, along with the known baseband transmit signal, and is provided to the non-linear estimation blocks. The weights of the MP model are learned based on the loop-backed SI signal, which only includes non-linear effects and excludes the effects of the SI channel. During the reconstruction phase, the weights that were trained and calculated during the estimation phase are stored in the non-linear reconstruction block. These stored weights are then utilized in subsequent transmissions, allowing for their reuse.

In the reconstruction phase, the non-linear weights acquired and saved during the estimation phase are utilized along with the baseband transmit signal to create the

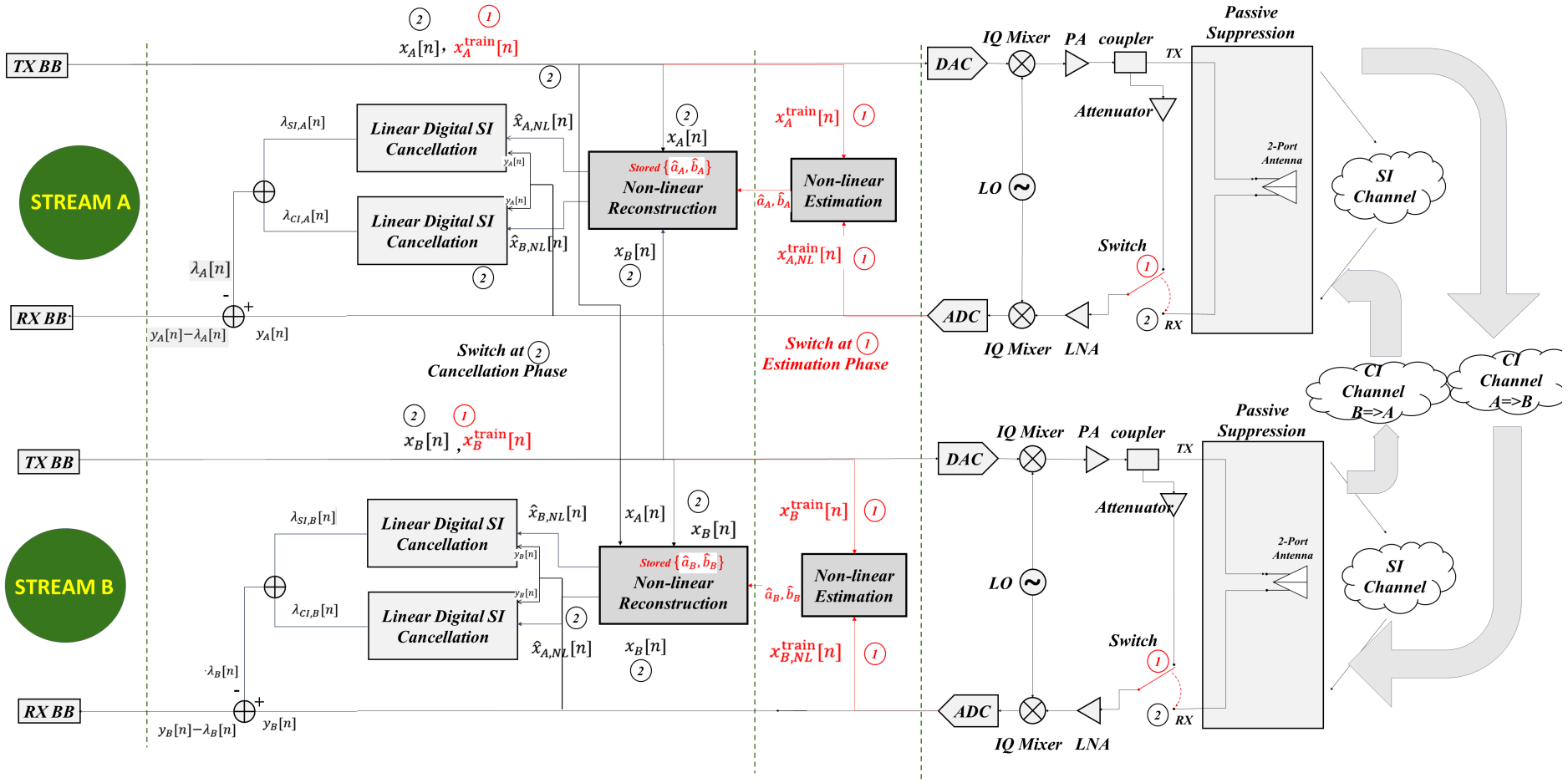

Figure 4.1 Proposed switched FD MIMO architecture

non-linear reference SI signal. Following this, linear SI cancellation employs both the non-linear reference SI signal and the received baseband SI signal to estimate the SI channel and reconstruct the SI signal. The estimation of the linear SI channel is performed on the Long Training Sequence field within the preamble of the received OFDM packet. The obtained SI channel estimate is then applied to the data portion of the OFDM packet to reconstruct the SI signal.

As seen in Figure 4.4, there is also cross interference for the receiver to reconstruct and subtract from the received signal to have a clear signal of interest. The cross-interference is also reconstructed by the linear DSIC block. This operation is also shown in Figure 4.4. The baseband transmitted signal is taken from the transmitter chain in stream B to reconstruct the cross-interference in stream A. This signal goes into the same block with MP coefficients for stream A. The same sequence is applied for the cross interference received in stream B. This time, the baseband transmit signal is taken from stream A and stored coefficients are taken from stream B. The baseband signals and stored weights are worked according to the 2.15 and cross-interference is reconstructed. To achieve SI cancellation, the received signal is processed by subtracting the reconstructed SI signal and CI (Common Interference) signal. Within the framework of this architecture, various digital linear SI cancellation algorithms can be employed, including time-domain estimation (TE) or frequency-domain estimation (FE) combined with time-domain reconstruction (TR) or frequency-domain reconstruction (FR). These algorithms provide different approaches for estimating and reconstructing the SI signal to effectively cancel out interference. [14]. In figures 4.3 and 4.2, it can be seen that the loopback cable

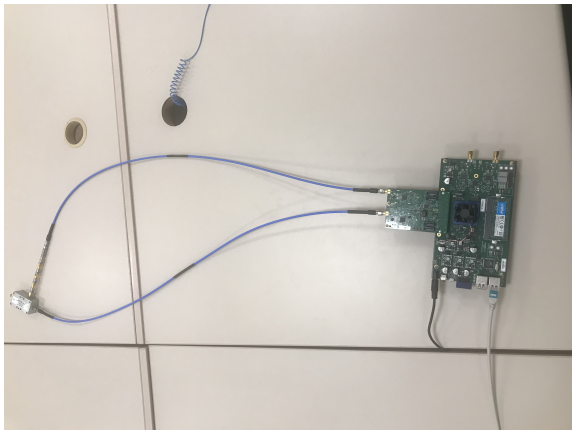

Figure 4.2 Training phase for Stream B

is connecting the transmitter port to the receiver port with 71 dB of attenuation. After training is done, loop-back cables are switched with the antennas to perform non-linear cancellation.

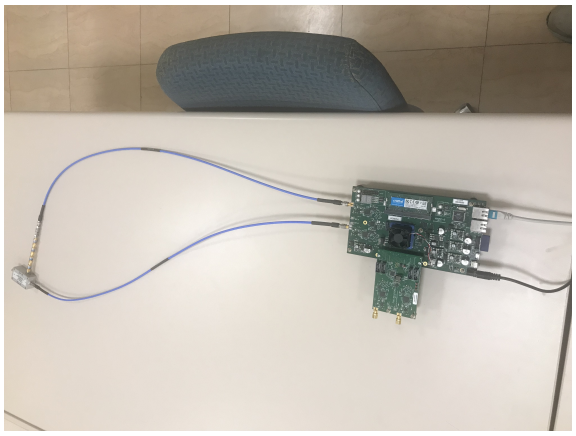

Figure 4.3 Training phase for Stream A

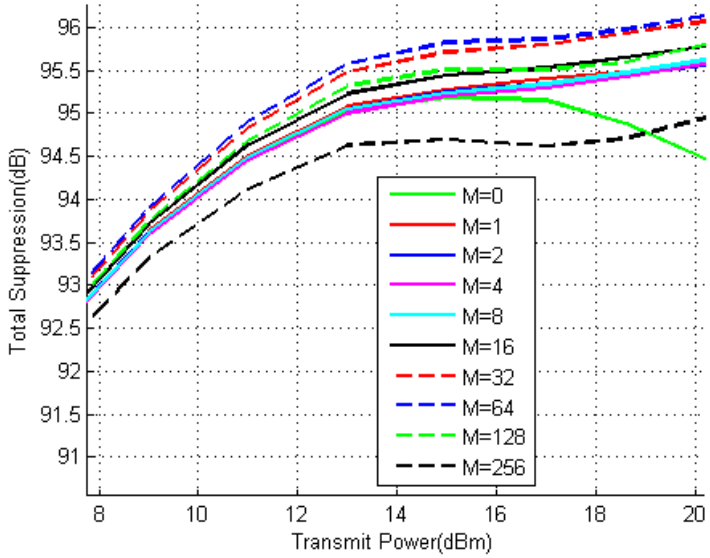

Figure 4.4 Training parameters for Stream A

4.2 Training Overhead and Data Rate Analysis

4.2.1 FD Communication with Linear only DSIC

As far as FD SISO communication is considered with linear only DSIC, transmitted data (the number of samples) is roughly doubled due to simultaneous transmission and reception in the same frequency band. On the other hand, the bit rate is not exactly doubled because of the overhead introduced in the preamble of the OFDM packet. Hence, the bit rate for FD SISO communication can be calculated as:

$$R_{SISO}^{FD} = \frac{2N.k_d}{T_p^{F,S} + T_d^{F,S}} \quad \text{bps}, \tag{4.1}$$

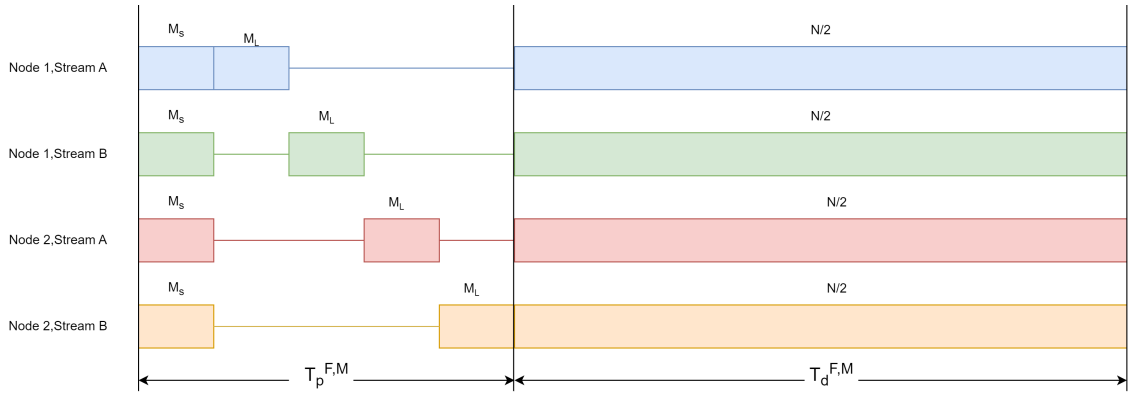

Figure 4.5 Frame structure of bidirectional FD MIMO communication utilizing only packet preamble for DSIC

where $T_p^{F,S}$ and $T_d^{F,S}$ denote the preamble and data transmission time of FD SISO, respectively. In FD communication, data transmission time ($T_d^{F,S}$) is the same as HD communication (2800 µs) whereas the number of preamble samples increases because of the overhead. For each stream, there are 30 STS (16 samples each) and 4.5 LTS (64 samples each). When one stream transmits its preamble the other stream stays silent. Thus, the total number of preamble samples becomes 1536 and $T_p^{F,S}$ is calculated as 76.8 µs. Then, with the current parameters, R_{SISO}^{FD} has a bitrate of 155.73 Mbps.

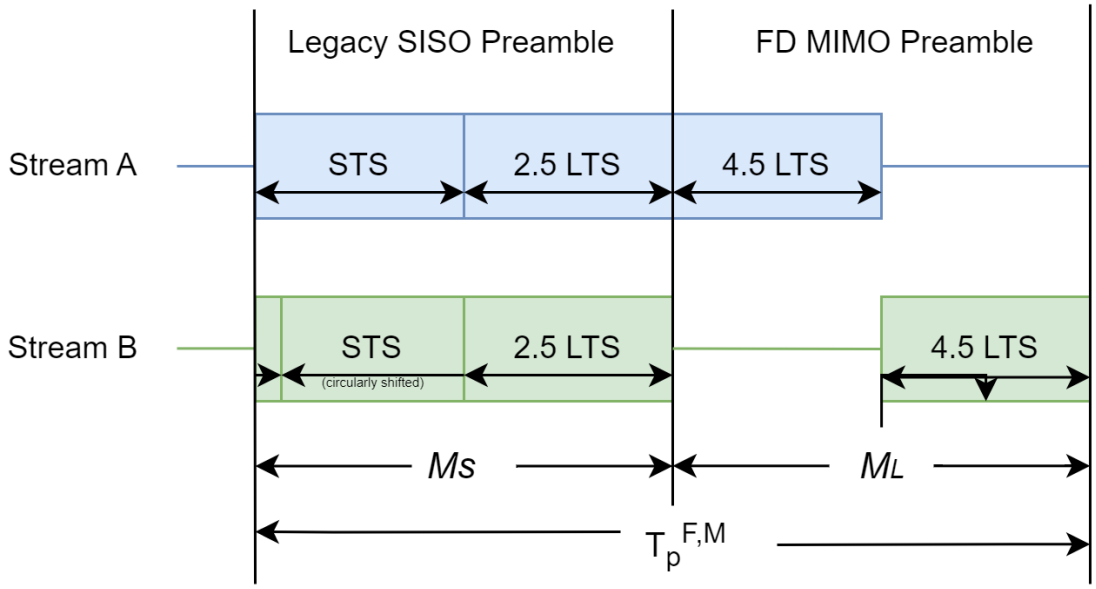

Figure 4.6 Frame structure for FD MIMO systems with linear only DSIC for Node 1

For FD MIMO communication, the bitrate formula can be derived as the combination of the previous two formulas. The frame structure is illustrated in Fig. 4.5. Data transmission time halves due to the MIMO framework while transmitted data (number of samples) is doubled due to the FD structure. However, the number of

preamble samples increases to estimate channel among different antennas as seen in Fig. 4.6. Hence, the bit rate for FD MIMO can be formulated as:

$$R_{MIMO}^{FD} = \frac{2N.k_d}{T_p^{F,M} + T_d^{F,M}} \quad \text{bps}, \tag{4.2}$$

where $T_p^{F,M}$ and $T_d^{F,M}$ denote the preamble and data transmission time of FD MIMO, respectively. In 2x2 MIMO, data transmission time ($T_d^{F,M}$) is the half of the SISO (1400 µs). On the other hand, the number of preamble samples increases because of the overhead. For FD communication at each node, In addition to 30 STS (16 samples each) and 4.5 LTS (64 samples each) transmission in the preamble, 4.5 LTS (64 samples each) is transmitted in turn for channel estimation of each antenna as illustrated in Fig. 4.6. Thus, the total number of preamble samples becomes 2688 and $T_p^{F,M}$ is calculated as 134.4 µs. Then, with the current parameters, R_{MIMO}^{FD} has a bitrate of 291.97 Mbps.

4.2.2 FD Communication with Nonlinear DSIC

As far as FD SISO communication is considered with nonlinear DSIC, transmitted data (the number of samples) is roughly doubled due to simultaneous transmission and reception in the same frequency band. On the other hand, the bit rate is not doubled because of the overhead for the training of the nonlinear DSIC. Hence, the bit rate for FD SISO with nonlinear DSIC communication can be calculated as:

$$R_{SISO,NL}^{FD} = \frac{2N.k_d}{T_p^{F,S} + T_{d_{tr}}^{F,S} + T_{d_{test}}^{F,S}} \quad \text{bps}, \tag{4.3}$$

where $T_{d_{tr}}^{F,S}$ and $T_{d_{test}}^{F,S}$ denote parts of data transmission time T_d, namely training and test for FD SISO, respectively. For linear channel estimation, there are 30 STS and 4.5 LTS for each node, the same as FD with linear-only DSIC. When one node transmits its preamble the other node stays silent and the total number of preamble samples is 1536 and $T_p^{F,S}$ is 76.8 µs as in (4.1). For nonlinear DSIC, the optimal training length is obtained as 10000 data samples [28, 29]. Thus, the overhead due to nonlinear DSIC for two nodes becomes 20000 samples and $T_{d_{tr}}^{F,S}$ is calculated as 1000 µs. The required time for the remaining 46000 samples ($T_{d_{test}}^{F,S}$) is equal to 2300 µs. Therefore, with the current parameters, $R_{SISO,NL}^{FD}$ has a bitrate of 132.67 Mbps.

For FD communication with 2x2 MIMO, data transmission time is halved and the number of transmitted samples is almost doubled. In addition to overhead in the

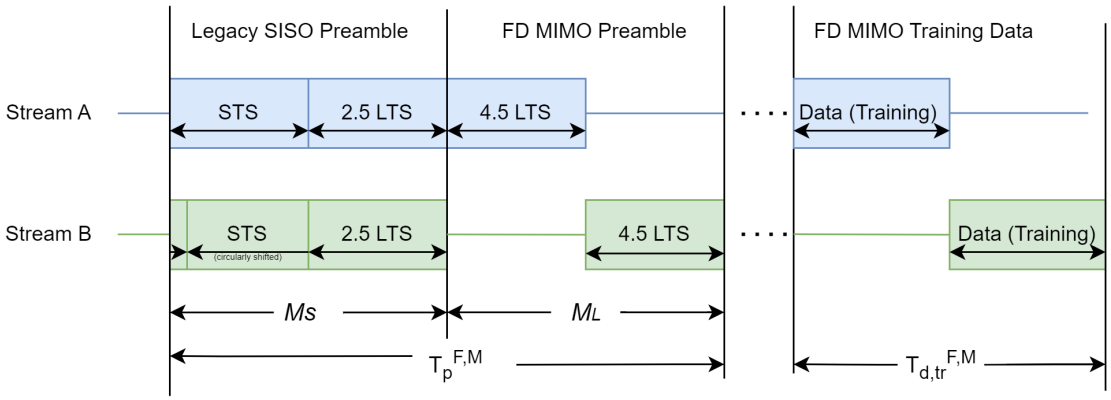

Figure 4.7 Frame structure for FD MIMO systems with linear and nonlinear DSIC for Node 1

preamble due to linear channel estimation, there is an overhead in data samples because of the training of the nonlinear DSIC. Thus, the bit rate for FD MIMO with nonlinear DSIC can be formulated as:

$$R^{FD}_{MIMO,NL} = \frac{2N.k_d}{T^{F,M}_p + T^{F,M}_{d_{tr}} + T^{F,M}_{d_{test}}} \quad \text{bps}, \tag{4.4}$$

where $T^{F,M}_{d_{tr}}$ and $T^{F,M}_{d_{test}}$ denote parts of data transmission time T_d, namely training and test for FD MIMO, respectively. In 2x2 MIMO, the number of preamble samples increases because of the overhead. At each node, in addition to 30 STS and 4.5 LTS transmission in the preamble, 4.5 LTS (64 samples each) is transmitted in turn for channel estimation of each antenna as shown in Fig. 4.7. Thus, the total number of preamble samples becomes 2688 and $T^{F,M}_p$ is calculated as 134.4 µs. Since the optimal training length for nonlinear DSIC in SISO is obtained as 10000 data samples, each stream requires 5000 samples in a 2x2 MIMO system. Thus, the overhead due to nonlinear DSIC for two streams becomes 20000 samples and $T^{F,M}_{d_{tr}}$ is calculated as 1000 µs. Since there are two streams in 2x2 MIMO, the required time for the remaining 23000 samples ($T^{F,M}_{d_{test}}$) is equal to 1150 µs. Therefore, with the current parameters, $R^{FD}_{MIMO,NL}$ has a bitrate of 196.11 Mbps.

For the proposed switched FD-MIMO structure, training is done once and the coefficients are recorded for subsequent transmissions. The data required for the training is considered just for the power-up. Since there will not be a need for any training data for the subsequent transmission, training overhead becomes insignificant. To calculate the data rate, we can consider 4.2 for switched FD-MIMO.

Data rate analysis results of the considered communication systems are given in Table 4.2. As seen in the table, FD MIMO with linear DSIC provides approximately

2 times the data rate in comparison to FD SISO with linear DSIC and HD MIMO communication, and approximately 4 times the data rate in regards to HD MIMO communication. However, as the transmit power is increased, linear DSIC becomes insufficient due to hardware-induced nonlinear distortions. By using nonlinear DSIC, the transmit power and thus the range increases for FD MIMO, while the achieved data rate becomes less than the FD MIMO with linear DSIC. This issue leads us to our proposed work. Since there is negligible overhead in the proposed system, the data rate is equal to the data rate of the linear MIMO system as shown in Table 4.2

Table 4.1 Data Rate of the Considered Communication Systems

	SISO	**MIMO**
HD	79.10 Mbps	155.38 Mbps
FD w/ Linear DSIC & SW MP	155.73 Mbps	291.97 Mbps
FD w/ Nonlinear DSIC (MP)	132.67 Mbps	196.11 Mbps

4.3 Performance Results

In this section, the total suppression performances of the proposed architecture and existing algorithms are compared. The measurements are performed with different transmit powers which vary between 5 dBm and 19 dBm.

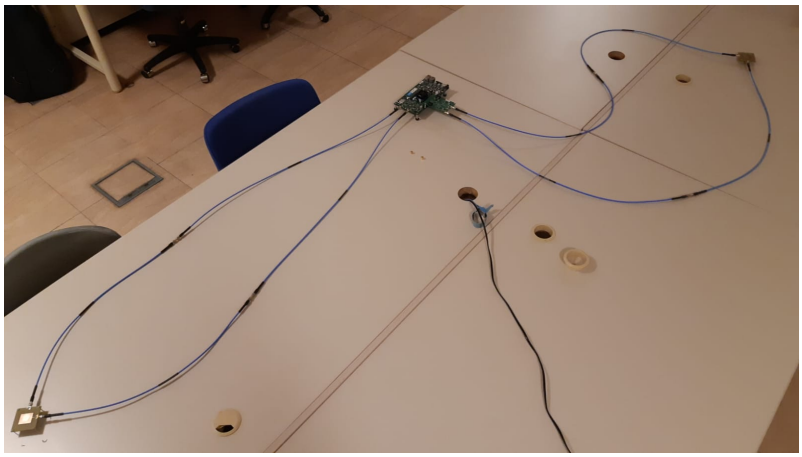

Figure 4.8 Setup for switched FD-MIMO architecture

Tests are performed up to 19 dBm of transmit power because SDR boards transceiver behaviour becomes unpredictable as RF circuitry enters saturation mode and non-linearities are beyond our model. Optimized memory and degree parameters are used for every algorithm. The FD-MIMO Parameters used for the experiments are presented in Table 4.1.

In Figure 4.8, we present our OFDM-based FD radio setup, which utilizes a dual port antenna [3] and the WARP v3 SDR to support the IEEE 802.11a/g physical

layer standard. The implementation of non-linear SI estimation/reconstruction and linear SI cancellation algorithms is done using MATLAB on a laptop computer. For the FD-SW radio architecture, the loopback functionality is achieved by switching the cables by hand. After the training operation, cables are removed and antennas are connected to the ports.

In the MATLAB environment, the transmitted waveform is generated and then transmitted to the SDR board through an Ethernet connection. From there, it is transmitted over the air using the antenna and received by the FMC-RF-2X2451 receiver board via the loopback cable. The received waveform is then transferred back to the MATLAB environment on the computer through the Ethernet connection. The non-linear SI estimation phase of the FD-SW radio is executed in MATLAB using the samples received from the FMC-RF-2X245 receiver board and main SDR board. Stream A is implemented in the main board while stream B is implemented in FPGA Mezzanine Card (FMC). MATLAB is also responsible for implementing the switching between the estimation and cancellation phases. In the training phase, collected data is processed and weights are calculated. Calculated weights are stored in the MATLAB workspace. Stored weights can be used as long as desired unless there is any change in hardware. Since the electronic components deteriorate over time, training should be done regularly for healthy and reliable processing.

As seen in 4.9, switched MP algorithm improves for high transmit powers. In 4.10 switched MP algorithm for stream B gives similar performance to existing linear and MP algorithms. The RF chain of stream B has lower isolation between TX and RX ports than the isolation of the hardware which is employing stream A. This difference in isolation is affecting more in higher transmit powers. Since there are 3-4 dBm of difference in isolation difference between boards for stream A and stream B, the same difference is observed in switched MP algorithm performance. The data shown in black in 4.9 and 4.10 represents the auxiliary solution to non-linear DSIC. The

Table 4.2 Parameters for SW/MP FD-MIMO Radio setup

Bandwidth	20 MHz
Center Frequency	2.41 GHz
Sampling Rate	40 MHz
Antenna Suppression	71 dBm
Noise Floor	-86 dBm
Transmit Power Range	5-19 dBm
# of Subcarrier	64 Mbps
Modulation	16-QAM
Memory & Degree(Stream A)	5 / 120
Memory & Degree(Stream B)	5 / 200

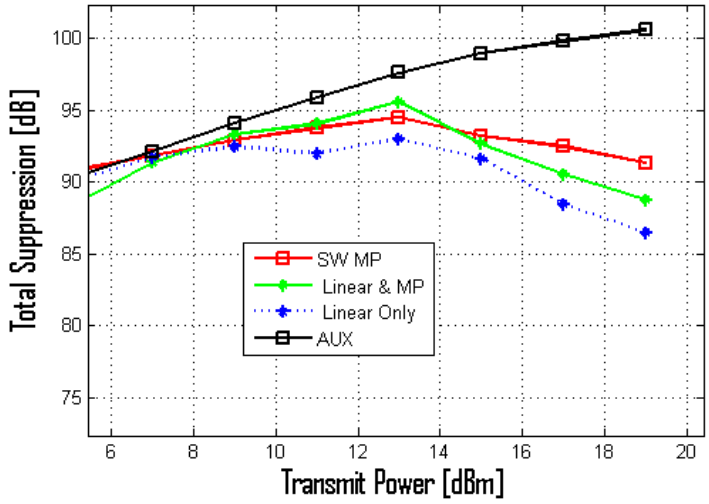

Figure 4.9 Suppression performance of Stream A with differential antenna

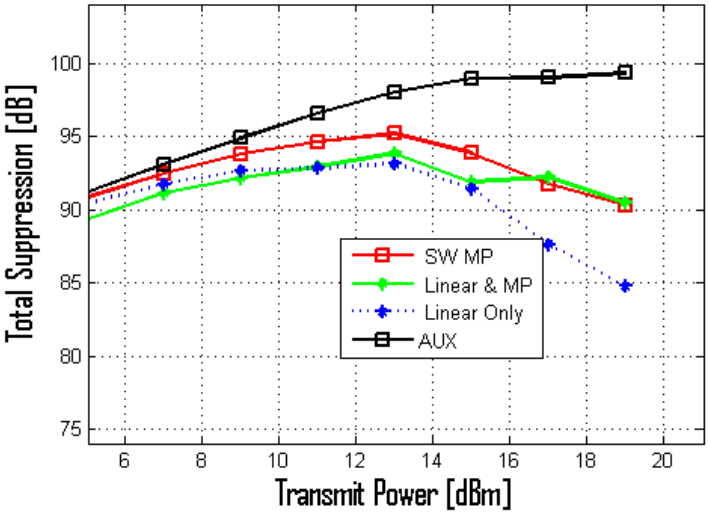

Figure 4.10 Suppression performance of Stream B with differential antenna

reference signal is taken from the auxiliary board while the cancellation operation is done. This solution is our upper limit as far as performance is concerned.

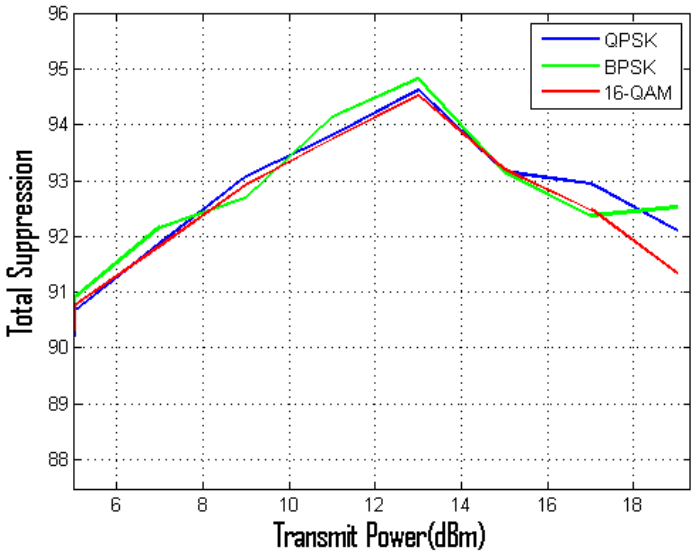

Figure 4.11 Suppression performance of Stream A with different data rates

Different data rates are considered in figure 4.11. BPSK, QPSK and 16-QAM modulation schemes are performed with the MIMO setup. As expected, the cancellation performance is not affected by the modulation schemes as seen in 4.11

Chapter 5

CONCLUSIONS

The results obtained in this study support the effectiveness of self-interference cancellation techniques in mitigating self-interference in full-duplex OFDM communication systems. The experiments conducted demonstrate that the proposed algorithms significantly reduce the level of self-interference, resulting in improved signal quality.

In the first part of the thesis, the digital circuitry block of the linear cancellation algorithm is integrated into the existing SDR board which employs IEEE 802.11 standard. The results show that real-time implementation performance is in cohesive with the results obtained from MATLAB.

Our experiments have demonstrated that the MIMO self-interference cancellation technique can effectively cancel out self-interference in full-duplex communication systems. By using switched MP architecture, we have observed improvement in the signal of interest quality while simultaneous transmission and reception.

The comparison of the proposed self-interference cancellation techniques with existing methods revealed that the proposed algorithm outperforms the current state-of-the-art techniques in terms of suppression performance. The improvement in suppression performance is attributed to the ability of the proposed algorithms to effectively estimate and cancel out the non-linear effects of the SDR hardware.

However, despite the promising results, there are still some limitations that need to be addressed. One of the major limitations is the complexity of the proposed algorithms, which may limit their practical implementation in real-time MIMO systems. Future research should focus on developing more efficient algorithms that can achieve similar or better performance with reduced computational complexity.

Another limitation is the sensitivity of the proposed algorithms to certain parameters such as signal power and interference power and isolation between transceiver

ports. Further investigations are needed to determine the optimal values of these parameters to achieve the best performance in different scenarios. The issue with the isolation between transceivers is related to the radio boards. If the boards are replaced with ones that have better RF circuitry, suppression results will get improve.

In conclusion, this study demonstrates the effectiveness of self-interference cancellation techniques in mitigating self-interference in full-duplex communication systems. The proposed algorithms outperform existing techniques in terms of suppression performance, but there is still room for improvement in terms of computational complexity and sensitivity to certain parameters. Future research should focus on addressing these limitations to enable the practical implementation of self-interference cancellation techniques in real-time systems.

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