AN 8-BIT 100 MS/s TIME-INTERLEAVED SAR-ASSISTED PIPELINE ADC WITH IMPROVED RESIDUE AMPLIFIER

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ABSTRACT

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Keywords: High-speed SAR logic, Residue Amplifier, SAR-Assisted Pipeline ADC, Simultaneous-Switching Noise (SSN), Zero-Crossing Detector (ZCD)

In a successive approximation register (SAR)-assisted pipeline analog-to-digital converters (ADC), SAR ADC and residue amplifier are the two blocks that determine the speed and power of the ADC. Among them, the residue amplifier is the most power-hungry. Traditionally, the residue amplifier uses a high-gain op-amp, but as the CMOS technology scales, the intrinsic gain of the transistor reduces. Hence, the residue amplifier is designed based on zero-crossing-based circuits (ZCBCs) as it is not affected by the scaling down of the CMOS technology. The limitation of the ZCBC-based residue amplifier is the overshoot voltage arising for technology nodes that have low f_T. Hence, a novel overshoot reduction technique is introduced in the residue amplifier. The overshoot voltage and time were simulated for different corner cases. The final range of the overshoot voltage and time after implementing the novel overshoot reduction technique was attained from 0.584 mV to 1.59 mV and 124 ps to 423 ps, respectively. The percentage reduction in the overshoot time and voltage ranges w.r.t to the case when the overshoot reduction technique was not used ranges from 90.544 % to 98.012 % and 89.153 % to 97.67 %, respectively. The novel overshoot reduction technique was implemented in the 2-bit/cycle sub-radix V_{cm}-based SAR-assisted pipeline ADC. The post-layout simulation results show an SNDR, an SFDR, and an ENOB of 56.57 dB, 62.98 dB, and 9.1046 bits, respectively with a sampling speed of 25 MHz at a near Nyquist frequency of 11.328125 MHz, and the ADC consumes a power of 8.212 mW. The 2-bit/cycle sub-radix V_{cm}-based SAR-assisted pipeline ADC was implemented in a 4-channel Time-Interleaved ADC. The post-layout SNDR, SFDR, and ENOB were attained as 50.04 dB, 54.78 dB, and 8.0198 bits, respectively with a sampling speed of 100 MHz at a near Nyquist frequency of 44.140625 MHz.

ÖZET

İYİLEŞTİRİLMİŞ ARTIK YÜKSELTEÇLİ 8-BIT 100 MS/S ZAMAN ARALIKLI SAR YARDIMLI BORU HATTI ADC

CERIN NINAN KUNNATHARAYIL

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Anahtar Kelimeler: Yüksek hızlı SAR mantığı, Artık Yükseltici, SAR Destekli Boru Hattı ADC, Eşzamanlı Anahtarlama Gürültüsü (SSN), Sıfır Geçiş Dedektörü (ZCD)

Ardışık bir yaklaşım kaydı (SAR) destekli boru hattı analogdan dijitale dönüştürücülerde (ADC), SAR ADC ve kalıntı yükseltici, ADC'nin hızını ve gücünü belirleyen iki bloktur. Bunlar arasında, kalıntı amplifikatörü güce en aç olanıdır. Geleneksel olarak, kalıntı yükseltici yüksek kazançlı bir op-amp kullanır, ancak CMOS teknolojisi ölçeklendikçe transistörün içsel kazancı azalır. Bu nedenle, kalıntı amplifikatörü, CMOS teknolojisinin ölçeğinin küçültülmesinden etkilenmediği için sıfır geçiş tabanlı devrelere (ZCBC'ler) dayalı olarak tasarlanmıştır. ZCBC tabanlı artık yükselticinin sınırlaması, düşük f_T'ye sahip teknoloji düğümleri için ortaya çıkan aşırı gerilimdir. Bu nedenle, artık yükselticide yeni bir aşım azaltma tekniği tanıtılmıştır. Farklı köşe durumları için aşım voltajı ve süresi simüle edildi. Yeni aşım azaltma tekniğinin uygulanmasından sonra aşım voltajının son aralığı ve süre sırasıyla 0,584 mV ila 1,59 mV ve 124 ps ila 423 ps arasında elde edildi. Aşım süresi ve voltaj aralıklarındaki yüzde azalma, aşım azaltma tekniğinin kullanılmadığı duruma göre sırasıyla %90.544 ila %98.012 ve %89.153 ila %97.67 aralığındadır. Yeni aşma azaltma tekniği, 2 bit/döngü alt tabanı V_{cm} tabanlı SAR destekli ardışık düzen ADC'de uygulandı. Yerleşim sonrası simülasyon sonuçları, yaklaşık 11.328125 MHz Nyquist frekansında 25 MHz örnekleme hızıyla sırasıyla 56.57 dB, 62.98 dB ve 9.1046 bitlik bir SNDR, bir SFDR ve bir ENOB gösterir ve ADC bir güç tüketir. 8.212 mW. 2 bit/döngü alt tabanı V_{cm}-tabanlı SAR destekli ardışık düzen ADC, 4 kanallı Zaman Ara Eklemeli ADC'de uygulandı. Yerleşim sonrası SNDR, SFDR ve ENOB sırasıyla 50.04 dB, 54.78 dB ve 8.0198 bit olarak, 100 MHz örnekleme hızında 44.140625 MHz'e yakın Nyquist frekansında elde edildi.

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Aileme...
To my Parents...

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3GPP: Third Generation Partnership Project
ADC : Analog-to-Digital Converter
CDAC : Capacitive Digital-to-Analog
CMOS : Complementary Metal-Oxide Semiconductor
CML : Current Mode Logic
DAC : Digital-to-Analog Converter
DNL : Differential Non-linearity
DSPs — Digital Signal Processors
DVB-H : Digital Video Broadcasting - Handheld
DVB-T : Digital Video Broadcasting - Terrestrial
ENOB : Effective Number Of Bits
FFT : Fast Fourier Transform
FoM_W : Walden Figure of Merit
FoM_S: Schreier Figure of Merit
IEEE: Institute of Electrical and Electronics Engineers
IL : Interleaving Spurs
IMT-2020: International Mobile Telecommunication - 2020
INL : Integral Non-linearity
ITU-R: International Telecommunication Union Radiocommunication Sector
LNA: Low-Noise Amplifier
LSB : Least Significant Bit
MIMO: Multiple-Input Multiple-Output
MOSFET : Metal–Oxide–Semiconductor Field-Effect transistor
mmWave: Millimeter Wave
MSB: Most Significant Bit
NR: New Radio
OEC^{TM} : Output Edge Control
OSR : Oversampling Ratio
PCB : Printed Circuit Board
PVT : Process Voltage Temperature

SAR : Successive Approximation Register
SFDR : Spurious Free Dynamic Range
SiGe : Silicon Germanium
SNDR : Signal to Noise and Distortion Ratio
SNR : Signal to Noise Ratio
SSN : Simultaneous-Switching Noise
THD : Total Harmonic Distortion
TI : Time Interleaved
V2V: Vehicle-to-Vehicle
VDL : Variable Delay Line
VML : Voltage Mode Logic
WD : window Detector
ZCBCs : Zero-Crossing-Based Circuits
ZCD : Zero-Crossing Detector

1. Introduction

1.1 Motivation

The 5G requirements specified by the International Mobile Telecommunication - 2020 (IMT-2020) issued by the International Telecommunication Union Radio communication Sector (ITU-R) demand a downlink peak data rate of 20 Gbit/s, an uplink peak data rate of 10 Gbit/s, and a latency of 1 ms (ITU (2021)). The Third Generation Partnership Project (3GPP) has specified two frequency ranges for 5G New Radio (NR), which are sub-6 GHz and 24-100 GHz. In the millimeter wave (mmWave) communication system (i.e. in between 30 and 300 GHz), the overall loss in the mmWave system is larger than the microwave frequency band for a point-to-point link. mmWave multiple-input multiple- output (MIMO) provides a means to solve the attenuation loss by using large antenna array as the size of the antenna is inversely proportional to the frequency. Due to the large antenna array, higher throughput can be achieved by the use of spatial multiplexing. Moreover, due to the large spectrum in the mmWave band, this gives rise to a tremendous increase in the data rate paving the way for applications like WiGig, V2V communication and so on.

Fig.1.1 shows the architecture of a MIMO receiver that contains multiple antennas. The received signal is passed through the LNA and then down-converted by the mixer and passed through a low pass filter and finally, to the ADC to be converted to a digital format for the DSPs. The motivation of the Ph.D. thesis is to design the ADC system that will be integrated along with the RF block to form a single monolithic IC to function as the MIMO receiver that will improve the signal integrity between the blocks and hence, improve the performance of the complete system. The ADC specification attained for the system can be understood by the following example. For instance, for a full duplex WiFi radio, the bandwidth allocated is 80

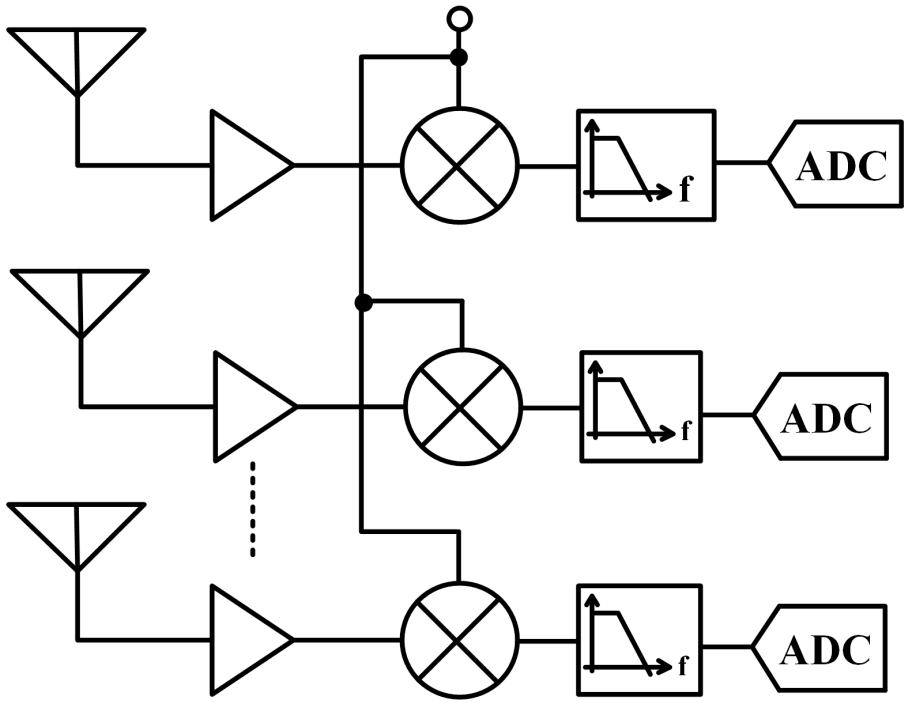


Figure 1.1 Block Diagram of a Digital MIMO Receiver

MHz. The transmit power is 20 dBm with the receiver noise figure to be 5 dB. The noise floor can be calculated as -174 + 10log(80 x 10^6) = -90 dBm. Hence, a 110 dB of overall self-interference cancellation is required to push it below the noise floor. If a 50 dB digital cancellation is considered then a 12-bit ($\approx$ 70 dB dynamic range) ADC can be used and the remaining 60 dB cancelled by the RF and antenna (Kalyoncu (2019)). By the use of a notch filter before the ADC (Golabighezelahmad, Klumperink & Nauta (2020); Kim, Joshi, Thomas, Ha, Larson & Cauwenberghs (2016); Moon, Kim, Kam, Jee, Choi & Lee (2019)), the dynamic range of the ADC can be reduced. Hence, the specification of the ADC is an 8-12 bit resolution ADC with a sampling rate of 100 MS/s is taken.

Data converters are divided into two categories: Oversampling converters and Nyquist-rate data converters. Nyquist-rate data converters operate for input signals close to the bandwidth of $f_s/2$, and mostly operate at a speed that is limited by the architecture and process. The most commonly used Nyquist-rate converters are the flash ADC, SAR ADC, and pipeline ADC. Oversampling ADCs are used for a limited bandwidth signal with a high sampling rate and are defined by the oversampling ratio (OSR). OSR is defined as the ratio between sampling frequency to the Nyquist frequency i.e. $f_s/2f_b$, where f_b is the highest input frequency, and f_s is the sampling frequency. The advantage of oversampling ADC is that it attains high resolution by using noise shaping techniques along with oversampling. The disadvantage of oversampling ADCs is that it requires a high-frequency clock and

also for the DSPs thereby increasing the hardware complexity and making it cost-in-efficient. Based on the specification of the ADC required for the MIMO system, a medium-high resolution, medium speed, and low power ADC are required. Among the different Nyquist-rate converters, SAR ADC has the advantage of low power but low speed, pipeline ADCs have high speed but low power, and flash ADC has high speed but power-inefficient. Hence, combining the advantage of SAR ADC and pipeline ADC, this thesis starts the ADC design with a SAR-assisted pipeline ADC.

1.2 Technical Challenges and Solutions

The intention of the thesis is to design an 8-12 bit ADC with a sampling speed of 100 MS/s for the monolithic MIMO receiver IC. To achieve low power, the MOSFETs of the technology are used. However, the MOSFETs have lower f_T compared to the HBT of the technology. Hence, the intention of the ADC design is to increase the speed. For a given technology node, the power of the ADC increases with the sampling frequency until a certain point, based on the technology node. After this point, the power increases at a much faster rate as the sampling frequency increases, and the normalized power efficiency (P/f_s) starts to degrade (Wei, Zhang, Datta Sahoo & Razavi (2013)). Hence, the single-channel ADC is designed until the point where the power and speed increase in a linear fashion. Then, time-interleaving will be used to increase the speed and keeps the transistor speed in the linear region of power and sampling speed.

1.3 Thesis Outline

The thesis intends to design an 8-12 bit resolution ADC with a speed of 100 MS/s with low power. Therefore, chapter 2 introduces SAR ADC and pipeline ADC. SAR ADC is used for its low power and pipeline ADC is used for its high speed. Combining the advantage of both of them gives the SAR-assisted pipeline architecture which is then explained in the chapter. Finally, the chapter concludes by illustrating the terms and parameters used to define the ADC.

Chapter 3 introduces a novel asynchronous SAR logic for the SAR ADC that was designed in the 8-metal CMOS process. The design was implemented by a former member of the group, and the analysis and measurements are done by the author of the thesis.

In chapter 4, the design of the single-channel V_{cm}-based SAR-Assisted pipeline ADC is explained and designed in the 130 nm BiCMOS process. The SAR ADC uses the novel asynchronous SAR logic explained in chapter 3. In this chapter a novel overshoot reduction technique is described for the residue amplifier designed based on the zero-crossing-based circuit (ZCBC). The post-layout results of the SAR-assisted pipeline ADC achieves an ENOB of 7.9344 bits and 6.6653 bits that corresponds to an SNDR of 49.53 dB and 41.89 dB with an input frequency of 520.83 kHz and at a near Nyquist rate of 7.5521 MHz, respectively with a sampling frequency of 16 MS/s. The INL and DNL were attained as -1.043/0.75 LSB and -0.86/1.13 LSB, respectively. The Walden Figure of Merit (FOM_W) at low frequency and at the Nyquist frequency was attained as 255 fJ/conversion-step and 615.77 fJ/conversion-step, respectively.

In chapter 4, the speed and resolution have not been met, hence, chapter 5 divides into two sections.

- Section 1: Section 1 describes the 2-bit/cycle SAR ADC and using the aforementioned architecture in the SAR ADC, a single-channel ADC is designed using a 2-bit/cycle sub-radix V_{cm}-based SAR-assisted pipeline. The post-layout results of the SAR-assisted pipeline ADC achieves an ENOB of 8.7109 bits and 8.6658 bits that corresponds to an SNDR of 54.2 dB and 53.93 dB with an input frequency of 1.3393 MHz and at a near Nyquist rate of 10.268 MHz, respectively with a sampling frequency of 28.571 MS/s. The INL and DNL were attained as +1.7067/-2.2149 LSB and +1.2867/-0.7459 LSB, respectively. The Walden Figure of Merit (FOM_W) at the Nyquist frequency was attained as 99.710 fJ/conversion-step.

- Section 2: This section improves the overshoot reduction technique and is implemented in the 2-bit/cycle sub-radix V_{cm}-based SAR-assisted pipeline. The post-layout results of the SAR-assisted pipeline ADC achieves an ENOB of 9.1216 bits and 9.1046 bits that corresponds to an SNDR of 56.67 dB and 56.57 dB with an input frequency of 1.171875 MHz and at a near Nyquist rate of 11.328125 MHz, respectively with a sampling frequency of 25 MS/s. The Walden Figure of Merit (FOM_W) at the Nyquist frequency was attained as 589.7 fJ/conversion-step.

In chapter 5, to improve the speed, the single-channel SAR-assisted pipelined ADC was time-interleaved. A 4-channel TI architecture is presented in this chapter. The post-layout specification of the SAR-assisted pipeline ADC achieves an ENOB of 8.2355 bits and 8.0198 bits that corresponds to an SNDR of 51.34 dB and 50.04 dB with an input frequency of 1.5625 MHz and at a near Nyquist rate of 44.140625 MHz, respectively with a sampling frequency of 100 MS/s. The Walden Figure of Merit (FOM_W) at the Nyquist frequency was attained as 2.4932 pJ/conversion-step.

Chapter 6 finally concludes the thesis with future works.

2. SAR-Assisted Pipeline ADC and Parameters to understand the ADC Performance

The most common Nyquist-rate date converters are the flash ADC, SAR ADC, and pipeline ADC. Flash ADC has high speed, however, it is less power efficient. In the case of SAR ADC, it is power-efficient but has slow speed, and pipeline ADC has high speed but is power hungry. Since, the ADC requirement is low power with a resolution of 8-12 with a sampling speed of 100 MS/s, the design of the ADC is based on a SAR-assisted pipeline ADC. This architecture uses the advantage of low power from SAR ADC and high speed from pipeline ADC. Hence, this chapter introduces the SAR ADC and then the pipeline ADC followed by which the SAR-assisted pipeline ADC is discussed. Finally, the parameters used to define the ADC are explained.

2.1 SAR-Assisted Pipeline ADC

2.1.1 SAR ADC

Successive-approximation register (SAR) ADC became a popular choice for the design of ADCs because of its capability to scale with technology and its low power. Fig. 2.1(a) and (b) shows the block diagram and working of a 3-bit SAR ADC, respectively. SAR ADC works on the principle of the binary search algorithm. The operation begins with the analog input sampled by the S&H. Consider an input voltage of $5.5V_{ref}/8$, where V_{ref} is the reference voltage of the DAC as shown in Fig. 2.1(a). The 3-bit register initializes the MSB bit to 1 and the remaining bits to 0. The DAC output will correspond to $V_{ref}/2$. Since, $5.5V_{ref}/8$ (V_{in}) > $V_{ref}/2$ then

the comparator output is set to logic 1. Then the next bit (MSB-1) is set to logic 1. The DAC output will correspond to ($V_{ref}/2 + V_{ref}/4$) = $6V_{ref}/8$. Then, $6V_{ref}/8$ is compared with V_{in}. Since, $V_{in} < 6V_{ref}/8$, therefore, (MSB-1) bit is set to 0 and then (MSB-2) bit is set to 1. The DAC output will corresponds to ($V_{ref}/2 + V_{ref}/8$) = $5V_{ref}/8$. Since, $V_{in} > 5V_{ref}/8$, therefore, (MSB-2) bit is set to 1. Therefore, the digital word corresponding to the input voltage of $5.5V_{ref}/8$ is 101.

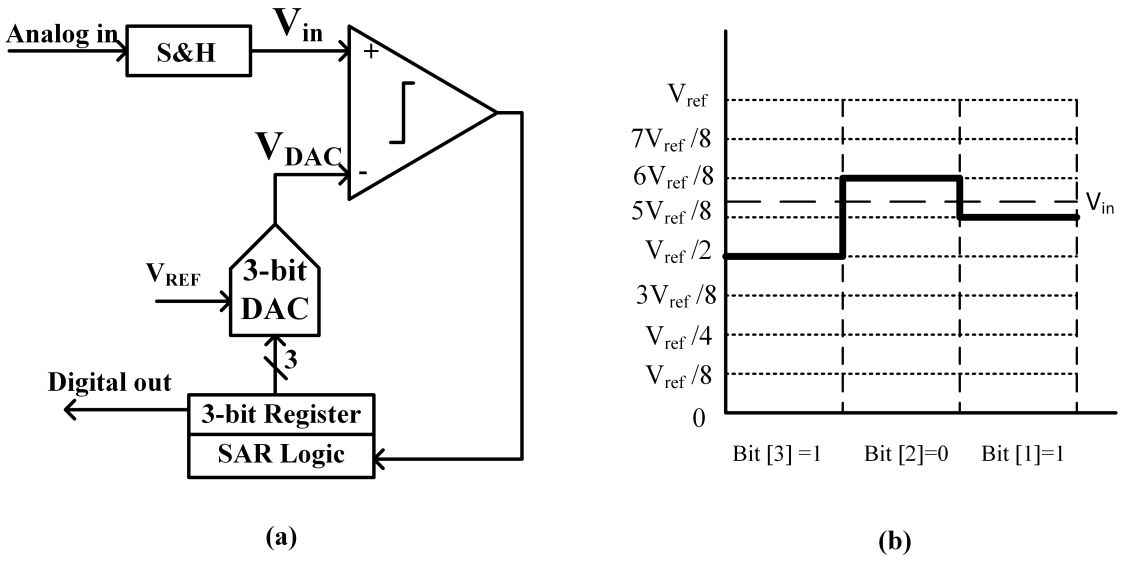


Figure 2.1 3-bit SAR ADC (a) Block Diagram (b) Working

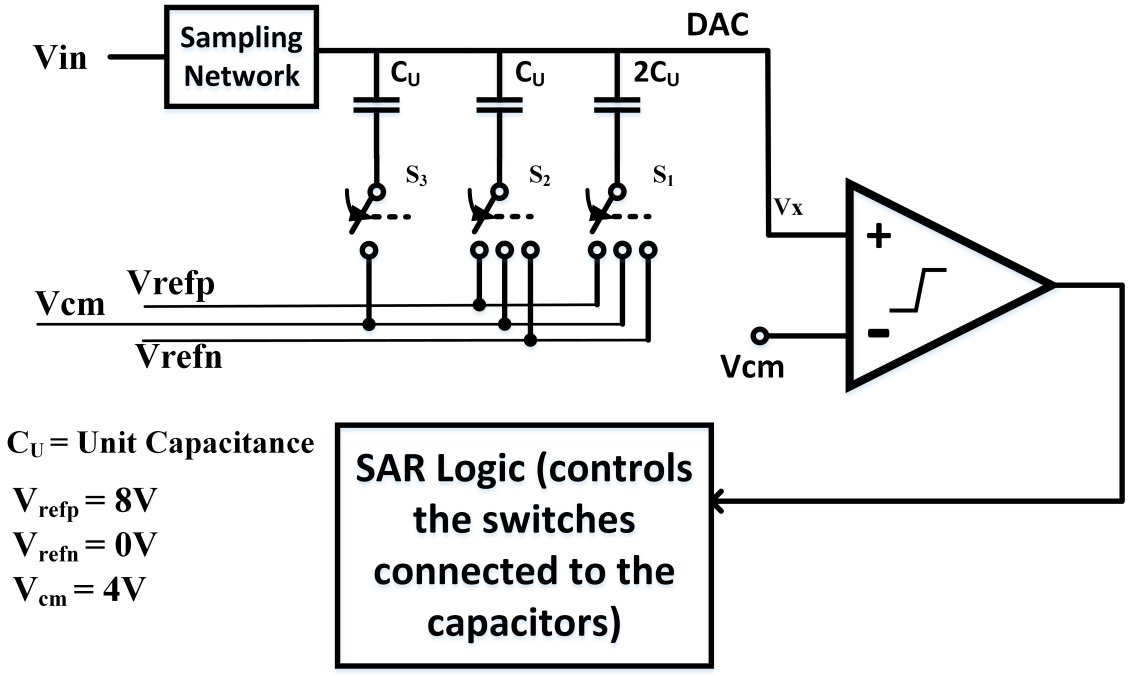


Figure 2.2 3-bit Vcm-based SAR ADC

With the understanding of the binary search algorithm, the working of Vcm-based differential SAR ADC is explained in Fig. 2.2. Considering the same example as in

Fig.2.1. The V_{in} is taken as $5.5V_{ref}/8$. Let V_{ref} be 8V, then V_{refp} = 8V, V_{refn} = 0V and V_{cm} = 4V. Therefore, the V_{in} = 5.5V. The working of the SAR ADC starts when the sampling network samples V_{in} on the top plate of the capacitors and all the bottom plates of the capacitors are connected to V_{cm}. Therefore, the charge stored in the capacitor is given by (2.1).

$$Q_{\text{in}} = (V_{\text{in}} - V_{\text{cm}})4C_{\text{u}} \tag{2.1}$$

Then, V_{in} is disconnected and the top-plates of the capacitors are kept floating. The charge in the capacitors is given by (2.2).

$$Q_1 = (V_{\text{x}} - V_{\text{cm}})4C_{\text{u}} \tag{2.2}$$

By charge conservation rule equation (2.1) and (2.2) are equal.

$$\begin{aligned}(V_{\text{in}} - V_{\text{cm}})4C_{\text{u}} &= (V_{\text{x}} - V_{\text{cm}})4C_{\text{u}} \\ V_{\text{in}} &= V_{\text{x}} = 5.5V\end{aligned} \tag{2.3}$$

Since, V_x (5.5 V) > V_{cm} (4V). Therefore, the comparator is set to logic 1 i.e. the MSB bit is 1. Since, comparator is set to logic 1, the S_1 is connected to V_{refn} (0V) and the remaining switches are still connected to V_{cm}. Now, the charge in capacitors is given by equation (2.4).

$$Q_2 = (V_{\text{x}} - V_{\text{cm}})2C_{\text{u}} + (V_{\text{x}} - V_{\text{refn}})2C_{\text{u}} \tag{2.4}$$

By charge conservation rule, equation (2.2) and (2.4) are equal.

$$\begin{aligned}(V_{\text{in}} - V_{\text{cm}})4C_{\text{u}} &= (V_{\text{x}} - V_{\text{cm}})2C_{\text{u}} + (V_{\text{x}} - V_{\text{refn}})2C_{\text{u}} \\ V_{\text{x}} &= 3.5V\end{aligned} \tag{2.5}$$

Since, V_x (3.5 V) < V_{cm} (4V). Therefore, the comparator is set to logic 0 i.e. the (MSB-1) bit is 0. Since, comparator is set to logic 0, the S_2 is connected to V_{refp} (8V) and the S_3 is still connected to V_{cm}. Now, the charge in capacitors is given by equation (2.6).

$$Q_3 = (V_{\mathrm{x}} - V_{\mathrm{cm}})C_{\mathrm{u}} + (V_{\mathrm{x}} - V_{\mathrm{refn}})2C_{\mathrm{u}} + (V_{\mathrm{x}} - V_{\mathrm{refp}})C_{\mathrm{u}} \tag{2.6}$$

Again by charge conservation rule, equation (2.4) and (2.6) are equal.

$$\begin{aligned}(3.5 - V_{\mathrm{cm}})2C_{\mathrm{u}} + (3.5 - V_{\mathrm{refn}})2C_{\mathrm{u}} = (V_{\mathrm{x}} - V_{\mathrm{cm}})C_{\mathrm{u}} + \\ (V_{\mathrm{x}} - V_{\mathrm{refn}})2C_{\mathrm{u}} + (V_{\mathrm{x}} - V_{\mathrm{refp}})C_{\mathrm{u}} \\ V_{\mathrm{x}} = 4.5V\end{aligned} \tag{2.7}$$

Since, V_x (4.5 V) > V_{cm} (4V). Therefore, the comparator is set to logic 1 i.e. the (MSB-2) bit is 1. Therefore, the digital word corresponding to the input voltage of 5.5V is 101.

2.1.2 Pipeline ADC

Pipeline architecture has the advantage of increasing the speed of the ADC. Fig. 2.3(a) illustrates the architecture of a 2-stage pipeline ADC. The sampled voltage is passed to a 3b ADC and then to a 3b DAC. The output of the 3b DAC is subtracted from the sampled voltage. The residue voltage is then amplified and then passed as input to the second stage of the pipeline ADC. Fig. 2.3(b) illustrates an example of the 2-stage pipeline ADC and shows the minimum and maximum input range is 0V and 8V, respectively. Let 6.3V be the sampled voltage by the sample and hold circuit in the first stage. Since each stage consists of 3b. Therefore, the LSB is 1V.

Since, 1 LSB = 1V, therefore, to amplify 1V for an input range of 0-8V for the 2nd stage, the gain of the amplifier must be 2^3 =8. When 6.3V is the input to the first stage, the digital output of the first stage (D[5:3]) is 110. The residue voltage for the first stage is defined as the difference between the analog input and digital value. The residual voltage attained is 0.3 and is amplified by 8 and becomes the analog input for the second stage of the pipeline ADC. The resultant analog voltage for the second stage is 2.4 V. For an input voltage of 2.4, the digital value corresponds to 010. Hence the digital word corresponding to an input of 6.3 V is 110010.

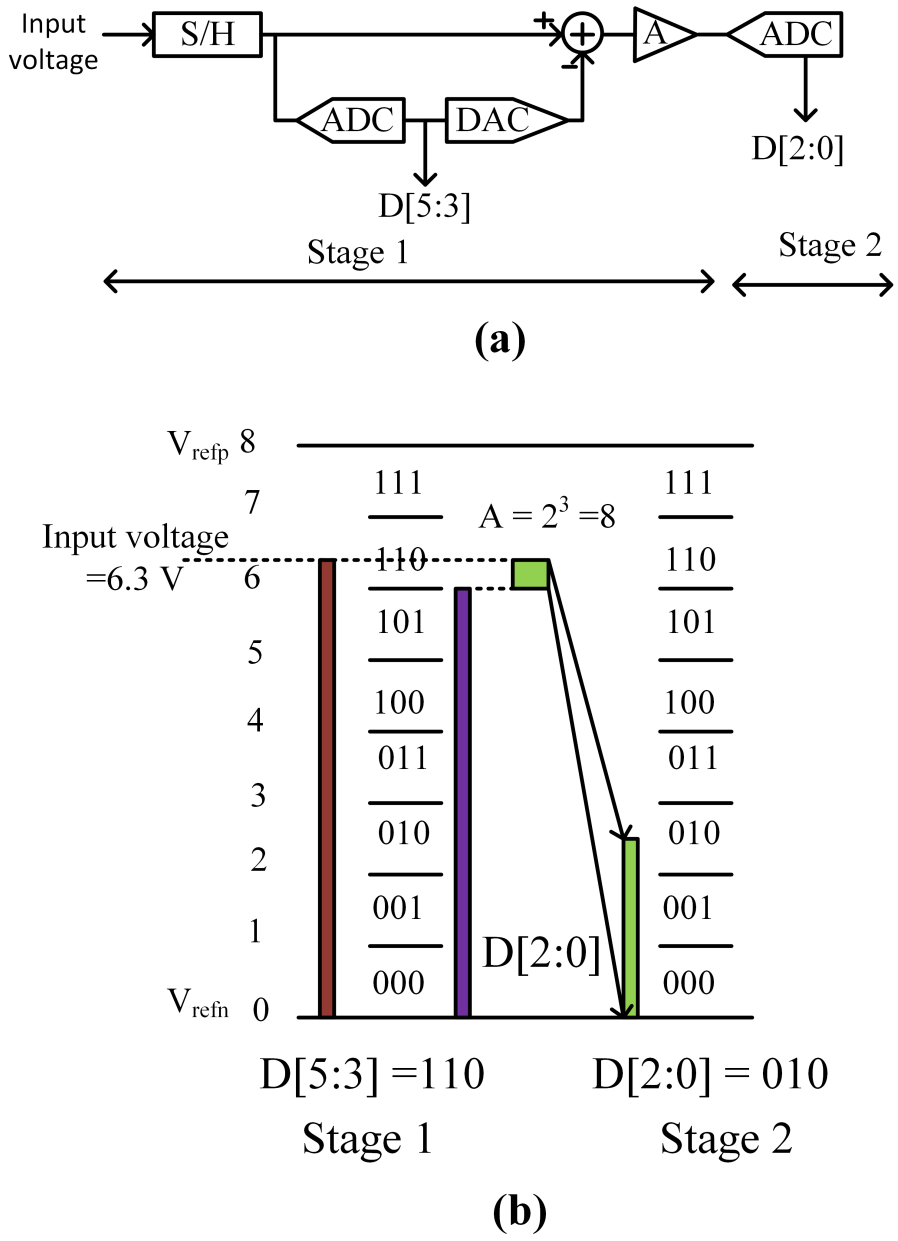


Figure 2.3 (a)Architecture (b) Example of a 2-stage Pipeline ADC

2.1.3 SAR-Assisted Pipeline ADC Architecture

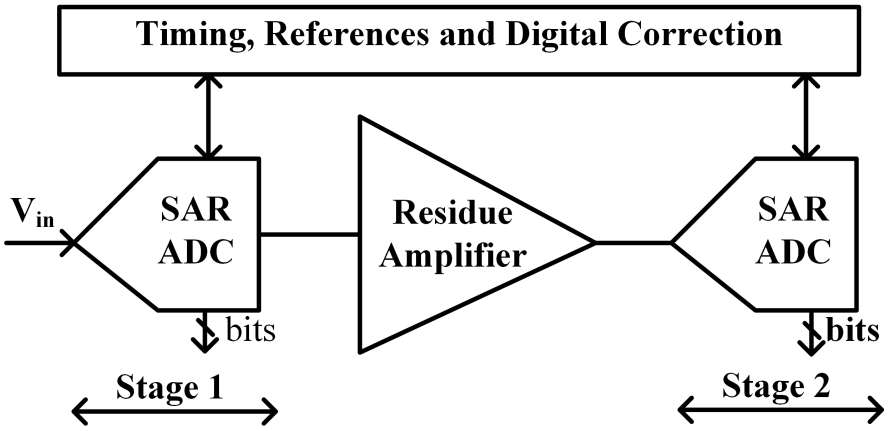


Figure 2.4 Block diagram of a Two-stage SAR-Assisted Pipeline ADC

Fig. 2.4 shows the block diagram of a two-stage SAR-assisted pipeline ADC. This architecture combines the advantage of low power from SAR ADC and speed from pipeline ADC.

2.2 Parameters to understand the ADC Performance

2.2.1 Terms

- Full-Scale Range (FSR): It is defined as the difference between the positive reference input (V_{ref+}) and the negative reference input (V_{ref-}). It can also be defined as the difference between the maximum and minimum input voltage applied to the ADC and is expressed as (2.8).

$$\mathrm{FSR} = V_{ref+} - V_{ref-} \tag{2.8}$$

- Resolution (N): It is defined as the number of bits an ADC can convert an analog signal.
- Least Significant bit (LSB): It is as the ratio between FSR and 2^N, and is expressed as (2.9).

$$\text{LSB} = \frac{V_{\text{ref+}} - V_{\text{ref-}}}{2^{\text{N}}} \tag{2.9}$$

- Static test: A static test is defined when a slowly varying signal like is ramp signal is applied to the ADC under test. The output results are similar to the results attained when a constant input is given to the ADC under test.
- Dynamic test: Dynamic test is performed to understand the dynamic errors in an ADC. The input given to the ADC is normally a sine waveform.

2.2.2 Dynamic Characteristics

- Signal-to-Noise and Distortion Ratio: Signal-to-Noise and Distortion Ratio (SNDR) is the fundamental frequency signal power level (P_s) to the noise plus distortion power level ($\text{P}_{\text{N+D}}$) ratio and is expressed as (2.10) in terms of dB. SNDR is usually expressed in terms of dB, V_{rms}, or %.

$$\text{SNDR} = 10log\frac{Ps}{P_{\text{N+D}}} \tag{2.10}$$

- Effective Number of Bits: The effective number of bits (ENOB) is the number of bits when both noise and distortion are considered. It is expressed as (2.11).

$$\text{ENOB} = 10log\frac{SNDR - 1.76}{6.02} \tag{2.11}$$

- Total Harmonic Distortion (THD): Total Harmonic Distortion (THD) gives information regarding the total amount of harmonic energy in the FFT plot for a given input frequency, and is expressed as (2.12). The range of the FFT plot is until the Nyquist frequency. It is usually expressed in terms of dB or %.

$$\text{THD} = \frac{\text{Summation of harmonic energy}}{\text{Fundamental Input Energy}} \tag{2.12}$$

- Signal-to-Noise Ratio (SNR): Signal-to-Noise Ratio (SNR) is defined as the ratio of the fundamental input energy to the noise energy in the spectrum excluding the harmonic energy and the fundamental energy for the given input

signal, and is expressed as (2.13). The spectrum is defined until the Nyquist frequency. In practice, only the first five harmonics are excluded as they are dominant. It is usually expressed in term of dB, V_{rms}, or %.

$$\text{SNR} = \frac{\text{Fundamental Input Energy}}{\text{Summation of noise energy}} \tag{2.13}$$

- Spurious Free Dynamic Range (SFDR): It is defined as the ratio of the signal in terms of rms to the rms value of the worst spurious signal in the frequency spectrum. It is usually expressed in dB, and is expressed in dB as (2.14).

$$\text{SFDR} = \text{Fundamental Input Energy} - \text{Max(all frequency except fundamental)} \tag{2.14}$$

2.2.3 Static Characteristics

- Ideal Transfer Function: A transfer function is a plot between the normalized analog input voltage with respect to the FSR and the digital code from the ADC. Fig. 2.5 illustrates a $+\frac{1}{2}$ LSB compensated ideal transfer function of a 3-bit ADC. In this transfer function, the first code (000) is only $+\frac{1}{2}$ LSB wide and the last code (111) is $1\frac{1}{2}$ LSB wide. The y-axis represents the digital code, and the x-axis represents the normalized analog input voltage with respect to the FSR.

- Offset Error: It is defined as the difference between the ideal offset point (0.5 LSB) and the actual offset point measured in LSB. An offset can be positive or negative. Fig. 2.6 shows the positive and negative offset. The offset voltage is converted to Volts as (2.15).

$$\text{Offset Voltage (V)} = \text{Error in LSB}(\frac{\text{Max Input}}{2^N}) \tag{2.15}$$

- Gain Error: The gain error is done after the offset error is calibrated. Gain error is defined as the difference between the midpoint of the last step of the ideal transfer function and the actual transfer function. Gain error is calibrated by scaling the output. Fig. 2.7 shows the positive and negative gain error.

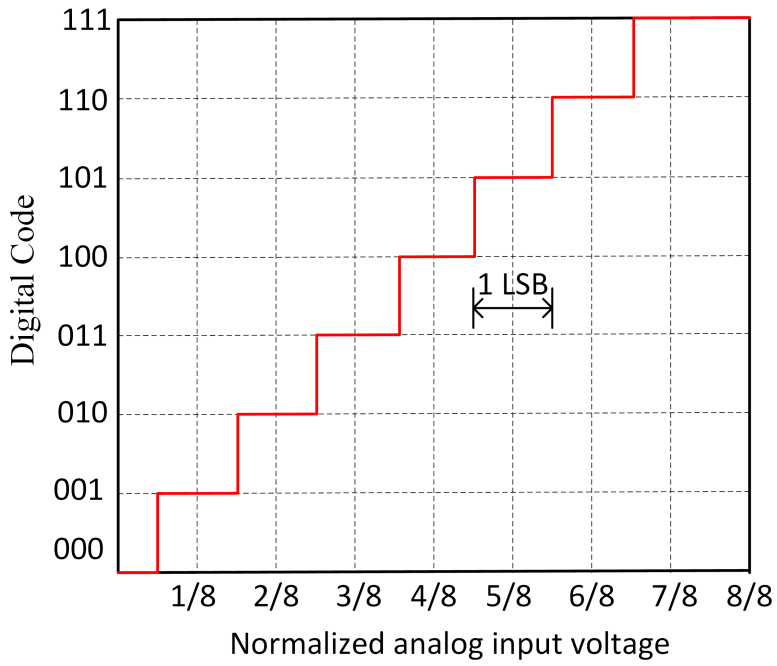


Figure 2.5 Compensated Ideal Transfer Function

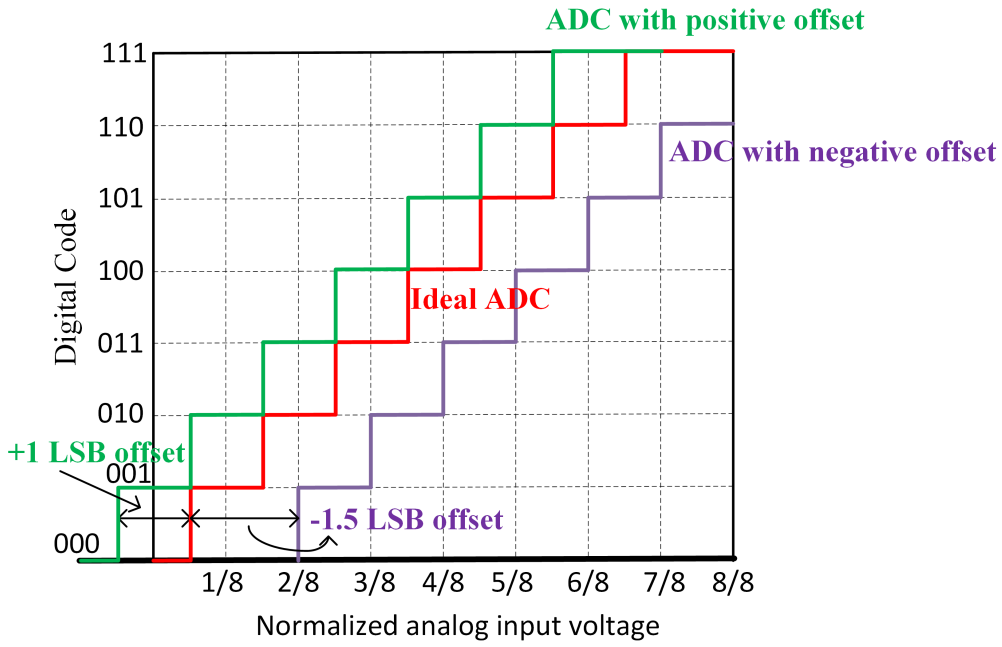


Figure 2.6 Positive and Negative Offset error

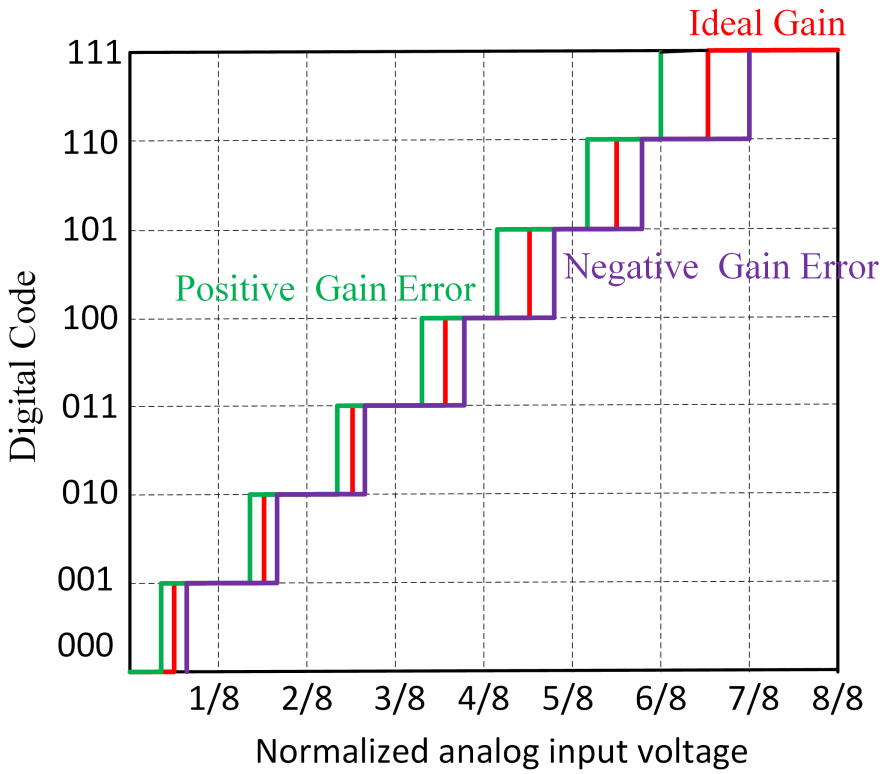


Figure 2.7 Positive and Negative Gain error

- Differential Non-Linearity (DNL): It is defined as the deviation of the actual code width from the ideal code width (1 LSB). Fig. 2.8 represents the DNL error in the ADC. As observed in code 001, the actual code width is $1\frac{1}{2}$ LSB wide. This is $+\frac{1}{2}$ LSB greater than the ideal code width (1 LSB).

  It can be observed that the lowest code width can be 0, which corresponds to a DNL of -1 LSB and the maximum code width can be greater than 2, which corresponds to a DNL of >+1 LSB. The two mentioned cases correspond to missing codes in an ADC. Hence, for an ideal ADC without any missing digital must have a DNL between -1 LSB and +1 LSB.

- Integral Non-Linearity (INL): INL is the deviation of the actual transfer characteristics from the ideal transfer characteristics. Fig. 2.9 represents the INL error in the ADC. As observed in the 001 code, the deviation of the actual transfer function from ideal transfer function is $+\frac{1}{2}$ LSB. Moreover, the shape of the INL give an idea of the harmonic present in the ADC. If the shape of the INL is quadratic, it means that even order harmonics are present, and if the shape is cubic, the presents of odd harmonics can be detected. A thumb rule between INL and SFDR is expressed as (2.16).

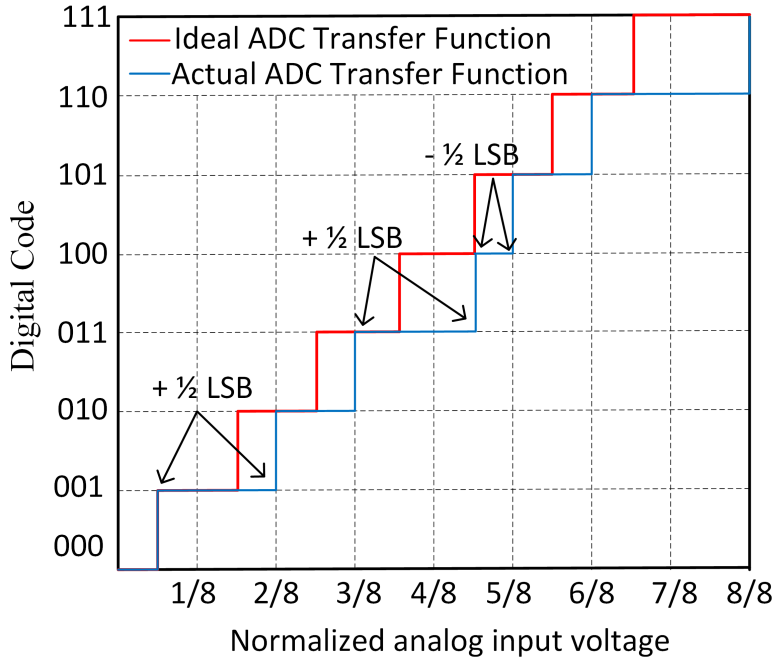


Figure 2.8 ADC Transfer Function with DNL Error

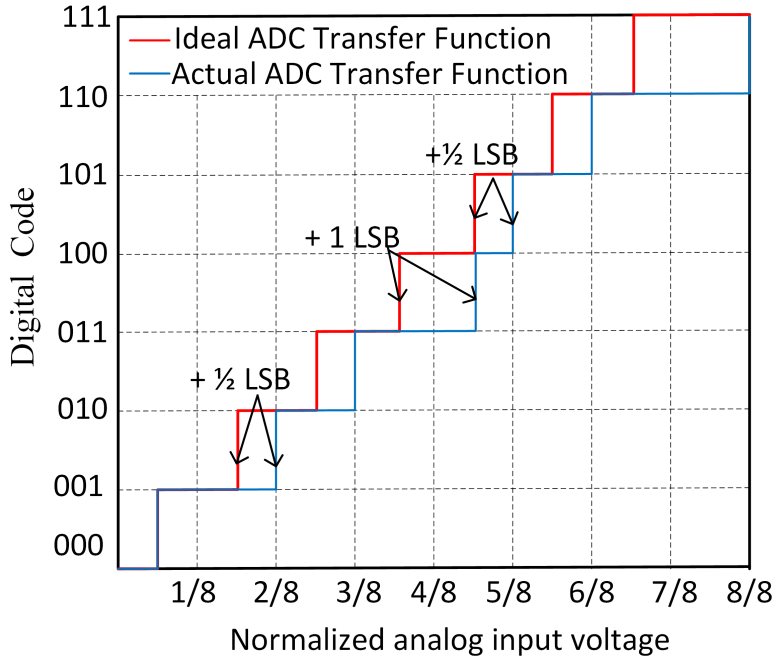


Figure 2.9 ADC Transfer Function with INL Error

$$\text{SFDR} \approx 20log(\frac{2^{\text{B}}}{\text{INL}}) \tag{2.16}$$

2.2.4 Figure-of-merit (FoM)

The figure-of-merit (FoM) is used to assess the power efficiency of the ADC. The two widely used FoMs in literature are Walden FoM and Schreier FoM.

- The Walden FoM (FoM_{W}) is defined as the energy used per conversion step in an ADC and is given by the equation (2.17).

$$\text{FoM}_{\text{W}} = \frac{P_{\text{ADC}}}{2^{ENOB} * f_{\text{s}}} \qquad [J/Conversion - steps] \tag{2.17}$$

  where P_{ADC} is the power consumed by the ADC and f_{s} is the frequency at which the ADC is sampled.

- The Schreier FoM (FoM_{S}) is denoted in terms of decibels and is calculated from SNDR, power consumed by the ADC, and sampling frequency. FoM_{S} is expressed as (2.18).

$$\text{FoM}_{\text{S}} = SNDR + 10log\frac{f_{\text{s}}/2}{P_{\text{ADC}}} \tag{2.18}$$

3. Proposed Asynchronous SAR logic

Successive Approximation Register (SAR) Analog-to-Digital Converters (ADC) have become a common choice in conjunction with high-speed ADCs because of their low-power and digital-friendly architecture. However, as the resolution of the SAR ADC increases, the number of conversion cycles increases which reduces the speed of the SAR ADC. Fig. 3.1 shows the block diagram of an N-bit SAR ADC. As shown in Fig. 3.1, a SAR ADC comprises three blocks: the digital-to-analog converter (DAC), the comparator, and the SAR logic. Many architectures have been proposed to solve issues arising from the DAC and the comparator (Chan, Zhu, Sin, Murmann, Seng-Pan & Martins (2017); Roh (2020)), but a few architectures focus on the SAR logic. From articles (Hong, Kim, Kang, Park, Choi, Park & Ryu (2015); Kunnatharayil, Abbasi, Ceylan, Arslan, Zirtiloglu & Gurbuz (2020); Shah & Sahoo (2017)), it can be observed that for technology nodes $\geq$ 65 nm, the SAR logic propagation delay is dominant. However, for technology nodes $\leq$ 45 nm, the SAR logic delay is not dominant. However, while increasing the speed of the SAR logic, simultaneous-switching noise (SSN) increases due to a large number of digital switches switching at the same time.

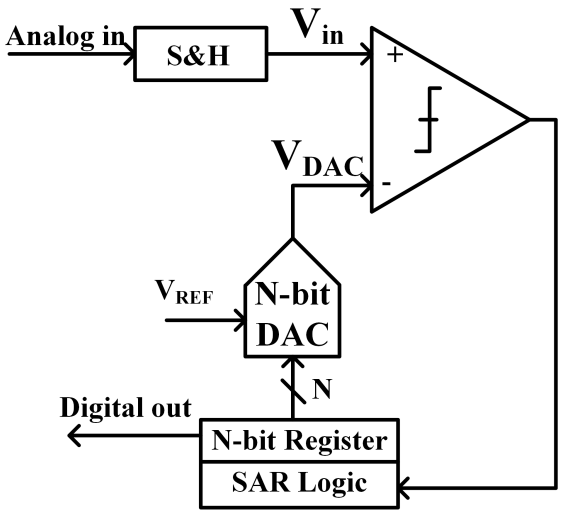


Figure 3.1 Block diagram of a N-bit SAR ADC

Substrate noise becomes an issue with feature size $\leq$ 250 nm (Wang, Murgai & Roychowdhury (2004)). Substrate noise is generated due to three mechanisms (Briaire & Krisch (2000)): 1) capacitive coupling of the source/drain and the substrate when reversed biased, 2) impact ionization, and 3) noise generated in the ground and power lines mainly due to Ldi/dt arising from the wire bond and package inductance. Among the three mechanisms, the noise generated in the power/ground line is the dominant compared to the impact ionization and the capacitive coupling from the source/drain and substrate (Badaroglu, Wambacq, Van der Plas, Donnay, Gielen & De Man (2006)). Many solutions are proposed to reduce the noise in the power/ground line like improving the packaging techniques that reduce the inductance (Diaz-Olavarrieta (1991)), increasing the number of ground/power pins to reduce the inductance, separating the analog and digital power lines. A better solution would be designing the circuit that reduces the SSN of the digital blocks which thereby reduces the noise in the power/ground line.

This chapter investigates a proposed asynchronous SAR logic with improved speed and better simultaneous-switching noise (SSN) compared to the conventional SAR logic. The proposed asynchronous SAR logic was designed by a former member of the group, and the measurement and analysis is done by the author of the thesis. Initially, Section I introduces the conventional SAR logic and the proposed asynchronous SAR logic based on handshake architecture. This section also compares the speed of the conventional and proposed SAR logic, and shows mathematically that the proposed SAR logic is faster than the conventional. The Section II introduces SSN and compares it with the conventional and proposed SAR logic, and proves mathematically that the proposed SAR logic has lower SSN compared to conventional SAR logic. Finally, Section III shows the measurement results of the 6-bit SAR ADC. This section also shows the simulation results comparing the speed of conventional and proposed SAR logic. Moreover, the SSN is simulated for the conventional, and proposed SAR logic and their performance was compared in terms of ENOB.

3.1.1 Conventional SAR Logic

A conventional SAR logic consists of a serial to parallel shift register (L_N - L_0) which activates the flip-flop from U_N to U_0, as shown in Fig. 3.2(a), based on the outputs of the shift register. Fig. 3.2(b) shows the timing diagram of the conventional SAR logic. The SAR logic is activated when one of the outputs of the comparator (COMP_P or COMP_N) is activated. For instance, COMP_P is activated by setting it to '0', as shown in Fig. 3.2(b). This activates Q_SR and COMP_DONE signals to '0' and '1', respectively. Hence, S_N is asserted to '1', and this activates D flip-flop U_N.

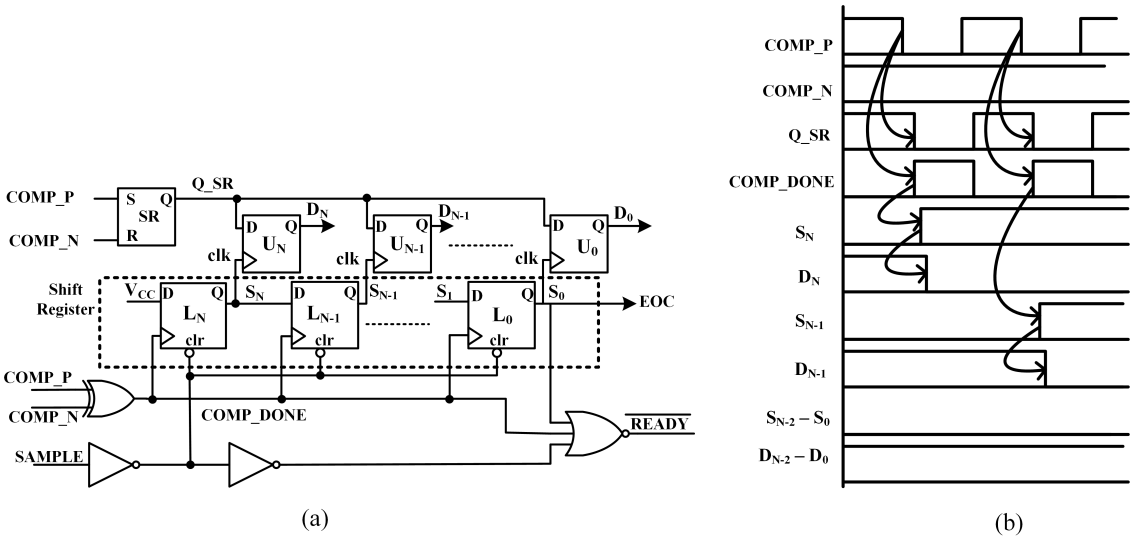


Figure 3.2 (a) Block diagram (Sadollahi et al. (2018)) and (b) Timing diagram of a conventional synchronous SAR Logic

With the knowledge of the working of the conventional synchronous SAR logic, the propagation delay of the SAR logic (T_{delay}) can be analyzed when the interconnect delay is ignored. T_{prop_D} is defined as the propagation delay from the output of the comparator connected to the SR latch to the input D of the D flip-flops (U_N-U_0), and is expressed as in 3.1. T_{prop_clk} is the propagation delay from the output of the comparator connected to the XOR gate to the input clk of the D flip-flops (U_N-U_0), and is expressed as in 3.2. T_{SR} defines the propagation delay of the SR latch, T_{XOR} is the propagation delay of the XOR gate, T_{SU,DFF_L} and T_{DFF_L} are the setup

time and clk-to-q delay of the D flip-flop (L_N), respectively. Based on 3.1 and 3.2, the critical path ($T_{critical}$) is defined by T_{prop_clk}. Hence, T_{delay} is the sum of the critical time ($T_{critical}$), the setup time and the clk-to-q delay of the D flip-flop (U_N), and is expressed as in 3.4.

$$T_{prop\_D} = T_{SR} \tag{3.1}$$

$$T_{prop\_clk} = T_{XOR} + T_{SU,DFF\_L} + T_{DFF\_L} \tag{3.2}$$

$$T_{critical} = max(T_{prop\_D}, T_{prop\_clk}) = T_{prop\_clk} \tag{3.3}$$

$$T_{delay} = T_{critical} + T_{SU,DFF\_U} + T_{DFF\_U} \tag{3.4}$$

However, the interconnect delay also contributes to the propagation delay of the SAR logic. The interconnect delay from the Q_SR and COMP_DONE will be dominant compared to the other interconnects because these signals are connected to 'n' D flip-flops, where 'n' is the number of conversions in a SAR ADC. If $T_{max\_Q\_SR}$ and $T_{max\_COMP\_DONE}$ are the maximum interconnect delay from signals Q_SR and COMP_DONE, respectively, then the maximum propagation of T_{prop_D} and T_{prop_clk} are expressed as 3.5 and 3.6, respectively.

$$T_{prop\_D\_max} = T_{SR} + T_{max\_Q\_SR} \tag{3.5}$$

$$T_{prop\_clk\_max} = T_{XOR} + T_{SU,DFF\_L} + T_{DFF\_L} + T_{max\_COMP\_DONE} \tag{3.6}$$

Hence, the maximum critical delay ($T_{critical\_max}$) is defined by $T_{prop\_clk\_max}$, and the maximum propagation delay (T_{delay_max}) is defined as 3.8.

$$T_{critical\_max} = T_{prop\_clk\_max} \tag{3.7}$$

$$T_{delay\_max} = T_{critical\_max} + T_{SU,DFF\_U} + T_{DFF\_U} \tag{3.8}$$

3.1.2 Proposed Asynchronous SAR Logic

The proposed asynchronous SAR logic (Kunnatharayil et al. (2020)) is designed based on a handshake architecture and implemented in a 6-bit V_{cm} based SAR

ADC, as shown in Fig. 3.3. The SAR ADC comprises a capacitive digital-to-analog (CDAC) converter, a comparator based on StrongArm latch, and an asynchronous SAR logic.

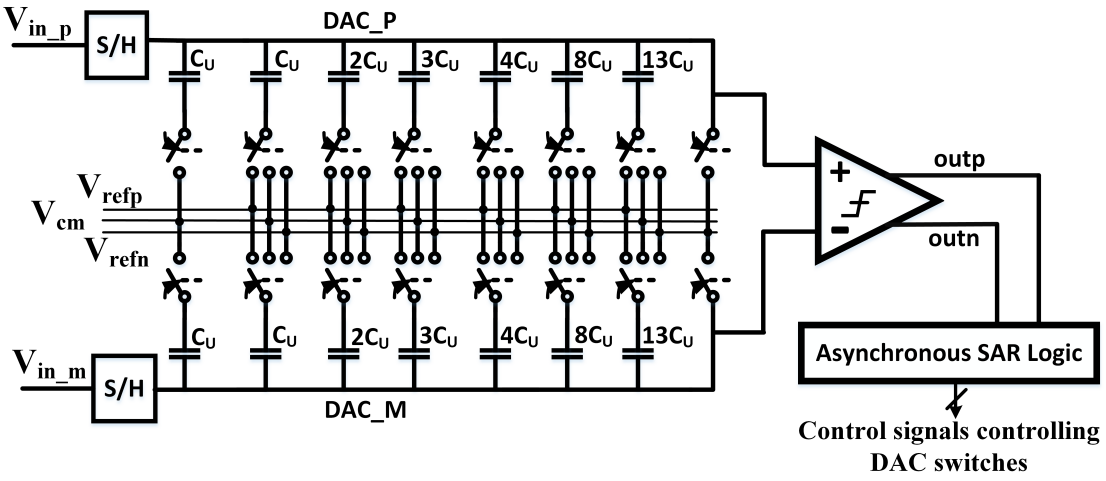


Figure 3.3 Schematic of a 6-bit V_{cm}-based SAR ADC

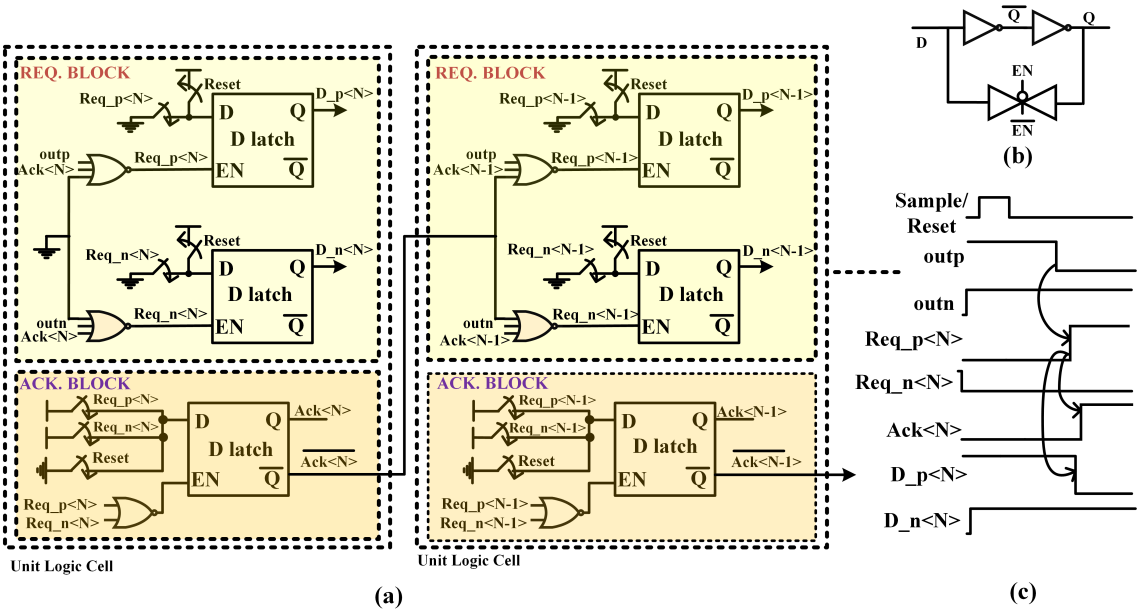


Figure 3.4 (a) Block diagram and (b) Timing diagram of the proposed asynchronous SAR logic (c) Schematic of latch

Fig. 3.4(a) and Fig. 3.4(c) show the block diagram and timing diagram of the proposed asynchronous SAR logic based on handshake protocol, respectively, and Fig. 3.4(b) shows the schematic of the positive level-sensitive D latch. The asynchronous SAR logic based on the handshake protocol comprises two blocks: a Request block and an Acknowledgement block. The Request block sends a Req signal to the Acknowledgement block which respond using an Ack signal. Once, the Ack signal is received, the unit logic cell, which comprises of Request block and Acknowledgement

block, stores the controls for the switches to the differential CDAC and activates the next unit logic cell.

The working of the SAR logic commences with the output of the comparator (outp and outn). Based on the decision of the comparator, one of its outputs will be activated. For instance, outp is activated by asserting to '0' as shown in Fig. 3.4(a) and then, Req_p<N> is set to '1'. This activates the Ack<N> signal and stores the control signals to the differential CDAC (D_p<N> and D_n<N>) in the D latches of the Request block and then, activates the next unit logic cell using $\overline{Ack<N>}$.

The propagation delay ($T_{delay,p}$) for the proposed SAR logic architecture is expressed as (3.11) when the interconnect delay is ignored, where $T_{delay,sw}$ is the propagation delay from the comparator outputs connected to the NOR gates of the Request block to D_p<N>/D_n<N> (to activate the switches of the CDAC), and $T_{delay,next\ blocks}$ is the propagation delay from the comparator outputs connected to the NOR gate of the Request block to $\overline{Ack<N>}$ (activates the next unit logic cell). $T_{NOR,Req}$ and $T_{NOR,Ack}$ are the propagation delay from the NOR gate of the Request and Acknowledgment block, respectively. $T_{D\ latch,Req}$ and $T_{D\ latch,Ack}$ are the propagation delay of the D latch of the Request and Acknowledgment block, respectively.

$$T_{delay,sw} = T_{NOR,Req} + T_{D\ latch,Req} \tag{3.9}$$

$$T_{delay,next\ blocks} = T_{NOR,Req} + T_{NOR,Ack} + T_{D\ latch,Ack} \tag{3.10}$$

$$T_{delay,p} = max(T_{delay,sw}, T_{delay,next\ blocks}) \tag{3.11}$$

When the interconnect delay is considered, the interconnect of the output of the comparator will dominate all other interconnects. If the max interconnect delay of the output of the comparator (outp/outn) is T_{max_out}, then the maximum propagation delay of the proposed SAR logic is expressed as (3.12).

$$T_{delay,p,max} = max(T_{delay,sw}, T_{delay,next\ blocks}) + T_{max\_out} \tag{3.12}$$

On comparing 3.8 and 3.12, it is evident that the propagation delay for the proposed SAR logic architecture is less compared to the conventional architecture because the critical path of the conventional SAR logic contains two D flip-flops and a logic gate, whereas the proposed SAR logic has a latch and two logic gates in its critical path.

3.2 Simultaneous-Switching Noise (SSN)

In high-speed, high-density integrated circuits (ICs) simultaneous-switching noise (SSN) has become of great concern. This is due to the fact that when many output drivers switch at the same time, a large current is drawn from the power supply which creates a power/ground noise called simultaneous-switching noise (SSN). The two noise parameters that define SSN are ground bounce and V_{cc} bounce. When the ground potential shifts to a non-zero value due to the simultaneous switching, it is called the ground bounce. Similarly, when the supply voltage changes from its reference value, it is called V_{cc} bounce. A ground bounce occurs when the I/O pins switch from 1 to 0, while V_{cc} bounce occurs mainly when the I/O pins switch from 0 to 1.

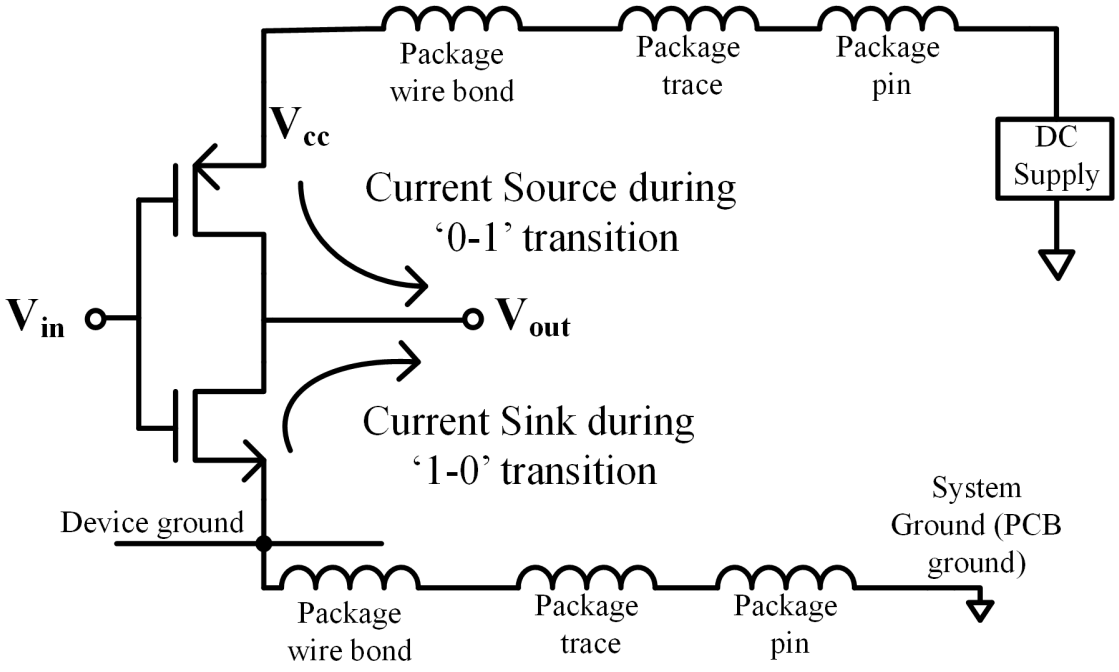


Figure 3.5 An Inverter switching with Parasitic Inductance

Let us consider the circuit in Fig. 3.5, where the inverter undergoes switching. As shown in Fig. 3.5, the device ground is connected to the system ground (PCB ground) through a series of inductance. The inductance arises from the wire bond of the package, the package trace, and then from the package pin. Hence, the effective inductance (L_{eff}) is expressed as (3.13).

$$L_{\text{eff}} = L_{\text{wire bond}} + L_{\text{trace}} + L_{\text{pin}} \tag{3.13}$$

where, $L_{\text{wire bond}}$, L_{trace}, L_{pin} are the inductance arising from the wire bond of the package, package trace, and package pin, respectively.

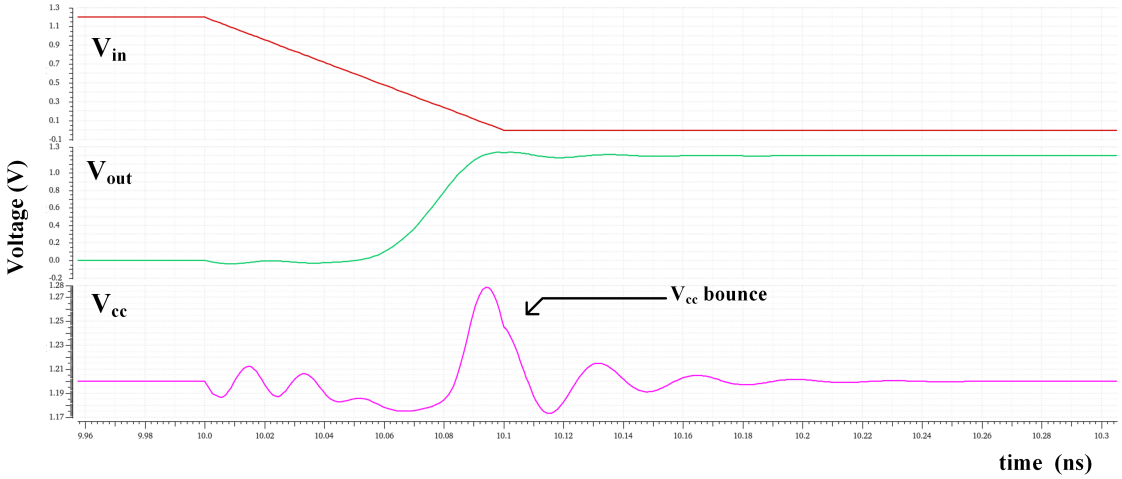


Figure 3.6 V_{cc} bounce plot based on the circuit in Fig. 3.5

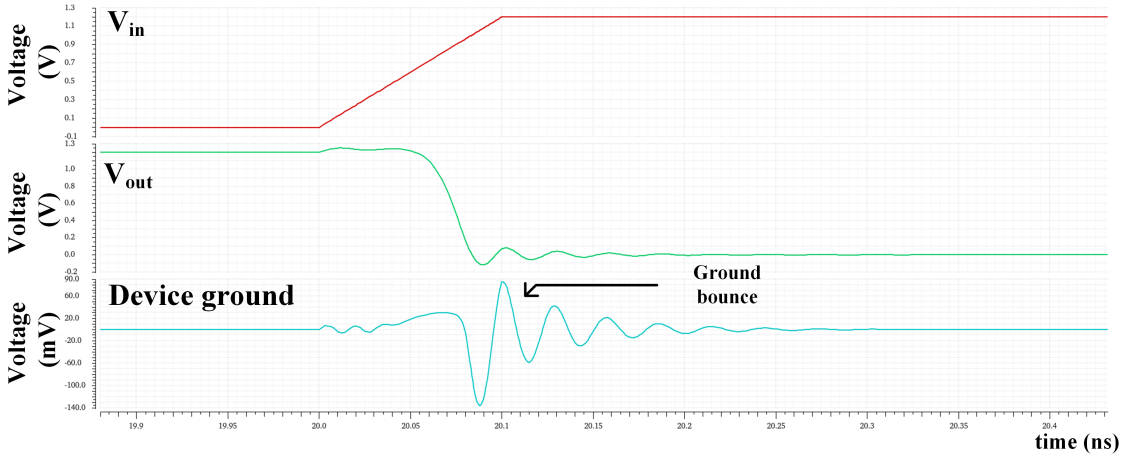


Figure 3.7 Ground bounce plot based on the circuit in Fig. 3.5

Suppose the output of the inverter switches from 0-1, a current is sourced from the supply creating a V_{cc} bounce, as shown in Fig. 3.6, and when the output of the inverter switches from 1-0, a current sink occurs creating a ground bounce, as shown in Fig. 3.7. The amount of current sourced or sunk from the output node depends on 3.14.

$$V = L_{\text{eff}} \frac{di}{dt} \tag{3.14}$$

Based on 3.14, the amplitude of the V_{cc} bounce and ground bounce is directly proportional to the effective inductance (L_{eff}). The problem arises if the ground bounce or V_{cc} is transferred to the circuits in the design. Suppose the ground bounce is transferred to the circuits in the design and the ground bounce is higher

than V_{IL} threshold of the input, then the input will be considered as logic "1", and hence, creates a glitch. Similarly, this phenomenon is also applied to V_{cc} bounce.

3.2.1 Parameters defining Ground bounce and V_{cc} bounce

The parameters that define ground bounce and V_{cc} bounce are as follows. V_{OLP} (peak) and V_{OLV} (valley) define the ground bounce parameters, and V_{OHP} (peak) and V_{OHV} (valley) define the V_{cc} bounce, as shown in Fig. 3.8. Moreover, the width of the pulse is also an important parameter. For instance, if an input buffer has a minimum recognizable pulse width of 5 ns at 1.2 V then any pulse width less than 5 ns will not be detected by the input buffer even if the amplitude is greater than 1.2 V (Microsemi (2008)).

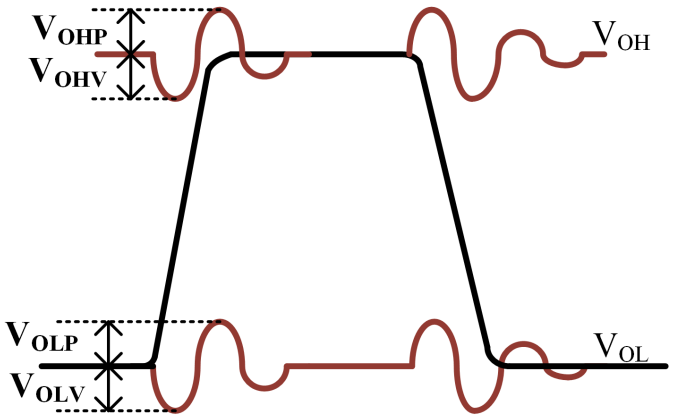


Figure 3.8 Parameters defining Ground bounce and V_{cc} bounce

3.2.2 Factors influencing Ground bounce and V_{cc} bounce

3.2.2.1 Effect of Capacitive load

As the capacitive load changes, the amplitude of the V_{cc} bounce and ground bounce also changes. If the capacitance increases for the same amount of current, the rate of change of voltage across the capacitor will change slowly based on 3.15. Hence, the amplitude of the bounce reduces, however, the pulse width increases.

$$\frac{I}{C} = \frac{dV}{dt} \tag{3.15}$$

3.2.2.2 Effect of Output Slew rate

The output slew rate (dV/dt) also affects the ground bounce and V_{cc} bounce. As the slew rate slows down, the amplitude of the ground bounce and V_{cc} bounce will be smaller. However, this will affect the performance such as the speed of the circuit.

3.2.3 Techniques to overcome SSN

i. Package Inductance Reduction

Based on 3.14, the amplitude of the ground bounce and V_{cc} depends on the effective inductance (L_{eff}) arising from the wire bond of the package, the trace of the package, and the pin. If the inductance was reduced then the amplitude of the bounce will also reduce (Swaminathan, Kim, Novak & Libous (2004)). Hence, flip chip becomes an attractive option to reduce the effective inductance (L_{eff}).

ii. Multiple V_{cc} pins and GND pins

Another method to reduce the effective inductance (Leff), when the die is wire bonded to the package, is to place multiple GND and V_{cc} pins. Suppose there were four GND pins and they are wire bonded. The total inductance (L_T) arising from the wire bond from the GND pin will be the parallel combination of all the inductance arising from the wire bond from all the GND pins, which can be expressed as 3.16.

$$\frac{1}{L_T} = \frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3} + \frac{1}{L_4} \tag{3.16}$$

where, L_1, L_2, L_3, L_4 are the inductance arising from the wire bond from first, second, third and fourth GND pins, respectively. If $L_1 = L_2 = L_3 = L_4 = L$, then

$$L_T = \frac{L}{4} \tag{3.17}$$

Hence, the total inductance arising from the wire bond of the GND pin will be L/4 as expressed in 3.17. Thereby, reducing the effective inductance (L_{eff}).

iii. Output Edge Control (OEC^{TM}) Technique

Output Edge Control (OEC^{TM}) technique (Instruments (1998); Madani (1996)) is a trademark of Texas Instruments Incorporated. The idea behind OEC^{TM} is to slow down the output falling and rising time of the output transistor while maintaining the total propagation delay. In Fig. 3.9(a) shows the typical layout of an NMOS and 3.9(b) shows the serpentine fashion of the polysilicon gate. Based on Fig. 3.9(b), the resistance due to the polysilicon and the capacitance from the gate creates a distributed RC network that slows down the turnon of the next segment, hence, the rise time and fall time are slowed. Fig. 3.10 shows the equivalent circuit of Fig. 3.9(b).

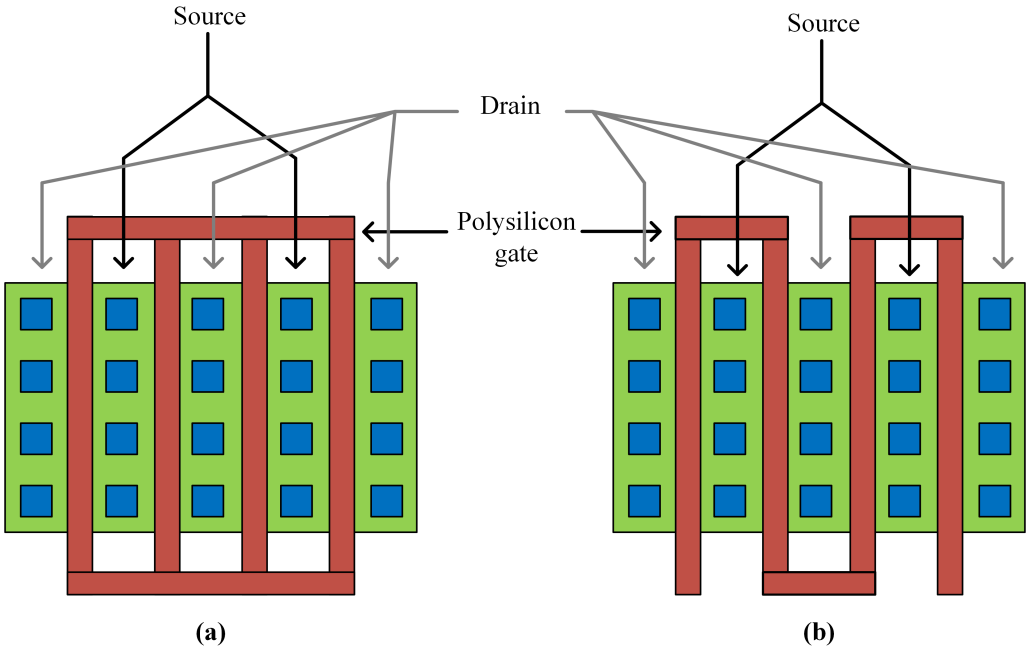


Figure 3.9 (a) Typical NMOS layout (b) Serpentine NMOS layout

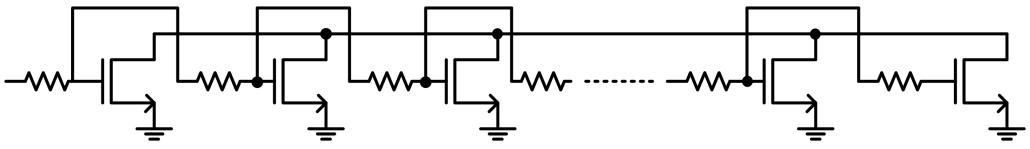


Figure 3.10 Distributed transistor

iv. Separate Analog and Digital GND

A very common technique used is to separate the analog and digital GND so that noisy digital ground does not affect the analog ground.

v. Wire bond on to the substrate

Rather than using a chip carrier, the die can be wire bonded on the substrate, thereby reducing the inductance arising from the package frame and pin. Hence, the effective inductance (L_{eff}) is reduced.

3.2.4 Comparison of SSN on Conventional and Proposed SAR logic

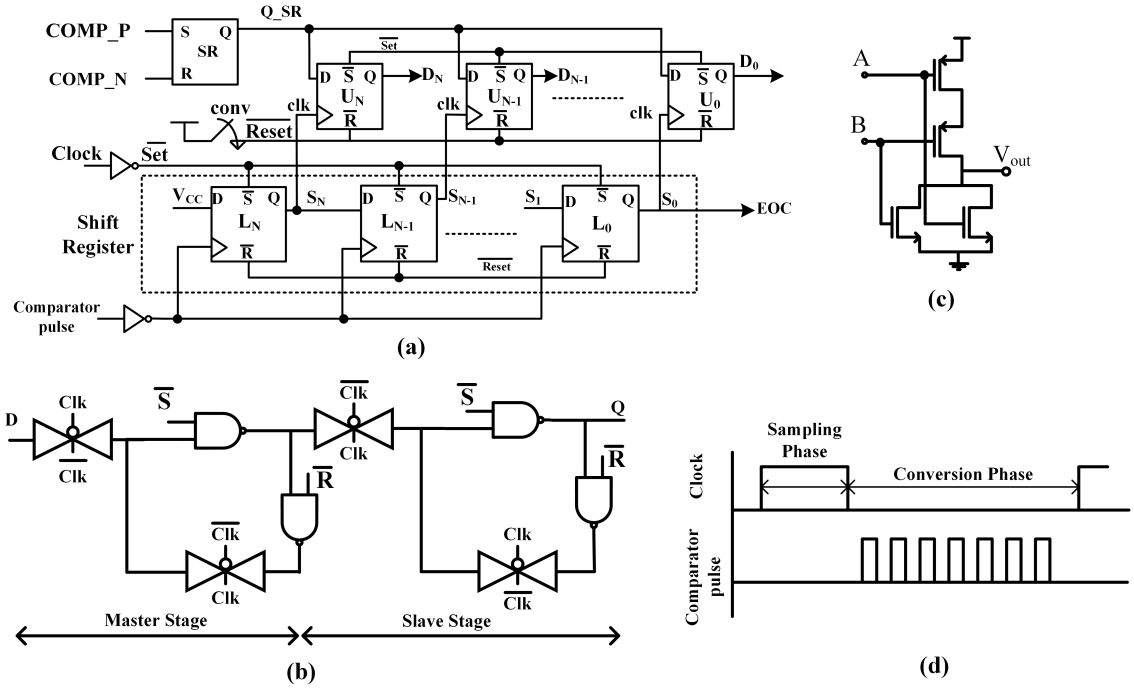


Figure 3.11 (a) Block diagram of the implemented conventional SAR Logic (b) Schematic of the positive edge triggered D Flip-flop with SET and RESET (c) Schematic of the NAND gate (d) Waveform for clock and comparator pulse

Based on the discussion of the conventional and proposed SAR logic, this section would like to analyze them in terms of V_{cc} bounce and ground bounce. The schematic of a conventional SAR logic is described in Fig. 3.11(a). A positive edge-triggered D FF with set and reset was used and the schematic is shown in Fig. 3.11(b), and the schematic of the NAND gate is shown in Fig. 3.11(c), and Fig. 3.11(d) shows the waveform for the clock and comparator pulse signal. During the reset phase of the SAR ADC, the reset pin ($\overline{R}$) of the flip-flop is activated by the $\overline{Reset}$ signal, and the set pin ($\overline{S}$) in the flip-flop is activated by the clock signal of the ADC after the reset phase. After the reset phase, the conv signal shown in Fig. 3.11(a) is activated always. During the sampling phase, the set signal ($\overline{Set}$) is activated to activate only the required switches in the CDAC, and during the conversion

phase, the set signal is deactivated. In the sampling phase, each flip-flop (L_N) in the shift register will have two simultaneous switching in both the power and ground lines created by the NAND gates connected to the $\overline{S}$ pin and $\overline{R}$ pin, respectively in the flip-flop. Similarly, again there will be two simultaneous switching in both the power and ground line created by the NAND gates in the flip-flop (U_N) activated by the shift register. Hence, for a 1-bit SAR ADC with a single-ended input, the SAR logic during the sampling phase will have four simultaneous switching in both the power and ground lines. For a differential input 1-bit SAR ADC, there will be two sets of SAR logic to control the differential DAC. Therefore, there will be eight simultaneous switching in both the power and ground lines. Therefore, for an 'n' conversion SAR ADC, there will be 8n simultaneous switching in both the power and ground line. Now, if the V_{cc} bounce and ground bounce created due to the 8n simultaneous switching in both the power and ground lines does not settle during the sampling phase then the bounce will affect the conversion phase.

In the conversion phase, during the first positive level of the pulse created by the comparator pulse shown in Fig. 3.11(d), the outputs of the comparator (COMP_P and COMP_N) are attained. In the negative edge of the comparator pulse, the flip-flop L_N in the shift register in Fig. 3.11(a) is activated which then activates the flip-flop U_N. Based on the comparator output, the flip-flop U_N gives appropriate signals to the DAC. To analyze the simultaneous switching noise in the conversion phase, let's consider a 1-bit single-ended input SAR ADC that requires only one SAR logic which comprises of one flip-flop L_N from the shift register and one flip-flop U_N that is activated by L_N. In the positive level of the comparator pulse, the NAND gates in the master stage of the L_N flip-flop will have one switching to V_{DD} and ground. Once, the comparator pulse goes low then there is one switching to V_{DD} and ground from the slave stage of L_N. In the worst case, the NAND gates of the master stage of the U_N flip-flop are activated at the same time the NAND gates are activated in the slave stage of the L_N flip-flop. This creates two simultaneous switching in both the power and ground lines. Later, after the positive trigger in the clk of the flip-flop U_N, the NAND gates of the stave stage of flip-flop U_N undergo one switching to V_{DD} and ground. Hence, for a 1-bit single-ended SAR ADC, there are three adjacent simultaneous switching occurring. Firstly, one switching to V_{DD} and ground by the NAND gates in the master stage of the L_N flip-flop. Secondly, two simultaneous switching occurs when the slave stage of L_N and the master stage of U_N are activated at the same time. Finally, one switching to V_{DD} and ground by the NAND gates in the slave stage of the U_N. Therefore, for a 1-bit or 'n' conversion differential-ended SAR ADC, the three adjacent simultaneous switching occurs for each conversion and they are as follows:

i. Two switching to V_{DD} and ground by the NAND gates in the master stage of the L_N flip-flop.

ii. Four simultaneous switching occurs when the slave stage of L_N and the master stage of U_N are activated at the same time.

iii. Two switching to V_{DD} and ground by the NAND gates in the slave stage of the U_N

In the case of the proposed SAR logic, Fig. 3.4(a) shows the block diagram of the proposed SAR logic. It can be noticed that a unit logic cell comprises three latches. Hence, for a 1-bit differential input SAR ADC with one unit logic cell, there will be three simultaneous switching to both V_{DD} and ground lines during the sampling phase. Hence, for an 'n' conversion SAR ADC, there will be 3n simultaneous switching to both V_{DD} and ground lines in the sampling phase. During the conversion phase, one of the outputs of the comparator is activated based on its input either Req_p<N>/Req_n<N> is activated. Based on Fig. 3.4(a), if Req_p<N> is activated then the D latch with Req_p<N> connected to the EN pin is activated, this creates one voltage and ground bounce. In the Acknowledgment block, the NOR gate is activated by switching from 1 to 0 creating a ground bounce. In the worst case, when both the D latch of the Request block and NOR gate of the Acknowledgement block switch simultaneously, there can be two simultaneous switching to the ground line and one switching to the V_{DD} line. Then, the next adjacent switching occurs in the D latch of the Acknowledgment block. This creates one switching to V_{DD} and ground line. Hence, in the conversion phase of the proposed SAR logic for an 'n' conversion differential SAR ADC will have two adjacent simultaneous switching as follows:

i. Two simultaneous switching to the ground line and one switching to the V_{DD} line by the D latch in the Request block and NOR gate in the Acknowledgement block.

ii. One switching to both V_{DD} and ground line by the D latch in the Acknowledgment block

On comparing the conventional and proposed SAR logic during the sampling phase, it can be verified that the number of switching in the proposed SAR logic is lesser compared to the conventional SAR logic. Moreover, during the conversion phase there are lesser number of adjacent and simultaneous switching in the proposed SAR logic compared to the conventional SAR logic.

3.3 Results

The proposed asynchronous SAR logic based on handshake protocol is fabricated in an 8-metal CMOS process. Fig. 3.12 shows the chip micrograph and zoomed layout view of the ADC. The ADC occupies 0.016 mm^2.

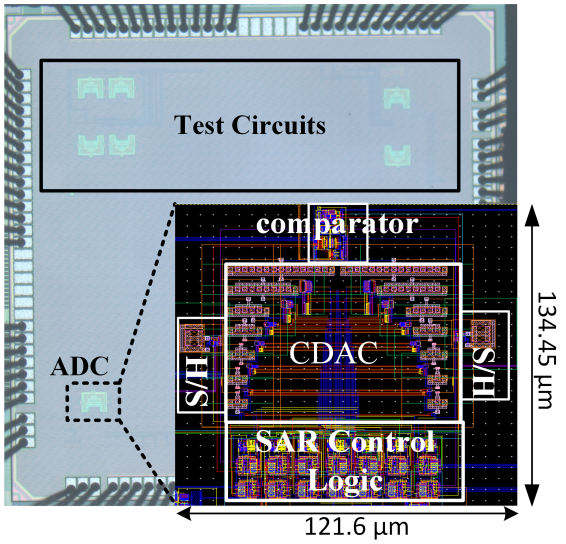


Figure 3.12 Chip micrograph with zoomed-in layout view

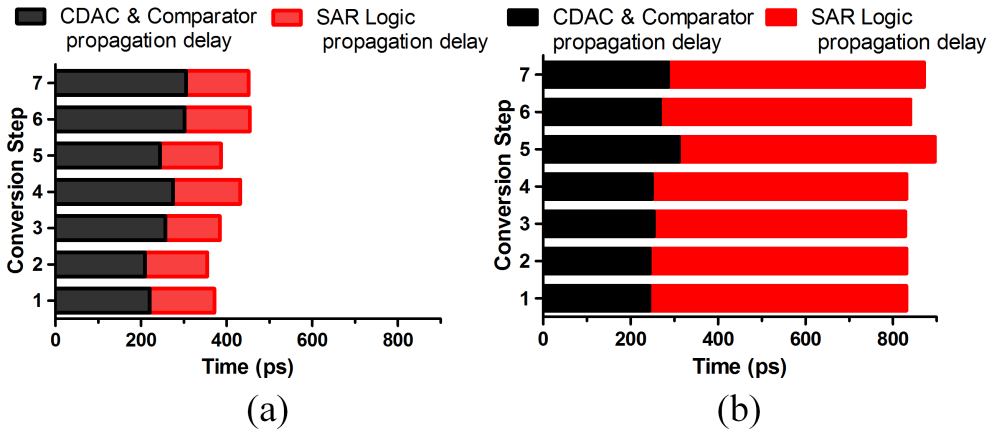


Figure 3.13 Simulated propagation delay for the (a) Proposed and (b) Conventional SAR logic for every conversion cycle

Fig. 3.13(a) and (b) show the simulated propagation delay for the SAR ADC with the proposed and conventional SAR logic, respectively for every conversion cycle. It can be observed that the average propagation delay for the proposed and conventional SAR logic are 0.145 ns and 0.582 ns, respectively. It can be observed from Fig. 3.13 that the simulated propagation delay of the SAR logic almost remains the same

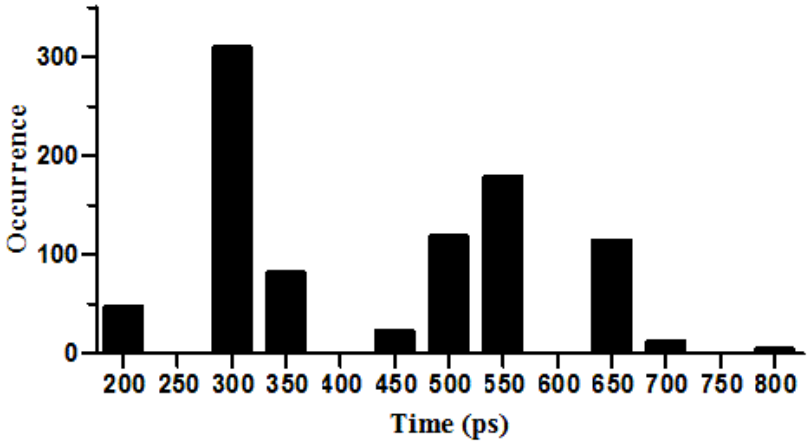


Figure 3.14 Histogram plot showing the measured propagation delay for one conversion of the SAR ADC

whereas the sum of the propagation delay of the CDAC and the comparator varies. Fig. 3.14 shows the histogram plot of the measured propagation delay for one conversion of the SAR ADC. The propagation delay includes the CDAC settling time, the comparator delay, and the SAR logic delay. The minimum propagation delay is measured as 0.214 ns. From simulations, one of the cases from many conversion cycles, the average propagation delay of the SAR logic is 0.145 ns. This result can be validated from measurement (Fig. 3.14) as the minimum total propagation delay that includes the CDAC, the comparator, and the SAR logic is 0.214 ns. Hence, the propagation delay of the SAR logic is less than 0.214 ns.

The SSN of the proposed SAR logic and the conventional SAR logic were compared using the parameters shown in Fig. 3.8. In the simulation setup, the power and ground lines for the analog circuit and digital circuit were kept separate. Since, the major contribution of the SSN is due to $L_{eff}di/dt$ noise, where L_{eff} is the sum of the series inductance from the package bond wire, package trace, and package pin, therefore, an inductor was placed to the power and ground line of the digital block. In the digital block, we have only considered the SAR logic to analyze the SSN from the SAR logic. The inductance was varied from 1 nH to 9 nH with a step size of 1 nH. Fig. 3.15 (a) and (b) shows the waveform for the V_{cc} bounce and ground bounce for the proposed and conventional SAR logic, respectively when an inductor of 1 nH was added in series to the power and ground line of the SAR logic. A sampling period of 5 ns was chosen to make sure the sampling network has enough time to track the input as close to each other. In Fig. 3.15(a) shows a clock signal with 5 ns as the sampling phase and the remaining as the conversion phase. The ground signal and V_{DD} signal show the ground bounce and V_{cc} bounce during the sampling and conversion phase, respectively. The comparator pulse shows that there are seven

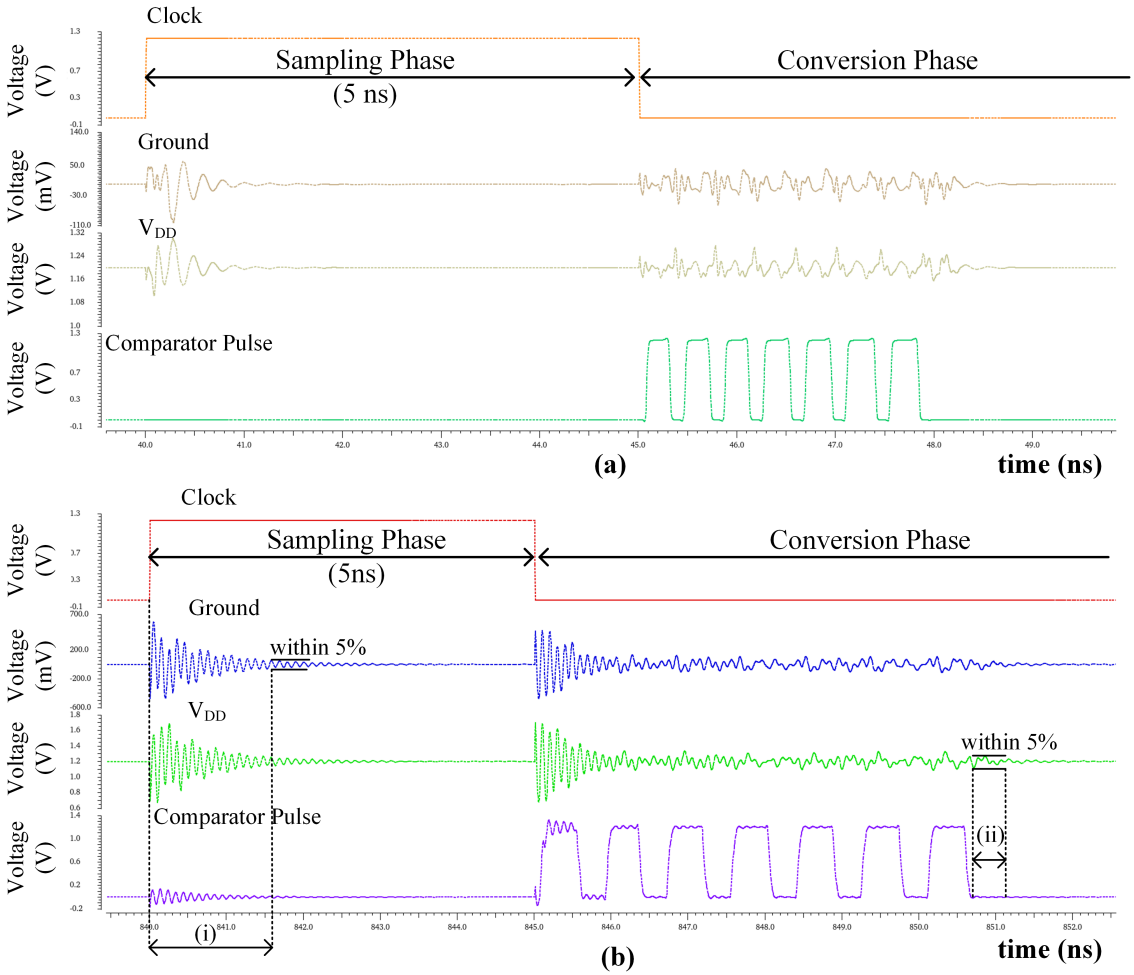


Figure 3.15 Simulated waveform showing the ground and V_{cc} bounce when a 1 nH inductor is connected to the power and ground supply of the SAR Logic for the (a) proposed and (b) conventional SAR logic

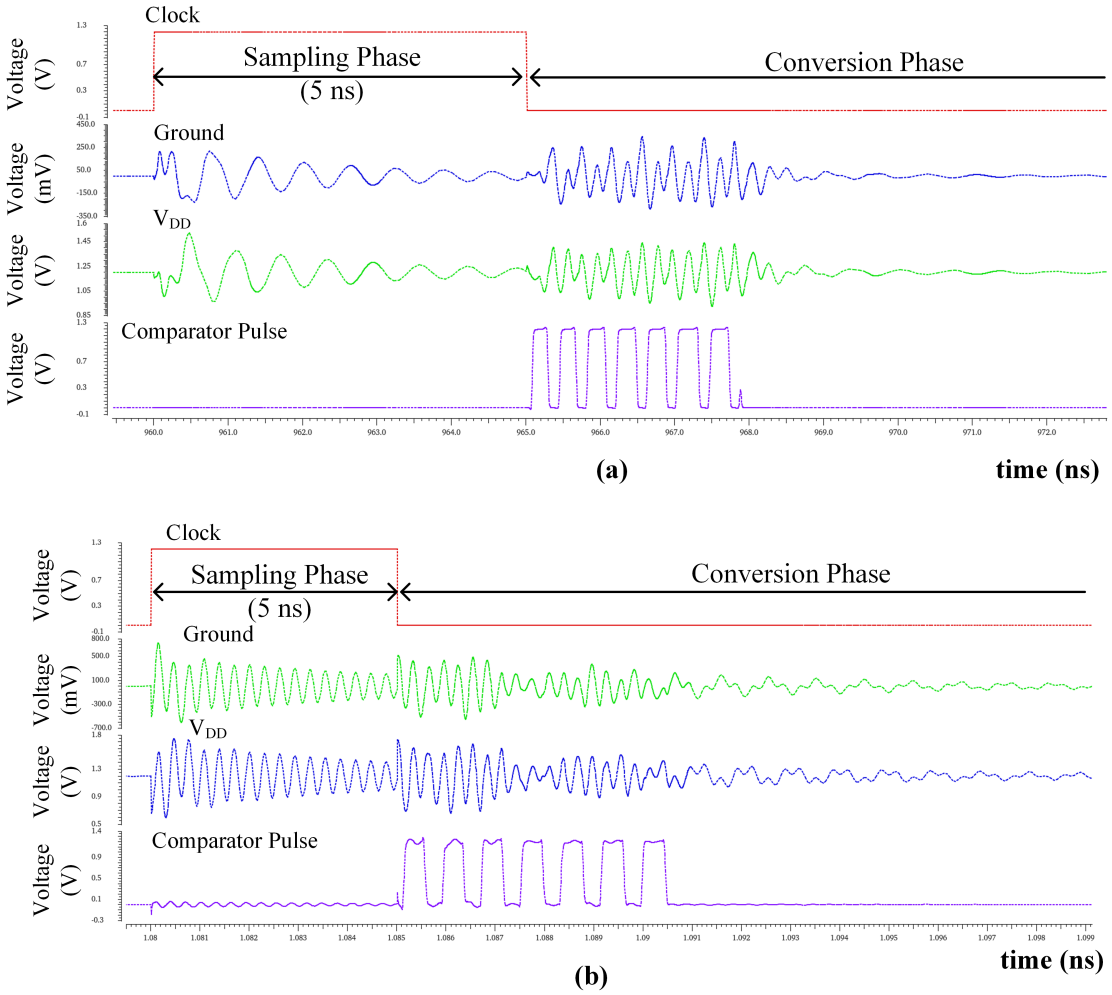


Figure 3.16 Simulated waveform showing the ground and V_{cc} bounce when a 9 nH inductor is connected to the power and ground supply of the SAR Logic for the (a) proposed and (b) conventional SAR logic

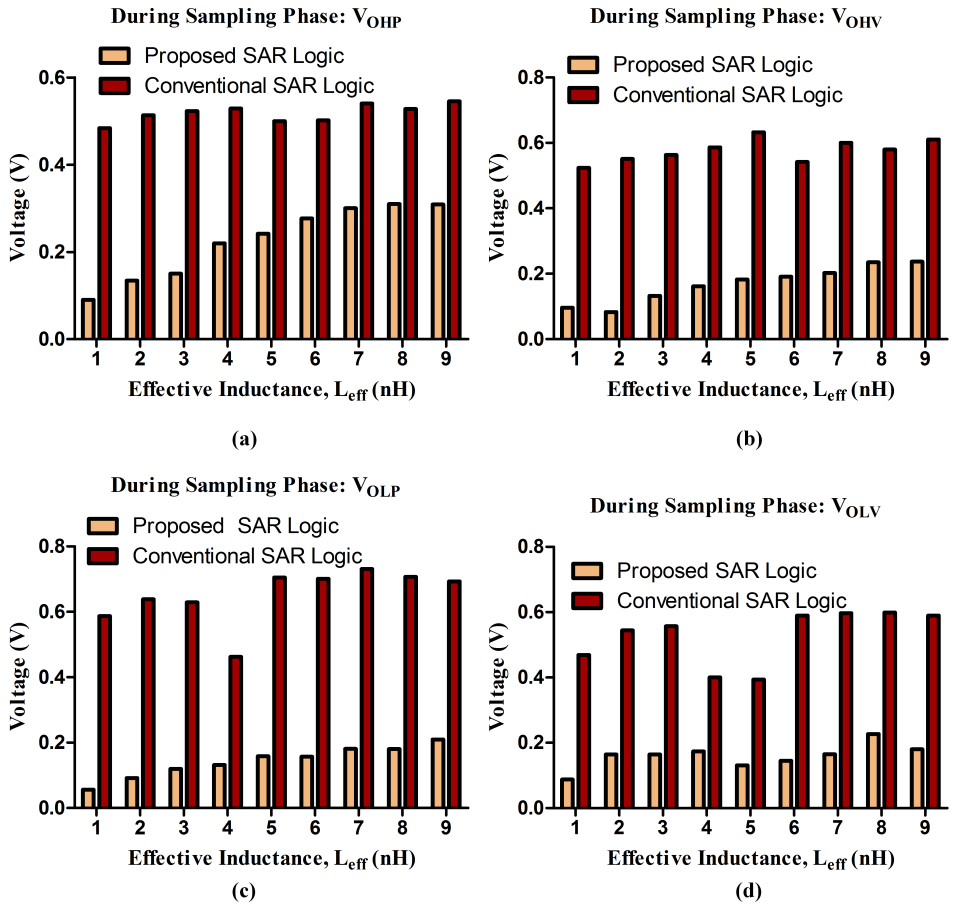


Figure 3.17 Comparison of simulated ground and V_{cc} bounce parameters: (a) V_{OHP} and (b) V_{OHV} (c) V_{OLP} and (d) V_{OLV} for conventional and proposed SAR logic during the sampling phase

conversions occurring and at each positive level of the pulse the comparator in SAR ADC provides an output. Fig. 3.15(b), (i) designates the settling time of the ground signal during the sampling phase. The settling time for the ground bounce during the sampling phase is calculated from the rising edge of the clock signal to the point when the ground signal reaches 5% of the final value. Similarly, the settling time of the V_{cc} bounce during the sampling phase is calculated from the rising edge of the clock signal to the point when the V_{DD} signal reaches 5% of the final value. In Fig. 3.15(b), (ii) denotes the settling time of the V_{cc} bounce during the conversion phase. It is defined as the time from the falling edge of the last comparator pulse to the point where the V_{DD} signal reaches within 5% of its final value. Similarly, the settling time of the ground bounce during the conversion phase is the time taken from the falling edge of the last comparator pulse to the point where the ground signal reaches within 5% of its final value. Fig. 3.16(a) and (b) show the ground and V_{cc} bounce when a 9 nH inductor is connected to the power and ground supply of the SAR Logic for the proposed and conventional SAR logic, respectively.

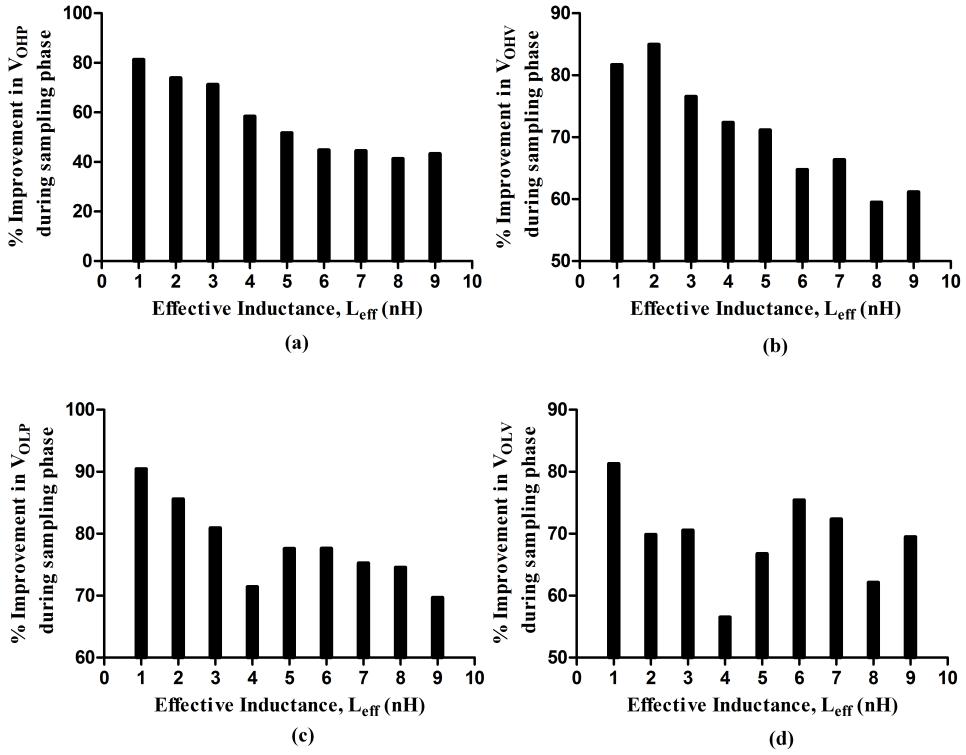


Figure 3.18 Percentage improvement of the proposed SAR logic w.r.t the conventional SAR logic in terms of the SSN parameters during the sampling phase

Fig. 3.17 compares the ground and V_{cc} bounce parameters (a) V_{OHP} and (b) V_{OHV} (c) V_{OLP} and (d) V_{OLV} for conventional and proposed SAR logic during the sampling phase for different effective inductance L_{eff}. Fig. 3.18 shows the percentage improvement of the proposed SAR logic w.r.t the conventional SAR logic in terms of the SSN parameters during the sampling phase. It can be observed that V_{OHP}, V_{OHV}, V_{OLP} and V_{OLV} has at least 40 %, 50 %, 65 % and 50 % improvement compared to the conventional SAR logic, respectively.

Fig. 3.19 compares the ground and V_{cc} bounce parameters (a) V_{OHP} and (b) V_{OHV} (c) V_{OLP} and (d) V_{OLV} for conventional and proposed SAR logic during the conversion phase for different L_{eff}. Fig. 3.20 shows the percentage improvement of the proposed SAR logic w.r.t the conventional SAR logic in terms of the SSN parameters during the conversion phase. It can be observed that V_{OHP}, V_{OHV}, V_{OLP} and V_{OLV} has at least 50 %, 20 %, 20 % and 40 % improvement compared to the conventional SAR logic, respectively. Fig. 3.21 shows the difference in ENOB for different effective inductance (L_{eff}) values w.r.t to the ENOB without inductance for the proposed and conventional SAR logic. From Fig. 3.21 it can be observed that the simulated ENOB without considering the effective inductance (L_{eff}) for the proposed and conventional SAR logic designed in the same architecture i.e. 6-bit V_{cm} SAR ADC are 5.8204 and 5.2321 bits, respectively. It can be observed that the number of bits are

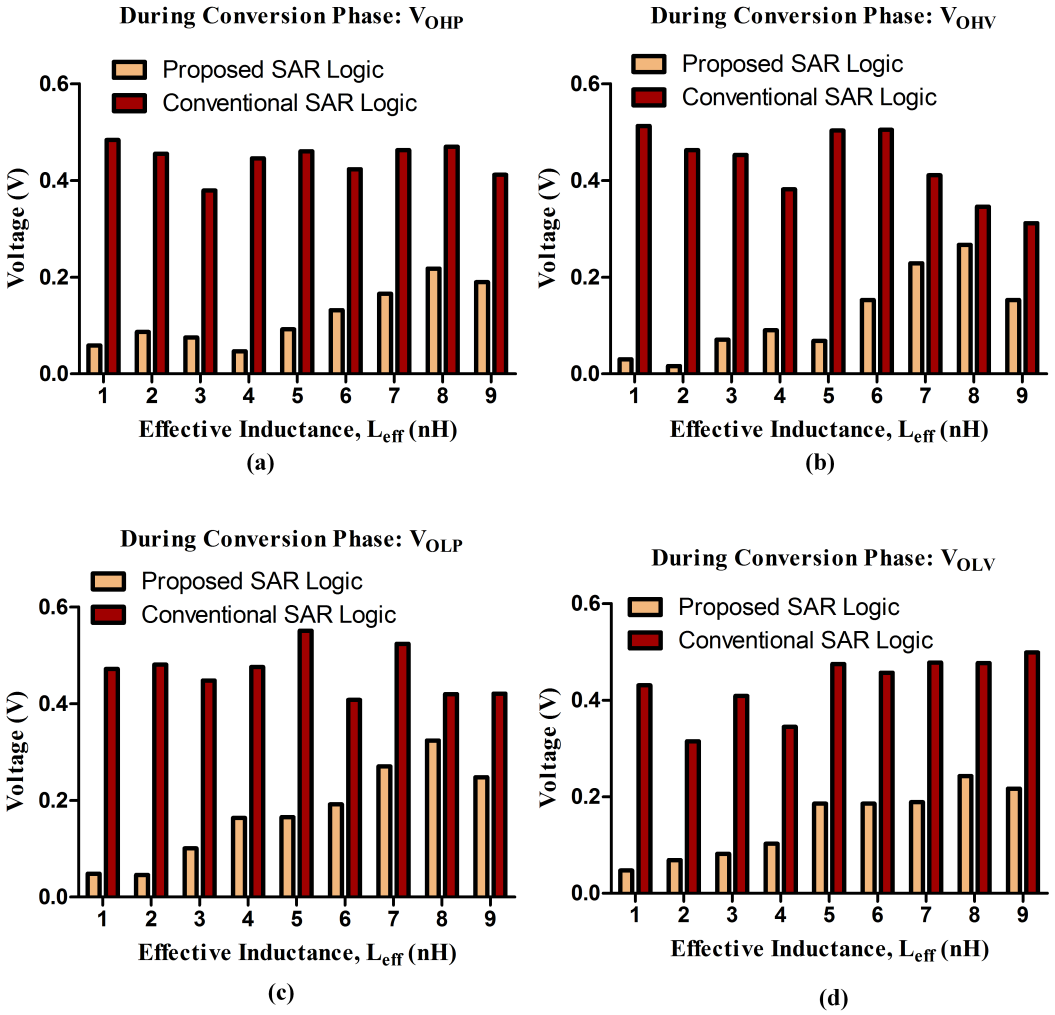


Figure 3.19 Comparison of simulated ground and V_{cc} bounce parameters: (a) V_{OHP} and (b) V_{OHV} (c) V_{OLP} and (d) V_{OLV} for conventional and proposed SAR logic during the conversion phase

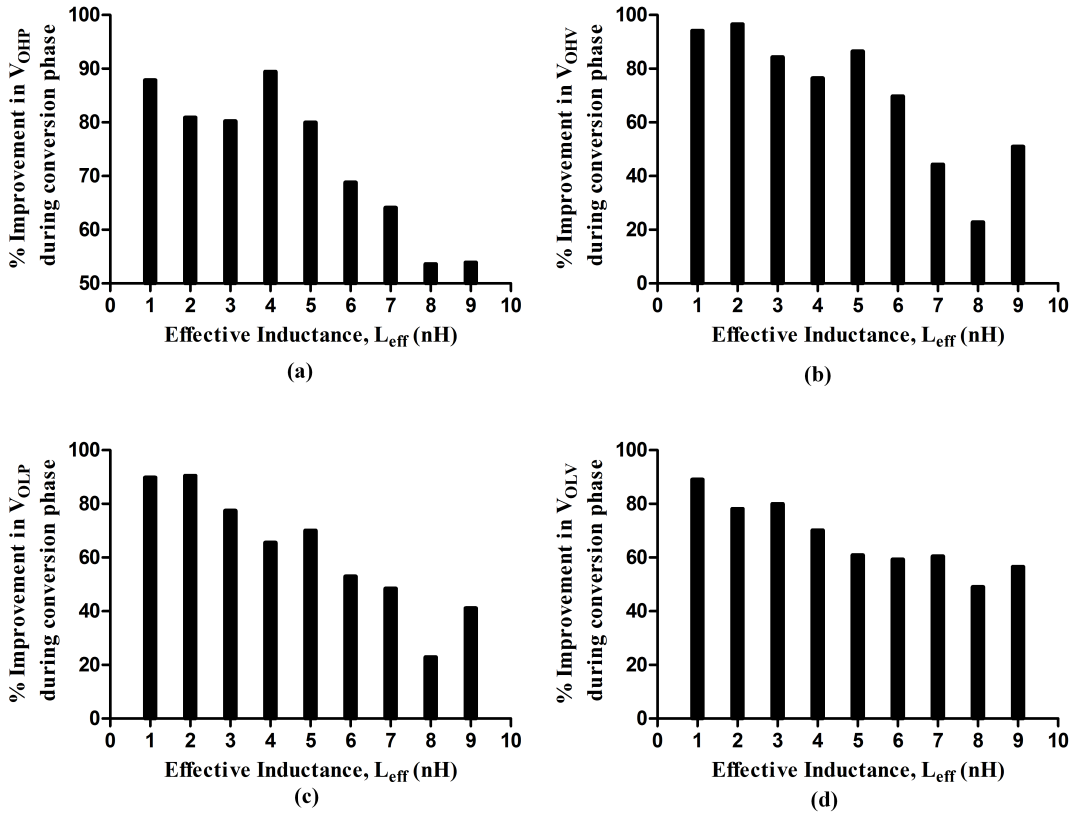


Figure 3.20 Percentage improvement of the proposed SAR logic w.r.t the conventional SAR logic in terms of the SSN parameters during the conversion phase

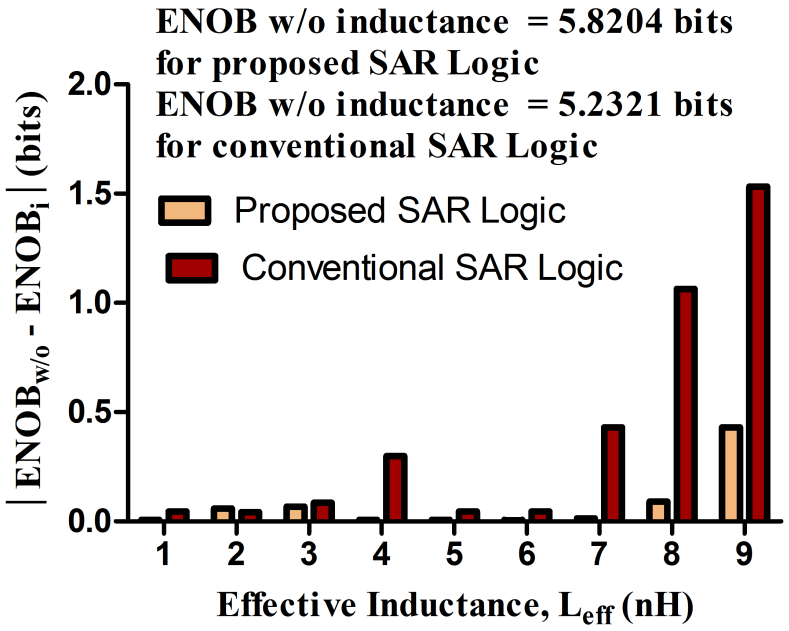


Figure 3.21 Difference in ENOB for different effective inductance (L_{eff}) values w.r.t to the ENOB without inductance for the proposed and conventional SAR logic

reduced faster in the case of SAR ADC designed with the conventional SAR logic. It is noticed that the number of bits reduced by more than 1-bit for L_{eff} greater than 8 nH. However, the maximum reduction in the ENOB is around 0.4 bits in the SAR ADC designed using the proposed SAR logic. Fig. 3.22(a) and (b) shows the settling time required for the power supply and ground signal, respectively during the sampling phase. From Fig. 3.22(a) and (b), it is observed that when the effective inductance (L_{eff}) is greater or equal to 4 nH, the settling time for both the power supply and the ground exceeds 5 ns, and the proposed SAR logic has a maximum settling time of 4.2 ns. Hence, by using the proposed SAR logic the noise created in the V_{DD} and ground subsides before entering the conversion phase. In Fig. 3.23, the maximum time to settle for the V_{DD} and ground is around 1 ns which is less than the settling time taken by the conventional SAR ADC.

Table 3.1 compares the proposed asynchronous SAR logic based on handshake protocol with recent works (Cao, Chen, Ni, Y. & Ren (2018); Chang & Hsieh (2017,1); Shah & Sahoo (2017)). As observed from Table 3.1, the proposed SAR logic is more than 75.3 % faster than the conventional SAR logic, and comparable with the speed of the other compared works.

Fig. 3.24 (a) shows the measured SNDR, SFDR, and ENOB of 32 dB, 42.65 dBc, and 5.023 bits, respectively at an input frequency of 1.3477 MHz with a sampling speed of 30 MS/s for the SAR ADC. Fig. 3.24 (b) shows the measured SNDR, SFDR and

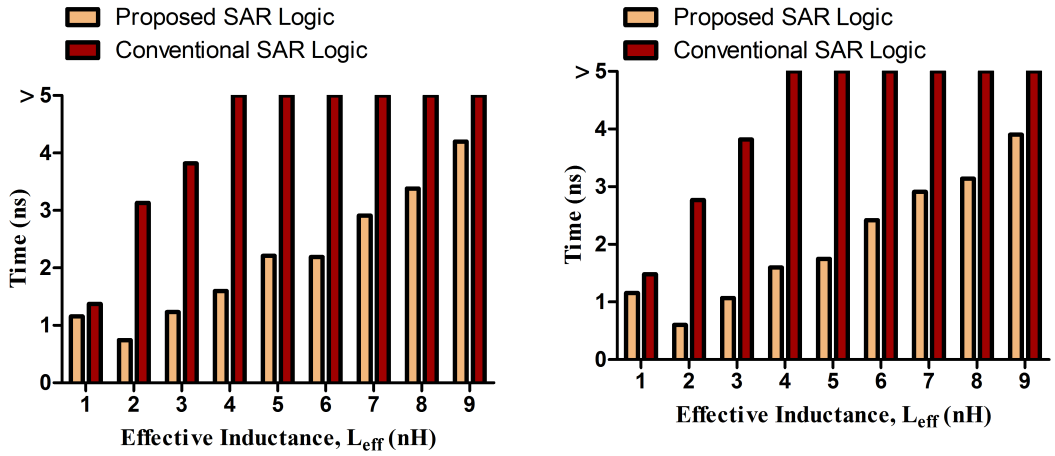


Figure 3.22 Settling time for the (a) power supply and (b) ground during the sampling phase

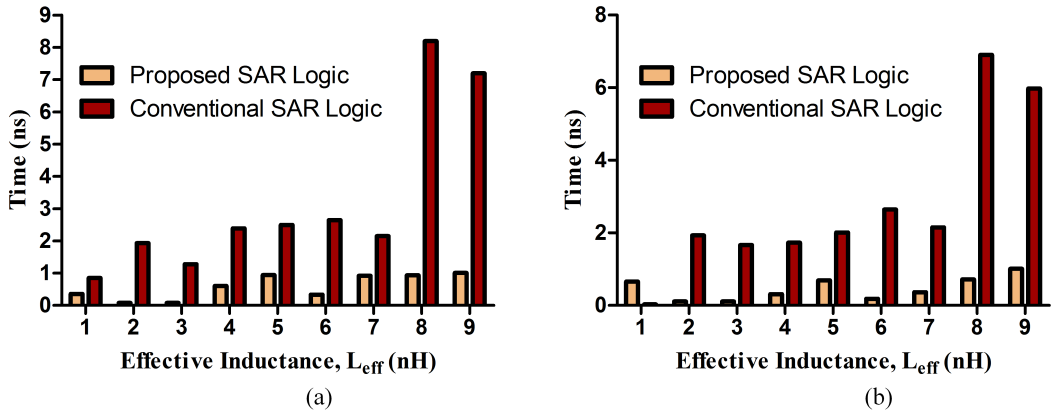


Figure 3.23 Settling time for the (a) power supply and (b) ground during the conversion phase

Table 3.1 Comparison of the SAR logic to recent works

	This work	**Shah** (2017)	**Cao** (2018)	**Chang** (2017)	**Chang** (2018)
Process [nm]	90	65	65	40	40
Architecture	VML	VML	VML	CML	CML
Single conversion delay (ns):					
Conventional method	**0.587**	0.21	0.24	-	-
Proposed method	**0.145**	0.15	0.13	0.300	0.200
% reduction in delay	**75.3**	25.71	45.83	-	-
Power (mW)*	**0.165**	0.844	-	-	0.99**

*power of the SAR Logic normalized w.r.t to the number of conversions
**total power of the digital block

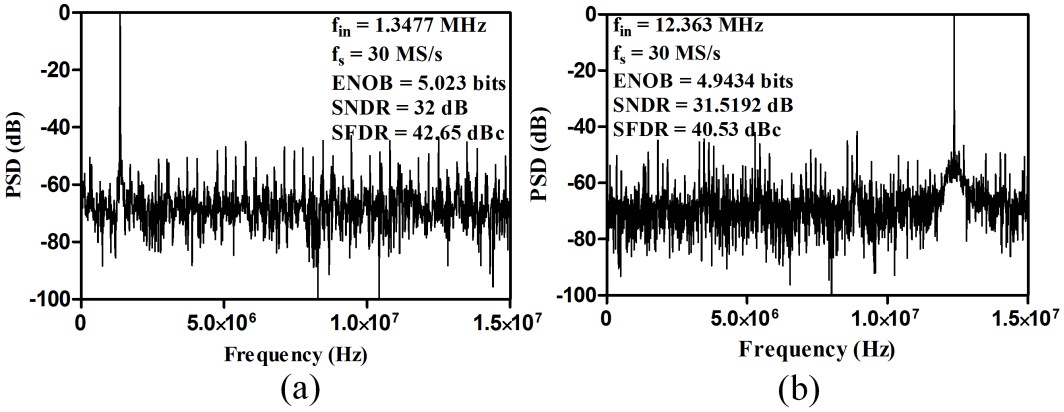


Figure 3.24 Measured spectrum for an input frequency of (a) 1.3477 MHz and (b) 12.363 MHz sampled at 30 MS/s

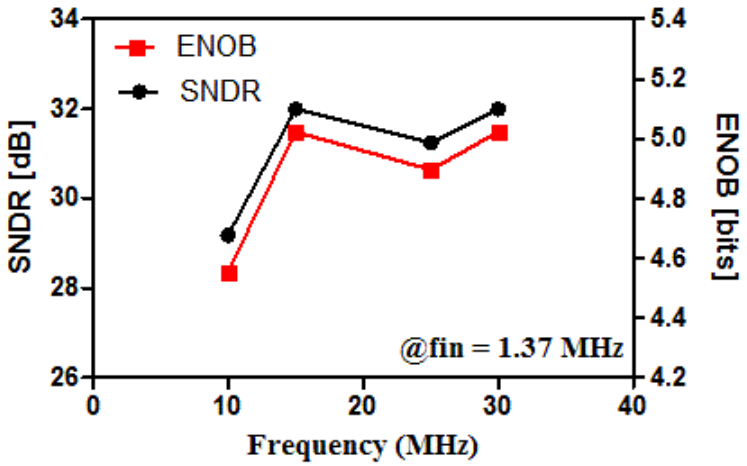


Figure 3.25 Measured SNDR and ENOB versus sampling frequency

ENOB are 31.51 dB, 40.53 dBc, and 4.9434 bits, respectively with a sampling speed of 30 MHz at near Nyquist frequency. Fig. 3.25 shows the measured SNDR and

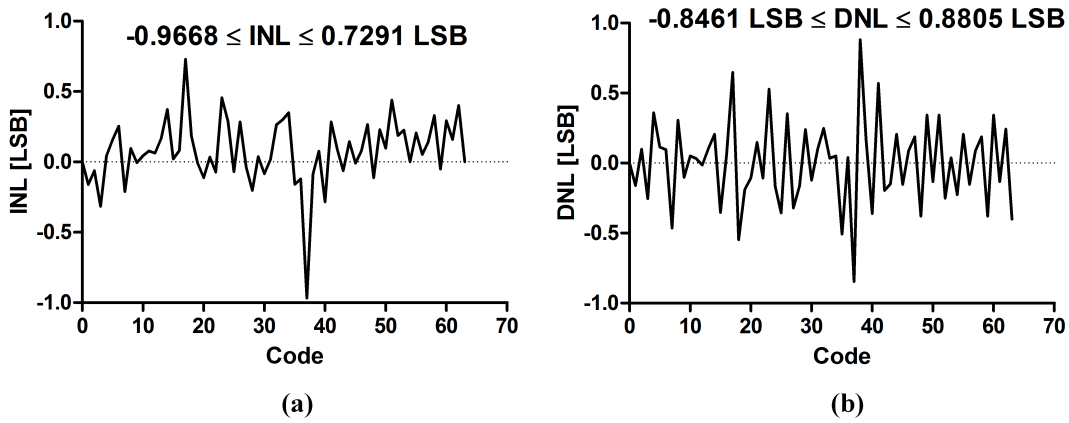


Figure 3.26 Measured INL and DNL

Table 3.2
Measured Performance Summary

Supply Voltage [V]	1.2
Resolution [bit]	6
Sampling Rate [MS/s]	30
SNDR @ 1.3477 MHz input [dB]	32
SFDR @ 1.3477 MHz input [dBc]	42.65
ENOB @ 1.3477 MHz input [bits]	5.023
SNDR @ Nyq [dB]	31.5192
SFDR @ Nyq [dBc]	40.53
ENOB @ Nyq [bits]	4.9434
DNL [LSB] INL [LSB]	+0.88/-0.84 +0.72/-0.96
Power [mW]	0.212
FoM_W @ Nyq [pJ/conversion-step]	0.229

ENOB at an input frequency of 1.37 MHz for different sampling frequencies. The measured INL and DNL are within -0.9668/+0.7291 LSB and -0.8461/+0.8805 LSB, respectively, as shown in Fig. 3.26. Table 3.2 shows the performance parameters of the ADC.

4. Single Channel SAR-Assisted Pipeline ADC with a Novel Overshoot Reduction Technique

In a SAR-assisted pipeline ADC, SAR ADC and residue amplifier are the two blocks that determine the speed and power of the ADC. Among them, the residue amplifier is the most power-hungry. Traditionally, the residue amplifier uses high-gain op-amp, but as the CMOS technology scales, the intrinsic gain of the transistor ($g_m r_0$) reduces (Lee, Chandrakasan & Lee (2012)). Hence, alternative approaches such as inverter-based circuits (Chae & Han (2009); Chae, Souri & Makinwa (2013)), ring amplifier (Hershberg, Weaver, Sobue, Takeuchi, Hamashita & Moon (2012a,1)) and zero-crossing-based circuits (ZCBCs) were introduced to circumvent the scaling issue. Among the three approaches mentioned, the zero-crossing-based circuits (ZCBCs) were selected as they replaced the high-gain op-amp using a zero-crossing detector (ZCD) and a pair of current sources (Brooks & Lee (2009); Fiorenza, Sepke, Holloway, Sodini & Lee (2006)) and reduces power. However, the major limitation in a ZCBC-based residue amplifier is the overshoot voltage. The overshoot voltage is signal polarity dependent and depends on the nonlinearity of the current source. Moreover, the overshoot voltage reduces the speed of the ZCD and the input range for the next stage of the pipeline ADC. Hence, this chapter introduces a novel technique to detect the zero-crossing of the residue voltage of the SAR ADC accurately and reduces the overshoot voltage in the ZCBC.

This chapter introduces the residue amplifier designed using the conventional differential ZCBC, and then discusses the novel technique to detect the zero-crossing of the residue voltage of the SAR ADC with a minimum amount of overshoot. The novel technique is then implemented in a 1-bit/cycle V_{cm}-based sub-radix SAR-assisted pipeline ADC along with the proposed SAR logic explain in chapter 3. Finally, this section presents the post-layout simulation results.

4.1 A Novel Technique to Minimize Overshoot in ZCBC

4.1.1 Differential Zero-Crossing-Based Circuit

4.1.1.1 Conventional Zero-Crossing-Based Circuit (ZCBC)

A conventional ZCBC consists of a ZCD, current sources and feedback capacitors to amplify the residual voltage of the ADC, as shown in Fig. 4.1(a). The timing diagram of the ZCBC (Brooks & Lee (2009)) is shown in Fig. 4.1(b). During Φ_1 phase, Φ_1 switch is activated and the SAR ADC translates the sampled analog signal to digital format. At the end of the Φ_1 phase, the residual voltage stored in capacitors C_{T_p} and C_{T_m} of the SAR ADC is available as input to the ZCD. In the Φ_{2I} phase, Φ_{2I} is activated to reset capacitors (C_{T2_p} and C_{T2_m}) of the next stage SAR ADC. Moreover, the feedback capacitor C_1 is reset during the overlap of Φ_{2I} and Φ_1 phase. The nodes V_{tp_p} and V_{tp_m} are connected to V_{DD} and ground, respectively and the bottom plates of the capacitors are connected to V_{cm} for a V_{cm}-based SAR ADC. At the end of Φ_{2I} phase, E_1 is activated to charge the capacitors of the V_{cm}-based SAR ADC by current source I_1. The current sources enable the voltage at V_{in+} and V_{in-} to move towards each other. Once, V_{in+} and V_{in-} become equal to each other i.e. the zero-crossing has been detected, the ZCD deactivates E_1 and E_2. Due to the finite delay of the control logic, there is an overshoot voltage. The overshoot voltage (V_{ov}) depends on the rate of change of the output ramp slope (dV_{tp_p}/dt) and time for overshoot (T_D) (Shin, Rudell, Daly, Muñoz, Chang, Gulati, Lee & Straayer (2014)).

$$V_{ov} = V_{o\_p} - V_{cm} \tag{4.1}$$

$$V_{ov} = T_D \frac{dV_{tp\_p}}{dt} = V_{ov1} + V_{ov2} \tag{4.2}$$

where T_D is the time taken to overshoot, V_{ov1} is the static offset due to delay from the control logic and V_{ov2} is the non-linearity of the ramp output from the current source. It can be observed from (4.2) that the overshoot voltage decreases the input

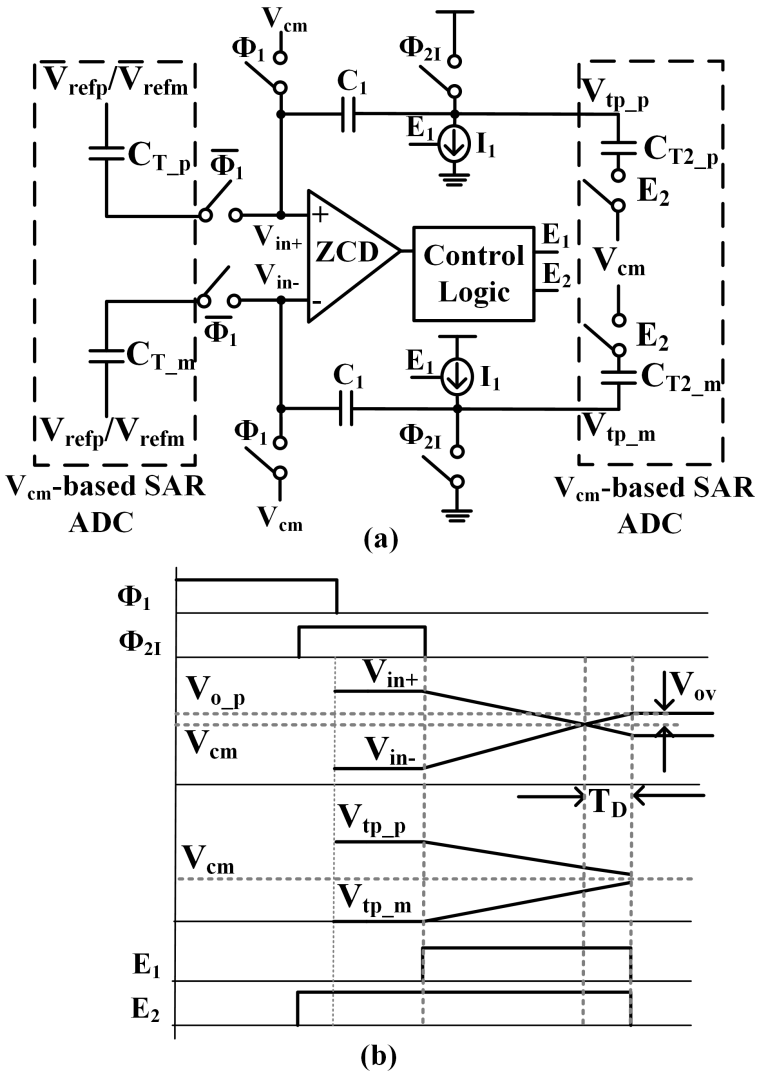


Figure 4.1 (a) Block Diagram and (b) Timing diagram of a Conventional Zero-Crossing-Based Circuit (ZCBC)

range to the next stage of the pipeline ADC. Moreover, the effect of overshoot voltage increases in circuits designed with larger feature size because of the increase in gate delay. Due to the large gate delay, the time taken for the control logic to deactivate the current source will increase.

The coarse and fine current source technique (Shin et al. (2014)) to detect the zero-crossing is the most widely used method to reduce overshoot voltage. In this method, a coarse current source is activated to detect the coarse threshold. Then, the ZCD enters the fine phase where a fine current source is applied to detect the zero-crossing. The disadvantage of this technique is that during the fine phase the speed of the residue amplifier is reduced. Hence, to overcome the speed problem due to the fine current source, the proposed technique uses a two-step method to detect zero-crossing with minimum overshoot voltage and increases the speed of the

residue amplifier.

4.1.2 Proposed Differential Zero-Crossing-Based Circuit (ZCBC)

4.1.2.1 Proposed Zero-Crossing-Based Circuit (ZCBC)

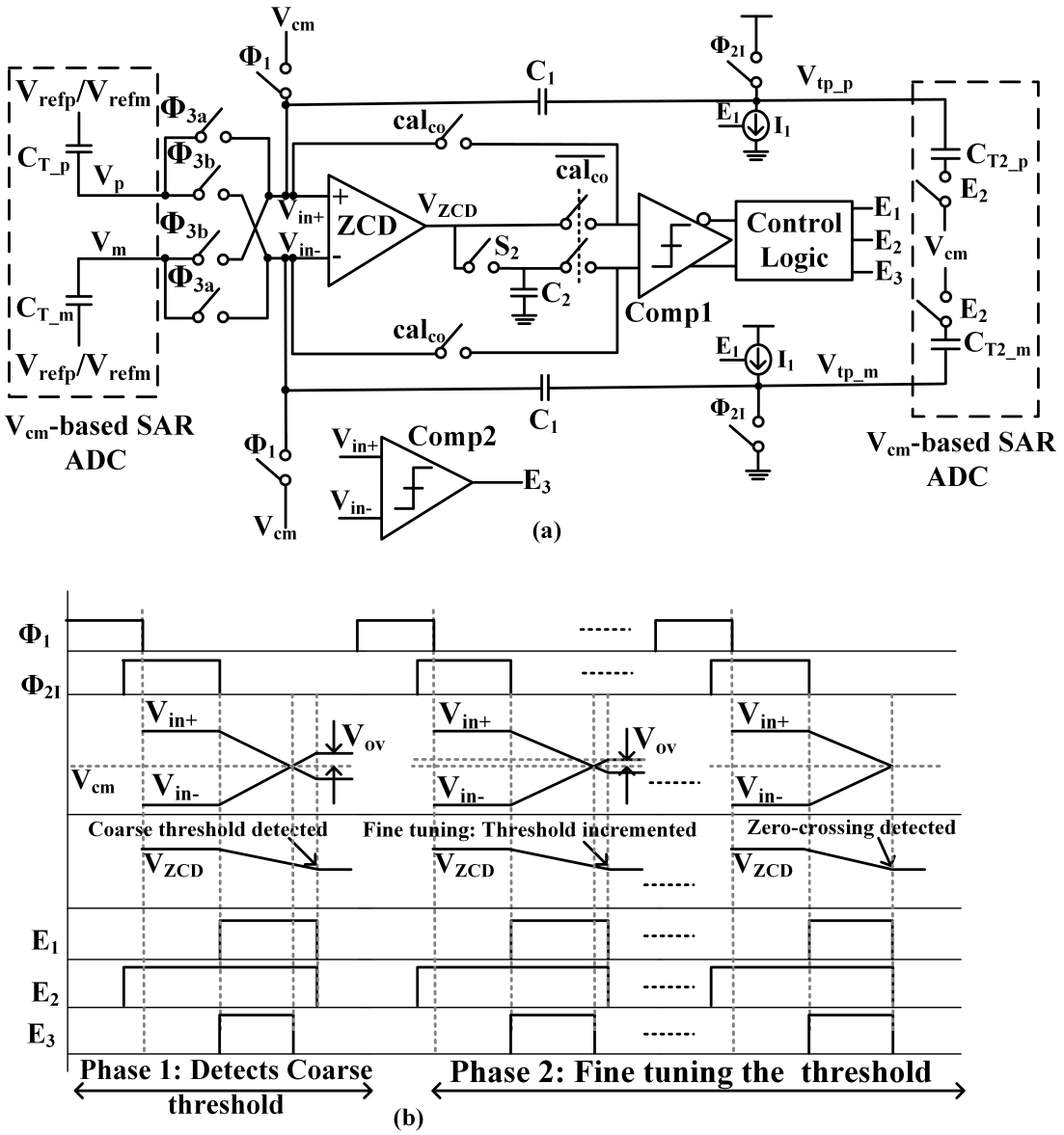


Figure 4.2 (a) Block Diagram and (b) Timing Diagram of the Proposed ZCBC

The proposed ZCBC intends to detect the zero-crossing without much overshoot

such that the speed of the residue amplifier can be increased. Fig. 4.2(a) illustrates the block diagram of the proposed ZCBC to improve the speed of the residue amplifier. The proposed idea detects the threshold of the ZCD in the presence of the finite delay from the control logic and the comparator (Comp1). The operation of the proposed technique is done along with the foreground calibration of the ADC.

The working principle is divided into two steps:

i. Coarse threshold tuning

ii. Fine threshold tuning

Coarse Threshold Tuning:

Fig. 4.2(b) illustrates the timing diagram of the proposed ZCBC during step 1, in which the coarse threshold is detected. During Φ_1 phase where the Φ_1 switch is activated, the maximum differential dc voltage is sampled as inputs to the V_{cm}-based SAR ADC. This voltage is selected because the voltage difference between the top plates in the positive DAC (V_p) and minus DAC (V_m) of the V_{cm}-based SAR ADC will be the maximum. Hence, the time taken for V_{in+} and V_{in-} to cross each other will be maximum. During Φ_1 phase, the sampled voltage is converted into a digital format by the V_{cm}-based SAR ADC and fed as input to the ZCD after the Φ_1 phase.

During Φ_{2I} phase, where Φ_{2I} switch is activated, the capacitors (C_{T2_p} and C_{T2_m}) in the second stage V_{cm}-based SAR ADC are in the reset condition. Moreover, during the overlap between the Φ_{2I} and Φ_1 phase capacitors C_1 is in the reset condition. By the end of the Φ_{2I} phase, the residual voltage of the SAR ADC is available as input to the ZCD. The overshoot voltage of the ZCD depends on the signal polarity of the residual voltage (Chang, Wu & Hsieh (2019)). This problem can be circumvented by the knowledge of the last conversion of the SAR ADC. Based on the last conversion one can detect whether V_p is greater than V_m or not. If $V_p > V_m$, then V_p and V_m are connected to V_{in+} and V_{in-}, respectively by activating Φ_{3a} else Φ_{3b} is activated. Hence, V_{in+} is always at higher potential than V_{in-}. This method does not require to level shift the capacitors like in the case of adaptive level shifting (ALS) (Chang et al. (2019)) which reduces the speed of the ADC by utilizing one step to level shift the capacitors.

Once V_{in+} and V_{in-} are connected to the residual voltage, switch S_2 is activated to charge the capacitor C_2 and cal_{co} is activated such that the residual voltage is connected to the comparator (Comp1). Then, E_1 is activated to charge the second stage capacitors of the SAR ADC. Once, the zero-crossing ($V_{in+} = V_{in-}$) is detected,

E_1 and E_2 are deactivated. E_1 and E_2 are deactivated after a finite delay from the comparator and the control logic, therefore, the voltage in the capacitor C_2 needs to be adjusted to incorporate the finite delay from the comparator and the control logic. Hence, the coarse threshold is attained from the above process.

Fine Threshold Tuning

In step 2, the coarse threshold is tuned in a fine manner such that the threshold is adjusted to eliminate delay from the comparator and control logic by the comparator (COMP1). The cal_{co} is deactivated such that the capacitor C_2 is connected to the comparator (Comp1). Fig. 4.2(b) illustrates the timing diagram of step 2. In the next Φ_1 phase, the same differential dc voltage is applied as an input to the V_{cm}-based SAR ADC as in step 1. At the end of the Φ_{2I} phase, the residual voltage of the SAR ADC is connected to the ZCD. Now, the threshold of the comparator (Comp1) is incremented and the comparator (Comp2) (Razavi (2015a)) detects whether V_{in+} is less than V_{in-}. If V_{in+} is less than V_{in-}, then in the next Φ_1 phase the threshold of the comparator (Comp1) is incremented again. The above process continues till V_{in+} is greater than V_{in-}. Once, the threshold is detected for the case when $V_{in+} > V_{in-}$, the threshold of the comparator (Comp1) is decremented once to attain the previous threshold. This will be the threshold of the comparator (Comp1) during the normal operation of the ADC. The reason to choose the threshold value when $V_{in+} < V_{in-}$ is that, during the normal operation of the ADC, there can be cases when the residual voltage is less than the threshold value and these cases will result in wrong results. These cases can be avoided if the threshold value is selected when $V_{in+} < V_{in-}$. The overshoot in the ZCD for the above threshold value acts as an offset that can be adjusted during the post-processing step.

4.1.2.2 Comparator Design

Fig. 4.3 shows the schematic of the static comparator (Comp1). The comparator consists of a pre-amplifier followed by a latch. M_1 and M_2 form the differential pair for the pre-amplifier, M_3 and M_4 form the latch and M_6 to M_n are activated by the switches from S_1 to S_n to increment the threshold of the comparator. While finding the coarse threshold, S_1 is activated and S_2 to S_n are deactivated. During the fine-tuning stage, the threshold is incremented by activating the next switch and deactivating the remaining switches. The width of the transistors from M_6 to M_n are incremented in a binary fashion.

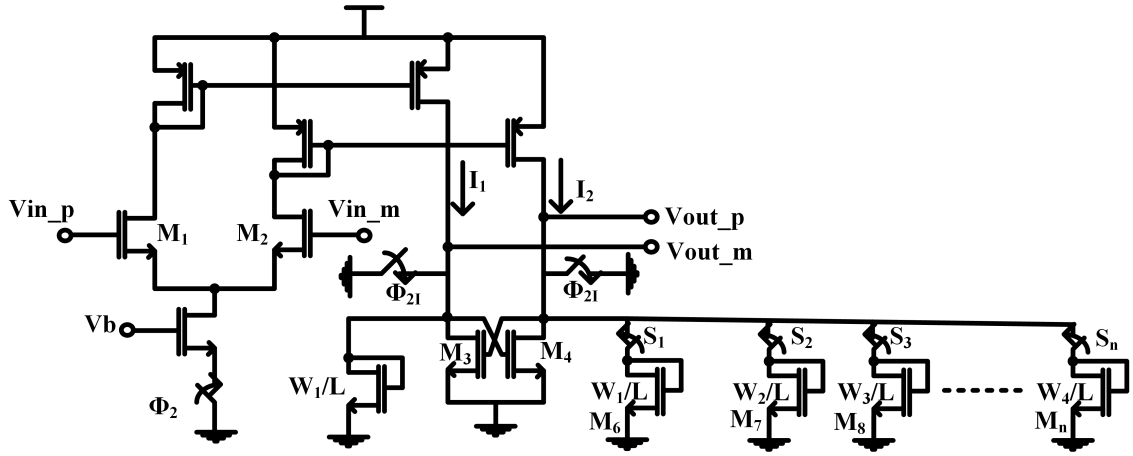


Figure 4.3 Schematic of the Comparator (Comp1)

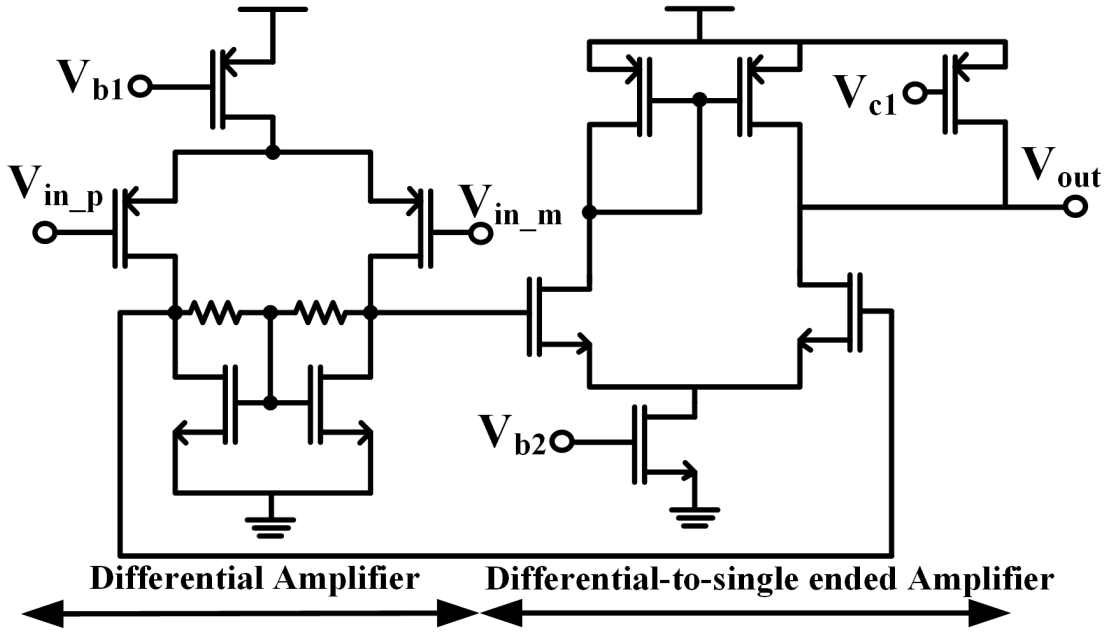


Figure 4.4 Schematic of the ZCD

4.1.2.3 Zero-Crossing Detector (ZCD)

Fig. 4.4 shows the schematic of the ZCD. The ZCD is designed using a differential pre-amplifier and a differential-to-single-ended amplifier to improve the common-mode rejection. A control signal V_{c1} is used to reset the capacitor C_2 before the coarse phase.

4.1.2.4 Manual Current Calibration

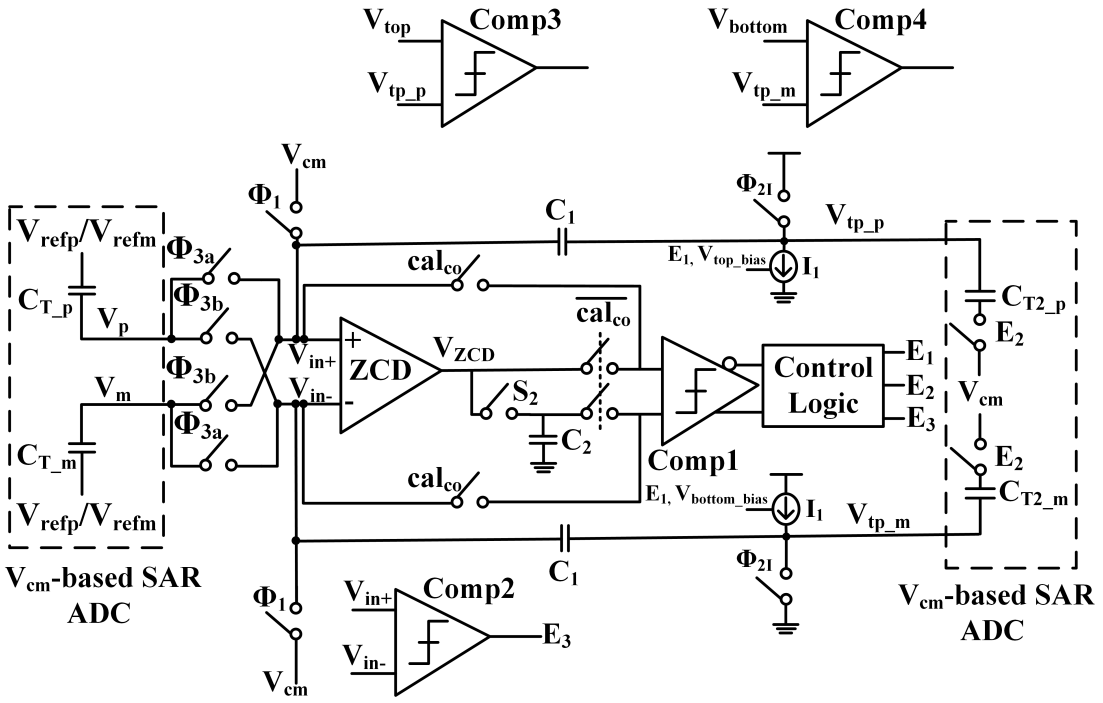


Figure 4.5 Manual Current Calibration

It is required that the current source I_1 in Fig. 4.5 be constant, hence, a manual current calibration technique is performed by Comp3 and Comp4 as shown in Fig. 4.5. Fig. 4.5 shows the circuit for manual current calibration. During the course tuning phase, E_2 acts as the pulse for the comparators: Comp3 and Comp4. V_{top} and V_{bottom} are bias voltages that are given externally such that the sum of V_{top} and V_{bottom} is equal to the supply voltage. V_{top_bias} and V_{bottom_bias} are voltages controlling the current source I_1 connected to the node V_{tp_p} and V_{tp_m}, respectively. The manual current calibration can be understood by the following example. Suppose current I_1 biased using V_{top_bias} has a current mismatch with the current source biased using V_{bottom_bias}, and V_{top} and V_{bottom} are biased with values 0.35 V and 0.85 V, respectively such that the supply voltage is 1.2 V. Due to the current mismatch, the voltage at node V_{tp_p} reaches 0.2 V and the voltage at node V_{tp_m} reaches 0.8 V. Ideally, the voltage at node V_{tp_p} must reaches 0.4 V i.e. supply voltage minus voltage at node V_{tp_m}. This mismatch in the voltage is detected by the comparators: Comp3 and Comp4 and hence, the bias voltage V_{top_bias} is adjusted to reduce the mismatch between the current source I_1 connected to the node V_{tp_p} and V_{tp_m}.

4.1.3 Post-Layout Simulation Results

The proposed residue amplifier based on ZCBC with overshoot reduction technique was implemented in an 8-bit 1-bit/cycle radix-1.793 V_{cm}-based SAR-assisted pipeline ADC that comprises two stages (Kunnatharayil, Gogebakan, Ceylan & Gurbuz (2022)). The first stage consists of a 5b V_{cm}-based SAR ADC with 1b redundancy and the second stage consists of a 4b V_{cm}-based SAR ADC. The radix-1.793 was chosen to address the capacitor mismatch during fabrication (Liu, Huang & Chiu (2011)). Fig. 4.6 shows the layout of the two-stage SAR-assisted pipeline ADC and is designed in 130 nm SiGe BiCMOS technology. The area occupied by the ADC is 0.684 mm^2.

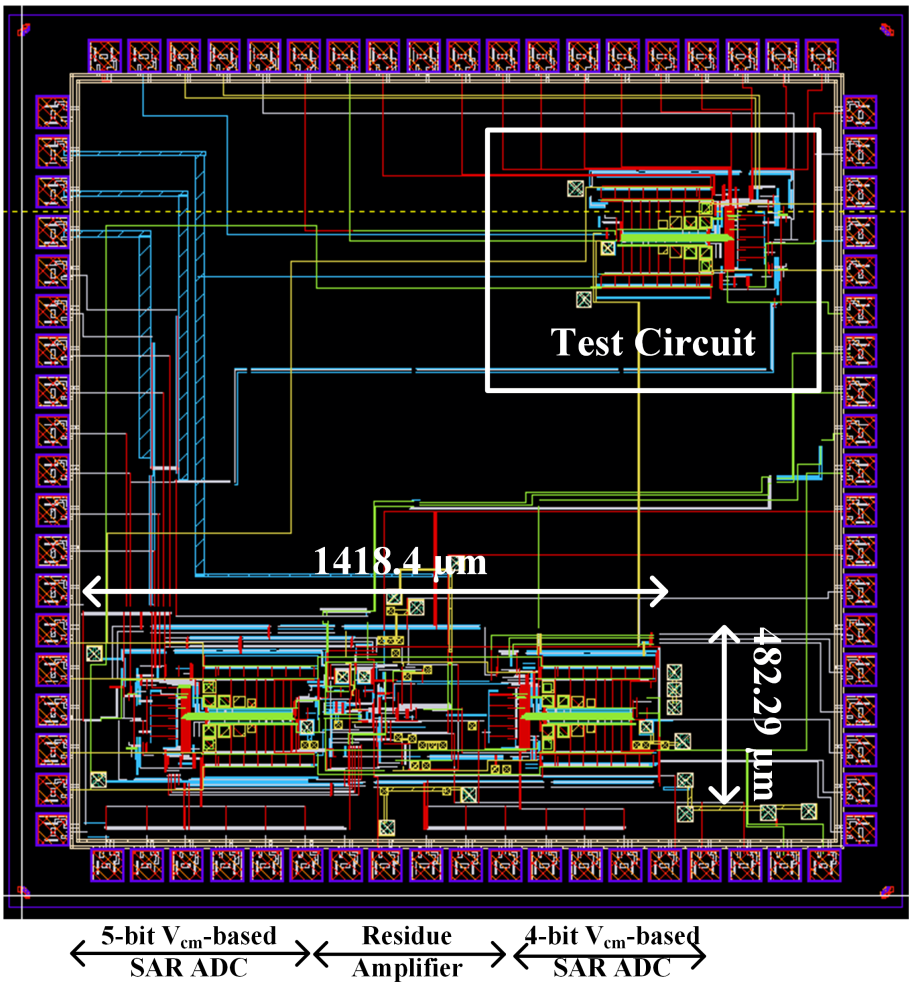


Figure 4.6 Layout of the 8b radix-1.793 V_{cm}-based SAR-assisted two-stage pipeline ADC

Fig. 4.7 shows the simulation waveform of the proposed ZCD in the tt corner case. Zero-crossing 1 is the first amplification of the residue amplifier after determining the coarse threshold. T_{D1} is the time difference when the residual voltage from the SAR

ADC is the input to the ZCD and when the ZCD inputs detect the zero-crossing. T_{D2} is the overshoot time due to the delay from the control logic and comparator. V_{ov1} is the overshoot voltage during zero-crossing 1 and is the difference between V_{cm} and V_{o_p}. In Fig. 4.7, zero-crossing 2 is the stage when the threshold of the comparator has been tuned to detect the zero-crossing in the presence of the artifacts that contribute to overshoot. T_{D3} and V_{ov2} is the overshoot time and overshoot voltage during zero-crossing 2 stage. V_{ov2} is the difference between V_{cm} and V_{o_p1}. Table 4.1 compares the overshoot voltage and the percentage reduction of overshoot time after the threshold has been tuned for different corner cases. During the stage: zero-crossing 1, the T_{D1} and T_{D2} was attained as 1.289 ns and 2.898 ns, respectively. Therefore, the total time for amplification was attained as 4.187 ns (T_{D1} + T_{D2}). After the threshold of the comparator was tuned, the maximum and minimum time for amplification was 1.59 ns and 1.34 ns, respectively, as shown in table 4.1. Moreover, the maximum and minimum percentage reduction in the overshoot time was attained as 95.68% and 76.57%, respectively. The maximum and minimum overshoot voltage after fining tuning the threshold were attained as 2.8 mV and 2.1 mV, respectively.

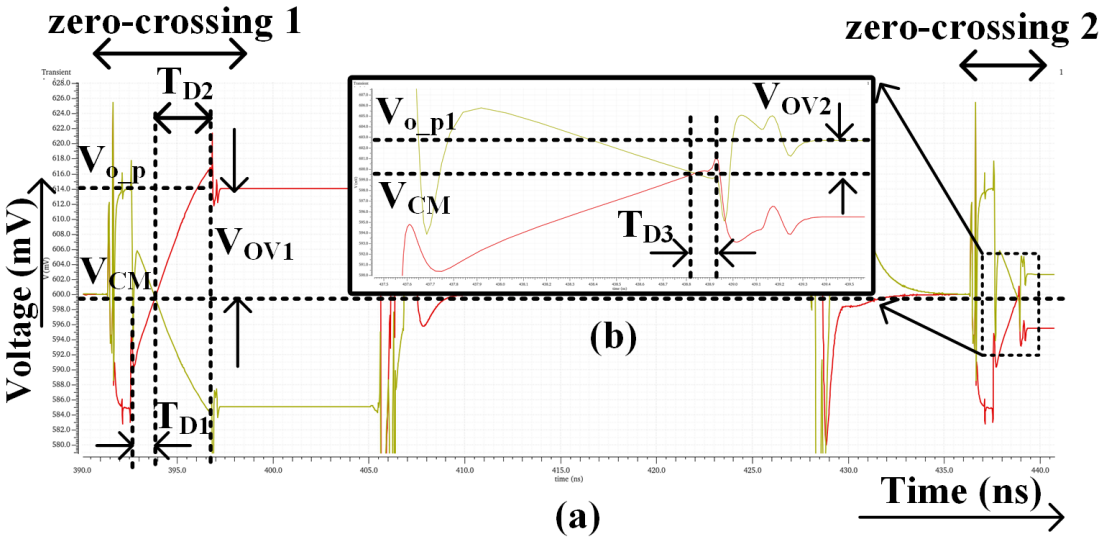
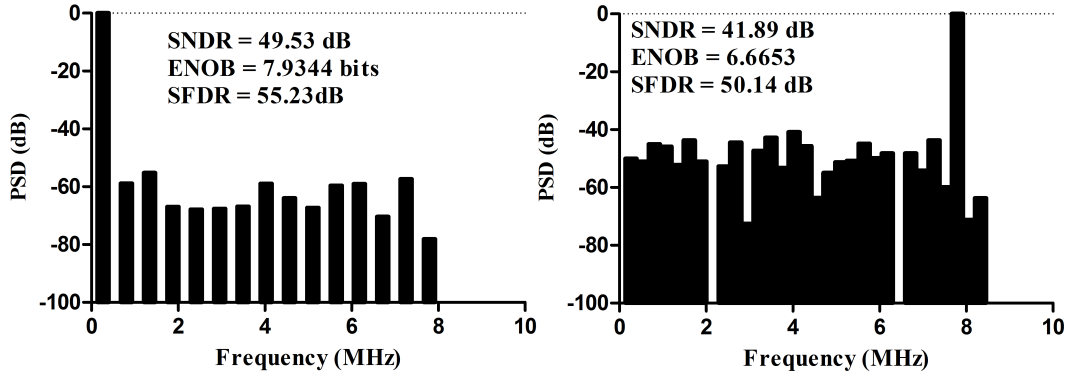


Figure 4.7 (a) Simulation waveform of the proposed ZCD and (b) zoom-view of the zero-crossing detection in the tt corner case

Table 4.2 shows the post-layout performance summary. Table 4.3 compares the performance parameters with state-of-art works (Hershberg, Weaver & Moon (2010); Shin et al. (2014); Tang & Pun (2012)). It can be observed that the two-step technique has an overshoot voltage range of 2.1 mV to 2.8 mV with an improved amplification time from 1.34 ns to 1.59 ns compared to the other works. The proposed two-step technique is implemented in an 8-bit radix-1.793 SAR-assisted two-stage pipeline ADC. The performance parameters of the ADC are shown in table 4.3.

Table 4.1 Comparison of Overshoot voltage and Percentage Reduction of Overshoot Time after fine-tuning the threshold for different Corner Cases

	Corner Cases				
	tt	***ss***	***fs***	***ff***	***sf***
V_{ov2} (mV)	2.1	2.3	2.4	2.8	2.2
T_{D3} (ps)	55.58	74.78	253.8	301.97	60.79
% reduction of Overshoot time ((T_{D2} - T_{D3})/(T_{D2})) x100	95.68	94.2	80.30	76.57	95.28
Total time for Amplification (ns)	1.34	1.36	1.54	1.59	1.35



(a) (b)

Figure 4.8 Post-layout simulation at an input frequency of (a) 520.83 kHz and (b) at near Nyquist frequency of 7.5521 MHz

The SAR-assisted pipeline ADC achieves an ENOB of 7.9344 bits and 6.6653 bits that corresponds to an SNDR of 49.53 dB and 41.89 dB with an input frequency of 520.83 kHz and at Nyquist rate of 7.5521 MHz, respectively with a sampling frequency of 16 MS/s. Fig. 4.8 represents the post-layout simulated FFT spectrum at an input frequency of 520.83 kHz and at Nyquist rate of 7.5521 MHz with a sampling frequency of 16 MS/s. Fig. 4.9(a) shows the post-layout SNDR and SFDR at different input frequencies for the sampling frequency of 16 MS/s. Fig. 4.9(b) shows the post-layout ENOB at different input frequency for the sampling frequency of 16 MS/s. Fig. 4.10 shows the INL and DNL.

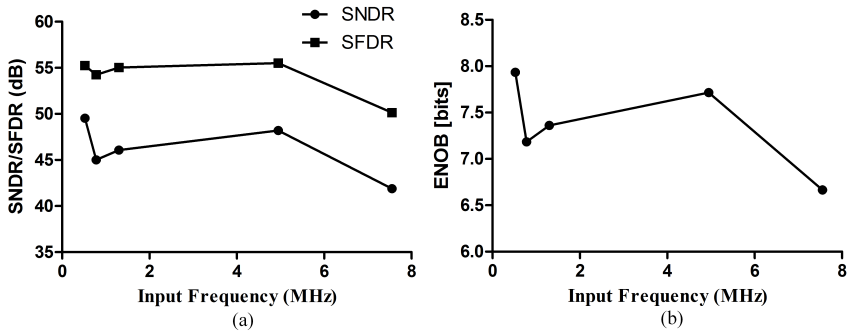


Figure 4.9 Post-layout (a) SNDR and SFDR (b) and ENOB for different input frequencies at a sampling frequency of 16 MS/s

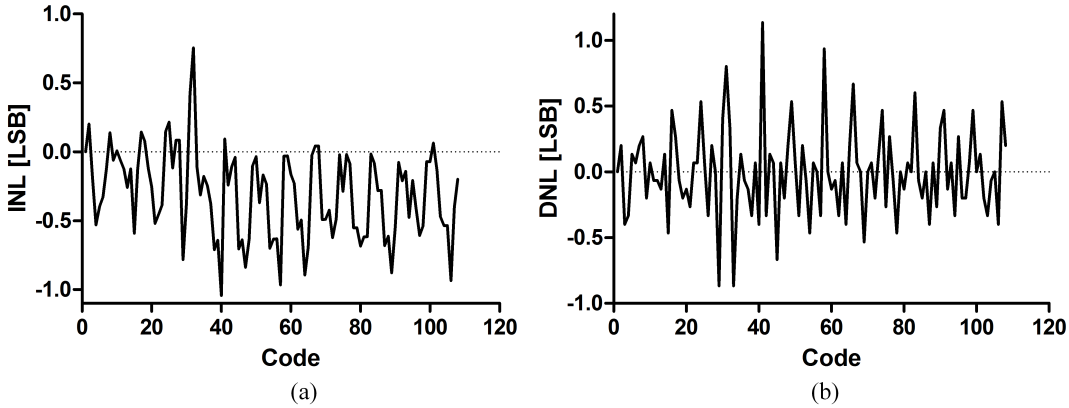


Figure 4.10 INL and DNL

Table 4.2
Post-Layout Performance Summary

Process [nm]	130
Supply Voltage [V]	1.2
Resolution [bit]	8
Sampling Rate [MS/s]	16
SNDR @ 520.83 kHz input [dB]	49.53
SFDR @ 520.83 kHz input [dB]	55.23
ENOB @ 520.83 kHz input [bits]	7.9344
SNDR @ Nyq [dB]	41.89
SFDR @ Nyq [dB]	50.14
ENOB @ Nyq [bits]	6.6653
DNL [LSB]	-0.86/1.13
INL [LSB]	-1.043/0.75
Power [mW]	1*
FoM_W @ Nyq [fJ/conversion-step]	615.77

*Power of the core ADC

Table 4.3 Performance Summary and Comparison

	This work (Kunnatharayil) (2022)	**Shin (2014)**	**Tang 2012**	**Hershberg 2010**
Architecture	Pipeline-SAR	Pipeline	Pipeline	Pipeline
Technology [nm]	130	55	180	180
Amplification Time (ns)	**1.34 - 1.59**	1.36	-	7
Overshoot Time (ps)	**55.58**	71.4-107.1	-	410
Overshoot Voltage (mV)	**2.1 - 2.8**	30	5	-
Supply Voltage [V]	1.2	1.1	1.8	1.8
Sampling Rate[MS/s]	16	200	20	20
SNDR [dB]	49.53	64.4	57.2	68.3
SFDR [dB]	55.23	82.9	66.8	76.3
ENOB [bit]	7.9344	10.44	9.2	11.1
DNL [LSB]	-0.86/1.13	-0.28/0.24	-0.6/0.31	-0.7/0.9
INL [LSB]	-1.043/0.75	-1.89/1.36	-0.99/0.41	-0.8/1
Total Power (mW)	1*	30.7	2.6	17.2
FoM_W [fJ/conversion-step] (at low frequency)	255	111	221	405.5

*Power of the core ADC

5. 2-bit/cycle sub-radix SAR-Assisted Pipeline ADC with an Improved Overshoot Reduction Technique

From chapter 4, the post-layout specification of the 1-bit/cycle sub-radix V_{cm}-based SAR-assisted pipeline ADC achieves an ENOB 6.6653 bits at a near Nyquist rate of 7.5521 MHz with a sampling frequency of 16 MS/s. This specification has not reached the required ADC specification. Therefore, to increase the speed of the SAR ADC, a 2-bit/cycle SAR ADC was implemented. This chapter is divided into two sections. The first section describes the 2-bit/cycle SAR ADC and using the aforementioned architecture in the SAR ADC, a single-channel ADC is designed using a 2-bit/cycle sub-radix V_{cm}-based SAR-assisted pipeline. Then, the post-layout simulations are described. In the second section, the overshoot reduction technique is improved and is implemented in the 2-bit/cycle sub-radix V_{cm}-based SAR-assisted pipeline ADC, and finally, the post-layout results are explained.

5.1 2-bit/cycle SAR ADC based on V_{cm} technique

Fig. 5.1 shows the architecture of a 7-bit 2-bit/cycle SAR ADC based on V_{cm} technique. The 2-bit/cycle SAR ADC (Song, Tang & Sun (2017)) was designed using V_{cm} technique to reduce the MSB capacitor when compared to the conventional technique (Liu, Chang, Huang & Lin (2010)) and hence, reducing the area. C_u is the unit capacitor.

Fig. 5.2 describes the working principle of a 2-bit/cycle SAR ADC based on V_{cm} technique with a differential dc input. During the sampling phase (step 1) the differential inputs (V_{inp} and V_{inm}) are connected to the top plates of the capacitors. Let V_{inp} be connected to differential dc input of 1.16 V and V_{inm} is connected to 0.04 V. The input range of the SAR ADC is from 0 to 1.2 V. Hence, V_{refp} is 1.2 V, V_{refm} is 0 V and V_{cm} is 0.6 V . The bottom plates of the capacitors are connected

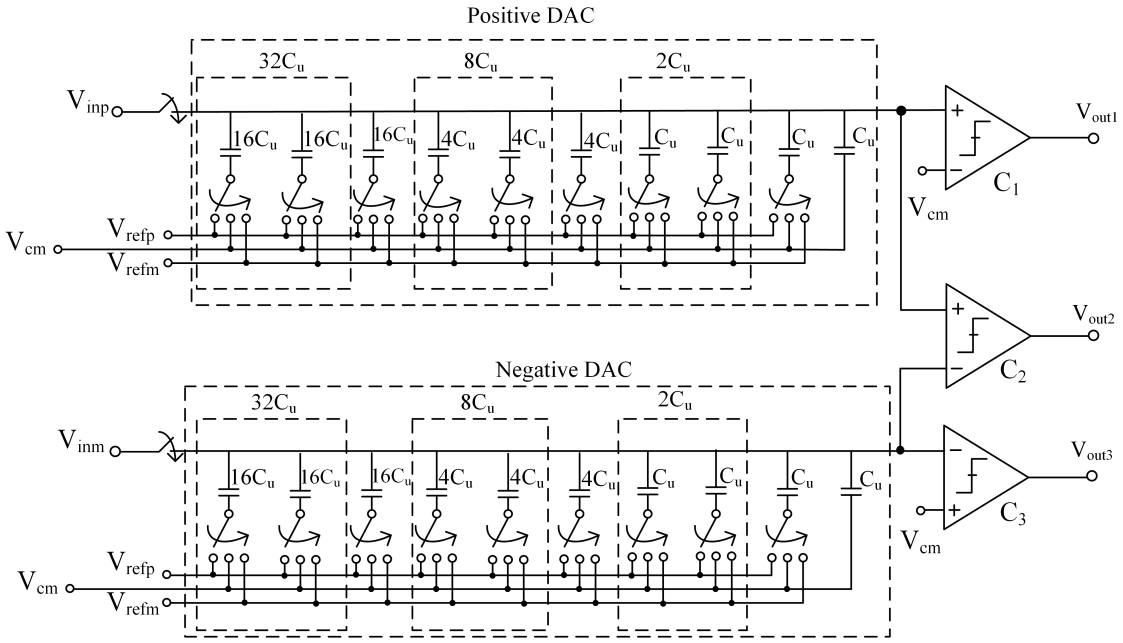


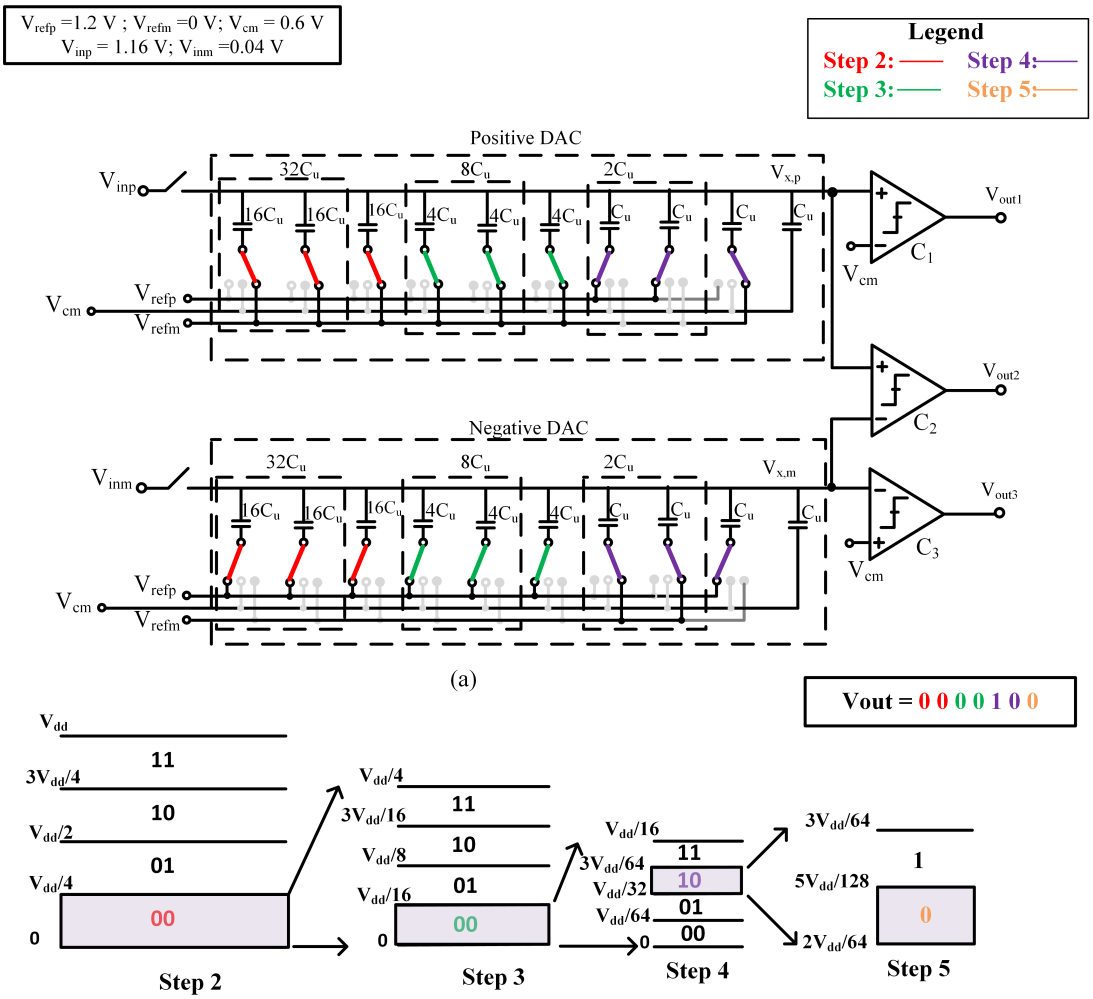
Figure 5.1 Schematic of a 7-bit 2-bit/cycle SAR ADC based on V_{cm} technique

to V_{cm}. Therefore, the charge stored in the capacitors in the positive ($Q_{sampling,p}$) and negative DAC ($Q_{sampling,m}$) are expressed as (5.1). In step 2, the bottom plates of the MSB capacitors in the positive and negative DAC i.e. $32C_u$ are connected to V_{refp}. Based on the principle of conservation of charge, the voltages at the top plates of the capacitors in the positive and negative DAC can be computed. If $V_{x,p}$ is the voltage on the top plates of the capacitors in the positive DAC then the charge in the capacitors can be expressed as (5.2). Then by conservation of charge principle, the voltage at $V_{x,p}$ can be computed as expressed in (5.3).

$$\begin{aligned} Q_{\text{sampling,p}} &= (V_{\text{in,p}} - V_{\text{cm}})64C_{\text{u}} \\ Q_{\text{sampling,m}} &= (V_{\text{in,m}} - V_{\text{cm}})64C_{\text{u}} \end{aligned} \tag{5.1}$$

$$Q_{\text{step2,p}} = (V_{\text{x,p}} - V_{\text{ref,p}})32C_{\text{u}} + (V_{\text{x,p}} - V_{\text{cm}})32C_{\text{u}} \tag{5.2}$$

$$\begin{aligned} Q_{\text{sampling,p}} &= Q_{\text{step2,p}} \\ V_{\text{x,p}} &= V_{\text{in,p}} + \frac{V_{\text{cm}}}{2} \\ V_{\text{x,p}} &= 1.46V \end{aligned} \tag{5.3}$$



(a)

(b)

Implementation Algorithm w.r.t V_{inp}	
$V_{out1}: V_{inp} + V_{cm}/2 > V_{cm}$	$\Rightarrow V_{inp} > V_{refp}/4$
$V_{out2}: V_{inp} + V_{cm}/2 > V_{inm} + V_{cm}/2$	$\Rightarrow V_{inp} > V_{refp}/2$
$V_{out3}: V_{cm} > V_{cm}/2 + V_{inm}$	$\Rightarrow V_{inp} > 3V_{refp}/4$

(c)

V_{out1}	V_{out2}	V_{out3}	Switches connected to positive DAC
1	1	1	00
1	1	0	01
1	0	0	10
0	0	0	11

(e)

Implementation Algorithm w.r.t V_{inm}	
$V_{out1}: V_{inp} + V_{cm}/2 > V_{cm}$	$\Rightarrow V_{inm} < 3V_{refp}/4$
$V_{out2}: V_{inp} + V_{cm}/2 > V_{inm} + V_{cm}/2$	$\Rightarrow V_{inm} < V_{refp}/2$
$V_{out3}: V_{cm} > V_{cm}/2 + V_{inm}$	$\Rightarrow V_{inp} < V_{refp}/4$

(d)

V_{out1}	V_{out2}	V_{out3}	Switches connected to negative DAC
1	1	1	11
1	1	0	10
1	0	0	01
0	0	0	00

(f)

Figure 5.2 (a) Schematic of the 7-bit 2-bit/cycle SAR ADC based on V_{cm} technique (b) Conversion algorithm in terms of digital output (c) Implementation algorithm w.r.t V_{inp} (d) Implementation algorithm w.r.t V_{inm} (e) Switch connection to the positive DAC (f) Switch connection to the negative DAC based

Similarly, if $V_{x,m}$ is the voltage on the top plates of the capacitors in the negative DAC then the charge in the capacitors can be expressed as (5.4). Then by conservation of charge principle, the voltage at $V_{x,m}$ can be computed as expressed in (5.5).

$$Q_{\text{step2,m}} = (V_{\text{x,m}} - V_{\text{ref,p}})32C_{\text{u}} + (V_{\text{x,m}} - V_{\text{cm}})32C_{\text{u}} \tag{5.4}$$

$$\begin{aligned} Q_{\text{sampling,m}} &= Q_{\text{step2,m}} \\ V_{\text{x,m}} &= V_{\text{in,m}} + \frac{V_{\text{cm}}}{2} \\ V_{\text{x,m}} &= 0.34V \end{aligned} \tag{5.5}$$

Based on (5.3) and (5.5) V_{out1} is '1' as the positive terminal of the comparator (C_1) is greater than the negative terminal of the comparator (C_1). Similarly, V_{out2} and V_{out3} are also '1'.

According to the outputs from V_{out1}, V_{out2}, V_{out3}, the switches to the positive and negative DAC are connected as shown in 5.2 highlighted in red as step 2. In Fig. 5.2(c) and (d) shows the implementation algorithm to connect the switches to the bottom plates of the positive and negative DAC based on the outputs from V_{out1}, V_{out2}, V_{out3} w.r.t V_{inp} and V_{inm}, respectively. In Fig. 5.2(e) and (f) describe the switch connections to the bottom plate of the positive and negative DAC, respectively, based on the output of V_{out1}, V_{out2}, V_{out3}. In Fig. 5.2(b), the text written in red shows the digital code after the step 2.

During step 3, the bottom plates of the last three capacitors are connected to the appropriate voltages based on the output in step 2. Then, the $8C_u$ capacitors in the positive and negative DAC are connected to V_{refp}. The charge stored in the capacitors in the positive ($Q_{step3,p}$) DAC is expressed as (5.6). Based on conservation of charge principle, $Q_{step3,p}$ will be equal to $Q_{sampling,p}$, as expressed in (5.7).

$$Q_{\text{step3,p}} = (V_{\text{x,p}} - V_{\text{ref,m}})48C_{\text{u}} + (V_{\text{x,p}} - V_{\text{ref,p}})8C_{\text{u}} + (V_{\text{x,p}} - V_{\text{cm}})8C_{\text{u}} \tag{5.6}$$

$$
\begin{aligned}
Q_{\text{sampling,p}} &= Q_{\text{step3,p}} \\
V_{\text{x,p}} &= V_{\text{in,p}} - V_{\text{cm}} + \frac{8V_{\text{cm}}}{64} + \frac{8V_{\text{refp}}}{64} \\
V_{\text{x,p}} &= 0.785V
\end{aligned}
\tag{5.7}
$$

Similarly, the charge in negative DAC can be expressed as (5.8), and by conservation of charge principle, $Q_{\text{step3,m}}$ will be equal to $Q_{\text{sampling,p}}$, as expressed in (5.9).

$$
Q_{\text{step3,m}} = (V_{\text{x,m}} - V_{\text{ref,p}})48C_{\text{u}} + (V_{\text{x,m}} - V_{\text{ref,p}})8C_{\text{u}} + (V_{\text{x,m}} - V_{\text{cm}})8C_{\text{u}} \tag{5.8}
$$

$$
\begin{aligned}
Q_{\text{sampling,m}} &= Q_{\text{step3,m}} \\
V_{\text{x,m}} &= V_{\text{in,m}} - V_{\text{cm}} + \frac{8V_{\text{cm}}}{64} + \frac{56V_{\text{refp}}}{64} \\
V_{\text{x,p}} &= 0.565V
\end{aligned}
\tag{5.9}
$$

According to the voltage attained at $V_{x,p}$ and $V_{x,m}$, the output logic at V_{out1}, V_{out2} and V_{out3} are '1'. Hence, the switches are connected to the bottom plates of the capacitors in the positive and negative DAC based on Fig. 5.2(e) and (f), respectively. In Fig. 5.2(b) the text highlighted in green shows the digital code after the step 3.

In step 4, the bottom plates are connected of the positive and negative DAC are connected based on the results of step 3. The charge stored in the capacitors in the positive ($Q_{step4,p}$) DAC is expressed as (5.10). Based on conservation of charge principle, $Q_{step4,p}$ will be equal to $Q_{sampling,p}$, as expressed in (5.11).

$$
Q_{\text{step4,p}} = (V_{\text{x,p}} - V_{\text{ref,m}})60C_{\text{u}} + (V_{\text{x,p}} - V_{\text{ref,p}})2C_{\text{u}} + (V_{\text{x,p}} - V_{\text{cm}})2C_{\text{u}} \tag{5.10}
$$

$$
\begin{aligned}
Q_{\text{sampling,p}} &= Q_{\text{step4,p}} \\
V_{\text{x,p}} &= V_{\text{in,p}} - V_{\text{cm}} + \frac{2V_{\text{cm}}}{64} + \frac{2V_{\text{refp}}}{64} \\
V_{\text{x,p}} &= 0.61625V
\end{aligned}
\tag{5.11}
$$

Similarly, the charge stored in the capacitors in the negative ($Q_{step4,m}$) DAC is expressed as (5.12). Based on conservation of charge principle, $Q_{step4,m}$ will be equal to $Q_{sampling,m}$, as expressed in (5.13).

$$
Q_{\text{step4,m}} = (V_{\text{x,m}} - V_{\text{ref,p}})60C_{\text{u}} + (V_{\text{x,m}} - V_{\text{ref,p}})2C_{\text{u}} + (V_{\text{x,m}} - V_{\text{cm}})2C_{\text{u}} \tag{5.12}
$$

$$
\begin{aligned}
Q_{\text{sampling,m}} &= Q_{\text{step4,m}} \\
V_{\text{x,m}} &= V_{\text{in,m}} - V_{\text{cm}} + \frac{2V_{\text{cm}}}{64} + \frac{62V_{\text{refp}}}{64} \\
V_{\text{x,p}} &= 0.62125V
\end{aligned}
\tag{5.13}
$$

According to the voltage attained at $V_{x,p}$ and $V_{x,m}$, the output logic at V_{out1}, V_{out2} and V_{out3} are '1', '0' and '0', respectively. Hence, the switch connections to the bottom plates of the capacitors in the positive and negative DAC are shown in violet. In Fig. 5.2(b), the text in violet shows the digital code after the step 4.

In step 5, the bottom plates are connected to the positive and negative DAC are connected based on the results from step 4. The charge stored in the capacitors in the positive ($Q_{step5,p}$) DAC is expressed as (5.14). Based on conservation of charge principle, $Q_{step5,p}$ will be equal to $Q_{sampling,p}$, as expressed in (5.15).

$$
Q_{\text{step5,p}} = (V_{\text{x,p}} - V_{\text{ref,m}})61C_{\text{u}} + (V_{\text{x,p}} - V_{\text{ref,p}})2C_{\text{u}} + (V_{\text{x,p}} - V_{\text{cm}})C_{\text{u}} \tag{5.14}
$$

$$
\begin{aligned}
Q_{\text{sampling,p}} &= Q_{\text{step5,p}} \\
V_{\text{x,p}} &= V_{\text{in,p}} - V_{\text{cm}} + \frac{1V_{\text{cm}}}{64} + \frac{2V_{\text{refp}}}{64} \\
V_{\text{x,p}} &= 0.606875V
\end{aligned}
\tag{5.15}
$$

Similarly, the charge stored in the capacitors in the negative ($Q_{step5,m}$) DAC is expressed as (5.16). Based on conservation of charge principle, $Q_{step5,m}$ will be equal to $Q_{sampling,m}$, as expressed in (5.17).

$$
Q_{\text{step5,m}} = (V_{\text{x,m}} - V_{\text{ref,p}})61C_{\text{u}} + (V_{\text{x,m}} - V_{\text{ref,m}})2C_{\text{u}} + (V_{\text{x,m}} - V_{\text{cm}})1C_{\text{u}} \tag{5.16}
$$

$$
\begin{aligned}
Q_{\text{sampling,m}} &= Q_{\text{step5,m}} \\
V_{\text{x,m}} &= V_{\text{in,m}} - V_{\text{cm}} + \frac{1V_{\text{cm}}}{64} + \frac{61V_{\text{refp}}}{64} \\
V_{\text{x,p}} &= 0.593125V
\end{aligned}
\tag{5.17}
$$

According to the voltage attained at $V_{x,p}$ and $V_{x,m}$, the output logic at V_{out2} is '1'. In Fig. 5.2(b), the text in orange colour shows the digital code after the step 5.

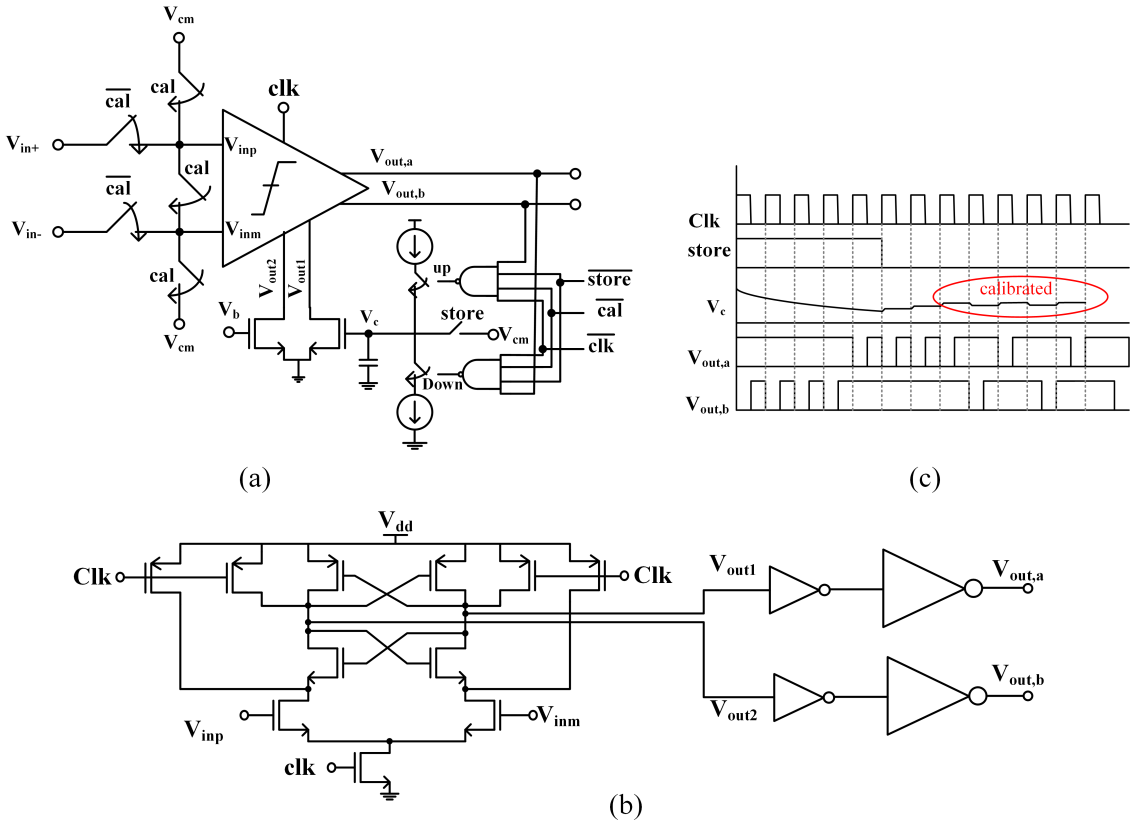


Figure 5.3 (a) Block diagram of the comparator with calibration (b) Schematic of the comparator (c) Timing diagram of the comparator with calibration

5.1.1 Error Sources

The SAR ADC is subjected to two types of error sources: Static and Dynamic error sources.

5.1.1.1 Static Error

The static error sources arise from DAC mismatch and comparator offset.

Comparator offset:

Comparator offset arises due to transistor mismatch. One of the techniques to reduce offset voltage is to use a pre-amplifier before the comparator. This technique requires a high voltage gain amplifier that dissipates large power. In this work, a self-calibrating design proposed by (Miyahara, Asada, Paik & Matsuzawa (2008)) was implemented along with the StrongARM latch (Razavi (2015b)).

Fig. 5.3(a) shows the block diagram of the comparator along with the calibration circuit used (Kunnatharayil, Abbasi, Ceylan & Gurbuz (2021)). Fig. 5.3(b) describes the schematic of the StrongARM latch, and Fig. 5.3(c) shows the timing diagram of the comparator along with the calibration circuit.

Capacitor Mismatch in the DAC:

Random process variation creates capacitor mismatch. The blackline in Fig. 5.4 shows the transfer curve when there is no capacitor mismatch and the red line shows when there is a capacitor mismatch. It can be observed due to the capacitor mismatch the differential nonlinearity (DNL) and the integral nonlinearity (INL) will arise due to missing codes and non-uniform width.

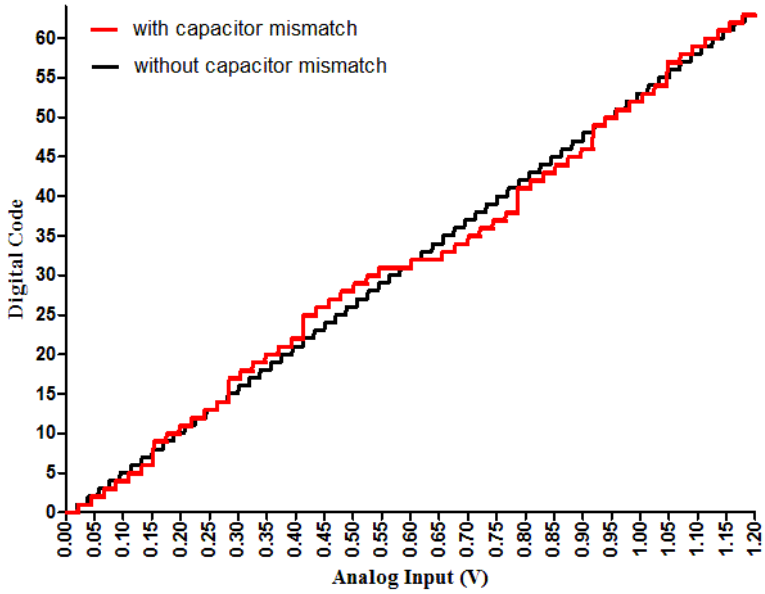


Figure 5.4 Transfer curve showing with and without capacitor mismatch

A common technique is to design the DAC array using the common-centroid technique (Verma & Chandrakasan (2007)) . In this work, a sub-radix approach (Liu, Huang & Chiu (2010)) is used as this technique uses a digital calibration which gives the designer flexibility during the measurement. Based on the mismatch from the technology, a 5 % mismatch is taken. A MATLAB code was written to simulate the exact algorithm to be implemented in Cadence based on (Liu et al. (2010)). In this example, a 1.92 radix V_{cm} based SAR ADC having 5.4967 bits at a sampling frequency of 111.1 MS/s and an input frequency of 1.7361 MHz was simulated in MATLAB. As seen in Fig. 5.5(a) show an ENOB of 5.4947 when there is no capacitor mismatch with a radix of 1.92. Fig. 5.4(b) shows an ENOB of 5.2028 when there is a capacitor mismatch and Fig. 5.4(c) shows when the capacitor mismatch was calibrated using the LMS algorithm. The ENOB was attained as 5.4438 bits

which are close to the ideal case.

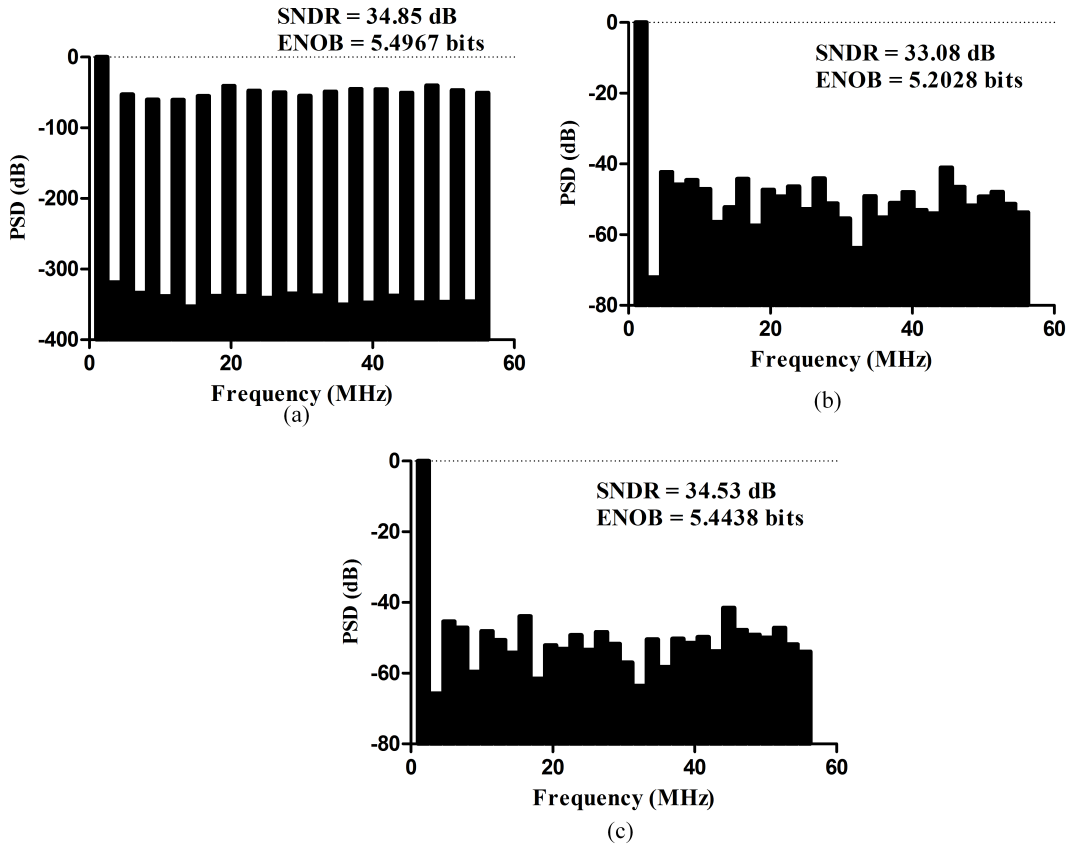


Figure 5.5 FFT plot of (a) an ideal (b) with capacitor mismatch (c) calibrated in the presence of capacitor mismatch for a 5.4967-bits 1.92 radix V_{cm} based SAR ADC

5.1.1.2 Dynamic Error

There are two types of dynamic errors. Firstly, in Fig. 5.2 the node $V_{x,p}$ and $V_{x,m}$ was assumed that the voltage change occurs abruptly. However, the voltage at these nodes settles gradually based on the on-resistance (R_{on}) of the switches in the bottom plate of the positive and negative DAC (McCreary & Gray (1975)). For an N-bit resolution SAR ADC, the settling time is attained as

$$t \geq \tau ln(2^{N+1}) \tag{5.18}$$

where τ is the time constant defined by R_{on} and the effective capacitance seen by the switch. This effect is mitigated by providing enough time to settle at the expense of speed.

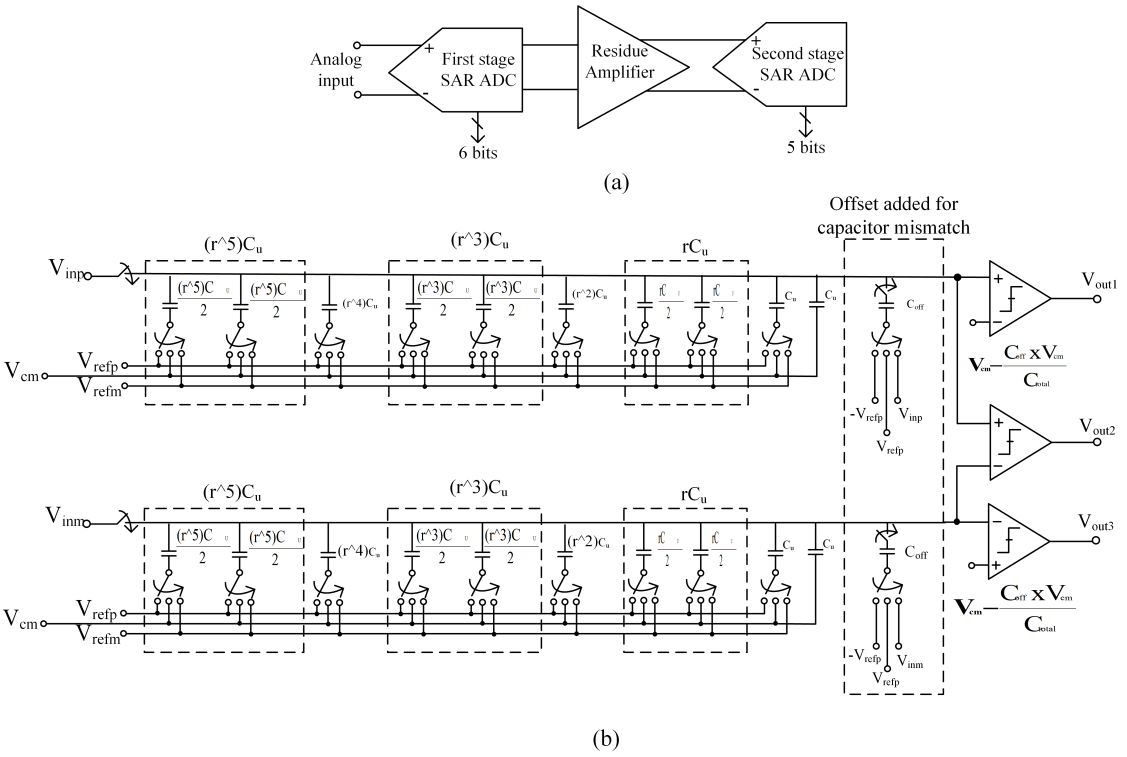


Figure 5.6 (a) Block diagram of the Single-Channel SAR-Assisted Pipeline ADC (b) Schematic of the SAR ADC

Second dynamic error arises due to the switching of the bottom plates from V_{cm} to V_{refp} or V_{refm}. This creates a current flow through the wire bond of the package and then to the switches. This effect can be mitigated by using on-chip reference buffers.

5.1.2 Architecture of the Single-Channel SAR-Assisted Pipeline ADC

The single-channel SAR ADC comprises a 6-bit first stage SAR ADC with one-bit redundancy followed by a residue amplifier, and then the second stage SAR ADC comprising of 5 bits. The SAR ADC of the first and second stages are designed based on a 2-bit/cycle with a sub-radix technique for capacitor mismatch calibration. The SAR ADC also incorporates the comparator offset. Fig. 5.6(a) shows the block diagram of the Single-Channel SAR-Assisted Pipeline ADC, and Fig. 5.6(b) describes the schematic of the 2-bit/cycle sub-radix V_{cm}-based SAR ADC.

5.1.3 Post-layout and Simulation Results

Fig. 5.7 shows the layout of the 10-bit 2-bit/cycle radix-1.97 two-stage SAR-assisted pipeline ADC and is designed in 130 nm SiGe BiCMOS technology. The residue amplifier is designed using the overshoot reduction technique in chapter 4. The active area occupied by the ADC is 1.634 mm^2.

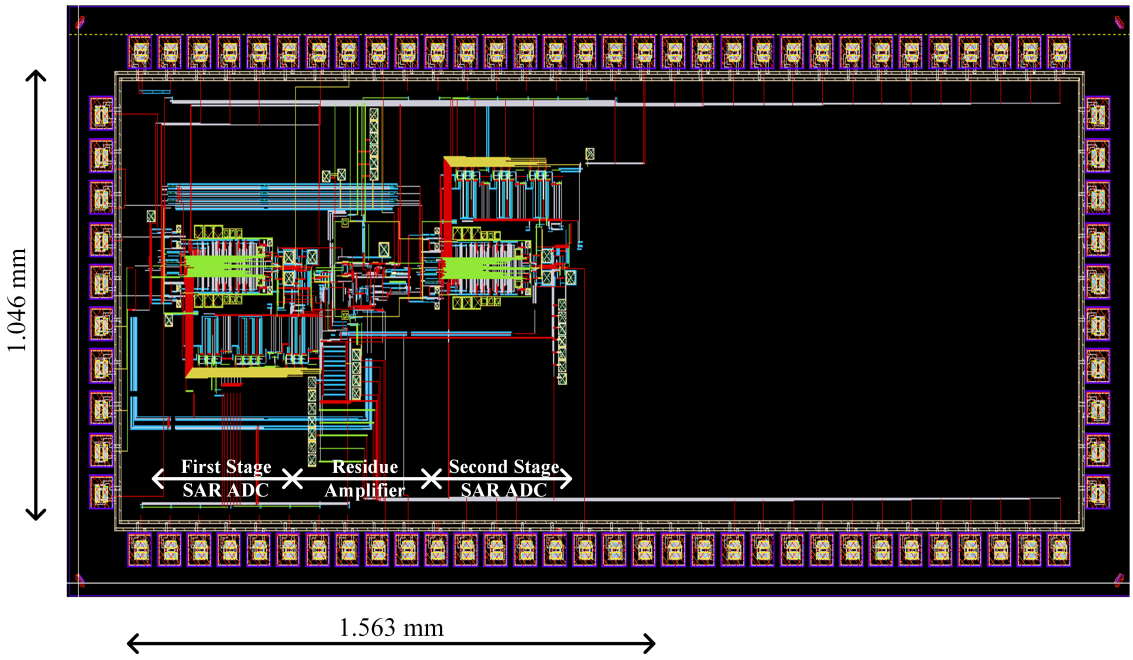


Figure 5.7 Layout of the 10-bit radix 1.97 V_{cm} based SAR-assisted two-stage pipeline ADC

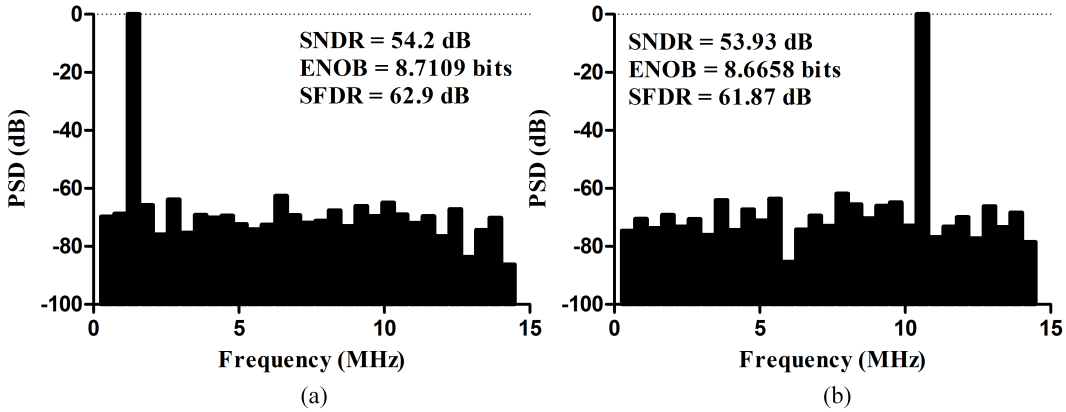
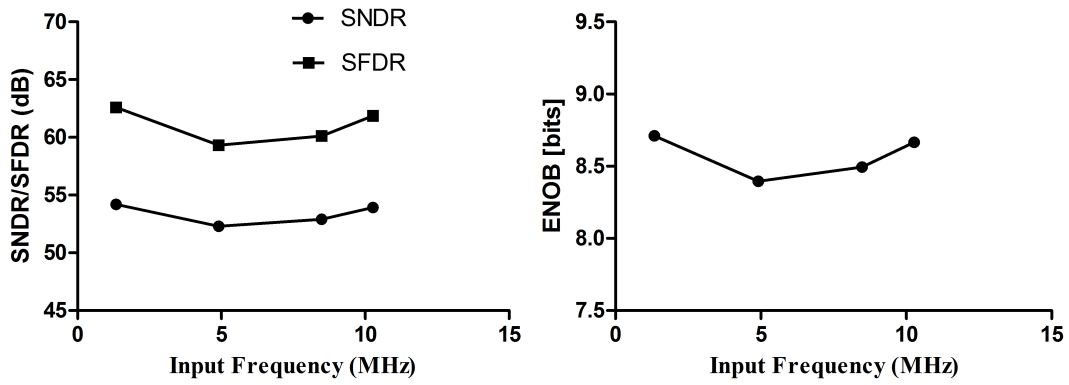


Figure 5.8 Post-layout simulation at an input frequency of (a) 1.3393 MHz and (b) at near Nyquist frequency of 10.268 MHz

Fig. 5.8 (a) shows the post-layout SNDR, SFDR, and ENOB of 54.2 dB, 62.9 dB, and 8.7109 bits, respectively at an input frequency of 1.3393 MHz with a sampling speed of 28.571 MS/s for the SAR ADC. Fig. 5.8 (b) shows the post-layout SNDR,



(a) (b)

Figure 5.9 Post-layout (a) SNDR and SFDR (b) and ENOB for different input frequencies at a sampling frequency of 28.571 MS/s

SFDR, and ENOB of 53.93 dB, 61.87 dB, and 8.6658 bits, respectively with a sampling speed of 28.571 MHz at near Nyquist frequency of 10.268 MHz. Fig. 5.9(a) shows the post-layout SNDR and SFDR at different input frequency for the sampling frequency of 28.571 MS/s. Fig. 5.9(b) shows the post-layout ENOB at different input frequencies for the sampling frequency of 28.571 MS/s. The INL and DNL are attained as +1.7067/-2.2149 LSB and +1.2867/-0.7459 LSB, respectively, as shown in Fig. 5.10. Table 5.1 shows the performance parameters of the ADC.

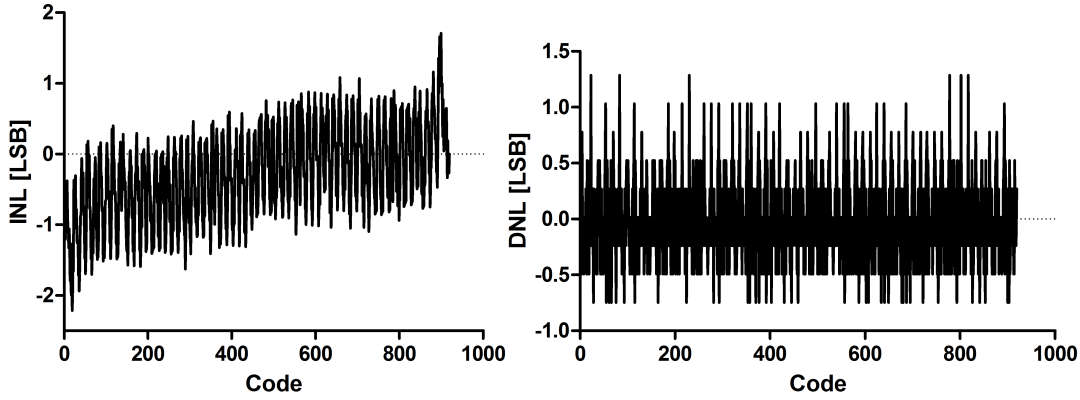


Figure 5.10 Post-layout INL and DNL

Table 5.1
Post-Layout Performance Summary

Process [nm]	130
Supply Voltage [V]	1.2
Resolution [bit]	10
Sampling Rate [MS/s]	28.571
SNDR @ 1.3393 MHz input [dB]	54.2
SFDR @ 1.3393 MHz input [dB]	62.9
ENOB @ 1.3393 MHz input [bits]	8.7109
SNDR @ Nyq [dB]	53.93
SFDR @ Nyq [dBc]	61.87
ENOB @ Nyq [bits]	8.6658
DNL [LSB] INL [LSB]	+1.2867/-0.7459 +1.7067/-2.2149
Power [mW]	1.157
FoM_W @ Nyq [fJ/conversion-step]	99.710

5.2 Improved Version of the Overshoot Reduction Technique

5.2.1 Overshoot Reduction Technique

As observed in Table 4.1, the difference in time taken to overshoot(T_{D3}) between the tt (typical typical) and ff (fast fast) corner case is 246.39 ps, which implies that as the magnitude of the current sources increases the comparator cannot detect the zero-crossing easily because of the slow nature of the comparator. Hence, the comparator designed has been changed to detect a larger magnitude change of current. In this section, the improved version of the reduced overshoot is implemented with the 2-bit/cycle sub- radix V_{cm}-based SAR ADC.

As discussed in 4.1.2.1, the proposed technique is divided into two steps that are as follows:

i. Coarse threshold tuning

ii. Fine threshold tuning

5.2.1.1 Coarse Threshold Tuning

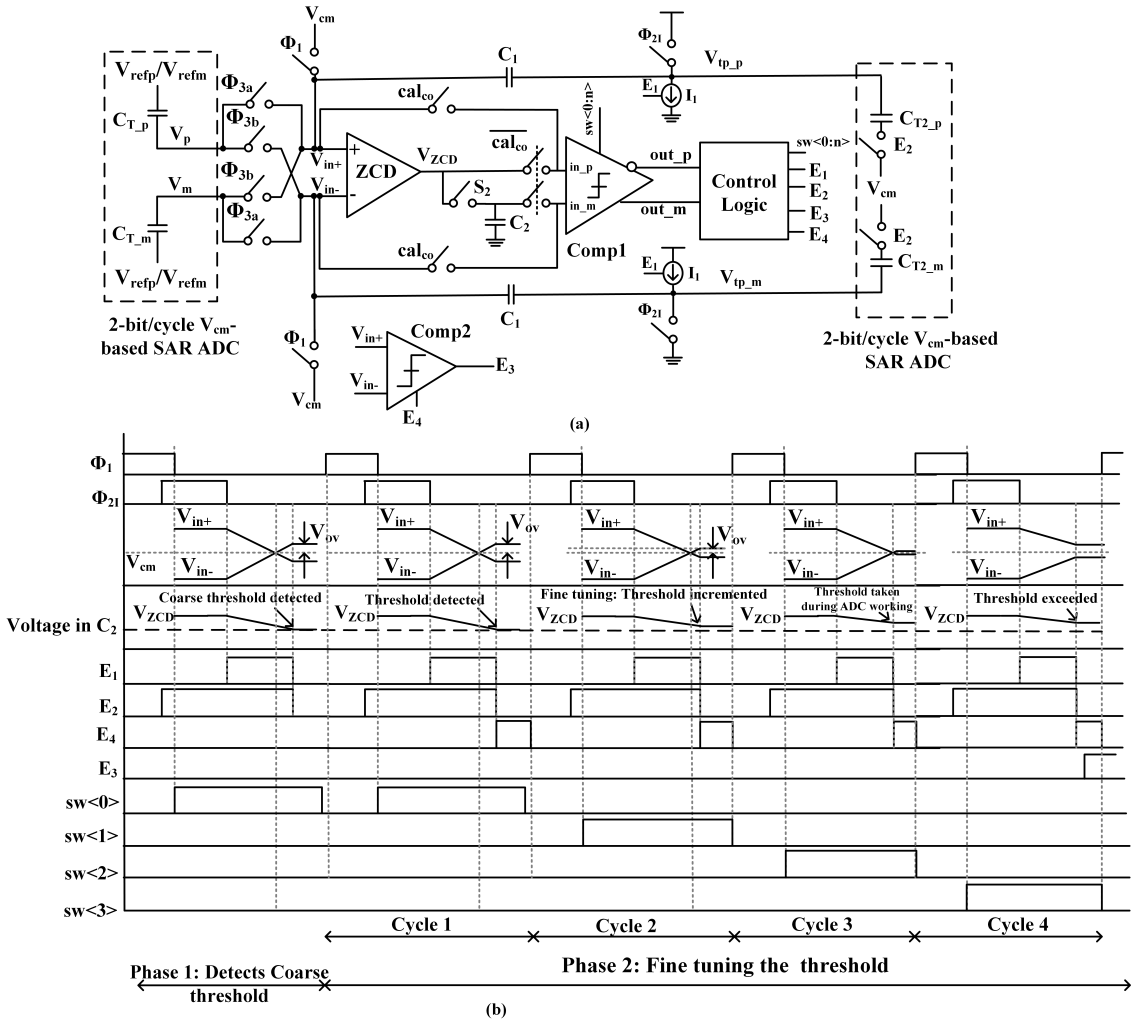


Figure 5.11 (a) Block Diagram (b) Timing diagram of the Improved Overshoot Reduction Technique

Fig. 5.11(a) and (b) shows the block diagram and timing diagram of the improved overshoot detection technique. In step 1, as shown in Fig. 5.11(b), during Φ_1 phase, the maximum differential dc voltage is sampled and the sampled voltage is converted into a digital format by the 2-bit/cycle V_{cm}-based SAR ADC. The residual voltages after the final conversion of the SAR ADC are fed as input to the ZCD after the Φ_1 phase. The voltages are fed as input in a manner such the V_{in+} is always at a higher potential than V_{in-}. This is because the overshoot voltage is signal polarity dependent. During the overlap of Φ_{2I} and Φ_I phase, the capacitor C_1 is reset. Moreover, during Φ_{2I} phase, the capacitors (C_{T2_p} and C_{T2_m}) in the second stage V_{cm}-based SAR ADC are in the reset condition.

Once V_{in+} and V_{in-} are connected to the residual voltage from the SAR ADC, switch S_2 is activated to charge the capacitor C_2, and cal_{co} is activated such that

the residual voltage is connected to the comparator (Comp1), as shown in Fig. 5.12. During the coarse threshold tuning phase, switch<0> is activated in the comparator COMP1. After the Φ_{2I} phase, E_1 is activated to charge the second stage capacitors of the SAR ADC. Once, the zero-crossing ($V_{in+} = V_{in-}$) is detected, E_1 and E_2 are deactivated. E_1 and E_2 are deactivated after a finite delay from the comparator and the control logic, therefore, the voltage in the capacitor C_2 needs to be adjusted to reduce the finite delay from the comparator and the control logic. Hence, the coarse threshold is attained from the above process.

5.2.1.2 Fine Threshold Tuning

After the coarse threshold is detected, the fine tuning of the threshold is the next step. In the next Φ_1 phase i.e. cycle 1 as shown in Fig. 5.11(b), the same differential dc voltage is applied as an input to the 2-bit/cycle V_{cm}-based SAR ADC as in step 1. At the end of the Φ_{2I} phase, the residual voltage of the SAR ADC is available as inputs to the ZCD. During the Φ_{2I} phase, cal_{co} is set to logic '0' such that the capacitor C_2 and V_{ZCD} (output of the ZCD) are connected as inputs to the comparator COMP1 which has switch<0> connected in the unit comparator cell<0>, as shown in Fig. 5.12 and the remaining unit comparator cells are off. In comparator COMP1, there are 'n' unit comparator cell. After Φ_{2I} is deactivated, E_1 activates the current sources I_1. Thereby pushing V_{in+} and V_{in-} closer to each other. During this phase when V_{ZCD} crosses the voltage in the capacitor C_2, the threshold is detected by the unit comparator cell <0> in comparator COMP1. This threshold incorporates the delay from the ZCD and control logics. After the threshold is detected, E_4 activates the comparator COMP2 to check if V_{in+} is greater or less than V_{in-}. If V_{in+} is less than V_{in-}, E_3 is set to low stating that the threshold does not detect V_{in+} equal to or greater to V_{in-} and hence the next switch in the unit comparator cell is activated.

In the next Φ_1 phase i.e. cycle 2, the same procedure is followed until the end of Φ_{2I} phase. In this cycle the next unit comparator cell<1> is activated by activating switch<1>, and deactivating all other switches in the comparator cell. In each unit comparator cell, the width of the M_1 transistor (drawn in gray) is incremented to change the threshold of the comparator. Once E_1 is activated, the current sources I_1 pushes V_{in+} and V_{in-} closer to each other. Using the new threshold in the comparator, V_{ZCD} is compared with the voltage in the capacitor C_2. Due to the new threshold from the unit comparator cell <1>, the comparator output will flip be-

fore the voltage V_{ZCD} becomes equal to the voltage in the capacitor (C_2). In this manner the overshoot voltage is reduced and the zero-crossing of the V_{in+} and V_{in-} is detected, as shown in cycle 2. This process continues till a case happens such as shown in cycle 4 where the threshold is so high that V_{in+} is greater than V_{in-} that activates signal E_3. Once, E_3 is activated it means that the previous threshold from the unit comparator cell i.e. in cycle 3 using switch <2>, accurately detects the crossing point of V_{in+} and V_{in-}.

The sizing of the M_1 transistor is chosen by finding the maximum width of M_1 transistor when the threshold exceeds as shown in cycle 4 in Fig. 5.11(b) for all the five corner cases. With the knowledge of the largest width for M_1, the number of unit comparator cells are decided.

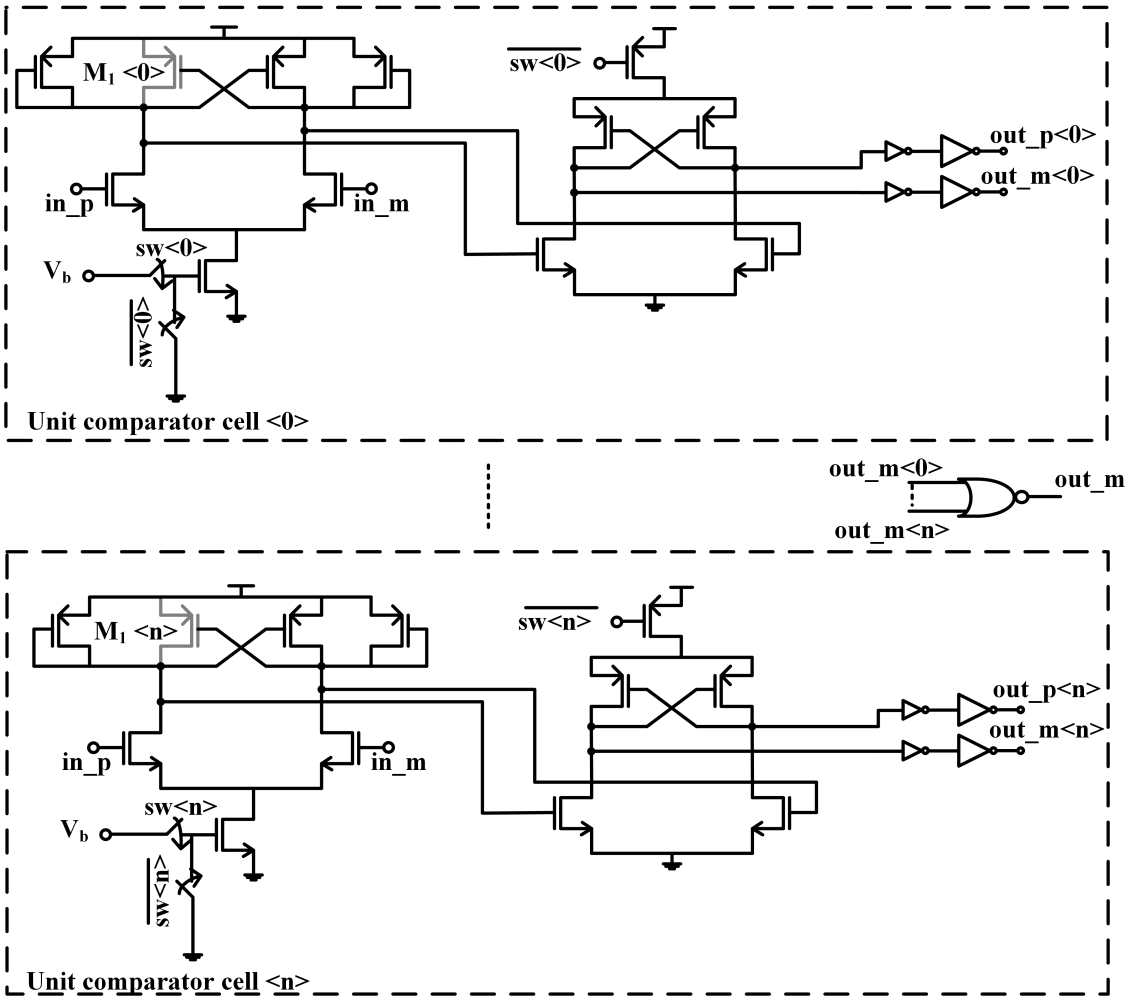


Figure 5.12 Schematic of the comparator (COMP1)

5.2.2 Results

The improved version of the overshoot reduction technique was implemented in an 10-bit sub-radix 2-bit/cycle V_{cm}-based SAR-assisted two-stage pipeline ADC. Fig. 5.13 shows the layout of the 10-bit sub-radix two-stage SAR-assisted pipeline ADC, and is designed in 130 nm SiGe BiCMOS technology. The active area occupied by the ADC is 0.8812 mm^2.

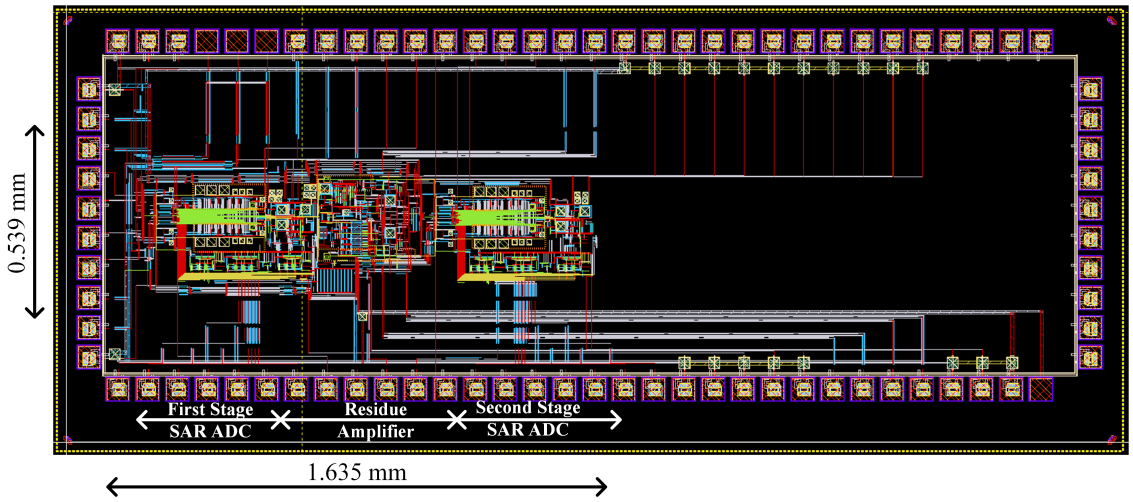


Figure 5.13 Layout of the 10-bit sub-radix V_{cm} based SAR-assisted two-stage pipeline ADC

Fig. 5.14 shows the simulation waveform of the proposed ZCD in the tt corner case. Zero-crossing 1 is the first amplification of the residue amplifier after determining the coarse threshold. T_{D1} is the time difference when the residual voltage from the SAR ADC is the input to the ZCD and when the ZCD inputs detects the zero-crossing. T_{D2} is the overshoot time due to the delay from the control logic and comparator. V_{ov1} is the overshoot voltage during zero-crossing 1 and is the difference between V_{cm} and V_{o_p}. In Fig. 5.14, zero-crossing 2 is the stage when the threshold of the comparator has been tuned to detect the zero-crossing in the presence of the artifacts that contribute to overshoot. T_{D3} and V_{ov2} is the overshoot time and overshoot voltage during zero-crossing 2 stage. V_{ov2} is the difference between V_{cm} and V_{o_p1}.

Table 5.2 compares the overshoot voltage and time, and the percentage reduction of overshoot voltage and time after the threshold has been tuned for different corner cases. During the stage: zero-crossing 1, the T_{D1} as 2.5264 ns. After the threshold of the comparator was tuned, the maximum and minimum overshoot time (T_{D3}) was 423 ps and 124 ps, respectively, as shown in table 5.2. Moreover, the maximum and minimum percentage reduction in the overshoot time was attained as 98.012%

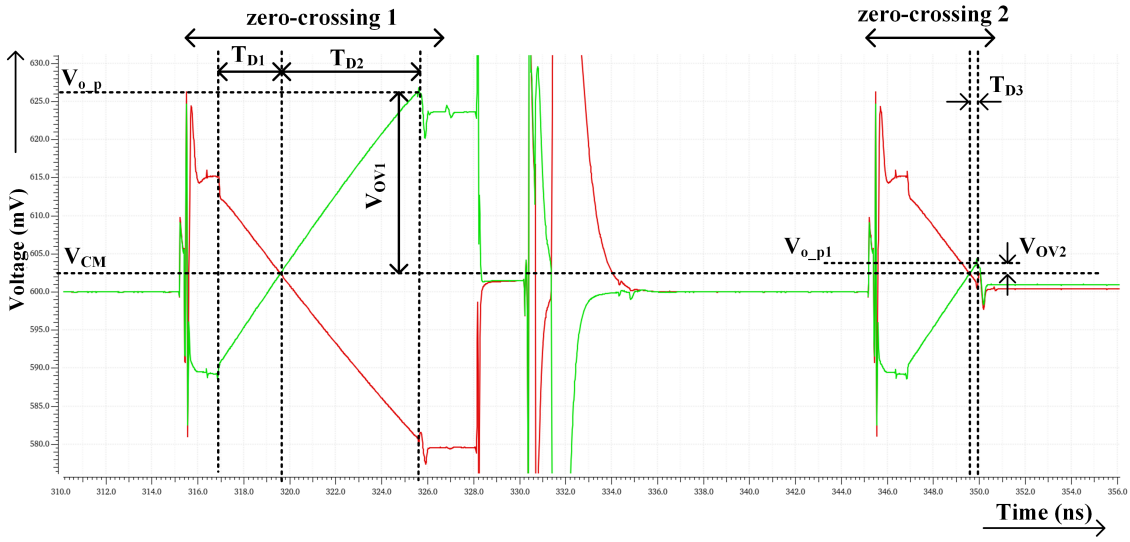


Figure 5.14 Simulation waveform of the improved overshoot reduction technique in the tt corner case

and 90.544%, respectively. The maximum and minimum overshoot voltage after fining tuning the threshold was attained as 1.59 mV and 0.584 mV, respectively. The maximum and minimum percentage reduction in the overshoot voltage was attained as 97.67% and 89.153%.

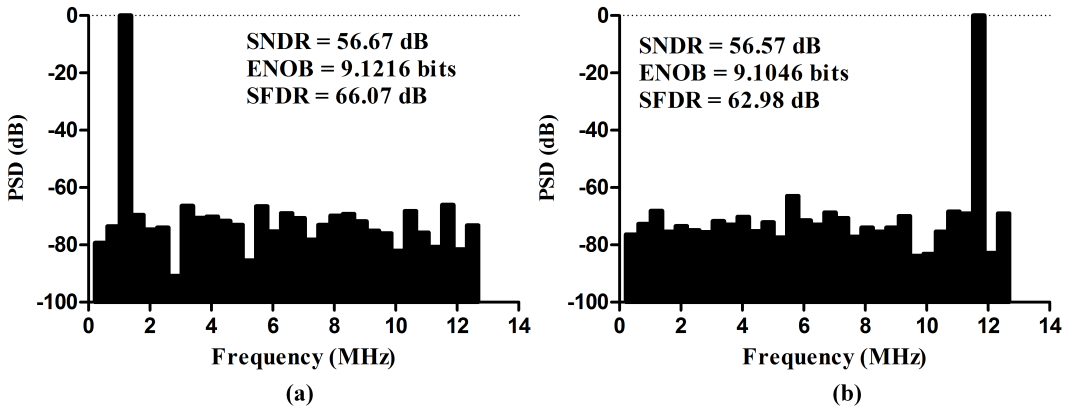


Figure 5.15 Post-layout simulation at an input frequency of (a) 1.171875 MHz and (b) at near Nyquist frequency of 11.328125 MHz

Table 5.2 Comparison of Overshoot Voltage and Time, and Percentage Reduction of Overshoot Time and Voltage after fine-tuning the threshold for different Corner Cases

	Corner Cases				
	tt	***ss***	***fs***	***ff***	***sf***
$\mathbf{V_{ov1}}$ **(mV)**	23.689	10.971	18.43305	25.1807	25.11485
$\mathbf{V_{ov2}}$ **(mV)**	1.0925	1.19	1.59	0.829	0.584
% reduction of Overshoot voltage $\mathbf{((V_{ov1} - V_{ov2})/(V_{ov1}))\ x100}$	95.388	89.153	91.374	96.707	97.67
$\mathbf{T_{D2}}$ **(ns)**	5.9615	3.70993	5.3879	4.8293	6.2396
$\mathbf{T_{D3}}$ **(ns)**	0.25772	0.3508	0.423	0.166	0.124
% reduction of Overshoot time $\mathbf{((T_{D2} - T_{D3})/(T_{D2}))\ x100}$	95.6769	90.544	92.149	96.55	98.012

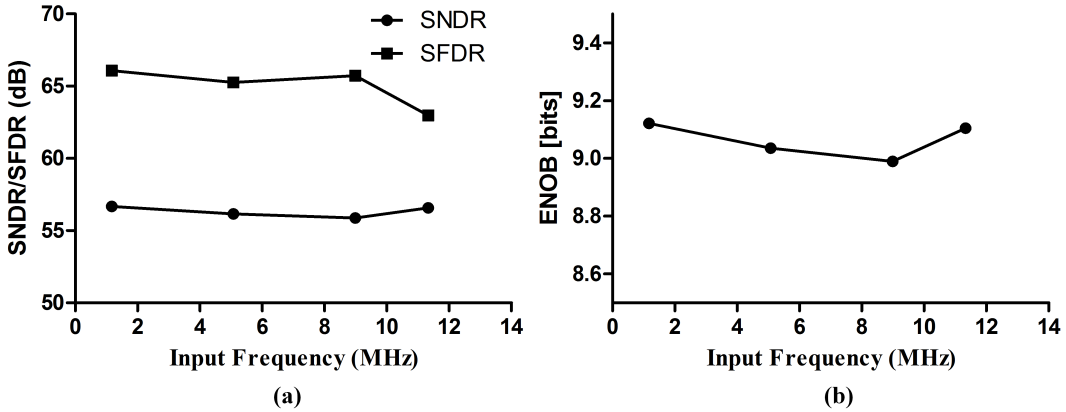


Figure 5.16 Post-layout (a) SNDR and SFDR (b) and ENOB for different input frequencies at a sampling frequency of 25 MS/s

Table 5.3
Post-layout Performance Summary

Process [nm]	130
Supply Voltage [V]	1.2
Resolution [bit]	10
Sampling Rate [MS/s]	25
SNDR @ 1.171875 MHz input [dB]	56.67
SFDR @ 1.171875 MHz input [dB]	66.07
ENOB @ 1.171875 MHz input [bits]	9.1216
SNDR @ Nyq [dB]	56.57
SFDR @ Nyq [dB]	62.98
ENOB @ Nyq [bits]	9.1046
Power [mW]	8.212
$\mathrm{FoM_W}$ @ Nyq [fJ/conversion-step]	589.70

Fig. 5.15 (a) shows the post-layout SNDR, SFDR, and ENOB of 56.67 dB, 66.07 dB, and 9.1216 bits, respectively at an input frequency of 1.171875 MHz with a sampling speed of 25 MS/s for the SAR ADC. Fig. 5.15 (b) shows the post-layout SNDR, SFDR and ENOB of 56.57 dB, 62.98 dB and 9.1046 bits, respectively with a sampling speed of 25 MHz at near Nyquist frequency of 11.328125 MHz. Fig. 5.16(a) shows the post-layout SNDR and SFDR at different input frequency for the sampling frequency of 25 MS/s. Fig. 5.16(b) shows the post-layout ENOB at different input frequency for the sampling frequency of 25 MS/s. The performance of the ADC is compared with the state-of-the-art works (Digel, Groezing & Berroth (2012); Hershberg et al. (2010); Shin et al. (2014); Tang & Pun (2012)), as shown in Table 5.4. As observed from Table 5.4, the overshoot voltage is low compared to other state-of-the-art-works and has a considerable low overshoot time compared with the other works.

Table 5.4 Performance Summary and Comparison

	This work (from Chapter 5)	**This work (from Chapter 4)**	**Shin (2014)**	**Tang (2012)**	**Hershberg (2010)**	**Digel (2012)**
Architecture	Pipeline-SAR	Pipeline-SAR	Pipeline	Pipeline	Pipeline	SAR
Technology [nm]	130	130	55	180	180	130
Foundry	IHP	IHP	-	-	-	IHP
Overshoot Time (ps)	**124 - 423**	**55.58**	71.4-107.1	-	410	-
Overshoot Voltage (mV)	**0.584 - 1.19**	**2.8**	30	5	-	-
Supply Voltage [V]	1.2	1.2	1.1	1.8	1.8	1.3
Sampling Rate (MS/s)	25	16	200	20	20	22
SNDR [dB]	56.67	49.53	64.4	57.2	68.3	49.3
SFDR [dB]	66.07	55.23	82.9	66.8	76.3	59.8
ENOB [bit]	9.1046	7.9344	10.44	9.2	11.1	7.9
Total Power (mW)	8.212	1*	30.7	2.6	17.2	3.3
FoM_W (fJ/conversion-step)	589.7 **	255	111	221	405.5	630

*Power of the core ADC

**at Nyquist frequency

5.2.3 Measurement Challenges

Based on Fig. 5.13, there are 84 I/O pads in total with a dimension of 10 x 32 I/O. According to the number of I/O pads on the chip, a square chip carrier with 132 pins was selected as shown in Fig. 5.17(a) with a dimension of 12.065 mm x 12.065 mm. The dimension of the die is 1.42 mm x 3.52 mm. Using the dimension of the die and the chip-carrier, the length of the wire-bond (l) can be calculated using the Pythagoras theorem using equation 5.19. Fig. 5.17(b) shows the wire-bond length calculation.

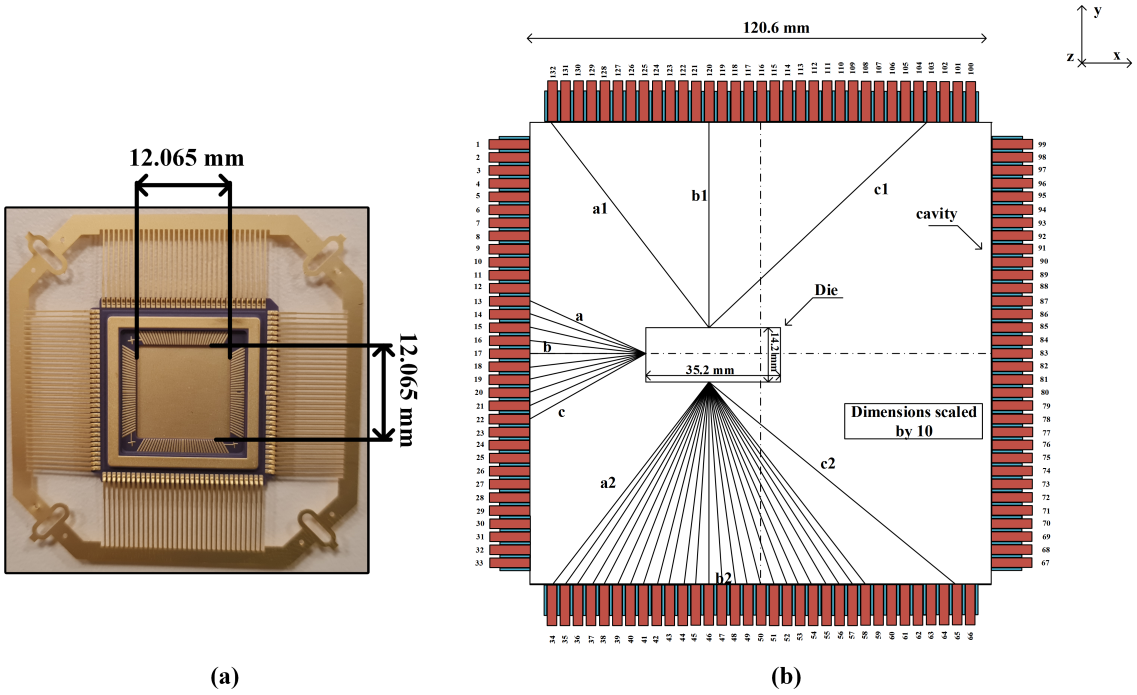


Figure 5.17 (a) Chip carrier and (b) Wire bond length calculation

$$l = \sqrt{x^2 + y^2 + z^2} \tag{5.19}$$

where z is the difference between the cavity height and die height, y is the perpendicular distance between the die and the cavity which is shown as b1, b, and b2 in Fig. 5.17(b), and x is the distance between the point on the die to the point where the wire-bond will be connected on the chip frame in the x-axis. The chip is placed more towards the left because the input signals which are greatly affected by the inductance are placed on the left side of the die. Hence, to reduce the inductance from the wire bond for the input pins, the die is placed more closely to the left.

Based on Fig. 5.17(b), lines are drawn from a single point to the frame of the chip carrier. This method was selected because the pitch between the I/O pads is 100 μm which is a small value, and hence, one can calculate the x distance from the

point source to attain an approximate idea of the x distance. In Fig. 5.17(b) all dimensions are scaled up by 10. Based on Pythagoras theorem the length of the wire bond was calculated. From Fig. 5.17(b), it can be observed that a, a1,a2,c, c1, and c2 shows the largest distance, and b,b1,b2 show the shortest distance between the die and the cavity. The values attained are shown below:

a = 3.32946 mm, b = 3.01 mm, c = 3.47922 mm

a1 = 6.80254 mm, b1 = 5.36 mm, c1 = 7.83115 mm

a2 = 6.7047 mm, b2 = 5.295 mm, c2= 8.33869 mm

Using the thumb rule, a 1mm wire-bond length = 1 nH (Steyaert & Craninckx (1994)), in the simulation an inductor was placed at the I/O pads based on the length attained above. It was observed that the ENOB of the single channel reduced from 9 bits to 5.1362 bits. Fig. 5.18 shows the ENOB of the single-channel ADC when simulated with the inductance due to the wire-bond. It can be observed that the inductance of the wire-bond drastically reduces the ENOB of the ADC. Hence, the aim is to reduce the length of the wire bond.

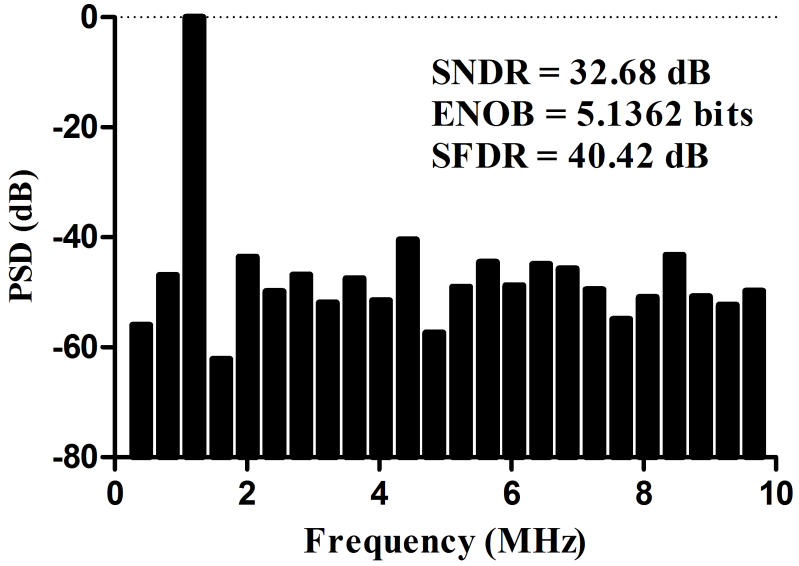


Figure 5.18 Post-layout simulation with the inductance connected to each I/O pad due to the wire bond

5.2.3.1 Wire bond reduction techniques

The complete board was designed in OrCAD PCB Editor. The board can be divided into two boards: the outer and inner board. The inner board is the board where the die will be placed and all wire bond reduction techniques will be done. The board other than the inner board is defined as the outer board. Fig. 5.19 shows the inner and outer board.

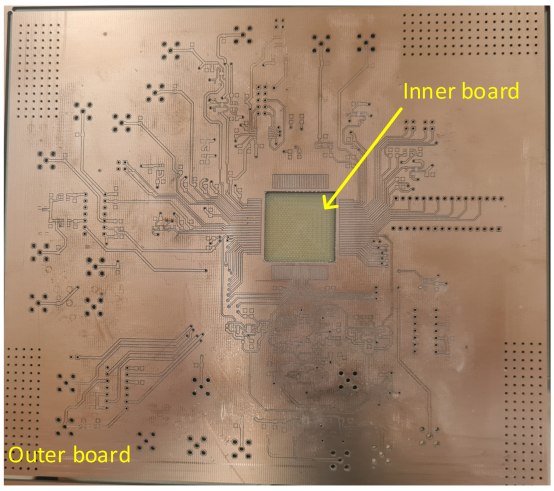


Figure 5.19 4-layer board fabricated for the single-channel ADC

Two ideas were proposed to reduce the effect of the inductance due to wire bond

i. Wire bond to the PCB

ii. Flip chip

1. Wire bond to the PCB

The techniques implemented to wire-bond onto the PCB are as follows:

i. Wire bond to the Copper (Cu) surface of the PCB

ii. Wire bond to the Aluminium (Al) deposited surface

iii. Wire bond to the Gold (Au) deposited surface

i. Wire bond to the Copper (Cu) surface of the PCB

The first trial was to wire-bond to the Cu surface of the PCB. The mask of the inner board was designed in OrCAD PCB editor and is shown in Fig. 5.20(a). Using the mask, the PCB was milled using the LPKF ProtoMat. The pattern attained is shown in Fig. 5.20(b). However, Cu surface of the PCB cannot stick with Au of the wire bond.

ii. Wire bond to the Aluminium (Al) deposited surface

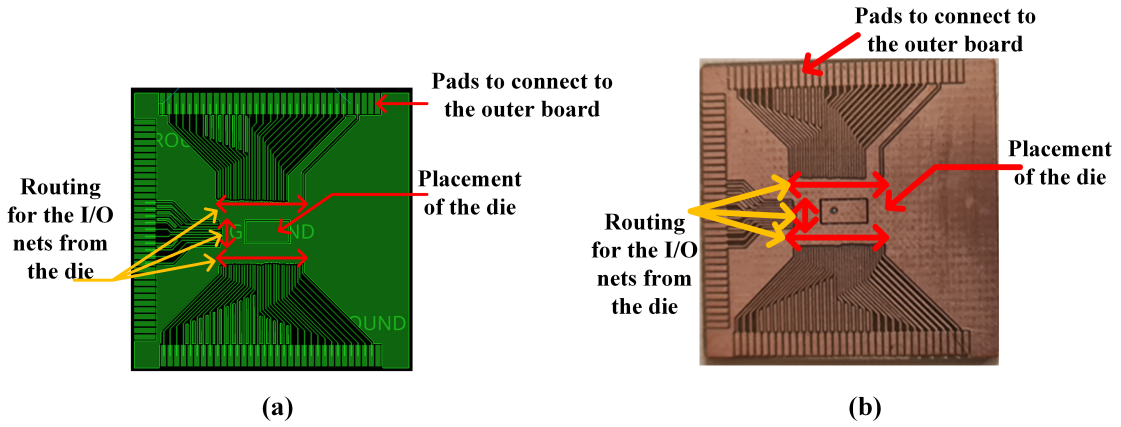


Figure 5.20 (a) Mask of the inner board and (b) Board fabricated based on the mask

The second technique used was to deposit Al on the FR4 substrate. The procedure to coat with Al and pattern it is as follows:

i. Firstly, the PCB substrate is cleaned using IPA (Isopropyl Alcohol) and Acetone to remove the organic impurities on the substrate. Then, the substrate is dried using N_2 air.

ii. The dried substrate is then placed inside the electron beam depositor and then coated with 20 nm of Cr, and then, 1 μm of Al. A thick Al is coated to ensure that the surface roughness is less than 1 μm so that the wire bond (made of Au) can stick to the Al after deposition.

iii. Then, a thick layer of photoresist is deposited on top of the Al deposited surface. This is used to protect the underlying Al when milled with the LPKF ProtoMat. Using the mask of Fig. 5.20(a), the pattern was generated as shown in Fig. 5.21(a).

Another version of the inner board coated with Al was tried as shown in Fig. 5.21(b) where the patterned PCB was placed inside the chip carrier. In this version, the above two steps were performed except for the third step. From this experiment it is observed that the mechanical stress created from the milling process during LPKF ProtoMat removes the Al and hence, a thick photoresist was deposited to withstand the mechanical stress from the LPKF ProtoMat. However, wire bonding onto the Al board was not successful as the Al was not able to stick very well due to the surface roughness of the board.

iii. Wire bond to the Gold (Au) deposited surface

To wire bond onto the PCB surface, initially, the surface must be coated with Au. The process followed is as follows:

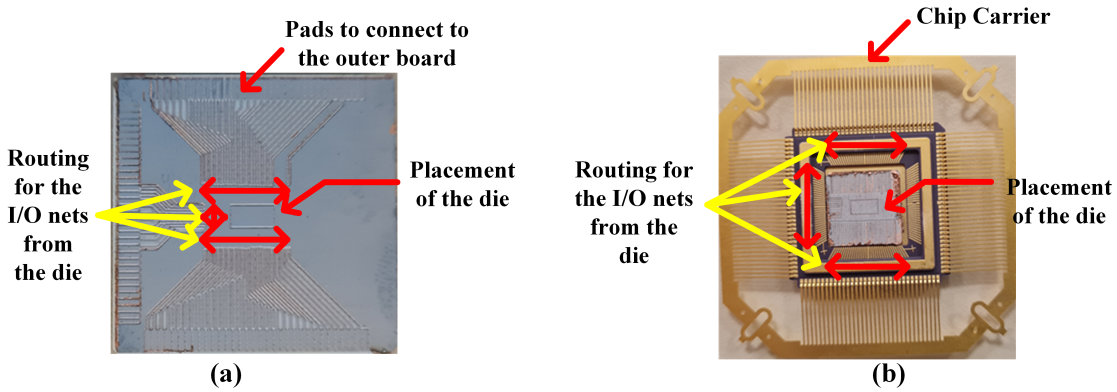


Figure 5.21 Patterned Board after Al deposition (a) on the inner board and (b) inside the chip carrier

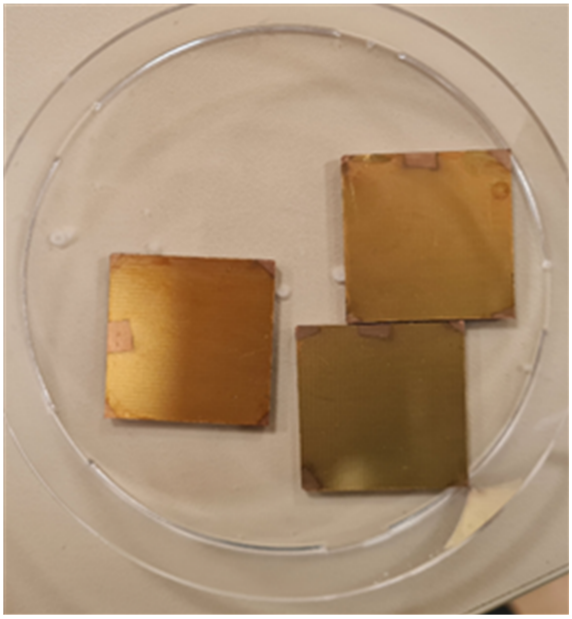


Figure 5.22 Sample coated initially with 20 nm Ni and then 200 nm of Au

i. **Cleaning process**: Initially, the inner PCB substrate was decontaminated by IPA and Acetone, and dried in an oven at 60 ^{0}C for 15 minutes.

ii. **Lithography Process**: Then, the photoresist AZ 5214E was dropped on the inner substrate, and spin-coated with 2000 rpm. Afterwards it was soft baked on a hot plate with a temperature of 115 ^{0}C for 80 s. The expected photoresist thickness is around 1.95 μm. The lithography process was conducted through Midas UV mask aligner system in SUNUM facilities at Sabanci University. To perform the lift-off process an image reversal technique was used to create the negative of the positive mask on top of the PCB and patterned.

iii. **Thermal Evaporation**: Then, Ni is thermally deposited with 30 nm of thickness. This layer acts as an adhesive for gold coating. Afterwards the gold layer

was deposited with a thickness of 250 nm using 1.5 gm of Au. Fig. 5.22 shows the deposited Au.

However, the wire bond could not stick on the deposited Au surface because of the surface roughness. To attain a smooth surface, the thickness of the Au needs to be increased to 1 μm, however, a 7.5 gm of Au is required to deposit it which is not a feasible solution because the thermal boat can hold up to 4 gm of Au.

2. Flip Chip technique

The flip chip technique was attempted to completely eliminate the wire bond. To fabricate the board for flip chip, wet etch technique is used rather than the milling process. The reason for the wet etch technique is due to the fact that LPKF ProtoMat has a minimum resolution of 150 m. However, the I/O pads have a width of 80 μm with a pad-to-pad pitch of 100 μm which is less than the minimum resolution of LPKF Protomat, hence, the wet etch technique was utilized to fabricate the inner board.

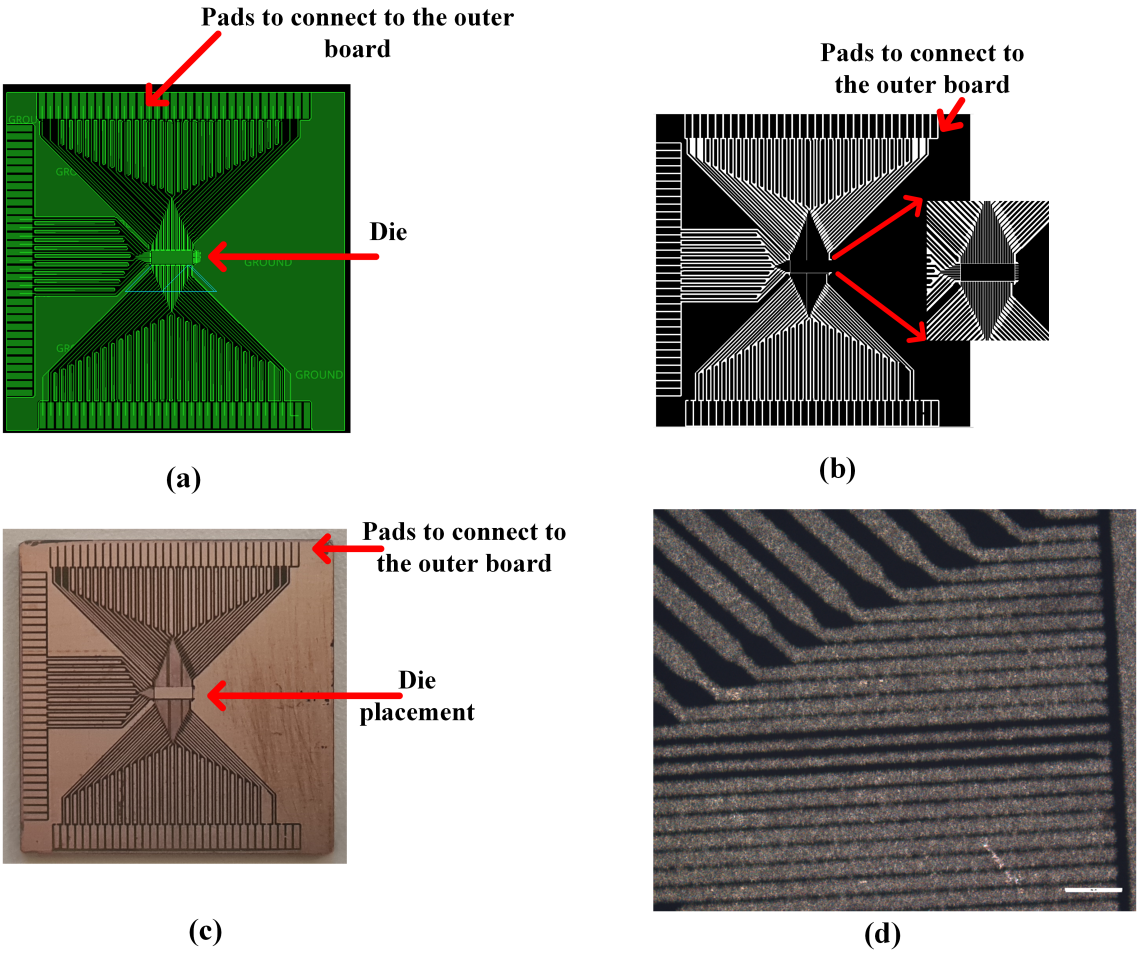


Figure 5.23 (a) Layout, (b) mask (c) patterned PCB and (d) zoomed-in view of the patterned PCB for the inner board using flip chip

The procedure to fabricate the inner board is as follows:

i. Initially, the layout of the flip chip was designed in OrCAD PCB Editor as shown in Fig. 5.23(a).

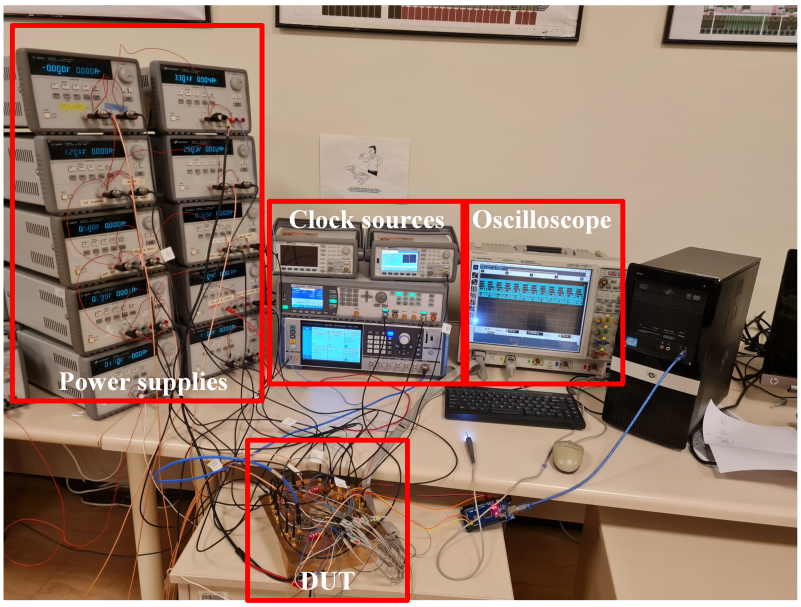
ii. The inner PCB was cleaned using IPA (Isopropyl Alcohol) and Acetone to remove the organic impurities on the substrate. Then, the substrate is dried in an oven at 60 ^{0}C for 15 min.

iii. Afterwards the lithography was performed. A positive photoresist AZ 5214E is dropped on the substrate and then spin-coated at 2000 rpm. Then, the substrate is soft baked on a hot plate at 115 ^{0}C for 80 s. The expected photoresist thickness is around 1.95 μm. The Midas UV mask aligner system in SUNUM facilities at Sabancı University was used to illuminate UV rays on the mask. Since the photoresist is a positive photoresist which means all the surfaces coated in black as in Fig. 5.23(b) will not allow UV rays to penetrate and all the transparent surfaces will allow UV rays to pass through. Those areas illuminated with UV rays will become soft and can be removed by the developer. The developer is made of water, HCl and H_20_2 having the concentration ratio of 200:50:10 (H20:HCl:H_20_2), respectively. The substrate was etched in the developer solution for 5 min and 30 s. The flip chip board is shown in Fig. 5.23(c).

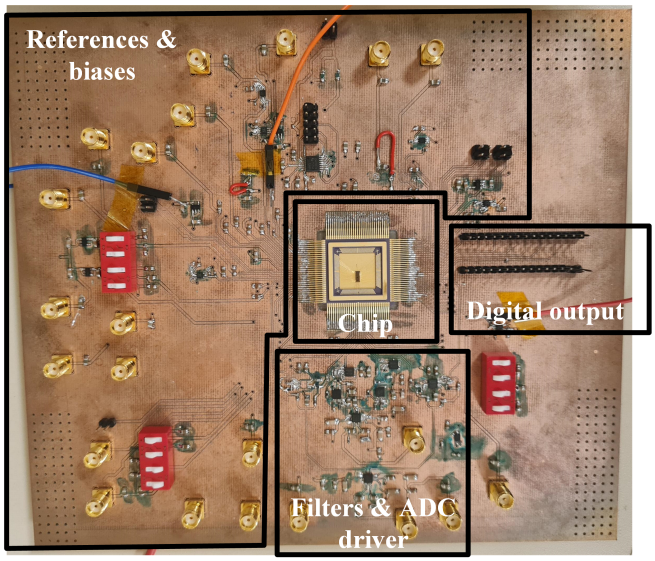
However, on close examination under the microscope, it was observed that some traces were thin and some areas were short, as shown in Fig. 5.23(d). If the inner PCB was further etched then some traces will be completely etched. Hence, the wire-bond technique to the chip carrier was used to perform the final measurement as flip chip and wire bonding on the surface of the PCB was a failure.

5.2.4 Measurement Results

Fig. 5.24(a) and (b) show the measurement setup and board for the single-channel ADC, respectively.



(a)



(b)

Figure 5.24 (a) Measurement setup and (b) board for the Single-channel ADC

The SNDR, ENOB, and SFDR are 14.74 dB, 2.156 bits, and 21.04 dB, respectively for an input frequency of 292.97 KHz at a sampling frequency of 12.5 MS/s, as shown in Fig. 5.25. The reduction in the ENOB is mainly due to two reasons:

i. The inductance created due to the wire bond combined with the package trace and pin.

ii. The reference signals for the ADC was coupled with the sampling frequency from the board and also the noise created from the PCB.

For instance, the VCM signal for the first stage as shown in Fig. 5.26(a) must be

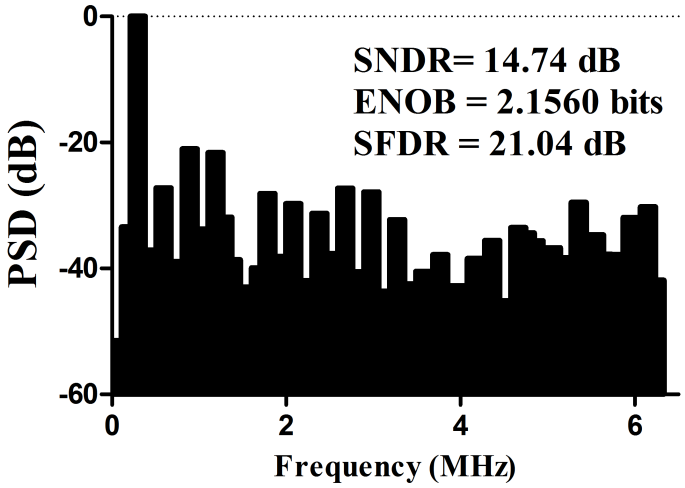


Figure 5.25 FFT plot for the Single-channel ADC

0.6 V, however, due to the noise of the board and coupling from the sampling clock, the VCM signal is not a perfect dc. From Fig. 5.26(a), it can be observed from the yellow box, the peak value of the noise is 0.797 V, and hence, the amplitude is 0.197 V. The first stage of the ADC has one-bit redundancy which means that it can be handled 1 LSB error i.e. 0.01875 V, where the full-scale range is 1.2 V and the number of bits for the first stage is 6 bits. Since, the amplitude of the noise is 0.197 V which is greater than 0.01875 V, thereby reducing the ENOB of the ADC. Moreover, as observed from Fig. 5.26(b) in the yellow box, the sampling frequency of 22.5 MS/s is coupled which reduces the ENOB.

The Vrefp signal for the first stage is shown in Fig. 5.27. It can be observed from the yellow box in Fig. 5.27(a) that the amplitude of the noise is 37.10 mV, and the sampling frequency is coupled to the signal, as shown in the yellow box in Fig. 5.27(b).

In a similar manner, the Vrefn signal for the first stage is shown in Fig. 5.28 is affected by the coupling of the sampling clock and the noise from the board. It can be observed from the yellow box in Fig. 5.28(a) that the amplitude of the noise is 29 mV, and the sampling frequency is coupled to the signal, as shown in the yellow box in Fig. 5.28(b).

The above two reasons for the reduction in the ENOB can be cross-verified from post-layout simulations. Three cases were considered for the analyses. Firstly, the ENOB was attained without the effect of the wire bond and coupling from the board. Secondly, the ENOB was attained due to the effect of the wire bond, trace from the package, and pin. Finally, the ENOB was attained for the above two reasons i.e.

due to the inductance from the wire bond, package trace and pin and also from the noise from the board along with the coupling from the sampling frequency. As observed from Fig. 5.29(a), the ENOB attained is 9.0578 bits. On the adding inductance contributed from the wire bond, trace from the package and pin, the ENOB reduced to 3.4826 bits, as shown in Fig. 5.29(b). Finally, the ENOB is further reduced to 2.9981 bits due to the coupling from the sampling frequency, noise from the board and inductance arising from the wire bond, trace from the package and pin. The ENOB attained from post-layout simulation matches with measurement results. Hence, this proves that the reduction in ENOB is due to the inductance created due to the wire bond combined with the package trace and pin,

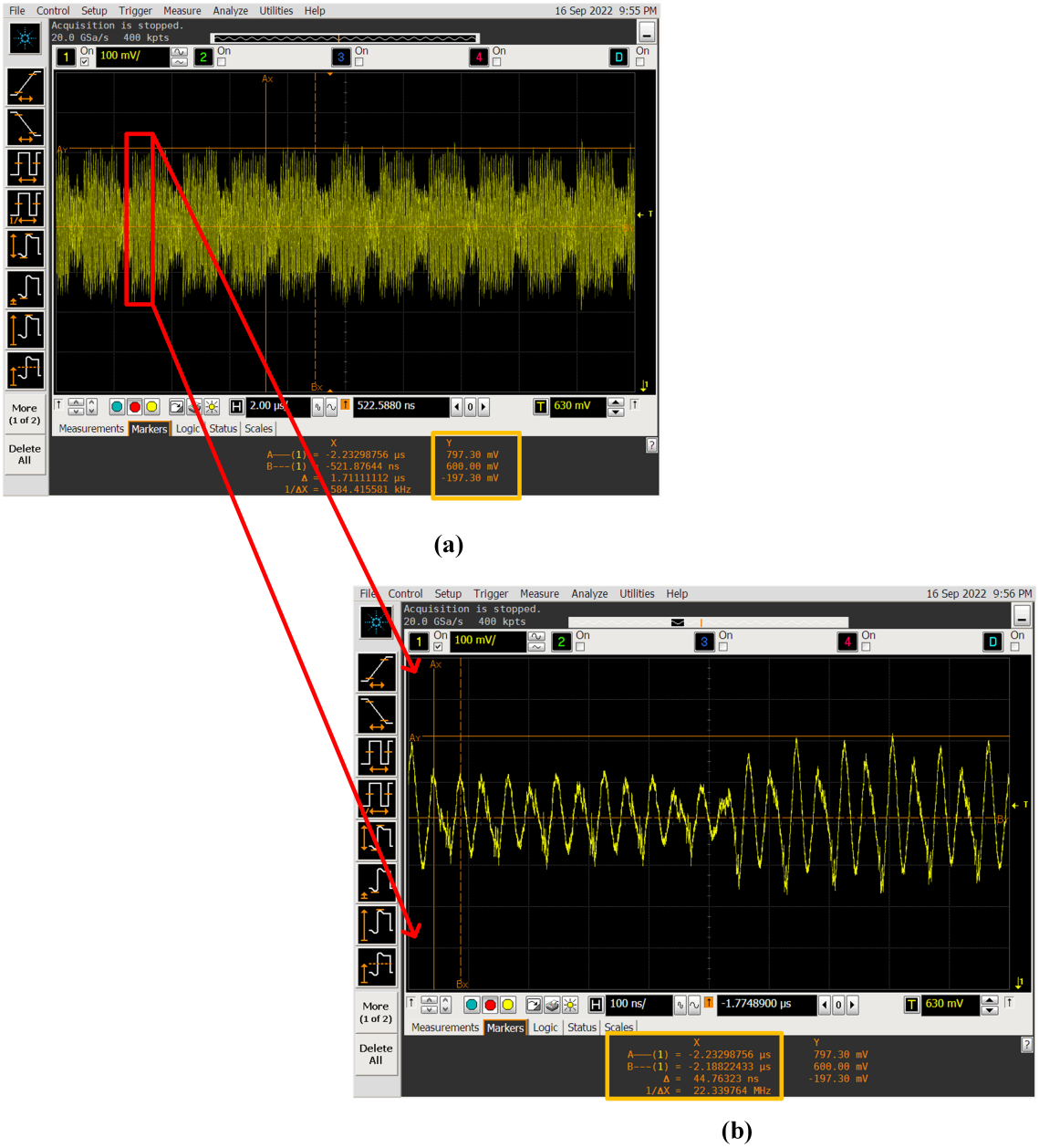


Figure 5.26 (a) VCM signal for the first stage and (b) its zoomed-view

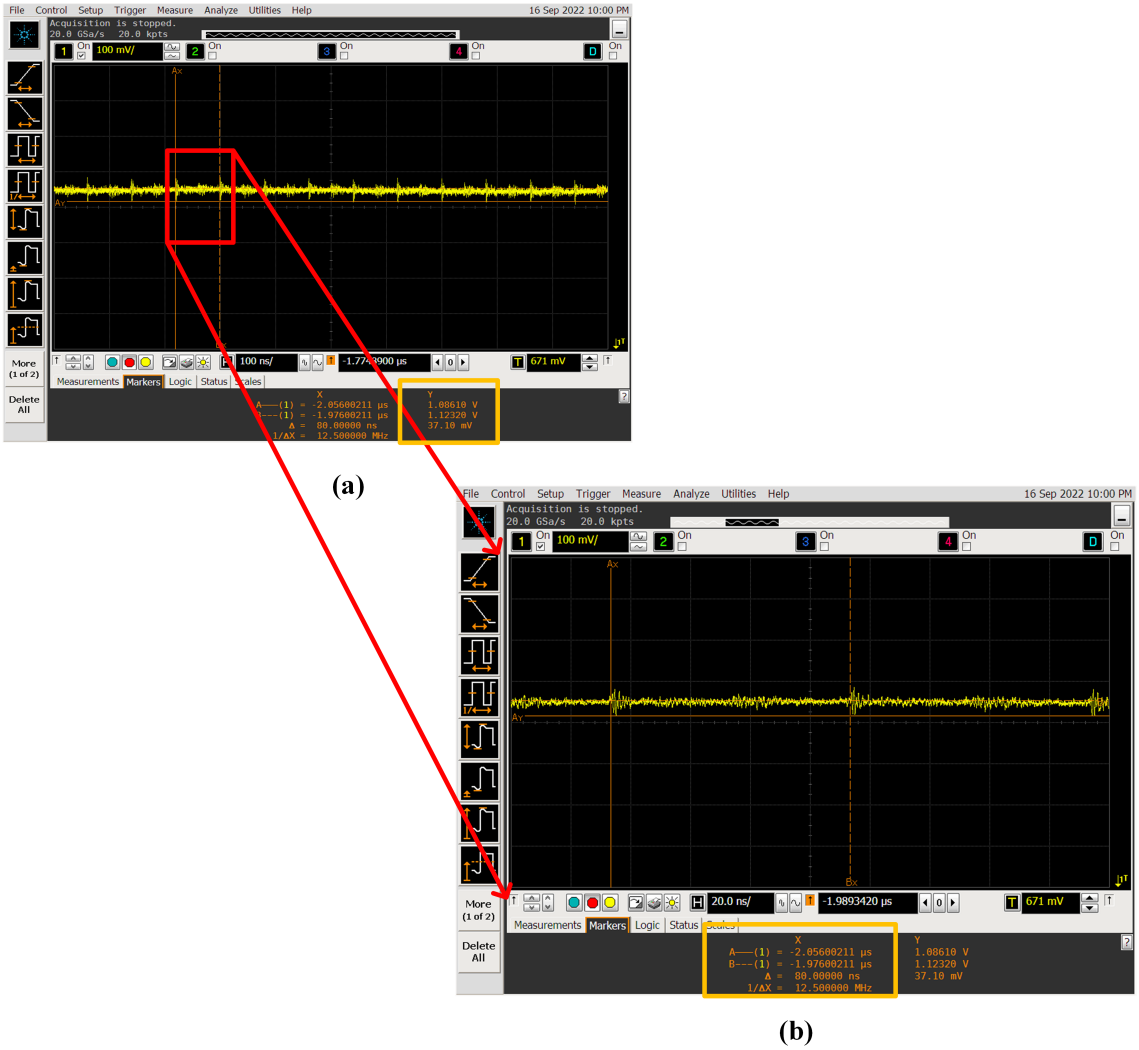


Figure 5.27 (a) Vrefp signal for the first stage and (b) its zoomed-view

the reference signals for the ADC getting coupled with the sampling frequency from the board and also the noise created from the PCB.

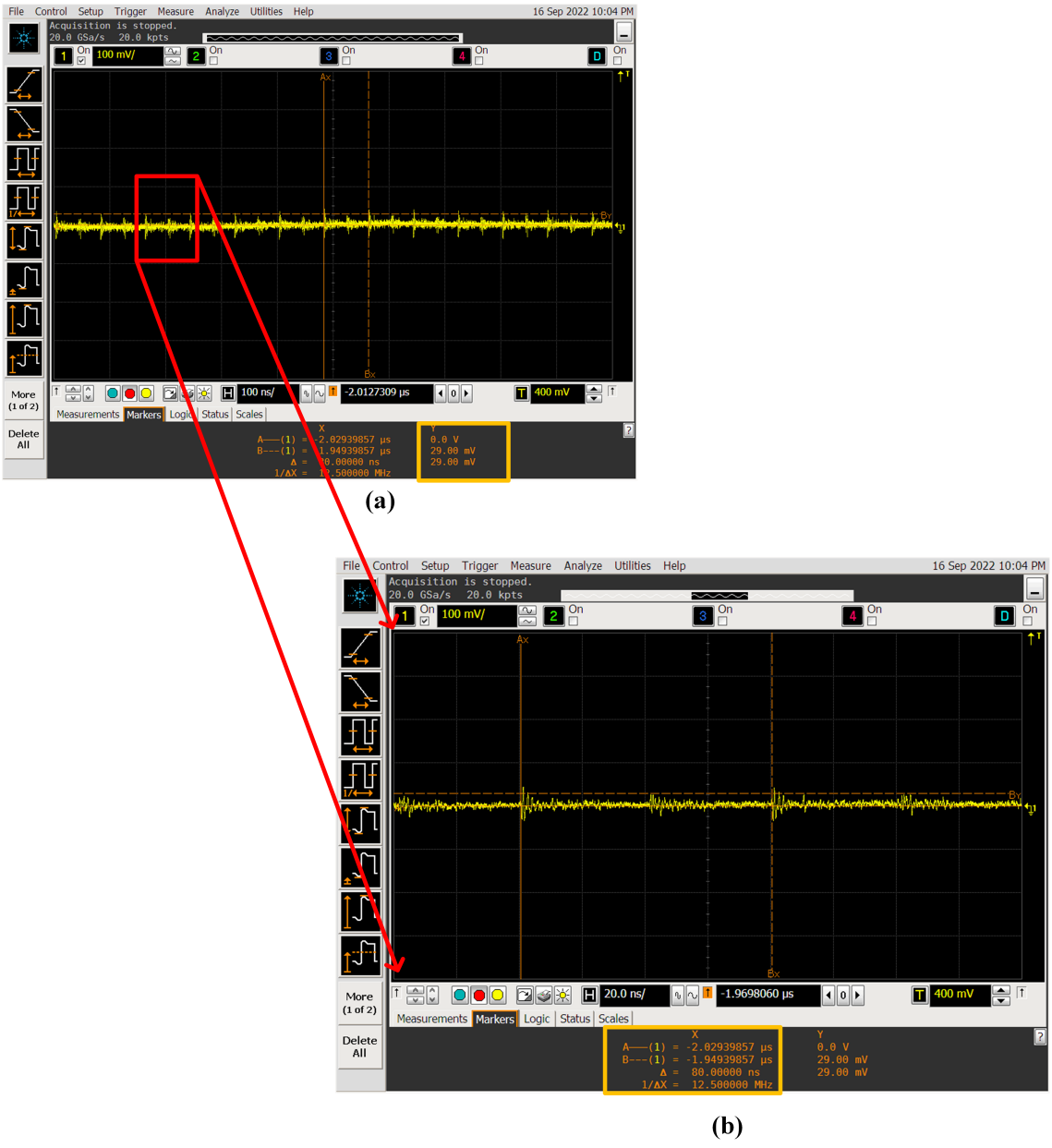


Figure 5.28 (a) Vrefn signal for the first stage and (b) its zoomed-view

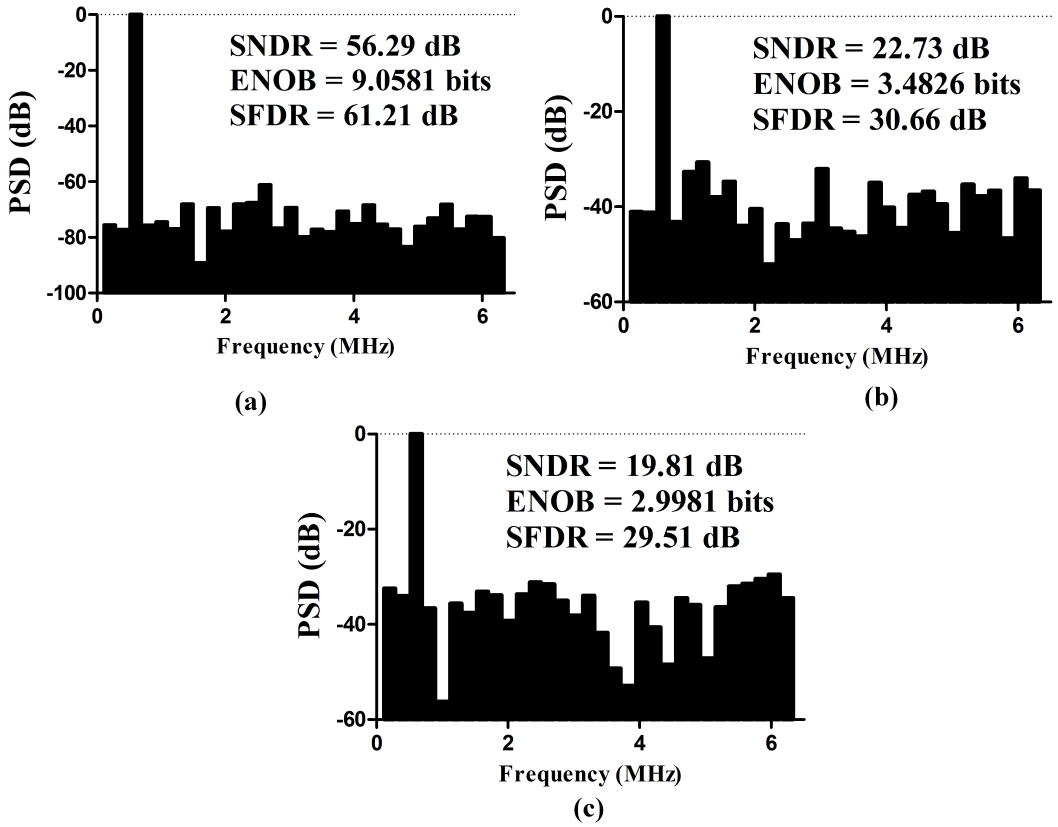


Figure 5.29 FFT plot (a) without the effect from inductance and board, (b) with the effect of the inductance and (c) with the effect of the inductance and from the board

6. 4-channel Time-Interleaved SAR-Assisted Pipeline ADC

To finally reach the specification of the ADC required for the MIMO architecture, the single-channel designed using 2-bit/cycle sub-radix Vcm-based SAR-Assisted pipeline ADC was used in the implementation of the 4-channel TI ADC. Hence, this chapter introduces the concept of time-interleaving, followed by which the inter-channel mismatches are discussed. Then, the time-skew calibration technique is discussed and finally, the post-layout simulation results are explained.

6.1 Time-Interleaving

For a given technology node, the power of the ADC increases with the sampling frequency until a certain point, based on the technology node. After this point, the power increases at a much faster rate as the sampling frequency increases, and the normalized power efficiency (P/f_s) starts to degrade (Wei et al. (2013)). Due to this drawback, a single-channel ADC operating at a high frequency will be less power-efficient. To mitigate this drawback, time-interleaving has become a popular choice in high-speed ADCs (Chan, Zhu, Sin, Ben U & Martins (2016); Le Tual, Narayan Singh, Curis & Dautriche (2014); Verbruggen, Iriguchi & Craninckx (2012)). For an 'N'-channel time-interleaved (TI) ADC, each channel works with a maximum sampling speed of f_s/N. Hence, the power dissipated by the single-channel ADC in the TI architecture will be in the linear region of the power vs sampling frequency for that technology node and hence, making the system power-efficient.

Fig. 6.1 illustrates the basic working principle of an N-channel time-interleaved ADC. In this technique, the input to the ADCs is sampled at f_s/N with a phase shift of $2\pi/N$, as shown in Fig. 6.1, where f_s is the sampling frequency. The digital outputs of each ADC are multiplexed to form the digital output of a high-speed

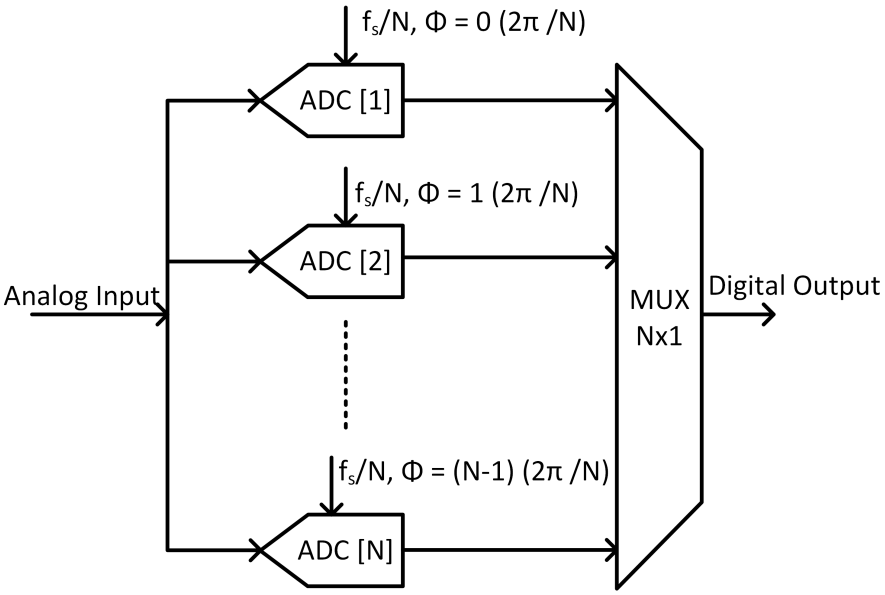


Figure 6.1 Block Diagram of Time-interleaving

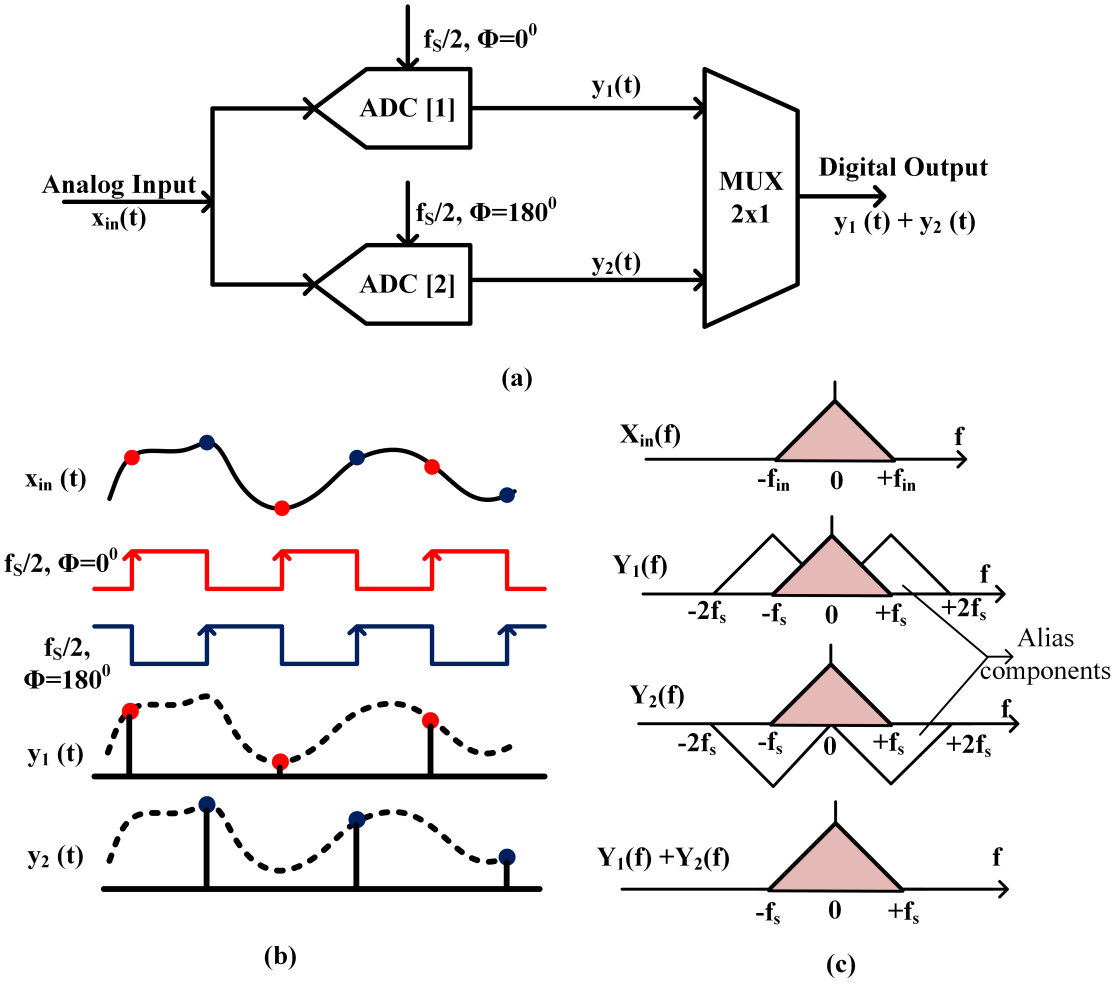


Figure 6.2 (a) Block Diagram (b) Timing Diagram (c) Frequency Response of 2-channel Time-interleaving

ADC. Based on the working principle of TI ADC, a two-channel TI ADC is explained in Fig. 6.2. Fig. 6.2(a) shows the block diagram of a two-channel TI ADC. ADC [1] is sampled at a sampling frequency of f_s with a phase of $\Phi = 0^0$, and ADC [2] is sampled at a sampling frequency of f_s with a phase of $\Phi = 180^0$. The timing diagram is shown in 6.2(b) and $y_1(t)$ and $y_2(t)$ are the discrete output of ADC [1] and ADC [2], respectively. The frequency response is shown in 6.2(c) and $X_{in}(f)$, $Y_1(f)$, $Y_2(f)$ and $Y_1(f) + Y_2(f)$ is the frequency response of $x_{in}(t)$, $y_1(t)$, $y_2(t)$ and multiplexed out of $y_1(t)$ and $y_2(t)$, respectively. As observed from Fig.6.2(c), the alias components of $Y_1(f)$, $Y_2(f)$ needs to be perfectly symmetric to cancel out. However, practically it is difficult to cancel the alias components. The difficulty arises from inter-channel mismatches, which are offset, gain, timing, and bandwidth mismatches between channels.

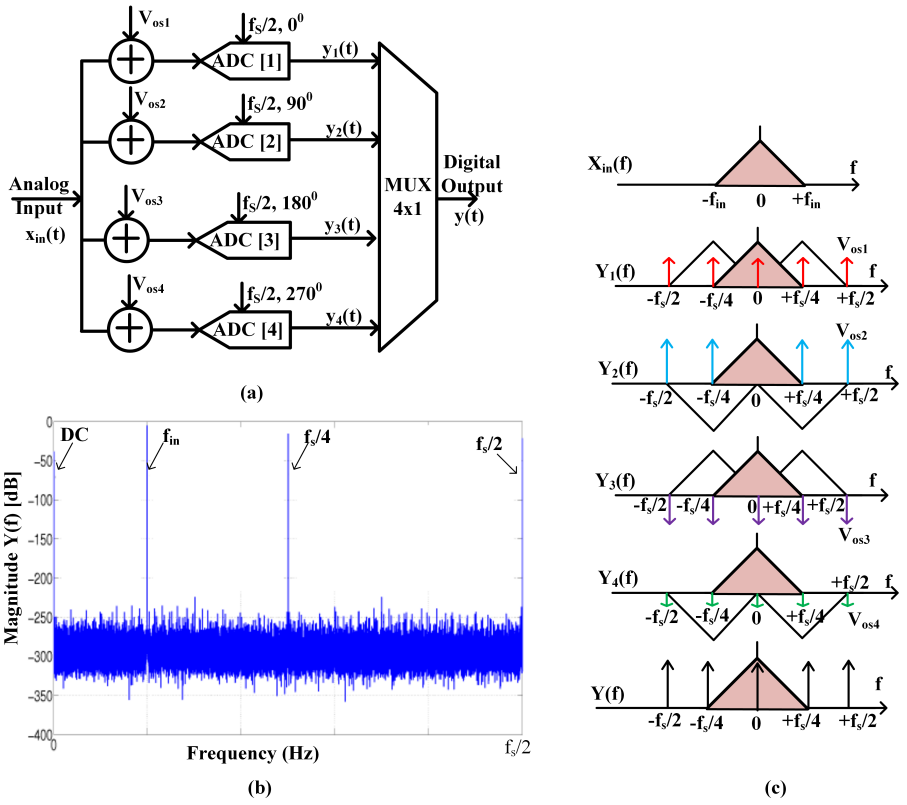


Figure 6.3 (a) Block Diagram (b) Frequency Response (c) Output Spectrum due to offset error in a 4-channel Time-interleaving

Offset Mismatch

Fig. 6.3(a) shows the block diagram of a 4-channel TI ADC when an offset is added to each ADC. Offset is generated by the comparator in the ADC and is random in nature. Fig. 6.3(b) illustrates the frequency response of $Y_1(f)$, $Y_2(f)$, $Y_3(f)$, $Y_4(f)$ when an offset is added to the ADCs and Y(f) shows the frequency response at the output of a 4x1 multiplexer due to the above offsets. Fig. 6.3(c) shows the output

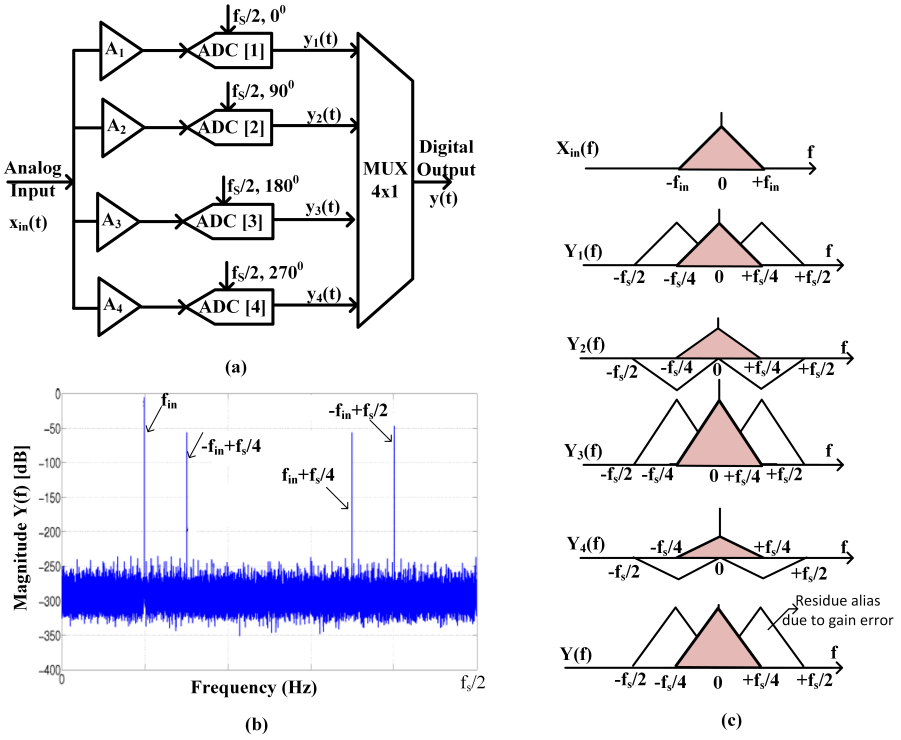


Figure 6.4 (a) Block Diagram (b) Frequency Response (c) Output Spectrum due to gain error in a 4-channel Time-interleaving

spectrum due to the offsets in the ADCs.

Gain Mismatch

Fig. 6.4(a) shows the block diagram of a 4-channel TI ADC when a gain is added to each ADC. Gain mismatch arises from the artifacts from the sampling network such as charge injection and clock feedthrough. Fig. 6.4(b) illustrates the frequency response of $Y_1(f)$, $Y_2(f)$, $Y_3(f)$, $Y_4(f)$ when a gain is added to the ADCs and Y(f) shows the frequency response at the output of a 4x1 multiplexer due to the above gains. Fig. 6.4(c) shows the output spectrum due to the gains in the ADCs.

Timing Mismatch

Timing mismatch arises due to the finite propagation delay from the clock, and variation from the sampling network or clock buffers. The impact of timing mismatch can be understood by considering the timing error from Fig. 6.5. Fig. 6.5 shows an input signal $x_{in}(t)$ that is sampled by a 2-channel TI ADC. The first channel samples at time t_1 and the second channel samples Δt away from t_2, and t_2 is the time where the second channel had to sample without timing mismatch. This change in sampling time creates an error voltage ΔV_{TE} and is described as (6.1).

$$\Delta V_{\mathrm{TE}} = \frac{dx_{\mathrm{in}}}{dt}\Delta t \tag{6.1}$$

From Fig. 6.5, $y_1(t_1)$ and $y_2(t_2 + \Delta t)$ can be expressed as (6.2) and (6.4), respectively

$$y_1(t_1) = x_{\mathrm{in}}(t_1) \tag{6.2}$$

$$y_2(t_2 + \Delta t) = x_{\mathrm{in}}(t_2) + \Delta V_{\mathrm{TE}} \tag{6.3}$$

$$y_2(t_2 + \Delta t) = x_{\mathrm{in}}(t_2) + \frac{dx_{\mathrm{in}}}{dt}\Delta t \tag{6.4}$$

From (6.4), it can be observed that $y_2(t_2)$ is added with a derivative of the input signal x_{in} which corresponds to a 90^0 phase shift in the frequency domain. Hence, when the outputs are added in the frequency domain, the alias components do not cancel out.

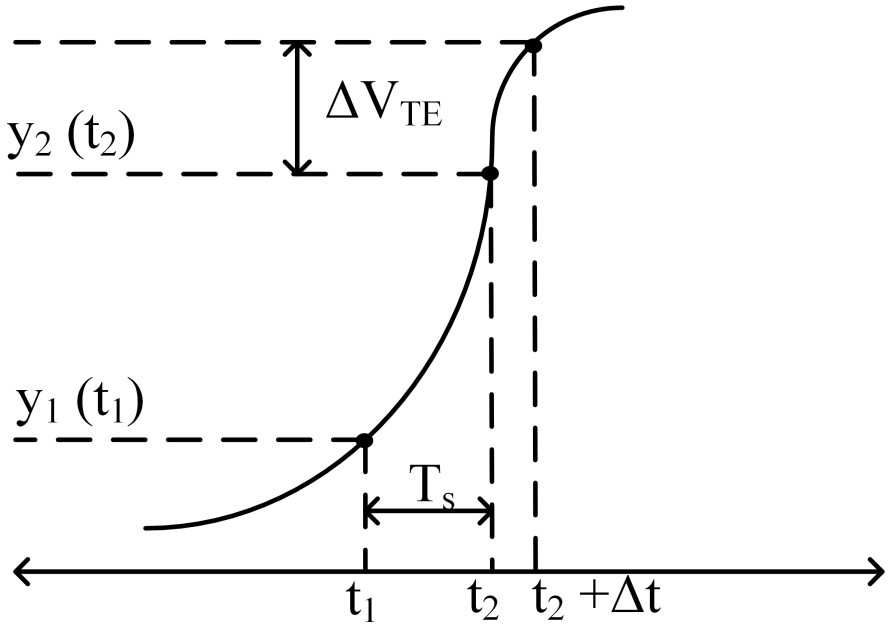


Figure 6.5 Timing Error due to error in sampling the input signal

Bandwidth Mismatch

Due to bandwidth mismatch, the frequency response of the sampling network changes with different input frequencies. This change in the magnitude and phase response manifest as gain and timing error (Kurosawa et al. (2001)). Fig. 6.6 shows the degradation in the SNR with bandwidth mismatch $\sigma(\Delta$ BW/BW). It can be observed that for bandwidth with 10x greater than the input frequency, an SNR of 12

bits can be attained if the bandwidth mismatch is less than 0.3%. Moreover, when the bandwidth is 2x greater than the input frequency, the SNR can be achieved of 9 bits when the bandwidth mismatch is less than 0.3% (Kurosawa et al. (2001)).

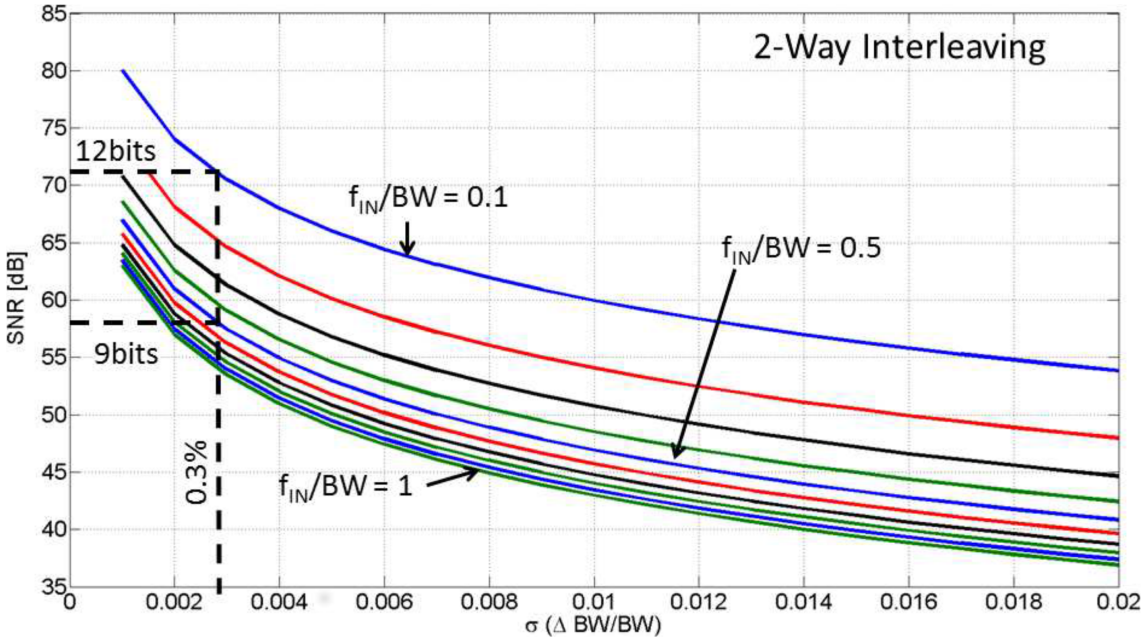


Figure 6.6 SNR Vs Bandwidth Mismatch for 2-channel TI ADC (Kurosawa et al. (2001))

Among the different 'interleaving (IL) spurs', the timing mismatch is the most difficult, as this error is dependent on the amplitude and frequency of the input signal. Many articles are found in the literature that tries to solve the timing mismatch. In (Greshishchev & et al. (2010); Poulton, Neff, Muto, Liu, Burstein & Heshami (2002)), a timing mismatch is calibrated in the foreground by using a signal generator that provides a test signal to the different channels in the TI-ADC. Then the relative timing information between the channels is exacted and analyzed using Fourier analysis. However, this technique is not able to track process, voltage, and temperature (PVT) variations. In (Hung-Chu Chen & Pileggi (2014); Stepanovic & Nikolic (2013)), uses an extra ADC to calibrate the timing mismatch. The extra ADC is used as a reference. However, this technique is less power-efficient. This work uses the technique by (Song et al. (2017)), this idea requires a comparator that acts as a window detector and detects a certain voltage region called the window to analyze if there is a timing mismatch.

6.2 Architecture of the Time-Interleaved ADC

This section introduces the architecture of the time-interleaved ADC along with the timing mismatch calibration. Each channel is implemented using a 2-bit/cycle sub-radix V_{cm}-based SAR-assisted pipeline ADC and the timing mismatch is implemented using the technique in (Song et al. (2017)).

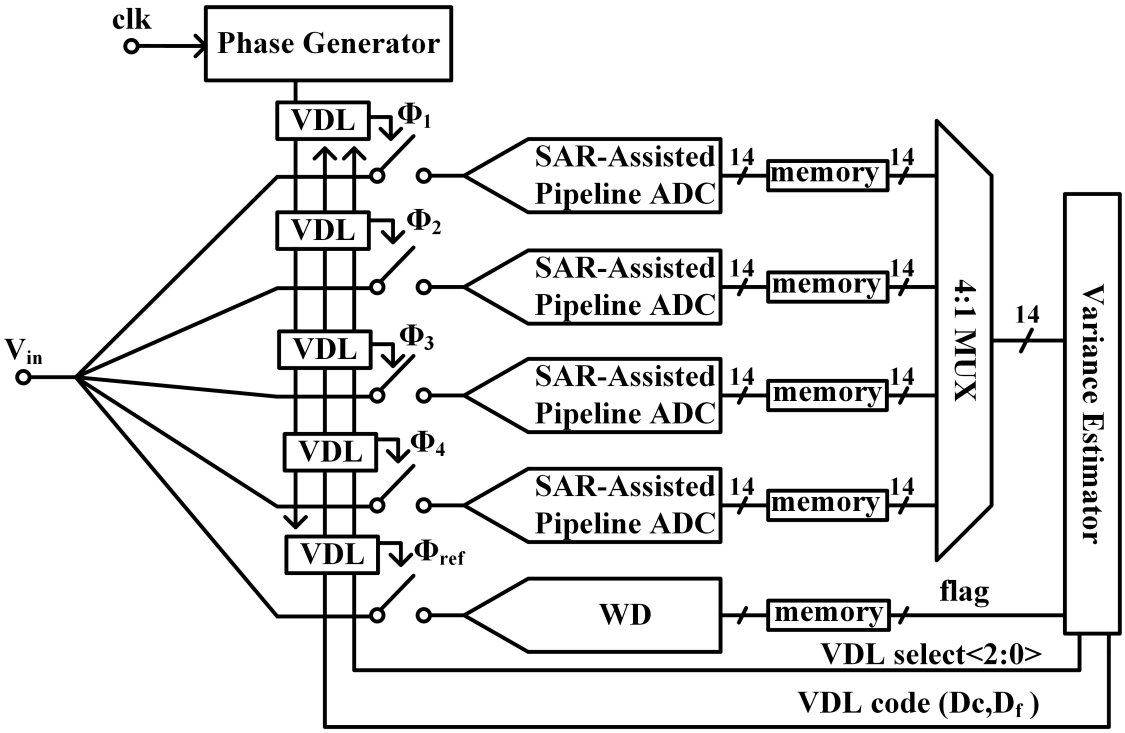


Figure 6.7 Architecture of the 4-channel TI ADC

Fig. 6.7 shows the architecture of the time-interleaved ADC, where each channel is designed based on the 2-bit/cycle sub-radix V_{cm}-based SAR-assisted pipeline ADC. A phase generator is designed to create clocks for each channel that is phase shifted by 90^0. A variable delay line (VDL) is used to create a delay in clock to adjust the timing mismatch. The window detector (WD) detects whether the input is within 1 LSB. The digital output of each channel is stored in a memory and then passed to 4:1 mux that stores the digital data in memory and then passed to a variance estimator that estimates the variance among the channel.

Fig. 6.8(a) shows the block diagram of the window detector that comprises a comparator (Razavi (2015b)), XOR gate, a positive-edge trigger flip-flop, and a current starved inverter to adjust the delay. When the reference clock (Φref) is logic '1', the comparator is in the reset phase and the capacitor C_1 tracks the input signal. During the negative edge of the Φ_{ref}, the comparator compares the input voltage

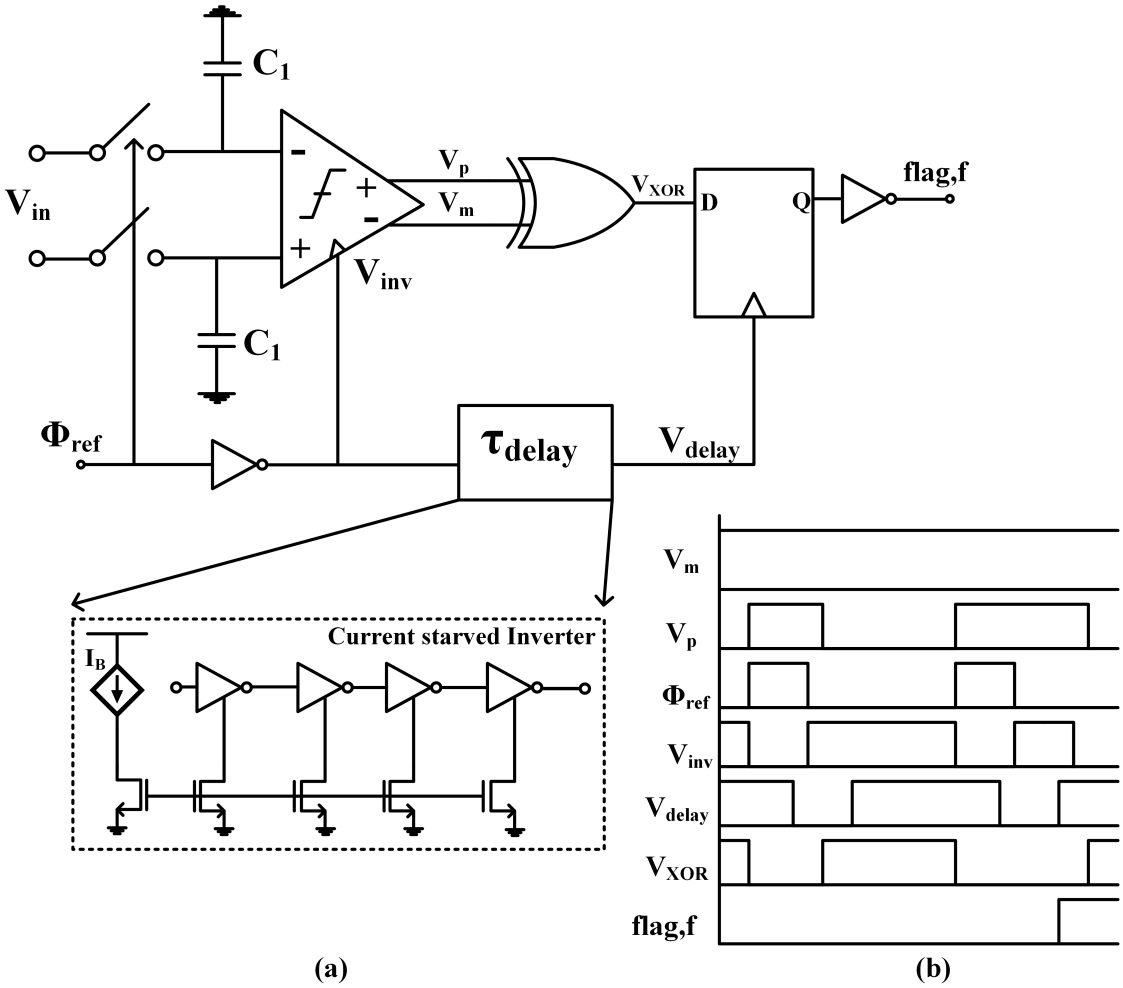


Figure 6.8 (a)Block diagram and (b) Timing diagram of the window detector

V_{in} and at the same time Φ_{ref} is delayed by the τ_{delay} block. The τ_{delay} block is adjusted such that $\tau_{delay} = \tau_{comparator} + \tau_{XOR}$, where $\tau_{comparator}$ is the delay of the comparator and τ_{XOR} is the delay from the XOR gate, when $|V_{in}| = W$. If $|V_{in}| < W$, then the comparator will take long time to compare in comparison to $\tau_{comparator}$, and hence, will activate the flag f to '1', as shown in Fig. 6.8(b). When $|V_{in}| > W$, then the comparator will take less time to compare in comparison to $\tau_{comparator}$, and hence, will not activate the flag f. The width of the window (W) is taken as 1 LSB such that the SNR is high (Song et al. (2017)).

The basic idea of the time-skew calibration is shown in Fig. 6.9. The window detector (WD) activates the flag when the input signal is within a certain window (W). Once, the flag is activated the variance estimator collects the digital output of the corresponding channel design based on 2-bit/cycle sub-radix SAR-assisted pipeline ADC. The digital outputs from all the 4-channels are collected when the flag ='1'. Then the collected digital outputs are plotted as shown in Fig. 6.9. When there is time-skew between the channels, the ADC code will be scattered to the

corners. Once, the variable delay lines (VDL) are calibrated, the ADC outputs will not be scattered as shown in Fig. 6.9.

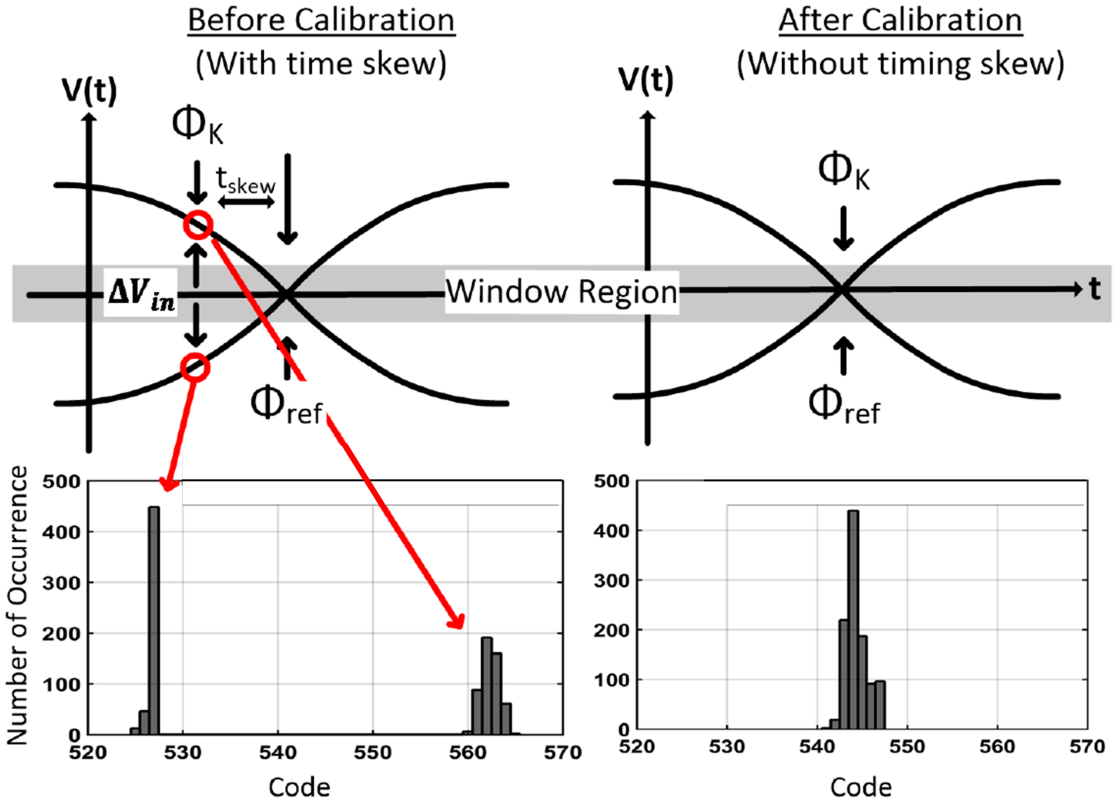


Figure 6.9 Idea of the time-skew calibration (Song et al. (2017))

Fig. 6.10 shows the block diagram of the phase generator where S_1 to S_4 are 90^0 apart with 25% duty cycle. The block diagram of the variable delay line (VDL) is shown in Fig. 6.11. The VDL can fine-tune and coarse-tune the clock signal. The coarse tuning was designed for 1 ps for each step and a fine-tuning of 200 fs for each step.

6.3 Post-Layout Results

Fig. 6.12 shows the layout of the 4-channel TI ADC with each channel designed based on 2-bit/cycle sub-radix Vcm-based SAR-assisted pipeline ADC. The 4-channel TI ADC is designed in 130 nm SiGe BiCMOS technology. The active area occupied by the ADC is 12 mm^2.

Fig. 6.13 (a) shows the post-layout SNDR, SFDR, and ENOB of 51.34 dB, 64.32 dB,

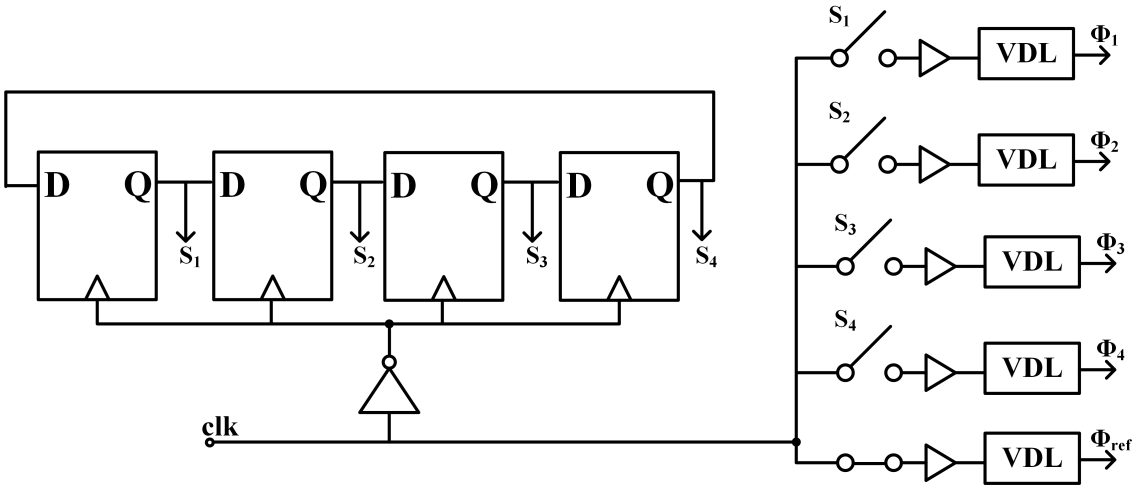


Figure 6.10 Block Diagram of phase generator

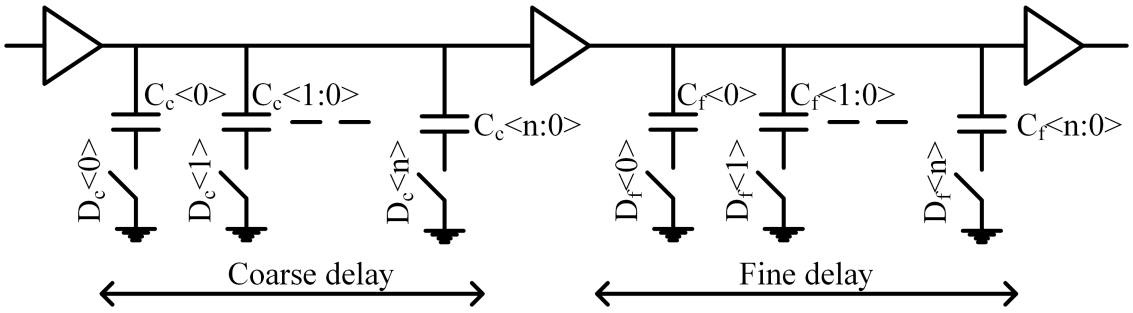


Figure 6.11 Block diagram of the variable delay line (VDL)

and 8.2355 bits, respectively at an input frequency of 1.5625 MHz with a sampling speed of 100 MS/s for the 4-channel TI ADC. Fig. 6.13 (b) shows the post-layout SNDR, SFDR, and ENOB of 50.04 dB, 54.78 dB, and 8.0198 bits, respectively with a sampling speed of 100 MHz at a near Nyquist frequency of 44.140625 MHz. Fig. 6.14(a) shows the post-layout SNDR and SFDR at different input frequencies for the sampling frequency of 100 MS/s. Fig. 6.14(b) shows the post-layout ENOB at different input frequencies for the sampling frequency of 100 MS/s. Table 6.1 shows the performance parameters of the 4-channel TI ADC.

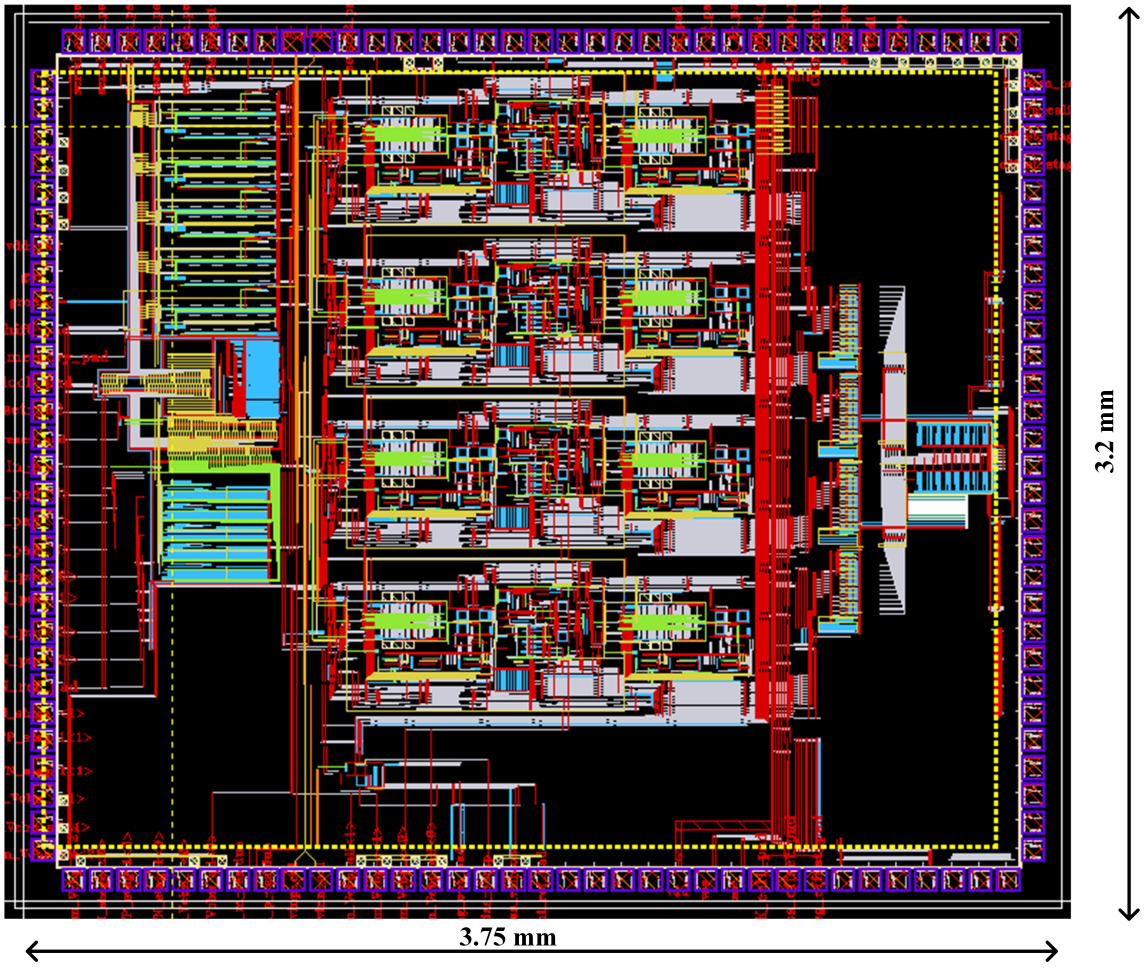


Figure 6.12 Layout of the 4-channel TI ADC

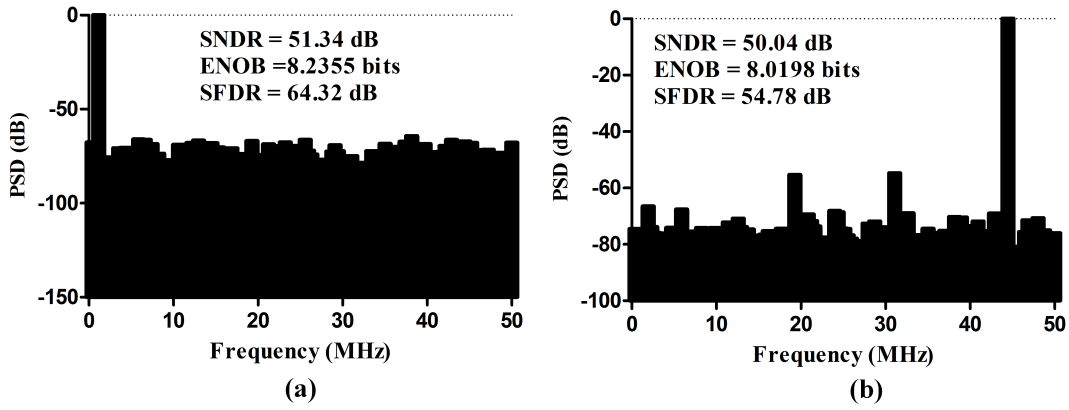


Figure 6.13 Post-layout simulation at an input frequency of (a) 1.5625 MHz and (b) at near Nyquist frequency of 44.140625 MHz

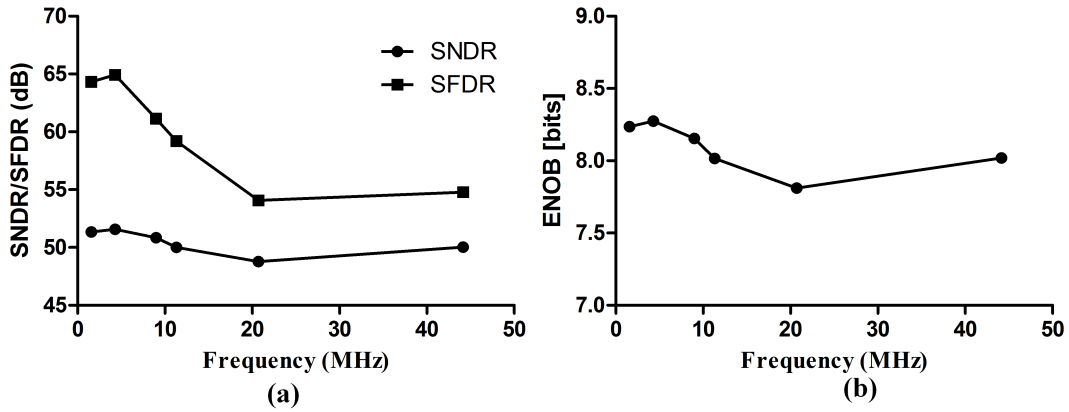


Figure 6.14 Post-layout (a) SNDR and SFDR (b) and ENOB for different input frequencies at a sampling frequency of 100 MS/s

Table 6.1
Post-Layout Performance Summary

Process [nm]	130
Supply Voltage [V]	1.2
Resolution [bit]	10
Sampling Rate [MS/s]	100
SNDR @ 1.5625 MHz input [dB]	51.34
SFDR @ 1.5625 MHz input [dB]	64.32
ENOB @ 1.5625 MHz input [bits]	8.2355
SNDR @ Nyq [dB]	50.04
SFDR @ Nyq [dB]	54.78
ENOB @ Nyq [bits]	8.0198
Power [mW]	64.71
FoM_W @ Nyq [pJ/conversion-step]	2.4932

7. CONCLUSION AND FUTURE WORK

The motivation of the dissertation started with the need to create a monolithic IC MIMO receiver that combines the RF blocks with the ADC. The ADC requirement for the MIMO receiver is that it requires an 8-12 bit with a sampling speed of 100 MS/s with low power. Based on the different types of ADC, the SAR-assisted pipeline ADC was chosen as it combines low power of the SAR ADC with the high speed of the pipeline ADC. A SAR ADC comprises three blocks: a DAC, a comparator, and a SAR logic. Based on the literature, it can be observed that for technology nodes $\geq$ 65 nm, the SAR logic propagation delay is dominant. Hence, a novel asynchronous SAR logic was designed based on a handshake architecture (the proposed SAR logic was designed by a former member of the group, and the analysis and measurement was done by the author of the thesis). The novel SAR logic was designed in a 6-bit V_{cm}-based SAR ADC and was compared with the conventional SAR logic designed in the same V_{cm}-based SAR ADC. Simulation results show a 75.3 % reduction of delay in a single conversion compared to the conventional SAR logic. The power consumed by the proposed SAR logic is 0.165 mW. On further analysis of the novel SAR logic, it was observed that the design can also reduce the impact of simultaneous-switching noise (SSN) on the SAR logic. These simultaneous-switching noise are created due to noises generated in the ground and power lines mainly due to Ldi/dt arising from the wire bond and package inductance. These SSN creates substrate noise which impacts the circuit. A simulation setup was created where an inductor varying from 1 nH to 9 nH with a step size of 1 nH was placed in series to the power supply and ground connected only to the proposed SAR logic and conventional SAR logic in the 6-bit V_{cm}-based SAR ADC. The series inductance was used to mimic the inductance arising from the wire bond and package inductance. The SSN parameters: V_{OHP}, V_{OHV}, V_{OLP}, and V_{OLV} were extracted for the proposed and conventional SAR logic during the sampling and conversion phase. It was observed that V_{OHP}, V_{OHV}, V_{OLP} and V_{OLV} has at least 40 %, 50 %, 65 % and 50 % improvement compared to the conventional SAR logic, respectively, during the sampling phase for different inductance values (L_{eff}) varied from 1 nH to 9 nH with a step size of 1 nH. Moreover, the V_{OHP}, V_{OHV},

V_{OLP} and V_{OLV} has at least 50 %, 20 %, 20 % and 40 % improvement compared to the conventional SAR logic, respectively, during the conversion phase for different inductance value (L_{eff}) varied from 1 nH to 9 nH with a step size of 1 nH.

Additionally, the difference in ENOB for different effective inductance (L_{eff}) values w.r.t to the ENOB without inductance for the proposed and conventional SAR logic was analyzed. It was observed that the ENOB reduced faster in the case of SAR ADC designed with the conventional SAR logic compared to the proposed SAR logic. It was observed that the number of bits reduced by more than 1-bit for L_{eff} greater than 8 nH in the case of conventional SAR logic, and the maximum reduction in the ENOB is around 0.4 bits in the SAR ADC designed using the proposed SAR logic.

Also, the settling time required for the power supply and ground signal during the sampling phase and conversion phase was analyzed for both the conventional and proposed SAR logic. It was observed that when the effective inductance (L_{eff}) is greater or equal to 4 nH, the settling time for both the power supply and the ground exceeds 5 ns in the conventional SAR logic, and the proposed SAR logic has a maximum settling time of 4.2 ns during the sampling phase. During the conversion phase, the maximum time to settle for the power and ground line is around 1 ns which is lesser than the settling time taken by the conventional SAR ADC.

The proposed asynchronous SAR logic based on handshake protocol was fabricated in an 8-metal CMOS process and occupies an area of 0.016 mm^2. The SNDR, SFDR, and ENOB were measured to be 32 dB, 42.65 dBc, and 5.023 bits, respectively at an input frequency of 1.3477 MHz with a sampling speed of 30 MS/s for the SAR ADC. The SNDR, SFDR, and ENOB were measured as 31.51 dB, 40.53 dBc, and 4.9434 bits, respectively with a sampling speed of 30 MHz at near Nyquist frequency. The measured INL and DNL are within -0.9668/+0.7291 LSB and -0.8461/+0.8805 LSB, respectively. The Walden Figure of Merit (FOM_W) at Nyquist frequency was attained as 0.229 pJ/conversion-step.

The proposed asynchronous SAR logic was then implemented in a sub-radix V_{cm}-based SAR-assisted pipeline ADC with a novel overshoot reduction technique implemented in the residue amplifier. This technique reduces the overshoot voltage and overshoot time created by the residue amplifier designed based on the zero-crossing-based circuit (ZCBC). The overshoot voltage and time degrade the dynamic range for the next stage SAR ADC and reduces the speed of the amplifier, respectively. The overshoot voltage was simulated for different corner cases and the range of the overshoot voltage was attained from 2.1 mV to 2.8 mV with an overshoot time ranging from 55.58 ps to 301.97 ps. The percentage reduction in the overshoot time

ranges from 80.30 % to 95.68 %. The area occupied by the ADC is 0.684 mm^2. The SAR-assisted pipeline ADC achieves an ENOB of 7.9344 bits and 6.6653 bits that corresponds to an SNDR of 49.53 dB and 41.89 dB with an input frequency of 520.83 kHz and at Nyquist rate of 7.5521 MHz, respectively with a sampling frequency of 16 MS/s. The SFDR attained was 55.23 dB and 50.14 dB with an input frequency of 520.83 kHz and at Nyquist rate of 7.5521 MHz, respectively with a sampling frequency of 16 MS/s. The INL and DNL were attained as -1.043/0.75 LSB and -0.86/1.13 LSB, respectively. The Walden Figure of Merit (FOM_W) at low frequency and at the Nyquist frequency was attained as 255 fJ/conversion-step and 615.77 fJ/conversion-step, respectively.

To improve the speed of the SAR-assisted pipeline ADC, the SAR ADC was designed using a 2-bit/cycle sub-radix V_{cm}-based SAR-assisted pipeline ADC along with the novel overshoot reduction technique. The 10-bit sub-radix two-stage SAR-assisted pipeline ADC occupies an area of 1.634 mm^2. The post-layout SNDR, SFDR, and ENOB were attained as 54.2 dB, 62.9 dB, and 8.7109 bits, respectively at an input frequency of 1.3393 MHz with a sampling speed of 28.571 MS/s. The post-layout SNDR, SFDR, and ENOB were attained as 53.93 dB, 61.87 dB, and 8.6658 bits, respectively with a sampling speed of 28.571 MHz at a near Nyquist frequency of 10.268 MHz. The INL and DNL were attained as +1.7067/-2.2149 LSB and +1.2867/-0.7459 LSB, respectively. The Walden Figure of Merit (FOM_W) at the Nyquist frequency was attained as 99.710 fJ/conversion-step.

To further improve the overshoot voltage and time, the comparator COMP1 was modified. The overshoot voltage was simulated for different corner cases and the range of the overshoot voltage was attained from 0.584 mV to 1.59 mV with an overshoot time ranging from 124 ps to 423 ps. The percentage reduction in the overshoot time ranges from 90.544 % to 98.012 %. The percentage reduction in the overshoot voltage ranges from 89.153 % to 97.67 %. The overshoot voltage attained is the lowest in the state-of-the-art works and has a comparable overshoot time with the other compared works. The improved version of the overshoot voltage and time reduction technique was implemented in the 2-bit/cycle sub-radix V_{cm}-based SAR ADC. The active area occupied by the ADC is 0.8812 mm^2. The post-layout SNDR, SFDR, and ENOB were attained as 56.67 dB, 66.07 dB, and 9.1216 bits, respectively at an input frequency of 1.171875 MHz with a sampling speed of 25 MS/s for the SAR ADC. The post-layout SNDR, SFDR and ENOB were attained as 56.57 dB, 62.98 dB, and 9.1046 bits, respectively with a sampling speed of 25 MHz at a near Nyquist frequency of 11.328125 MHz. The Walden Figure of Merit (FOM_W) at the Nyquist frequency was attained as 589.7 fJ/conversion-step. To the author's knowledge, the implemented 2-bit/cycle sub-radix V_{cm}-based SAR-assisted

pipeline ADC has a better performance compared to the SAR ADC designed in IHP 130 nm BiCMOS technology until now.

The 2-bit/cycle sub-radix V_{cm}-based SAR-assisted pipeline ADC was implemented in a 4-channel Time-Interleaved ADC with time-skew calibration. The active area occupied by the TI ADC is 12 mm^2. The post-layout SNDR, SFDR, and ENOB were attained as 51.34 dB, 64.32 dB, and 8.2355 bits, respectively at an input frequency of 1.5625 MHz with a sampling speed of 100 MS/s for the 4-channel TI ADC. The post-layout SNDR, SFDR, and ENOB were attained as 50.04 dB, 54.78 dB, and 8.0198 bits, respectively with a sampling speed of 100 MHz at a near Nyquist frequency of 44.140625 MHz. The Walden Figure of Merit (FOM_W) at the Nyquist frequency was attained as 2.4932 pJ/conversion-step.

For future works, the SAR ADC resolution and power can be improved by the combination of noise shaping SAR ADC (Guo & Sun (2016)) with the technique implemented to reduce the KT/C noise as suggested by (Kapusta, Zhu & Lyden (2014); Liu, Tang, Zhao, Shen & Sun (2020)). With these techniques, the area of the SAR ADC is reduced as the total sampling capacitance can be made smaller than the KT/C noise criteria. The above techniques also help in improving the ENOB attained from the ADC.

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