PROCESS INTEGRATION AND TECHNOLOGY DEVELOPMENT FOR LOW-COST, ACCESSIBLE HIGH DENSITY INTERCONNECT (HDI) PRINTED CIRCUIT BOARDS (PCBs)

by
EKIN ASIM ÖZEK

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Approved by:

Asst. Prof. Murat Kaya Yapıcı
(Thesis Supervisor)

Prof. Dr. Yasar Gürbüz

Asst. Prof. Dr. Sinan Kazan

Approval Date: December 17, 2021

ABSTRACT

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Thesis Advisor: Asst. Prof. Dr. Murat Kaya Yapici

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With the growing demand towards 5G and beyond mobile communications, multilayer printed circuit boards utilizing microvias and populated network of electrical wiring to enable highly dense three-dimensional circuit assemblies; otherwise known as high-density interconnect printed circuit boards (HDI-PCB), are becoming a critical enabler for next generation electronic equipment. Although the fundamental difference between HDI-PCBs and traditional PCBs is essentially in the density of electrical interconnects, such difference calls for a paradigm shift in the printed circuit board architecture requiring multilayer stack-up with laser-drilled microvias, buried and blind vias for layer-to-layer electrical interfacing as well as linewidths with resolutions far below typical PCBs.

All in all, HDI-PCBs require new fabrication strategies, optimized unit processes (e.g. lithograpy, etching, via drilling and plating) and integration thereof with stringent process control to achieve the specifications set-forth by different HDI-PCB classifications, which understandably comes at a cost and requires special infrastructure. The intention of this thesis is therefore to provide an accessible and low-cost process flow to realize HDI-PCBs by leveraging the capabilities of mechanical drilling to their extent along with basic lab equipment to achieve Type-III-based, 2-N-2 HDI-PCB architecture.

A detailed and optimized fabrication flow is developed in order to establish a reliable and repeatable process flow starting from stacking of the “base” materials (prepreg/core/Cu laminates) up to the final solder mask level. In the developed HDI-PCB process technology, each unit process is experimentally verified and optimized, after which all the unit processes are sequentially performed to achieve an integrated process flow.

Specifically, the developed and optimized unit processes include: prepreg/copper lamination, mechanical microvia (100 µm) drilling, microvia metallization (electroless and electroplating of copper, reverse-etch of overfilled vias), high-density fine line lithography and low-undercut etching.

Accordingly, based on the developed process technology, prepreg/Cu lamination was achieved with a 5.93% height difference for sequential build-up architecture. Drilling of 100 µm vias in 175 µm via pads with center-to-center spacing of 250 µm was achieved within a 10% error margin throughout 10×10 cm active HDI board area. Dry and liquid photoresists systems for patterning of copper layers with 50 µm line width and 50 µm line gap is achieved on 18 µm copper foils. Electroless copper plating for the metallization of holes and selective copper electroplating for via filling process flow is developed and realized. Dry film solder mask (75 µm) application was achieved by streo-microscope assisted manual alignment and UV-box flood exposure system, overcoming the limits of typical mask aligner system for thick materials requiring large depth-of-focus microscopes for alignment.

ÖZET

DÜŞÜK MALİYETLİ, ERİŞİLEBİLİR YÜKSEK YOĞUNLUKLU ARA BAĞLANTILI(HDI) BASKI DEVRE KARTLARI (PCB) İÇİN SÜREÇ ENTEGRASYONU VE TEKNOLOJİ GELİŞTİRİLMESİ

EKİN ASIM ÖZEK

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Anahtar Kelimeler: yüksek yoğunluklu bağlantı, baskı devre kartı, HDI-PCB, çok katlı, süreç teknolojisi, üretim

5G ve ötesi mobil iletişime yönelik artan taleple birlikte, son derece yüksek yoğunluklu devre yapılarını oluşturmak için mikro vialardan ve yoğun elektrik bağlantılarından yararlanan çok katmanlı devre kartları, yüksek yoğunluklu ara bağlantılı baskı devre kartları (HDI-PCB) olarak bilinen teknoloji, yeni nesil elektronik ekipmanlar için kritik bir etkinleştirici teknoloji haline geliyor. HDI PCB'ler ve geleneksel PCB'ler arasındaki temel fark esasen elektrik ara bağlantılarının yoğunluğunda olmasına rağmen, bu fark devre yığını oluşturmada yaklaşım farklılığı gerektirir. HDI-PCB'lerde lazerle delinmiş mikrovialar, gömülü ve kör vialar ile katmandan katmana elektrik bağlantısı sağlanır ve geleneksel PCB'lere göre oldukça yüksek çözünürlük ile daha dar hat genişlikleri gerekir.

Sonuç olarak, HDI-PCB'ler yeni üretim stratejileri, optimize edilmiş birim süreçleri (ışıklandırma, aşındırma, via delme ve bakır kaplama, vb.) ve bunların farklı HDI-PCB sınıflandırmaları tarafından ortaya konan spesifikasyonları elde etmek için maliyetli ve yüksek süreç kontrolü gerektiren entegrasyonu gerektirir. Bu nedenle, bu tezin amacı, Tip-III tabanlı 2-N-2 HDI-PCB yapısını elde etmek için temel laboratuvar ekipmanı ile birlikte mekanik delme yeteneklerinden yararlanarak HDI-PCB'leri gerçekleştirmek için erişilebilir ve düşük maliyetli bir süreç akışı sağlamaktır.

"Temel" malzemelerin (prepreg/core/Cu laminatlar) istiflenmesinden başlayarak nihai lehim maskesi seviyesine kadar güvenilir ve tekrarlanabilir bir süreç akışı oluşturmak için ayrıntılı ve optimize edilmiş bir üretim akışı geliştirilmiştir. Gelişmiş HDI-PCB süreç teknolojisinde, her birim süreç deneysel olarak doğrulanmış ve optimize edilmiş,

ardından tüm birim süreçlerin entegre edildiği bir süreç akışı elde etmek için sırayla gerçekleştirilmiştir. Spesifik olarak, geliştirilmiş ve optimize edilmiş ünite süreçleri şunları içerir: prepreg/bakır laminasyonu, mekanik mikro via(100 µm) delme, mikro via metalizasyonu (elektrotsuz bakır kaplaması, akımlı bakır kaplaması, aşırı doldurulmuş yolların tersine aşındırılması), yüksek yoğunluklu ince çizgi litografisi ve düşük desen altı aşınmalı bakır aşındırması.

Buna göre, geliştirilen proses teknolojisine dayalı olarak, sıralı yapı mimarisi için %5,93 yükseklik farkı ile prepreg/Cu laminasyonu elde edilmiştir. Merkezden merkeze 250 µm aralıklı 175 µm via pad'leri içinde 100 µm vialaların delinmesi, 10×10 cm aktif HDI PCB alanı üzerinde %10'luk bir hata payıyla 18 µm bakır folyolar üzerinde 50 µm çizgi genişliği ve 50 µm çizgi aralığı ile bakır tabakaların şekillendirilmesi kuru ve sıvı fotorezist sistemleri ile sağlandı. Deliklerin metalizasyonu için akımsız bakır kaplama ve doldurma işlemi akışı için seçici akımlı bakır kaplama geliştirildi ve gerçekleştirildi. Kuru film lehim maskesi (75 µm) uygulaması, hizalama için geniş odak derinliği mikroskopları gerektiren kalın malzemeler için tipik maske hizalama sisteminin sınırlarını aşarak, streo-mikroskop destekli manuel hizalama ve UV-kutu sistemi ile sağlandı.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

1. INTRODUCTION

Since the dawn of the modern electronic age, printed circuit technology has been the primary enabler for modern electronic devices. It was unavoidable that the unique property of multiple connections at a single solder step, resulting in vast numbers of connections, would become important, and it would continue to be so. Furthermore, printed circuit technology has demonstrated its technological value as it has improved and evolved in response to designers' needs, constraints and advancements in packaging technology, and market demands for smaller, lighter, and less expensive products.

Advances in printed circuit technology have been a series of revolutions that have been required to keep up with the smaller and denser component architecture's massive interconnection needs, resulting in evolutionary eras when new generations of printed circuit technologies are suggested and adapted. Planar non-conductive boards with conductive patterns establishing connections between circular rings around holes that component leads sit through were the first generation of printed circuits. The ability to embed a conductive surface into a hole in a non-conductive material was the next major breakthrough that emphasized the importance of printed circuit technology and laid the foundation for what we see today. The plated through-hole was conceived as a result of this revolution, enabling integrated circuitry on two sides and across multiple layers. We would not have the ubiquitous electronic items that have become essential in our life without the invention of the plated through-hole.

Board technology progressed reliably and slowly as long as the components had leads that penetrated the circuit board. Surface mount technology, on the other hand, ushered in a new era of technological advancement. Surface mount is more environmentally friendly because component leads do not penetrate the substrate board. Component sizes

were no longer limited by the necessity for relatively large through-hole leads, board technology had to adapt to accommodate this change. These next-generation boards have ability to shrink down to the size of a chip. Furthermore, inner layers might be used without leaving any space for holes through the board, resulting in full three-dimensional electrical interconnects. Leads can now escape from any location on the package because they are no longer needed to pass through the package's boundary. To accommodate more board connections, board designers and manufacturers were compelled to invent ways to access these ever-smaller connection points. Instead of using lead connections, this was usually accomplished by penetrating the board with vias whose primary function was circuit continuity rather than lead connection. Board feature dimensions began to shrink from fractions of an inch to thousandths of an inch as a result of the introduction of the Ball Grid Array (BGA), where traditional manufacturing technologies could no longer keep up with this demand.

A new revolution in technology had begun, called the Density Revolution, which is still going on. The term "high-density interconnect" (HDI) has been officially coined. At first glance, HDI appeared to present a challenge in the form of smaller vias due to the near impossibility of mechanical drilling. As a result, HDI immediately raised key challenges in printed circuit technology, including materials, imaging, metallization (including gold plating), testing, assembly, and design (which is particularly important due to the complex geometries involved, but also due to the electrical properties of printed circuit boards). The board has progressed from a simple interface device to an essential component of the overall product design.

1.1. Evolution of Electronics

Electronics is a very new industry, having only been around for almost 60 years. The invention of communications, radar, and ammunition fusion (particularly the radar-altimeter electronic fusion for the first atomic bomb) spurred electronics to become the world's greatest industry, surpassing all others, during World War II. To produce a functional unit, all electronic components must be integrated and assembled. In recent

years, the design and fabrication of these linkages have evolved into a distinct field known as electronic packaging. The printed wire board has been the basic building block of electronic packaging since the 1940s (PWB). To produce the most sophisticated prototypes of these printed wire boards, the high-density interconnect (HDI) printed circuit boards (PCBs), this thesis delves into advanced design principles and fabrication techniques in depth.

The fundamental principles, key benefits, and potential stumbling blocks that must be considered when selecting high-density interconnection methods for electronic systems, as well as the currently available choices, are discussed in this chapter.

1.2. The Traditional Multilayer

The conventional multilayer PWB has been around for more than 50 years. The design guidelines have been evolving with minor differences. In 1968, the ROM for the Hewlett-Packard HP-9100 desktop programmable computer was built from a 16-layer FR-4 multilayer with sheets of PTFE interleaved between the prepreg layers. The 512 64-bit words of the basic operating system were created by etching 1s and 0s onto 0.150 mm traces and gaps, which were subsequently read by high-speed pulses through coupling. The 100-step programmes, as well as the variables, were stored in the ferrite memory. The computer was turned from a million-dollar, air-conditioned office behemoth to a desktop computer for "everyman" thanks to this concept. The ROM PWB was necessary because integrated circuits (ICs) had only 12 gates per chip at the time, which was significantly less than the 32,768 bits (131,072 gates) required for the operating system ROM. Consider how, three years later, in 1971, Hewlett-Packard introduced the HP-35 calculator, which reduced the desktop to the size of a pocket-sized portable calculator. This progress in the device level signaled the start of the modern era of portable electronics.[1]

1.3. Multilayer Problems

Multilayer PWB design flow has not changed in 50 years and still conventional layer structures of signal, power, and ground are present. Copper traces, spaces, and via holes have gotten smaller over the years, but not significantly so that new products from component vendors (particularly IC) rely on HDI. Current and future integrated circuits technologies that show the trend of increasing clock rates and operating frequencies are sensitive to multilayer TH capacitance and inductances. The adoption of HDI in mobile devices has led the high-performance, volume, and cost-sensitive market segments such as automotive, telecom, consumer electronics, to abandon multilayer in favour of HDI-enabled technologies. Classical multilayer PWB offers reduced functionality and design flexibility with greater cost as compared to HDI so that HDI design flow adoption becomes unavoidable for advanced products.

1.4. High-Density Interconnect Multilayer Platform

Fabrication has established itself as the most important link between the base materials and the final value presenting product. In order to produce essentially comparable HDI structures, industry around the world is currently using more than twenty different process flows. Microvia fabrication and small (100 μm) through-holes are straightforward outcomes of advances in lasers, CNC tooling, etching, and processable materials. Alignment, fine-line lithography, metallization, and plating are only a few examples of fundamental problems. This thesis provides a hybrid methodology of alignment and fabrication process flow linking cleanroom processes with industry standards of HDI. On the HDIs, they all have to perform at a very high level. Although this is a time-consuming process to develop and maintain, it is valuable technology to attain and utilize in all printed circuit board manufacturing processes.

1.5. Basics of High-Density Interconnect Technology

1.5.1. Interconnect Density

Three interconnected performance measurements or metrics for the HDI process must be considered when creating an HDI design. Complexity of Assembly measures the difficulty of surface-mounted component assembly. Component Density (C_d), which is measured in components per square inch (or per square centimeter), and Assembly Density (A_d), which is measured in leads per square inch (or per square centimeter), are two key metrics in electrical design.

$$C_d = {}^{p}/_{a}, \quad (1)$$

$$A_d = {}^{1}/_{a} \quad (2)$$

Component Complexity (C_c) is a measure of the degree of sophistication of components, as measured by the average number of leads (I/Os) per part. The component lead pitch is a second metric to consider.

$$C_C = {}^{1}/_{p} \quad (3)$$

The density (or complexity) of a printed circuit (W_d) is determined by the average length of traces on that board per square inch, including all signal layers. Inches per square inch or centimetres per square centimetre are the metric units. A second parameter is the number of traces per linear inch or centimetre. The PWB density was calculated assuming that each net had an average of three electrical nodes and that each component lead was a net node. As a result, an equation [2] is derived that states that the PWB density is equal to β times the square root of the parts per square inch multiplied by the average number of leads per part. β is 2.5 for high analog/discrete, 3.0 for analog/digital, and 3.5 for digital/ASIC:

$$PWB\ Density\ (W_d) = \beta\sqrt{[C_d]}C_c = \beta\sqrt{[parts\ per\ sq.cm]}(ave.leads\ per\ part) \quad (4)$$

Where *p* denotes the number of components (parts), *l* denotes the total number of leads on all components, and *a* denotes the area of the board's top surface (square inches).

1.5.2. High-Density Interconnect Specifications

When it comes to HDI design, the International Product Code Guidelines, Standards, and Specifications can be used as a starting reference point (www.ipc.org). Four of these standards are critical in HDI design [3] :

- IPC-2226, Sectional Design Standard for High-density Interconnect (HDI) Printed Boards
- IPC/JPCA-2315, Design Guide for High-density Interconnect Structures and Microvias
- IPC/JPCA-4104, Dielectric Materials for High-density Interconnect Structures: Qualification and Performance Specification (HDI)
- IPC-6016, High-density Interconnect (HDI) Structures Qualification and Performance Specification

As a review, these standard-setting documents are briefly discussed in relation to specific HDI design techniques.

IPC-2226 standard covers microvia formation, wiring density selection, design principles selection, interconnecting structures, and material characterisation. Microvia printed circuit boards must meet the specifications outlined in this document.

IPC-4104 standard identifies high-density interconnect structure materials. The slash sheets that define many of the thin materials used for HDI can be found in the IPC-4104 HDI Materials Specifications. In high-performance multilayers, material properties are the most important factor. The selection of materials, which will determine performance and fabrication technology, is still the most important step in HDI design. There are an increasing number of new materials available for HDI design that are not available for conventional multilayers. Dielectric Insulators (*IN*), Conductors (*CD*), and Conductor and Insulators (*CI*) are the three main material types represented in the slash sheets of material

characteristics.

These insulator materials come in four varieties:

- Copper clad resins (RCF, polyimide film, etc)
- Laminates (reinforced epoxy, Cyanate Ester, etc.)
- Liquids (epoxies, photosensitive, BCBs, etc.)
- Films (un-reinforced epoxy, liquid crystal polymers, etc.)

Reinforced and non-reinforced laminates and prepregs are two types of materials that can be classified mechanically. Non-reinforced materials have a lower dielectric constant (Dk), they are thinner than reinforced laminates, and they may be photo-imageable, while reinforced materials have better dimensional stability, a lower coefficient of thermal expansion (CTE), and they are less sensitive to thermal cracking. The most common HDI materials are glass reinforced laminates and resin-coated copper foils (RCF), in this thesis glass reinforced laminates and glass reinforced prepreg-Cu pairs are used in stackup fabrication.

IPC-6016 document contains general specifications for high-density substrates not covered by other IPC documents such as IPC-6011, the generic PWB qualification, and performance specifications.

1.5.3. Basic High-Density Interconnect Structures

A new technology is needed to efficiently fabricate high performance, high frequency interconnect array packages with large number of I/Os. The true usefulness of HDI may be recognised when it comes to extremely small holes known as microvias, despite the recent development of concepts such as sequential multilayer and Buildup Multilayer (BUM). The HDI Design Committee of the IPC defines a microvia as any hole with a diameter of less than 150 um.

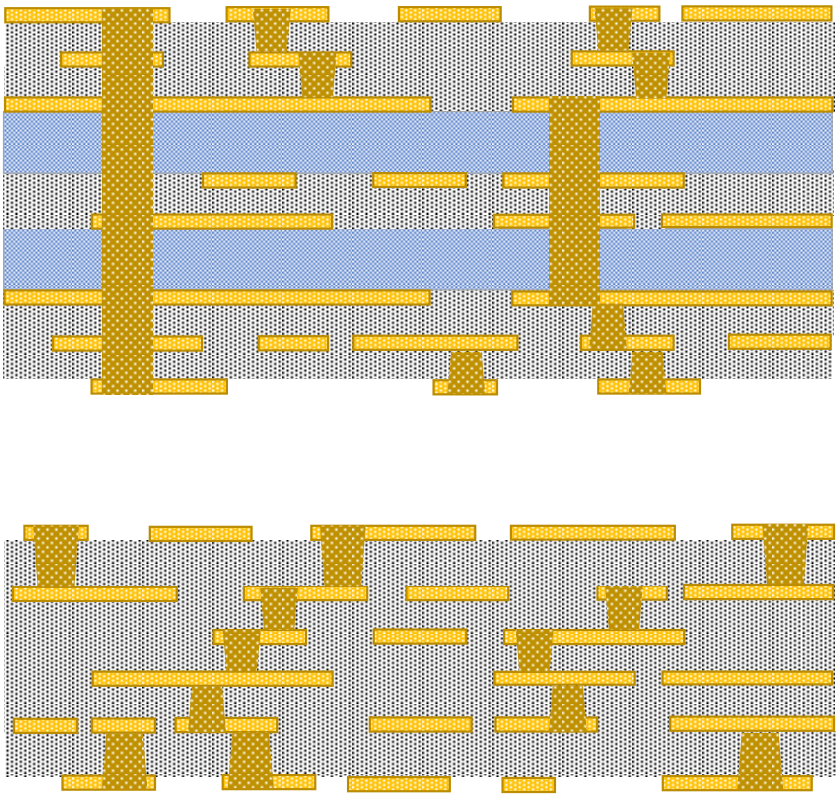


Figure 1 Most common stack-ups: Sequential buildup (top) and any-layer structure (bottom).

1.5.4. Seven Most Common High-Density Interconnect Stack-Ups

Micron (micrometre) ranges are becoming more relevant in packaging technology as package sizes shrink. The two most fundamental HDI structures that are widely available are "buildup" or "sequence buildup" structures and "any-layer" structures. As shown in Figure 1, these two can bear a striking resemblance to one another. IPC-2226 Design Standard for HDI Printed Boards has a type-based organisational structure. Type I, Type II, Type III, Type IV, Type V, and Type VI are the six distinct types of characteristics. It is important to remember that the extra microvia structure could be present on a different sort of structure rather than as categorized in IPC-2226. Furthermore, this classification is based on microvia appearance, blind vias may exist in all types. As a result, the following definitions apply to all forms of HDI boards:

TYPE I 1 [C] 0 or 1 [C] 1 – with through vias connecting the outer layers. A high-density interconnect substrate with interconnected plated microvias and plated through-holes for

connectivity is specified in this construction. A single microvia layer is fabricated on one or both 1[C]0 or 1[C]1 side of a PWB substrate core in Type 1 topologies. A single microvia layer is fabricated on one or both sides 1[C]0 or 1[C]1 of an underlined PWB substrate core in Type 1 architectures. Conventional PWB building processes are typically used to create the PWB core substrate. This substrate could be either rigid or flexible. The substrate might be as basic as a single circuit layer or as complex as a premade multilayer PWB with buried vias (BV), depending on the purpose. A single layer of dielectric material is then applied to the top of the core substrate to complete the construction. Microvias appear in the dielectric between layers 1 and 2, as well as between layers n and n-1. The structure's layers 1 through n are then connected by through-holes. Depending on the device's intended purpose, the microvias and through-holes are then metallized or filled with conductive material. The fabrication, as well as the circuitry for layers 1 and n, is finished.

TYPE II 1 [C] 0 or 1 [C] 1 – with buried vias in the core and may have through vias connecting the outer layers. Except for Type I, Type II contains all of the HDIs layers present in Type I. The differentiating feature of the distinction is in the core layer [C], where through-via containing core exists in Type II structure. It is feasible to fabricate through-vias in the core before laminating the HDI layers using Type II of the design. The only difference is that the core through-vias are drilled and metallized before the HDI layers are laminated.

Type III ≥ 2 [C] ≥0 – may have buried vias in the core and may have through vias connecting the outer layers. An HDI substrate with interconnected plated microvias and plated through-holes for connectivity is specified in this construction. The development of two microvia layers on either one 2[C]0 or both 2[C]2 sides of an undrilled PWB substrate core is classified as a Type III construction. Conventional PWB building processes are typically used to create the PWB core substrate. This substrate could be either rigid or flexible. The substrate might be as basic as a single circuit layer or as complex as a premade multilayer PWB with buried vias, depending on the purpose. A layer of dielectric material is then applied to the top of the core substrate to complete the construction. Microvias connect layers 2 and 3, and layers n-1 and n-2 of the dielectric. It's critical to metallize or fill the initial microvia layer with a conductive material before circuitizing the device. After that, the second layer of dielectric material is applied to the

circuitized layer, and microvias are fabricated for layers 1 and 2, as well as layers n and n-1, as shown in Figure 2. Then, to connect layers 1 and n, through-holes are drilled. The microvias and through-holes are metallized or filled with a conductive substance to complete the design. The fabrication, as well as the circuitry for layers 1 and n, is completed.

TYPE IV ≥ 1 [P] ≥0 – where P is a passive substrate with no electrical connection. This concept proposes a high-density interconnect substrate in which microvia layers serve as redistribution layers on top of an existing drilled and metallized passive substrate. Typically, the PWB or metal core substrate is created using standard PWB processes. This substrate might be rigid or flexible.

TYPE V – Coreless constructions using layer pairs. This construction depicts a high-density interconnect substrate in which the microvias may appear in any layer. Cores are drilled, metallized, and pattered before lamination in this architecture. Pre-patterned cores are then laminated and vias are filled with conductive material to complete the design. A rigid or flexible substrate may be used for this purpose.

TYPE VI - Alternate constructions. This construction proposes a high-density interconnect substrate in which core structure does not appear. Prepreg/Cu layers are laminated, patterned, and metallized sequentially to achieve any-layer structure.

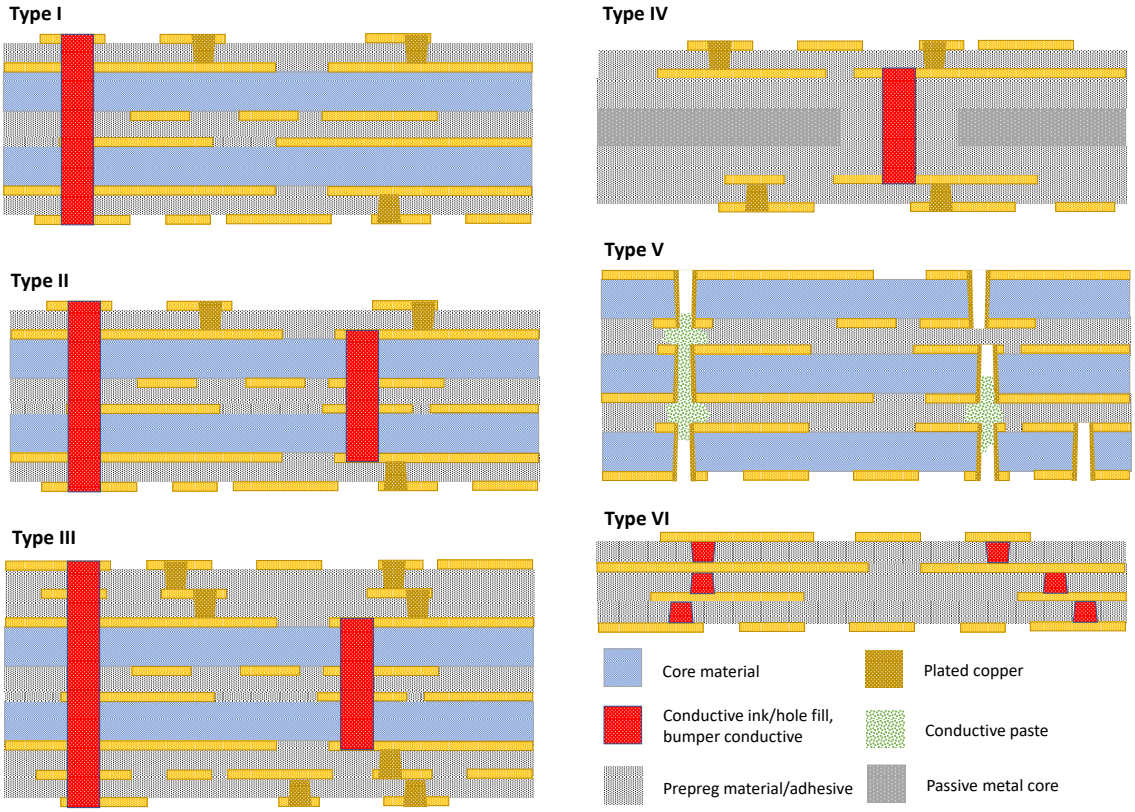


Figure 2 IPC-2226 six types of HDI structures.

1.6. The Layer Stack-Up Alternatives

Many of the more typical HDI stack-ups used to reduce the number of through-hole vias in a design are shown in Figure 3. The three most popular HDI stack-ups are shown with the IPC-Type structures (I, II & III). Dielectric materials such as standard prepregs, laser-drillable prepregs, RCCs, reinforced RCCs, and BC cores are all viable between Layers-1 and Layer-2. It is feasible to employ a "skip-via" from Layer-1 to Layer-3, as shown in Figure 3, if the dielectric is thin enough, eliminating the cost of an IPC-Type III structure and therefore saving money. Any dielectric thickness less than 0.005 inches (0.125 mm) connects GND and PWR, resulting in lower power supply (PS) impedance and lower PS resonances and noise.

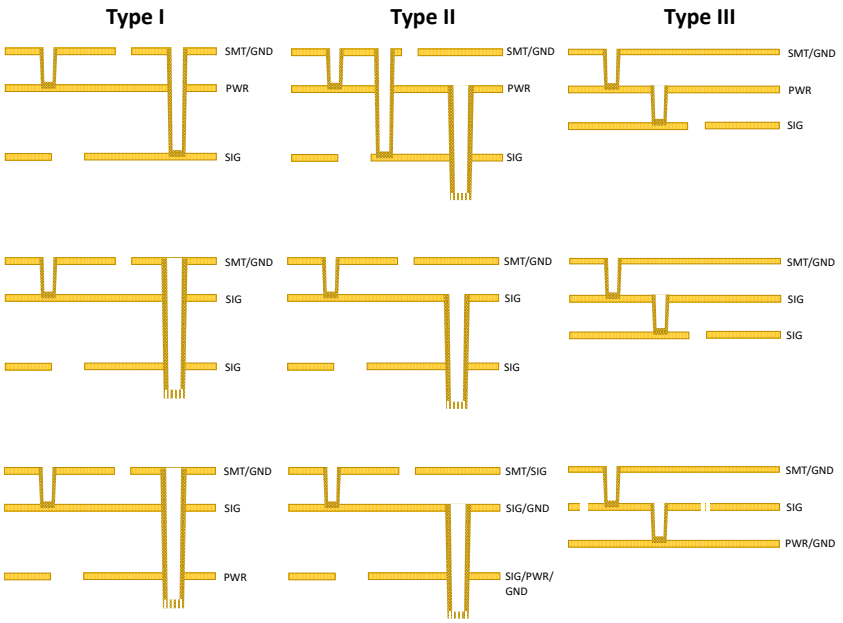


Figure 3 Surface layer alternatives for the most common stack-up architectures.

1.7. Stacked Vias

HDI is compounded further when fine-pitch ball-grid-arrays (BGAs) are used and the design parameters do not provide for clearance for staggered blind vias. This is an unavoidable problem when working with HDI. When this problem occurs, it is important to stack microvias one on top of the other or a microvia on top of the buried via. These two scenarios are depicted in Figure 4: On the left, a microvia is layered on top of a filled and remetallized buried via; on the right, a microvia is placed on top of a filled and remetallized buried via. The right figure comprises two laser-drilled microvias. The microvia in the bottom layer (Layer 2/3) has been entirely plated.

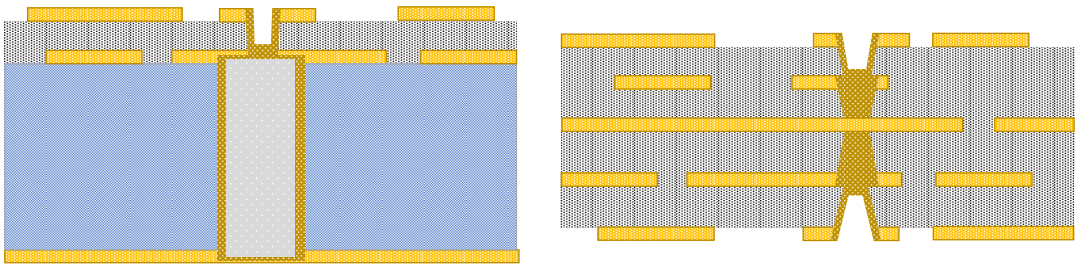


Figure 4 Stacked microvia configuration: Microvia placed on top of the filled and capped buried via (left), and microvia stacked sequenctially on eachother (right).

2. OVERALL PROCESS FLOW AND RELATED FABRICATION PROCESSES

2.1. Materials for High-Density Interconnect

The materials utilized to fabricate HDI circuits are discussed in this chapter. There are several excellent guidelines on printed circuit board materials (for example, Coombs' Printed Circuits Handbook), but specific focus on those materials that are unique to HDI's manufacturing process are investigated. Given that nearly all HDI boards have layers that are identical to those on traditional printed circuit boards, a thorough examination is beneficial.

Based on BPA Consulting Ltd. statistics, the global HDI materials market was 51 million square metres in 2006, and 83 million square meters in 2020 with majority of the utilized materials being laser-drillable prepregs, resin coated copper, and conventional prepregs.

2.1.1. Dry Photo Film Dielectric

Photosensitive dry film dielectrics were originally considered to be the ultimate high-density interconnect (HDI) dielectric due to the fact that no additional equipment was required to create the vias. This was not the case, as these were negative acting photosystems. It was necessary to use ultraviolet energy to cure the dielectric permanently, as a result of negative action. It would be beneficial for cleanroom users to utilize dry photofilm dielectrics since this material is already suitable for Class-100 environment, however, over the years, because of the fact that expensive cleanroom infrastructure requirement, this dielectric is limited to original equipment manufacturers (OEMs) in Japan, who have their own manufacturing facilities.

2.1.2. Photo Sensitive Liquid Dielectric

Liquid photosensitive dielectrics degrade similarly to dry film. They have the advantage of producing less waste and allowing for finer coating thickness control. The significant demand for crucial coating equipment and clean-room space is their main disadvantage for industry players. Yet for the research and prototyping purposes, after MEMS chips or ICs are fabricated, dependence for PWBs for testing and measurement to outer suppliers are not ideal. For emerging high frequency applications such as beam forming systems, unconventional buildups are necessary, however, photosensitive liquid photo dielectric is not a common material utilized.

2.1.3. Copper Foil

The sole conductor of electrical currents available to designer is copper metal on printed wiring boards (PWBs). Copper foils come in three different types that are commonly utilised in the fabrication of printed wire boards.

- Electroplated
- Electrodeposited
- Wrought (rolled annealed)

2.1.3.1. Electroplated Copper

The fundamental function of electroplated copper is to deposit copper in through holes. As a result, the HDI fabrication process flows at least includes a step that electroplates via holes. The number of electroplating steps is determined according to type selection, intended application, and metallization scheme (additive, semi-additive, subtractive).

2.1.3.2. Electrodeposited Copper

Electrodeposited (ED) copper foil is the most often used foil in the fabrication of printed circuit boards. Copper is electroplated onto a cylindrical drum, commonly made of

titanium, using a pure copper sulfate/sulfuric acid solution in an electrochemical process. ED foil is used in the production of electronic devices. The thickness of the generated foil is determined by the rotation speed.

2.1.4. Core and Prepreg Materials

The fundamental material components of printed circuit boards are polymer resin (dielectric), which may or may not contain fillers, reinforcement, and metal foil. The layers of dielectric material, either with or without reinforcement, are placed between the layers of metal foil to form a printed circuit board.

The majority of the dielectric materials used in the fabrication of printed circuit boards are reinforced in the resin system as part of the overall design. It is the most frequent type of reinforcement to have fibreglass woven into the structure. Fabric made of woven fibreglass is comparable to any other sort of cloth in that it is composed of separate filaments that are woven together to make one continuous piece of material on a weaving loom. The use of various diameter filaments and weaving patterns can result in a plethora of different types of glass fabric.

2.2. Common Fabrication Technologies for High-Density Interconnect

2.2.1. Fabrication Processes for High-Density Interconnect

In 1980s, researchers aimed to reduce the size of vias in printed circuits, which led to the development of High-Density Interconnect printed circuits. Although the innovator's identity is unknown, early pioneers include Larry Burgess (creator of the LaserVia), Dr. Charles Bauer (inventor of photodielectric vias) [4], and Dr. Walter Schmidt [5] (development of plasma-etched vias). In the late 1970s, laser drilled vias were initially employed in multilayer mainframe computer systems. These vias were not as small as today's laser-drilled vias, and they were only available in FR-4, a difficult-to-manufacture material. The first production build-up or sequentially printed boards were released in 1984 with Hewlett-laser-drilled Packard's FINSTRATE computer boards, IBM-SLC

YASU's [2], and Dyconex's DYCOstrate.

Laser drilled microvias were never planned for Finstrate board bt HP. They were developed by reverse engineering their 32-bit microcomputer CPU. High yield and lower cost attracted great attention towards laser processing of microvias and laser via technology is adopted in the industry, yet for prototyping purposes, mechanical vias are still viable down to 100 um in diameter.

Fabrication process developed within this thesis is given schematically in Figure 5. Yellow boxes refer to a process that requires cleanroom conditions, dashed outline refers to shaping and forming processes having HDI sized (features smaller than 150 µm) features, and grey boxes are performed at regular laboratory conditions. Process flow starts with the preparation of the core layer coded as 1.0, followed by patterning of the active core coded as 1.1. Prepreg-Cu layer pairs are laminated to both sides of the core structure at each lamination step and each new layer increments the first digit by one. Each step explained in the schematic fabrication process flow described in Figure 5 has a corresponding cross-sectional representation with step-specific modification plotted in Figure 6.

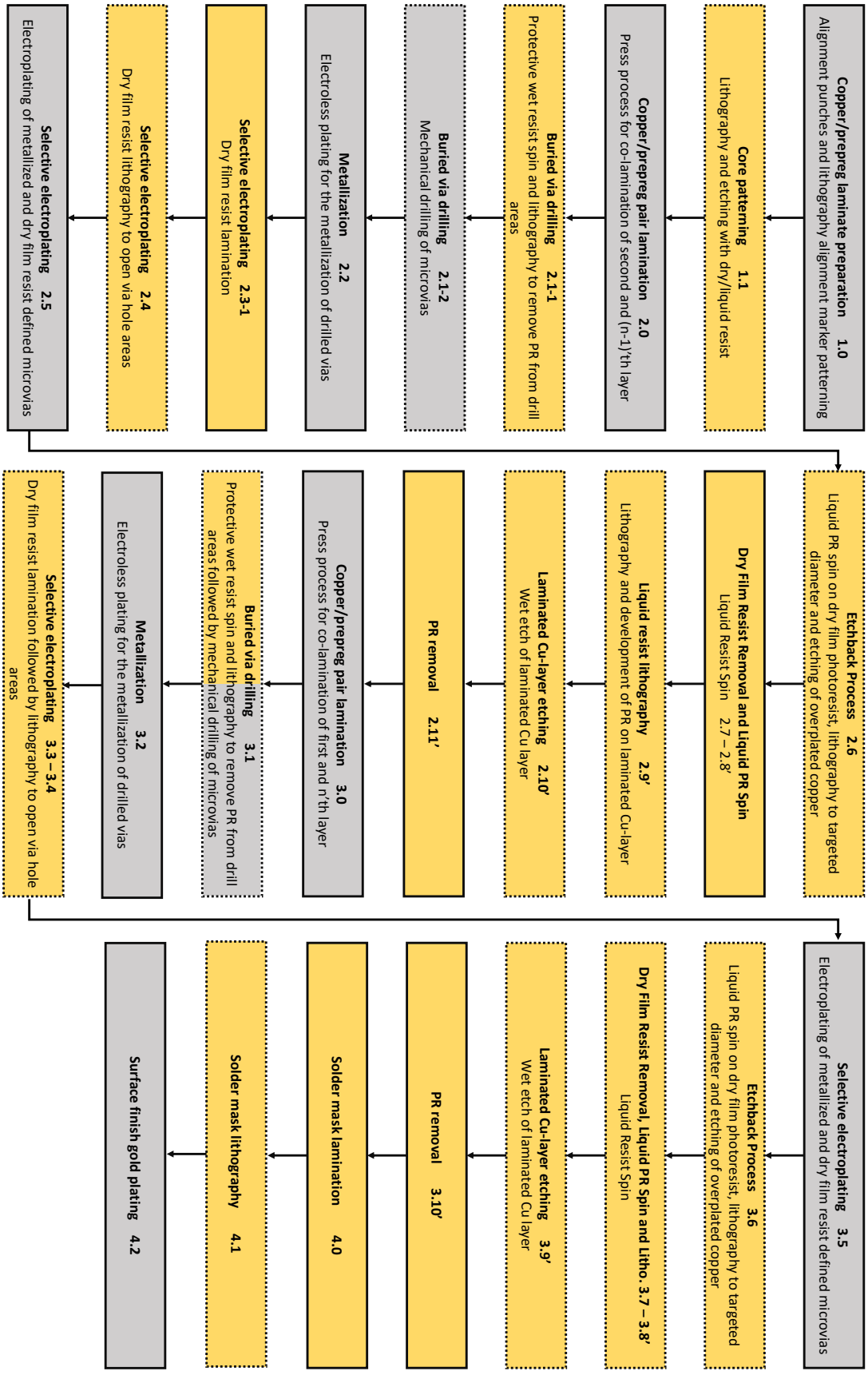


Figure 5 Schematic representation of developed fabrication process for 2-N-2 structre within this thesis.

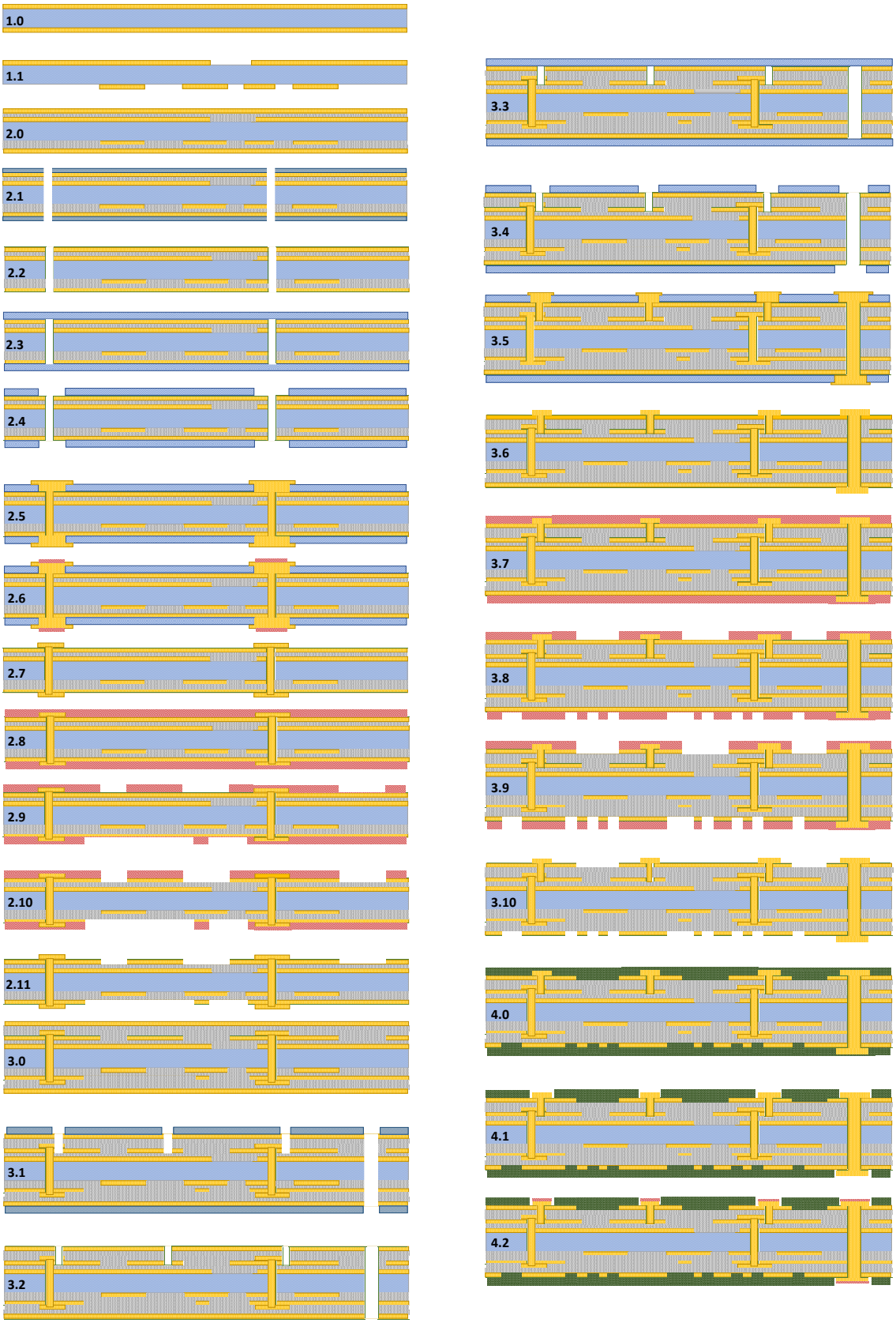


Figure 6 Cross-sectional schematic representation of fabrication process for 2-N-2 stack-up within this thesis.

2.2.2. Metallization Processes and Procedures

Vertical electrical interconnects are ubiquitous in HDI structures and may be the most important element of the functional stackup. The vertical interconnect elements used in HDI processes can be metallized in one of five different ways are given below. The following procedures apply:

1. Electroless and electroplating copper in the conventional sense (Figure 7.a)
2. Conventional conductive graphite or other polymers, as opposed to graphite oxide (Figure 7.b)
3. Electroless Copper, both fully additive and semi-additive scheme (Figure 7.c)
4. Conductive Pastes or Inks (Figure 7.d)
5. Fabrication of Solid Metal Vias

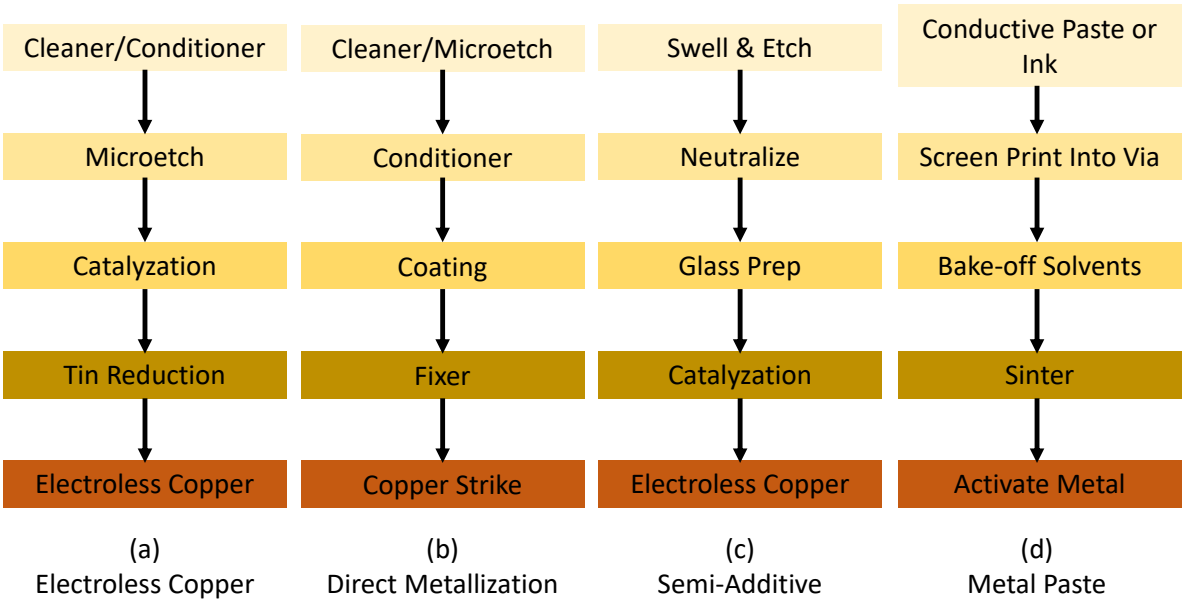


Figure 7 Four common processes for the metallization of vias.

2.2.3. Mechanical Drilling Via Technology

Mechanical drilling was previously the most often employed method of via production on a global scale. However, as a growing number of designs require microvias with a diameter of less than 0.20 mm, novel solutions have evolved. This trend has been accelerated by the growing popularity and use of blind and buried vias. When using a

mechanical drill, the vertical walls are parallel to one another, which is referred to as anisotropic drilling. There are numerous non-mechanical drilling processes that are isotropic, meaning their walls recede laterally in lockstep with their depth, or have sloping walls, meaning the entry opening is larger than the exit opening. While a larger entry opening facilitates less troublesome metallization, the isotropic retreating wall can complicate metallization and plate-up.

Mechanical vias can either be opened with depth control or directly, which would require different fabrication routes in terms of metallization and lamination. In Figure 8, depth-controlled drilling of blind vias (left) and sequential lamination-based blind via fabrication process is described (right).

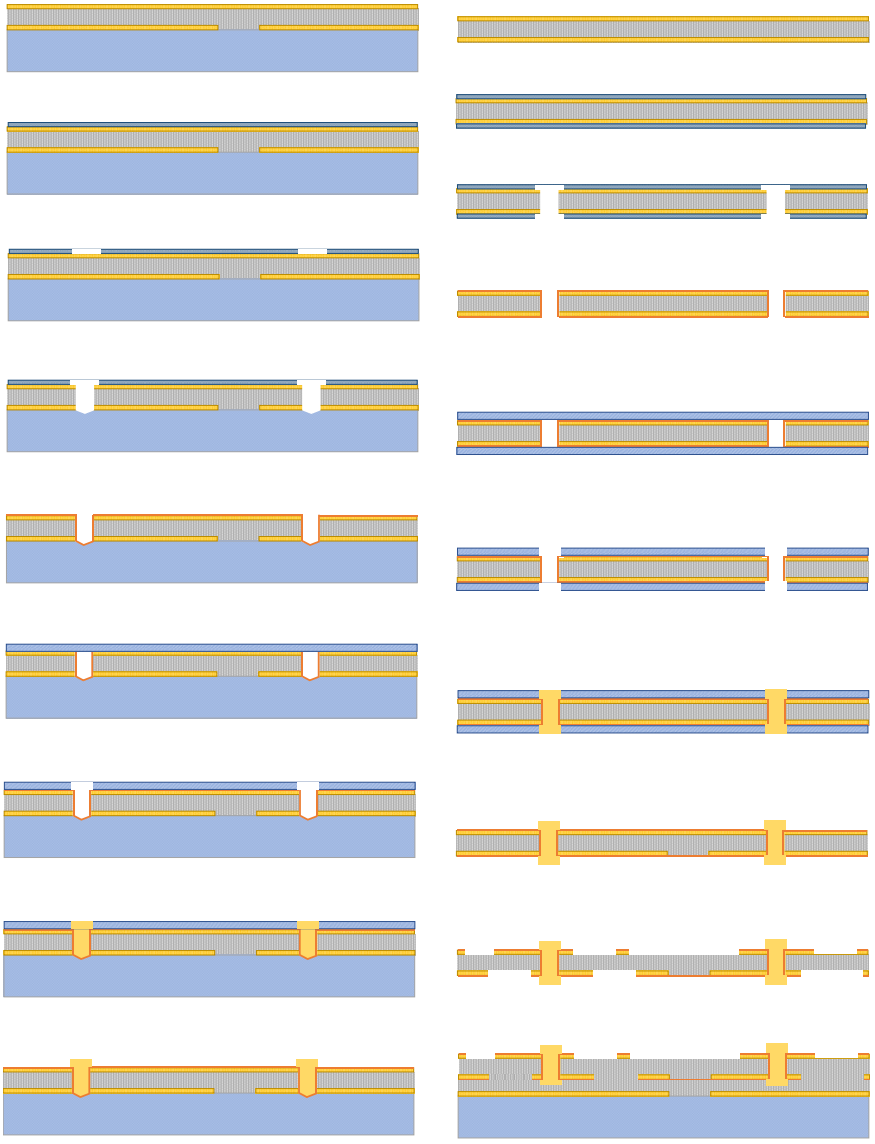


Figure 8 Mechanical drilling of blind vias: (a) controlled depth drilling, and (b) sequential lamination.

2.2.4. Desmear and Metallization

To ensure the reliability of plated through-holes and blind vias, detailed hole preconditioning and metallization are required. The desmear process is used to clean interconnects and via pads of residual via formation residues to prove a tightly adherent contact between the succeeding metallized coating and the interconnects and via pads. Residues are produced by the heat generated during drilling and by items left on the via pads following mechanical drilling. Additionally, it is meant to create topographical modification or micro-roughening in the resin by the desmear process, which can be performed using alkaline permanganate, plasma, or a combination of the two.

Numerous investigations undertaken by experts in the field of PTV/BV dependability have established that long-term reliability is strongly influenced by the quality and consistency of the copper deposit contained within the through-hole and blind vias. Most of the consumers and PCB designers are unaware that the metallization process performed prior to copper electrodeposition application is critical for establishing a homogeneous copper layer in blind vias and through-holes. The methods utilised to establish conduction through these vertical interconnect elements determine whether or not the electroplated copper is continuous and adheres to the resin and any supporting structures, such as glass or other fibre material. There are multiple methods available for making vias conductive, including the following:

1. Electroless Copper
2. Palladium-based Direct Metallization
3. Graphite
4. Carbon Black
5. Conductive Polymer

These metallization techniques have been extensively explored in recent years for both plated through-hole and blind via metallization applications. Electroless copper specifics and procedure will be discussed in greater detail later in this chapter since the utilized metallization process is electroless copper plating in this thesis work. It is vital to begin with the desmear procedure, as it is critical to the metallization process' overall performance and must be done first.

2.2.4.1. The Alkaline Permanganate Process

In comparison to the dry plasma method, the alkaline permanganate method is a multi-step procedure that is meant to remove smear and microroughen the resin. Desmearing the inner layer enables the electroless copper and acid copper to adhere well to it, as the smear is removed during the process. Additionally, this method is used to ensure that the resin surface is sufficiently prepared for the catalyst and electroless copper to adhere to the resin. Four stages comprise the desmear procedure:

1. Sweller
2. Permanganate
3. Neutralizer
4. Etch on glass (Optional)

Solvent/Sweller/Hole Cleaner

The solvent's function is to expand the resin, making it more susceptible to attack by the permanganate solution that follows. The dwell time, concentration, and temperature are all critical aspects. If the dwell time in the solvent is short, the permanganate will remove just a small amount. When the dwell period in the solvent is prolonged, the solvent may penetrate further than necessary and persist in the resin during permanganate processing.

Permanganate

By oxidising the resin bonds, permanganate is utilised to remove resin from the body. It is made of permanganate and hydroxide components. The duration of the permanganate and hydroxide solutions, their concentrations, the temperature, and the amount of residue remaining in the solution are all critical factors to consider. Resin may not be completely removed if the dwell time in the permanganate is too short. If the stay time in the permanganate solution is extended, a significant amount of resin is lost, resulting in an uneven profile on the hole wall. Additionally, an excessive dwell time may result in reduced topography along the hole wall, as a result of resin being removed beyond that swollen by the solvent stage.

Neutralizer

The neutralizer's purpose is to remove any permanganate residue that may have remained on the panel following cleaning. The duration of the dwell, the sulfuric acid concentration, and temperature of the neutralizer are all critical factors to consider. Allowing permanganate to remain on the panel will obstruct proper catalyst adsorption, resulting in electroless copper gaps in the resin, hole wall pullaway, and general contamination of the via pads and interconnects, among other issues. Separation of plating is more possible if permanganate is left on the copper inner-layer or via pad following plating.

2.2.4.2. Electroless plating

To deposit copper coating on the board surface and along the via wall, an electroless copper plating process is utilized. Its purpose is to carry electricity through the hole, allowing for more copper accumulation in acid copper plating to occur. A total of four key pretreatment processes are required before the electrolytic copper process can begin:

1. **Cleaning and Conditioning**

The cleaner/conditioner is designed to remove debris from both the surface and from crevices in the via hole surface. Additionally, it conditions the glass and resin to ensure that the catalyst adheres effectively to their surfaces. The duration of time spent in a solution, its concentration, and temperature are all significant factors to consider.

2. **Microetching**

The microetch process micro-roughens the copper surface to improve the bonding between the electroless and laminate copper layers. Consideration factors are the copper content, sulfuric acid concentration, oxidizer concentration, dwell period, and temperature for microetching. A shallow etching depth can result in poor electroless adhesion. A high etch rate might result in a reduction in copper thickness and a negative etchback.

3. Catalization

The catalyst is designed to deposit palladium on the surface of the via hole. Following that, the palladium will operate as an activation point for the electroless copper deposition process. This is preceded by a pre-dip that acts as a sacrificial bath prior to the addition of the catalyst. The pre-dip process removes oxides from the catalyst, hence reducing copper contamination. Additionally, it aids in the adsorption of common ions into the catalyst. Acid normality, chloride normality, stannous chloride concentration, catalyst concentration, dwell duration, and temperature all play a role in the performance of the catalyst. Void development, insufficient adhesion, and hole wall pullaway are all possible outcomes of insufficient catalysis.

4. Electroless Copper Bath

The basic formulation of electroless copper baths is composed of five major components:

- The presence of copper ions, usually in the form of copper sulphate or copper chloride.
- A reducing agent, usually formaldehyde.
- pH adjusters (commonly sodium hydroxide) - used to maintain a pH between 11 and 13.
- Chelating agents, which are substances that help to keep the copper ion in solution.
- Chemicals that are proprietary to the manufacturer, such as stabilisers, wetting agents, ductility enhancers, and grain refiners.

Using the electroless copper bath, copper coating is applied to the board surface as well as along the via wall. It conducts electricity through the via holes, allowing for increased accumulation of electrolytic copper plating. The concentration of bath components, the bath temperature, the micro-roughening of the resin, and the amount of palladium adsorption all have an impact on the plating rate of the electroless copper bath.

2.2.4.3. Metallization with Electroless Copper for Microvias and High Aspect Ratio Through-Holes

Securing metallization for blind vias or smaller holes with diameters of 4 mils or less, and

through-hole aspect ratios (AR) of 10:1 or greater, is a difficult task. The ability to maintain appropriate process solution flow in the through-holes, sufficient palladium adsorption on the resin and glass, and the ability to minimise and remove hydrogen gas bubbles that occur as a by-product of the electroless copper deposition are all critical success criteria. Gas bubbles created as a result of hydrogen gas formation are frequently blamed for small hole voiding, particularly in vias with a high aspect ratio and blind vias that are very small. The electroless deposition reaction shown below demonstrates that the creation of H2 gas can sometimes become caught in the via, preventing copper from being deposited:

$$Cu^{2+} + 2HCHO + 4OH \longrightarrow Cu^{+} + 2HCOO^{-} + 2H_2$$

It is possible to effectively fill a high AR via by the use of an adequate volume of hydrogen gas during this reaction. The result can be voided, thin and/or irregular plating. The equipment set-up, when the electroless plating process is performed in the horizontal mode, must be agitated properly in order to displace gas bubbles from the via during the plating process. Plated sample should be agitated both vertically and horizontally continuously and the sample has to be flipped in regular intervals since reaction simultaneously occurs on the other side of the board. For high aspect ratio vias, providing a mechanism of refilling chemical reactants into the via while displacing the material (reactants and by-products) that remains is a difficulty. It is vital to expel the gas bubble before it has a chance to develop a void. Schematic representation of electroless plating is given in Figure 9.

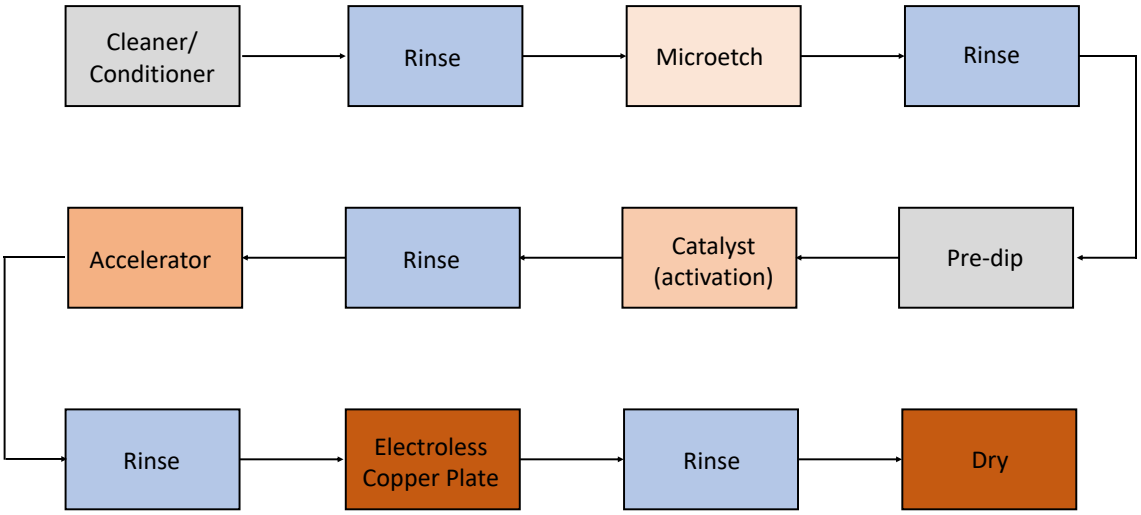


Figure 9 Schematic representation of electroless plating.

2.2.5. Direct Current Plating Theory

Direct Current (DC) plating is by far the most common and oldest method of electroplating, having existed for hundreds of years. Copper baths containing sulfuric acid are frequently utilised in the fabrication of printed circuit boards, and the configuration of the plating setup in the simplest form is given in Figure 10. To impact the formation of grain structure, grain refiners, wetting agents, and brighteners are added to the basic electrolyte mixture of water, copper sulphate, and sulfuric acid. Electric field is used to redirect copper ions away from the solution during electroplating. To maintain a steady level of copper ion concentration, a solution of copper metal is dissolved in the electrolyte. When an electric current is delivered to a surface, the following reactions take place at the copper anode and sample cathode respectively:

$$Cu_{(s)} \rightarrow Cu^{+2}{}_{(aq)} + 2\ e^-$$

$$Cu^{+2}{}_{(aq)} + 2\ e^- \rightarrow Cu_{(s)}$$

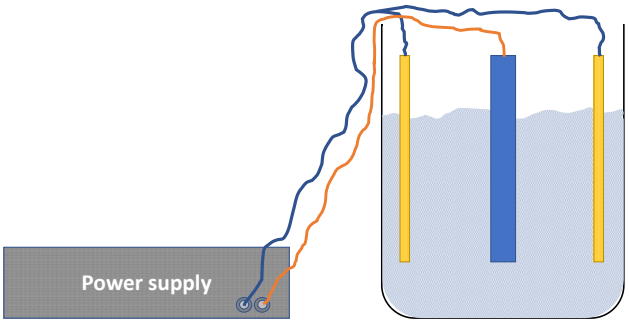


Figure 10 Schematic representation of direct current plating setup

2.3. Fine Line Imaging and Etching

This chapter is primarily concerned with image transfer processes, such as resist lamination, resist spinning, resist stripping, and etching fine lines, equipment, and materials for fine-line image transfer.

2.3.1. The Process of Image Transfer

HDI imaging requires significantly more severe controls than standard print and etch applications. To obtain finer lines and gaps, smaller via pads on vias, and plated through-holes, increased vigilance in terms of phototool quality, imaging parameters, and surface preparation is necessary.

2.3.2. The Typical Image Transfer Procedure

At the moment, contact printing is the most often used technique for photolithography of PWBs. Radiation in non-exposure zones is one of the most critical issues that can develop in contact printing, particularly with fine-line boards. The other is a representation of the board's dirt, defects, or other unexpected characteristics. While projection imaging and laser direct imaging have the potential to address some of these concerns, they are not yet widely used in cleanroom environments. This chapter contains a plethora of supplementary information on image transfer operating methods, equipment, and material selection for the full range of image transfer procedures.

2.3.3. Fine-line Adhesion Resist

Fine-line and, by default, extremely dense circuit characteristics necessitate an integrated imaging technique. In this regard, the experimenter exercises extreme caution to

guarantee that the resist adheres to the copper surface. While the next item discusses the resist lamination parameters and their relative importance for adhesion, it is also necessary to examine the surface preparation of the copper foil prior to the lamination process.

2.3.4. Lamination of Dry Film Photoresist

Thermal transfer from the rolls to the resist/copper interface is performed by passing heat through the polyester film coversheet and resist to ensure proper resist to copper conformation and adhesion. Thermally heated rolls can be manufactured in a variety of ways, including using cartridge heaters or putting surface heaters to the inside surface of a hollow roll. Other laminators use an infrared source attached to the laminator to heat the roll's exterior surface. When it comes to achieving the appropriate lamination of the resist, pressure is significantly more important than temperature; nonetheless, temperature is critical for reducing the resist's viscosity and therefore increasing flow. [6]

2.3.5. Spin Coating of Liquid Photoresist

According to standard procedure, a few millilitres of resist is placed (dispensed) on a substrate that has been rotated at a rate of several thousand revolutions per minute either prior to or shortly after. Centrifugal force causes the dispensed resist to spread uniformly to the desired film thickness, and any excess resist is spun away from the substrate's perimeter. Meanwhile, a small amount of solvent is emitted from the resist film, limiting its thinnability on the one hand and making it sufficiently stable to withstand the handling of the coated PCBs on the other.

2.3.6. Etching

The chemical and mechanical components of etching are given new meaning when HDI is used since the aspect ratio of etched lines and copper thickness is getting close to one in some designs. Because the etching chemical may result in severe undercutting as well

as the loss or lifting of the resist, the experimenter must ensure that the resist adheres strongly to the copper surface prior to etching. Numerous issues arise when etching, some of which are interconnected and others that are distinct. Process optimization may have beneficial impacts in one or more of the above-mentioned problematic areas.

2.3.6.1. Etch Undercut

First and foremost, while addressing etch undercut, it is important to remember that the wet etching of PWBs is isotropic. In other words, one can see both a lateral attack on the copper traces as well as an attack on the copper in the z-axis direction on the copper. Even when equipment and process modifications are made, the lateral undercut does not disappear completely.

3. DEVELOPMENT AND OPTIMIZATION OF PREPREG COPPER LAMINATION PROCESS

The lamination of 18 µm thick copper foils to the prepreg surface is achieved by a process based on hot pressing (Figure 11). For the lamination process, the optimum temperature and pressure values between 150-200˚C and 200-400 psi were determined experimentally. Desktop LPKF Multipress S press device, which was used for these processes and which can offer 9 different temperature, pressure and time profiles with microprocessor support, had been used. Mechanical roughening of the copper surface in the interlayers, chemical oxidation [7], [8] or surface modification with plasma processes [9] are involved in HDI PCB production processes to increase adhesion. Low roughness profile copper foils showed sufficient resistance to delamination on prepreg surface: delamination or surface defects did not occur on copper traces during the multistep fabrication process.

In a typical multi-layer press process setup, from top to bottom as shown in Figure 11: upper mold part, upper press cushion, upper press plate, copper foil, prepreg, core-core, prepreg, copper foil, lower press plate, lower press shroud, and lower die piece line up throughout the assembly.

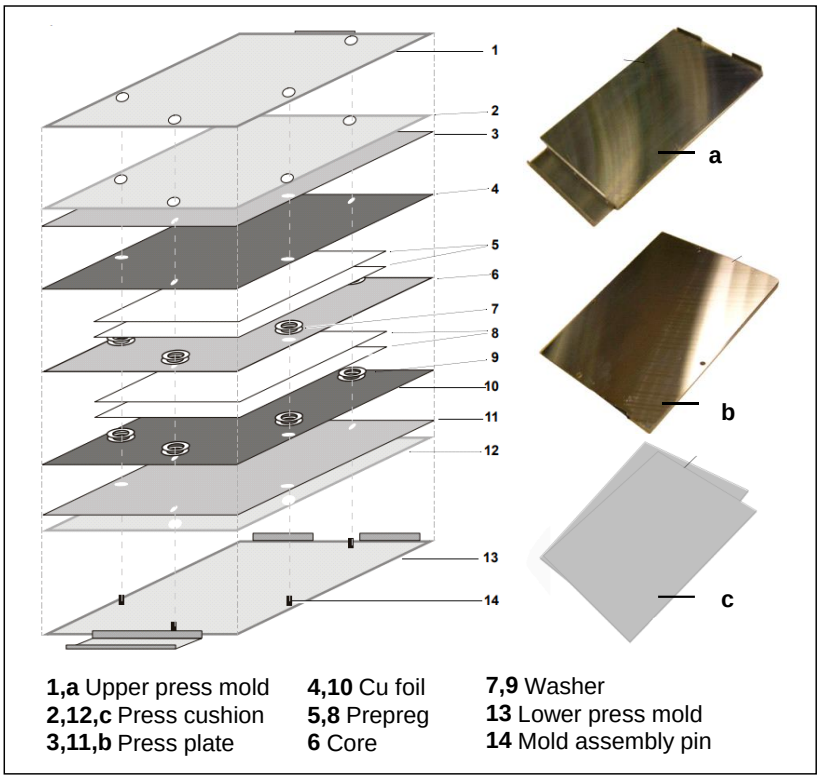


Figure 11 Typical multilayer press process setup.

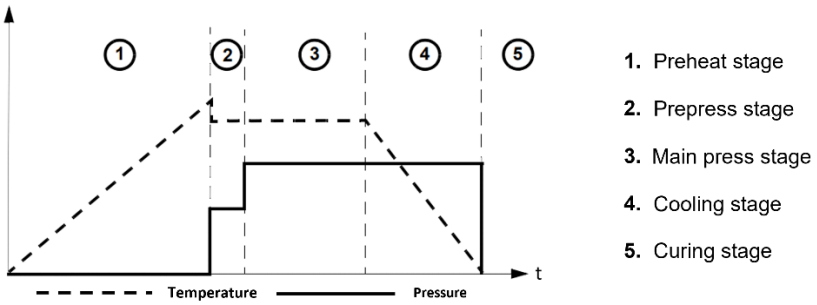


Figure 12 Press profile: Temperature and pressure over time.

The pressing process consists of five steps: preheating, prepressing, main pressing, cooling and curing. For each step, the optimal values for the pressure, temperature and time parameters is given in Table 1 for a 10 cm by 10 cm stackups to be processed and the press profile required for a successful lamination process is given in obtained (Figure 30).

Table 1 Press profile values for eavh of the five stages of lamination.

	Pre-heating stage	Pre-pressing stage	Main press stage	Cooling stage	Curing stage
Temperature	200 °C	200 °C to 180 °C	180 °C	180 °C to RT	RT
Pressure	-	80 N/cm^2	150 N/cm^2	150 N/cm^2	-
Duration	10 min	10 min	60 min	3 hours	12 hours

In the pre-heating phase, which constitutes the first step in the pressing process, heating is carried out to the temperature specified in the press profile without the installation of a multi-layer mold. When the preheating temperature reaches the optimal value, the multi-layer press assembly mounted on the press die is placed inside the pressing chamber. At this stage, increasing the temperature higher than the temperature to be applied during the main pressing stage compensates for the sudden temperature drop that occurs when the press die is placed in the chamber. Temperature of the press die at the beginning of the prepress stage is 185 °C.

The prepress stage is necessary to eliminate air gaps created during the press process. It is also necessary to eliminate temperature differences across the layers to increase interlayer adhesion. In the prepress stage, the temperature, time and pressure values are as 180°C, 10 minutes and 80 N/cm2 (116 psi), respectively.

The main pressing stage is the step in which the discrete layers are formed into a multi-layer structure. Pressure and temperature values are kept constant throughout the main pressing stage. The initial press values in the main pressing stage are 150 N/cm2 (217.5 psi) for 60 minutes at 180 °C.

During the cooling phase, the heating surfaces are turned off and the pressed sample is allowed slowly descend to ambient temperature. It is necessary to keep the pressure at the level of the main pressing stage during the cooling stage to prevent air penetration into the still soft prepregs.

After removing the multi-layered structure from the press mold, it is left at room temperature for at least twelve hours.

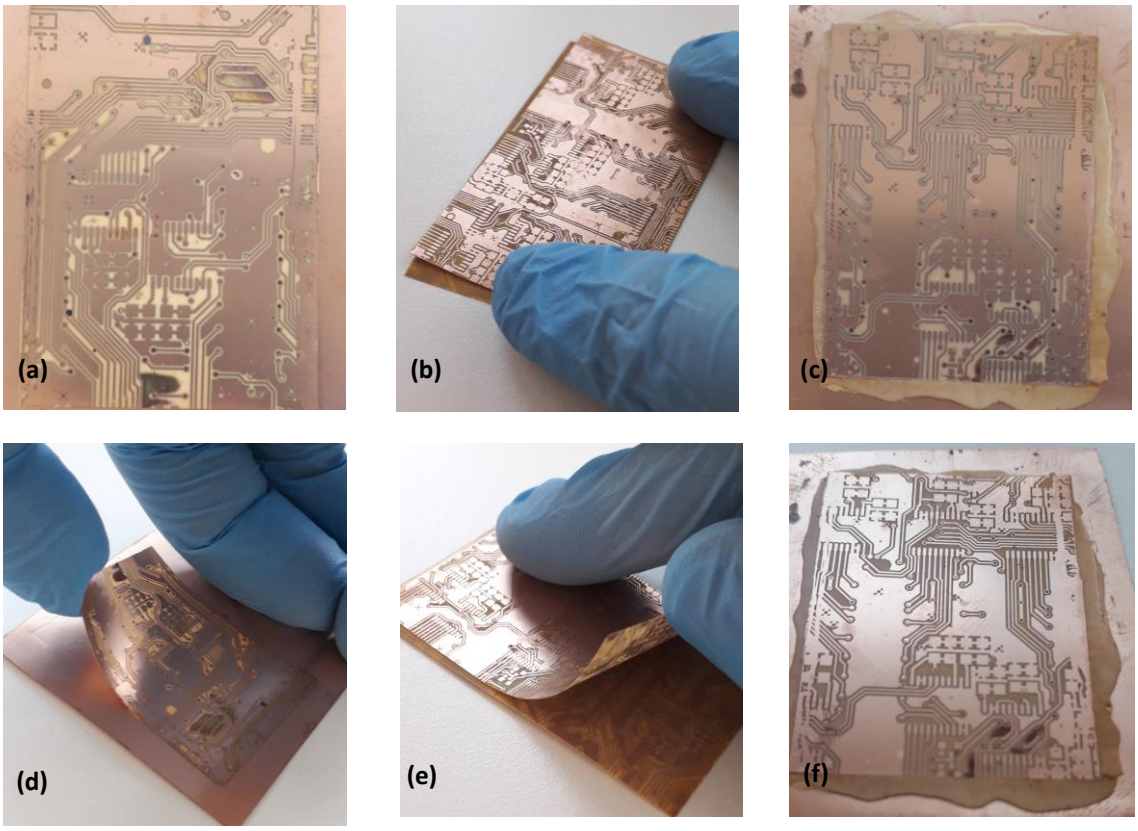


Figure 13 Preliminary press experiments carried out for bare cores and prepreg interleaved sample

Preliminary press experiments were carried out by following the press profile shown in Figure 12 and Table 1. In Figure 13, copper-insulator, insulator-insulator, and insulator-prepreg-copper printing experiments were carried out with Isola Astra MT77 samples without any adhesion promoting coating process. It was observed that the samples without prepreg insertion performed an unsuccessful interlayer bonding (Figure 13 a,b,d,e). It can be seen that some resin melted and flowed from the edges as expected from the sample that prepreg material pressed with cores (Figure 36 c,f), but unlike the pressing processes without prepreg insertion, it was observed that this sample provided successful lamination.

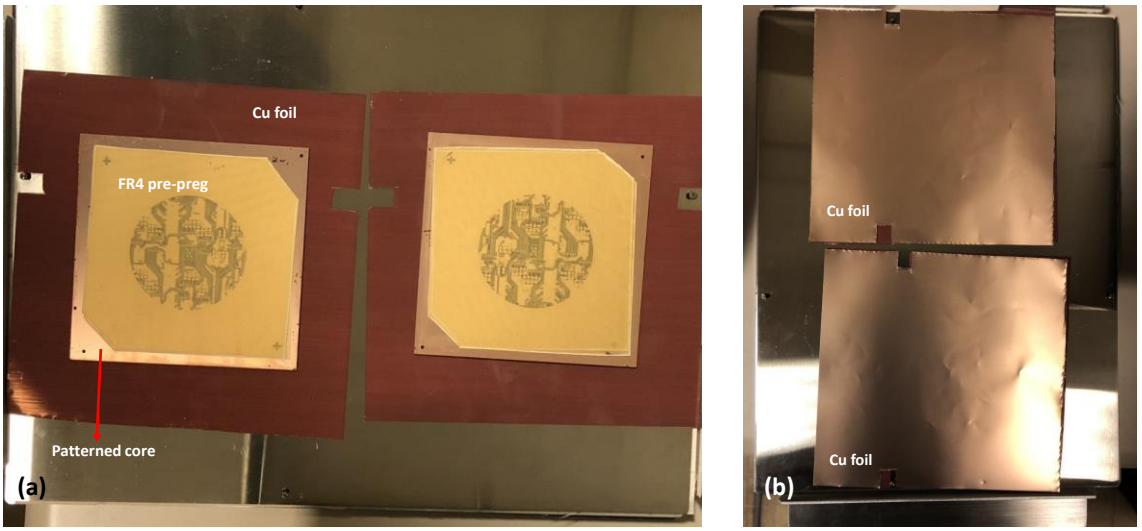


Figure 14 Lamination setup on press plates for layer 1 and layer n: Cu foul of layer n, prepreg, patterened core, prepreg from bottom to top (left) and full stack-up before lamination is shown (right).

In Figure 14, 1 and n'th prepreg layer lamination setup is given. Figure 14 (a) shows copper foil, prepreg, patterned core, and prepreg layer on press plate from bottom to top respectively. It can be seen that prepregs are cut on diagonal edge to prevent prepreg flow to alignment fiducials. The First Cu-prepreg layer's copper foil is placed on prepregs for lamination. Excess copper from sides (2 cm) provides extra space for prepreg to flow on during lamination before causing contamination on press plates, where this excess copper foil is trimmed after lamination.

An important parameter for the press process is thickness uniformity after lamination. Thickness variation throughout the stackup causes uneven photoresist (PR) thickness profile leading to discontinuities in developed resist traces. Photoresist profile that shows thickness and width variation causes uneven etch profile throughout the board. It is found out that pressing 10 cm by 10 cm stackups and restricting the circuit pattern containing area to 7.5 cm by 7.5 cm is suitable to achieve successive processes following lamination.

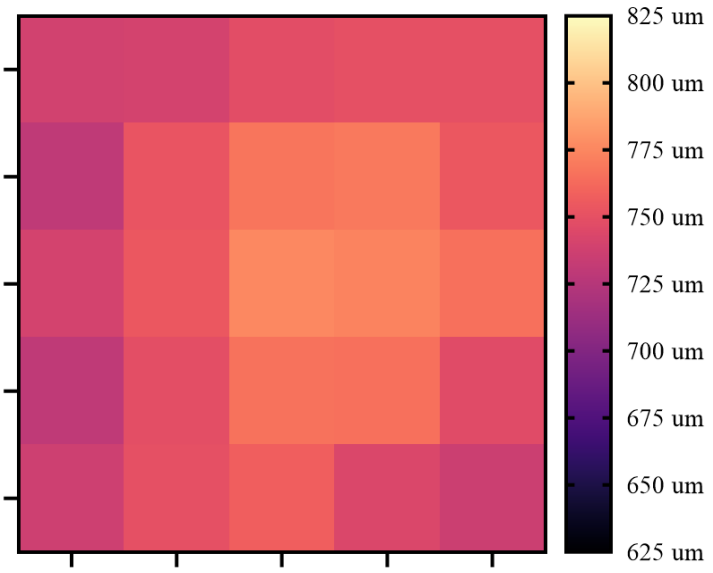


Figure 15 Stack-up thickness measurements after lamination.

The graphical representation of the PCB stack thickness measurement is given in Figure 15, the smallest and largest value for the color scale was determined around 10 percent of the average thickness. Before the stack patterning process, a measurement was made from 16 points with a 1 micrometer precision measuring device. The average thickness was calculated as 750 µm, the smallest measured thickness was 729 µm and the largest measured thickness was 775 µm. The maximum height difference across the stack is 5.93%.

4. DEVELOPMENT AND OPTIMIZATION OF MECHANICAL VIA FORMATION PROCESS

Laser processing techniques have gained importance in recent years as an alternative to mechanical drilling in the creation of vias. It is possible to obtain smaller sizes in laser vias, also called microvias. In addition to the size criterion, laser vias may be preferred in cases where the number of vias, processing time, and cost are important. Due to the heat generated during the drilling process in the via fabrication process, a thin resin layer and carbon layer may form on the via wall facing inside the via, and organic residues may remain. This prevents the metallization of the vias by electroplating. Similarly, copper bumps may form around the vias after drilling. For this reason, cleaning processes called "desmear" and "deburr" are generally integrated into HDI fabrication processes [10, 11].

Chemical etching technique is a well-known desmear and pretreatment method to modify the surface topography of the drilled hole wall in HDI PCB fabrication. It consists of three stages: sweller, oxidizer, and neutralizer. In this process, sweller occupies the free volume of the epoxy polymer network and weakens the intermolecular and intramolecular bonding forces. During oxidation, erosion of the swollen polymer takes place, creating micro-voids up to a few micrometers. The copper filled into these micro-voids increases the fixation to the inner surface of the porous dielectric material. This process provides a more consistent dielectric surface texture for consistent coating throughout the through via [12]. Various chemical treatment methods have been reported to remove debris, as well as to support the metal coating and to modify the surface topography of the drilled glass-epoxy laminate. High concentration sulfuric acid (96-98%) and chromic acid have been used for many years in HDI PCB applications to create micro-roughness and remove contamination inside the vias [13].

In recent years, it has been observed that the "desmear" process is performed with processes based on plasma techniques, especially in sensitive multi-layer PCBs used in military applications [14]. Therefore, processes based on plasma (oxygen-nitrogen) technique can be utilized to ensure the cleaning and surface activation of the drilled vias. Manually mechanical sanding and chemical mechanical planarization techniques are applicable when necessity for the deburr process occurs.

High-quality cleaning of the vias is very important to increase the bondability of the copper to be deposited by electroplating of the micro vias to the dielectric wall of the holes [15]. Desmear treatment with plasma is considered an effective cleaning method for high performance HDI structures with its easy control and low contamination. Plasma desmear uses plasma with high activity that reacts with macromolecule materials and glass fiber. The gaseous waste products and unreacted ions arising from the reactions are discharged with an air pump to form the cleaned wall of the holes. The initial plasma process parameters predicted for O_2-CF_4-based plasma chemistry to be used for cleaning microvias with a diameter of 100 micrometers are given in Table 2 [16]. Figure 16 shows scanning electron microscope (SEM) images of two micro vias (a) after drilling and (b) after plasma desmear treatment. However, dimensions exceeding 4-inch critical dimension for processing in cleanroom environment is challenging. Also reported RF power and gas volumes are not achievable within the cleanroom and laboratory infrastructure within this work. Unlike the chemical desmear process, only single sided processes can be performed on the stackup, leading to excessive process durations. With the listed reasons above, wet chemical desmear processing is applied for the 2-N-2 stack-up fabrication in this thesis work.

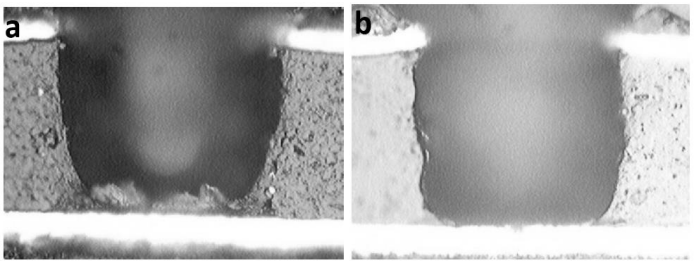


Figure 16 Scanning electron microscope (SEM) images of two micro vias (a) after drilling and (b) after plasma desmear treatment

Table 2 Plasma desmear proses parameters for RF power, O_2 flow, CF_4 flow, duration and pressure.

RF(W)	V O_2 (ml/dakika)	V CF_4 (ml/dakika)	t (min.)	Pressure (mtorr)
2700	700	300	10	40

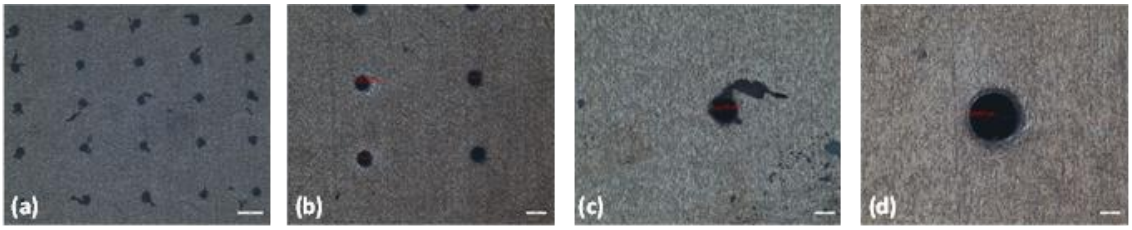


Figure 17 100 µm via drilling process: (a) Exit surface microscope image for 500 µm thick core samples with 100 µm drill bit, (b) Entry surface microscope image for 500 µm thick core samples with 100 µm drill bit, (c) Copper chips left on the exit surface, measured via exit side diameter is 113 µm, (d) via entry surface, measured diameter of entry side is 124 µm.

During the development of mechanical via hole formation process, mechanical vias with a diameter of 100 µm were opened. Figure 17 shows vias drilled through a core layer (500 µm). 124 µm through-hole diameter on the inlet surface and 114 µm through-hole diameter on the exit surface of the via profile obtained with a 100 µm drill bit were measured. During the experiments carried out throughout the optimization period, the successful drilling limit of the Protomat S104 drilling device with a 100 µm drill bit was investigated. While no success was observed on 2 mm thick stack-ups with 100 µm drill bit, successful through-holes were opened in the stackups with maximum height of 750 µm.

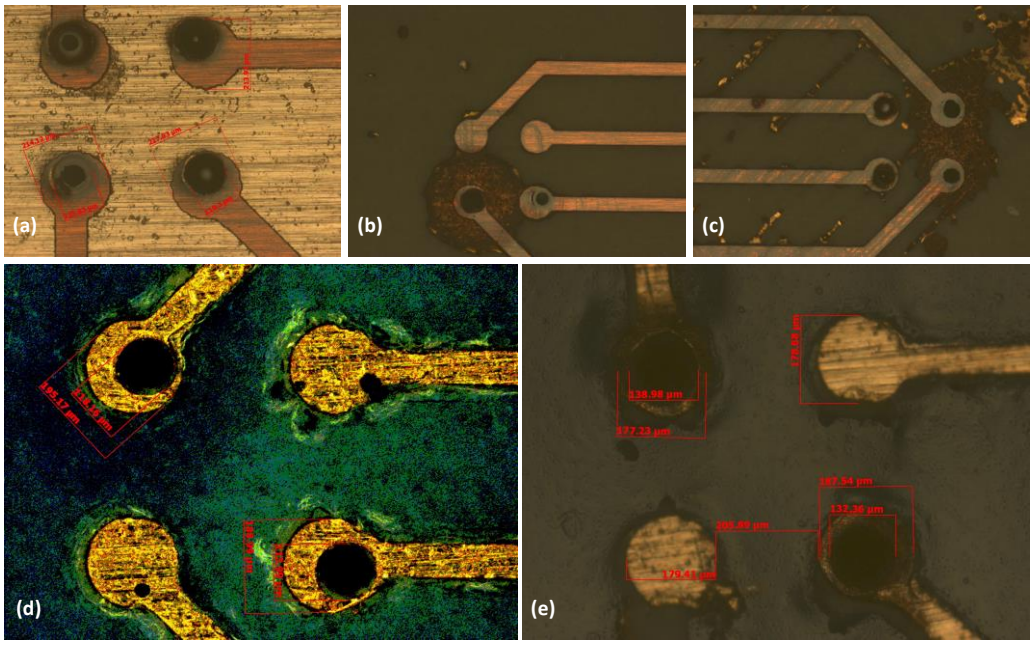


Figure 18 Mechanical vias opened through via pads: (a) Via drilled on patterned PR on Cu foil, (b,c,d,e) Via drilled on patterened Cu foil.

Prior to the opening of the vias, which is the first step after lamination of the layers, the sample surface is coated with PL177 photoresist so that the copper is not scratched: secured from the mechanical deformation that drilling head employs that these deformations lead to discontinuities in the via region. Figure 19 shows the surface discontinuities caused by mechanical deformation on the copper surface left as copper residues after etching. The reason for this surface irregularity is that the Protomat S104 head scrapes/erodes the copper surface while the alignment markers are being patterned on the copper surface as shown in Figure 19a.

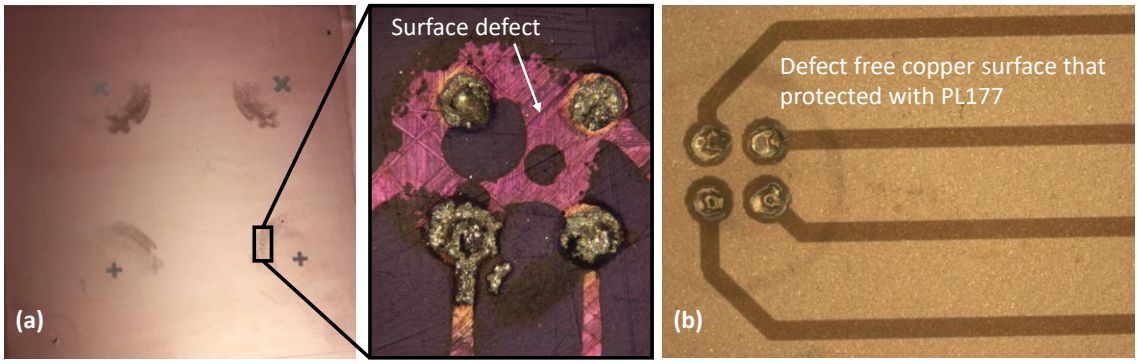


Figure 19 Surface defects due to mechanical drilling: (a)alignment marks and surface defects occurred on Cu foil during alingment marker creation, (b) elimination of surface defects with protective PR application prior to drilling

PL177 protective photoresist is patterned by lithography by the size of the via hole diameter (100 µm) on the via places prior to drilling so that the polymeric material would not be peeled off by the drill bit and adhered to the surface of the hole. If any drag in contaminants reaches the metallization baths, an autocatalytic reaction occurs, which consumes bath lifetime much sooner than the predicted use period for the baths.

The surface irregularity is eliminated by applying an additional photoresist coating and lithography step to the process flow and the via region can be drilled and metallized properly as in Figure 19b.

5. DEVELOPMENT AND OPTIMIZATION OF THROUGH HOLE METALLIZATION PROCESS

Staggered and stacked vias are the two main types of vias encountered in HDI PCBs. In order to provide electrical connection between PCB layers, the formed vias generally need to be filled with copper (Cu). In the copper filling process, a thin copper film based on electroless (autocatalytic) plating is formed on the drilled vias. Following electroless plating, the vias are patterned with photolithograpy of dry film photoresist to ensure that electroplated copper will be selectively deposited that only the vias are filled with copper (Cu) and the initial copper foil thickness and surface profile do not subject to change. Appropriate electroplating processes development for void-free filling of vias require optimization on experimental conditions such as current density, plating time, and solution chemistry (copper sulfate: sulfuric acid: chloride: additives).

Copper plating process development experimented on untreated copper-clad PCB surfaces, and the final experimental conditions are determined by testing the initial conditions on multilayer PCBs containing via structures. As an alternative to Cu-electroplating of vias, within the scope of this thesis, the application of copper and silver conductive inks with appropriate viscosity by dispensing or screenprinting techniques are applied.

Copper via plating baths typically have high concentrations of copper (up to 250 g/L copper sulfate—$CuSO_4$) and lower acid concentrations (about 50 g/L sulfuric acid—H_2SO_4) to promote rapid filling. In addition, organic additives in electroplating baths are used to control the coating rate and to obtain acceptable topological properties. These additives and their concentrations are investigated to meet the technical requirements of

the HDI, such as the size of the vias that need to be filled, their yield, the surface copper thickness, the tolerance of the copper distribution across the panel, and the shape of the conductor line after coating. In addition to copper sulphate and sulphuric acid, additives such as carriers (plating carriers—25-100 ml/l), brighteners (brightener—2-10 ml/l), straighteners (leveler—5-15 ml/l), and wetter (wetter—5-8 ml) are also included [17]. Theoretically, as an electroplating bath additive, it is possible to fill vias only with the aid of carrier and brightener. However, for smaller vias with high aspect ratio conformal filling and analysis difficulties are problems of two-component systems.

Both carrier and leveler act as "suppressor" (inhibitors) but can be classified in different ways and into different types of suppressors. Type I suppressors such as carriers can be disabled by the brightener, while type II suppressors cannot be disabled. Carriers are typically high molecular weight polyoxyalkyl compounds [18]. They are typically adsorbed on the surface of the cathode and interact with chloride ions to form a thin layer. As a result, by increasing the effective thickness of the carrier diffusion layer, it reduces the coverage rate [19], the energy level on the cathode surface topography is equalized (allowing the same number of electrons for coating at any cathode surface point), so that the resulting copper deposit is more homogeneous and evenly distributed.

On the other hand, brighteners increase the coating rate by reducing suppression. They are typically low molecular weight sulfur-containing compounds, also called grain refiners.

Straighteners are generally composed of nitrogen-containing polymers, and they selectively adsorb to high current density areas such as local protrusions, preventing overcoating of copper in high current density areas [20].

Table 3 Ideal electroplating bath composition for void-free via filling.

Wetter	Brightener	Supressor	Cupper Sulphate	Suphiric Acid	Chloride Ion
7 mL/L	1 mL/L	4 mL/L	200 g/L	50 g/L	50 ppm

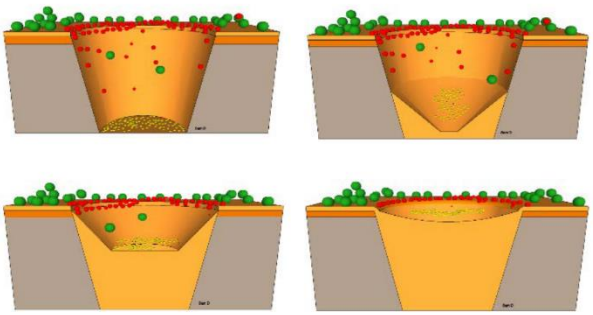


Figure 20 Functioning mechanism of suppressor, straightener and brightener, green, red and yellow, respectively.

The ratios given for the plating bath content in Table 3 are an example experimental recipe that will enable the vias to be electroplated with high efficiency without gaps [21]. Suppresser, straightener, and brightener additives are shown in Figure 20 in green, red and yellow, respectively. Wetting molecules are mainly adsorbed on the coating surface during the active coating process, while the straightener is selectively adsorbed on negatively charged sites due to its positive charge. Thus, excess coating on the edges of the via opening is prevented; gaps in the middle of the via and void formation are prevented by closing prematurely. Since the brightener is a small molecule containing sulfur, it spreads faster and accelerates the coating. During the coating process, the geometry of the conductor line constantly changes, the brightener condenses in the path, causing a rapid coating in the path. This is called the curvature enhanced accelerator coverage (CEAC) [22]. Finally, when the conductor is aligned with the surface of the line and the coating ratios on the line and the surface are equal, the via is filled without gaps. In Table 4, cross-sectional images of the samples taken from the coating bath at ten-minute intervals are given [23].

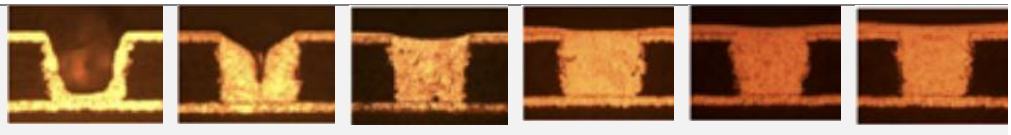
	10 min	20 min	30 min	40 min	50 min	60 min
Ø 100µm						

Table 4 Cross-sectional images of the samples taken from the coating bath at ten-minute intervals are given.

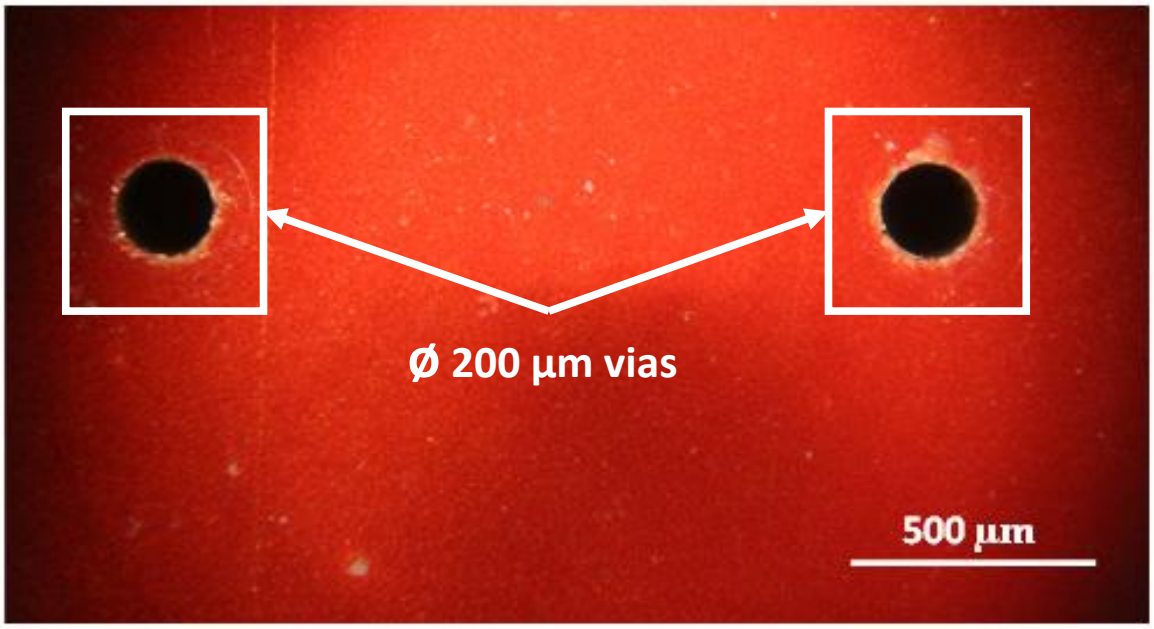


Figure 21 200 µm throughholes drilled on PR coated prepreg/Cu laminate.

For the electroplating of the vias, the copper thin film is coated conformally into the vias with the electroless coating technique, which allows metallization to the polymer surface and provides electrical connection between surface copper and via hole. In the electroless coating process, the PC Electroless Copper Kit (Solutions A, B, C, and D) electroless coating solution kit supplied from Transene company is used. Following this, with the electroplating process described above, the vias of different geometries and requirements specified in the process flow is filled. 200 µm vias to be used in electroless copper optimization experiments drilled on PR coated prepreg/Cu laminate can be seen in Figure 21. Before the electroless coating process, the sample to be coated undergoes the following cleaning and surface modification process.

1. Persulfate Etching (2 minutes)

   Produces a dull pink copper surface. Ammonium persulfate and sulphuric acid concentrations are 200 g/L and 10 ml/L respectively. Treatment is followed by rinsing the sample with water.
2. 10% Sulfuric Soak (2 minutes)

   Sulphuric acid soak removes insoluble salts. Treatment is followed by rinsing the sample with water.
3. 33% HCL Immersion (2 minutes)

   HCl immersion eliminates harmful drag-in to electroless plating baths.

The electroless plating bath starts directly after immersion in HCl, the last step of the cleaning process. Electroless coating process comprises three baths prescribed by the PC Electroless Copper Kit (Solutions A, B, C, and D) consisting of four solutions acquired from Transene Company. Cleaned copper coated epoxy/glass laminates immersed in Solution C for two minutes. The samples are kept in the solution without mixing or shaking. After the samples are rinsed with water, they are transferred to the next solution. Samples are kept in Solution D for two minutes without agitation or mixing. After two minutes, the samples will be thoroughly rinsed in distilled water. The electroless coating bath is optimised for use in the range of 30-45°C but solution is kept at the optimum operating temperature of 40°C during the copper deposition bath for uniform coating thickness. Higher temperature speeds up the deposition rate to much that results in excess H_2 accumulation inside the via hole. If H_2 bubbles inside the via holes cannot be removed effectively, then electroless copper solution cannot replace these H_2 bubbles, resulting in gaps and voids in via hole plating. During the coating process, the samples are midly agitated. The electroless plating bath is suitable to be used to deposit copper layers as thin as 0.5 µm. Electroless coating steps followed in this thesis work are listed below.

i. Sensitizing Solution C (2 min immersion) - Seeds the epoxy/glass laminate. Then it will be rinsed with water.
ii. Activator Solution D (2 min immersion) - Activates the autocatalytic layer required for copper deposition. After this step, the sample will be thoroughly rinsed.
iii. 5% Sulfuric Acid Immersion (4 minutes immersion) – Accelerates electroless copper deposition, protects against drag-in contamination, then rinses with water.
iv. Electroless Copper Solution A+B (10 minutes) – The sample midly agitated in the Cu coating bath, while keeping the bath temperature kept optimally at 40°C. The sample is rinsed with water after coating.
v. 5% Sulfuric Immersion (short) - Neutralizes the surface. The sample will then be rinsed with water.
vi. 20% HCl Acid Soak (10-60 sec.) – After a short HCl dip, the sample will be rinsed with water.

In Figure 23, electroless copper coating bath and cross-sectional microscopy image of electroless Cu plated 200 µm vias are presented.

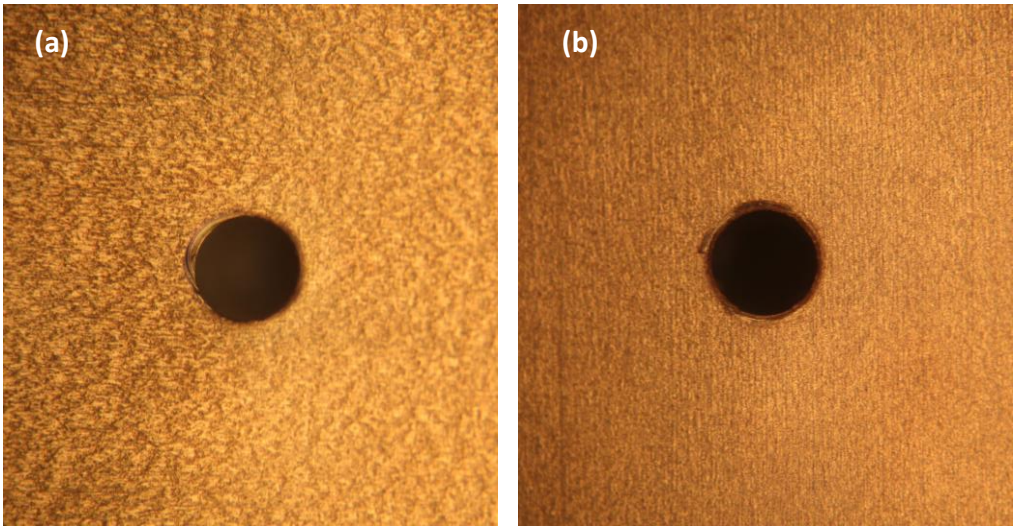


Figure 22 Cleaning and surface preparation after drilling: (a) before the chemical cleaning procedure, (b) after the chemical cleaning procedure described above.

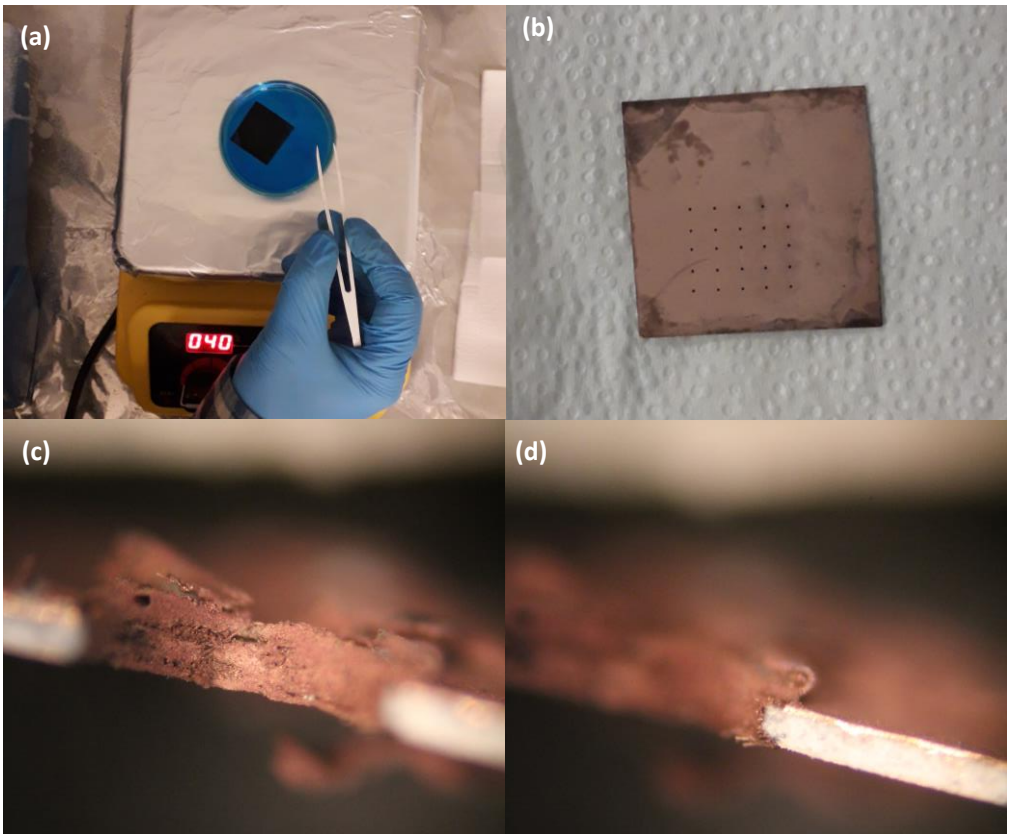


Figure 23 Electroless Cu plating: (a)lectroless Cu deposition bath, (b) sample after Cu deposition bath immersion, pink Cu color is achieved, (c, d) Crosssectional microscope image of plated vias.

Electroplating bath of Transene Company was used for the experiments of electroplating of the 200 µm vias. This electroplating bath is premix of copper sulphane and sulphiric

acid without additives. The electroplating bath is shown in Figure 24(b). Electroplating is continued for half an hour with a constant current of 200 mA, with a 1:1 ratio of anode to cathode ratio. The electroplating setup is shown in Figure 24.

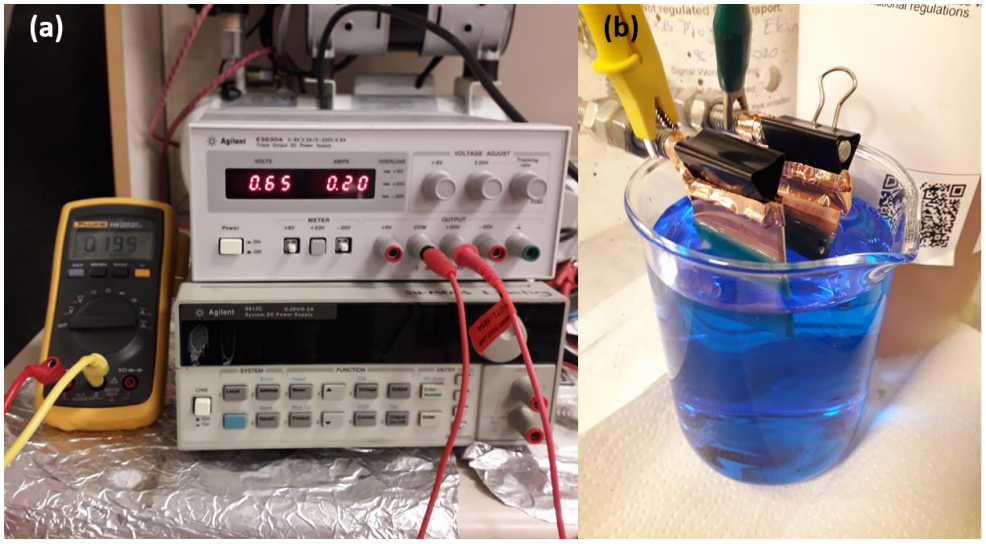


Figure 24 Electro plating setup: (a) power supply current monitor, (b) electroplating bath.

SEM images of the metallized and electroplated Astra MT77 are shown in Figure 25. The samples were cut mechanically through the via diameters and placed in the 45° SEM sample holder. It has been observed that a consistent copper coating is formed as a result of electroplating in the holes drilled into the area of 1 cm by 1 cm in the laminate material. Successful metallization followed by electroplating resulted in uniform copper coating through via wall that can be seen in Figure 25 a), b), c), d). Figure 25 e), f) demonstrates unsuccessful metallization caused by lack of electroless copper plating, as a result electroplated copper did not deposit on via wall.

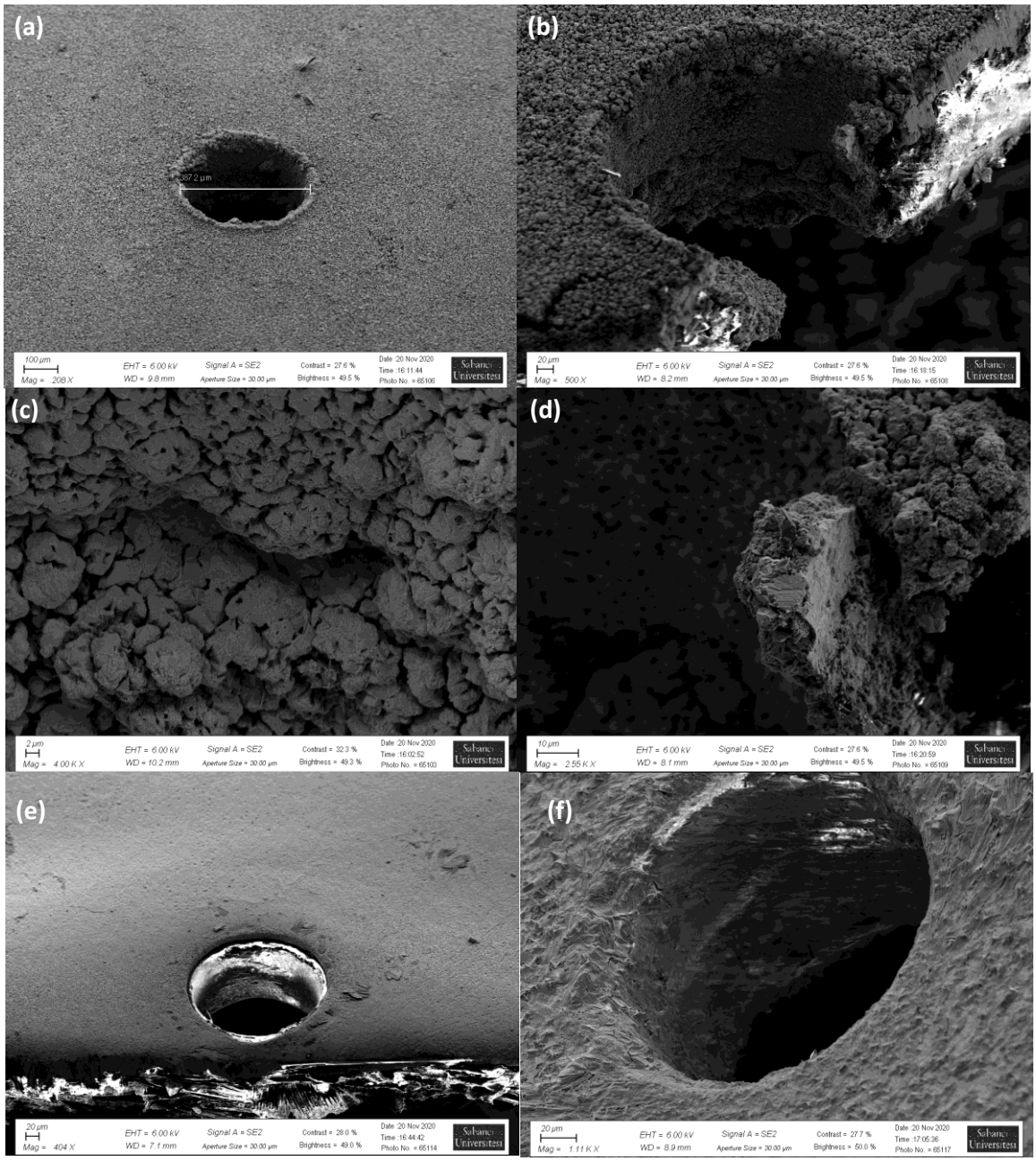


Figure 25 SEM images of electroplating result; (a) MT77 sample, (b) MT77 wall cross-sectional view, (c) MT77 plated in-hole wall surface, (d) MT77 inner-hole wall copper thickness, (e) unsuccessful electroless plating resulted in unmetallized via wall and, (f) partially plated via.

The measurable bath parameters are current density, concentration of copper sulfate and sulfuric acid solutions, and bath temperature. Factors such as air mixing, mechanical agitation and chemical stability cannot be followed due to the limitations of the simple experimental setup constructed in a beaker.

Electroplating experiments for microvias with 100 µm in diameter and 780 µm in depth (AR 1:7.8) are performed with premixed, commercially available copper sulphate:sulphuric acid Cu electroplating bath from Transene Inc. Figure xx presents the electroplating results where plated copper excessively grows on the edge of the via opening, leading to void containing through-holes and via pad conglomerate. Additive free acid type Cu electroplate bath may result in successful coating on planar surfaces, however, results presented in Figure 26 shows that additive free (eg. Brightener, leveller, supressor) bath directly deposits Cu on via hole edge where electric potential is highest around it, leading to immature closure of via hole. Further investigation showed that there was thin electroplated Cu in the through hole.

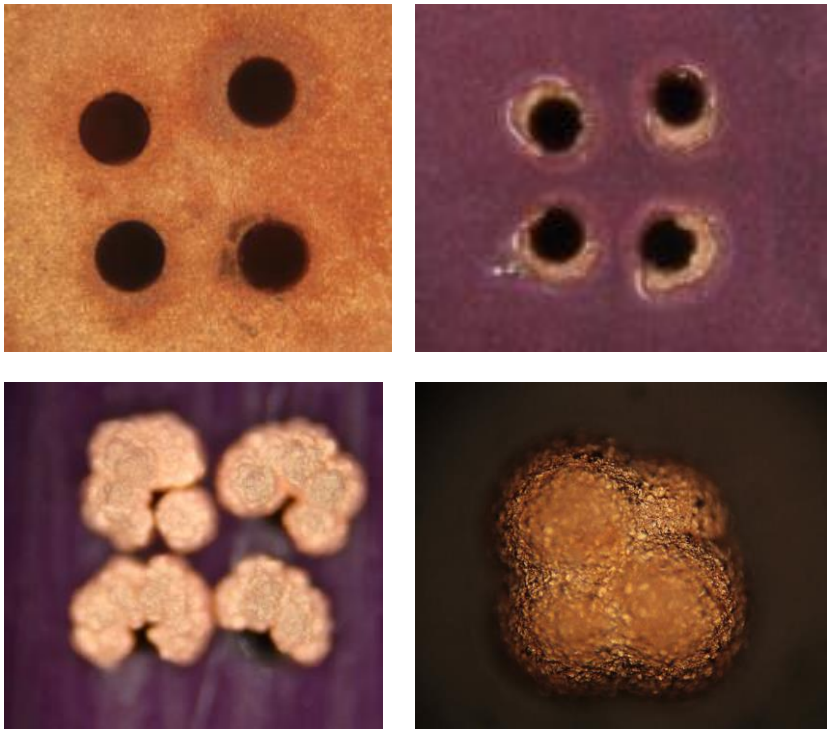


Figure 26 Electroplating of via holes with Transcene Acid Type copper plating bath.

Further development for electroplate bath chemistry is achieved by adding premixed leveler-brightener solution along with chloride to the plating solution and integrating air agitation to the plating beaker. Plating chemistry of CuSO4, H2SO4, Cl- and additive concentration is given in Table 5 where the resulting via filling profile is given in Figure 27.

Table 5 Optimized via filling bath composition

Copper Sulphate	Suphiric Acid	Chloride Ion	Additive Solution	Current Density
75 gr/lt	50 gr/lt	50 mgr/lt	15 ml/lt	1.5 A/dm^2

Figure 27 Microvia filling with optimized, additive enhanced plating acid type bath..

The filling profile in Figure 27 was obtained by observing the controlled-advanced in-hole copper filling at regular time intervals. In addition to via filling during plating, copper growth is observed around the walls of the holes. The vias of the 120 µm diameter drilled along the stack-up, however electroplating is continued till total via closure is observed; 60 µm of copper is overplated as a result. To overcome the problem of Cu growth over dry film resist, etch-back technique has been developed to meet the specific criteria in the Multilayer HDI PCB Specifications Table (see Appendix-2: HDI requirements). Development and results for the etch-back technique is further explained in Chapter 7.

6. DEVELOPMENT AND OPTIMIZATION OF LITHOGRAPHY AND ETCHING PROCESS ON PREPREG-COPPER LAMINATES

In HDI PCBs, photolithography technique utilized to pattern ~18micron thick copper foils in different layers at a resolution of ≤ 2 mil (~ 25 μm) (line width, and distance between lines). Relatively thin AZ 5214(1.53 μm at 4000 rpm – 2.18 μm at 2000 rpm), which offers strong surface adhesion in lithography processes, that is resistant to wet etching processes, is applied with spin coating in scneraios where copper thickness and PR trace gap ratio of ~ 3:4. In the case of thicker copper where aspect ratio approaches to 1:1, and AZ 4620 (12 μm) photoresist materials is used. In high viscosity materials, AZ EBR (PGMEA-propylene glycol methyl ether acetate) is used to remove the thick layer formed around the sample after spin coating and to dilute the resist. The samples are illuminated with Midas MDA-60MS mask aligner, Fortex double-sided UV box, and in-house built litography setup. Developer solutions used for the illuminated resist are AZ400K(1:4) for AZ4620, MIF726 for AZ5214, and 1% NaOH solution for dry film photoresist and solder mask.

After patterning the photoresist, the copper layer is wet etched with the Transene CE-100 ferric chloride solution. Initial etching experiments were carried out at room temperature, the etch rate and the amount of under-cut is determined. Optimization of etch parameters started with these conditions. The etch rate is expected to be 0.5 μm, so if deemed necessary the solution is either diluted or heated to provide more controlled etch and under-cut profile. Since the copper surface can be easily oxidized, the copper oxide layer on the surface is removed by immersing the sample in Transene COR-100 copper oxide remover solution before PR spinning. After etching, the photoresist layer is stripped from the surface either with Technistrip P1316 solution or acetone and isopropil alcohol wash. Process development studies based on PL 177 photoresist are evaluated in larger samples

and scaling studies presented in Appendix C. The fabrication steps that require lithographic processes consists of either dry film resist lamination and patterning or liquid resist spin coating and patterning. Dry film resist application for etching had been the initial goal for HDI PCB fabrication since this process is widely adapted in the industry for the patterning of the PWB boards.

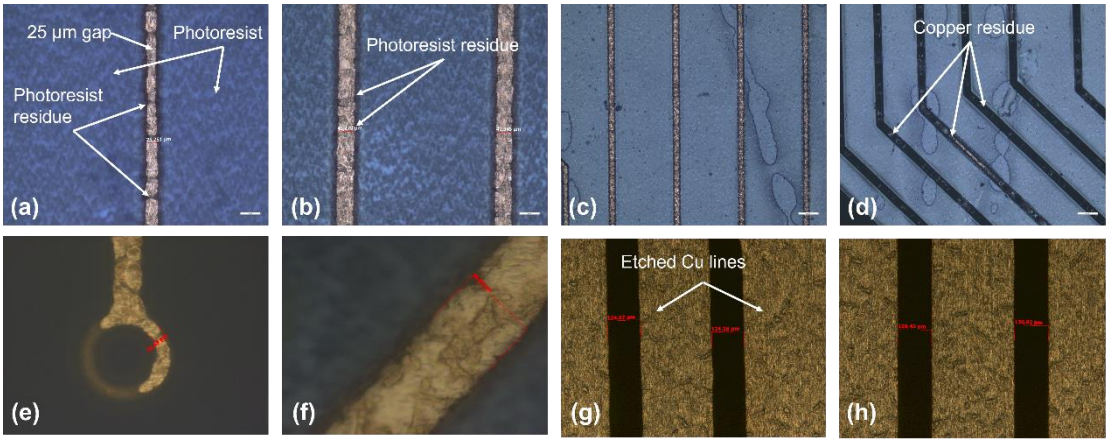


Figure 28 Dry film resist lithography and etching experiments: (a,b,c) 25 µm line opening in dry film photoresist, (d) copper residue after etching,(e,f) dry film residues after development, and (g,h) residue-free etching profile after plasma PR residue ablation.

The dry film resist (Ordyl Alpha940- 40 µm) is laminated on the prepreg-copper laminate at low speed at 115 °C. Various illumination and development time studies conducted; as a result, illumination energy of 40 mJ/cm^2 and development time of 5 minutes in 1% NaOH solution with moderate agitation is achieved. Initial experiments were targetted to obtain patterns under 50 µm along the photoresist, hovewer, it was observed that the residual photoresist material and photoresist bridges remained in the channels. These channels and residues cause residual coppers after copper etching. Plasma abletion application is an effective process for ablaiting photoresist residues from inside of the lines and breaking photoresist bridges before etching while using dry film resist. The residues seen in Figure 28 b), e), f) cause the copper residues seen in Figure 28d after etching. N_2 plasma application has been found effective way to remove these bridges and resulting copper residue but with the expense of line width expansion after the plasma application as shown in Figure 28 g), h). Dry film resist should be used when the average minimum line gap is 130 µm and above.

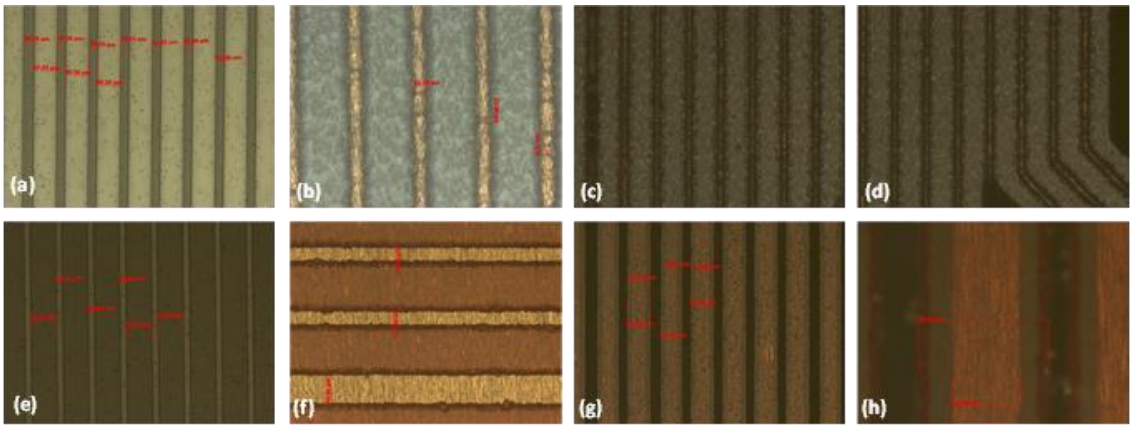


Figure 29 Lithography with dry film photo resist and AZ4620 with same transparency: (a)Transparency having 25 µm openings, (b)Developed dry film resist, (c, d) Etching results with dry film resist, residual copper.

High density pattern containing mask was designed to investigate the lithography performance for HDI standarts. Dry film resist and AZ4620 are patterned with the same mask to investigate for their etching performance. Patterns of dry film resist is shown in Figure 29 a), b), c), d) and patterns with AZ4620 in Figure 29 e), f), g), h). Figure 29e shows the high line density region of the mask used in the fabrication of the samples where 50 µm copper trace and 50 µm gap is achieved after etching. Line gaps in the mask designed with under-cut correction, where line gaps are 25 µm in developed PR trace.

The preliminary etching experiments are done with the recipes that had been developed on sample sized boards (3 cm by 3 cm) are applied on a 10 cm by 10 cm, 5 mil thick, 18 µm copper-laminated core material on their both sides sequentially. The cleaning process of the copper surfaces to be coated with resist is completed by rinsing with deionized water after washing with acetone and isopropyl alcohol respectively. Sample is hard baked at 130 °C for 90 seconds to evaporate the solvents from the surface of the cleaned core material. Since the pattern resolution planned to be transferred on PR with copper thickness is AR ~1:3, AZ4620 photoresist material is used. The spin coating process is completed by spinning the photoresist at 500 rpm for 10 seconds and spinning at 2000 rpm for 20 seconds. The coated photoresist thickness is aimed to be 12 µm. Soft bake is performed on the hot plate for 180 seconds at 110 °C. Photolithography was carried out with Midas mask aligner. The illuminated photoresist was developed in a 1:4 solution of AZ400K and deionized water for 3.30 minutes with moderate agitation. Figure 30 shows the photoresist lines that protects the copper during etching. Figure 30a shows ~200 µm

and 500 µm lines and a 200 µm wide via pad pattern is presented in Figure 30 c). In Figure 30b and Figure 30d, 60 µm line width and 50 Via pad in µm radius is shown.

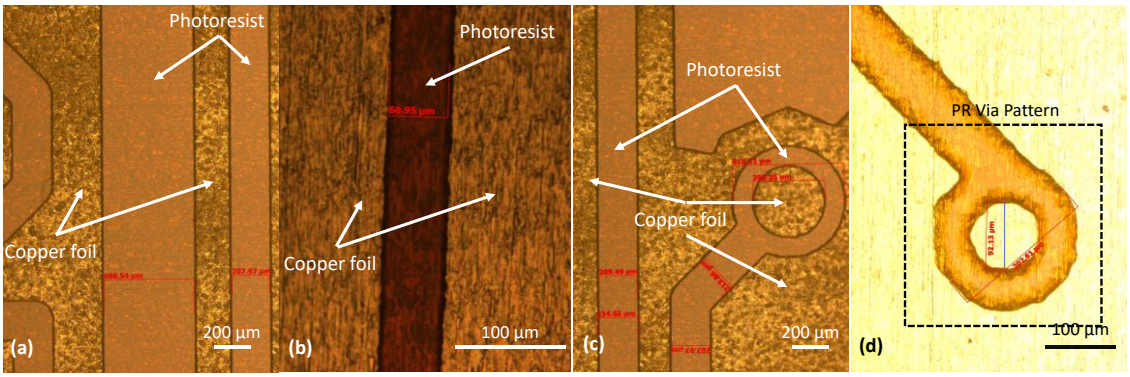


Figure 30 Lithography of AZ4620: (a) ~200 µm and 500 µm lines, (b) 60 µm line, (c) 200 µm wide via pad and, (d) 100 µm via pad.

After patterning, the copper layer is wet etched with Transene CE-100 solution containing ferric chloride. The etching rate and under-cut profile were determined by etching at room temperature with slow agitation. The etching results before optimization are given in Figure 31. Lines with a photoresist width of 220 µm, shown in Figure 31 a), resulted in copper line width of approximately 130 µm as a result of the isotropic nature of wet etching with ferric chloride. Under-cut profile is approximately 40 µm as shown in Figure 30 b), c), d).

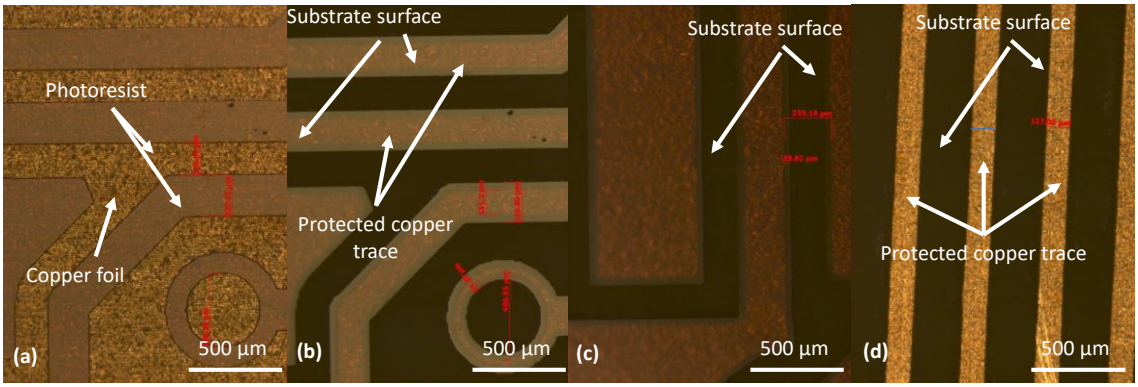


Figure 31 Etching results: Slow agitation at room temperature.

Increasing the etchant temperature to 50 ºC, decreased the etch time to 8 minutes from 13 minutes, resulting in 21 µm under-cut. Further improvement on etch rate was achieved by increasing the etchant temperature to 80 ºC while agitating the solution strongly, that resulted in 12 µm under-cut where undercut amount and the metal thickness ratio reached

approximately to 0.55 with temperature and agitation optimization. In Figure 32, optimized etching results are given. 10cm by 10cm prepreg-copper laminates are given in Figure 32 (a) and Figure 32 (b), etched specimens with 190 µm line width (a) and 40 µm line width(b) are shown.

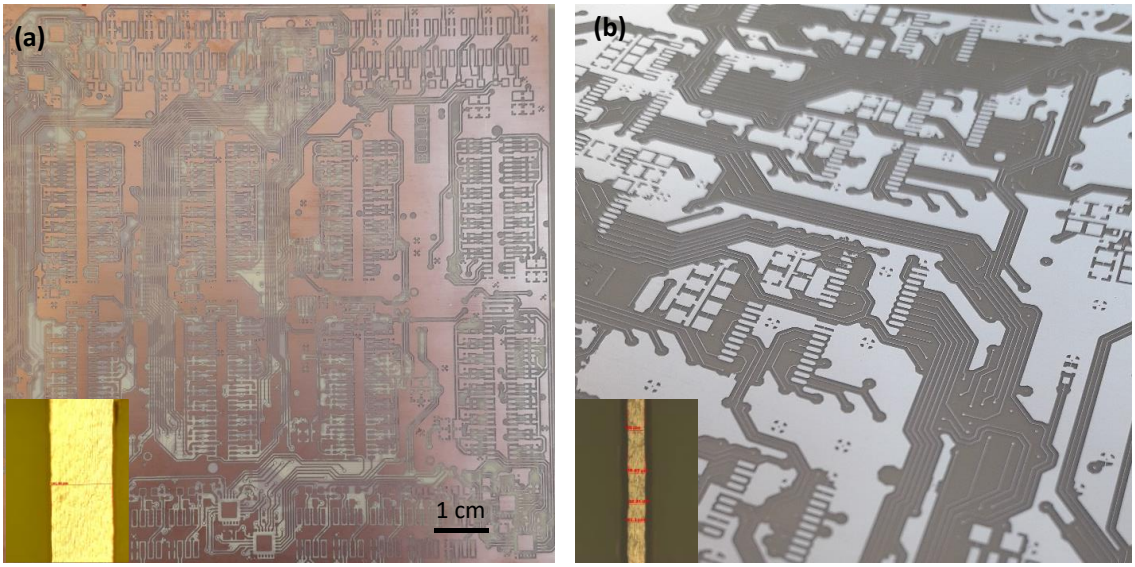


Figure 32 Optimized etching results for 10 cm bu 10 cm samples: strong agitation with 80 ºC etchant.

At the end of the process optimization, a 3.30-minute etching recipe was determined, in which under-cut was reduced by heating the etchant and introducing strong agitation. If lower undercut amount is necessary, intermittently stopping the etching and hard baking the sample at 130 °C can be applied to reflow the resist to protect the sidewall to decrease undercut.

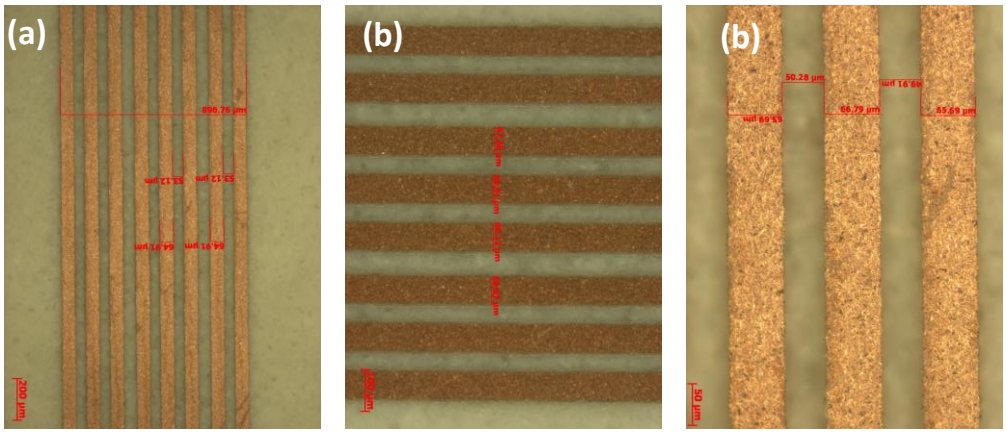


Figure 33 Etching results: Further improvements for undercut by hardbaking AZ5214.

Relatively thin resist of AZ5214 is also investigated for patterning studies. Since this resist material is thinner compared to AZ4620, when it is exposed to heat treatment after being developed, it reflows much less than in thick resists such as AZ4620, thus being suitable for extra hardbake step to promote further resist adhesion to copper surface. This hard bake step helps to protect the lines shaped by lithography during etching. Patterning studies with AZ5214 are shown in Figure 33. Line gaps are realized as 50 μm indicating that undercut amount can be further decreased with AZ5214 based etching.

7. PROCESS INTEGRATION FOR 2N2

Lamination, hole drilling and metallization if there are vias, dry film resist lamination, wet resist spinning, photolithography, and etching are the fabrication processes used in each layer of the production flow. Apart from these processes, the fabrication flow should include nickel and gold plating for the final surface finish, as well as solder mask application. Development and optimization of each of these steps are discrete processes. These development and optimization studies have been discussed in previous chapters. However, individually optimized processes may not perform well in stack-up fabrication; additional process integration work may be required.

While laminating the first and nth layers, which are Prepreg-Cu layers, to the second and n-1st layers, the prepreg thickness and number of prepregs affect the final stack-up thickness, whereas the layer thickness affects the path travelled by the drill bit during mechanical drilling. Drilling efficiency decreases significantly for a 2-N-2 stack when 300 µm thick prepregs are used in the second and n-1st layers, as well as the first and nth layers after the core layer. When the stack thickness exceeds 1 mm, 100 µm drill bits are not viable to be used to create vias. When laminating each new prepreg-Cu layers, it is not feasible to use prepregs thicker than 5 mil. Throughout the stack-up integration, a 5 mil thick prepreg is used for the lamination of prepreg-Cu pairs.

There are two wet etching recipes optimised for the 18 µm thick copper foil in the etching processes applied in each layer beginning with the core layer during the fabrication process. While the relatively thick AZ4620 resist allows for etching on 18 µm copper foil that meets HDI requirements, it is better suited for etching thick copper layers (35 µm) in non-critical dimension scenarios.

Etchback process is employed in the fabrication flow after selective copper plating of the vias. In order to ensure that the vias are totally filled with copper, plating is continued further continued. As a result, 60 µm copper was grown on dry film resist surface on x-y plane. This mushroom-shaped excess copper formation may cause problems in lithography and following lamination steps, an extra lithography and etching step, 'etchback', is introduced to the fabrication process. Etchback process requires to spin photoresist on top of a existing dry film resist and lithpgraphy. After soft bake, it has been observed that the AZ4620 resist material forms bubbles in cases where the surface has been electroplated or etched. In Figure 34 (c), (d), bubbles are depicted in regions where AZ4620 is subjected to height difference during the lithography process used to reduce the diameter of the electroplated copper grown on the dry film from 180 µm to 120 µm. Although these bubbles are not visible on the dry film resist surface, they are visible in the via region, indicating a difference in height. Figure 34 (b), similar PR defect formation is observed, indicating that AZ4620 material with the regular spin parameters cannot be utilized for etchback and etching processes where there is a hight difference in surface. As a result, the AZ4620 resist is suitable for etching the 35 µm copper layers and in applications where there is no difference in surface.

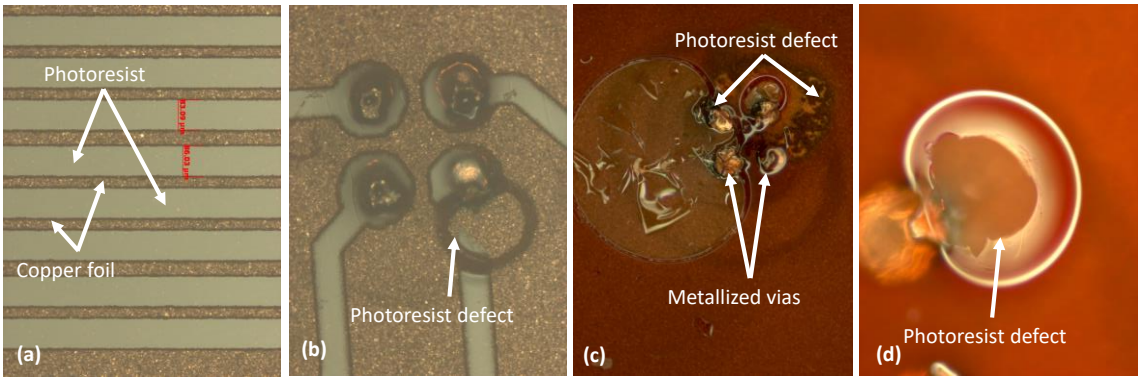


Figure 34 Etchback process development with AZ4620.

AZ5214 resist is used to back-etch the excess copper that grew on the surface in the x-y direction during electroplating. Spinning the resist on the dry film revealed conformal coating, despite the presence of a copper height difference on the surface. Figure 35 presents the result of etchback process, where for (a, a') 186 µm copper protrusions protected by a 150 µm circular pattern masked AZ5214. Without agitation, (a, a') copper ridges were etched at room temperature without agitation. The average copper diameter

was reduced from 186 µm to 126 µm following etching. Resulting electroplated vias created by the etchback technique are presented in Figure 35.

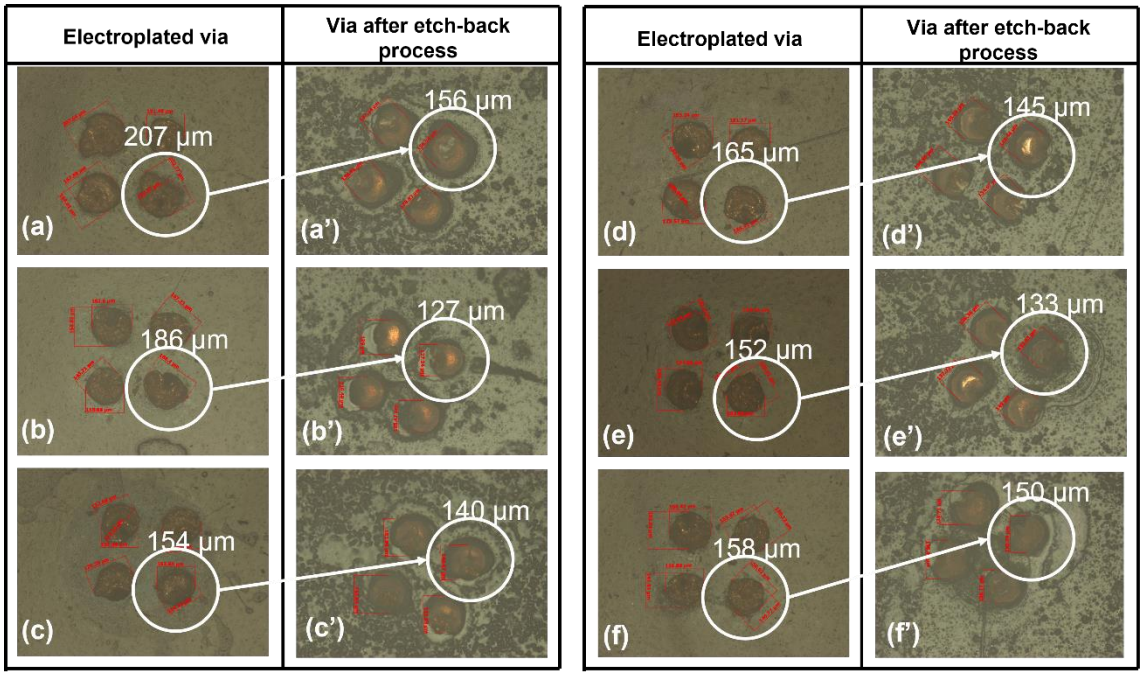


Figure 35 Etchback process with AZ5214.

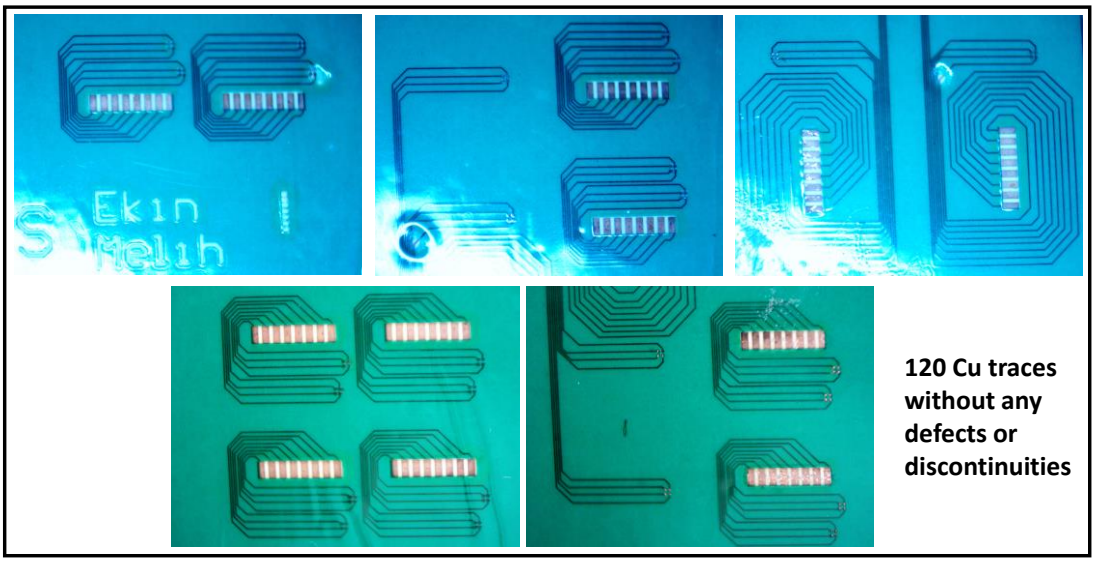


Figure 36 Realized copper traces with 50 µm line width and 50 µm trace gap under patterened solder mask

The patterning of the solder mask is another critical aspect of the process integration. As a matter of fact, a dry film resist with a thickness of 75 µm was used as the solder mask in this experiment. Unlike the dry film resist, the solder mask adhered strongly to the

acetate mask during hard contact and delaminated from the sample surface while trying to align. Therefore, when laminating the dry film solder mask, the polyester film on the surface should be kept until prior to development.

The results of dose tests on the relatively thick dry film solder mask resist are depicted in Figure 37. There are 250 µm distance between the centres of the illuminated mask's circular paterns, which corresponds to the diameter of the mask and the center-to-center spacing of the mask. Additionally, it contains patterns with widths ranging from 30-40-50-100 µm, which are used to determine the smallest possible solder mask bridge. The dry film solder mask is illuminated with a power of 13.5 mW/cm for 3.5, 10, 20, 25, and 30 seconds. The protective polyester film between the resist and mask was removed after illumination, and the samples were allowed to sit for 10 minutes before being developed. Using a different amount of illumination energy, the best result was obtained for the resist developed in 1% NaOH solution for 5 minutes.

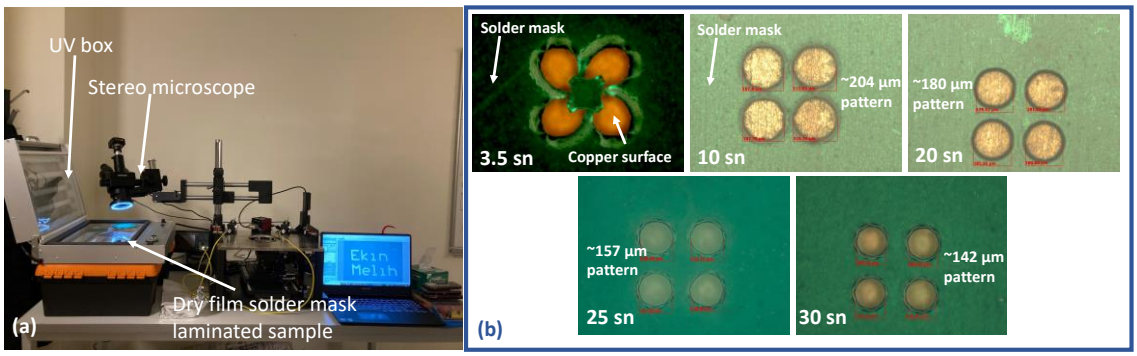


Figure 37 Solder mask lihography experiments: in-house build solder mask lithogprahy setup (a), dose tests for dry film solder mask(b)

Following the completion of the dose tests, patterning that required the alignment of the first and nth layers with the solder mask paterning mask were not succesfully completed in Midas mask aligner which is used to pattern copper layers with thicknesses of 18 um and 35 um. Device's microscopes were not able to resolve the alignment markers beneath the 75 micrometre thick resist. In order to solve this problem, experimental setup depicted in Figure 37 (a) was created. Fortex's Double Sided UV Box and a stereo microscope with a larger field of view is combined. The UV box, in conjunction with an on-board digital timer, is used to adjust the total amount of applied energy. The stereo microscope was able to resolve the alignment markers despite the 75 µm thick resistin being present. However, due to the lack of a micromanupulator in this setup, it is difficult to ensure that

the sample and mask are perfectly aligned; the sample and mask were manually aligned. Vacuuming with a flexible transparent film ensures that the mask and the sample are in contact with each other. As a result, because this device was not intended for HDI production, the system's margin of error was to high to achieve the precise alignment that was required. Manual alignment with the UV box revealed a misalignment of at least 30 µm. In Figure 38, developed solder mask and created solder mask bridges are presented.

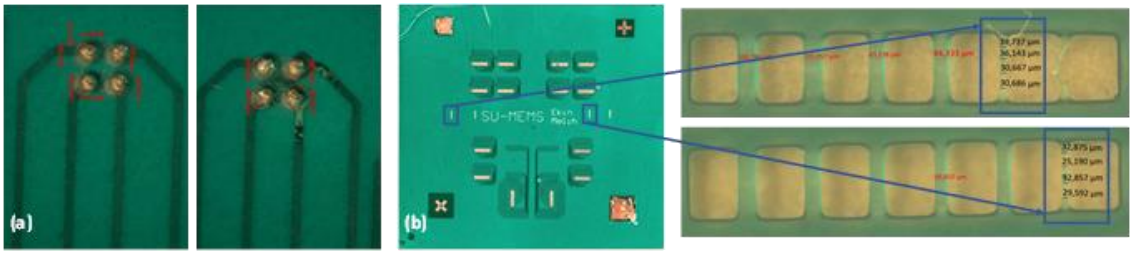


Figure 38 Solder mask lithography: (a) developed solder mask pattern and, (b)developed solder mask bridges.

8. CONCLUSION

Main focus of this thesis was to introduce fabrication process flow and integration techniques for HDI-PCB structures, along with investigating each fabrication process in relation with HDI fabrication process and development and optimization of individual processes for the proposed fabrication process. Within this focus, several fabrication process flows and sub-process flows for various types of HDI structures are investigated and cleanroom compatible fabrication process for Type-III HDI structure is introduced.

The outcomes of the studies in this thesis can be classified in two general aspects: process developments and optimizations on epoxy-based glass reinforced/Cu substrates and process integration and fabrication flow design.

Key outcomes and contributions of this study are:

- Presented and realized process flow for Type-III HDI stackup that is low-cost, accessible
- Introduced reverse etchback process of electroplated vias with liquid photoresist and lithography on dry film resist, and etching
- Etching recipe development and undercut reduction optimization with etchant temperature, reflow, agitation rate experiments
- 100 µm microvias using low-cost mechanical drilling and employed Cu-foil surface protection method with PL177 photoresist spin and lithography from mechanical damage/deformation caused by CNC-head scraping
- Employed lithography setup for thick solder mask illumination, which has potential for further development to be utilized in Cu-foil etching lithography

Processes and materials involved in HDI-PCB fabrication are discussed with great detail in Chapter 2. In Chapter 2.2, proposed fabrication flow has been introduced and presented in great detail for the Type-III 2-N-2 structure. In Chapter 3, Chapter 4, Chapter 5, and Chapter 6 development and optimization processes for prepreg/Cu lamination, mechanical microvia formation, throughhole metallization, lithography and etching are discussed. This is a successful fabrication process development study for manufacturing a HDI-PCB that is cleanroom compatible, covering most common type of stackup architecture. Besides obtaining a repeatable fabrication process flow and successful sub-processes, it should be noted that having the process parameters for prepreg/Cu laminates and layer pairs allows the experimenter to access and achieve further process designs and other HDI types.

Mechanical microvias were achieved within the HDI limits of having diameter smaller than 150 µm using commercially available Protomat S104. Microvias structures upto AR: 7.8 are successfully metallized with electroless copper plating, and selectively filled with optimized copper electroplating process. Lithography processes are optimized for the patterning of copper layers, achieving PR gap to copper thickness ratio of 0.72. Developed etching recipe was optimized for minimum under-cut amount, down to 12 µm for 18 µm copper foil thickness. Dry and liquid photoresists systems for patterning of copper layers with 50 µm line width and 50 µm line gap is achieved on 18 µm copper foils. Prepreg/Cu layer pair laminations was achieved with a total of 5.93% height difference for sequential build-up architecture which consist of two lamination steps. Drilling of 100 µm vias in 175 µm via pads with center-to-center distance of 250 µm was achieved within a 10% error margin throughout 10 cm by 10 cm active HDI board area. Dry film solder mask, 75 µm in thickness, application process is developed, with overcoming the device limits of mask aligner system for thick materials with specifically process built lithography setup.

Individual process development and optimizations presented in this thesis will be instrumental in gaining and transferring the state-of-the-art in HDI-PCB fabrication. This thesis presents a process integration and repeatable fabrication process that starts with the

preparation of the core structure and ends with solder mask applied and selectively gold plated Type-III HDI structure.

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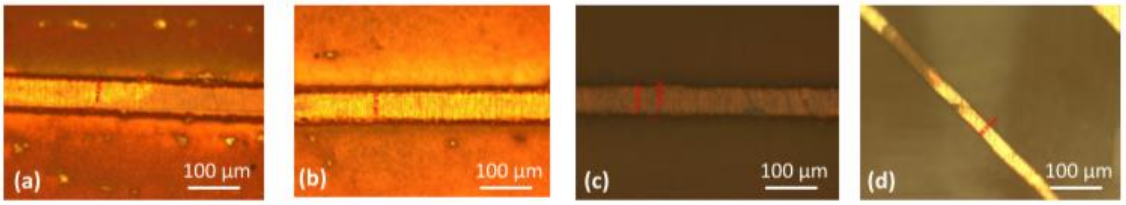
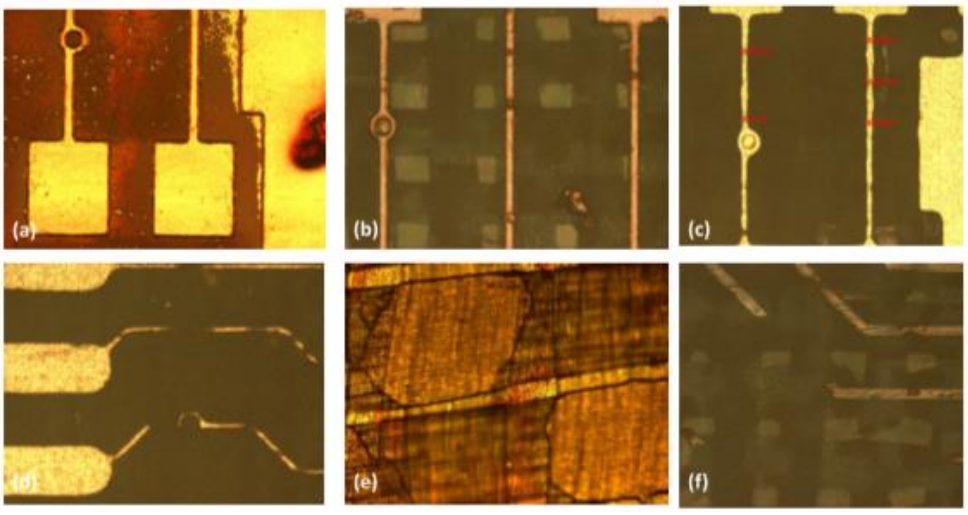
APPENDIX A

Effect of Inconsistent Prepreg Topograhy on Shaping

Patterning studies were also carried out on a semi-cured sample produced by the project group, with the 18 micron copper-coated sample using the hot pressing method and the prototype core material produced in-house. Controlled etching profile of the core material produced by the project group is shown in the figure.



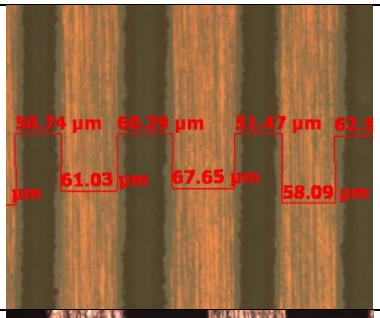
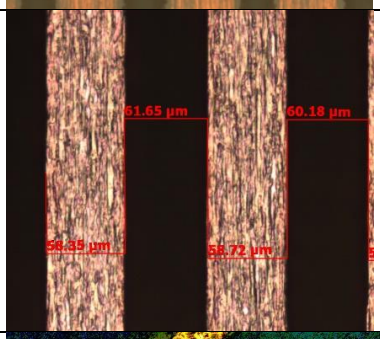
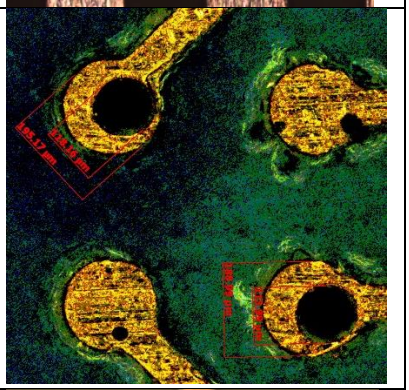
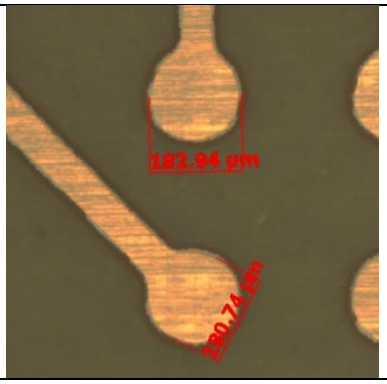
It has been observed that the patterened HC-5 sample has both successful and inconsistent etching areas in different regions on the surface. Since the surface topography of the produced prepreg material does not show uniformity throughout the sample; caused by e-glass intersections that are leading to varying thickness profile. The structural texture of e-glass was observed on copper during lamination. Irregular line widths and broken lines were observed in these regions. Another problem encountered is that there are air gaps in the intersection areas of the e-glass threads. In the wet etching process, these regions form areas where etching cannot be controlled. Inconsistent line thickness is observed.

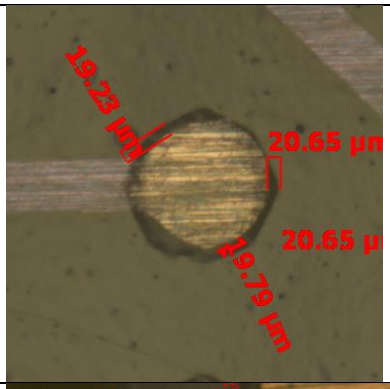
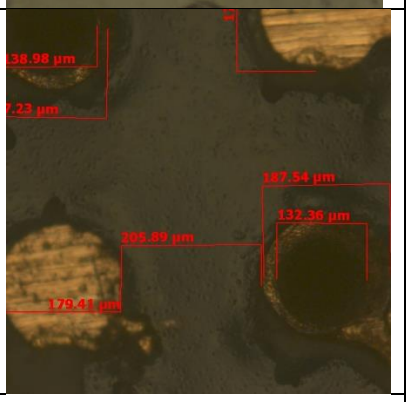
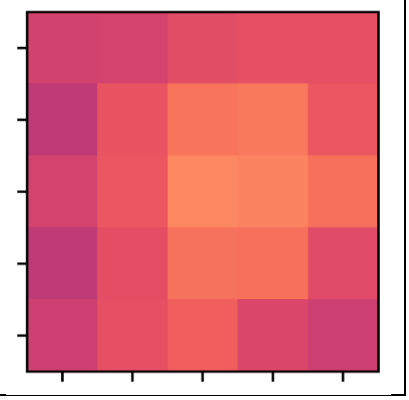


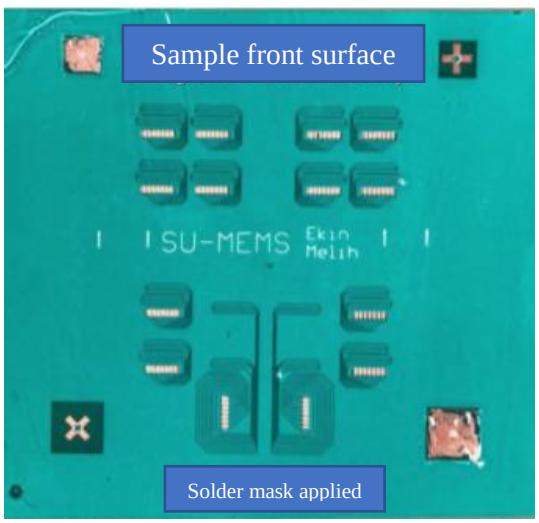
However, throughout the board surface, some regions showed local consistency similar to the ideal situation, showed a consistent etch profile in accordance with the expectations. Consistency of the produced core material thickness profile, copper surface formation, copper-prepreg adhesion, and the production of void-free, high-consistency prepregs are fundemantel structural criterias for successful microfabrication on the surface.

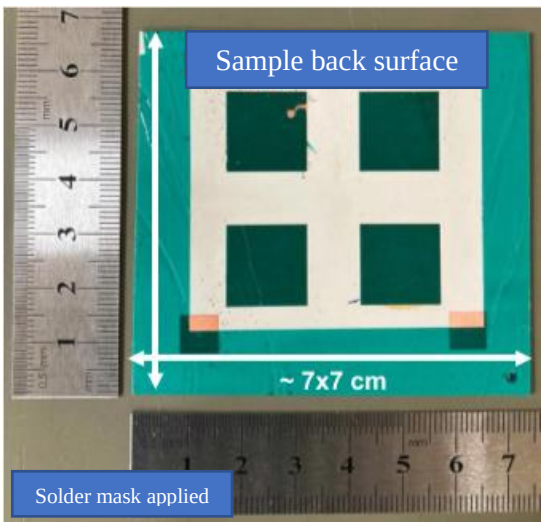
APPENDIX B

HDI PCB Requirements and Fabricated Stack-up Specs

Gerek Adı	Level A	Level B	Level C	Realized Process Outcome	
Minimum line width	127 µm	75 µm	50 µm✓	50 µm✓	
Minimum line gap	127 µm	75 µm	50 µm✓	50 µm✓	
Minimum mechanical via diameter	102 µm✓	76 µm	51 µm	100 µm✓	
Microvia capture land size	406 µm	330 µm	229 µm	175 µm✓	

Solder mask to capture land gap	-	-	-	20 µm✓	
Distance between to vias	-	-	-	200 µm✓	
PCB thickness variation	-	-	-	Average 750 µm✓, min.729 µm, max. 775 µ	



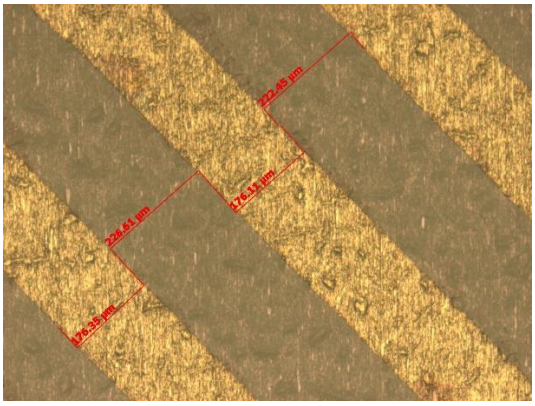


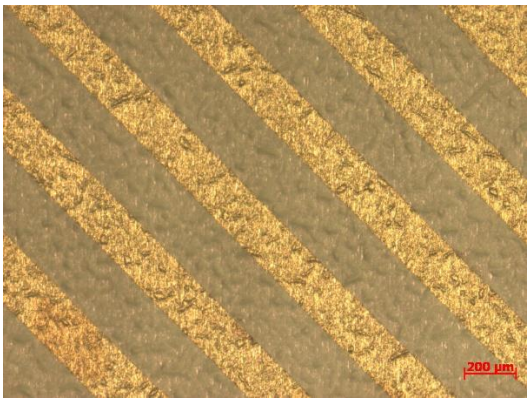
APPENDIX C

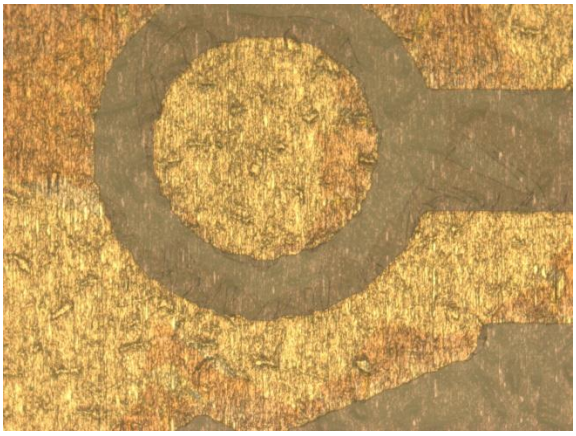
PL177 Protective Photoresist Spin and Lithography Parameters

Resist	PL177
Acceleration	500
Spin speed	2000
Air flow	Blocked
Soft bake time	8 min
Soft bake temperature	110 °C
Exposure dose	400 mJ/cm^2
Development	AZ 400K:DI 1:4 15 min

Spin and patterning parameters for PL177







Resist	PL177 Diluted with AZ EBR 1:0.5
Acceleration	500
Spin speed 1	2000
Spin time 1	120 sec
Spin speed 2	4000
Spin time 2	180 sec
Air flow	Blocked
Soft bake time	15 min
Soft bake temperature	90 °C
Exposure dose	100 mJ/cm^2
Development	AZ 400K:DI 1:4

Spin and patterning parameters for diluted PL177