High Responsivity Power Detectors for W/D-Bands Passive Imaging Systems in 0.13µm SiGe BiCMOS Technology

Berktug Ustundag[*], Esref Turkmen[*], Barbaros Cetindogan[#], Mehmet Kaynak[#], Yasar Gurbuz[*]

[#]*IHP, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany*
[*]*Sabanci University, Orta Mahalle, Universite Cd. No:27, 34956 Istanbul, Turkey*
yasar@sabaciuniv.edu

***Abstract* — This paper presents the design, implementation and measurement results of power detectors (PDs) operating at W-band and D-band. Two detectors are designed and fabricated in 0.13µm SiGe BiCMOS technology. The measured minimum NEPs are 0.43 and 4.2 pW/Hz$^{1/2}$, and the peak responsivities are 772 and 132 kV/W for the W-band and D-band power detectors, respectively. Both the PDs have wideband input matching to improve the performance over the entire bandwidth and occupy less than 0.37 mm^2 of area. The fabricated chips demonstrate the state-of-the-art responsivity performance to be utilized in W/D-bands radiometer systems.**

Index Terms* — *Millimeter wave detectors, Millimeter wave circuits, millimeter wave radiometry

I. Introduction

Design of millimeter-wave (mm-wave) integrated circuits (ICs) is an active area of research, driven by the potential applications and enabled by the advancements in process technologies such as CMOS and SiGe BiCMOS. The unique properties of mm-wave spectrum such as low attenuation through fog, rain and dust and the existence of atmospheric propagation windows at 94 and 140 GHz are especially significant for passive imaging systems. Aircraft guidance, low visibility navigation, surveillance, beacon detection, oil spill detection, search and rescue, ground navigation, concealed weapons detection are some of the passive imaging applications that could potentially benefit from high performance mm-wave ICs [1].

Power detector is one of the fundamental blocks of a radiometer system. The sensitivity of a radiometer is determined by couple of factors such as the pre-detection gain-bandwidth, integration time and the noise equivalent power (NEP) of the detector. The PD has a large impact on the system specifications such that the noise and the responsivity of the detector dictate the required gain of the pre-detection stage.

SiGe HBTs are widely used in high frequency and low power applications since bandgap engineering enables SiGe process to achieve high cutoff frequency (f_t), maximum oscillation frequency (f_{max}), early voltage (V_A), high breakdown voltage (BV_{CEO}) and low 1/f corner frequency [2]. In this work, we present two high responsivity power detectors, operating at W-Band and D-Band using IHP's SG13G2 0.13µm SiGe BiCMOS process featuring HBTs with 300 and 500 GHz f_t and f_{max} respectively.

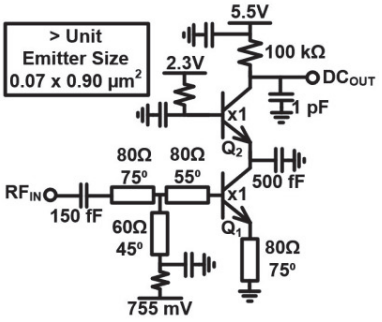


Fig. 1. Circuit schematic of the designed W-band power detector.

II. Circuit Design

A. W-Band Power Detector

The schematic of the W-Band PD is shown in Fig. 1. The input power is detected through the input transistor (Q1) that generates a DC current proportional to the input power which than reflected on to a load resistor to obtain the corresponding DC voltage at the output. The output transistor (Q2) has several desired functions. It essentially acts as a buffer between the load resistor and the input. The use of Q2 fixes the collector voltage of Q1 thus helping Q1 to stay out of saturation independent of the input power. Q2 could still be saturated in this case, but now the maximum voltage drop at the output is determined by the BV_{CEO} of Q2 instead of Q1. This is useful since it is shown that a SiGe HBT biased with a forced emitter current could have BV_{CEO} as high as the twice of an HBT biased from base [3]. This feature allows the designer to use a larger load resistance and high supply voltage without having dynamic range limitations and the large load will improve the responsivity of the detector. However, the use of Q2 has several drawbacks as well. Even though the output noise is dominated by Q1 and the load resistor, Q2 also contributes slightly to the overall NEP of the detector. Having Q2 also requires an additional bias voltage at the base which might not be desirable for single supply designs. Also, using a large load at the output also means that a relatively large supply voltage (5.5V in this design) is required to keep Q2 out of saturation which might not be applicable for certain system specifications.

The choice of load is crucial since both the responsivity and the NEP of the detector are largely affected by this resistor.

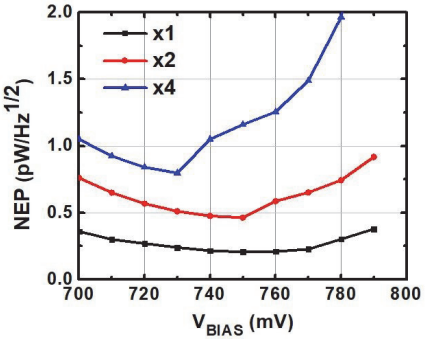


Fig. 2. NEP versus bias voltage for different number of transistors.

An analysis presented in [4] shows that the NEP is inversely proportional, and the responsivity is proportional to the load size. Having an arbitrarily large load is also not useful since the input impedance of the low frequency amplifier following the detector stage would lower the effective load impedance.

The bias point and the input transistor size are also extremely important to ensure having a low NEP. The HBT should operate in a non-linear region to maximize the second order response of the transistor. Fig. 2 illustrates the NEP vs bias point and the number of transistors. Using minimum number of transistors and biasing at the edge of active region results in minimum NEP. Based on Fig. 2, the bias voltage is set as 755mV.

Input matching is also significant since any reflected power would decrease the responsivity of the detector. Low bias current coupled with minimum number of transistors pose difficulty to achieve wideband matching. Nevertheless, in this design, the use of a shorted stub at the base of Q1 allowed us to obtain approximately 20 GHz of bandwidth with S11 better than -10dB.

The RF short capacitors at the collector of Q1 as well as the other bypass capacitors were implemented with metal-insulator-metal (MIM) capacitors. The capacitor at the collector of Q1 was used to cancel the fundamental harmonic of the input signal. Microstrip lines (MSLs) were used as TLs. MSLs were meandered whenever possible to keep the layout of the detector as compact as possible. Full chip EM simulations were performed in ADS to ensure a first pass design.

B. D-Band Power Detector

Fig. 3 presents the circuit schematic of D-band PD. A common-emitter topology was utilized in this design since at higher frequencies it is expected that the NEP would be higher due to lower responsivity caused by the weaker second order response of Q1. Therefore, in D-band PD circuit Q2 (cascode transistor) was not used to avoid its higher noise contribution. Consequently, the load resistance is also reduced to 20 kΩ with lower supply voltage of 3V and the additional bias voltage is removed.

The transistor size was doubled to bring the real part of the input impedance closer to 50 Ω to allow for a wideband

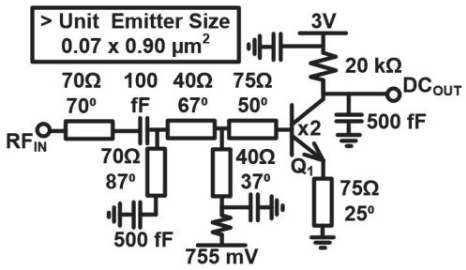


Fig. 3. Circuit schematic of the designed D-band power detector.

matching and double stub matching was employed utilizing shorted stubs. This ultimately increases the input ohmic losses, thus lowering the responsivity and increasing the minimum achievable NEP, while also keeping the overall NEP over the bandwidth lower compared to a narrowband matched detector. The bias voltage was kept the same as 755 mV for the reasons explained earlier. Similar to W-band PD design, all the TLs were meandered to reduce the total area.

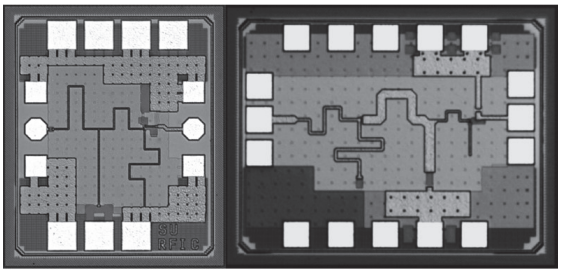
The 100 fF capacitance is used as DC block and also for matching purposes. All the resistors were implemented using polysilicon resistors. Custom designed pads with reduced area which would still allow for a reliable probe contact were used to minimize the shunt capacitance of the pads.

III. Results

The die photos of the PDs are shown in Fig. 4. The W-band PD occupies 0.35 mm^2 (0.54 x 0.65 mm) and the D-band PD occupies 0.37 mm^2 (0.69 x 0.53 mm) of area including the RF and DC pads. Both the power detectors consume less than 150 µW of power.

W-Band s-parameters were measured using a R&S WR10 frequency extension module configured with the VNA and 100µm GSG probes. The reference plane was set to probe tips by SOLT calibration using an Impedance Standard Substrate (ISS). The S-Parameters of the D-Band PD was measured using a R&S WR6.5 frequency extension module configured with the VNA and 75 µm pitch sized probes. Responsivity measurements of the PDs were performed using a coherent test setup shown in Fig. 5, consisting of a signal generator, VDI active multiplication chains, directional couplers, down-conversion mixers, and an oscilloscope to measure the output voltage changes. The input signals to the DUTs were AM modulated at 1 kHz with 100% modulation depth to emulate the effect of Dicke switching. The output noise power of the detectors at 1 kHz were measured using a spectrum analyzer and an external low-noise pre-amplifier (SRS 550), while the input of the PDs externally was terminated by 50 Ω. The gain of the pre-amplifier was de-embedded from the measurements.

S-parameter results are shown in Fig. 6. Input return loss of the chip remains below -8 dB from 77 to 109 GHz. S11 of the D-band PD is better than -8 dB between 118 and 165 GHz. The input power of the PDs kept below -35 dBm to ensure the detectors are not compressed.



(a) (b)

Fig. 4. Die photo of (a) the W-band PD (b) the D-band PD.

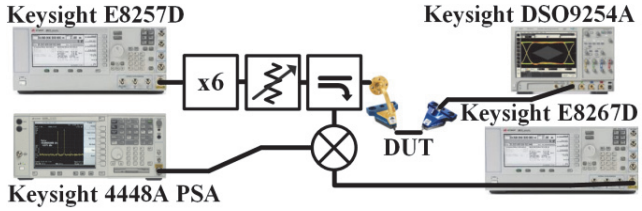
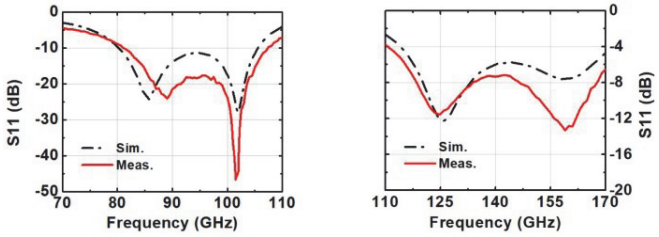
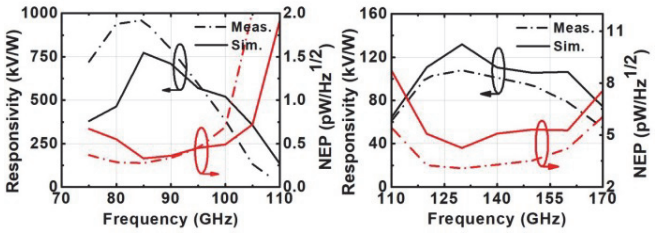


Fig. 5. Measurement setup for the responsivity



(a) (b)

Fig. 6. Simulated and measured S11 of the (a) W-Band PD (b) D-Band PD.



(a) (b)

Fig. 7. Simulated and measured responsivity and NEP results of the (a) W-band and (b) D-band PDs.

Fig. 7 shows the simulated and measured NEP and responsivity results of both the PDs. The peak responsivity of the W-Band PD is 772 kV/W and it stays above 450 kV/W between 80 to 100 GHz and the NEP is better than 0.5 pW/Hz$^{1/2}$ in the same frequency range, whereas for the D-Band PD, the peak responsivity is 132 kV/W and is above 100 kV/W for around %80 of the entire bandwidth. The NEP is slightly higher than simulations and it is better than 5.5 pW/Hz$^{1/2}$ between 120-160 GHz.

IV. Conclusion

The comparison of the presented PDs with recently reported state-of-the-art W-band and D-band PDs in SiGe BiCMOS technologies are presented in Table 1. Compared to other studies, better responsivity performances have been achieved through higher value load resistors. Although it results in lower compression point such as around -35 dBm, this is not a priority performance criterion for passive imaging applications. The measured minimum NEP of the W-Band is 0.43 pW/Hz$^{1/2}$ whereas the D-Band achieves 4.2 pW/Hz$^{1/2}$ of NEP at 1 kHz. The inputs of the both detectors are matched to 50Ω over a wide bandwidth to minimize the average NEP for wideband systems. The presented PDs are suitable for highly integrated mm-wave radiometer systems with excellent NETD performance.

TABLE I
Comparison With Reported W/D-Bands SiGe BiCMOS PDs

Ref.	Tech. f_t/f_{max} (GHz)	NEP (pW/Hz$^{1/2}$)	Resp (kV/W)	R_{LOAD} (kΩ)	S_{11} <-8 dB (GHz)	Area (mm^2)
[4]	0.18µm SiGe 200/200	0.5	91	23	75-100	0.43
[5]	0.12µm SiGe 200/265	3	12	0.75	86-102	0.14
[6]	0.13µm SiGe 300/500	0.4	80	10	78-87	0.2
W-band PD	**0.13µm SiGe 300/500**	**0.43**	**772**	**100**	**77-109**	**0.35**
[7]	90nm SiGe 300/350	1.25	14.5	1	N/A	0.02*
[8]	0.13µm SiGe 250/370	2.9	3	N/A	125-170	0.1
[9]	90nm SiGe 260/300	0.7	11	0.6	154-170	0.23
D-band PD	**0.13µm SiGe 300/500**	**4.2**	**132**	**20**	**118-165**	**0.37**

* Excluding pads

Acknowledgement

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