

# A Tunable SiGe BiCMOS Gain-Equalizer For X-Band Phased-Array RADAR Applications

Esref Turkmen, Abdurrahman Burak, Tahsin Alper Ozkan, *Student Member, IEEE*,  
and Yasar Gurbuz, *Member, IEEE*

**Abstract**—This paper presents a compact-size tunable gain-equalizer for X-Band Phased-Array RADAR applications in a  $0.25\mu\text{m}$  SiGe BiCMOS technology. An isolated NMOS based variable resistance was used for the first time to tune the slope of the gain-equalizer. For NMOS, an isolated body created by a deep n-well was utilized to reduce insertion loss due to the substrate conductivity. Furthermore, the power-handling capability of the tunable gain-equalizer was improved thanks to the resistive body-floating technique. The designed tunable gain-equalizer operates in the frequency range from 8 to 12.5 GHz with a measured positive slope of 1 dB/GHz and 1 dB tunable slope. The effective chip area excluding the pads is  $0.21\text{ mm}^2$ , and the total area including pads is  $0.31\text{ mm}^2$ . To authors best knowledge, this study is the first tunable gain-equalizer in SiGe technology presented for X-band phased-array RADAR applications.

**Index Terms**—slope-compensation, T/R Module, isolated NMOS

## I. INTRODUCTION

THE phased-array RADAR systems have been widely used in commercial and defense applications for a long time. A transmit/receive (T/R) module, which enables fast beam scanning and electronic beam control, is a crucial part of the modern phased-array RADAR systems because of its decisive effects on the system performance. The modern phased-array RADAR systems consist of several thousands of T/R modules, therefore; manufacturing costs, size, and integrability are important specifications for a T/R module. Recent advances and continued progress in the SiGe HBT BiCMOS technology have made it possible to build low-cost and fully-integrated compact size T/R modules with a competitive, sometimes even better, radio frequency (RF) performance compared to III-V counterparts [1]–[4].

The overall gain behavior of a T/R module has a tendency of deterioration as the operating frequency increases, and this results a negative slope which decreases analog-to-digital conversion resolution and 3-dB bandwidth of the T/R module, and it also contributes to pulse amplitude measurement error of the RADAR [5]. A gain-equalizer with a positive slope is able to compensate these issues as well as it enables fine-tuning of unwanted gain deterioration due to the process variations. A block diagram of a T/R module core-chip that includes a gain-equalizer is presented in Fig. 1.

Recently, there have been many published gain-equalizer studies that offer solutions for different problems. Gain equal-

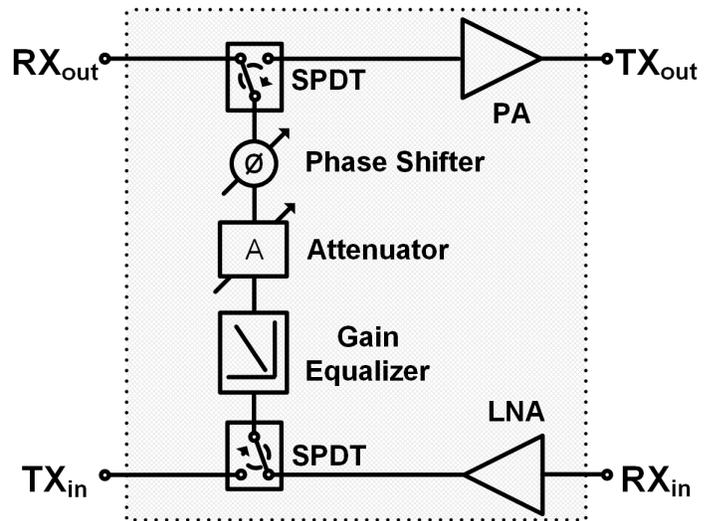


Fig. 1. Simplified block diagram of a typical T/R module core chip

izers are used in order to handle the inter-symbol interference (ISI) problems, the degradation of receiver eye-opening, timing jitter, and voltage margin problems in high-speed data transmission systems. While in [6], hybrid gain equalizer achieved up to 22 Gb/s data transmission speed successfully with low power consumption, in [7], passive gain equalizer played a key role in achieving up to 8 Gb/s with 1024 I/O lines. In order to handle the amplitude behavior of the systems, [8] offers a solution to flatten the output gain of travelling wave tube amplifiers. In [9], [10], an active gain equalizer is employed to obtain variable tunability and flatten the gain behavior of the systems. However, since these designs offer off-chip solutions, they cannot be used in the phased array applications. In [11], the tunable gain equalizer solution with tee network is offered with a good slope compensation. In this work, since the circuit is realized in III-V technology, high-cost implementation limits the usage of this circuit in modern phased array applications. In [12], amplitude equalization is applied with RF-MEMS switches which costs larger area and manufacturing unreliability due to the mechanical effects of RF-MEMS structure. In summary, there are no studies that handle the aforementioned problems such as analog-to-digital conversion resolution and pulse amplitude measurement errors in the phased-array RADAR applications.

In this paper, we present a compact-size tunable gain-equalizer implemented in IHPs  $0.25\mu\text{m}$  SiGe BiCMOS tech-

Authors are with the Faculty of Engineering and Natural Sciences, Sabanci University, Istanbul, Turkey. e-mail: yasar@sabanciuniv.edu  
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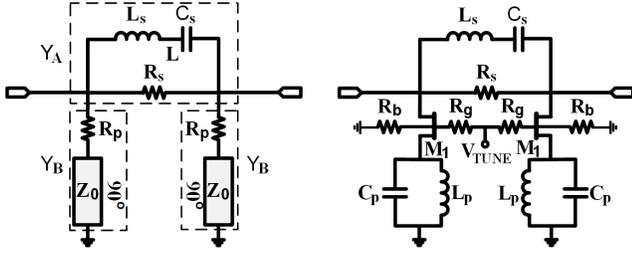


Fig. 2. (a) Conventional gain-equalizer topology. (b) Proposed compact-size tunable gain-equalizer topology.

nology, SG25H3, for X-band phased array RADAR applications. An isolated NMOS (iNMOS) created by a deep n-well was used for the first time as a variable resistor to have a tunable slope across the interested frequency range. Moreover, the resistive body-floating technique was applied to enhance the power-handling capability of the MOS-based variable resistance. To authors best knowledge this study is the first tunable gain-equalizer which handles the problems due to the negative slope nature tendency of a T/R module.

This paper is organized as follows. Section II describes the proposed gain-equalizer circuitry. Section III shows the simulations and measurement results of the design, and conclusions are given in Section IV.

## II. CIRCUIT DESCRIPTION

The conventional gain-equalizer topology consists of series and shunt resistances, quarter-wave transmission lines, and series LC-resonator is shown in Fig. 2(a), and this topology can be considered as a pi-network attenuator. The resistance-based pi-network attenuator provides a constant attenuation in an ideal case. However, the modified pi-network attenuator with frequency dependent structures can be utilized to obtain the desired slope over the desired frequency range.

The input impedance of a short-circuited quarter-wave transmission line and a parallel LC-resonator can be expressed as (1) and (2), respectively. As could be seen from these equations, they have similar impedance behavior over frequency. Therefore, as presented in Fig. 2, the short-circuited quarter wave stubs in the conventional gain-equalizer topology were replaced by the parallel LC-resonators,  $C_p$  and  $L_p$ , to significantly reduce the chip area.

$$Z(f) = jZ_0 \tan\left(\frac{\pi f}{2f_0}\right) \quad (1)$$

$$Z(f) = j \frac{1}{2\pi C} \frac{f}{f_0^2 - f^2} \quad (2)$$

The calculated admittances of the proposed compact-size tunable gain-equalizer topology are presented in (3) and (4). The Y-parameters of the conventional topology can be expressed as (5), and the S-parameters derived from the Y-parameters were presented in (6) and (7). The calculated S-parameters of the conventional topology shows that the different slopes can be obtained by changing the  $R_p$  resistor value, without deteriorating return loss behavior of the equalizer and

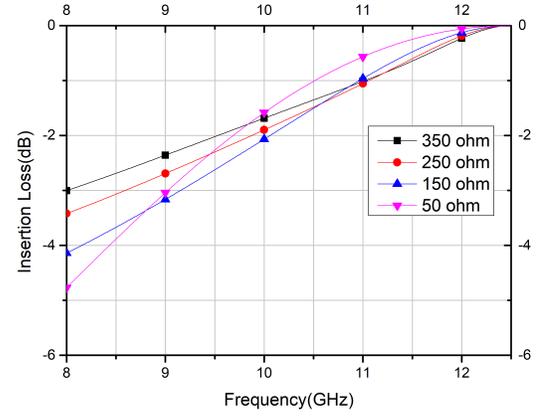


Fig. 3. Simulated insertion losses of the gain equalizer with  $R_p$  values.

changing the frequency which provides the minimum insertion loss.

$$Y_A = \frac{1 + sR_sC_s + s^2C_sL_s}{R_s(1 + s^2C_sL_s)} \quad (3)$$

$$Y_B = \frac{1 + s^2C_pL_p}{R_p(1 + s^2C_pL_p) + sL_p} \quad (4)$$

$$Y = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} Y_A + Y_B & -Y_A \\ -Y_A & Y_A + Y_B \end{bmatrix} \quad (5)$$

$$S_{11} = S_{22} = \frac{(1 - Y_{11}R_L)(1 + Y_{22}R_L) + Y_{12}Y_{21}R_L^2}{(1 + Y_{11}R_L)(1 + Y_{22}R_L) - Y_{12}Y_{21}R_L^2} \quad (6)$$

$$S_{12} = S_{21} = \frac{-2Y_{21}R_L}{(1 + Y_{11}R_L)(1 + Y_{22}R_L) - Y_{12}Y_{21}R_L^2} \quad (7)$$

From these equations (3) - (7), the tunability functionality can be implemented in two ways: by replacing the constant shunt resistor  $R_p$  with variable resistor and by switching different  $L_s$  and  $C_s$  values which resonates at the same frequency. The second method can be implemented by switching constant value inductors and capacitors and tunable inductors and capacitors. However, switching between various fixed values inductors and capacitors will consume more area and tunable inductors and capacitors will lead to power consumption, we focus on the first method. In Fig. 3, the effect of the first method on the tunability concept is shown. In this simulation environment, while  $C_s$  and  $L_s$  values are kept constant,  $R_p$  value is swept from  $50\Omega$  to  $350\Omega$ . This figure indicates that 2-dB tunable slope can be achieved by varying the resistor value from  $50\Omega$  to  $350\Omega$  in an ideal environment.

The tunability function was implemented by replacing the shunt resistor  $R_p$  with an NMOS based variable resistor. The formula of the on resistance of an NMOS can be expressed as (8) while  $V_{DS} \ll 2(V_{GS} - V_{TH})$ . As expressed in (8), the aspect ratio and the overdrive voltage of the NMOS are the main attributes to determine the on-state resistance of the transistor. Employing large size NMOS would lead to

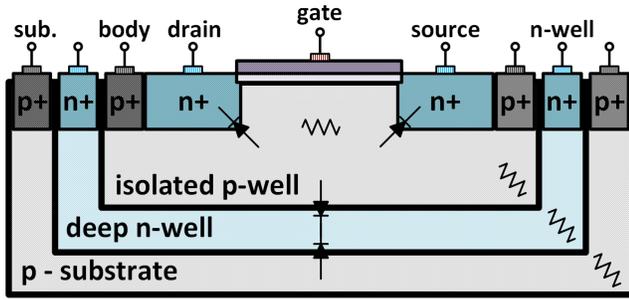


Fig. 4. Cross sectional view of the iNMOS.

lower resistance which provides more tuning range. However, a larger transistor brings larger parasitic capacitance which deteriorates the performance of the gain-equalizer. Therefore, the NMOS with the channel width of  $60 \mu\text{m}$  is selected to achieve a maximum possible tuning range. In order to obtain variable resistor behavior,  $V_{GS}$  voltages of the NMOSs are adjusted from the DC pad. As shown in (8), the resistance of the NMOS is inversely proportional to the gate voltage which implies that as the gate voltage increases the on-resistance of NMOS decreases. Subsequently, the slope of the gain equalizer increases as shown in Fig. 3.

$$R_{on} = \frac{1}{(\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}))} \quad (8)$$

In this design, for the NMOS, an isolated body, Fig. 4, created by a deep n-well and the body floating technique was used for two reasons. As illustrated in the Fig. 5, to reduce the losses due to the drain-body capacitance  $C_{db}$ , the source-body capacitance  $C_{sb}$ , and the substrate conductivity  $R_{sub}$ , a high-value resistance  $R_b$  is added, which is commonly used in RFCMOS switches [13], [14]. In this design, the body of both NMOSs are connected with  $10\text{k} \Omega$  resistance. The second reason is the power handling performance of the variable resistance was improved with the body-floating technique. As could be seen from the Fig. 6, the drain-body and source-body diodes ( $D_{db}$  and  $D_{sb}$ ) will be turned on at the negative cycle of high powers, and the linearity performance of the conventional NMOS will be degraded earlier because of the rapid increase of the current on the diodes  $D_{db}$  and  $D_{sb}$  due to small resistance of  $R_{sub}$ . However, for the iNMOS with the body-floating technique, the current on the diodes  $D_{db}$  and  $D_{sb}$  increases smoothly because of the high-value resistance  $R_b$  and back-to-back diodes  $D_{pn}$  and  $D_{np}$  which arise from deep n-well creation keep that node at the open for both cycles of the high RF input power. This second effect is also used in RFCMOS switches to improve the power handling capacity of the switches [15]–[17]. The body-floating technique also leads to an improvement in the power handling capability in this works as seen from the Fig. 7.

### III. SIMULATION AND MEASUREMENT RESULTS

The die photo of the tunable gain-equalizer is shown in Fig. 8. The effective chip area excluding the pads is  $0.21\text{mm}^2$  and the total area including pads is  $0.31\text{mm}^2$ . The S-parameter measurements were performed using Rohde & Schwarz ZVL

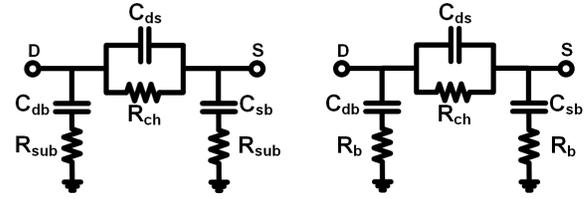


Fig. 5. Simplified small-signal equivalent circuit models of the variable resistance: (a) NMOS (b) iNMOS with body-floating.

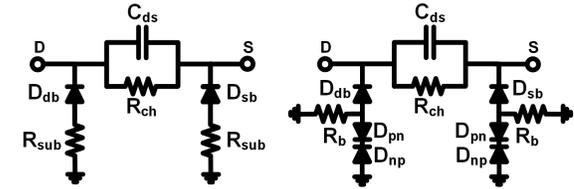


Fig. 6. Simplified equivalent circuit models of the variable resistance to investigate the power linearity: (a) NMOS (b) iNMOS with body-floating

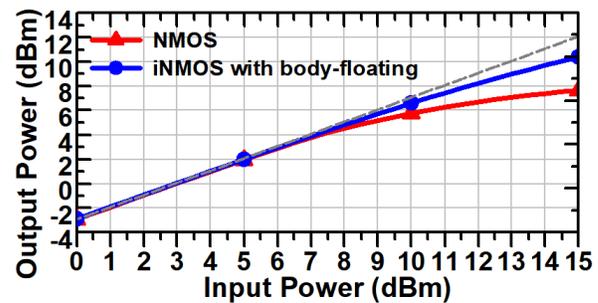


Fig. 7. Simulated on-state power linearity of the NMOS and the iNMOS with body-floating

vector network analyzer with Cascade-Microtech 40 GHz-GSG- $100\mu\text{m}$  probes. The output power of the network analyzer was set to 0 dBm, and the network analyzer was calibrated by Short-Open-Thru-Load (SOLT) method with an Impedance Standard Substrate (ISS) from Cascade-Microtech to move the reference plane to the probe tips. Fig. 9 shows the simulated and measured insertion loss results of selected points of tunable gain-equalizer. The measured insertion loss results cover between the highest slope and the lowest slope. The differences between the RF model of NMOS and the measured NMOS cause the difference between simulation and measurements. The designed tunable gain-equalizer operates in the frequency range from 8 to 12.5 GHz with a measured positive slope of about 1 dB/GHz and almost 1 dB tunable slope over the frequency range from 8 to 12 GHz. The measured minimum insertion loss is 2.2 dB. The measured phase response of the gain equalizer is shown in Fig. 10. Since the gain equalizer will be configured for the slope of any value (between the highest and the lowest value of slope), the phase response difference will only change the reference phase state of the system. The simulated and measured return losses of the tunable-gain equalizer are shown in Fig. 11. The return losses are better than 10 dB across X-band.

The linearity of the tunable equalizer was evaluated by the single-tone test. A 10 GHz sinusoidal input signal is

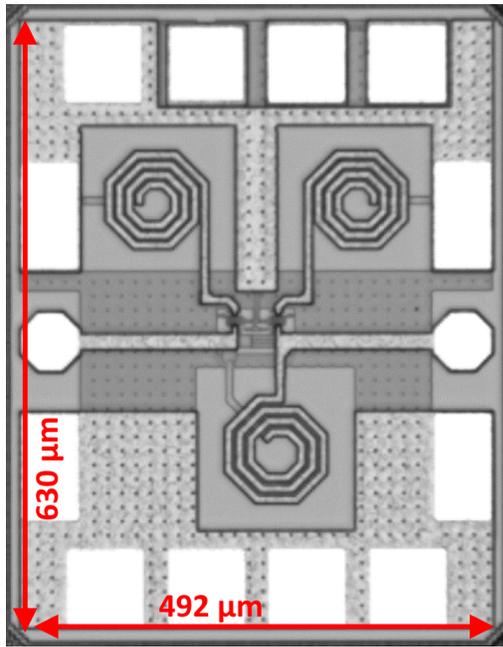


Fig. 8. Chip micro-photograph of the designed tunable gain-equalizer

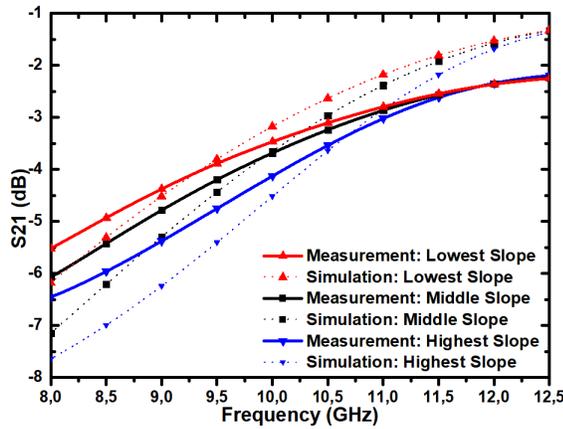


Fig. 9. Simulated and measured  $S_{21}$  results of the gain-equalizer

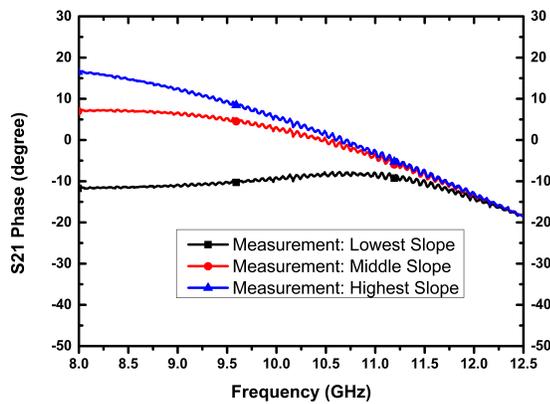


Fig. 10. Measured  $S_{21}$  phase result of the gain-equalizer

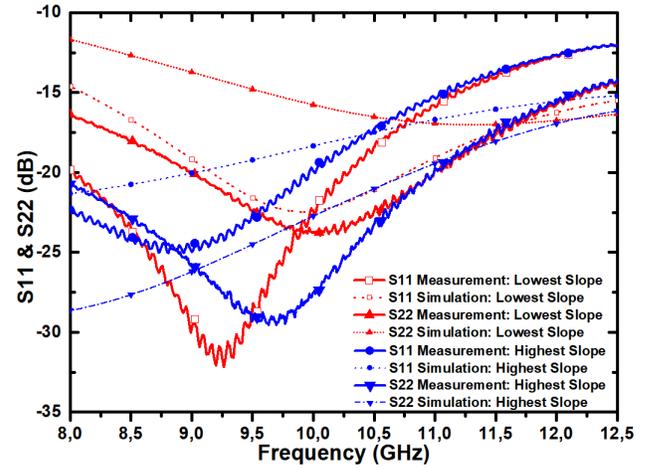


Fig. 11. Simulated and measured return losses of the gain-equalizer

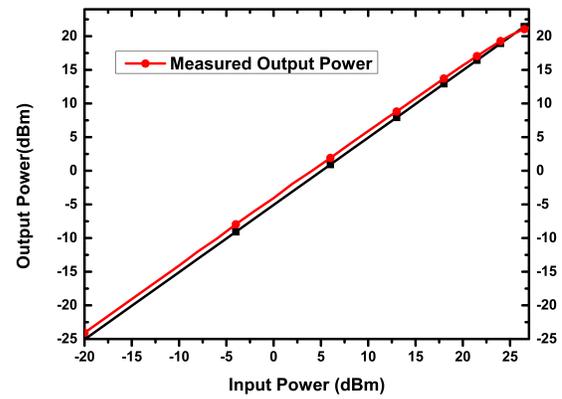


Fig. 12. Measured OP1dB of the gain-equalizer

applied at different power levels by Agilent PSG-E8257D signal generator and the output power is measured by Agilent E4417A power meter configured with E9325A power sensor. The IP1dB point is measured as 24.5 dBm. The linearity measurement is shown in Fig. 12.

The comparison of the proposed structure and other designs in the literature is presented in Table I. The figure of merit (FoM) as given in the following equations:

$$K = BW(\text{GHz}) \cdot (\text{Max.slope} - \text{Min.slope})(\text{dB}/\text{GHz}) \quad (9)$$

$$FoM = \frac{\text{abs}(\text{AverageIL}) \cdot 1\text{mm}^2 \cdot \text{abs}(K)}{\text{Area}[\text{mm}^2]} \quad (10)$$

is used to evaluate the performance of the designed tunable gain equalizer. Although [9] has a high tunability range, it consumes high power which makes this design impractical for phased array applications. In [10], high tunability range with gain is achieved. However, due to the large value of the passive components, this design cannot be realized on-chip applications. Since the proposed compact-sized work is realized in SiGe BiCMOS technology with a tunability

TABLE I  
COMPARISON TABLE BETWEEN REFERENCES AND THE PROPOSED GAIN EQUALIZER

Ref.	Tech.	Freq. [GHz]	Frac. BW[%]	Gain Slope (dB/GHz)	Tunability Range (dB)	Size	Gain dB	Power diss. [mW]	FoM
[8]	SIW Resonator	13-13.5	3.77	NA	0	19 x 9.8 x 1.76 mm <sup>3</sup>	-0.83	0	-
[9]	PIN Diode	3 - 5	50	4	16	NA	-2	150	-
[10]	350 nm SiGe HBT	0.1-1	163	18	29	16 x 16 x 1.2 mm <sup>3</sup>	10	NA	0.12
[11]	GaAs	0-18	200	0.67	14	1.1 x 1.8 mm <sup>2</sup>	-2.7	0	2.01
<b>This Work</b>	<b>250 nm SiGe</b>	<b>8-12.5</b>	<b>43.9</b>	<b>1</b>	<b>1</b>	<b>0.31 mm<sup>2</sup></b>	<b>-2.2</b>	<b>0</b>	<b>2.85</b>

attribute, low insertion loss, this work can be realized in phased array RADAR systems to compensate negative slope behavior.

#### IV. CONCLUSION

The design, implementation and measurement results of a compact-size tunable gain-equalizer for X-band phased-array RADAR applications were presented. The tunability was performed by an NMOS based variable resistor. An iNMOS was used to reduce the losses which arise from the substrate conductivity, and the resistive body-floating technique was applied to enhance the power-handling capability. The designed tunable gain-equalizer operates in the frequency range from 8 to 12.5 GHz with a positive slope of about 1 dB/GHz and almost 1 dB tunable slope. To the authors best knowledge, the proposed tunable gain-equalizer is the first work that utilizes an iNMOS based variable resistor to obtain the desired slope characteristic.

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