

A 7-Bit Reverse-Saturated SiGe HBT Discrete Gain Step Attenuator

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Abstract—In this study, the analysis, design and measured results of a fully integrated 7-bit step attenuator implemented in a 0.25- μm Silicon-Germanium (SiGe) BiCMOS process technology, are described. The attenuator is designed based on delicately ordered and cascaded Π /T type attenuation blocks, which are comprised of series/shunt switches employing SiGe hetero-junction bipolar transistors (HBTs) with peak f_T/f_{max} of 110/180 GHz. HBTs are employed as a series switch to decrease the insertion-loss of the attenuator. Moreover, to authors' best knowledge, this is the first study presenting the effect of employing reverse-saturated HBTs as a shunt switch for each attenuation blocks. Thanks to this advancement, the highest input-referred 1-dB compression point (IP_{1dB}) is reported for Si-based similar studies. This method also decreases the insertion-loss of the proposed attenuator. The measurements result in the state-of-the-art performance with 28.575 dB attenuation range by 0.225 dB gain steps while maintaining 7-bit amplitude resolution across 6.6 GHz to 12.8 GHz frequency band, where RMS phase error remains below 3.3° and insertion loss (IL) is less than 12.4 dB. The measured IP_{1dB} of the attenuator is 13.5 dBm while drawing 8 mA from 3.3 V supply. The die occupies an area of 1.37 mm x 0.56 mm excluding pads.

Index Terms—BiCMOS integrated circuits, Phased arrays

I. INTRODUCTION

THE applications of the modern phased-array RADAR systems have emerged in commercial and defense applications for a long time. In these systems, transmit/receive (T/R) modules play a crucial role due to the fast beam scanning and electronic beam control ability of these modules. Since the number of T/R modules is high, manufacturing costs, size, and integrability are important specifications for these modules. In SiGe HBT technology, thanks to the recent advances and progress in the SiGe technology, low-cost, fully-integrated compact size T/R modules with a competitive, sometimes even better, radio frequency(RF) performance compared to III-V counterparts have been published, recently [1]–[4].

Amplitude control blocks such as voltage controlled attenuators and variable gain amplifiers (VGAs) have been widely employed in T/R modules to provide high directivity, low sidelobe levels, high precision beam tailoring/steering ability, better null points, and accurate beam scanning/tracking response [5], [6]. Attenuators are preferable to VGAs in terms of their higher linearity, wider bandwidth, lesser temperature dependency, lower control complexity and easy compensation of phase imbalance [6]. There are two types of mostly used attenuator topologies: continuous/analog and digital/step [7].

Since the step attenuators remove the requirement for a digital-to-analog converter in the control path, they are preferred over analog designs [8].

In the present study, for the first time in the literature, a 7-bit phase corrected discrete gain step attenuator built with cascaded Π /T-type controllable resistive networks consisting of RS SiGe HBT switches, has been reported.

This paper is organized as follows. Section II describes the proposed attenuator circuitry. Section III shows the simulations and measurement results of the design. In Section IV, performance benchmarking of the attenuator with respect to the state-of-the-art attenuators is presented and conclusions are given in Section V.

II. CIRCUIT DESCRIPTION

A. Circuit Topology

The proposed attenuator is comprised of eight cascaded T-type and Π -type attenuation blocks with RS SiGe HBT shunt switches, of which schematic diagrams are shown in Fig. 2. To compensate for phase differences inserted while transiting between the reference and attenuation states, the R-L-R networks are placed as shown in Fig. 2, which act as low pass filters [5]. Fig. 1 shows a detailed schematic of the presented attenuator. The bit order is customized to achieve minimal sourcing and loading interaction between the individual attenuation blocks. Consequently, attenuation units with 14.4 and 7.2 dB relative attenuations are placed to the front and back end of the cascaded structure, where other 0.225 dB, 0.45 dB, 0.9 dB, 3.6 dB and 1.8 dB attenuating units are located in-between them, respectively. Since to restrain undesired transformation in source-load impedances and phase variation is more difficult when 14.4 dB attenuation is achieved with a single Π -type network, in this design, the 7th bit is constructed with a couple of concurrently switched 7.2 dB attenuation blocks. In this circuit, while C_1 and L_1 are used for input-matching, C_2 and L_2 are used for output-matching.

B. Comparison of FET and HBT switches as a Series Switch

The Π - and T-type attenuation units are substantially dependent on the parasitic elements induced by the switching devices concerning their relative attenuation range, flatness, bandwidth, phase variation, IL and P1dB [6]. Principally, $R_{on} \times C_{off}$ product, preferred to be as low as possible, is an accustomed metric to evaluate switching performance of the transistors. The capacitor models for off-stated HBT and FET are shown in Fig. 4. To make a choice among HBT and FET available in the process library as a series switch, their C_{off} values are compared to each other with

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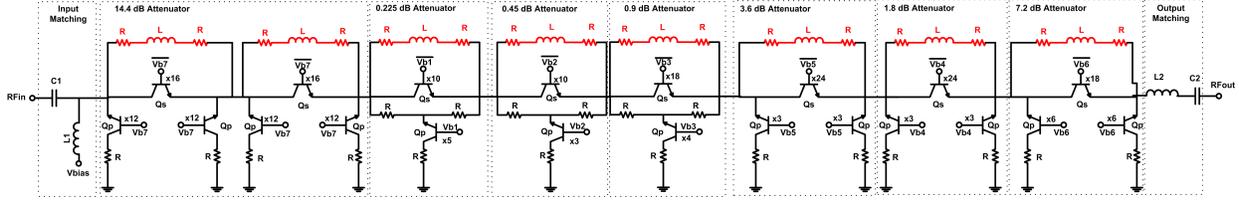


Fig. 1. Schematic of the proposed attenuator with phase correction.

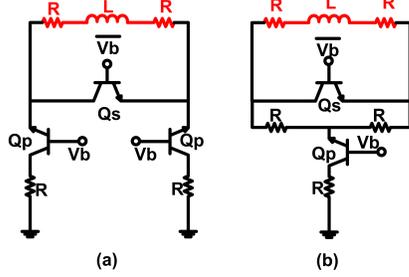


Fig. 2. The schematics of the used (a) Pi-type and (b) T-type attenuation blocks.

a simulation at 10 GHz, where HBT and FET are sized with the total emitter length of $10.92 \mu\text{m}$ and the width of $79 \mu\text{m}$, respectively, to demonstrate the same R_{on} of 10Ω . As a result, the HBT and FET have shown $C_{off,HBT}$ of 16.3 fF and $C_{off,FET}$ of 46.4 fF, which reveals that HBTs remarkably outperform FETs as a series switch. Since our work has a high number of transistors brought by eight cascaded Pi- and T-type networks, its performance might have significantly degraded due to parasitic effects of FETs; thereby, although FETs do not consume static power HBTs are employed, where a low DC power dissipation is not a primary design specification.

C. Comparison of the attenuation level of T-type and Pi-type networks

In order to decide the appropriate attenuation network type with respect to the attenuation level, the detailed analysis of the T/Pi-type networks are performed. In Fig. 3, the model of the both networks in the reference mode and the attenuation mode are shown. As a calculation method, Y-parameters are selected for T/Pi-type attenuation networks. Then, the conversion from Y-parameters to S-parameters are performed. Finally, the difference between S_{21} parameters in both the reference mode and in the attenuation mode is found as the attenuation level.

The calculated admittances of the Pi-type attenuator network in both modes of operation(the reference mode and the attenuation mode) are shown in (1)-(2). The Y-parameters of the Pi-type attenuator network in the reference mode and in the attenuation mode can be expressed as (3) and (4), respectively.

$$Y_{A1(B1)} = \frac{(2R_4 + sL_2)(1 + sR_{on(off)}C_{on(off)}) + R_{on(off)}}{(2R_4 + sL_2)R_{on(off)}} \quad (1)$$

$$Y_{A2(B2)} = Y_{A3(B3)} = \frac{1 + sR_{off(on)}C_{off(on)}}{R_{off(on)} + R_5 + sR_5R_{off(on)}C_{off(on)}} \quad (2)$$

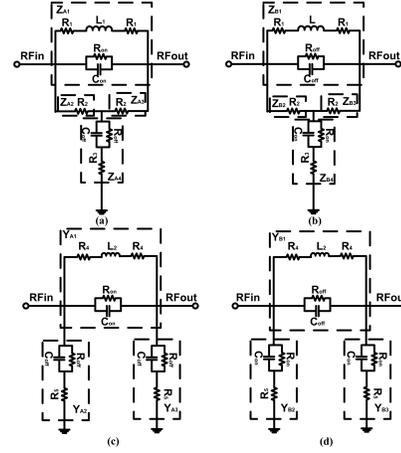


Fig. 3. The schematics of the used (a) T-type attenuation block in the reference mode (b) T-type attenuation block in the attenuation mode (c) Pi-type attenuation block in the reference mode and (d) Pi-type attenuation block in the attenuation mode.

$$Y_{on} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} Y_{A1} + Y_{A2} & -Y_{A1} \\ -Y_{A1} & Y_{A1} + Y_{A2} \end{bmatrix} \quad (3)$$

$$Y_{off} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} Y_{B1} + Y_{B2} & -Y_{B1} \\ -Y_{B1} & Y_{B1} + Y_{B2} \end{bmatrix} \quad (4)$$

The calculated impedances of the T-type attenuator network in both mode of operation(reference mode and attenuation mode) are shown in (5)-(7). The Y-parameters of the T-type attenuator network in the reference mode and in the attenuation mode can be expressed as (9) and (11), respectively. The S-parameters derived from Y-parameters are presented in (12 and 13. Since we calculate Y-parameters of both Pi and T-type attenuation networks, this formula can be applied for both case. The attenuation level can be obtained from the difference between S_{21} parameter difference between the reference mode and the attenuation mode. The formula of the attenuation level Pi and T-type attenuator networks can be expressed in 14.

$$Z_{A1(B1)} = \frac{(2R_1 + sL_1)R_{on(off)}}{(2R_1 + sL_1)(1 + sR_{on(off)}C_{on(off)}) + R_{on(off)}} \quad (5)$$

$$Z_{A2(B2)} = Z_{A3(B3)} = R_2 \quad (6)$$

$$Z_{A4(B4)} = \frac{R_{off(on)} + R_3 + sR_3R_{off(on)}C_{off(on)}}{1 + sR_{off(on)}C_{off(on)}} \quad (7)$$

$$\begin{aligned} Denominator_{on(off)} &= Z_{A2(B2)}Z_{A3(B3)} \\ &+ Z_{A2(B2)}Z_{A4(B4)} + Z_{A3(B3)}Z_{A4(B4)} \quad (8) \end{aligned}$$

$$Y_{11,on(off)} = \frac{1}{Z_{A1(B1)}} + \frac{Z_{A3(B3)} + Z_{A4(B4)}}{\text{Denominator}_{on(off)}} \quad (9)$$

$$Y_{21,on(off)} = -\frac{1}{Z_{A1(B1)}} - \frac{Z_{A4(B4)}}{\text{Denominator}_{on(off)}} \quad (10)$$

$$Y_{22,on(off)} = \frac{1}{Z_{A1(B1)}} + \frac{Z_{A2(B2)} + Z_{A4(B4)}}{\text{Denominator}_{on(off)}} \quad (11)$$

$$S_{11} = S_{22} = \frac{(1 - Y_{11}R_L)(1 + Y_{22}R_L) + Y_{12}Y_{21}R_L^2}{(1 + Y_{11}R_L)(1 + Y_{22}R_L) - Y_{12}Y_{21}R_L^2} \quad (12)$$

$$S_{12} = S_{21} = \frac{-2Y_{21}R_L}{(1 + Y_{11}R_L)(1 + Y_{22}R_L) - Y_{12}Y_{21}R_L^2} \quad (13)$$

$$\text{AttenuationLevel} = S_{21,off} - S_{21,on} \quad (14)$$

From this formula, the required attenuation level can be obtained by calculating the resistance values and the number of the transistors. During the implementation of the attenuator, when a high attenuation level is required, Π -type attenuation network is chosen since two shunt switches to the ground increases the capability of the attenuation level of the network. When a low attenuation level is required, T-type attenuation network is chosen.

D. Reverse-Saturation Method

Besides the selection of HBTs, which is necessitated by poor switching capability of FETs, additional design methodologies had to be explored to reduce the parasitic elements because the lossy silicon-based substrate induces relatively more parasitic effects and they are particularly troublesome for the deployed attenuator topology [6]. It is reported in [10] that if the shunt connected HBTs are in RS mode, IL improves because electrons have a higher potential barrier during their leakage to ground due to higher doping concentration in the emitter than the collector. Furthermore, in [11] it has been proven that parasitic capacitors to substrate can significantly exacerbate IL, operational bandwidth, attenuation range and gain flatness, while causing more abrupt phase changes during the transition between reference and attenuation modes of the Π - and T-type step attenuators. As well as the previously mentioned simulation that confirms $C_{off,HBT}$ is 65% lower than $C_{off,FET}$ for the devices having the same R_{on} , shunt parasitic capacitors of the same transistors are also investigated. Fig. 4 represents the capacitor models for the (a) FET and (b) the HBT, where D, S, C, E and B denote drain, source, collector, emitter and body, respectively. The simulation for the FET results in C_{DB} of 10.3 fF and C_{SB} of 11.98 fF, which are almost equal due to device symmetry. On the other hand, for the HBT, C_{CB} is 24.5 fF and C_{EB} is 1.9 fF. If the capacitor models are shown in Fig. 4 are substituted into Π -type attenuator, total parasitic shunt capacitance values on the signal path are shown on TABLE I. These values demonstrate that compared to NMOS, HBT Π -attenuator leads a lower total shunt parasitic capacitor added to the signal path. Moreover, when the Q_p devices are routed in RS configuration, since the emitter has a

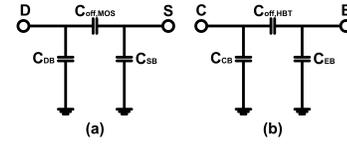


Fig. 4. Capacitor models for off-stated (a) HBT and (b) FET.

considerably smaller (1.9 fF) shunt capacitor than the collector (24.5 fF) due to its better physical isolation from the substrate [10], RS HBT configuration leads a much lower total shunt capacitor on the signal path. Furthermore, it is verified in [12] that, RS method boosts the power handling capability of the HBTs due to the higher doping concentration of the emitter and graded doping profile of the base of the HBTs. The reason behind this behavior, the junction between base and emitter at high RF power creates a lower loss path toward the ground than the junction between base and collector. This lower loss path will lead to further diminishing of the RF power in the conventional HBT switch topology. Consequently, the analysis reveals that employing HBTs instead of FETs and configuring them in RS mode are enabling approaches to realize the proposed 7-bit attenuator operating with the state-of-the-art amplitude resolution across the specified attenuation range along with its' lower phase error, acceptable source-load return losses. Furthermore, IP_{1dB} , is the highest ever reported, in the literature.

TABLE I
TOTAL PARASITIC SHUNT CAPACITANCES ON THE SIGNAL PATH

	Operating Mode	
	Reference	Attenuation
NMOS	137.4 fF ($3*C_{DB} + C_{SB} + 2*C_{off,NMOS}$)	44.6 fF ($3*C_{DB} + C_{SB}$)
HBT	108 fF ($3*C_{CB} + C_{EB} + 2*C_{off,HBT}$)	75.4 fF ($3*C_{CB} + C_{EB}$)
RS HBT	62.8 fF ($3*C_{EB} + C_{CB} + 2*C_{off,HBT}$)	30.2 fF ($3*C_{EB} + C_{CB}$)

III. SIMULATION AND MEASUREMENT RESULTS

The die photo of the attenuator is shown in Fig. 5. The die occupies an area of 0.71mm². The S-parameters were measured using Agilent 20 GHz 8720ES network analyzer while the bias voltages were applied with Agilent E3631A triple output DC power supplies. To control an attenuation unit, only one bias voltage was applied because each of them has its own inverter to inversely bias series and shunt devices. A couple of 150 μ m pitch-sized GSG probes were used on the QFB packaged and wire-bonded die while measuring S-parameters. The output power of the network analyzer was set to 0 dBm, and the network analyzer was calibrated by Short-Open-Thru-Load (SOLT) method with an Impedance Standard Substrate (ISS) from Cascade-Microtech to move the reference plane to the probe tips. Fig. 6 shows that the measured input (a) and output (b) RLs are above 13 dB from 6.6 to 12.8 GHz, while IL (c) varies from 8.9 to 12.4 dB. Furthermore, Fig. 6 (d) illustrates the inserted phase which differs from -12° to 8°. The measured discrete gain steps are represented in Fig.

7, where the coverage of 28.575 dB attenuation range with the gain increments of 0.225 dB is evident. The RMS phase and RMS amplitude errors of the attenuator are shown in Fig. 8. These results present that the 7-bit amplitude resolution of the proposed attenuator with a less than 3.3° RMS phase error from 6.6 to 12.8 GHz.

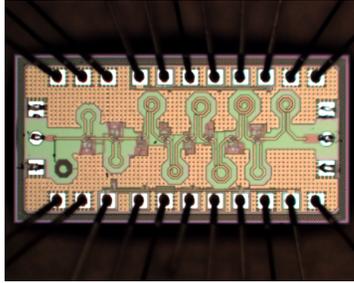


Fig. 5. Chip micro-photograph of the designed attenuator

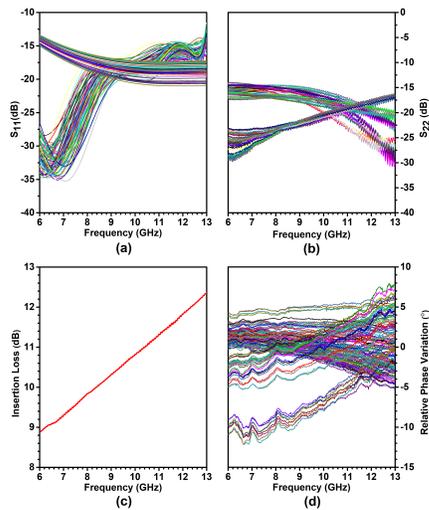


Fig. 6. (a) S_{11} , (b) S_{22} , (c)IL, and (d)relative phase variation of the attenuator

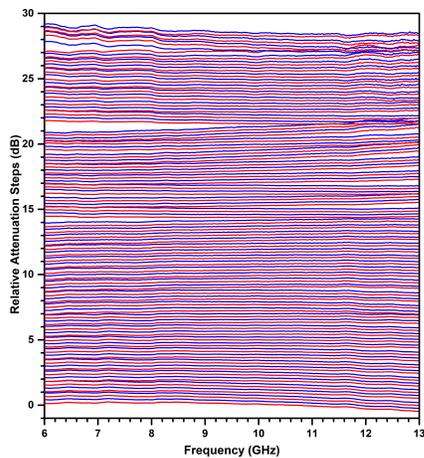


Fig. 7. The measured relative attenuation steps of the attenuator

The linearity of the attenuator was evaluated by the single-tone test. A sinusoidal input signal is applied at different

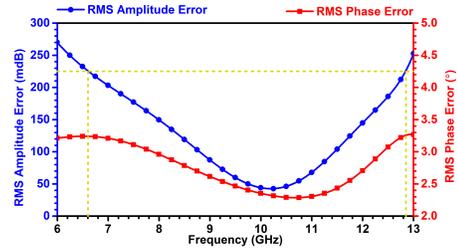


Fig. 8. The measured RMS amplitude and RMS phase error of the attenuator

power levels by Agilent PSG-E8257D signal generator and the output power is measured by Agilent E4417A power meter configured with E9325A power sensor. In the reference mode, at the center frequency(10GHz) the attenuator exhibits an IP_{1dB} of 13.5 dBm while drawing 8 mA from 3.3 V power supply. The IP_{1dB} of the attenuator varies from 12.5 dBm to 14 dBm over the 6.6 GHz to 12.8 GHz and the linearity measurement at the 10 GHz is shown in Fig. 9.

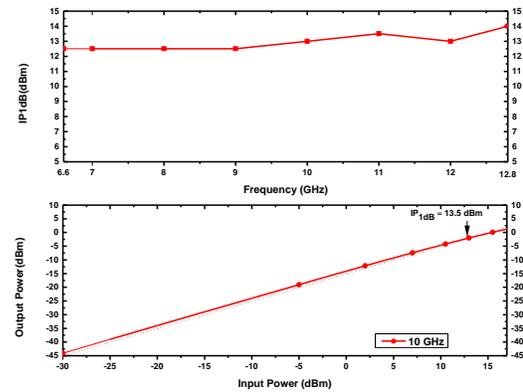


Fig. 9. Top: Measured IP_{1dB} of the attenuator over frequencies Bottom: Measured IP_{1dB} of the attenuator at 10 GHz

The two tone measurement was performed to evaluate the input third-order intercept point (IIP3). The spacing of the two tones is selected as 10 MHz. As shown in Fig. 10, 29 dBm IP_3 value is measured.

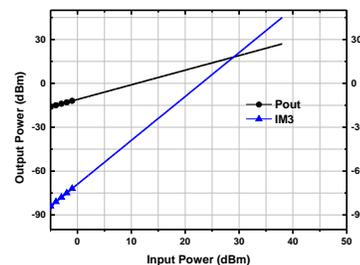


Fig. 10. Measured two-tone intermodulation ($f_1 = 9.995$ GHz, $f_2 = 10.005$ GHz) response at 10 GHz versus input power

TABLE II
PERFORMANCE SUMMARY OF THE IMPLEMENTED 7-BIT SiGe HBT ATTENUATOR AND PREVIOUSLY REPORTED ATTENUATORS

Ref.	BW (GHz)	Process Tech.	Att. Range (dB)	Eff. # of Bits	LSB (dB)	IL (dB)	RL (dB)	IP1dB (dBm)	RMS Amp. Err. (dB)	RMS Phase Err. (°)	Die Area (mm ²)	P _{DC} (mW)	IIP3 (dBm)
[5]	8-12	0.18 μm CMOS	31.5	6	0.5	<11.3	>11	13	<0.4	<2.2	0.52	0	28
[8]	10-50	0.12 μm BiCMOS	11	4	0.9	2-3	>8	5	N/A	<3	0.15*	0	-
[9]	10-67	0.18 μm BiCMOS	32-43	4	3	<15.2	>8.7	13	N/A	N/A	0.77	0	-
[11]	7.7-10.8	0.25 μm SiGe BiCMOS	16.51	7	0.13	<12	>15	12.5	<0.13	2.3 - 3.1	0.29*	0	-
[13]	0-20	0.13 μm SiGe BiCMOS	31.5	6	0.5	<7.2	>12	10	<0.37	<4	0.98	0	25
This Work	6.6-12.8	0.25 μm SiGe BiCMOS	28.4	7	0.225	<12.4	>13	13.5	<0.225	2.3 - 3.3	0.71*	26.4	29

* Excluding Pads.

IV. PERFORMANCE BENCHMARKING

TABLE II represents the performance summary of our attenuator and the similar studies reported in the literature. The attenuators described in [5], [8], [9], and [13] have less bit resolution than our attenuator and exploit the benefits of using smaller technology nodes featuring devices with lower R_{on} and parasitic capacitors, which provide a significant advantage in performance as mentioned earlier. Moreover, [8] and [9] both suffer in terms of RLs and [8] has only 11 dB of attenuation range with a low IP_{1dB} of 5 dBm. [11] mainly differs from the presented attenuator by employing FETs to switch attenuation units. Nevertheless the isolated NMOS devices are used in [11] to prevent performance degradations due to C_{off} , FET, C_{DB} and C_{SB} , in our design, RS HBTs enable 7-bit amplitude resolution in a much wider frequency band and attenuation range along with a higher IP_{1dB} , while keeping IL and RMS phase errors almost the same at a cost of 26.4 mW DC power dissipation.

V. CONCLUSION

A 7-bit discrete gain step attenuator, fabricated on 0.25 μm SiGe BiCMOS process technology, has been presented. Additionally, this study is the first attenuator that incorporates RS HBTs to switch Pi- and T-type attenuation networks. The developed attenuator exhibits state-of-the-art performance with its 13.5 dBm IP_{1dB} and 7-bit amplitude resolution in 28.575 dB attenuation range with an RMS phase error of below 3.3° across 6.6 to 12.8 GHz frequency range, which substantiate this work to be considered as a strong candidate for gain control in transceiver chains of phased array radars.

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