SiGe BiCMOS Active Phase Shifter Design for W-band Automotive Radar Applications

by

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for W-band Automotive Radar Applications

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Abstract

In this thesis, the design and measurement results of the fabricated LNA and phase shifter chips to be utilized in W-band Automotive Radar Applications are presented. The chips are manufactured using 0.13μm and 0.25μm SiGe HBT technologies. Observing the high insertion loss of the fabricated 4-bit MEMS based digital phase shifter which is around 15.3-18.1dB, two active phase shifter designs based on different vector-modulator topologies are offered. Amongst these structures, three-way active phase shifter is composed of Wilkinson power divider/combiner which separates the input signal into three vectors, additional phase lines dividing the 360^o phase spectrum into three regions by adding 120^o consecutive phase to each vector and LNAs to rotate the main antenna beam in these regions by the weighted sum of vectors. According to measurement results of the 100mW consuming 1.65mm^2-sized chip, continuous 360^o phase shifting is clearly achieved with 11dB peak gain at 77GHz, no insertion loss up to 90GHz and return losses better than 10dB for all the phase states. On the other hand, a two way I/Q type MEMS based active phase shifter is also in fabrication. The continuous phase shifting is realized in I- and Q-separated two amplification stages, using weighted sum method, to rotate in a single 90^o quadrant and then employs 1-bit (0^o-180^o) MEMS phase shifter blocks to cover 360^o in 4 states by shifting this quadrant about 90^o. The simulation results of 3.74mm^2 chip point out above-15dB input/output return loss and a variable 3-7.5dB gain at 77GHz with the tuned LNA voltages. Using these active phase shifters, phased array radars could provide higher gain in a smaller die area with reduced cost due to the used SiGe technology and automotive radars with high perfromances could be achieved.

W-band Otomotiv Radar Uygulamaları için

SiGe BiCMOS Aktif Faz Kaydırıcı Tasarımı

Efe Öztürk

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Özet

Bu tezde, W-band otomotiv radar uygulamalarında kullanılmak üzere üretilen LNA ve faz kaydırıcı yongaların tasarım ve ölçüm sonuçlarına yer verilmektedir. Yongalar, 0.13μm and 0.25μm SiGe HBT teknolojileri kullanılarak üretilmiştir. Üretilen MEMS bazlı 4-bit dijital faz kaydırıcının, 15.3-18.1dB arasında seyreden yüksek iletim kaybını gözlemledikten sonra, vektör modülasyonu topolojisi kullanan iki adet aktif faz kaydırıcı önerilmektedir. Bu yapılar arasında üç kollu olan, giriş sinyalini üçe ayıran Wilkinson güç bölücü/toplayıcı, her hatta aralarında 120^o faz farkı olacak şekilde 360^o'lik spektrumu üç bölgeye bölen ek faz hatları ve ana anten ışınını bu bölgeler arasında ağırlıklı vektör toplama yöntemiyle döndürmeye yarayan LNA'lerden oluşmaktadır. Ölçüm sonuçlarına göre, 100mW güç harcayan 1.65mm^2 boyutundaki bu yonga, 77GHz'te 11dB maksimum kazanç ile, 90GHz'e kadar iletim kaybı olmaksızın ve bütün faz aşamaları için yansıma kayıpları 10dB'nin üstünde seyrederek, sürekli bir şekilde 360^o'lik faz kaydırmayı açıkça gerçekleştirmektedir. Diğer taraftan, iki kollu I/Q yapıda MEMS bazlı aktif faz kaydırıcı yapı da üretimdedir. Sürekli faz kaydırma işlemi, ağırlıklı vektör toplama yöntemiyle, spektrumun 90^o'lik tek çeyreğinde I ve Q olarak ayrılmış iki güçlendirme aşamasından, ve ardından, 360^o'yi 4 aşamada tamamlayacak şekilde bu çeyreği sürekli 90^o kaydıran 1-bit'lik (0^o-180^o) MEMS faz kaydırıcı bloklarından geçerek gerçekleşmektedir. Bu 3.74mm^2'lik yonganın simülasyon sonuçları, 15dB üstünde giriş/çıkış yansıma kaybına ve değişen LNA voltajları ile 77GHz'te 3-7.5dB arasında seyreden bir kazanca işaret etmektedir. Bu aktif faz kaydırıcıları kullanılarak, faz dizinli radarlardan, benimsenen SiGe teknolojisi sayesinde düşük maliyet ve daha küçük bir alanda daha fazla kazanç elde edilebilir, ve yüksek performanslı otomativ radarlar yapılabilir.

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1. Introduction

A phased array radar is composed of multiple antennas being fed by signals with varied phases which end up rotated radiation patterns to reinforce the total antenna gain in the desired direction and suppress otherwise electronically, which eliminates the mechanical beam steering and results in faster positioning, higher scan rate and multimode operation. While providing enhanced performance over the case in a single antenna system, by using this directivity, either a fixed or a continuously scanning radiation pattern could be obtained. This is illustrated in Fig. 1 which highlights the phased array topology, its elements and the scanning beam [1]. The amplitude-even received signals are shifted in phase with the help of phase shifters and, then, being amplified to increase the signal level. As a final step, the resulting signals are gathered using a power divider/combiner structure to attain the output signal to be modulated in latter stages. Thus with this architecture, distinct amount of simultaneous operations like searching, tracking, altitude finding and terrain following by using wide, narrow, flat fan shaped and pencil beams, respectively, become possible [2].

The topology is widely utilized in many applications such as weather forecasting, radio astronomy, air and surface target tracking for martial purposes and many more. A safety

related application exists in imaging applications, such as concealed weapon-detection, security screening and videos enhancement of low-visibility scenes [3]-[4]. Another security application would be to use this scanning property in automotive radars for blind side detection, crash avoidance, low speed stop-and-go, keeping safe-drive distance with the traffic, road traffic control, lane change assistance and automated parking purposes in W-band frequencies. For these purposes, 76-77GHz and 77-81GHz frequency bands were allocated for long and short range radar applications [5]-[7].

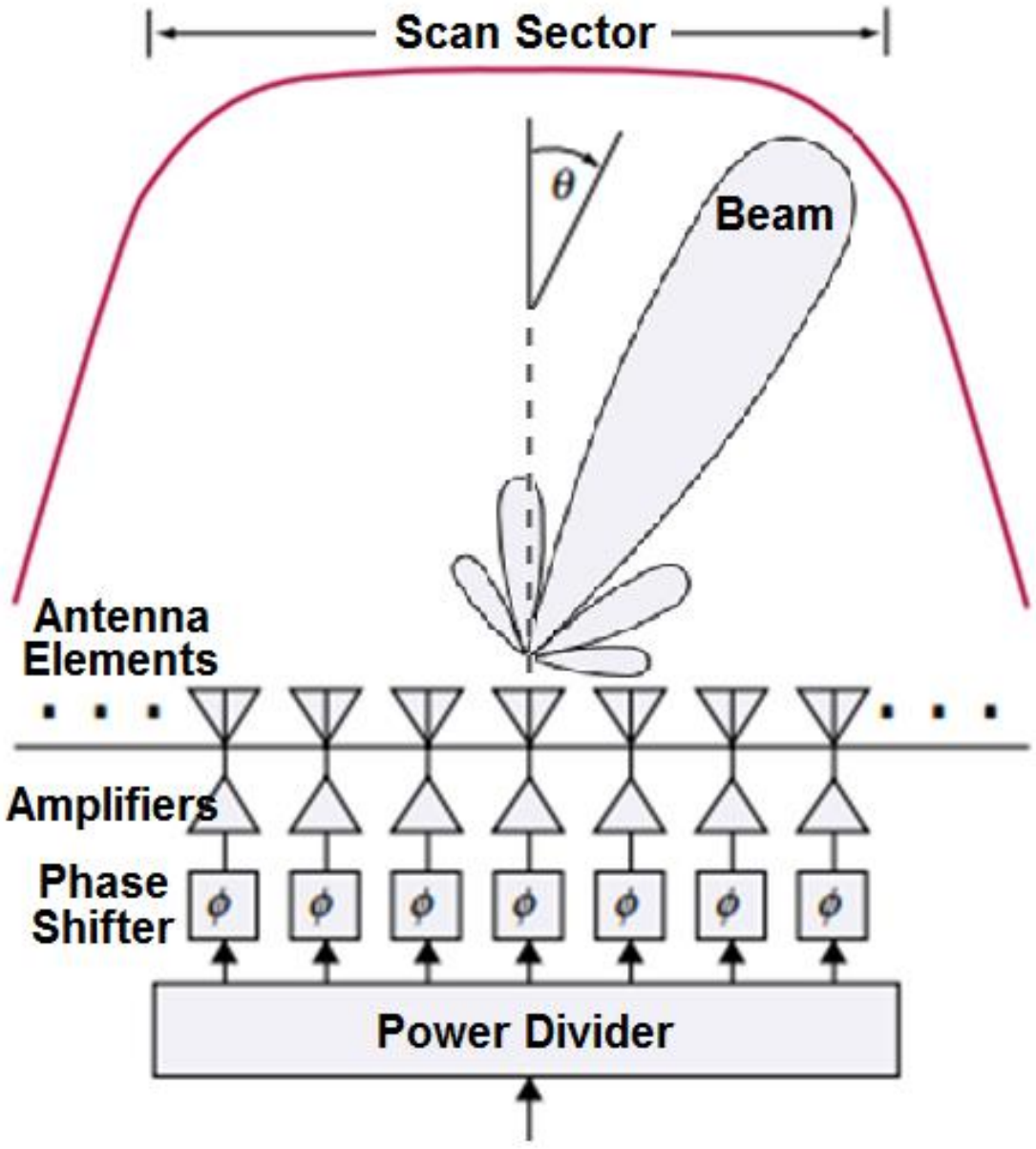

Fig. 1: Phased array antenna structure [1]

One of the critical issues at 77GHz and beyond is the low level of received signals due to both the limited power output of solid state power amplifiers and also the high free space path loss created by shorter wavelengths (around 70dB for 1-meter at 77GHz). In order to increase the received signal level at the receiver, one can use conventional antenna technologies such as high gain phased array design, better design of single element antennas and higher gain low noise amplifiers with low loss phase shifters [8]. With the logic in Fig. 1, the overall performance of the system increases proportional to the number of radiating elements. However the drastic increase in the cost as well as in the size and complexity is the major drawback. Mutual coupling and substrate losses as other disadvantages exist on the antenna part and a careful design should be realized considering wider scanning angle and beamwidth which should enable low level sidelobes and also avoid blind spots. Moreover, from the circuit part, low loss phase shifters with high bit-resolution performances for better beam steering function and very low noise amplifiers with high gain to compansate the low level signals should be provided. Considering the wide range and importance of application fields, high quality and low cost transceiver units are required.

As applications require higher operation frequencies, antenna sizes become comparable with other circuit elements, and as a result, highly integrated, single chip solutions for full T/R modules are possible by utilizing cost-effective SiGe BiCMOS technology [9]-[10]. Therefore, in this thesis, the design and fabrication of low noise amplifier and phase shifter circuits which will be built on this technology and utilized in W-band automotive phased array radars are presented.

The organization of this work is as follows. In Chapter 2, low noise amplifier basics are mentioned. In this context, firstly, some of the important figures of merit are given and the trade-offs between these are examined. Then, some commonly-used topologies are shared in the sense of a correct optimization.

Chapter 3 consists of two low noise amplifier deisgns based on the topologies stated previously. Related I-V curves, biasing conditions, inductor and matching network designs are presented with simulation setup. After the fabrication of SiGe BiCMOS chips, simulation and meausrement results are compared and will be used in active phase shifter design in Chapter 5.

Chapter 4 gives a short information about phase shifter fundamentals, some important quality defining parameters and topologies.

Considering the details in former chapter, three different phase shifter designs are introduced in Chapter 5: a MEMS based 4-bit digital phase shifter using switched-line topology, a three-way active phase shifter and a MEMS based two-way active phase shifter using different vector modulator topologies. Simulation and measurement results of each are evaluated.

Finally, the thesis is concluded with a brief summary which discusses the performances of all the chips for a complete phased array radar structure and some future works are listed.

2. Low Noise Amplifier Basics

The information in a communication system is modulated and radiated into space using a transmitting antenna, and on the receiving part, a noisy signal with reduced power is picked up. In order to use that signal for certain applications, a pre-amplification stage is often needed. In that case, Low Noise Amplifiers (LNA) compose the first front-end active stage of receivers with the purpose of enabling enough gain and introducing as low noise as possible to the system to bring the RF signal to desired levels to be processed later and lower the noise of cascaded stages. By this way, the noise of each component, as shown in Fig. 2, is reduced by the total gain of the former stages whereas the noise of very first component is directly injected to the overall noise figure:

$$F_{TOTAL} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \ldots G_{n-1}} \quad (1)$$

where F_n and G_n are noise factor and available gain of the n^{th} component. In this Friis formula, F_1 and G_1 belong to the LNA, and as seen, the noise contribution of each component is divided by G_1. Therefore in a receiver chain, it is required to have a high gain and low noise from the very first component which is LNA.

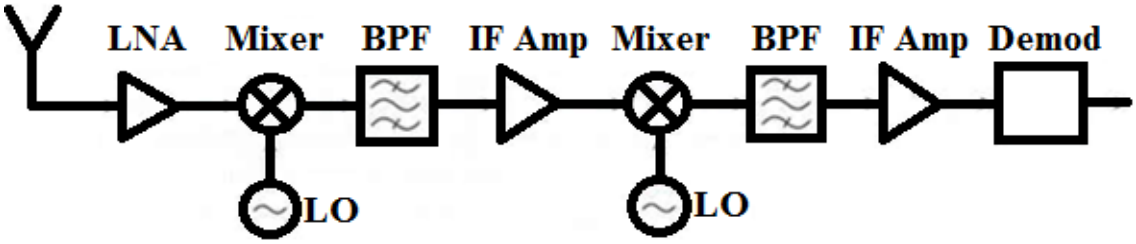

Fig. 2: Block diagram of a double-conversion superheterodyne receiver

The outline of this chapter is as follows. In Section 2.1, important parameters which determine the quality of an LNA design are introduced. Then, the most common design topologies are discussed in the context of contradicting parameters in Section 2.2.

2.1 Important LNA Parameters

The design of an LNA is managed by many parameters such as Noise Figure (NF), Gain (G), stability (K), input/output return loss (IRL/ORL), isolation, linearity (1dB compression point: P_{1dB}, third-order intercept point: IP_3), bandwidth, frequency of operation and power consumption. Each of these parameters are competing such that, for improved power transfer at input and output, minimum noise figure and maximum gain should be compromised, for example, or gain is adversely affected to increase the stability. Thus, to overcome the trade-offs, a careful design procedure should be carried out for the generic amplifier system shown in Fig. 3.

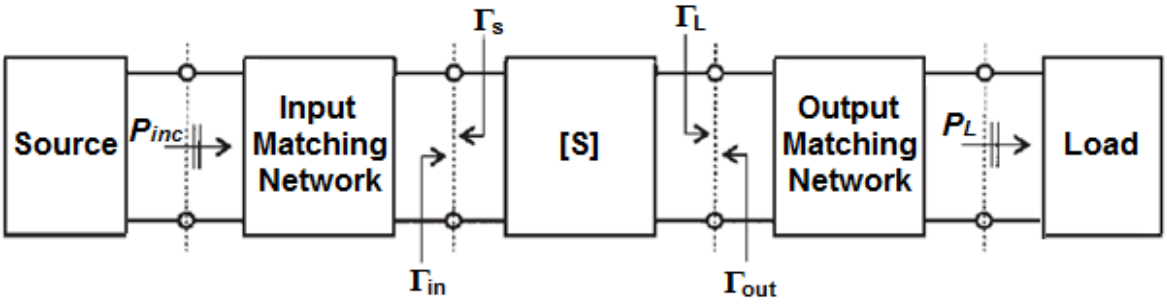

Fig. 3: A typical amplifier system with matching networks [11]

2.1.1 Noise Figure

The ratio of input SNR (Signal-to-Noise-Ratio) to output SNR defines the noise factor, F (Noise Figure, $NF = 10logF$). In other words, it emphasizes the degradation in SNR of input signal due to the circuit elements that the signal passes. When the RF signal is amplified, the noise is also amplified at the same level and may distort the main signal in a noisy network. Therefore output noise power increases greatly, which will eventually increase the noise figure:

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{S_{in}}{N_{in}}\frac{N_{out}}{S_{out}} \tag{2}$$

where S_i and N_i are the signal and noise powers respectively. As stated previously, the noise by the first component in a receiver chain directly contributes to the overall noise figure using the Friis formula for cascaded networks in Eq. 1. Thus, it is required to have a low noise amplifier providing as low N_{out} as possible.

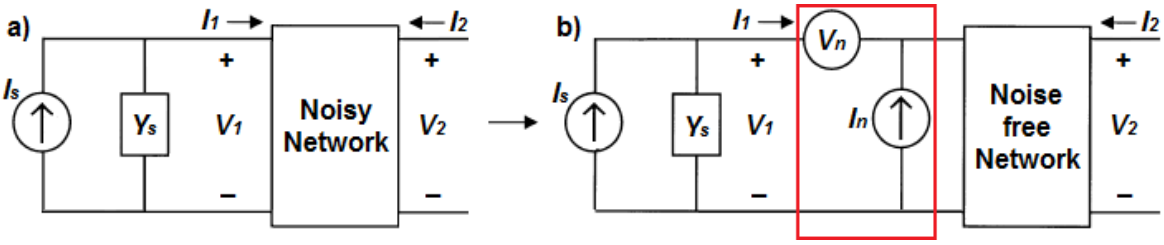

Fig. 4: A noisy two-port network and its noise-free counterpart with noise sources replaced

Considering the two-port noisy network shown in Fig. 4, the noise generated is expressed as:

$$F = F_{min} + \frac{R_n}{G_s}\left|Y_s - Y_{opt}\right|^2 \tag{3}$$

where $Y_s = G_s + jB_s$ and $Y_{opt} = G_{opt} + jB_{opt}$ are, respectively, the source admittance and optimum source admittance which results in minimum noise figure, F_{min} is the minimum achievable noise factor in the presence of $Y_s = Y_{opt}$ at the input and R_n is the equivalent noise resistance of the transistor [11].

It is essential to visualize the influence of noise on Smith Chart to better view the trade-offs between parameters such as gain, VSWR and stability. As a result of the noise figure expression in Eq. 3, noise figure circles are drawn on Smith Chart. By adjusting the source reflection coefficient Γ_s, since all other parameters are fixed for the transistor, noise figure is selected amongst the constant noise figure circles under certain bias conditions. If $\Gamma_s = \Gamma_{opt}$, the lowest possible noise factor which is $F = F_{min}$ could be attained (see Fig. 5).

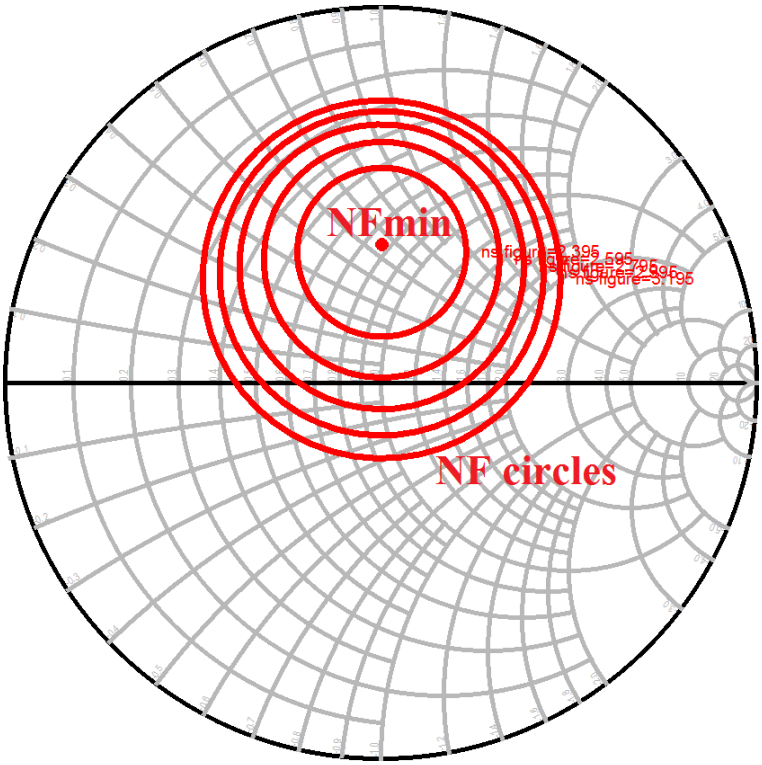

Fig. 5: Constant Noise Figure circles in the Smith Chart

2.1.2 Gain

After acquiring the noisy and low-power signal from the receiving antenna, an appropriate level of gain should be added to modulate the signal by increasing its amplitude or power. Although the definition can be referred as voltage gain, current gain or power gain in electrical circuits, gain in RF amplifiers refers to power gain which has also different definitions in itself [11].

If the input impedance Z_{in} is conjugately matched to source impedance Z_s, maximum power generated at the source can be transferred to input which is defined as the available power, P_A. Then, the gain of amplifier is defined as transducer power gain, G_T:

$$G_T = \frac{power\ delivered\ to\ the\ load}{power\ available\ from\ the\ source} = \frac{P_L}{P_A} \tag{4}$$

This equation can be expanded by utilizing the signal flow chart method to come up with the wave expressions. As a result, G_T becomes:

$$G_T = \frac{(1-|\Gamma_L|^2)|S_{21}|^2(1-|\Gamma_s|^2)}{|1-\Gamma_s\Gamma_{in}|^2|1-S_{22}\Gamma_L|^2} = \frac{(1-|\Gamma_L|^2)|S_{21}|^2(1-|\Gamma_s|^2)}{|1-\Gamma_L\Gamma_{out}|^2|1-S_{11}\Gamma_S|^2} \tag{5}$$

where input reflection coefficient is $\Gamma_{in} = S_{11} + (S_{21}S_{12}\Gamma_L)/(1-S_{22}\Gamma_L)$ and output reflection coefficient is $\Gamma_{out} = S_{22} + (S_{21}S_{12}\Gamma_S)/(1-S_{11}\Gamma_S)$.

Neglecting the reverse gain ($S_{12} = 0$), unilateral power gain, G_{TU} is found:

$$G_{TU} = \frac{(1-|\Gamma_L|^2)}{|1-S_{22}\Gamma_L|^2}\ x\ |S_{21}|^2\ x\ \frac{(1-|\Gamma_s|^2)}{|1-S_{11}\Gamma_S|^2} = G_S\ x\ G_o\ x\ G_L \tag{6}$$

The maximum unilateral power gain $G_{TU,max}$ is achieved in case of $|S_{11}|, |S_{22}| < 1$ when input and output are matched ($\Gamma_S = S_{11}^*$ and $\Gamma_L = S_{22}^*$). However this may not be suitable for all cases since it neglects the reverse gain and assumes unilateral type matching, $\Gamma_L = S_{11}^*$ and $\Gamma_L = S_{22}^*$. Therefore bilateral design is introduced which takes S_{12} into account and used to derive a more general expression through simultaneous conjugate matching.

Using the same procedure, available power gain (G_A, when output conjugately matched to load: $\Gamma_L = \Gamma_{out}^*$) and operating power gain (G_P) are extracted as:

$$G_A = \frac{power\ avaliable\ from\ the\ amplifier}{power\ available\ from\ the\ source} = \frac{|S_{21}|^2(1-|\Gamma_s|^2)}{(1-|\Gamma_{out}|^2)|1-S_{11}\Gamma_S|^2} \tag{7}$$

$$G_P = \frac{power\ delivered\ to\ the\ load}{power\ supplied\ to\ the\ amplifier} = \frac{(1-|\Gamma_L|^2)|S_{21}|^2}{(1-|\Gamma_{in}|^2)|1-S_{22}\Gamma_L|^2} \tag{8}$$

Using these gain expressions above, it is observed that $G_P, G_A \geq G_T$, unless conjugate matching condition is utilized where $G_P = G_A = G_T$ in that case.

As noise figure circles, it can be very helpful to generate a graphical depiction of gain on Smith chart to simplify the understanding of trade-offs between amplifier parameters. To do so, radius and center information for different gains should be derived from unilateral gain expression found in Eq. 6 with respect to Γ_S and Γ_L. As a result, Fig. 6 is drawn.

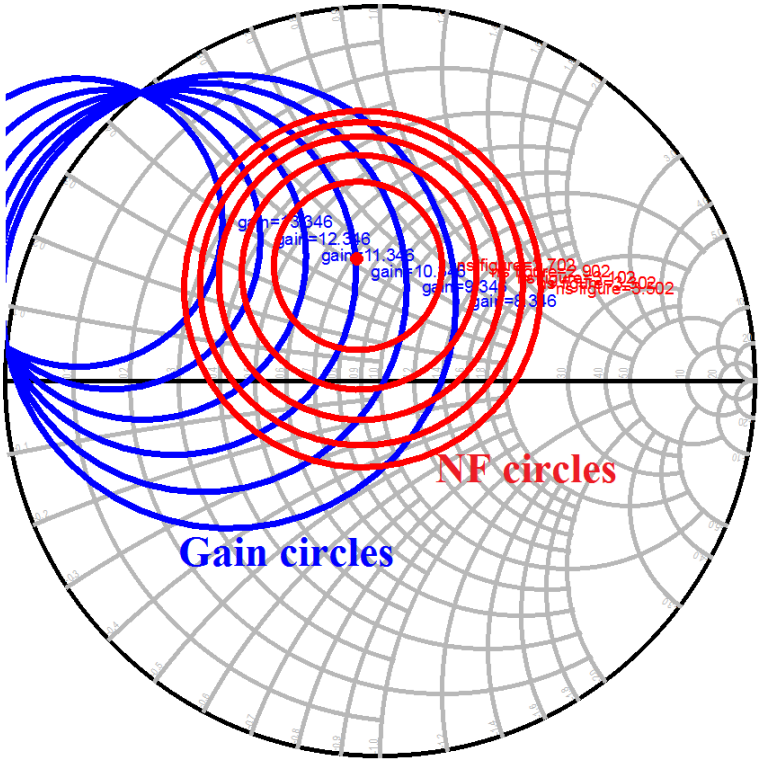

Fig. 6: Constant Gain and Noise Figure circles in the Smith Chart

2.1.3 Stability

A stable performance is one of the requirements that all amplifiers must satisfy in the operation frequency band. In case of an unstable structure, RF circuits oscillate, which means that the magnitude of reflected voltage wave will tend to increase with the added gain. In other words, below expression must hold for a stable operation.

$$|\Gamma_L|, |\Gamma_S|, |\Gamma_{in}|, |\Gamma_{out}| = V^-/V^+ < 1 \quad (9)$$

Even without a direct input signal, noise generated in the circuit is reflected with gain continuously through the matching network. Then, it is possible that at some frequency, the amplified noise might reach to a certain level which the device is brought to nonlinear operation and could well be damaged due to this unstable behavior. Therefore, it is very important to eliminate the oscillation by forcing circuit to be unconditionally stable.

For the amplifier system shown in Fig. 3 to be unstable, input and output reflection coefficients $|\Gamma_{in}|, |\Gamma_{out}|$ must be greater than 1, assuming the input and output matching networks are passive that is to say that $|\Gamma_S|, |\Gamma_L| < 1$. This is only possible when the real part of impedance seen looking into port is negative, which means that the unstable region lies outside the unit circle on Smith chart. For unconditional stability:

$$|\Gamma_{[in,out]}| = \left| S_{[11,22]} + \frac{\Gamma_{[L,S]} S_{12} S_{21}}{1 - \Gamma_{[L,S]} S_{[22,11]}} \right| < 1 \quad (10)$$

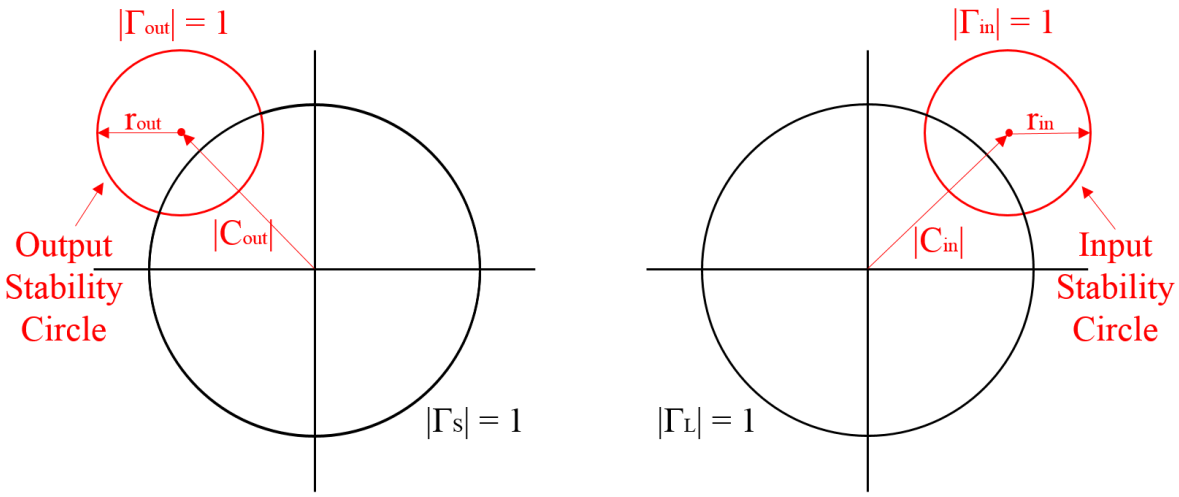

Fig. 7: Input and Output Stability circles in the Smith Chart [11]

To better view the safe operation regions for an amplifier, input and output stability circles can be placed on the Smith chart as noise and gain circles by using the above constraints in Eq. 10. They define the boundaries between stable and potentially unstable Γ_S and Γ_L. These boundaries are identified by setting $|\Gamma_{in}| = 1$ and $|\Gamma_{out}| = 1$. As a result, the radius and center

of stability circles are found as shown in Fig. 7. Then, the stable regions are determined considering $|S_{11}| < 1$ (or $|S_{22}| < 1$). If $|S_{11}| < 1$ is the case, for example, the unstable region lies in the area between $|\Gamma_L| = 1$ and $|\Gamma_{in}| = 1$ circles. Same notion also applies to output stability circle. However, since $|\Gamma_{in}| = 1$ and $|\Gamma_{out}| = 1$ were set while extracting the stability circles, there is a possibility that circuit may be potentially unstable at these boundaries.

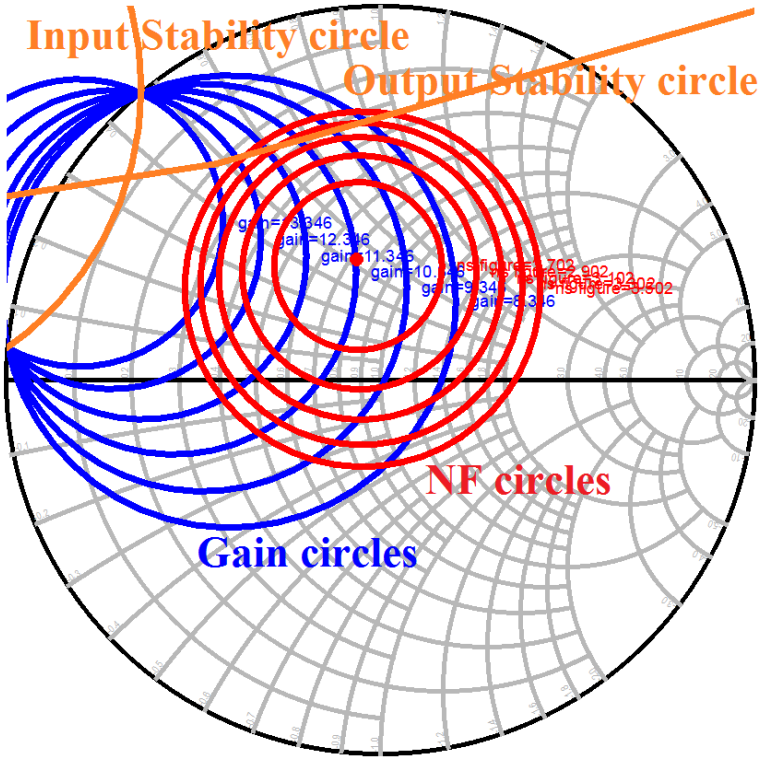

Fig. 8: Stability, Gain and Noise Figure circles in the Smith Chart

For simple analysis, Stern stability factor k is introduced to check unconditional stability:

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}||S_{21}|} > 1 \; and \; |\Delta| < 1 \tag{11}$$

where $\Delta = S_{11}S_{22} - S_{12}S_{21}$. Having calculated the location of stability circles, the Smith Chart in Fig. 6 can be updated as shown in Fig. 8.

.

2.1.4 Input / Output Return Loss and VSWR

Another figure of merit which the amplifier must satisfy is the input and output return losses that should be greater than a certain level (10dB generally). Doing so, the circuit will guarantee a high power transfer through the ports.

By inserting constant VSWR (standing wave ratio: $VSWR = (1 + |\Gamma|)/(1 - |\Gamma|)$) circles into Smith Chart (see Fig. 9), it is seen that the number of optimizations that must be accomplished between these trade-offs greatly increases.

Further, VSWR circles specific to input/output matching circuits can also be placed in the Smith chart. However, due to the feedback through transistor, matching circuits affect each other and complicate the matching process, which in turn points out a bilateral approach in matchings. Furthermore, it should be noted that Γ_{in} and Γ_{out} are functions of Γ_S and Γ_L under bilateral assumption and depend on each other, so does the input and output VSWR circles.

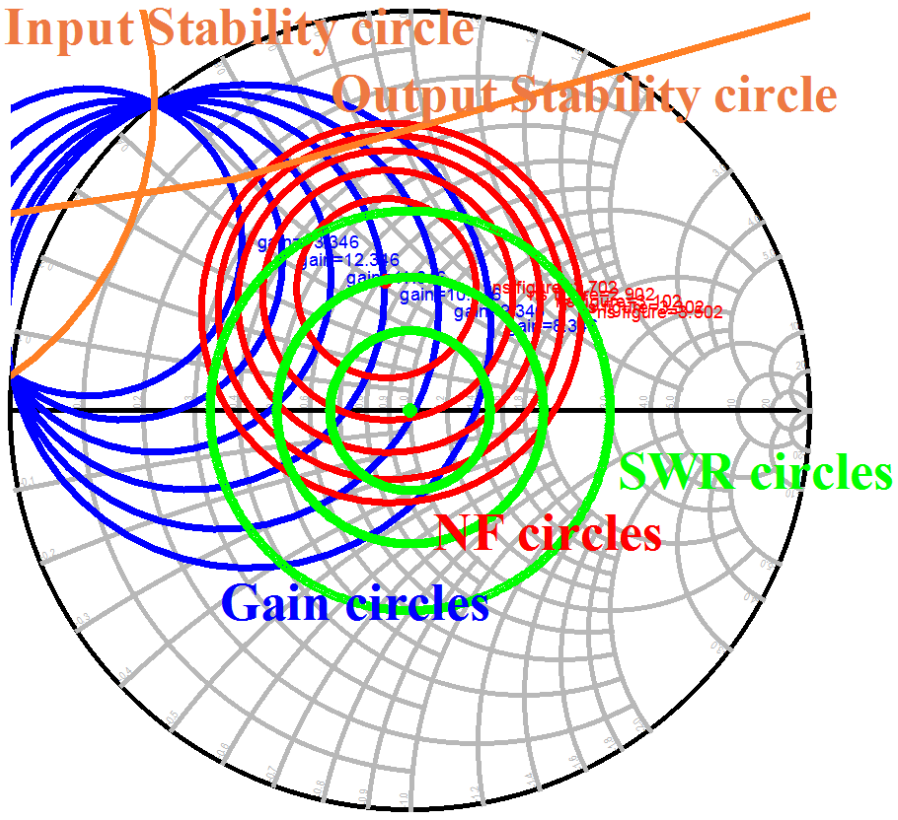

Fig. 9: VSWR, Stability, Gain and Noise Figure circles in the Smith Chart

2.1.5 Linearity

Another significant characteristic of an amplifier is the linearity which is mainly measured by the gain compression and defined as the point where gain is dropped by 1dB with the increasing input power.

A common gain compression plot with respect to changing input power including other linearity specifications is shown below in Fig. 10.

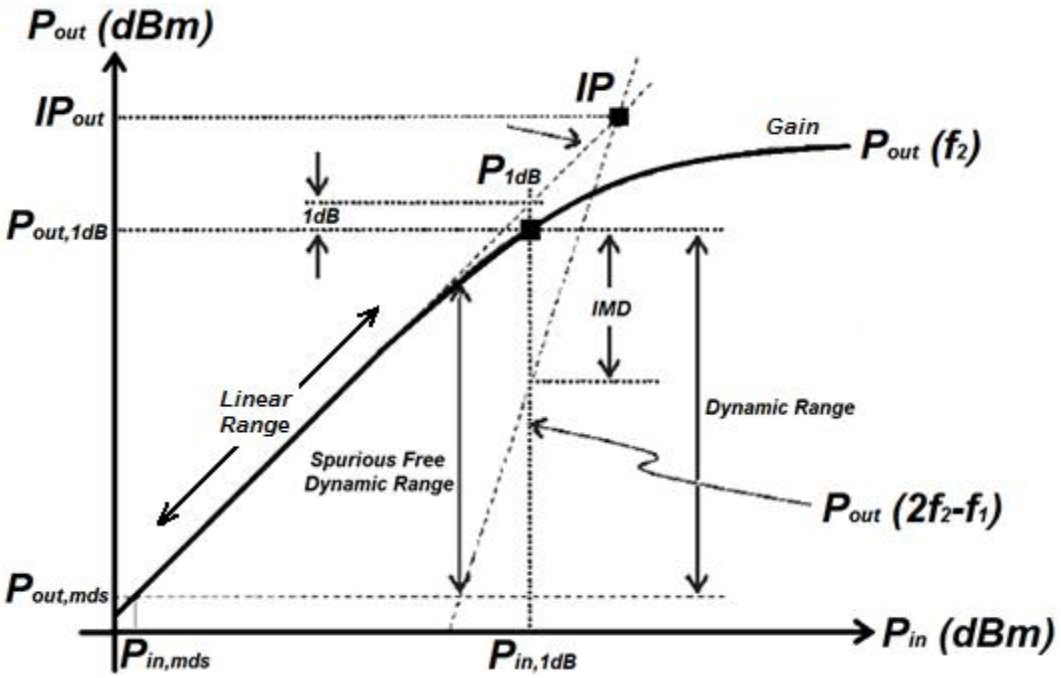

Fig. 10: Linearity measures of an amplifier

The output power may increase up to a certain level and then saturates due to decreasing transistor gain. This peak power is called saturation point (P_{SAT}) and operating beyond the compression point is not a normal operation for a linear amplifier. Furthermore, dynamic range (DR) is introduced to measure the linear operation range of an amplifier and expressed for the region below P_{1dB} until the minimum detectable signal power at the output ($P_{out,mds}$).

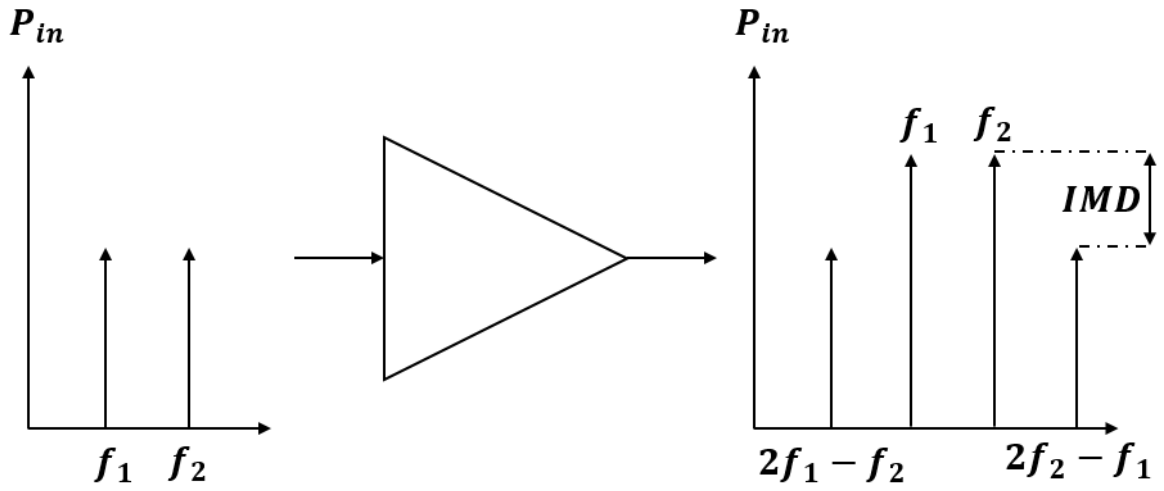

Fig. 11: 3rd order intermodulation distortion illustration

Nonlinear effects of transistors result in intermodulation distortion (IMD) and power loss at the desired frequency and creates multiple harmonics. They also introduce new undesired components to the frequency band of interest. As illustrated in Fig. 11, by applying two close harmonic tones (f_1 and f_2) to the amplifier input, the output is observed and IMD which is defined as the difference between the desired and undesired signals at the output is measured.

The two close tones ($x = A_1 cosw_1 t + A_2 cosw_2 t$) applied at the input will be transformed in the amplifier ($y = a_1 x + a_2 x^2 + a_3 x^3 + \cdots$) and create the linear and third order products, respectively as in Eq. 12 and Eq. 13:

$$a_1 A_1 \cos w_1 t \ \& \ a_2 A_2 \cos w_2 t \tag{12}$$

$$\frac{3a_3 A_1^2 A_2}{4} \cos(2w_1 - w_2)t \ \& \ \frac{3a_3 A_1 A_2^2}{4} \cos(2w_2 - w_1)t \tag{13}$$

There exists many other harmonics, however for the input RF signal located nearly between the two tones, the products above are surely the most critical ones which are very close to input signal and difficult to be filtered out. As shown in Fig. 10, output power changes proportionally to the input in the linear region whereas its third-order harmonic increases proportional to the third power ($A_1^2 A_2$ and $A_1 A_2^2$) of input signal. As a result, a third-order

intercept point (IP3) exists beyond the compression point and used as an amplifier linearity measure.

$$OIP_3 = P(f_1) + IMD/2 \quad (dBm) \tag{14}$$

Observing the following expression in Eq. 15 reveals that if each stage in a receiver chain has a gain more than unity (a_n^2), the IIP3 performance of the last stage ($A_{IIP3,n}^2$) becomes more critical on the IIP3 of overall system ($A_{IIP3,tot}^2$), which it seems that LNA has no direct impact on the overall IIP3 as its counterparts at latter stages.

$$\frac{1}{A_{IIP3,tot}^2} \approx \frac{1}{A_{IIP3,1}^2} + \frac{a_1^2}{A_{IIP3,2}^2} + \frac{a_1^2 a_2^2}{A_{IIP3,3}^2} + \cdots \tag{15}$$

The same expression also implies that LNA could have an IIP3-degrading effect due to its level of gain which, in contrast, lowers the noise figure of system. However the optimization is generally made on improving the noise figure response with high gain.

2.1.6 Isolation

Isolation (or reverse gain) of an LNA affects both the amplifier itself and the whole receiver system. In case of a low-isolation (S_{12}) in amplifier, circuit tends to oscillate with smaller gain values. On the other hand, LNA in a typical receiver chain, such as in Fig. 2, is followed by a mixer which introduces some leakage between its ports due to many reasons like substrate coupling, capacitive paths and bond wire coupling. The LO (local oscillator) signal might leak from the mixer to antenna. Therefore amplifier topologies providing sufficient amount of isolation should be selected.

2.2 LNA Topologies

After specifying the important parameters of an LNA, topology selection must be done in order to eliminate the tradeoffs between these parameters. Since it is almost impossible to attain very high gain and low noise figure with good linearity and perfectly matched input and outputs in a very wide bandwidth, circuit topology must be selected carefully considering the design specifications which will satisfy enough of each parameter. Therefore this section

gives insight into some of the most commonly used LNA topologies and highlights the advantages and disadvantages of each one regarding to these parameters.

2.2.1 Common Emitter / Source Configurations

This single-ended structure shown in Fig. 12 and Fig. 13 is the most basic and employed topology of all. It basically provides low noise, but also low gain. In order to increase the gain, generally, a cascode common base/gate stage or cascaded stages composed of the same structure are added [12]-[14]. While it exhibits good linearity and is fed by lower supply voltages, due to its poor isolation, input and output matching networks are difficult to be designed separately.

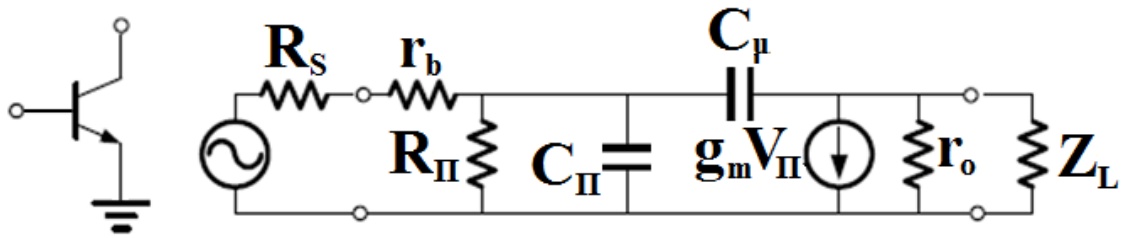

Fig. 12: Common emitter topology with high frequency small-signal model

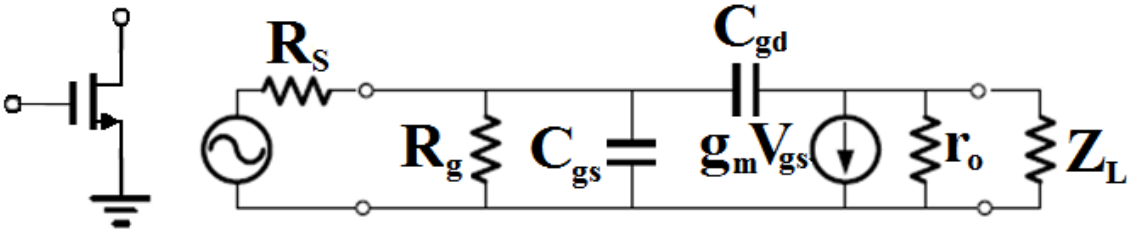

Fig. 13: Common source topology with high frequency small-signal model

Input impedance mainly consists of emitter-base capacitance (C_Π) and base resistance (r_b), which is $Z_{in} = r_b + 1/jwC_\Pi$ if parasitic resistances are neglected. Therefore it suffers from a very low input impedance which makes input matching hard.

To overcome this issue, some methods are applied. With the resistive termination R_P in Fig. 14, input matching is easily achieved and can be used in both narrowband and wideband

applications, but power loss through R_P and the serious noise figure degradation prevent the usage of this method.

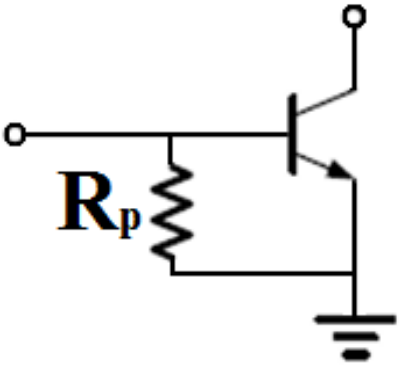

Fig. 14: Common emitter topology with resistive termination

As highlighted in Fig. 15, configurations using resistive shunt and shunt-series feedbacks allow broadband input matching. Although increased linearity is achieved through feedback mechanisms, their poor noise figure and stability performances make them unfavorable too.

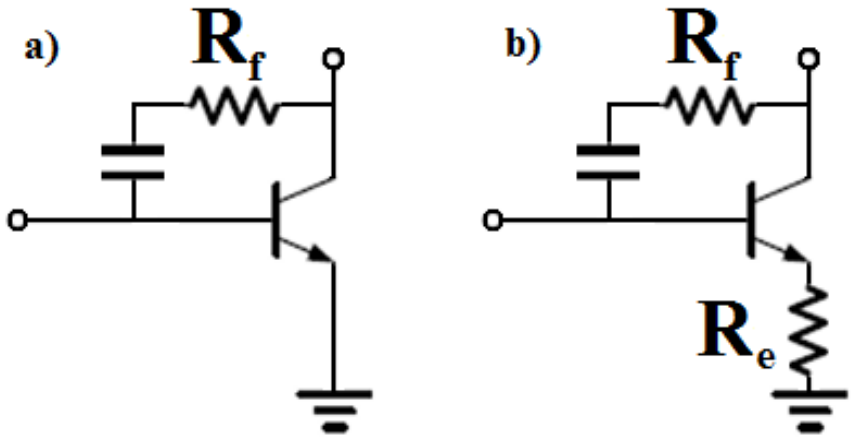

Fig. 15: Common emitter topology with resistive, a) shunt, b) shunt-series feedbacks

Collector feeding may be realized through the resistive load in Fig. 16a, but results in DC voltage drop across R_D which reduces the gain. Therefore inductive load is preferred (see Fig. 16b), since the inductor L_D causes a relatively smaller voltage drop. L_D also resonates with the output capacitor and allows the amplifier to operate at higher frequencies.

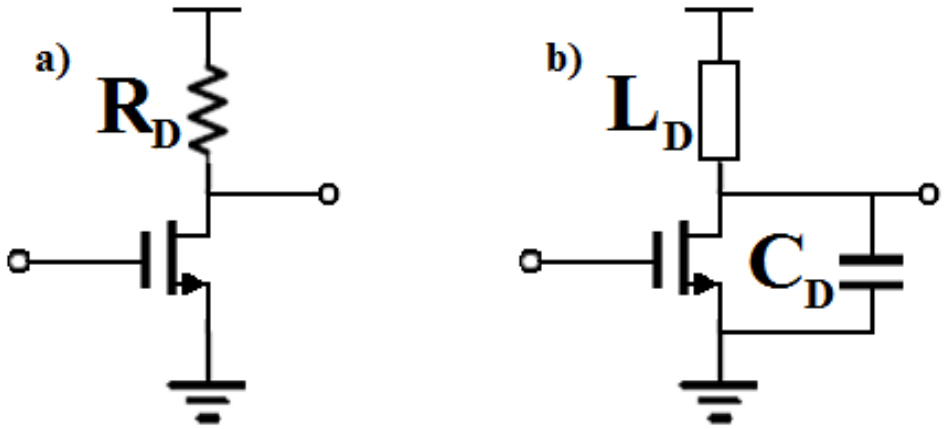

Fig. 16: Common source stage with, a) resistive load, b) inductive load

2.2.2 Common Emitter / Source with Degeneration

As another method to be able to match the input section easily, resistive source degeneration is used at the expense of reduced gain and increased noise figure, which is not desirable for an LNA. However, increasing source resistance helps improve stability since the amplifier gets less dependent on widely varying g_m. This structure is shown in Fig. 17.

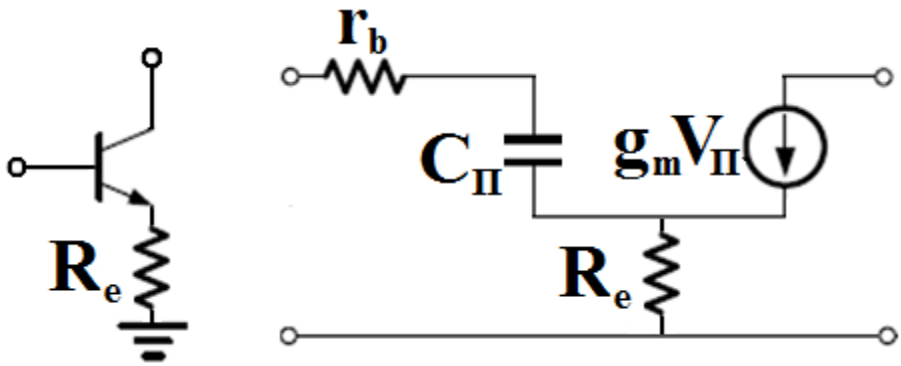

Fig. 17: Common emitter topology with source degeneration

Instead, inductive source degeneration (L_e) as a negative feedback can be an appropriate candidate for easy input matching. Moreover the parasitic effect of emitter-base capacitance is, then, eliminated by L_b (see Fig. 18).

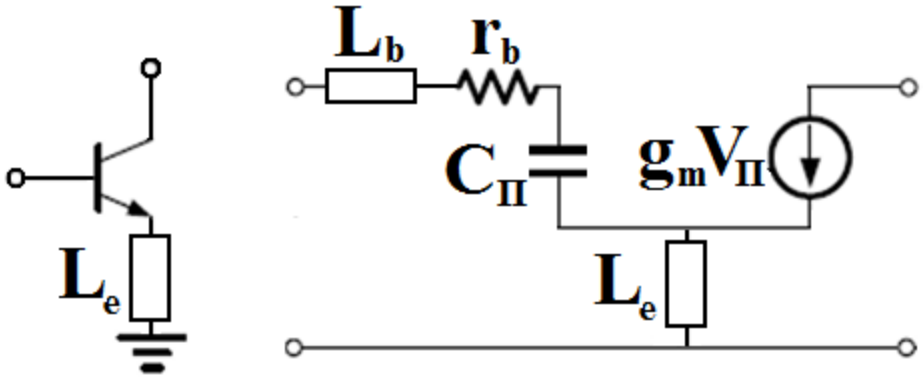

Fig. 18: Common emitter stage with degeneration inductance

In this circuit and its MOS counterpart, input impedances become respectively:

$$Z_{in}(w) = \left(r_b + \frac{g_m L_e}{C_{\Pi}}\right) + j\left[w(L_e + L_b) - \frac{1}{wC_{\Pi}}\right] \tag{16}$$

$$Z_{in}(w) = \frac{g_m L_s}{C_{GS}} + j\left[w(L_s + L_g) - \frac{1}{wC_{GS}}\right] \tag{17}$$

with transit frequency $w_t = g_m/C_{\Pi}$ (which is g_m/C_{GS} for MOS). The real part of this expression, $w_t L_e$, that should be matched to source impedance, does not cause thermal noise. As transit frequency goes higher, impedance matching might not be that safe due to very low inductor values around pH ranges. Thus, a capacitor is added in shunt with C_{GS} to enhance this inductor value by reducing w_t. The imaginary part sets the impedance matching at certain resonance frequency, $w_o = [(L_e + L_b)C_{\Pi}]^{-1/2}$, which is also a disadvantage for a wideband design. On the other hand, increased noise figure owing to resistive loss in L_b ($R_b = wL_b/Q_L$) can be alleviated by larger device size. Additionally, due to increased number of inductors, die are will be much larger.

2.2.3 Common Base / Gate Topology

A resistive input could also be obtained using a common base/gate topology as shown in Fig. 19. By setting correct bias conditions and device size, source impedance matching is achieved

since the resistance looking into the source is $1/(g_m + jwC_{GS})$ or $1/g_m$ approximately if $w \ll w_T$. The frequency independency of the input impedance lets designers to match the source over a very wideband. Furthermore this topology ensures better isolation and higher linearity as compared to common emitter/source designs.

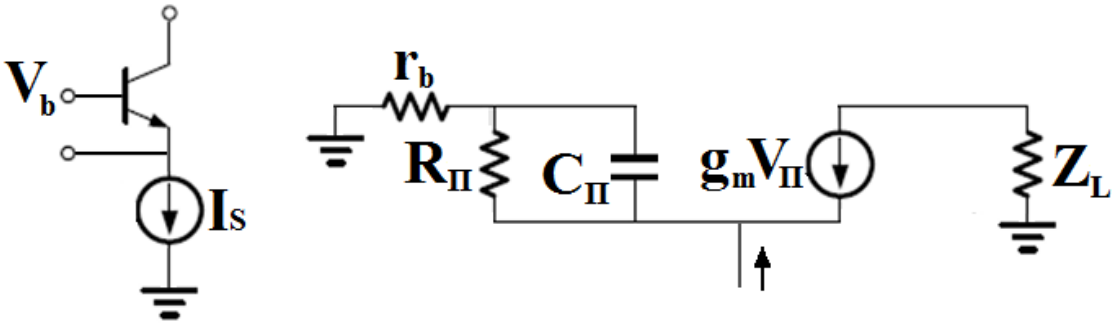

Fig. 19: Common base topology with high frequency small-signal model

However common base/gate architecture causes moderate noise figure with respect to common emitter/source, therefore not preferred.

2.2.4 Cascode Topology

Cascode topology has wide variety of usage in the current literature [3], [10]. The reason for that emanates mainly from its high output impedance resulting in higher gain compared to others. Furthermore, each stage contributes to a higher isolation between input and output ports by suppressing the Miller capacitance of M1, which is important to reduce the chance of oscillation and to increase the bandwidth. On the other hand, the noise figure is relatively higher than a single common source stage, a higher supply voltage is required and output voltage swing is very low.

As shown in Fig. 20, it is basically formed by a common-source stage (M2) followed by a current buffer (M1). Using the same logic, it is obvious that the degeneration inductance will be used to remove the effect of intrinsic capacitance of M1, while 50Ω to be matched at the source will be realized by setting L_g.

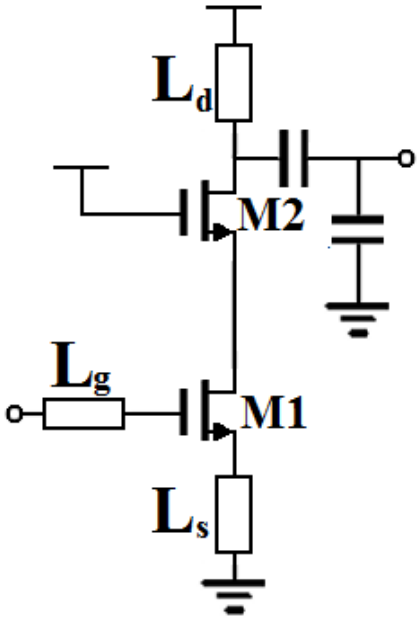

Fig. 20: Cascode common source amplifier topology

2.2.5 Folded Cascode Topology

For very low-voltage applications, folded cascode topology is utilized (see Fig. 21). Also they provide good isolation and increase stability. However the number of matching elements does not make this topology prefferable as previous topologies.

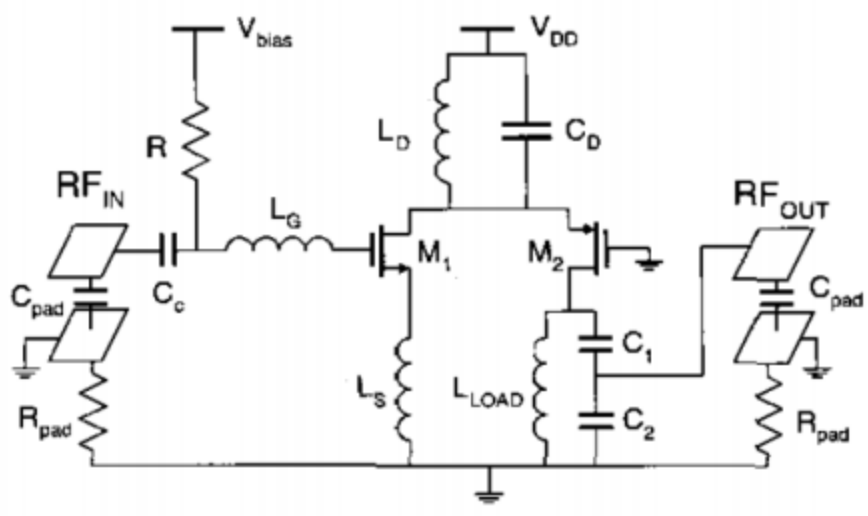

Fig. 21: Folded cascode topology

3. Low Noise Amplifier Design

In this chapter, simulation and measurement results of the fabricated LNA structures to be used in the W-band automotive radar receiver are presented. The chips are built using a low-cost SiGe HBT process which provides a high-level of integration. The steps until designing a wideband amplifier are clearly explained by comparing the fabricated chips. Finally a three-stage single-ended ultra-wideband LNA is proposed and measurement results are discussed. This three-stage structure will be used in the active phase shifter designs in Chapter 5.

3.1 Technology, Device & Topology Selection

In order to maintain high-performance and low-cost with high-reliability and low power, alternative integrated circuit technologies have been under investigation for many years. These specifications are, now, can be achieved through SiGe HBT (silicon-germanium heterojunction bipolar transistor) technology which greatly advances the conventional Si BJT, especially for high frequencies. In this context, the integration of germanium with silicon reduces the level of base-emitter potential barrier, which evidently boosts the current

gain with increased collector current. Moreover, the unity gain bandwidth product (f_t, where the current gain drops to 0dB) and maximum oscillation frequency (f_{max}) increases, allowing increased integrated circuit speed. Other advantages of this technology include the lowered noise figure and higher temperature robustness performances. Considering these reasons, LNAs in this chapter and phase shifters in Chapter 5 are built using 0.25μm 180/220 GHz & 0.13μm 300/500 GHz (f_t/f_{max}) SiGe HBT technologies which is commercially available by IHP-Microelectronics.

As was stated in Chapter 2, there exist various topologies with related trade-offs that can be used in LNA design. Working in the mm-wave frequencies does not allow designs to have high gain and also results in minimum noise figure to increase due to close operation to f_T. The gain-noise figure trade-off is basically what determines the topology, as well as the design complexity and supply voltage. Taking these into account, common-emitter topology, which is the most used driving circuit, is utilized in presented designs. While providing comparable gain and very low noise, its low output impedance can overcome matching networks with low quality factor. Another advantage is that supply voltages will be much lower since a single transistor is fed. In order to increase the gain further, cascode and cascade architectures are selected and discussion of the results of different configurations is shared. Although the cascaded structure has more insertion loss due to increased number of inductors at each stage, the configuration allows a simple design with relatively high gain and low noise if the first stage has enough gain to reduce the noise of latter stages.

It is explicit that a single stage, single-ended amplifier (the core, single BJT) will have the lowest noise figure, but the gain will not be enough for most applications. Therefore, cascode architecture should be manipulated to increase the overall gain while compromising on overall noise performance. For wideband applications, the number of stages should be increased therefore increasing the complexity and noise figure of design. As a result, a three-stage single-ended structure will resolve the noise figure issue, providing relatively high gain and having a wideband performance. Noise contribution of the latter stages are negligible, which yields a careful optimization on the first stage according to the lowest possible noise figure, and on the latter stages, optimization to highest gain. Moreover, owing to having no cascode parts, supply voltages will be much lower. Adding another stage provides a wider

bandwidth with a higher gain, but contradicts with the amplifier stability. In order to make the circuit unconditionally stable for the band of interest again, gain should be reduced, then. However, instead of using a 4 stage amplifier, a less-complex 3 stage design achieves almost the same specifications.

3.2 Design Procedure

To find the optimum bias point of a common-emitter stage, I-V curve, noise figure and associated gain plots of the transistor are extracted and can be seen in Fig. 22-23. By using this data for the three-stage LNA, an optimum point of 20µA of I_B at 1.5 V of V_{CE} is found which corresponds to 2.4dB of NF, 10dB of gain and 8mA of collector current approximately. This optimum point is also utilized for latter stages since the gain and noise figure performances are satisfying. The same optimization procedure with different bias conditions regarding to minimum noise figure and gain trade-off is also realized for the cascode LNA.

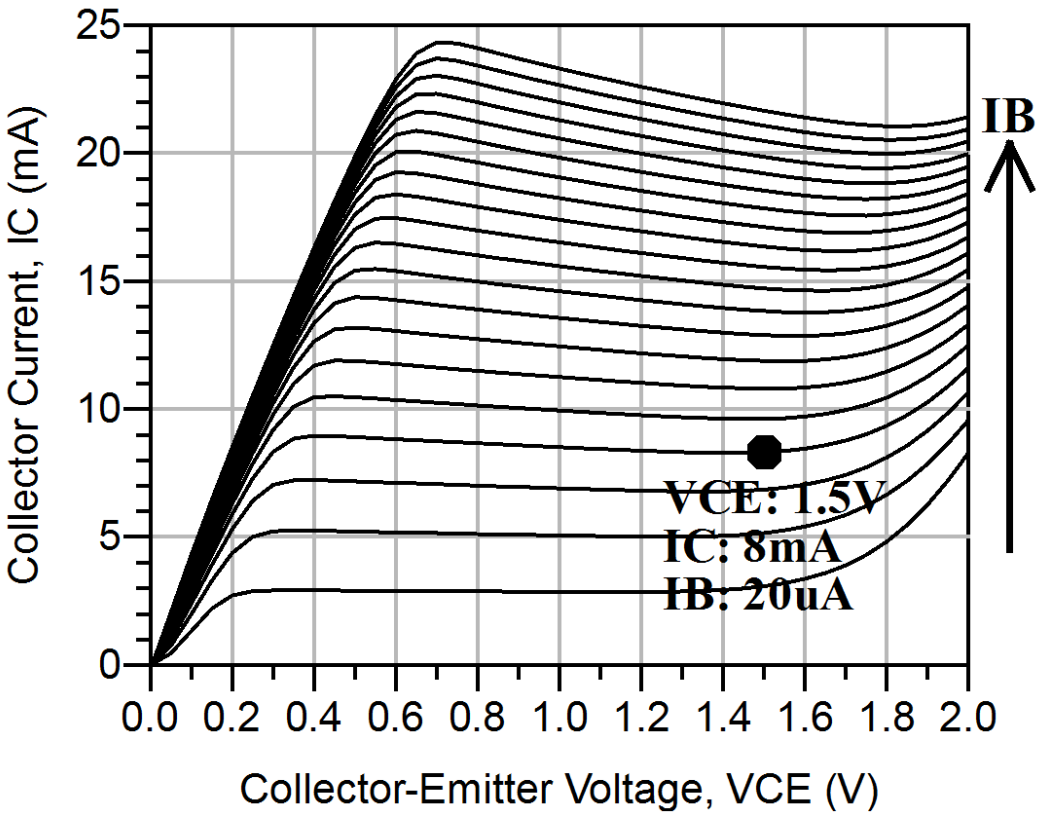

Fig. 22: I-V curve of IHP npn-SG13G2 HBT (Num. of emitters: 8)

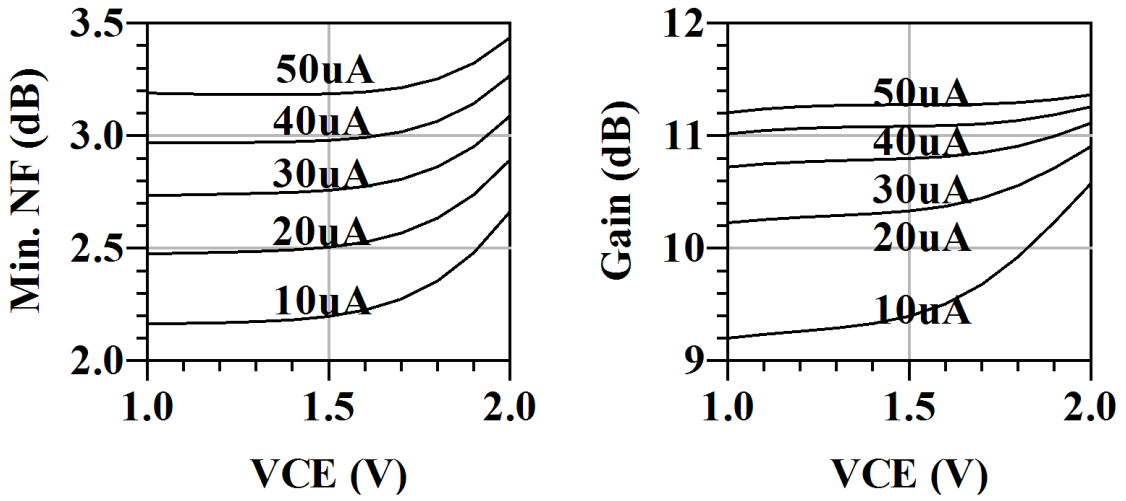

Fig. 23: NF_{min} and associated power gain of IHP npn-SG13G2 HBT (Num. of emitters: 8)

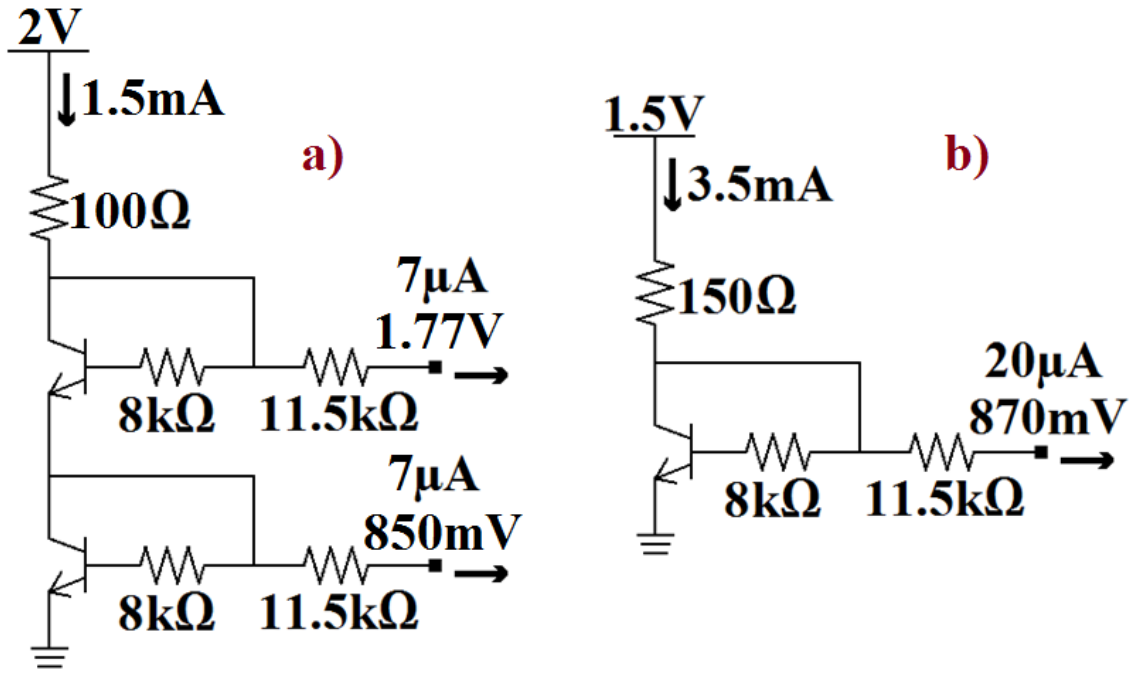

Fig. 24: Bias circuit of, a) single-stage cascode LNA for 7µA of I_B and 4mA of I_C at 2V of V_{CE}, b) three-stage LNA for 20µA of I_B and 8mA of I_C at 1.5V of V_{CE}

After finding the optimum bias points and placing the simple bias circuits as shown in Fig. 24, input and output matching networks are designed accordingly to extract the expected noise figure and gain, with respect to the contradicting performance parameters of HBT (see Fig. 25). Using the Smith chart, $Z_{S,opt}$ should be selected as $36 + j26\,\Omega$ for minimum noise

figure which means that a reduced gain from the first stage would be obtained while matching the input to 50 Ω. For the cascade stages, matching conditions are changed to acquire the maximum possible gain. Moreover, the unstable behavior of HBT ($K < 1$) under this bias condition points out the importance of matching networks (see Fig. 26).

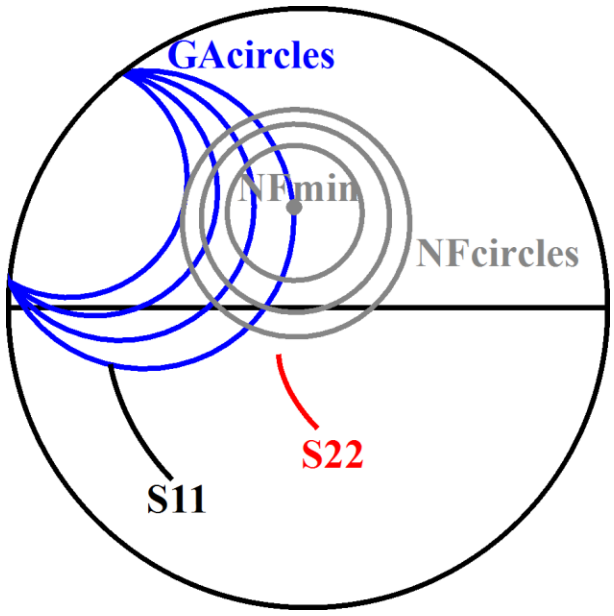

Fig. 25: IHP npn-SG13G2 HBT (Num. of emitters: 8) contradicting performance parameters on Smith Chart for the specified operating point

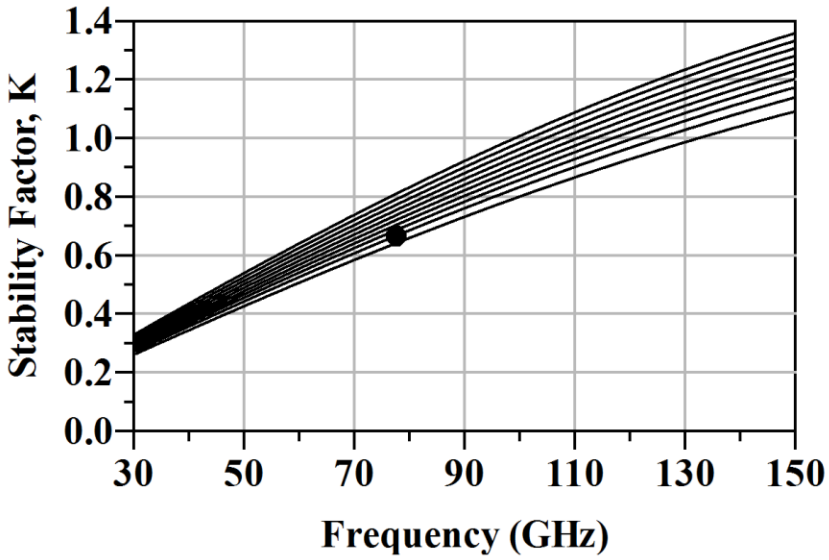

Fig. 26: Stability factor of IHP npn-SG13G2 HBT (Num. of emitters: 8) under different bias conditions

L-type and Π-type matchings, including the pad capacitances, are used in input, output and inter-stage matching networks as shown in Fig. 27-28. W-band does not allow designs to have high inductor values as in spiral structures at lower frequency bands. Thus, for the inductors, simple microstrip transmission lines are designed whose lengths are altering between 100μm and 155μm with fixed 3μm width for the LNA designs. As a result, the microstrip lines correspond to inductor values ranging from 55pH to 90pH with quality factor of 20 and parasitic resistances of 1.4Ω to 2Ω. Inductors are drawn in the upper most metal layer in a 7-layer technology [16] to lower the insertion loss and to be able to derive the maximum current without damaging the lines (3μm-thick TopMetal2). Additionally, ground shields are used below the inductors to enhance the quality factor performance by removing the substrate parasitic. Also, MIM (metal-insulator-metal) capacitors are utilized for RF ground, DC block and matching purposes. These foundry provided capacitors have high quality factors and are placed between TopMetal1 and Metal5 with a dielectric thickness of 40nm and relative permittivity of 6.75. For the upper and lower plates, 150nm thick special MIM layers and Metal5 layer are used. GSG pad capacitances of about 15fF are also included in the schematic level designs.

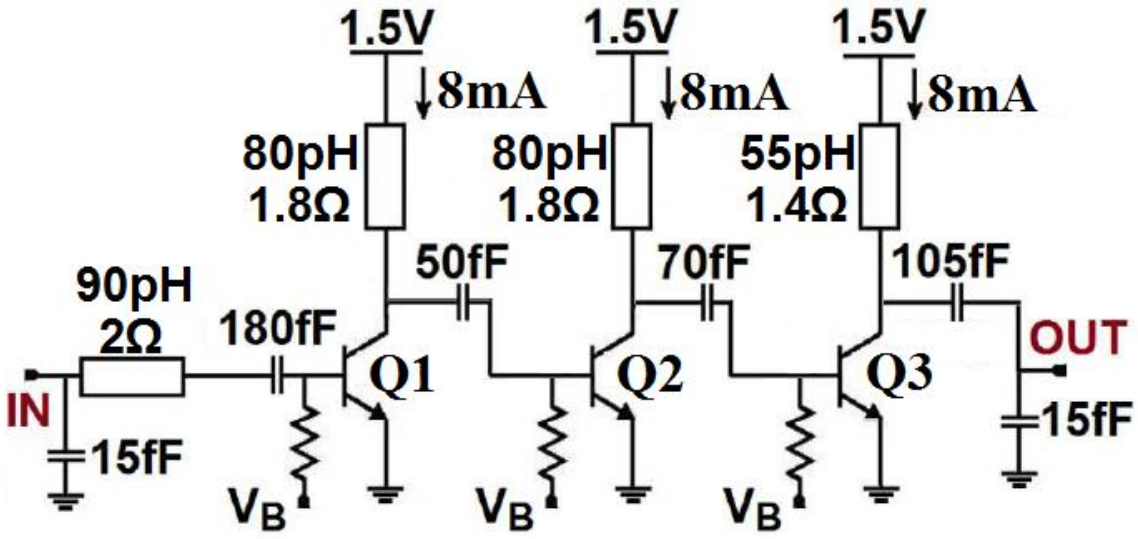

Fig. 27: Three-stage common-emitter LNA schematic

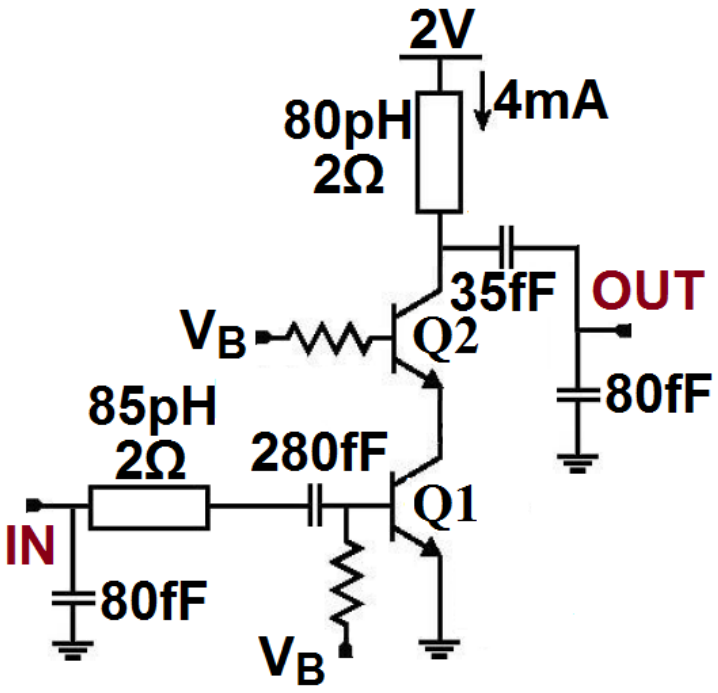

Fig. 28: Single-stage cascode LNA schematic

Considering all these design procedures, full EM simulations are performed in Agilent ADS software. Simulated LNAs are as shown in Fig. 27-28 and only HBTs are integrated to EM-simulated matching networks on schematic.

3.3 Simulation & Measurement Results

The designed LNAs were manufactured at IHP-Microelectronics by using SiGe HBT 0.13µm SG13G2 technology. The fabricated single-stage and three-stage LNA chips can be seen in Fig. 29-30. They occupy 0.18mm^2 and 0.2mm^2 of area respectively.

Measurements are conducted in the SUNUM labs (Sabanci University Nanotechnology Research and Application Center) using a PNA 5245A Network Analyzer.

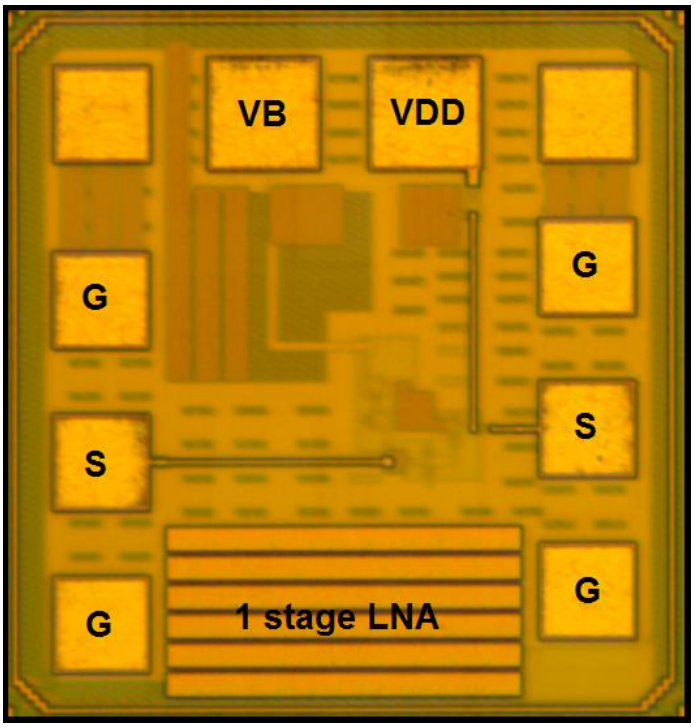

Fig. 29: Fabricated 1-stage cascode LNA, 0.18mm^2

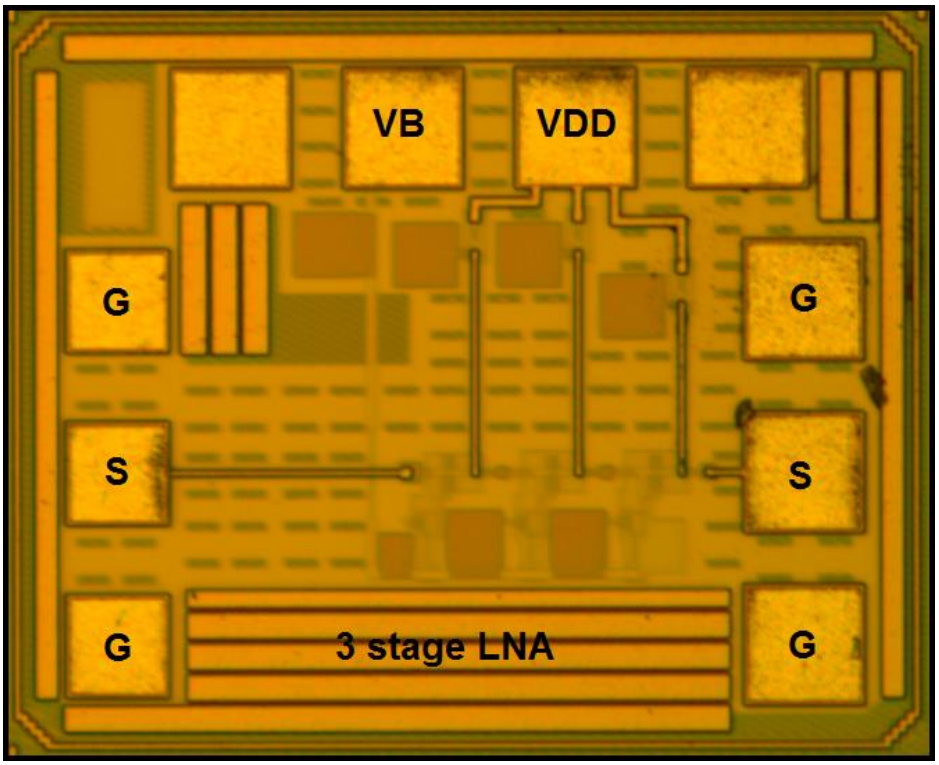

Fig. 30: Fabricated 3-stage single-ended LNA, 0.2mm^2

The edge operation conditions are as follows. The single-stage cascode structure derives 5.5mA of current in total and consumes 11mW of power. Three-stage cascade LNA, on the other hand, absorbs 51.75mW with 34.5mA.

In Fig. 31-32, measured (solid lines) and simulated (dashed lines) S-parameter performances of the LNAs are highlighted. Cascode LNA has 17dB peak gain at 80GHz from a single stage (see Fig. 31). In the 82-85GHz band, input and output return losses are both below 10dB with 16.5dB gain and 30dB isolation. The measured 3dB-bandwidth is 11GHz. From the simulations, average noise figure in this band is found to be 5.1dB and gain performance is parallel to measurement results. However a 3GHz frequency shift is observed at both input and output ports.

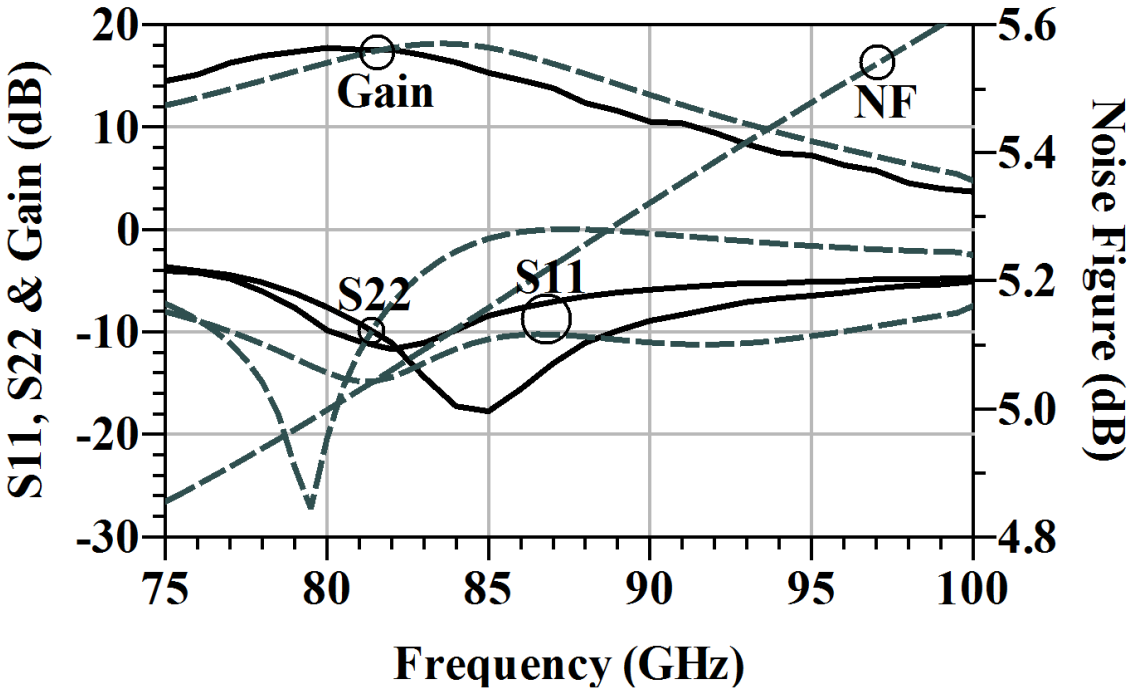

Fig. 31: Measured & Simulated (dashed) performance parameters of LNA1.

As stated in the previous sections, the wide band performance is attained from the three-stage LNA with a flat over 15dB gain throughout the entire W-band, with 21dB peak, as shown in Fig. 32. Input and output are well matched below 10dB in a minimum-25GHz bandwidth between 75-110GHz. The available setup allows measurements between 75-110GHz,

however in the simulations, 3dB bandwidth is found as 35GHz, covering the entire V-band & W-band. Noise figure is also very low for such high frequencies, which is 4.9dB on average in simulations, where isolation is more than 40dB.

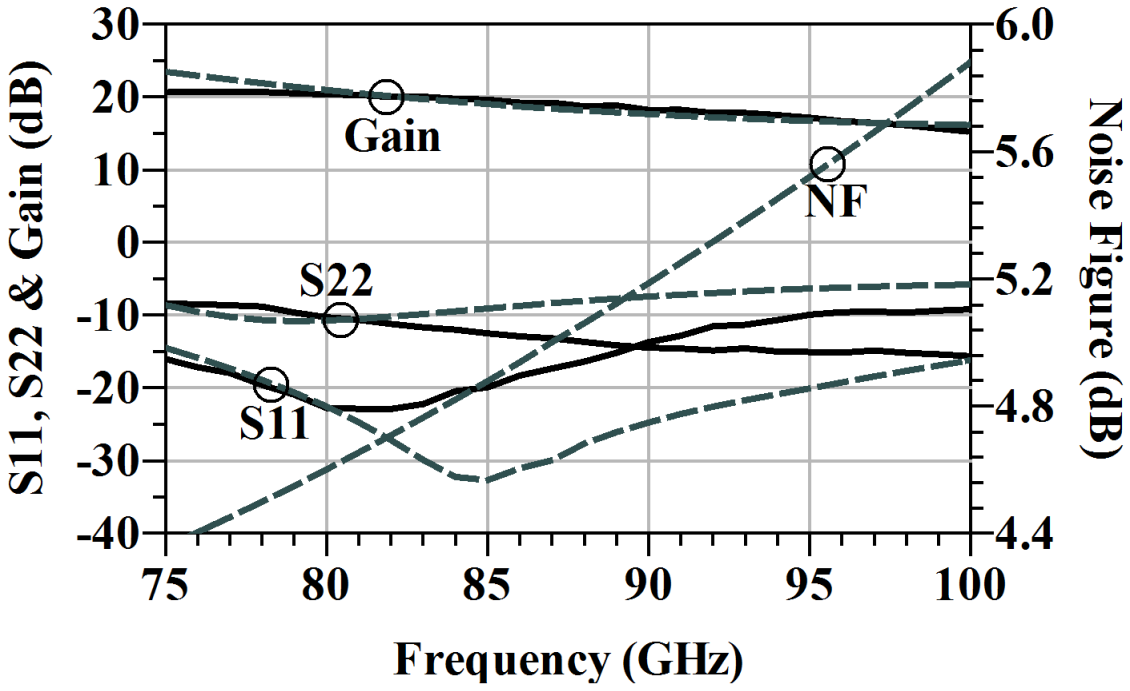

Fig. 32: Measured & Simulated (dashed) performance parameters of LNA3.

For the schematic design in which only lumped components are used for an overall look at the very first design steps, the noise figure is tried to be matched in the first stage without much compromise in gain, return loss and bandwidth. Considering the selected bias points and these constraints, the minimum noise figure is found near 70 GHz. However in full layout simulations, this frequency is shifted to 60 GHz being 4dB, and at 77 GHz, the noise figure is simulated as 4.45dB. From the simulations it is seen that the measured results almost overlaps the simulation results in gain and return loss performances.

In Fig. 33, input and output power handling performances extracted from the simulations of each are presented. From the results, it is seen that cascode and three-stage LNAs have output 1dB compression points of -6dBm and -4dBm. Furthermore three-stage LNA has a 5.5dBm of OIP3 (output third order intercept point) from two-tone intermodulation simulations.

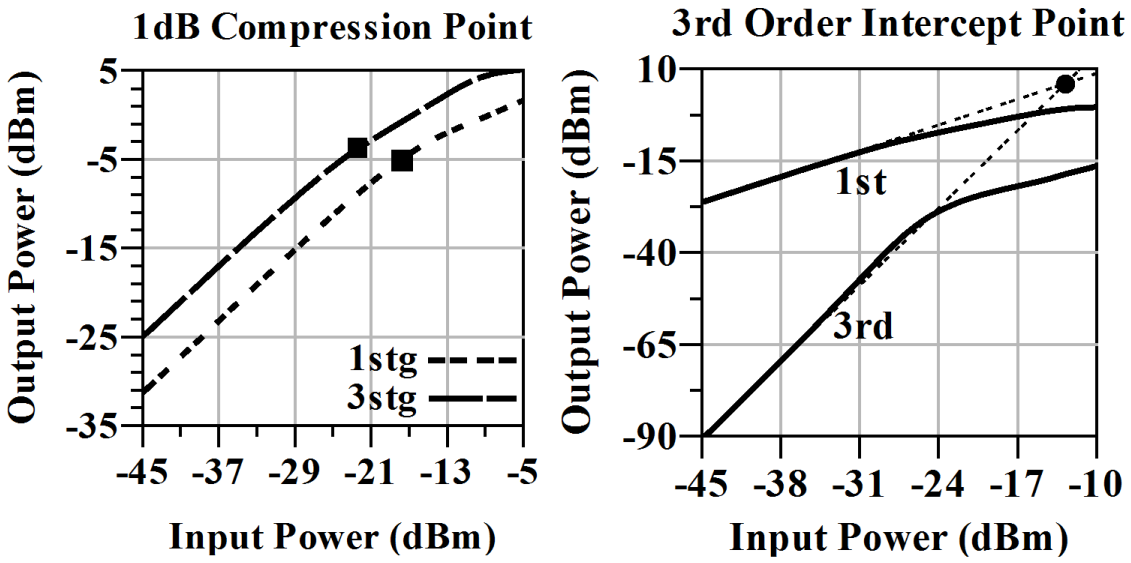

Fig. 33: Simulated Input / Output 1dB compression point of LNAs and IIP3 / OIP3 point of the three-stage LNA.

3.4 Conclusion

In this chapter, the design steps of single-stage cascode and three-stage cascade LNAs using 0.13µm SiGe HBT technology are presented with their simulation and measurement results. Having examined the results, it is obvious that these 0.2mm^2 chips with 17dB/21dB peak gain and 5.1dB/4.9dB noise figure (cascode/cascade LNAs) could be utilized in W-band automotive radar applications. The three-stage LNA achieves one of the best overall performances in the current literature (see Table I). In this table, some of the state-of-the-art LNAs operating in W-band are shown. According to the measurement results of this three-stage LNA, the highest bandwidth and gain with low noise figure are achieved while the input and output return losses are both better than 10dB for the whole frequency band which implies that this LNA could be used as a complete amplifier, not requiring any off-chip matching networks. Furthermore, the areas of use of the three-stage LNA will be examplified and a full radar performance will be studied in the next chapters.

TABLE I

COMPARISON OF STATE-OF-THE-ART W-BAND LOW NOISE AMPLIFIERS

Ref	Technology	Used Arch.	f_o (GHz)	Gain (dB)	NF (dB)	RL (dB) < 10dB	3dB BW (GHz)	Power (mW)	OP1dB (dBm)
[3]	0.18µm SiGe BiCMOS	2stage C-CE	77	14.5	6.9	76-85 GHz	14.5 (69-83.5)	37	3.1
[12]	90nm SiGe BiCMOS	4stage SE-CE	90	19	5.1	S11 not well	30 (75-105)	43	-3
[9]	0.13µm SiGe BiCMOS	4stage SE-CE	85-89	19	8	94-98 GHz	17 (80-97)	25	-3
[11]	0.13µm SiGe BiCMOS	2stage C-CE	110	20	4	100-115 GHz	20 (100-120)	17	-4 **
[4]	65nm CMOS	5stage SE-CS	90	27	6.8	S22 not given	10	36	NG
[13]	70nm GaAs mHEMT	4stage SE-CS	80-95	25	2.7 **	S11 not well	35 (70-105)	35	2 **
[14]	50nm InGaAs mHEMT	3stage SE-CS	57-110	16.4-23.2	2.1-2.8	75-90 GHz	NG	0.9	-1.4
[15]	0.1µm InP HEMT	3stage	94	19.4	2.5	S11 not well	35 (67-102)	18	NG
This Work	0.13µm SiGe BiCMOS	3stage SE-CE	77	21	4.5 **	75-100 GHz	> 25 (75-100)	50	-4 **

*C: cascode, SE: single-ended, CE: common-emitter, CS: common-source, NG: Not Given, **: simulated.*

For the return loss, a common frequency band is extracted where both input and output return losses are better than 10dB.

4. Phase Shifter Basics

In order to change the transmission phase of a network, phase shifters are utilized. They enable to rotate the input signal electronically, mechanically and magnetically having a 360^o of phase coverage area. Ideally, phase shifters should provide very low attenuation with negligible phase error and equal amplitude for all possible phase states.

Many phase shifter categories exist in literature such as digital/analog and active/passive structures. In contrast to digital phase shifters, analog ones are controlled by a voltage to shift the phase in full 360^o range. While being not as reliable as the digital phase shifters, they provide continuous phase shifts which may lead to increased number of bits in a smaller die size. Yet digital phase shifters are of first choice since they are more immune to phase variations with slight changes in control voltages. In this context, they introduce a set of discrete phase states using "off" states as the reference and "on" states providing the phase shift. Therefore, by switching between these modes, different phase states could be achieved.

On the other hand, active type phase shifters eliminate the attenuation problem in passive phase shifters by providing gain to the circuit so that amplifiers in the latter stages could be

removed, therefore reducing the cost and power consumption at the expense of low linearity. But, still passive type is more adopted due to reciprocity and higher linearity.

This chapter is dedicated to some of the important phase shifter parameters and commonly used topologies respectively in the following sections. In Chapter 5, implementations of some phase shifters will be presented.

4.1 Important Phase Shifter Parameters

All commercial and military phased array radar systems utilize phase shifters, which brings some design specifications as a result. In order to measure the quality of a phase shifter, many parameters exist such as power consumption, insertion loss, input/output return losses, linearity, operating frequency band and switching time. Yet the most crucial ones are phase/gain error performance and effective number of bits which are different than other radar building blocks.

4.1.1 Phase Error

As previously mentioned, ideal phase shifters should exert negligible phase deviation from the desired phase. However, unlike the other performance metrics, phase is harder to be controlled from the simulations and may lead to serious errors that cause overall gain errors due to vector summations of signals in a phased array system and a decrease in effective number of bits.

Phase error is calculated by using root-mean-square (RMS) method. After having all the phase states and each subtracted from the sum of a selected reference state and the desired phase at the output, the average error is calculated. Then shifting each phase state by the resulting average phase error, correct errors (Φ_n) are found which will be utilized to calculate RMS error, as shown:

$$RMS\ phase\ error = \sqrt{\frac{\sum(\Phi_n)^2}{N}} \tag{18}$$

where N is the total number of states. Using this relation, an error curve with respect to frequency is found which has a minimum centered at the operation frequency and error increases for the rest of the frequency band.

4.1.2 Gain Error

In practice, there is always a difference between insertion loss/gain of each state as in phase error. This basically emanates from the different circuit elements providing different phase shifts as will be shown in Section 4.3. Using the same method of finding the phase error, RMS gain error is calculated from individual gain of each state (A_n):

$$RMS\ gain\ error = \sqrt{\frac{\sum(A_n)^2}{N}} \tag{19}$$

4.1.3 Number of Bits

Having designed an N-bit phase shifter does not necessarilly mean that it will be operational for full N-bit. Owing to phase errors, some phase states may not be distinguishible from other states which will be modulated by the digital circuitry. Therefore an N-bit phase shifter should have phase states and RMS errors clearly separated by at least half of its least significant bit ($360^o/2^{N+1}$).

4.2 Phase Shifter Topologies

In this section, commonly used phase shifter topologies are discussed including switched-line, loaded-line, reflection type, switched filter and vector modulator phase shifters.

4.2.1 Switched-Line Phase Shifter

As shown in Fig. 34, the switched-line phase shifter [17]-[20] is composed of two signal paths such that phase shift can be controlled digitally by switching between the lines. In this case, the difference of electrical lengths of two delay lines determines the relative phase shift.

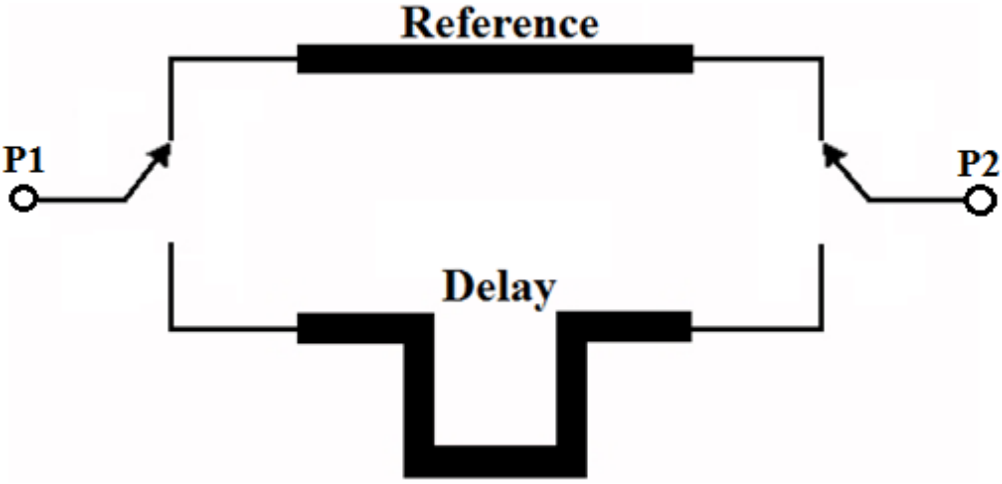

Fig. 34: Switched-line phase shifter illustration

The switches used in this figure are single-pole-double-throw (SPDT) switches and could be realized in many ways including MEMS, PINdiode, mechanical switches and FET. However, isolation of these two branches are of high importance, since any reflection on the "off-path" would cause loading on the "on-path" and, as a result, required phase and amplitude performances are adversely affected. It should also be noted that the overall performance of the phase shifting block is based on the SPDTs performance such as insertion loss. Other disadvantages are that RMS phase error is very frequency dependent and large die size is necessary due to long transmission lines.

Other configurations of switched-line phase shifter basically utilizes Hybrid, Lange or Rat-Race couplers which split the incoming signal into two by adding 90^{o} phase difference [21]-[23]. Variable reactances are placed at the ends of isolated ports to insert an additional delay element at the output port by switching between these (see Fig. 35). For lower phase shifting bit blocks, loaded-line phase shifters are generally used as shown in Fig. 36. In this case, return loss greatly depends on the reactance element, so does each phase state.

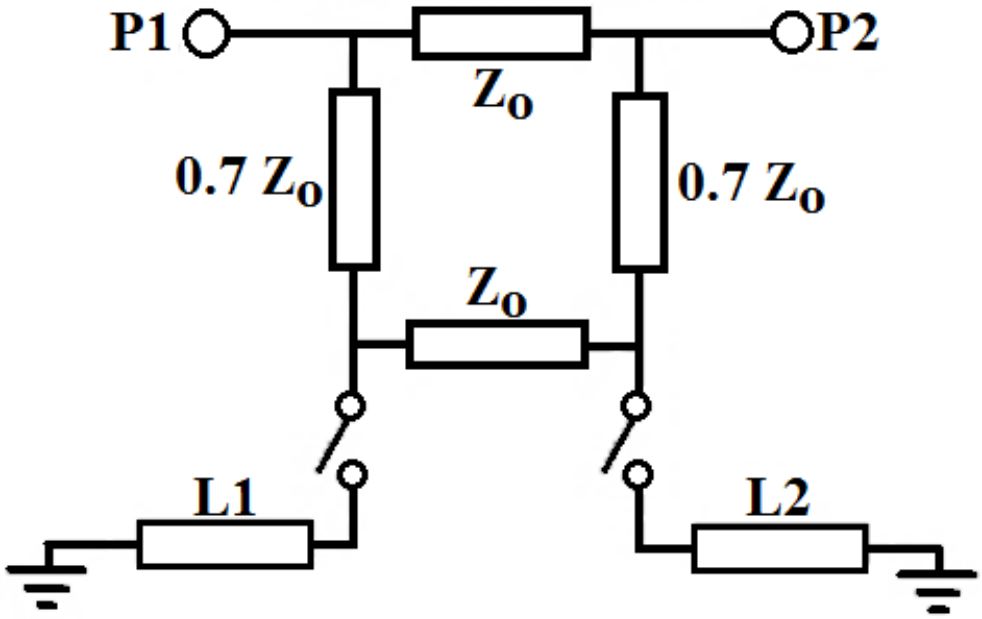

Fig. 35: 90° hybrid coupler type phase shifter illustration

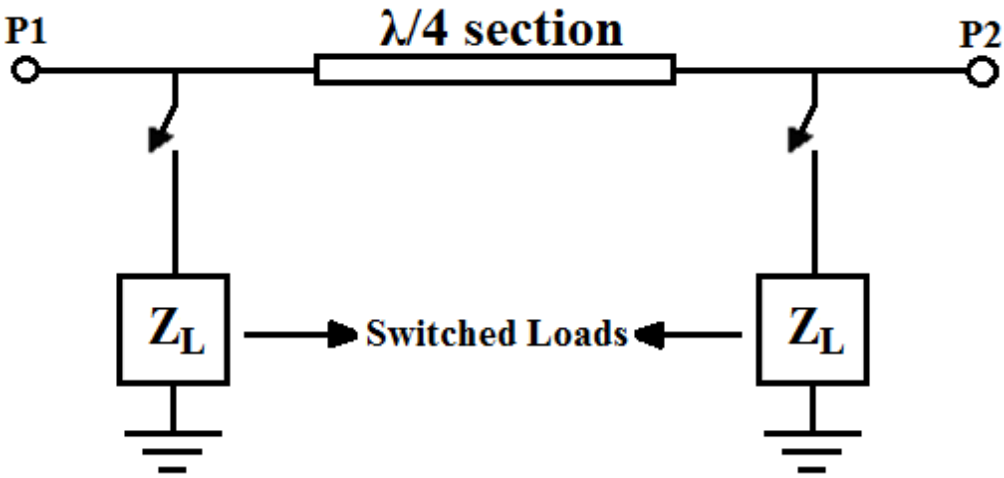

Fig. 36: Loaded-line phase shifter illustration

4.2.2 High-Pass / Low-Pass Phase Shifter

A high-pass/low-pass type phase shifter can overcome the low bandwidth and high chip area of switched-line type. The logic behind is the same except the phase providing part is made of high-pass and low-pass filters in either branch as shown in Fig. 37. The inductor and

capacitor component values should be chosen such that the cut-off frequencies of filters reside out of the interested frequency band.

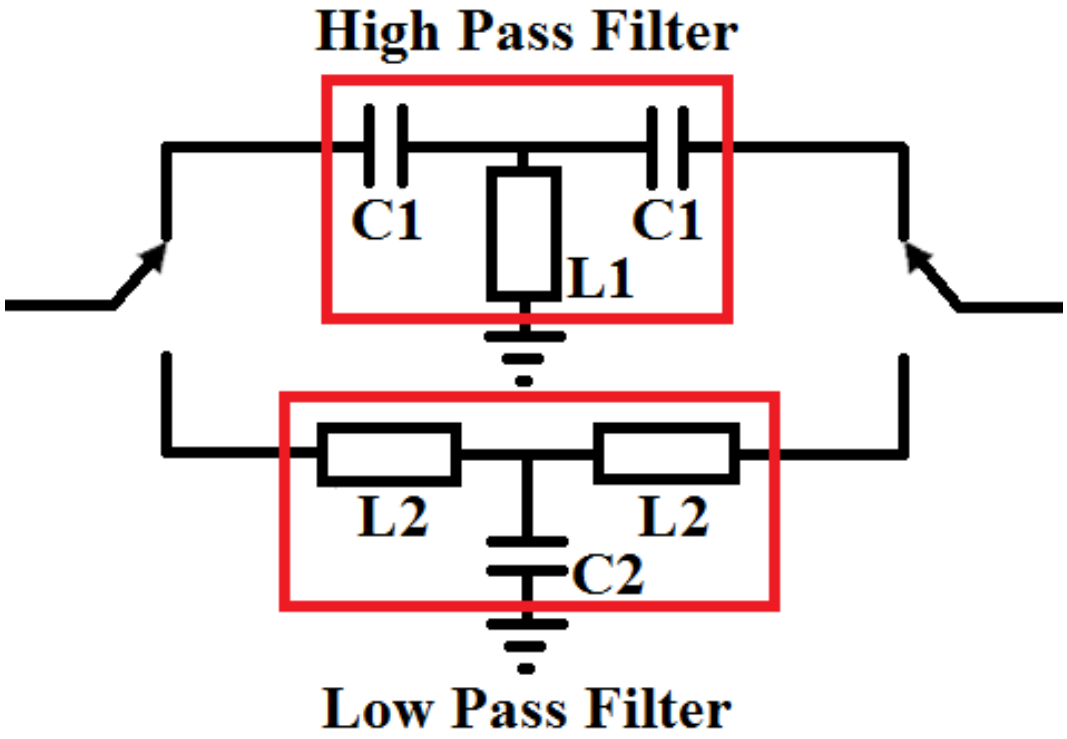

Fig. 37: High-pass/low-pass phase shifter illustration

4.2.3 Vector Modulator Phase Shifter

In this topology, input signal is divided into two and, after being amplified with different variable gain amplifier (VGA) gains and shifted by 90°, they are combined to get the desired phase shift at the output. Vector modulator type phase shifter is illustrated in Fig. 38 [24]-[28]. The 90° of phase difference is added to cover a single quadrant. Then the weighted sum of the two vectors determine the total phase shift. However, even little changes in voltage will tune the phase and, owing to summation of signals with different gains, amplitude of output signal varies relative to phase state. On the other hand, the advantage of vector modulator topology is that it provides gain without the use of an additional amplifier instead of previously mentioned topologies that causes insertion loss.

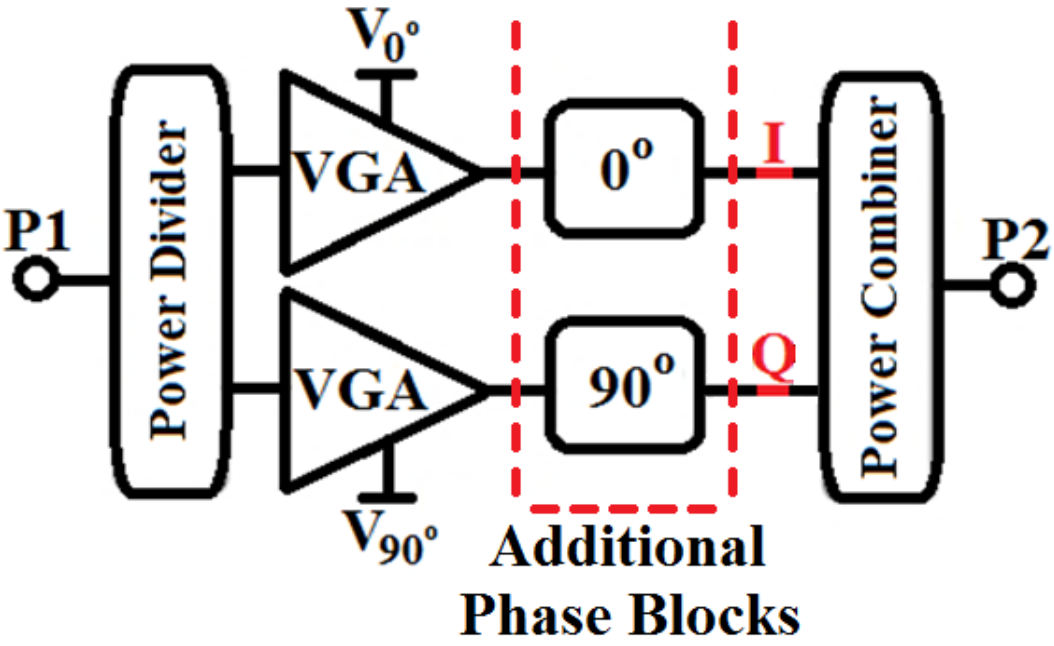

Fig. 38: 90° vector modulator phase shifter illustration

5. Phase Shifter Design

In this section, three different phase shifter designs are introduced. For the first design, MEMS technology is utilized and two two-bit digital phase shifters are fabricated [29]. On the other hand, the second design is composed of three LNAs to create an active analog phase shifter covering full 360° continuously [30]. Finally as a third design, two LNAs and two one-bit phase shifter blocks are integrated with Wilkinson power divider/combiner structures and form an analog I/Q type active phase shifter [31]. This chapter is dedicated to design steps, simulation results and measurement results of these fabricated phase shifters that are built on low-cost SiGe technology.

5.1 MEMS Based Digital Two-Bit LSb & MSB Phase Shifter Design

The final antenna array system to be designed is shown in Fig. 39 which is composed of antenna, LNA and 4-bit MEMS based phase shifter at each branch. Using phased array antennas, narrower beamwidth could be achieved to reject multipath clutter signals as well as to increase SNR through the increased antenna gain. Moreover, antennas and the rest of

the active circuits can be integrated on the same chip for further decrease in cost and for less number of iterations in the transceiver design.

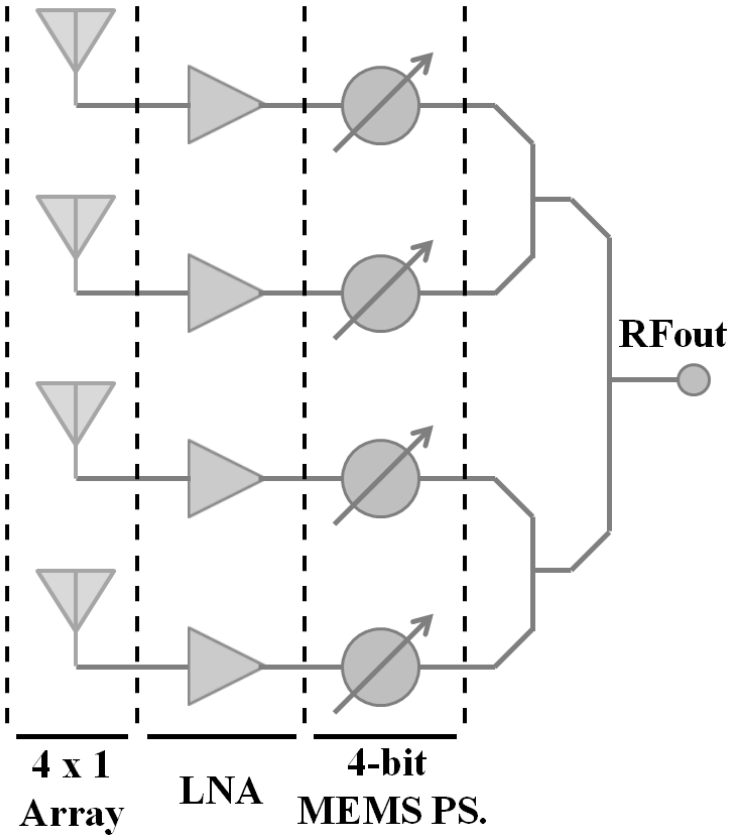

Fig. 39: A 4x1 phased array receiver structure using 4-bit MEMS based phase shifters

In this system, each antenna is followed by an LNA to amplify the RF signal and 4-bit MEMS based digital phase shifter for beam steering purposes. Finally, signals with different phases are combined by Wilkinson power combiners to obtain a single output with desired phase.

5.1.1 Digital Phase Shifter Design Procedure

The designed phase shifters are based on "delayed transmission line" model as shown in Fig. 40. To realize the phase shifts, SPDT (single pole double throw) switches and transmission lines with different lengths are used. The logic behind relative phase shifts ($\Delta\Phi$) could be extracted from the formula:

$$\Delta\Phi = \beta(d_2 - d_1) = \frac{2\Pi(d_2 - d_1)}{\lambda} \tag{20}$$

where β is the propagation constant of microstrip transmission line, λ is the wavelength and d_1 and d_2 are the lengths of transmission lines. Therefore by adjusting the lengths between SPDT switches and by switching between these possible paths, required phase shifts could be obtained (see Section 4.2.1).

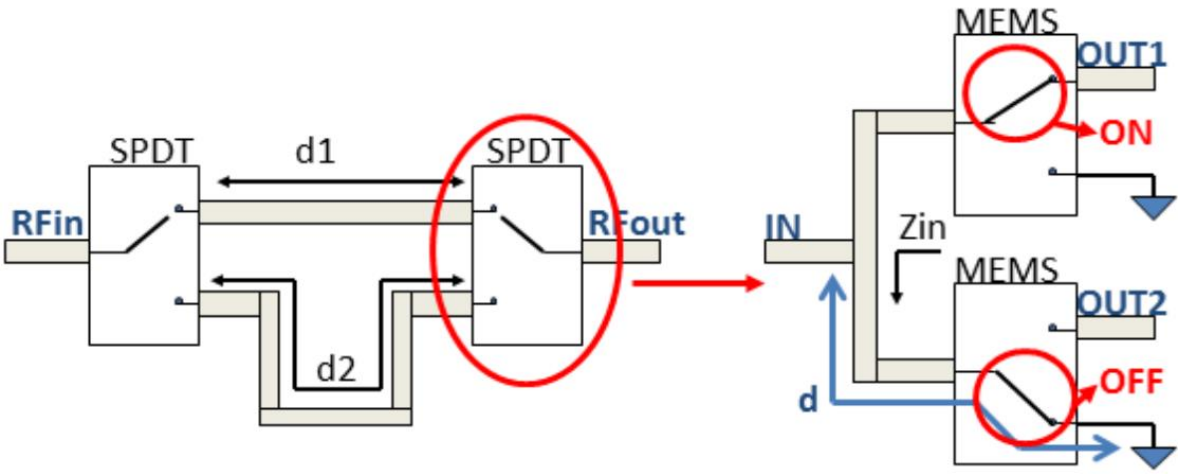

Fig. 40: Phase shifter topology based on delayed transmission line model

Each SPDT switch is also composed of two MEMS switches. If one of the switches is "off", then the other one should be "on" for the RF signal to follow the correct path. Furthermore the lengths of transmission lines which are used right before MEMS switches are critical. This is shown as d in Fig. 40. When the switch is down, the microstrip line section should act as a quarter wave transformer by setting Z_{in} to a very high impedance. By this way, there would be no reflected signals from the isolated path which may cause loading on the actual signal path and increase the insertion loss. Therefore d should be exactly $\lambda/4$ of quarter wavelength.

5.1.2 RF MEMS Switch

IHP RF-MEMS switches with layout model shown in Fig. 41 are used in SPDT blocks. They are embedded into the back-end-off-line (BEOL) of the 0.25µm SiGe BiCMOS process and are composed of a signal transmission line which carries the RF signal and a grounded membrane which moves with the applied voltage due to electrostatic force.

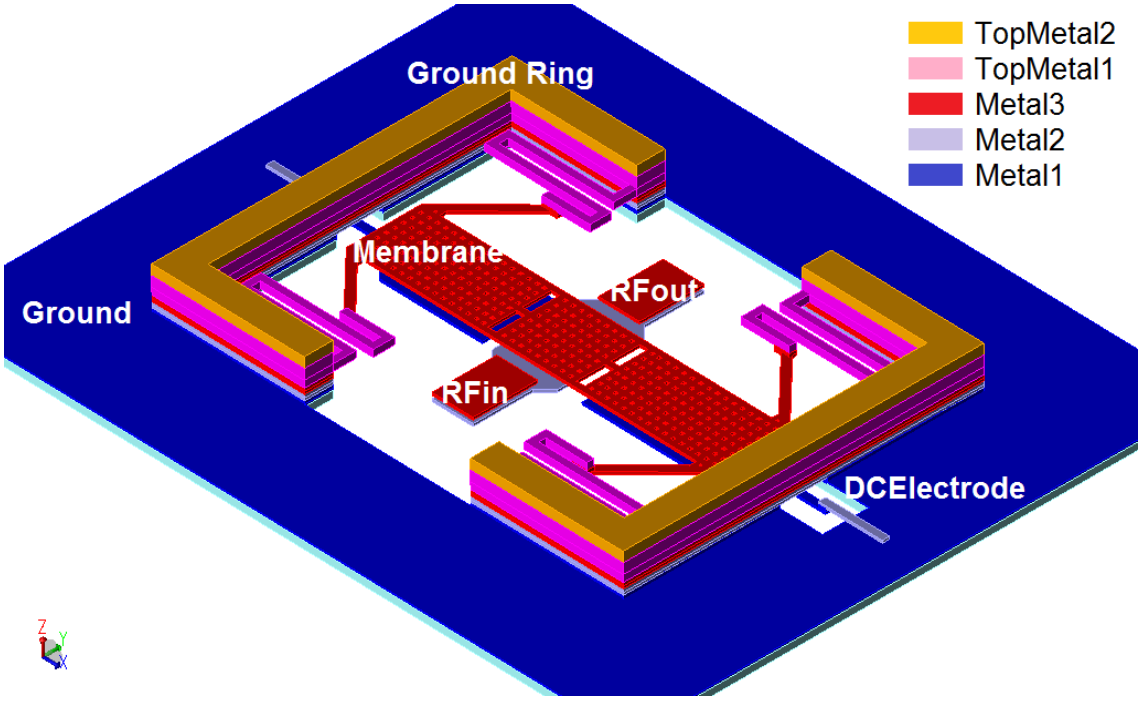

Fig. 41: IHP RF MEMS switch designed for 80GHz

The working principle of the shunt switch is that, in the "on" state, the capacitance between membrane (Metal3) and the RF signal path (Metal2) is very low, so that signal may be transmitted with a very low insertion loss. However, in the "off" state, membrane moves down with the applied voltage and this increases the capacitance (between Metal3 and Metal2) significantly so that signal transmission would not be possible. As a result, RF signal is isolated. The lengths of transmission line springs which are suspended to membrane and connected to ground ring (through TopMetal2 to Metal1) are also designed to provide the highest isolation at 80GHz.

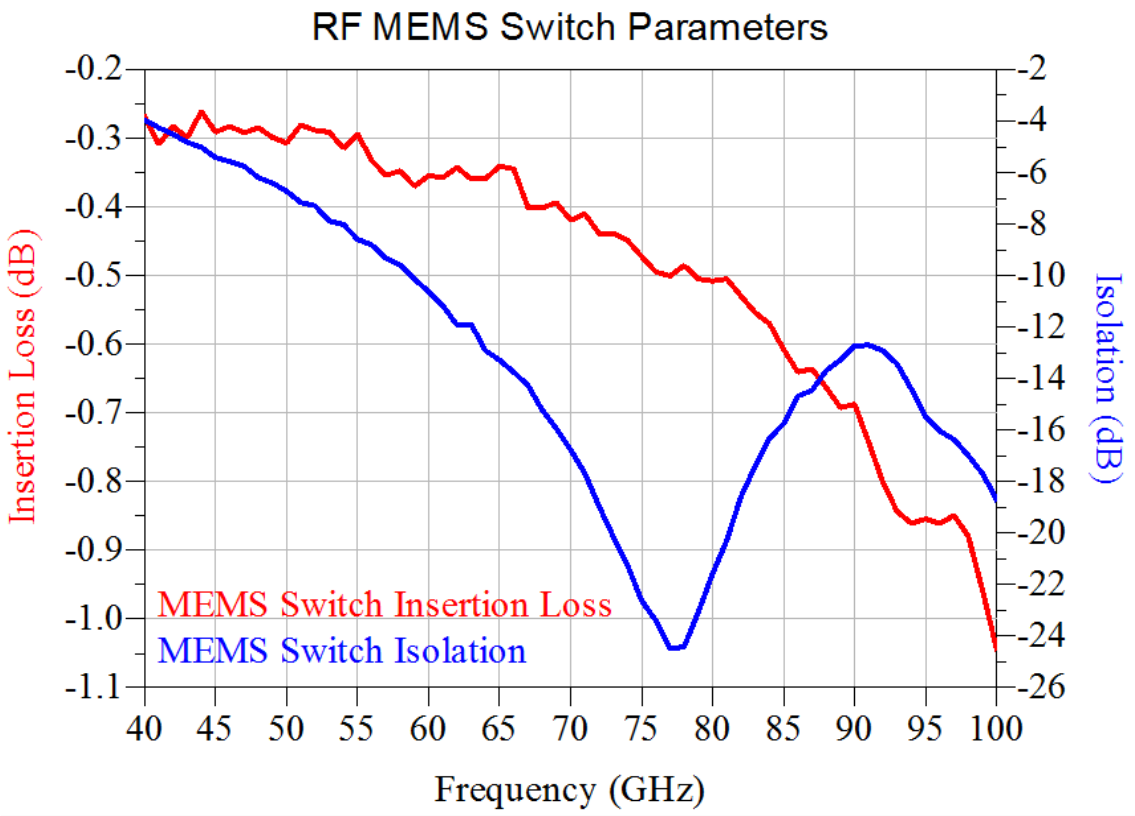

Fig. 42: IHP RF MEMS switch performance parameters

According to results shown in Fig. 42, over 20dB isolation in the "off" state and 0.5dB insertion loss in the "on" state are observed. To decrease the losses coming from the transmission circuit further, the most top metal layer is used as signal path and then MEMS switches are combined through vias.

5.1.3 Designed LSB & MSB Phase Shifters

After completing two different phase shifting blocks by adjusting transmission lines between MEMS switches, they are serially combined to change 2 bits in total, which is highlighted on the fabricated chips in Fig. 43-44. Integrating 22.5° and 45° phase shifting blocks will provide 90° of phase coverage (0° – 22.5° – 45° – 67.5°), while 360° (0° –90° – 180° – 270°) could be spanned by integrating 90° and 180° blocks, which are called LSB (Least Significant Bit) and MSB (Most Significant Bit) phase shifters respectively.

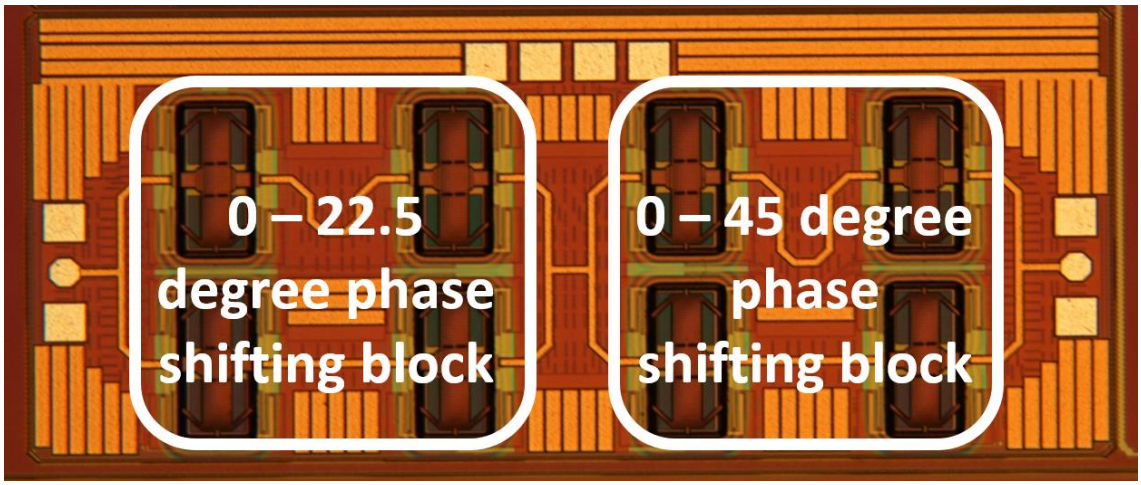

Fig. 43: Fabricated LSB phase shifter chip (2mm x 0.9mm)

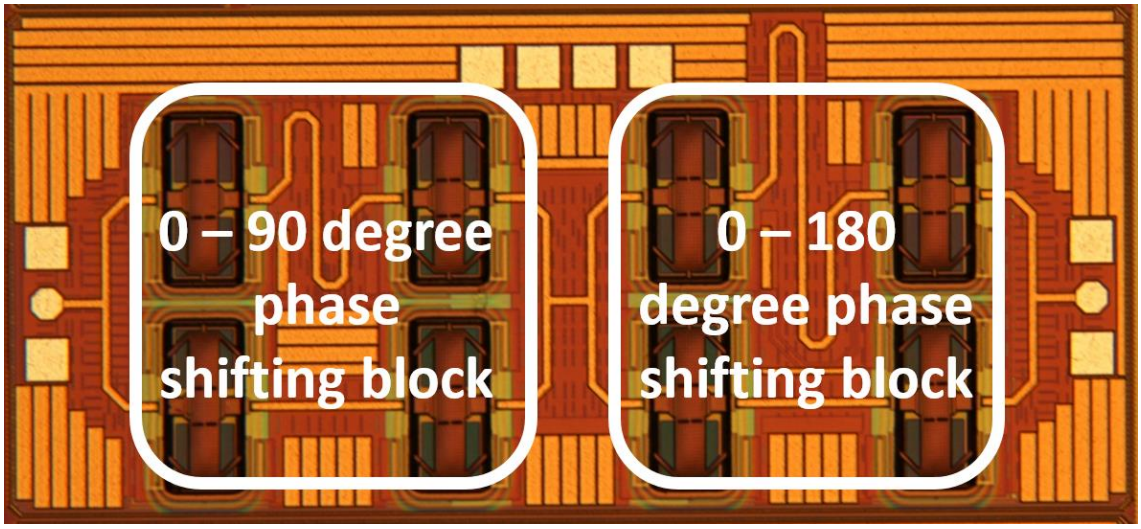

Fig. 44: Fabricated MSB phase shifter chip (2mm x 0.9mm)

In each phase step, RF signal is forced to follow one of the four different paths in each phase shifting block. In order to make one path "off" of "isolated", 40V is applied to MEMS control pads so that signal will be grounded through MEMS switch with the ring that encapsulates it. With the same logic, the signal will flow through the switch by applying no voltage to DC pads, and as a result, insertion between input and output would be possible with a very low insertion loss.

The symmetric placement of the MEMS switches improves the impedance matching and cancels out the undesired reflections with the quarterwave transformers. Using IHP SG25H1 technology, the difference between phase shifting lines becomes approximately 130µm (22.5° phase shifting lines) and 520µm (90° phase shifting lines) for LSB and MSB phase shifters while keeping the microstrip line width 15µm in order to achieve 50Ω of characteristic impedance (Z_o). Designed phase shifters occupy an area of 2mm x 0.9mm. To attain the lowest possible loss from the paths, the microstrip transmission lines are drawn in the most upper metal layer of the technology (TopMetal2) which has a thickness of 3µm and a height of 9.74µm above the ground plane (Metal1), and MEMS switches are combined through vias.

5.1.4 Simulation Setup

Simulations are completed using Agilent ADS simulation software. To obtain simulation results, measurement based switch parameters are loaded into the relevant data blocks in ADS and are combined with full EM simulated layout of the transmission circuit.

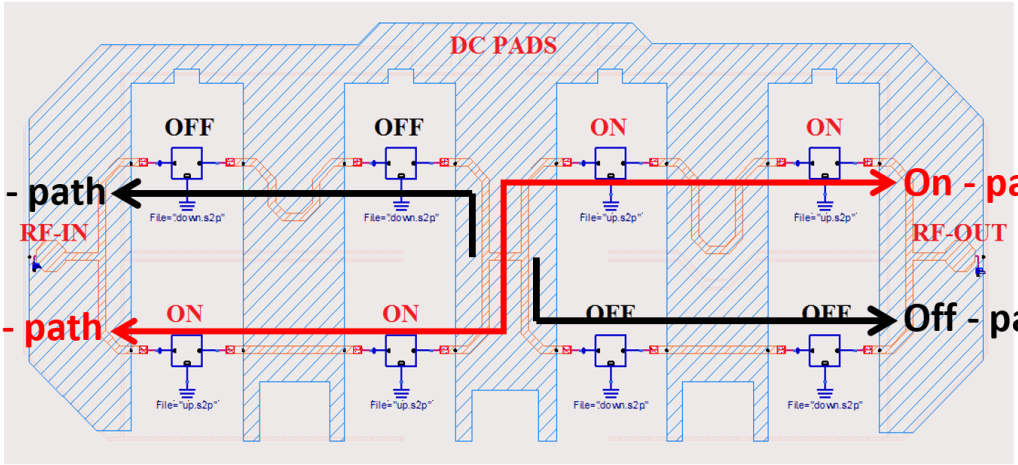

Fig. 45: Simulation setup of one of the possible phase states (45°) in LSB phase shifter

In Fig. 45, simulation setup of one of the possible LSB phase states is shown. RF signal will flow using the path highlighted in "red", and has 45° of phase shift. All the switches on that path are loaded with "on" case switch parameters as seen in the figure. The "black" paths,

however, show the "off" path or "isolated" paths and switch data blocks are loaded with "off" case parameters of the fabricated switch. In order to simulate the other phase states, all the possible data block combinations have been manipulated by switching between "on" and "off" case S-parameters.

5.1.5 Simulation & Measurement Results

When measurement results are obtained after fabrication of the phase shifters each occupying an area of 1.8mm^2, they are compared with simulation results. According to simulation results, insertion loss of 6dB and 7dB should be obtained in average for 4 different phase states at 77 GHz respectively for LSB and MSB phase shifters as shown in Fig. 46-47. However measurement results show higher insertion losses. About 2dB loss increase is observed for both of the phase shifters and 8.5dB insertion loss is achieved in average.

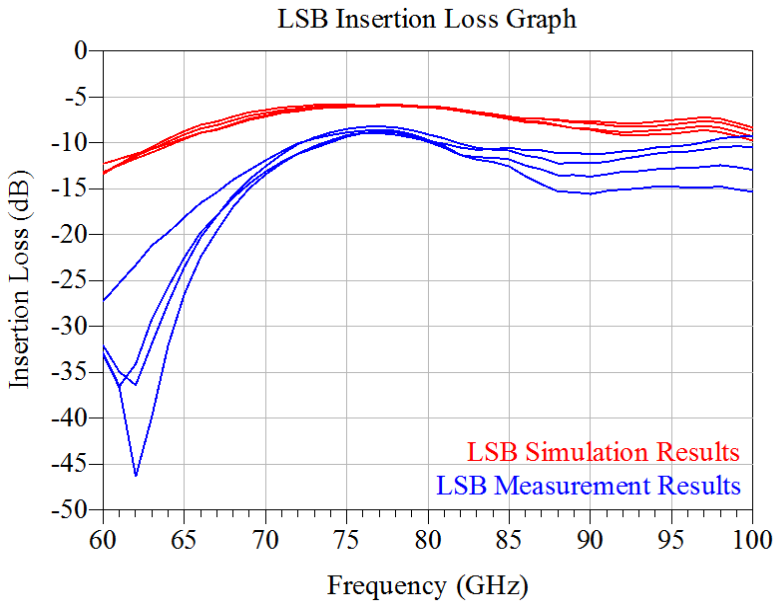

Fig. 46: LSB simulated and measured insertion loss results

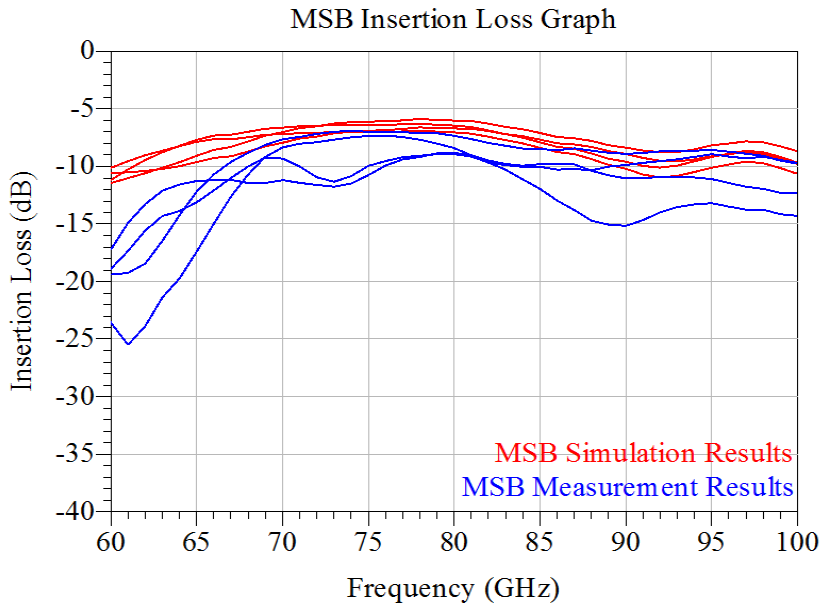

Fig. 47: MSB simulated and measured insertion loss results

For the input and output matchings, simulation and measurement results are almost parallel. As seen from the results in Fig. 48-49, return loss for all the states are better than 10dB and well-matched at 77GHz. The phase shifters are also working in a 10GHz bandwidth from 70GHz to 80GHz.

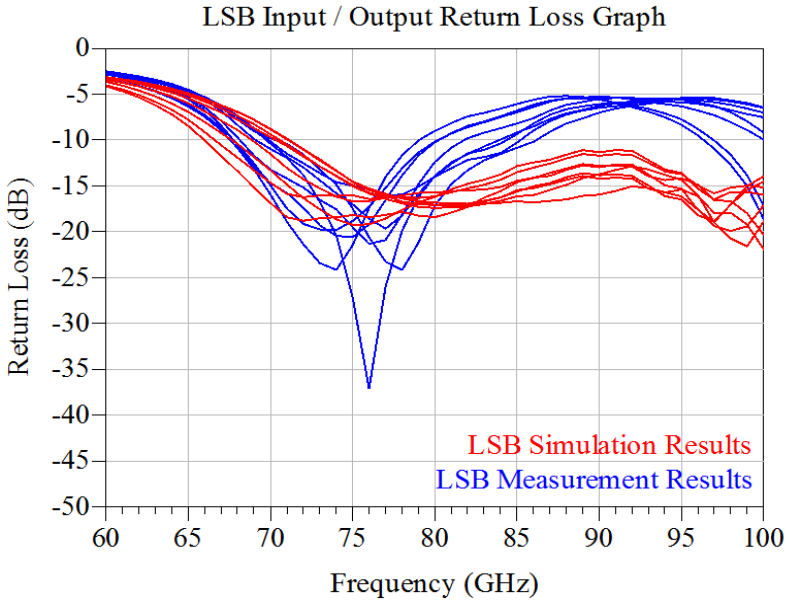

Fig. 48: LSB simulated and measured return loss results

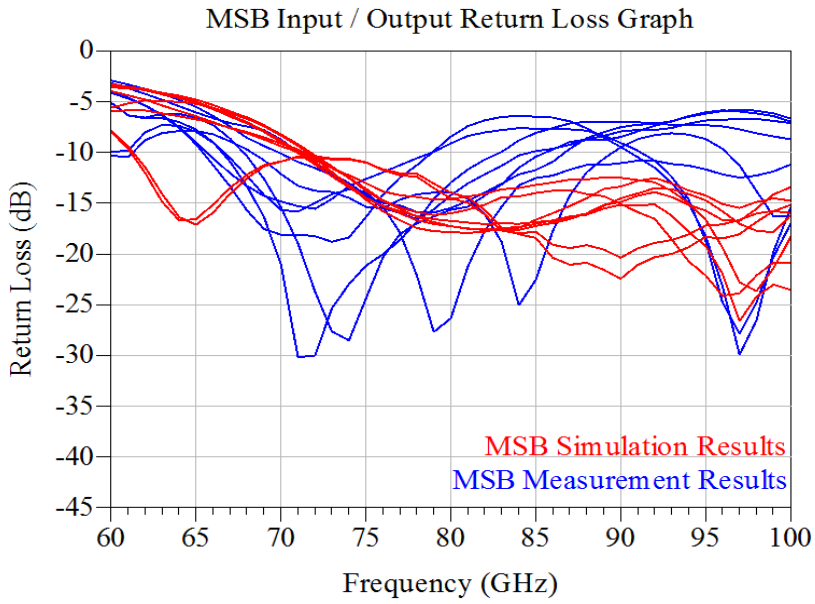

Fig. 49: MSB simulated and measured return loss results

Measured phase error performances of the chips are also parallel with the simulations as depicted in Fig. 50. In the simulations, 1.5° and 2° of phase deviation in average are observed respectively for LSB and MSB blocks. On the other hand, 3.5° and 10° of phase errors are measured.

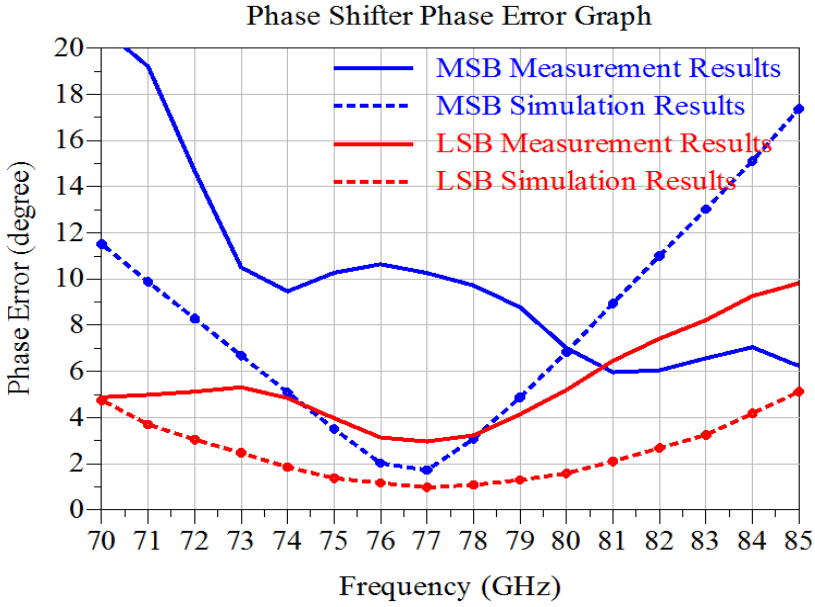

Fig. 50: LSB and MSB simulated and measured rms phase error graphs

Phase errors can easily be compansated by adjusting the transmission lines between switches. As the phase states of phase shifters in Fig. 51 are analyzed, it is obvious that correct results are achieved. Looking at the patterns, 90° and 360° can clearly be spanned with 22.5° and 90° of phase increments for LSB and MSB phase shifters.

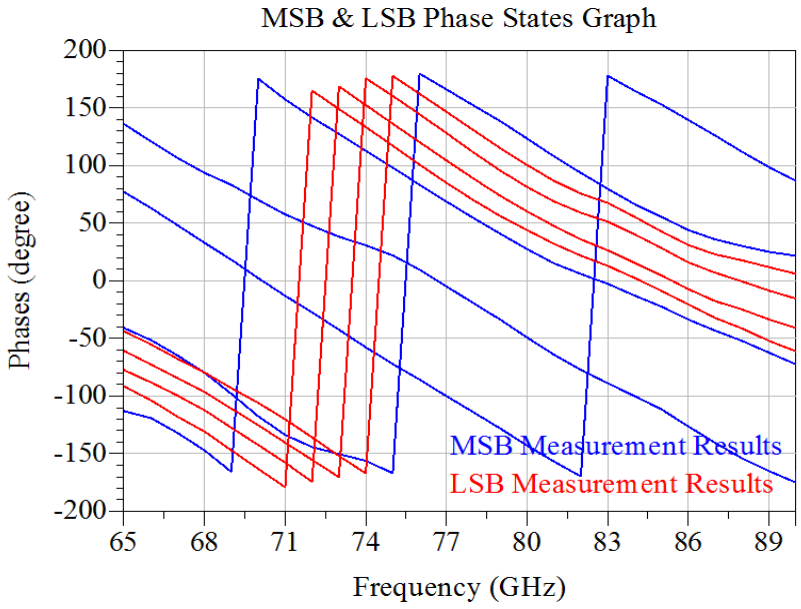

Fig. 51: LSB and MSB measured phase states graph

5.1.6 Design of 4-bit Digital Phase Shifter & Simulation Results

The large die size, so the high cost, prevents the fabrication of a single integrated radar chip. However the 4-bit structure in Fig. 39 is simulated and results are shared in this section.

Since 4-bit phase shifters are required, the fabricated 2-bit LSB and MSB blocks are serially combined to obtain a 4-bit phase shifter which spans 360° with 22.5° phase shifts in 16 steps. Simulation results are shown in Fig. 52-53.

According to simulation results, input and output return losses for all 16 phase states are found above 10dB (see Fig. 52). Minimum 11dB of output return loss is achieved at 77GHz. In Fig. 53, simulated insertion loss graph is presented. Using this data, the loss seems to vary between 15.3-18.1dB.

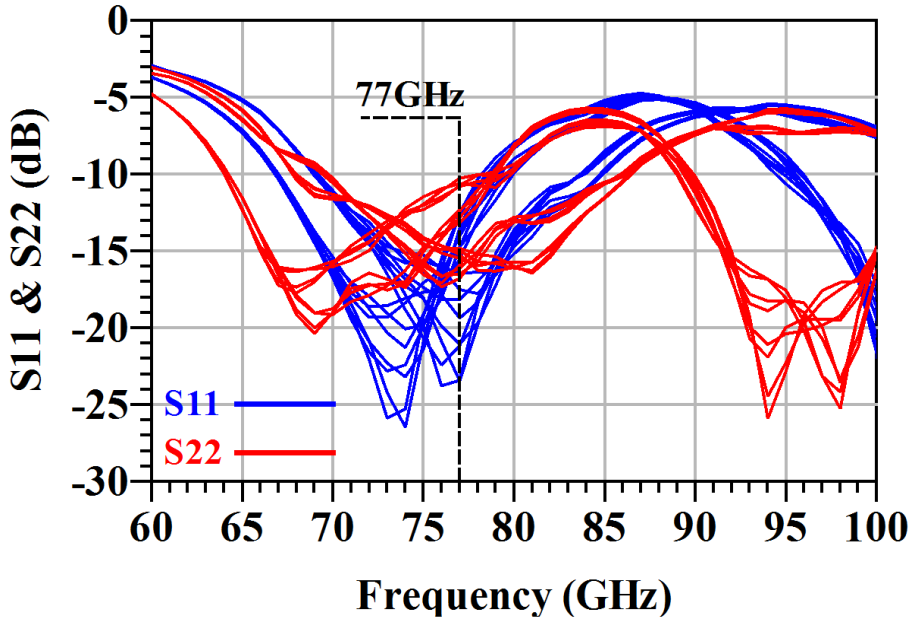

Fig. 52: Simulated input and output return loss of 4-bit phase shifter

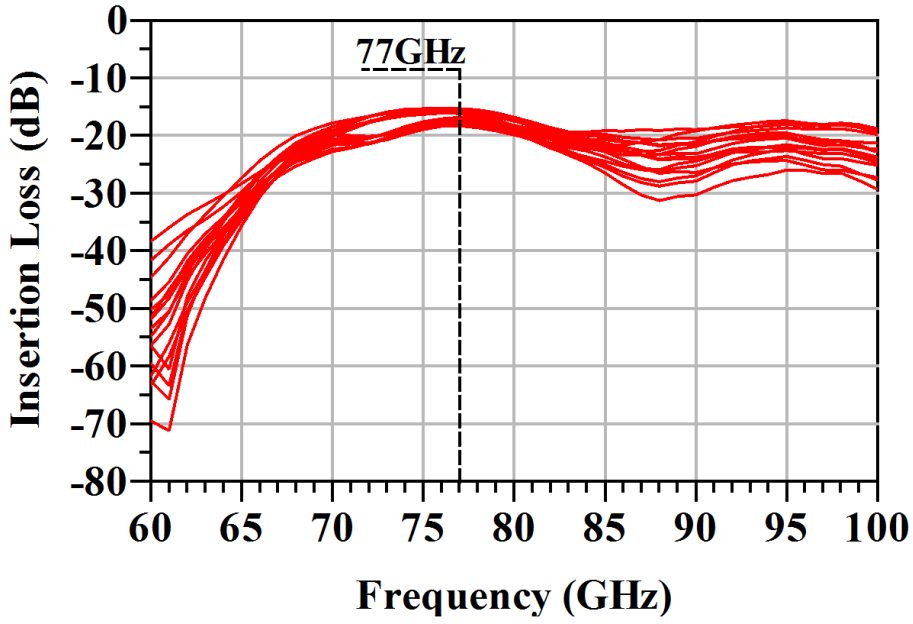

Fig. 53: Simulated insertion loss of 4-bit phase shifter

On the other hand, all 16 phase states of 4-bit phase shifter are shown with their rms error counterpart centered at 77GHz in Fig. 54-55 respectively. In simulations,7.5° of phase error is found at 77GHz.

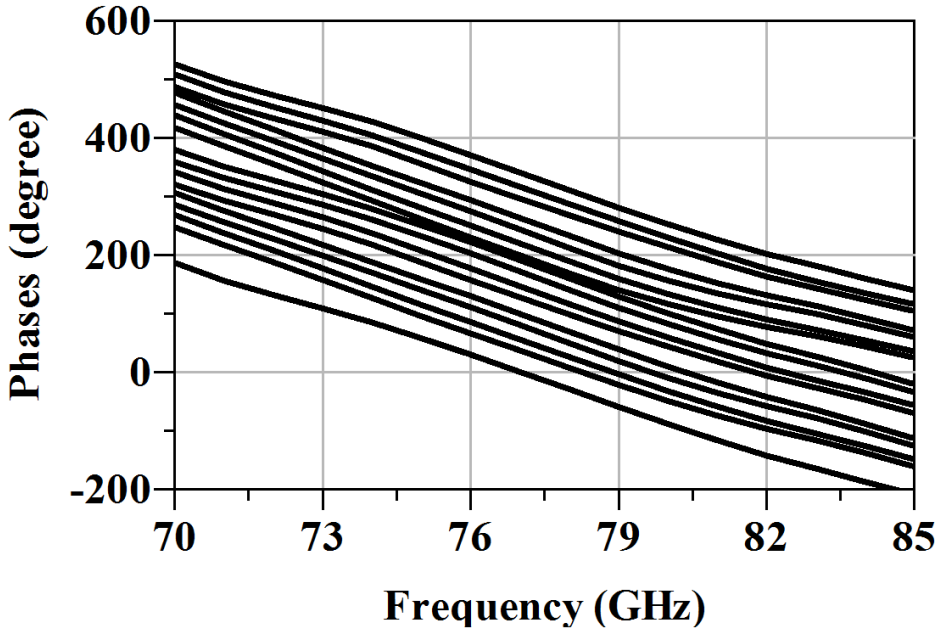

Fig. 54: Simulated phase states of 4-bit phase shifter

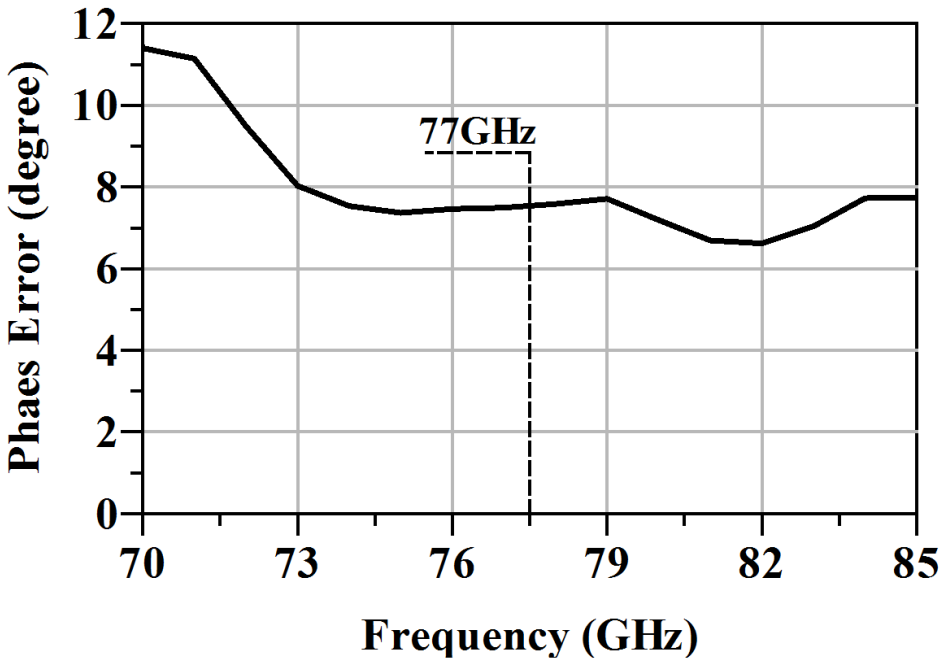

Fig. 55: Simulated phase error graph of 4-bit phase shifter

5.2 Three-Way Active Phase Shifter Design

Although the 4x1 arrayed receiver structure performs well in simulations, the large chip sizes requires to switch to a more compact design. Having a phase shifter with minimal loss and even gain is of paramount importance since at mm-wave band signals are at very low levels due to high losses. Therefore the proposed phase shifter could be used in overall receiver.

Unlike the system in Fig. 39, in this new technique, the spectrum is divided into three equal regions: 0^o – 120^o, 120^o – 240^o, 240^o – 360^o. As seen from the illustration of active phase shifter in Fig. 56, RF signal is split into three with each having same magnitudes and phases shifted by 60^o consecutively, which means that 0^o, 60^o and 120^o of phase shifts exist at the outputs of power divider. The same applies to symmetrical power combiner so that, in total, signals with 0^o, 120^o and 240^o of shifted phases occur at the three branches. By this way 360^o of phase coverage could be attained with the help of controlled gains of LNAs.

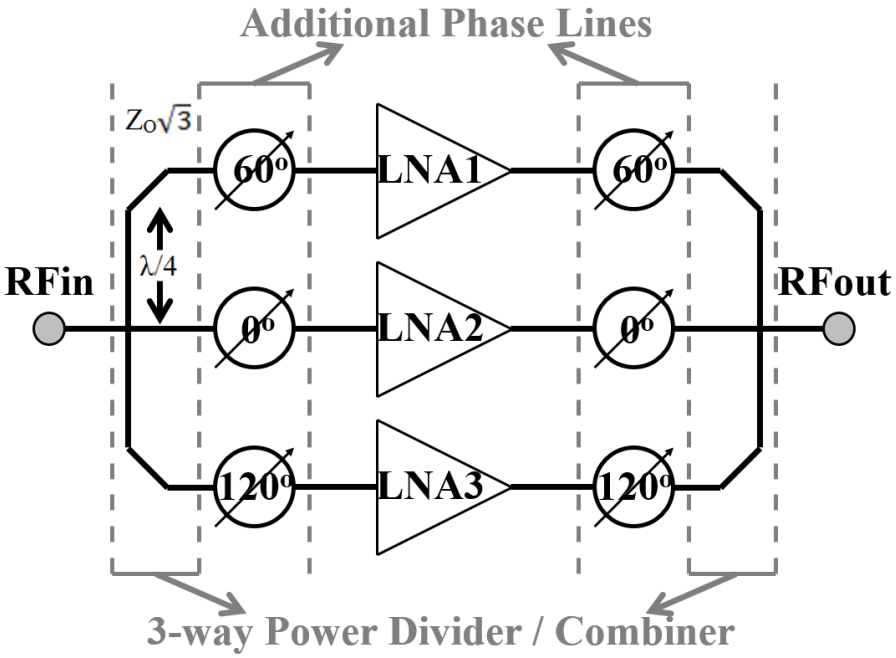

Fig. 56: 3-way active phase shifter structure

Between the power divider and combiner sections, in order to have a desired phase shift at the output, LNA gains should be altered accordingly (see Fig. 57). If it is required to obtain a phase between 0^o – 120^o coverage area, for example, one of the LNAs should be "off" so

that the vectoral addition of the magnitudes of all split signals would reside in that certain area. Furthermore, having one LNA "off" and others with changing gains (with the help of tuned LNA voltages) will guarantee the required area to be spanned due to different vectoral summations. Fig. 58 illustrates all the possible vectoral summations for three different phase regions. Each phase region is determined with one LNA brought to "off" mode.

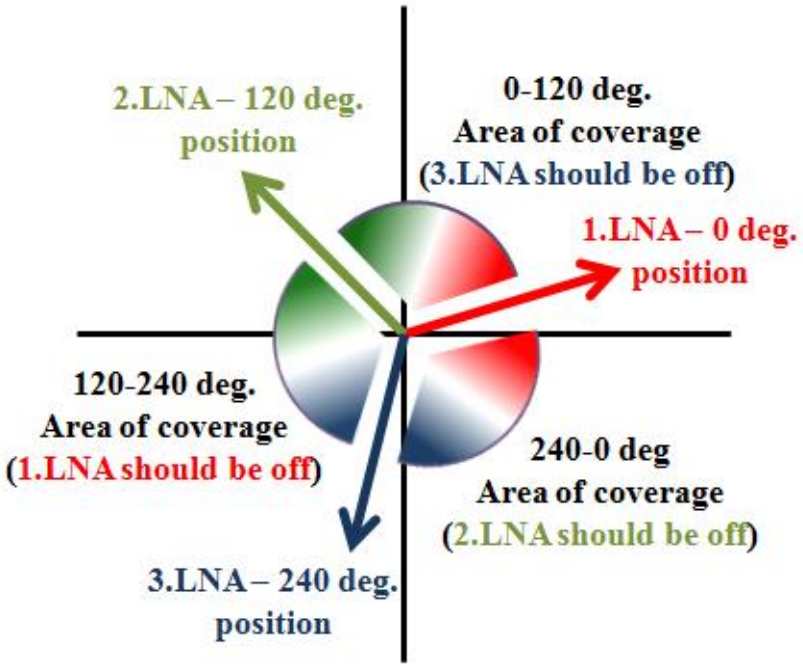

Fig. 57: Active phase shifter working principle

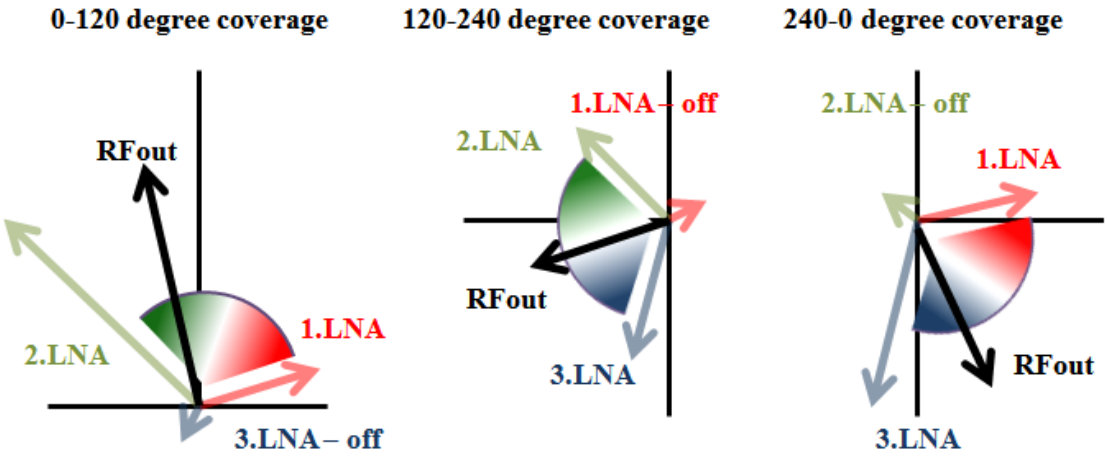

Fig. 58: Active phase shifter states

5.2.1 Active Phase Shifter Design Prodecure

Three-way Wilkinson power divider/combiner structures are placed at the ends of amplification stages as shown in order to have three vectors as shown in Fig. 59. Whereas power division is realized in the first section, latter microstrip transmission lines with certain lengths are integrated to provide the desired phase shifts to the three vectors. With the IHP SG13G2 technology, the width of 87Ω ($Z_o\sqrt{3}$) lines become 2.2µm at 77GHz. Furthermore, 50Ω isolation resistors are placed between the outputs which are not shown in the figure. The divider is combined with additional 15µm-width (Z_o) transmission lines to provide 0°, 120° and 240° phase shifts for the three vectors after integrating symmetrical power combiner.

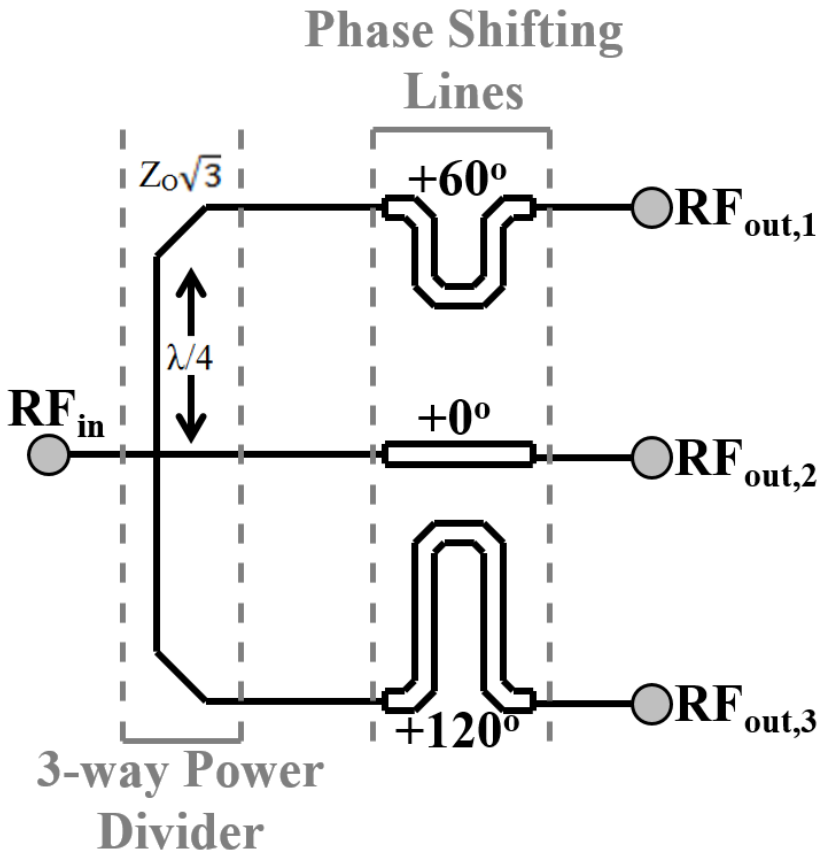

Fig. 59: Three-way Wilkinson power divider/combiner structure

Measurement results of the power divider excluding the phase shifting lines are shown in Fig. 60. Using this data, it is seen that input and output are matched above 10dB for the entire W-band with and insertion loss of 5.5dB at 77GHz and 30dB isolation between ports. With

the addition of phase shifting lines, insertion loss increases by 0.5dB maximum for the longest transmission line (for 120° phase). After the addition of phase shifting lines, proper phase states are obtained from simulations as seen in Fig. 61.

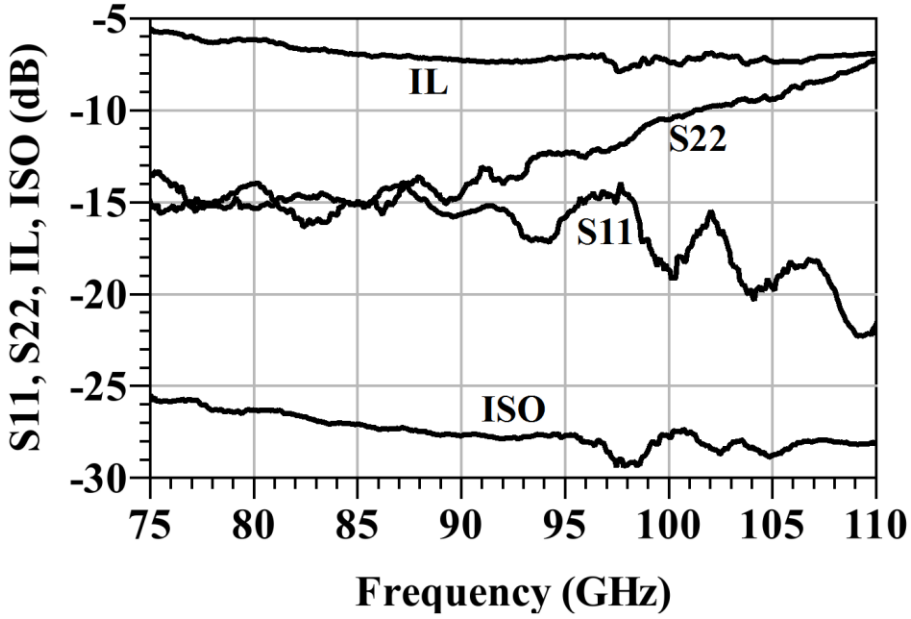

Fig. 60: Measurement results of the fabricated Wilkinson power divider/combiner

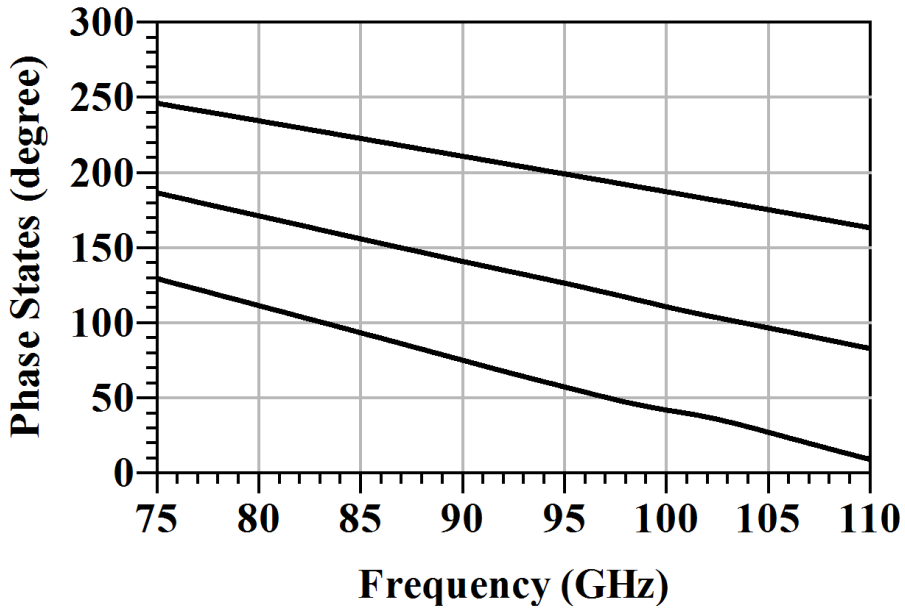

Fig. 61: Simulated phase of each output of Wilkinson power divider/combiner

Having completed the power divison part, the three-stage single-ended ultra-wideband LNA in Chapter 3 is integrated to each branch. However, to increase the stability at the expense of reduced gain and to be able to derive high-power input signals, resistive feedback circuits (30fF + 200Ω) are placed between base and collector ports of HBTs at the second and third stages (see Fig. 62). The overall noise figure is not affected much since the gain of first stage is high enough to suppress the noise of the latter stages.

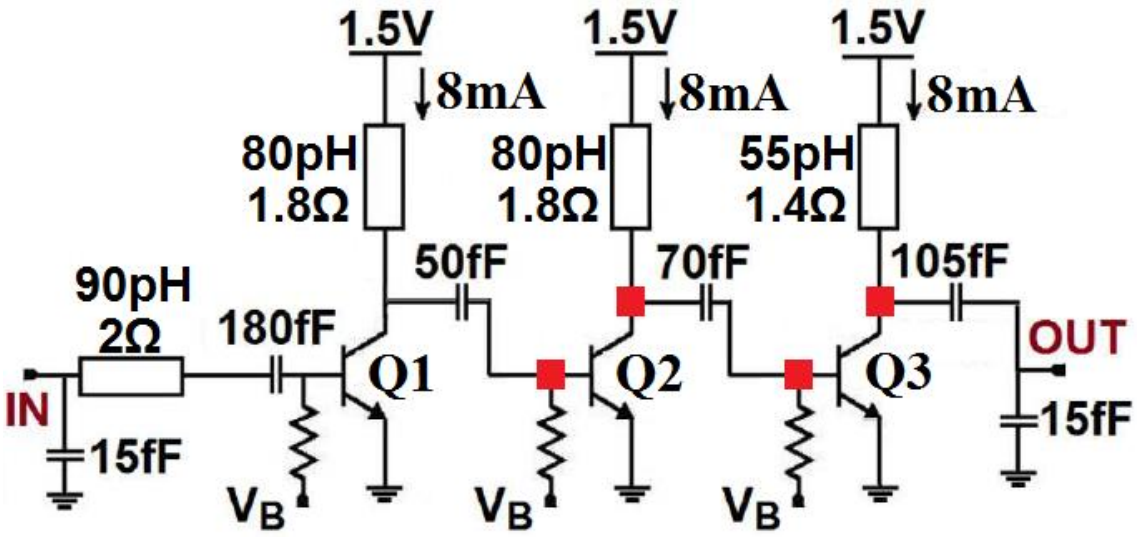

Fig. 62: Schematic of three-stage, single-ended, common-emitter LNA. Red marks show the collector-base feedback points (30fF + 200Ω)

The measurement and simulation results of 0.2mm^2 chip (see Fig. 63) is highlighted in Fig. 64 and revealed that the LNA can be used in the active phase shifter design. According to the measurement results (solid lines), wideband performance is achieved over a 25GHz of 3dB-bandwidth with a peak gain of 12dB at 75GHz as expected from the simulations (dashed lines). Input and output return loss are above 10dB over the entire band with noise figure of 5.8dB and isolation of 40dB at 77GHz. The gain can easily be increased up to 15dB by operating at higher bias voltages at the expense of increased power consumption and noise figure.

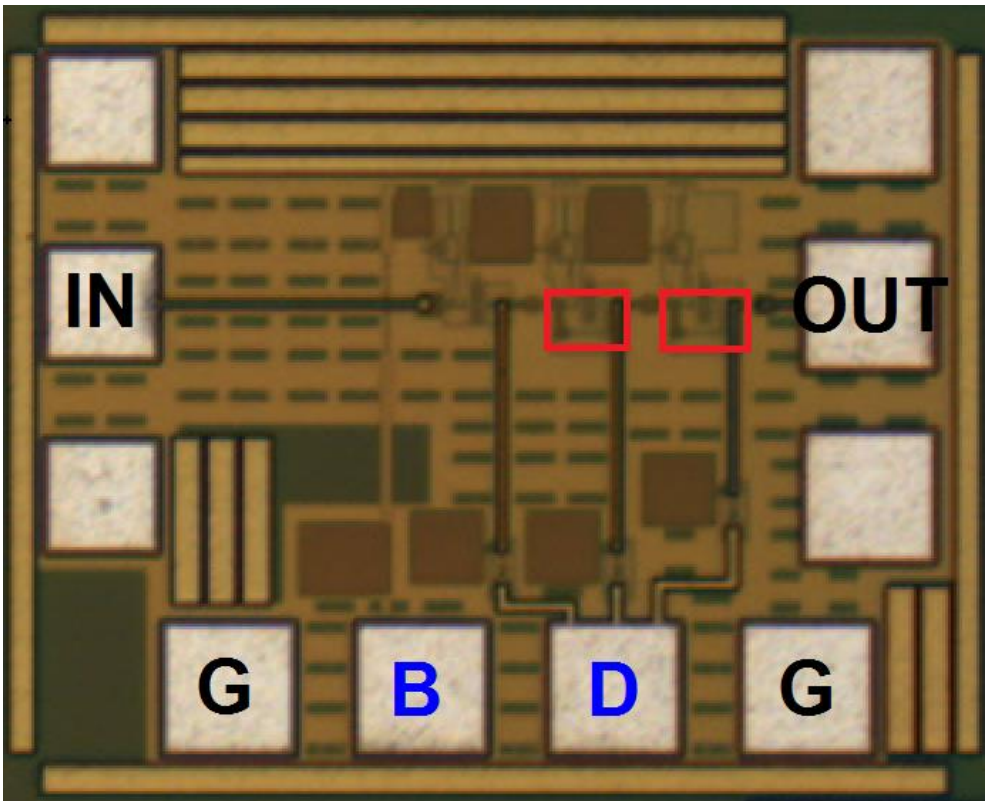

Fig. 63: Fabricated LNA chip (red block indicates the shunt resistive feedback)

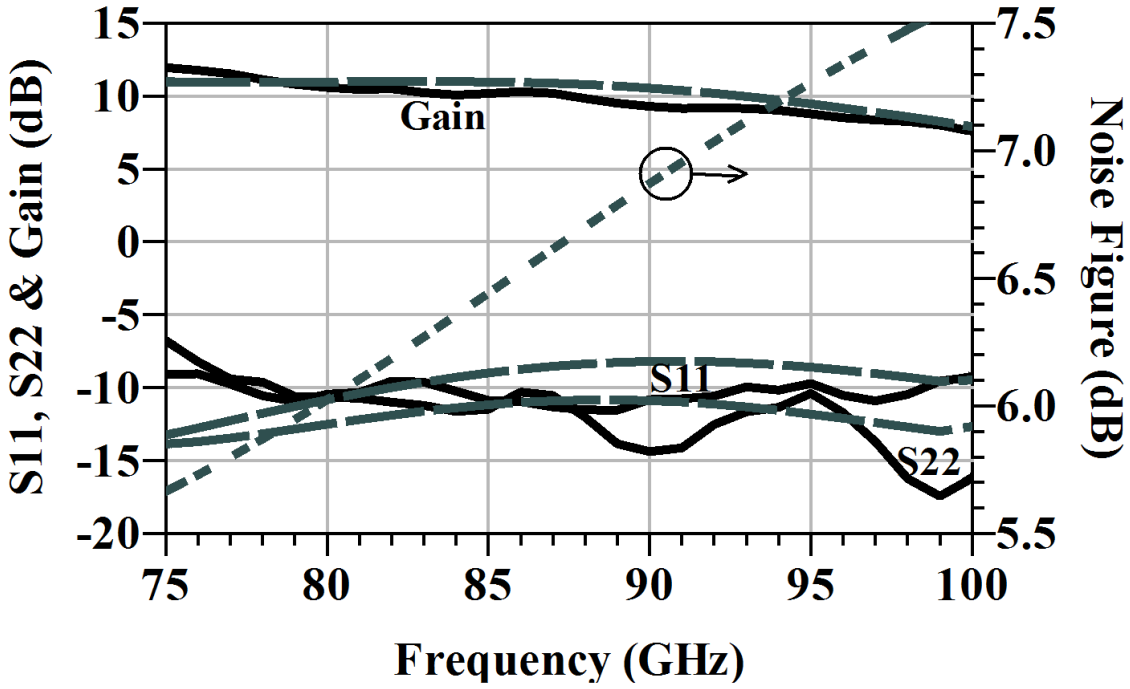

Fig. 64: Measurement and simulation results of the fabricated three-stage LNA

5.2.2 Simulation & Measurement Reuslts

After completing LNA and power divider/combiner, they are combined on a 1.5mm x 1.1mm single chip to compose the active phase shifter which is shown in Fig. 65. The chip utilizes IHP SG13G2 SiGe HBT technology.

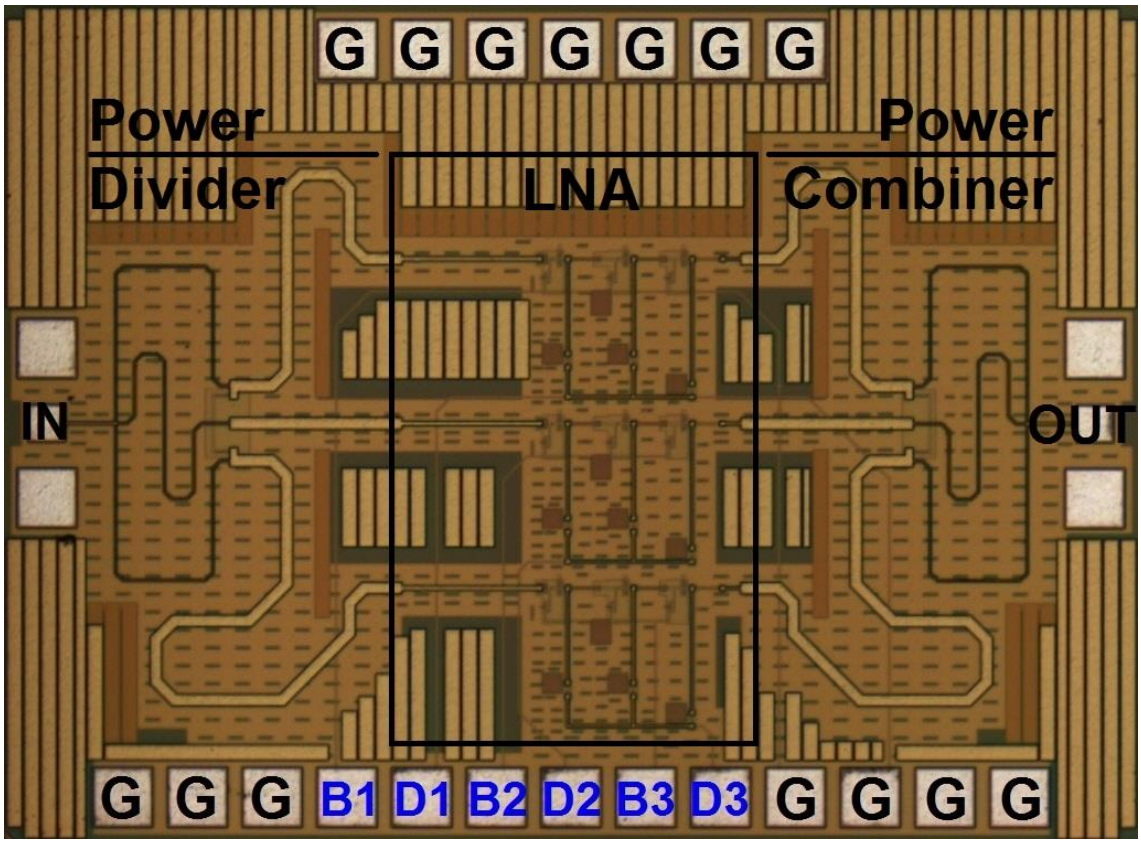

Fig. 65: Fabricated active phase shifter chip

Measurements are conducted in the SUNUM labs (Sabanci University Nanotechnology Research and Application Center) using a PNA 5245A Network Analyzer.

The comparison between measurements and simulations are given in Fig. 66-69. In these figures, input/output return loss and gain performances of the fabricated chip are stated. All the curves in these figures are obtained for different phase shifts which are realized by sweeping the base voltages of the three LNAs simultaneously between 0.8-1.5V (B1, B2, B3 in Fig. 65), where collector voltages are kept constant at 1.5V (D1, D2, D3 in Fig. 64) and one of the LNAs are "off" each time with no voltage applied.

Considering the results in Fig. 66-67, return losses perform well above 10dB for all the simulated phase shifting states throughout the entire W-band. Furthermore, the figures highlight the agreement between measurements and simulations.

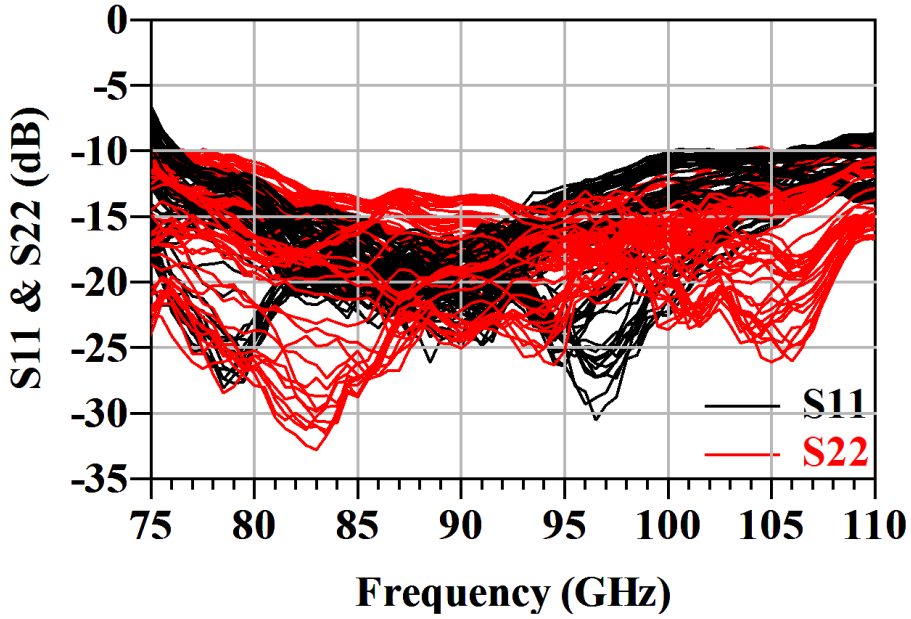

Fig. 66: Measured return loss results of the three-way active phase shifter

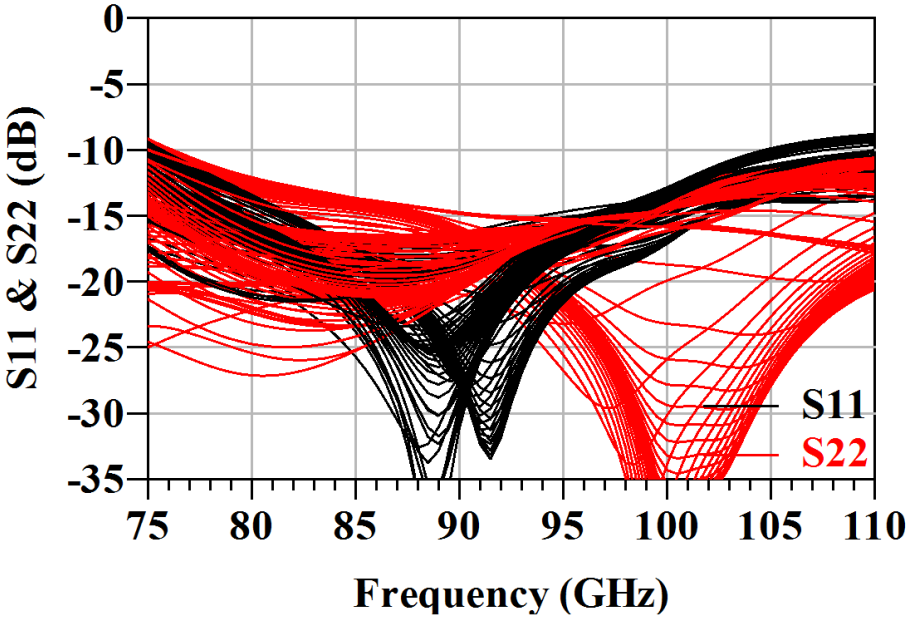

Fig. 67: Simulated return loss results of the three-way active phase shifter

Gain/insertion loss performances are similar to simulation results as shown in Fig. 68-69. However there exists a gain difference which simulation performs 3dB less between 80-85GHz. Using these four figures, it is explicit that the fabricated phase shifter can be used up to 90GHz without incurring any insertion loss. At 77GHz, it reaches maximum 11dB gain.

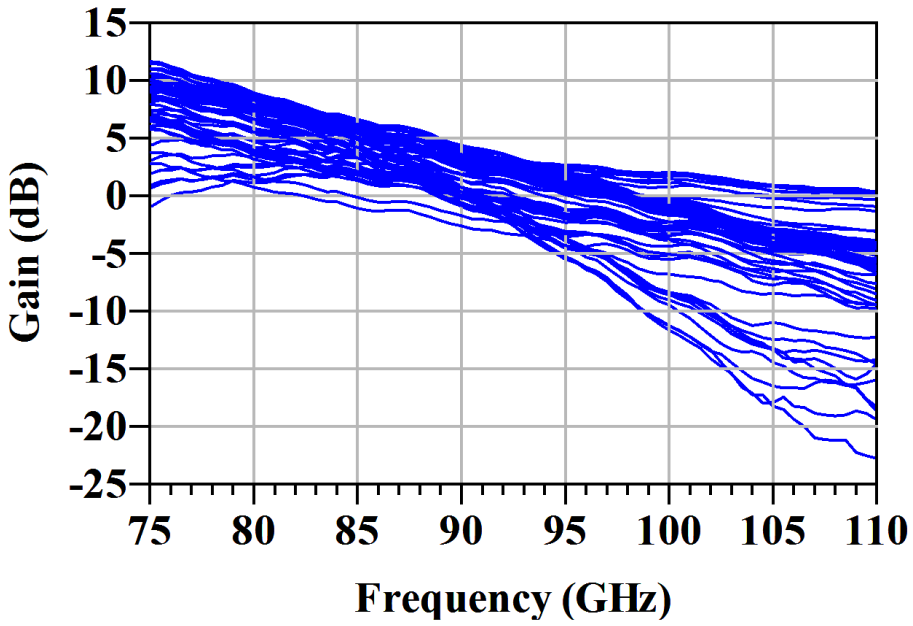

Fig. 68: Measured insertion loss/gain results of the three-way active phase shifter

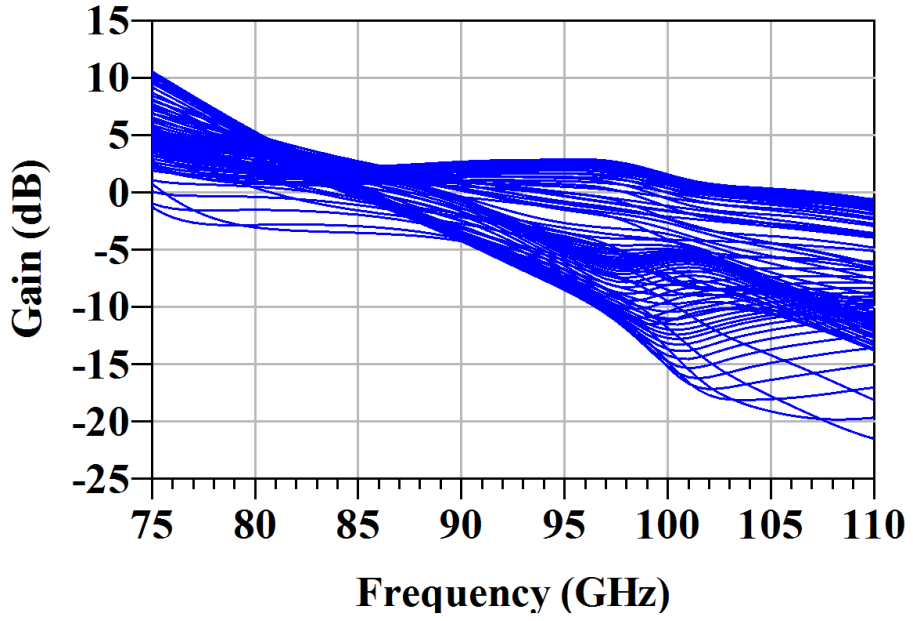

Fig. 69: Simulated insertion loss/gain results of the three-way active phase shifter

In Fig. 70-71, measured phases and related phase error graphs for all the phase states are presented. From Fig. 70, the pattern reveals that the fabricated phase shifter achieves the phase shifts correctly almost for the entire W-band.

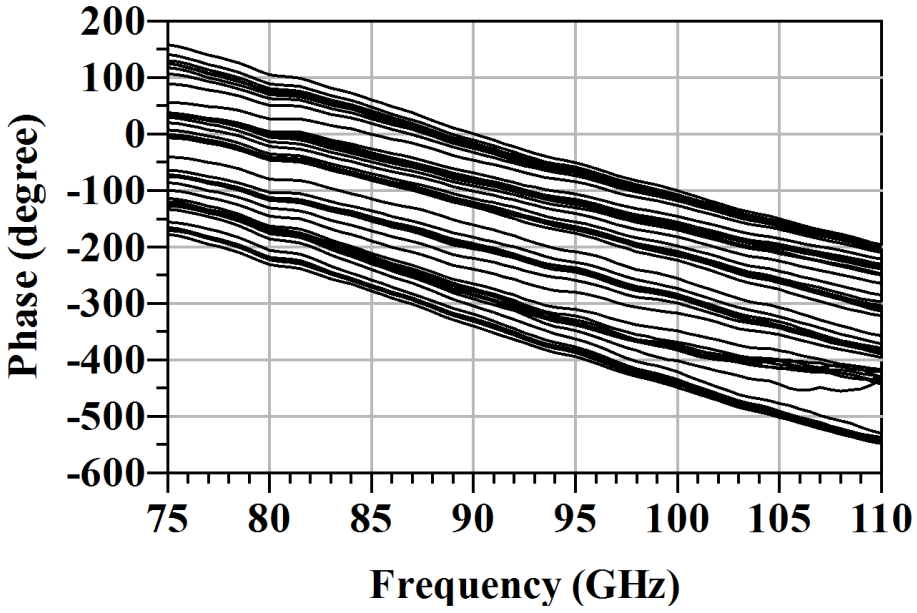

Fig. 70: Measured phase states graph of the three-way active phase shifter

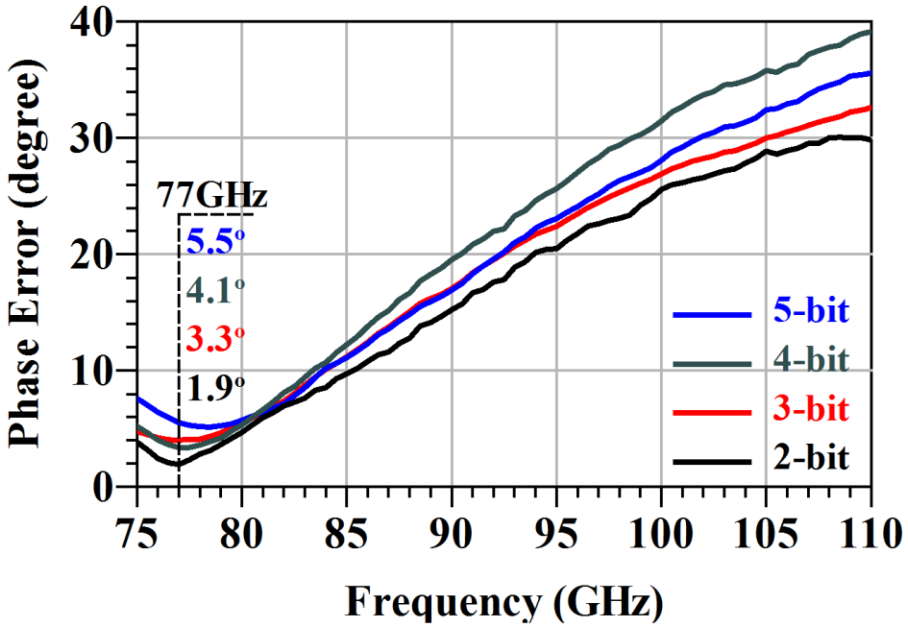

Fig. 71: Measured 2, 3, 4 and 5-bit rms phase errors of the three-way active phase shifter

However for a more appropriate analysis, Fig. 71 which shows the relative rms phase errors in case of the usage of phase shifter for 2, 3, 4 and 5-bit operations is presented. Using this graph, 1.9°, 3.3°, 4.1° and 5.5° of phase errors, relatively, are found at 77GHz. It is important to note that these errors are calculated from phase states achieved by 50mV steps so that, for digital operation, decreasing this voltage tuning step and having more states point out a wider bit resolution.

5.3 Two-Way I/Q Type MEMS Based Active Phase Shifter Design

Compared to previous designs, an I/Q topology is adopted in this phase shifter design which benefits two LNAs. Moreover, 1-bit phase shifter (0°/180°) is of switched-line type that uses MEMS switches to select between different length transmission lines is integrated at each branch with LNA. As a result, gain can be extracted out of this design as opposed to commonly studied passive phase shifters which introduce additional loss.

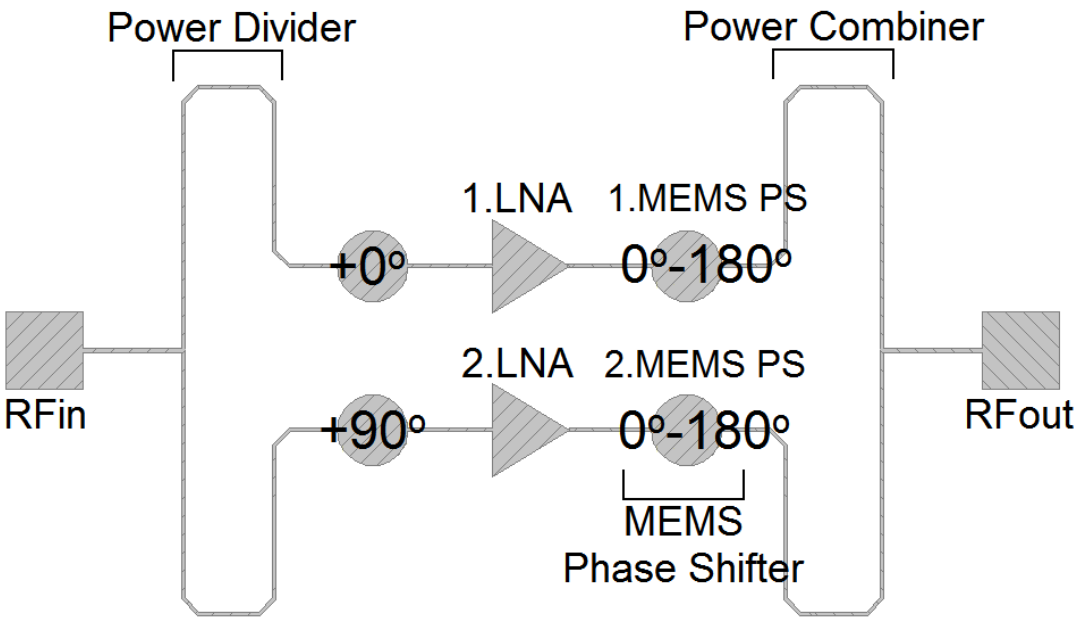

Fig. 72: Two-way active phase shifter structure

As seen from Fig. 72, RF signal is split into two with each having same magnitudes. However phases are shifted by 90° consecutively by using phase shifting lines, which means that 0°

and 90° of phase shifts exist at the two branches. This is done to get a 90° of phase coverage alone without the one-bit MEMS phase shifters by using LNA gains, as shown in Fig. 73a.

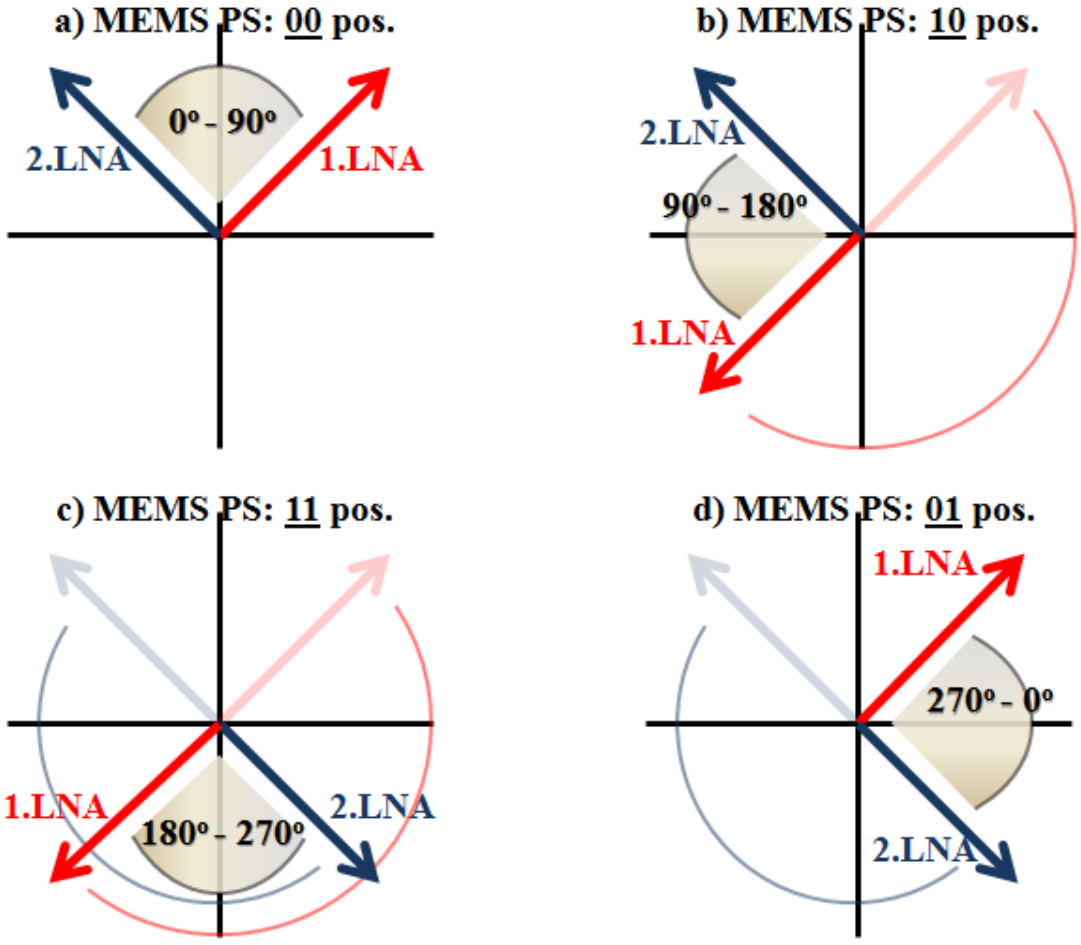

Fig. 73: Two-way active phase shifter working principle

To spread the phase coverage to 360°, the structure makes use of 1-bit MEMS phase shifters. As seen from the images in Fig. 73b, c, d, the phases in two branches are shifted by 180° separately so that 4 phase states occur in 360° of coverage. Between the power divider and combiner sections, in order to acquire a desired phase shift at the output, LNA gains should be changed. If it is required to obtain a phase between 180° – 270° area, for example, both 1-bit MEMS phase shifters should be brought to "on" mode (11 mode as in Fig. 73c) to enable 180° additional phase shifts to both branches. As a result, the desired area could be spanned with the help of LNAs. In this context, each different vectoral addition of gains of LNA1 and

LNA2 (see Fig. 72) could lead the phase of RF signal to reside in different position in that coverage area (see Section 4.2.3).

5.3.1 Design Procedure

The LNAs to be used in an active phase shifter should have enough gain range to provide clear quadrant sweeps as was in the three-way active phase shifter structure. For this phase shifter, new LNAs different than the ones in Chapter 3 were designed since the MEMS switches are built on 0.25µm SG25H1 technology. Fig. 74 shows the simplified schematic of designed LNA together with the bias circuitry. The LNA consists of two cascaded stages with two cascode HBTs (IHP-npn200_4) in each stage to increase the total gain. The circuit is biased with 2.5V from both the collector and base terminals and derives 5.4mA current in each stage (1.2mA from bias circuit), hence the total current of 10.8mA.

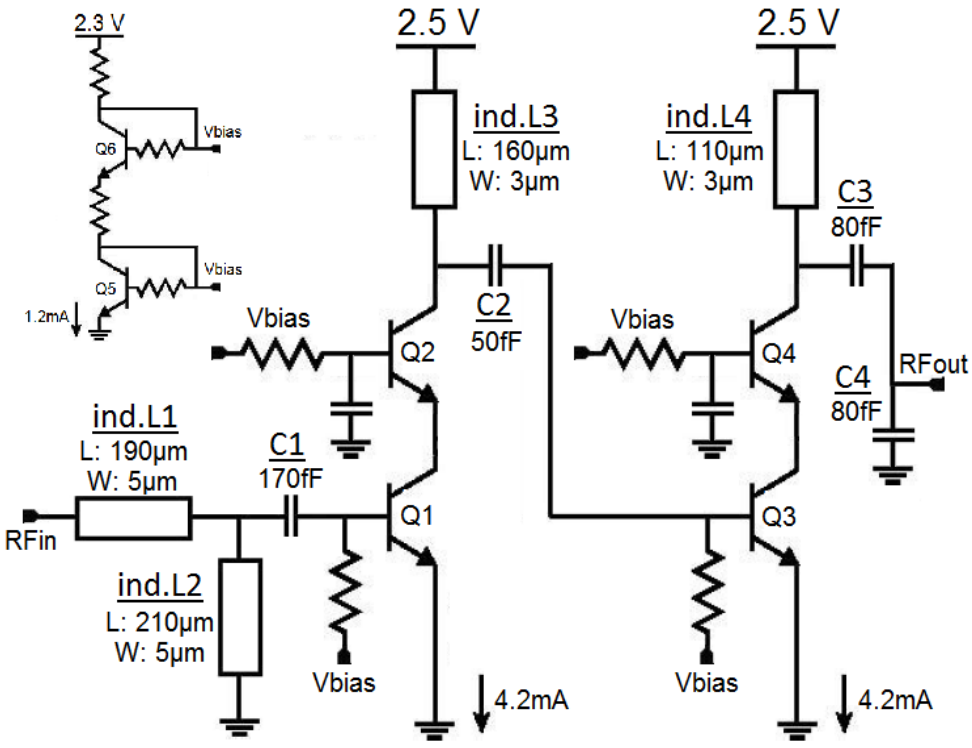

Fig. 74: Two stage cascode LNA schematic with bias circuit

The same optimization procedure was followed in this LNA design, with 5-metal layer technology being the only difference. The common base cascode stage is provided to increase the overall gain with a bit compromise on noise figure. As a result, the full EM-simulated design which occupies 0.21mm^2 of die area (see Fig. 75) was fabricated using IHP SiGe BiCMOS SG25H1 technology.

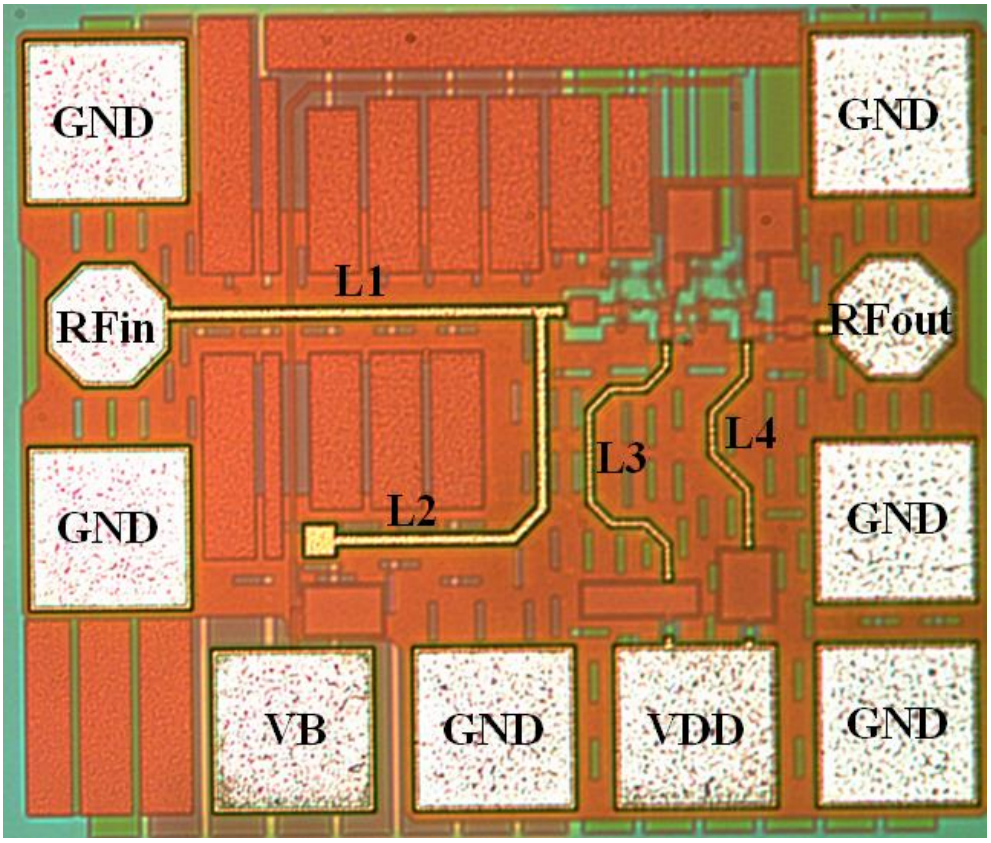

Fig. 75: Fabricated two stage cascode LNA

Fig. 76-77 shows the measurement results for fabricated LNA at 75-110GHz interval. At our frequency of interest (77GHz), the LNA gain changes from 0-14dB by changing base voltages from 1.8-2.3V (VB in Fig. 74). In this measurement, the base voltage tuned with 50mV steps while the collector voltage remains fixed at 2.5V (VDD in Fig. 74).

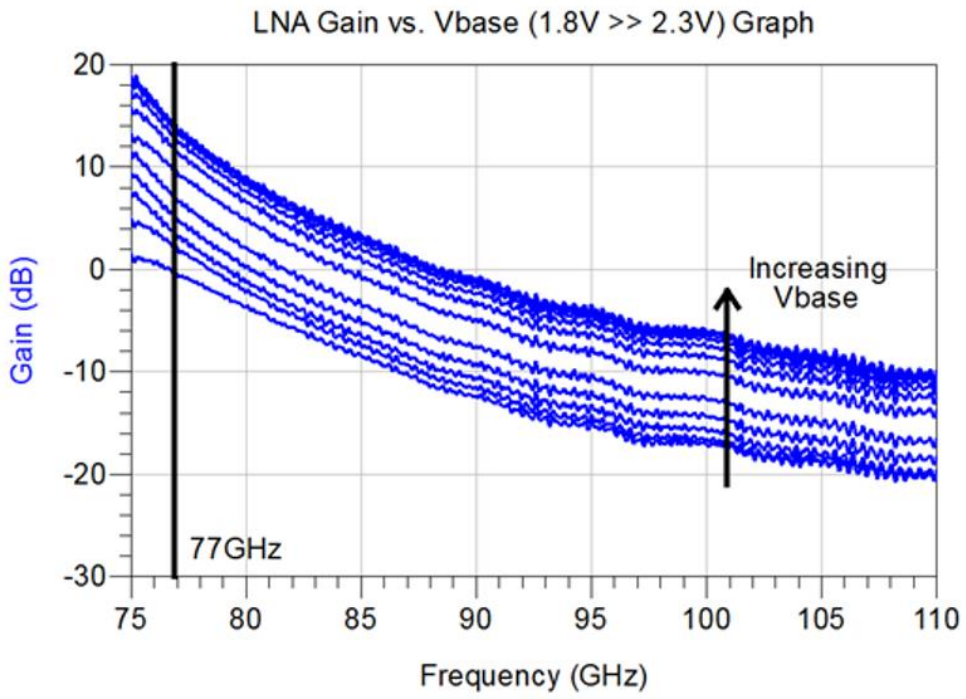

Fig. 76: LNA measured gain vs. base voltage

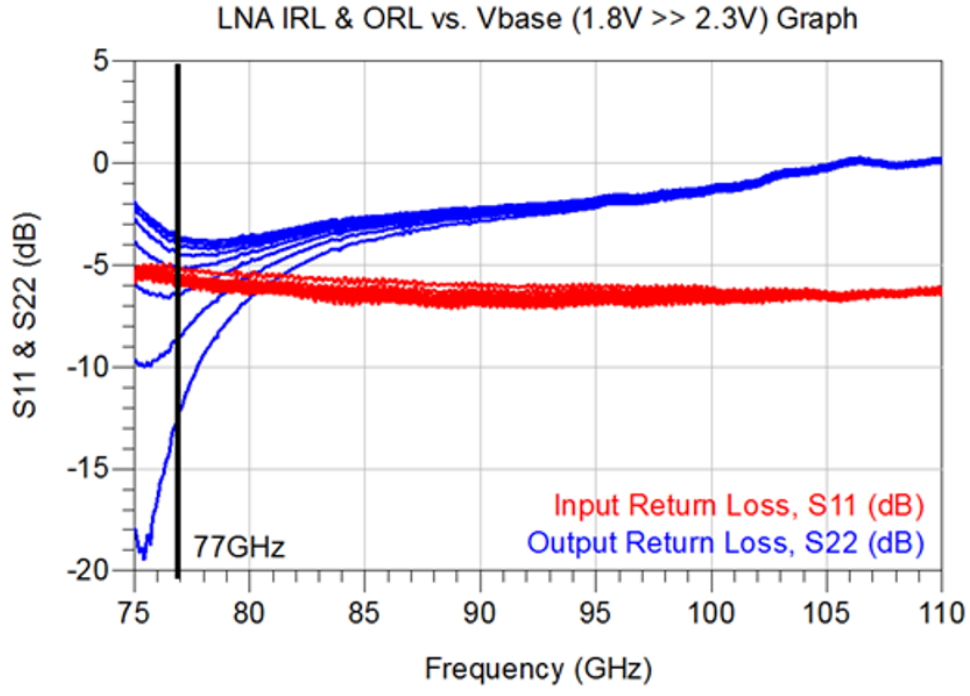

Fig. 77: LNA measured S11 and S22 vs. base voltage

Fig. 77 shows the measured input and output return losses for a single LNA. The input return loss is around 5dB for all values of different gains and the output return loss changes between 3-12dB. Although the additional matching circuitry could be used in the matching of LNAs, the overall system utilizes Wilkinson power divider/combiner which has high isolation between the output ports and will compansate for the performance of the input and output matching of LNAs. This will result in much better return loss for the active phase shifter as will be shown in Fig. 79.

However, it is worth to point out that the gain tuning mechanism works perfectly which is the first necessity for active phase shifter (Fig. 76). Moreover, based on ADS simulation results, the noise figure varies between 9-11dB for base voltages tuned from 1.8V to 2.3V. By using the G2 (0.13um) technology, which was adopted by the previous designs, noise figure levels around 6dB could also be obtained and further LNA gains would be possible. Also in the simulations, $P_{1dB,in}$ point (input referred 1dB compression point) is found as -22dBm at 2.5V bias voltage.

For the 1-bit MEMS blocks to be used at the ends of LNAs, the fabricated 2-bit MSB phase shifter in Fig. 44 (Section 5.1.3) should be divided into its blocks. In this context, only the 0^o-180^o phase shifting block will be integrated to LNAs. As was discussed previously, the average loss of 2-bit block is around 8.5dB, so that it is expected to have 4.3dB of insertion loss for the 1-bit block with input and output well matched to 50Ω. One disadvantage of using MEMS switches instead of other SPDT structures such as FETs and pin diodes is their high chip area.

After having the RF signal from the antenna and before transferring to the latter stages, Wilkinson power divider/combiner structures are utilized. Input signal is split into two basis I & Q vectors and orthognolly shifted by a λ/4 transmission line. Fig. 78 shows this structure. As its three-way counterpart in Fig. 59 (Section 5.2.1), power divider and combiner sections are symmetric. But an extra λ/4 length of transmission line right after the second output to provide 90^o of phase shifts. Using IHP SG25H1 technology, the width of 70.7Ω ($Z_o\sqrt{2}$) transmission lines with λ/4 lengths are optimized to 5.5um at 77GHz in the full EM simulations. ADS results are presented in Fig. 78. Based on obtained results, isolation between ports and input return loss are almost 40dB at 77GHz. Moreover, the output return

losses are below 25dB. For the designed power divider, the insertion loss (additional lines are included) is 3.8dB in average, where the insertion loss of ideal two-way Wilkinson power divider is 3dB.

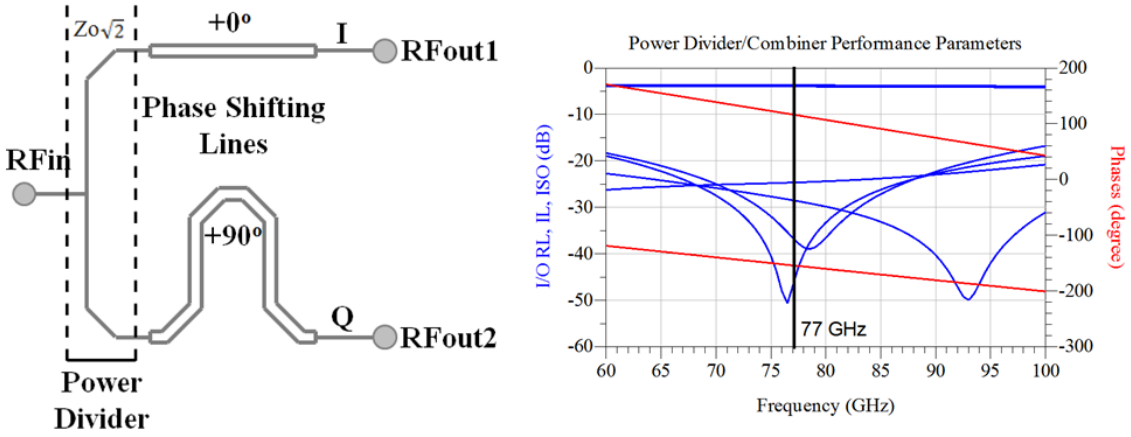

Fig. 78: Two-way Wilkinson power divider/combiner with 0°/90° phase shifting lines and corresponding ADS simulation results

5.3.2 Simulation & Measurement Results

Having simulation and measurement results for individual blocks, all were brought together in this new two-way topology (see Fig. 79-80). Based on these results, fabrication of the complete active phase shifter system is predicted to perform close to simulations since LNAs and 1-bit MEMS based phase shifters are already fabricated and working.

Fig. 79 shows the return loss of active phase shifter which is below 10dB for all modes around 77GHz. The results indicate that input and output return losses are better than 16.5dB. On the other hand, the gain changes between 3-7.5dB between 75-110GHz as the bias voltages are set between 1.8-2.3V, as shown in Fig. 80. The gain performance is also parallel to LNA gain in comparison to Fig. 76 as expected.

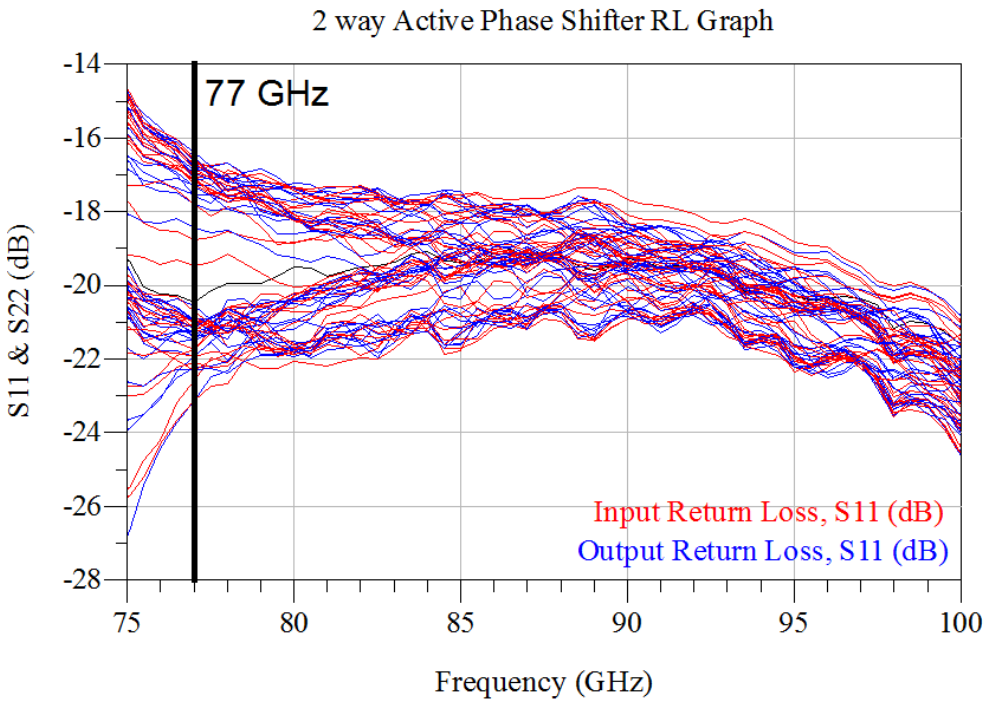

Fig. 79: Active phase shifter input and output return losses for all the states

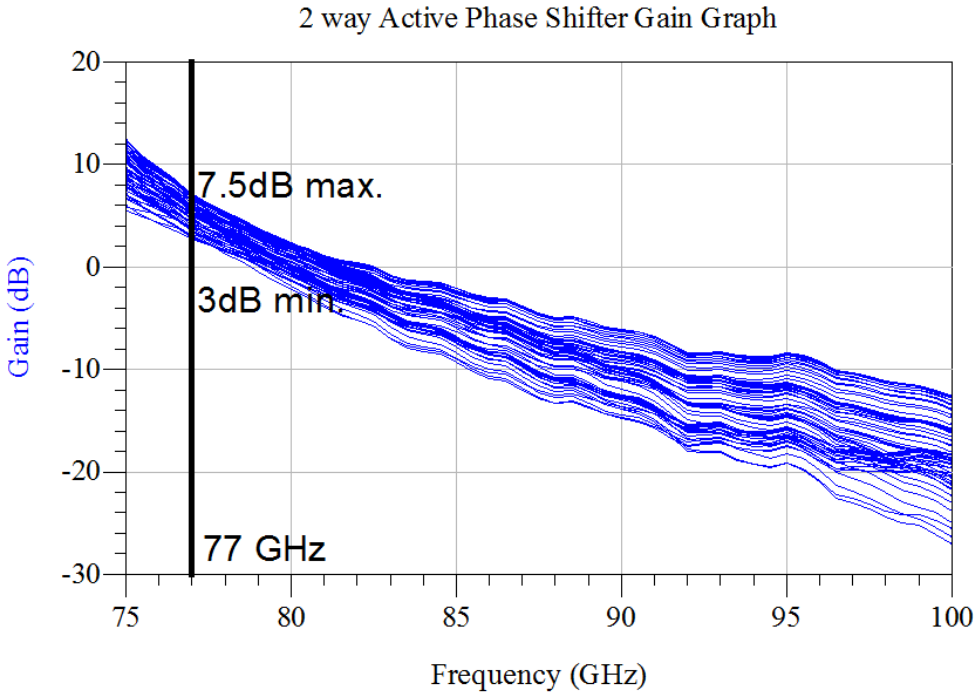

Fig. 80: Active phase shifter gain for all the states

In order to increase the overall gain, one can think of adding an LNA to the output of active phase shifter. Doing so, it is possible to achieve high gain levels (between 17-21.5dB) according to the LNA gain graph in Fig. 76.

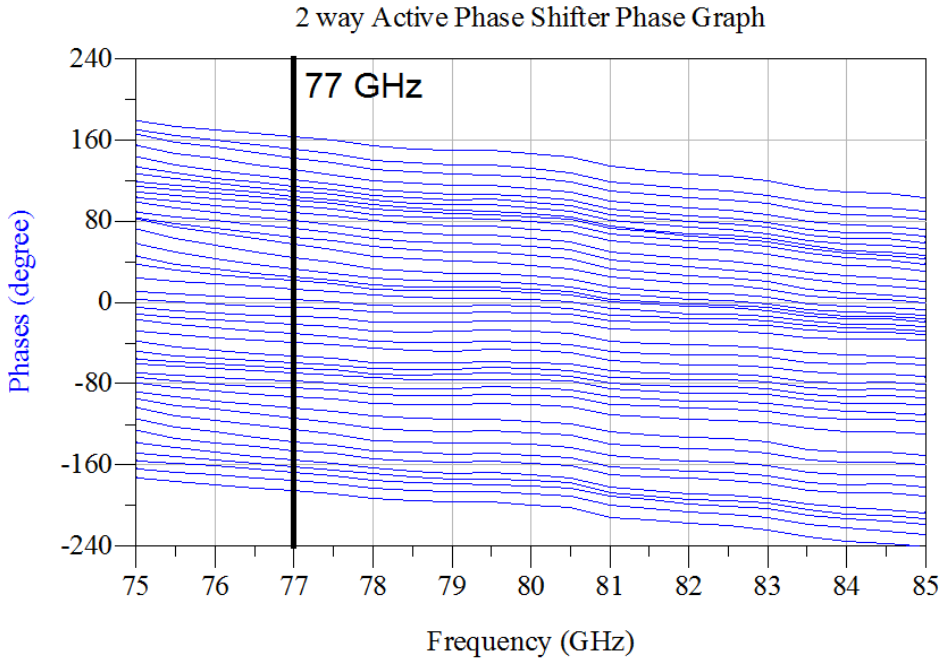

Fig. 81: Phase states of the active phase shifter

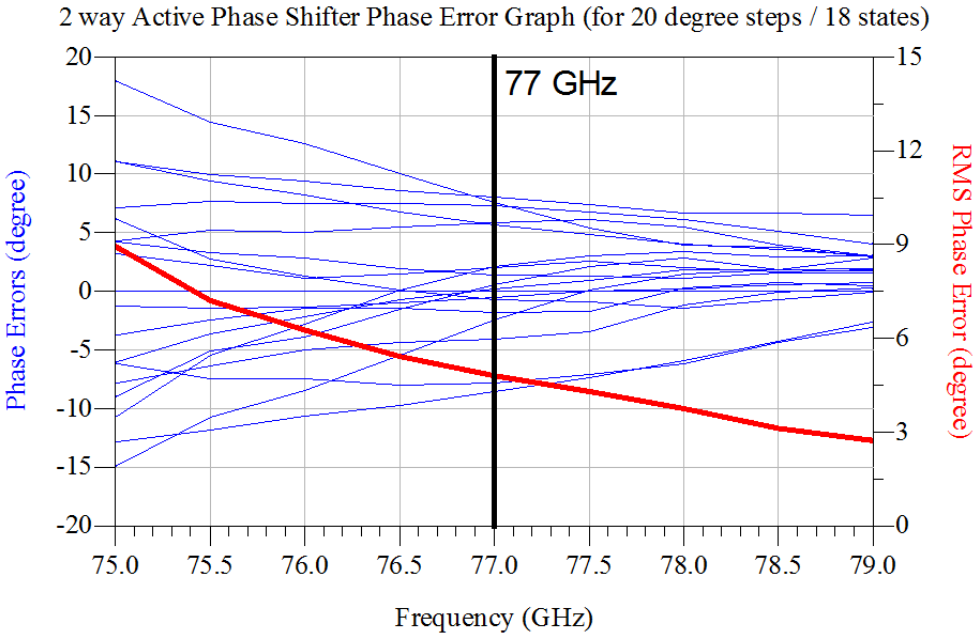

Fig. 82: Phase error performance of the active phase shifter for each state with 20° shifts

Fig. 81 shows the phase response of the phase shifter. Different phase states could be seen obviously with the changing LNA base voltages. In Fig. 82, rms phase error graph is presented with the phase error of states providing 20^o consecutive shifts (showing 18 states, other states are neglected for simplicity). According to Fig. 82, 4.8^o error centered at 77GHz is obtained and decreases below 3^o at 80GHz.

Fig. 83 shows the submitted layout to be fabricated at IHP. The overall chip area is $3.74mm^2$ (1.7mm x 2.2mm).

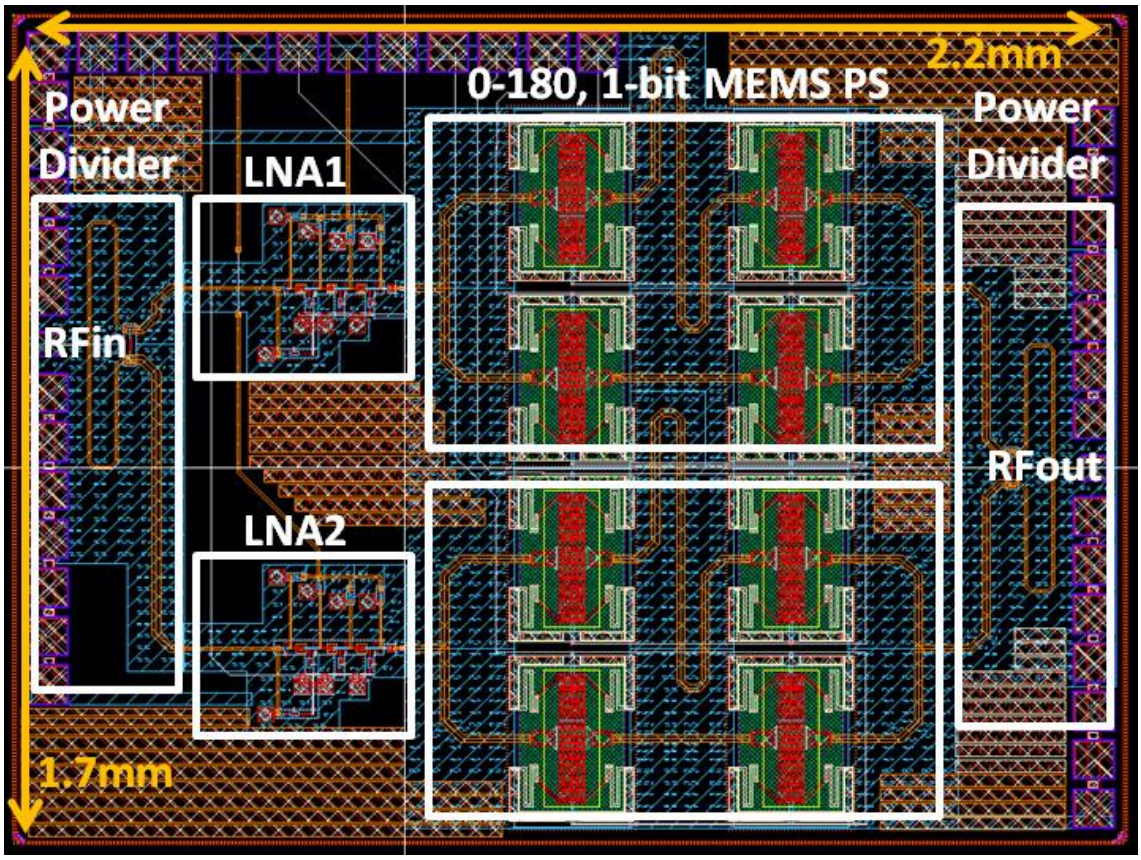

Fig. 83: Active phase shifter layout sent to fabrication

6. Conclusion & Future Work

6.1 Summary of Work

In this thesis, four LNA designs and three phase shifter designs with related measurement results are presented for 77GHz automotive radar applications. For the technology, commercially available IHP Microelectronics 0.13μm 300/500GHz SiGe HBT SG13G2 and 0.25μm 180/220GHz SiGe HBT SG25H1 are selected.

LNAs employ single-stage cascode, three-stage single-ended common emitter with/without shunt resistive feedback and two-stage cascode topologies. Amongst these, the three-stage architecture achieves the widest bandwidth which is more than 25GHz in W-band with input/output matchings and isolation being better than 10dB and 40dB as it was expected from simulations. Moreover, 21dB peak gain and a flat, over-15dB gain is obtained respectively at 75GHz and in full W-band. On the other hand, from the simulations, 4.9dB of noise figure, -4dBm of P1dB and 5.5dBm of OIP3 are observed. This 0.2mm^2 chip achieves one of the best LNA performances in the current literature. In order to improve the stability at the expense of gain reduction and a bit of noise figure degradation, shunt resistive feedback is placed at the second and third stages of this amplifier, which, in return, peak gain

is reduced to 12dB with 5.8dB noise figure. The third design is based on single-stage cascode topology. This can reach better gain and noise figure perfromances than the three-stage LNA with shunt feedback in a single stage, however the supply voltage increases. The measurement results reveal 17dB peak gain at 80GHz with both below 10dB input and output return losses in 82-85GHz. The isolation is around 30dB and the measured 3dB bandwidth is found to be 11GHz. Additionally, 5.1dB of noise figure and -6dBm of P1dB is achieved from the simulations. Using 0.25μm technology, two-stage cascode LNA is built. However, due to matching networks, return losses are below 10dB rule-of-thumb level, being around 5dB for input and 3-12dB for output with the changing biases. The noise figure is also a bit higher than the LNAs built on 0.13μm technology, which varies between 9-11dB as the bias voltages change.

To complete the phased array structure, phase shifters are required. In this context, switched-line as one of the commonly used topology is adopted and MEMS switches are placed in SPDT blocks in order to create two 2-bit digital phase shifters and then combined 4-bit phase shifter. These blocks change the phase by 22.5^o and 90^o steps to cover 90^o and 360^o respectively and measurement results point out that they achieve clear phase shifts with 3.5^o and 10^o rms phase errors. Having integrated the fabricated LSB and MSB blocks in a 3.6mm^2 4-bit phase shifter on the simulation environment leads above 10dB return loss in the 70-80GHz band for all 16 different phase states separated by 22.5^o and 7.5^o rms phase error. However, since the insertion loss of the individual blocks are high, the overall loss ranges between 15.3-18.1dB. Therefore two active phase shifters based on vector-modulator topologies are fabricated. The first one uses three-way Wilkinson power divider/combiner integrated to three LNAs (the three-stage, single-ended LNA with shunt resistive feedback) and phase shifting lines providing 120^o separation. While these lines are used to divide the 360^o phase spectrum into three regions, phase sweep is realized with tuned LNA gains where one of the LNAs is turned off each time. According to the measurement results of the 100mW consuming 1.65mm^2-sized chip, a continuous phase shifting is clearly obtained. The phase shifter also provides high gain at 77GHz, which reaches 11dB peak, and almost no insertion loss up to 90GHz. Input and output are also well matched over the entire W-band. On the other hand, a two way I/Q type MEMS based active phase shifter is also designed. This time, two-way power divider/combiner circuits are integrated with two LNAs (two-stage cascode

LNA), phase shifting lines providing 90° consecutive phase separation, and two 1-bit MEMS phase shifting blocks (0°/180°). The logic is to select the region out of four phase regions, which are created by phase shifting lines, with the help of 1-bit phase shifting blocks. Then LNAs are used to rotate the phase with the weighted sum of two vectors. Since isolation resistors are placed at the ends of power divider/combiner, the return loss of LNAs are compansated and brought to above 15dB level as shown in the simulation results. Moreover, a variable 3-7.5dB gain is achieved by tuned LNA biases. The 3.74mm^2 chip is in fabrication.

6.2 Future Work

Having observed the measured active phase shifter structures, the overall performance is greatly affected by the LNAs. Therefore more neat optimization process should be carried out for LNAs especially for the noise figure which are matched to their minimum below 77GHz. Furthermore, some other techniques should be utilized to enhance the stability without causing much decrease in the gain so that the three-way phase shifter would enable more gain. In the long term, the phase shifters are decided to be integrated with antenna array on a Rogers 3003 substrate, which allows W-band operation, due to the high manufacturing cost of the full radar. Considering the current simulation results, the automotive radar project will be finalized.

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