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A PFM Based Digital Pixel with Off-Pixel Residue Measurement for Small Pitch FPAs

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***Abstract*— Digital pixels based on pulse frequency modulation (PFM) employ counting techniques to achieve very high charge handling capability compared to their analog counterparts. Moreover, extended counting methods making use of left-over charge (residue) on the integration capacitor help improve the noise performance of these pixels. However, focal plane arrays (FPAs) with small pixel pitch are constrained in terms of pixel area, which makes it difficult to benefit from in-pixel extended counting circuitry. Thus, in this paper, the authors propose a novel approach to measure the residue outside the pixel using an analog-to-digital converter (ADC). A first prototype of the proposed pixel, in the form of a testbed, has been developed which is aimed at medium-wave infrared (MWIR) imaging arrays having small pixel pitch. The prototype is composed of a pixel front end, a 12-bit SAR ADC, a counter, and a comparator. The front-end is a modified version of the conventional design and has been designed and fabricated in 90nm CMOS, whereas off-the-shelf discrete components have been used to implement the ADC, comparator, and counter. Measured signal-to-noise ratio (SNR) at low illumination levels is 55dB.**

***Index Terms*— Digital Pixel, Pulse Frequency Modulation (PFM), Infrared Focal Plane Array (IRFPA)**

I. Introduction

Successful implementations of pixel sensors have been demonstrated many times in the literature. Both analog and digital versions of such pixel sensors can be found [1-5]. While analog pixels offer a larger fill factor, their digital counterparts provide a direct digital output and can significantly improve the charge handling capability [2]. Generally, a digital pixel either consists of an in-pixel analog-to-digital converter to perform the signal conversion or is based on a pulse frequency modulation (PFM) loop. While the former applies direct analog-to-digital conversion to the pixel, the latter incorporates multiple-self-reset operations using a comparator. PFM-based designs have shown better signal-to-noise ratio (SNR) and dynamic range performance [7]. Recently, a number of applications for infrared focal plane arrays (IRFPAs) requiring high-resolution, high frame rate and large-pixel-count images in medium-wave infrared (MWIR) regime have emerged such as optical flash thermography, industrial process monitoring and missile warning systems [2]. The requirements of high resolution and large pixel count drive the need for imaging arrays with small pixel pitch. Smaller pixel pitch means that the pixel is constrained in area. With the area constraint, analog pixels show limited charge handling capacity and below par SNR performance. Digital pixels, on the other hand, offer significant SNR improvement at the cost of increased area, though not at low illumination levels [2]. Therefore, a need arises to develop pixel architectures that can achieve acceptable SNR performance for small pixel sizes at low illumination levels.

Traditional PFM based implementations of digital pixels store charge in the digital domain, resulting in the charge handling capacity increasing exponentially, with respect to pixel area [2]. As shown in Fig. 1, these pixels typically consist of an integration capacitor, comparator, an in-pixel analog-to-digital converter consisting of a photocurrent-to-frequency converter (I-to-F converter) circuit connected to a counter, multiplexers to connect the counter to the output of ROIC, and pixel timing and control circuits. When operation begins, the integrating capacitor fills at a rate proportional to the photocurrent, and the progression of charging and resetting generates a pulse train whose frequency is proportional to the photocurrent. The pulse train is input to the counter, which then increments its contents with each pulse until the integration ends, at which point the contents of the counter represent a digital well with total integrated photoelectrons equal to the product of the digital count and the well capacity.

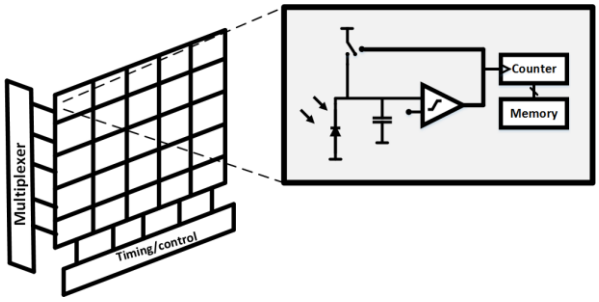

Fig. 1. Pixel components in a typical PFM-based pixel architecture.

Such PFM implementations can be found in [6-10], where excellent imaging results are obtained but only at high illumination levels when the detector current is large. To improve SNR at low illumination levels, an extended counting

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technique was proposed in [2], in which the left-over charge at the end of integration is computed (converted to digital) in-pixel and then stored in-pixel as well. This computation is carried out by counting the number of clocks from the time when integration is stopped until the next auto-reset. The additional bits obtained from this computation are added to the pixel count and form the LSB bits of the final output. This helps reduce quantization noise. The drawback of this technique is the increase in pixel area. The design in [2] was for a 30µm pixel pitch. With the ever-continuing trend towards smaller pitch FPAs, the required additional circuitry for extended counting cannot fit within the pixel area.

In this brief, the idea of residue measurement to improve SNR has been exploited, and a digital pixel, which is a modified version of the conventional PFM-based architecture, has been proposed along with a method to measure residue outside the pixel. The pixel design is targeted at MWIR FPAs employing Mercury Cadmium Telluride (MCT) detectors. Output characteristics, such as current and impedance, of such detectors have been modeled by the use of an MOS device as an input circuit within the pixel. A prototype has been developed as a proof-of-concept. In addition to a PFM-based pixel front-end, the prototype encompasses an ADC, a comparator, and a 6-bit counter. The idea is to exploit the superior SNR performance of digital pixels and at the same time keep the pixel size small by delegating residue measurement to an off-pixel ADC. It is worth pointing out that the integration time and charge handling capacity of the proposed pixel have been determined based on commercial MWIR ROICs targeting the applications mentioned earlier [11]. However, the proposed method can be used in any infrared ROIC, that implements residue measurement technique, to overcome the pixel area constraint.

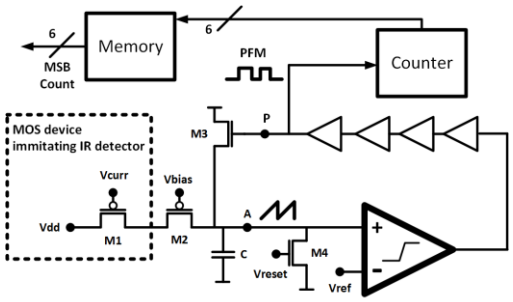
The paper is organized as follows: Section II describes a conventional PFM-based pixel; Section III provides background on the extended counting technique reported in [2]; Section IV describes the architecture of the proposed digital pixel; Section V presents the developed prototype; SNR measurement results are shown in Section VI; and finally, the concluding remarks are provided in Section VII.

II. Conventional PFM Based Digital Pixel

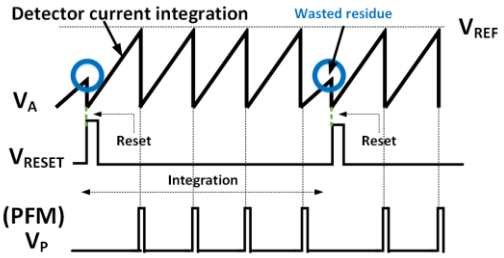
The schematic of a conventional pixel front-end is shown in Fig. 2(a). This architecture is based on a PFM loop. Detector current (or photocurrent) is imitated by the current supplied by device M1 and direct injection (DI) device M2. These devices have been sized to provide current in a range of 100pA-1nA, which is within the typical output current range of MWIR MCT detectors [12]. This current fills up the capacitor C at a speed determined by the magnitude of the current. Once the voltage at node A exceeds V_{ref}, the comparator switches to high and M3 turns on. This resets the capacitor to 0V, and the integration operation repeats until a controller block sends a manual reset signal (V_{RESET}) to stop integration. The 4 inverters in the loop create a delay to ensure that the capacitor is allowed enough time to discharge completely.

Every time the comparator switches, a short pulse is generated at node P. This is referred to as the PFM signal. This signal is fed to a counter as its clock. The integration operation continues until a manual reset signal turns M4 on. When this happens, the capacitor is discharged to 0V, and at this point the counter holds the digital value corresponding to the integration time, and eventually the number of charges collected. This count value is transferred to a memory in the form of a register. The period of this reset signal defines the duration of the integration phase.

Fig. 2(b) illustrates the operation of the pixel front-end. As shown, the residue at the end of the integration period is essentially wasted. The method proposed in [2] makes use of this left-over charge to improve the overall SNR of such a pixel for scenarios where the detector illumination is low and hence the current is low. The next section briefs this technique.



(a)



(b)

Fig. 2 (a) Schematic of a conventional PFM-based pixel. (b) Pixel timing diagram and operation.

III. Digital Pixel Based On Extended Counting

In extended counting, the integration phase is the same as in a conventional PFM-based digital pixel, as explained in the previous section. However, another phase is added in which the value of the left-over charge on the integration capacitor is calculated by the use of the same counter but with a different clock which is much faster than the PFM signal [2]. This phase is referred to as the fine quantization phase, which makes integration the coarse quantization phase. This phenomenon is the same as seen in a sub-ranging ADC where the signal range is reduced after a coarse quantization step and then further conversion is performed on the remaining signal. Therefore, during fine quantization, conversion of this left-over charge (or voltage) is carried out by using the same counter which computes the time required to trigger the comparator one more time. The residue enable signal shown in Fig. 3 is responsible for switching between the integration and

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residue phases. Integration of the photocurrent onto the integration capacitor is allowed to continue at this phase even though integration has logically ended. This counting is done until the next auto-reset event occurs, at which point the residue data is transferred to a register. An ALU then performs the computation described in [2] on the residue value to obtain the final output.

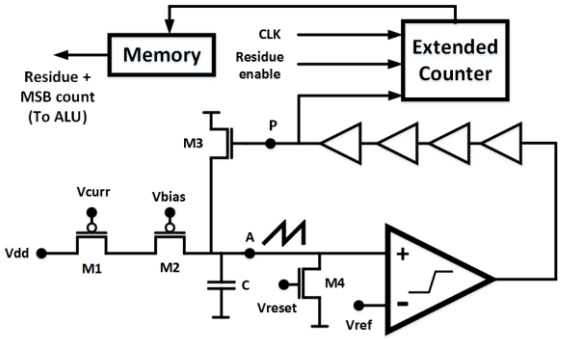

Fig. 3. Pixel architecture incorporating extended counting [2].

This technique produces excellent results, especially at low illumination levels, in which case the improvement in SNR is significant. However, the additional logic required to perform residue computation and the extra storage registers increase the area requirement of the pixel. FPAs with small pixel pitch will not allow the addition of this much circuitry to the pixel.

IV. Proposed Method Of Residue Measurement

Given the pixel area constraints, using the extended counting technique to measure residue does not seem feasible. To this end, a method is proposed in which a modified PFM-based pixel architecture is used for the front-end whereas residue measurement is performed off-pixel using a column ADC. MSB counting is carried out in the same way as in a conventional architecture. A 6-bit MSB counter turned out to be appropriate given the area constraints.

The ADC performs a direct conversion on the residue voltage, and the digital value obtained is simply appended to the MSB count value, forming the LSB bits of the final output. From a computational point of view, this method has a certain degree of simplicity compared to the extended counting method because residue bits do not have to go through any computations before being combined with the final output. An ALU is also not needed in this case. Moreover, as a result of the direct conversion, a clock signal is not required in the pixel. This implies that clock buffers, which would otherwise be required, can be avoided and simpler clock routing schemes can be used. Additionally, the potential noise introduced by the clock signal is also eliminated. However, the accuracy of the measured residue in the proposed method is dependent on the performance of the ADC. In addition, with a number of ADCs now being used, the power consumption of each ADC will need to be below a tight specification.

Major modifications to the pixel include the addition of a source follower and the use of a self-biased complementary differential amplifier in place of the comparator. Moreover, the pixel size is 15x15 um^2 and the design has been optimized to work at cryogenic temperatures by sizing the MOS devices appropriately and by using low-V_t devices to compensate for the V_t and mobility shift and the resulting variations at cryogenic temperatures. In Fig. 4(a), part of the full pixel front-end has been shown with the proposed modifications highlighted. The figure also provides a system-level perspective for an ROIC in which the pixel output (source follower) is interfaced with the column ADCs through row-select switches (not shown). Count values are read out by the controller after integration completes. The row select block, shown on the left side of the ROIC, selects the row for which residue conversion needs to be carried out. Results of the conversion (the residue values) are stored in the residue registers and shifted out immediately. Timing signals for integration and residue phases are generated by the controller.

Before discussing the proposed architectural modifications and pixel operation, it is worth looking at design considerations regarding the integration capacitor C. The size of the integration capacitor plays a vital role in the performance of the pixel. The size of this capacitor is largely decided based on the area constraint of the desired pixel sizes, leading to a capacitance value of 25 fF. Such a small-sized capacitor implies higher power consumption, due to increased switching activity, and a reduced charge handling capacity. However, it results in a lower quantization noise (refer to (2)).

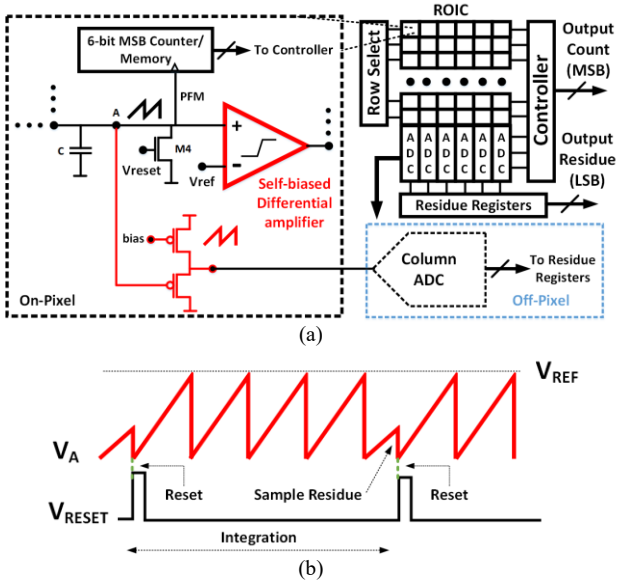

Fig. 4. Proposed modification to a conventional PFM-based pixel with ROIC architecture. (b) Timing diagram of proposed pixel.

The operation of the proposed pixel is shown in Fig. 4(b). The residue voltage is sampled by the ADC at the instant when integration is stopped. In a design with a full 2D array, the residue will have to be held on the integration capacitor before reset is issued. This will require minor changes in the design of the pixel front-end.

A. Source Follower

Delegating the pixel measurement job to an off-pixel circuit requires proper buffering at node A because this node is very sensitive and can be easily loaded by the ADC. This is done

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by adding a source follower, which is a very simple and concise circuit that can provide decent buffering performance and does not add too much area, inside the pixel. While adding the source follower does result in a level-shift of the integration waveform, this effect can be accounted for by adjusting the reference voltage of the ADC.

B. Comparator

A comparator in the form of a complementary self-biased differential amplifier has been added to the modified pixel. The self-biasing scheme helps avoid static power consumption from the otherwise needed bias circuitry and also removes one input signal from the pixel, thereby facilitating array routing in a DROIC implementation. The amplifier magnifies the difference between the voltage on the integration node and reference voltage V_{ref}. This voltage difference then drives the feedback inverters to generate the PFM signal. Fig. 5 shows the schematic of the designed amplifier. This topology provides larger switching currents than its quiescent current, which improves the speed at large input difference, making the PFM loop faster in high illumination conditions.

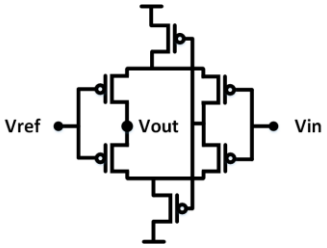

Fig. 5. Complementary self-biased differential amplifier.

C. ADC Architecture, Resolution and Power Consumption

For the prototype being presented, an off-the-shelf ADC component that mimics a column ADC has been employed to aid in the intended functional prototyping of the proposed technique. Therefore, it is important to select an architecture that provides the desired performance in terms of resolution and power consumption. For this purpose, the required ADC resolution has been derived by writing the below expression for charge quantization noise (N_Q)

$$N_Q = \frac{\Delta}{\sqrt{12}} \tag{1}$$

where Δ is LSB charge. Using $\Delta = CV_{LSB}$ we obtain

$$N_Q = \frac{C_{VLSB}}{\sqrt{12}} = C\frac{V_{ref}}{2^B\sqrt{12}} \tag{2}$$

where N_Q is the quantization noise, V_{ref} is the reference voltage and B is the ADC resolution. V_{ref} is set to a nominal value of 0.5V in the proposed design and can go up to 1V. Choosing N_Q=45 electrons [2], we obtain B=10 for a 25fF integration capacitor C. Thus, to account for additional conversion artifacts a 12-bit SAR ADC from TI is chosen for this prototype. The choice of SAR is dictated by its low power operation and acceptable resolution at the intended sampling rate (dictated by frame rate and array size).

D. Signal to Noise Ratio

A noise analysis for the proposed prototype has been performed using the noise breakdown provided in [2]. Various noise sources were identified with the detector noise, shot noise, and quantization noise being the dominant ones. Computation and application of the residue to the pixel output significantly reduce quantization noise. This improves SNR and is apparent in the measurement results reported in Section VI.

V. Digital Pixel Prototype

A block diagram of the prototype is shown in Fig. 6. As mentioned before, for this prototype the counter and comparator have been implemented using off-the-shelf components. The integration output generated by the front-end is fed to the comparator, which converts it to square pulses acting as a clock signal for the 6-bit counter. The processor acts as the control unit and generates the timing signals such as pixel reset. Before pixel reset is asserted, the counter holds the count value that corresponds to the number of auto reset events generated. This value, which forms the MSB part of the desired pixel output, is read by the processor. Furthermore, the voltage at the integration node is also sampled at the same time by the SAR ADC. This voltage essentially corresponds to the residue charge after integration. This value is converted to a 12-bit digital value and fed to the processor. The processor then appends this 12-bit residue to the 6-bit MSB.

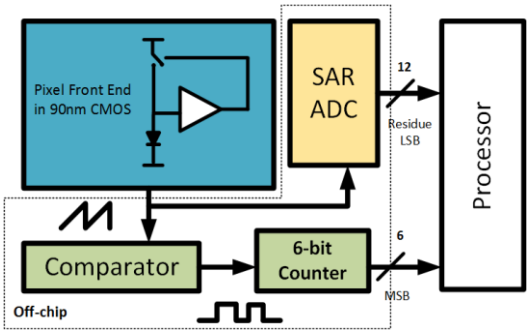

Fig. 6 The prototype system block diagram.

VI. Measurements And Results

Two kinds of measurements have been carried out to demonstrate the effectiveness of the proposed approach: (i) pixel front-end measurements to observe the integration operation; (ii) SNR measurements of data obtained from the prototype.

A. Front-End Measurements

The output of the pixel front-end has been measured by maneuvering the manual reset input of the pixel with a logic analyzer to set the integration time. These measurements have been conducted for various currents and integration durations. Fig. 7 shows the measurement results with a 170 µs integration time and 300 pA current. This plot has been adjusted to take account of the shift resulting from the source follower. Note that with a higher current, the frequency of the integration signal (V_{cap}) will increase.

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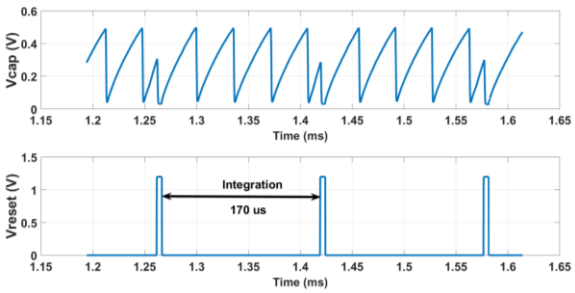

Fig. 7. Measured pixel operation with an input current of 300pA. Vcap corresponds to node A in Fig. 2(a)

B. *Prototype Measurements*

Output bits have been obtained for a set of collected electrons and SNR has been measured, as shown in Fig. 8. For a fixed integration time and input current, the value of the MSB count (D_{MSB}) is fixed. The total number of electrons collected (Ne^-) can be expressed as

$$Ne^- = \frac{C \times V_{ref} \times D_{MSB}}{1.602 \times 10^{-19}} \tag{3}$$

Moreover, SNR has been computed by calculating the mean and standard deviation (STD) of the measured data for a given number of collected electrons, as shown below

$$SNR_{dB} = 10\log_{10}\left[\frac{MEAN(data)^2}{STD(data)^2}\right] \tag{4}$$

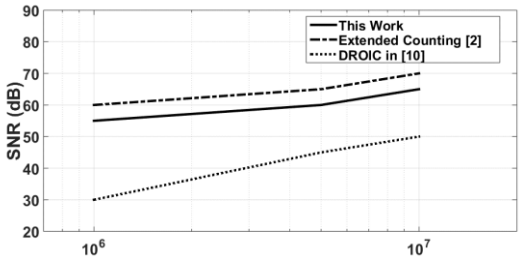

Fig. 8. SNR vs the number of collected electrons.

The SNR values have been compared with the results obtained in [2] and [10]. The former employs extended counting, and the latter uses a conventional PFM-based architecture. The improvement in SNR compared to [10] as shown in Fig. 8 can be attributed to the addition of residue, which represents the left-over charge on the integration capacitor at the end of the integration period, to the count value. This residue forms the LSB bits of the final output and adds strength to the signal component of the final output. SNR improves as a result. Greater improvement at low illumination (25dB) is due to the fact that the residue is a bigger part of the final output at low illumination (count value is small) and therefore has a higher impact.

Specifically, a comparison with [10] reveals that at low illumination (10^6 electrons) the proposed design achieves an SNR of 55dB as opposed to 30dB. Moreover, when the number of collected electrons is 10^7, this work reports 60dB compared to the 50dB SNR reported in [10]. SNR values obtained in this work are about 5dB less compared to the results reported in [2]. However, it should be noted that the results in [2] were obtained from a 2D pixel array as opposed to a single pixel in this work.

VII. Conclusion

A prototype of a digital pixel, intended for small pixel IR FPAs, with off-pixel residue measurement, has been demonstrated. The developed testbed comprising a fabricated PFM based pixel with an off-pixel (and off-chip) SAR ADC, counter and a comparator has been used to measure SNR. And as reported, SNR numbers breaking through the usual limitation at low illumination levels have been observed. Hence the proposed approach achieves the intended improvement in SNR performance by combining residue charge with the MSB count and at the same time allows concise pixel size by allowing off-pixel residue measurement.

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