Cryogenic measurements of a digital pixel readout integrated circuit for LWIR

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ABSTRACT

This paper presents and discusses the cryogenic temperature (77K) measurement results of a digital readout integrated circuit (DROIC) for a 32x32 long wavelength infrared pixel sensor array designed in 90nm CMOS process. The chip achieves a signal-to-noise ratio (SNR) of 58dB with a charge handling capacity of 2.03Ge- at cryogenic temperature with 1.3mW of power dissipation. The performance of the readout is discussed in terms of power dissipation, charge handling capacity and SNR considering the fact that the process library models are not optimized for cryogenic temperature operation of the Metal-Oxide-Semiconductor (MOS) devices. These results provide an insight to foresee the design confrontations due to non-optimized device models for cryogenic temperatures particularly for short channel devices

Keywords: ROIC, DROIC, digital ROIC, staring array, quantization noise

1. INTRODUCTION

For development of digital readout integrated circuits (DROICs) significant efforts has been deployed over the last decade in order to meet the third generation ROIC requirements Reducing the Size Weight and Power (SWaP) dissipation of infrared (IR) readout integrated circuits (ROICs) is a strongly followed trend by the industry. Power and area reduction has been obtained by performing the analog-to-digital conversion on ROICs which not only reduces the size and weight of the IR system as well as total power dissipation [1-3]. Aside from the SWaP trend in order to have high SNR, charge handling capacity of ROICs needs to be increased. In every imaging application, the most important parameter SNR is limited with the photon shot noise. In order to obtain higher SNR a ROIC is supposed to collect maximum signal electrons possible. The charge handling capability of typical analog ROICs are limited to $20Me^-$ .for MWIR application this much charge handling capability is adequate as the photon emittance is comparatively low in contrary to LWIR spectrum. In typical ROIC, an integration capacitor is used to store photo-generated charge, and integration capacitor area increases linearly with increase in storage capacity. In order to have fine resolution, small pixel dimension is inevitable thereby limiting the charge handling capability of analog ROICs. As matter of fact physical small pixel area puts the constraints on the value of integration capacitors to be used, thus restricts the upper bounds on SNR to be achieved.

In comparison to analog ROICs, the charge handling capacity increases exponentially with respect to pixel area in DROICs. It enables higher charge handling capacity along with higher SNR in a small pixel area. Moreover, by virtue of most implementation in digital domain these architectures are scalable with technology.

In literature various DROICs have been reported with serial, column parallel and pixel parallel conversion. Although column parallel architectures are very common [4, 5] ,pixel parallel conversion (digital pixels) offers a significantly higher dynamic range due to the exponential relationship between their charge handling capacity and pixel area, since the charge storage is in the digital domain. In DROICs with column parallel ADCs, signal chain resembles to an analog equivalent ROIC i.e charge is stored on an integration capacitor and charge handling capacity scales linearly with pixel area. Recent DROICs have been reported in terms of tremendous charge handling capacity in range of giga electrons and SNR extending up to 90 dB at room temperature[6].

2. METHODOLOGY

A 32 x 32 DROIC array with high charge handling capacity of 2.3Ge-, low power dissipation of 1mW and lowest quantization noise of 161e- has been reported in our previous work for Long Wave Infrared (LWIR) pixel sensor array

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[7]. The ROICs are usually reported at their room temperature (RT) because they can be validated through spice model simulations. In the actual operating conditions, however, the imagers have to be operated at cryogenic temperature (CT) [8, 9] for photonic imaging to reduce the noise due to the detectors.

Cryogenic temperature is defined as temperature below −150 °C, −238 °F or 123 K. At cryogenic temperatures the semiconductor devices are known to deflect from the general trend of various parameters such as carrier mobility of holes/electrons (μ0), threshold voltages (VTH0) and device parasitics but are difficult to model. Only recently an analog pixel ROIC has been reported in 0.35um CMOS technology operating at 77K-150K with an array size of 512 x 512 pixels, pixel size of 30um x 30um, charge handling capacity of 1Me- and 68mW of power dissipation with modified MOS device model [10] for optimum performance at 77K-150K. Another analog pixel ROIC [11] designed in 0.35um CMOS with an array size of 128 x 128 pixels, pixel size of 30um x 30um, charge handling capacity of 2.57Me- and 35.2mW of power dissipation at 50 frames per second (fps) has been reported.

This work presents, for the first time in the literature, the results of a DROIC with an array size of 32 x 32, pixel size of 30um x 30um, charge handling capacity of 2.01Ge- and 1.3mW of power dissipation at 250fps.

In the same chip, several NMOS and PMOS stand-alone test devices are placed to measure their current-voltage (I-V) curves at 300K and to determine the deviation from their spice model simulations at 77K. There are three different sets of device sizes Width/Length (W/L) 10um/10um, 600nm/100nm, and 120nm/100nm, for both NMOS and PMOS. These device aspects ratios are selected based upon minimum W/L, intermediate and the maximum W/L of transistors which have been used in actual design of DROIC, and to analyze the difference of temperature variations on small and long channel length devices.

3. RESULTS & DISCUSSION

3.1 DROIC and Test Devices Response at Room Temperature (300K)

The DROIC presented in this paper is based on pulse frequency modulation (PFM) method with coarse and fine quantization as explained in [7]. A 100MHz clock, together with 100μs residue measurement time, sets the lowest measurable photo-detector current (Iph) to 0.1nA with a quantization noise of 200 electrons for a 10fF integration capacitor (Cint). This digital pixel readout is able to perform at 400fps with 1mW of power dissipation and a peak SNR of 74dB.

3.2 DROIC and Test devices response at Cryogenic Temperature (77K)

The DROIC is cooled down to 77K using liquid nitrogen coolant. The DROIC reported in [7] now operates at 250fps with 1.3mW of power dissipation and a peak SNR of 58dB. The reason of this degradation becomes obvious from the I-V curves of the stand-alone MOS at 77K as shown in Figure. 1.

As the nominal model temperature of commercially available BSIM4 models is 25°C and valid temperature range is from -40°C to 125°C. The same device models are simulated in extended temperature range below -40°C and correlated with the measured IV curves leads to divergence .The measured I-V curves do not comply with any of process corner trends predicted by available models at 77K. In worst case, they even do not lie within model six sigma variations which refer to the manufacturing process quality control.

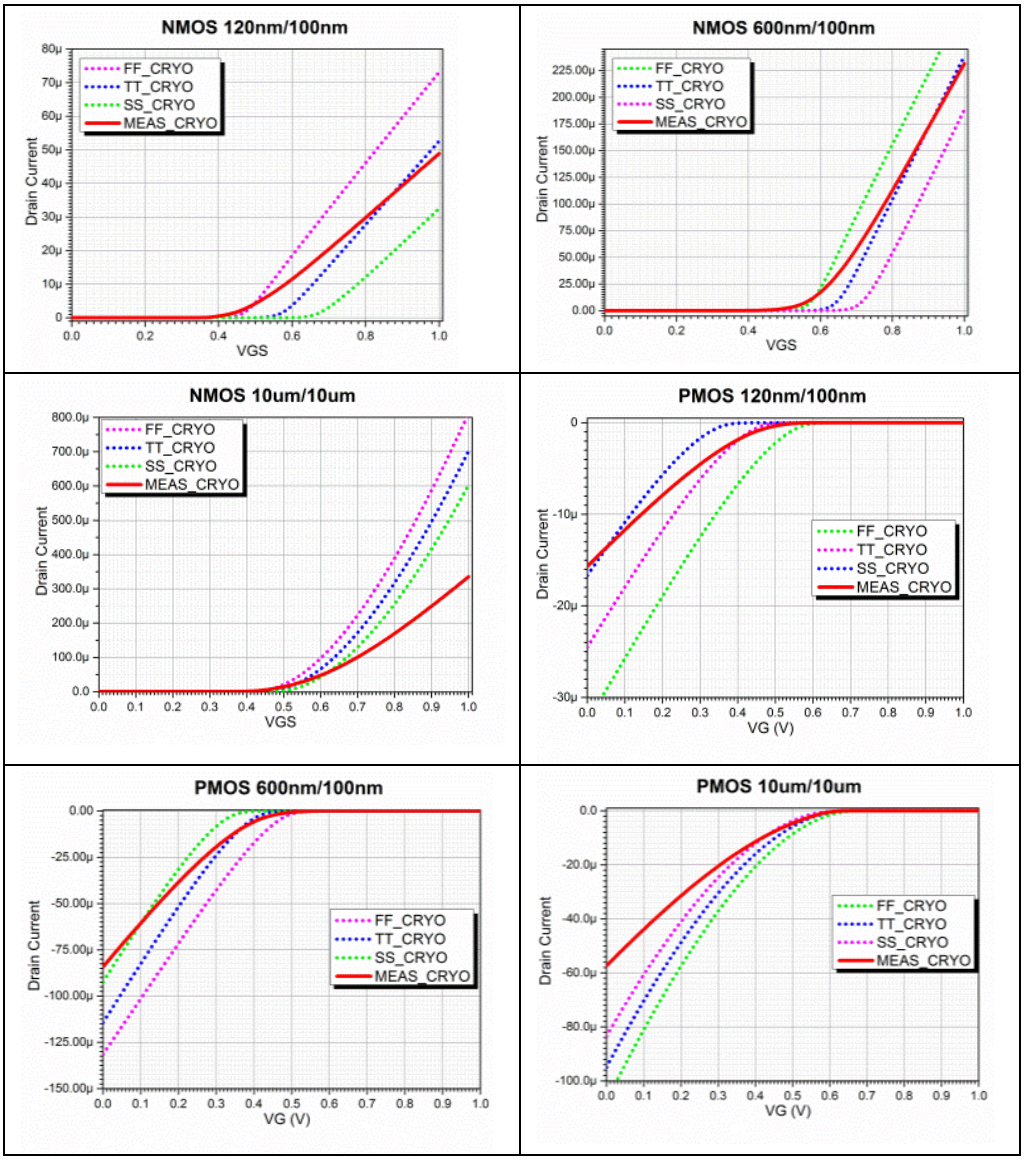

Figure 1. Device Measurements at 77K (FF_Cryo, TT_Cryo, SS_Cryo represent device process corners i.e. Fast-Fast, Typical-Typical and Slow-Slow at 77K)

The variation for MOS device models are due to temperature dependency of μ0 and VTH0; as the temperature is decreased from 300K to 77 K, it is observed that, μ0 is expected to increase by a factor of 3–6 and VTH0 is increased by about 0.2–0.4 V [11] for MOS devices.

At low temperatures, the thermal energy within silicon is not high enough to fully activate all of the donor and acceptor impurity atoms leading to the difference of carrier concentration than the dopant concentration and limits the device performance below 100 K temperature. At 77 K weak freeze out occurs which causes the increase of series parasitic resistance of Lightly Doped Drain (LDD) regions in MOS devices due to non-degenerate doping levels. These low temperature variations of μ0, VTH0 and parasitic resistance of LDD regions are not addressed by the room temperature models, consequently making the design of the ROIC challenging in terms of device performance.

Table 1 shows the VTH0 variation between the simulated and measured devices for both RT and 77K. Typical variation of trans-conductance (gm) with gate bias voltage can also be observed from graphs in Fig. 1. The slope of each curve

also indicates that μ0 increases up to intermediate electric fields (3-4MV/cm). Beyond that, strong electric fields arise leading to the onset of negative gm phenomenon [12].

The I-V curves are obtained using a semiconductor analyzer (HP 4155B) which can measure currents as low as 1pA. The threshold voltages (VTH) can be approximated from the measured I-V curves of the devices using quadratic extrapolation technique. Table 1 shows that the short channel devices have higher VTH variation as compared to the long channel devices at 77K, therefore, it is advisable to avoid use of small channel lengths even in the case of digital blocks for performance improvements at low temperatures same as the case for room temperature.

Table 1. Simulated vs Measured V_{TH} variation with respect to temperature.

Device Size	**Measured V_{TH} (mV)**	**Simulated V_{TH} (mV)**		
300K		FF	TT	SS
120nm/100nm	340	275.4	369.8	460.1
600nm/100nm	480	430.5	491.6	549.3
10um/10um	360	216.8	243.5	270.1
77K				
120nm/100nm	-440	-231.1	-341.9	-447.9
600nm/100nm	-450	-289.9	-366.6	-438.2
10um/10um	-350	-144.9	-171.2	-197.7

Since the DROIC has not been precisely designed and optimized for 77K operation, therefore, the supply voltages have to be increased in order to compensate for VTH0 and μ0 variations.

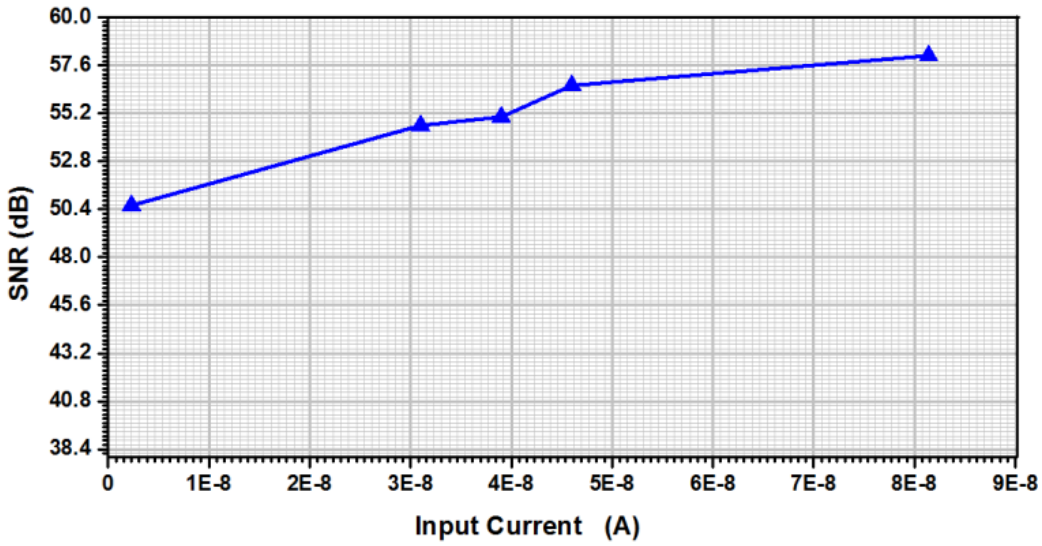

Figure 2. 32x32 pixel array SNR measurements for a wide input dynamic range (1nA-80nA) photo-detector current (I_{ph})

With gradual increase of Iph at input of the pixel array, SNR also increases as demonstrated in Fig. 2. At the highest detectable Iph of 80nA SNR is 58dB, and at the lowest Iph of 1nA the SNR is 50.4dB. Due to the increased charge handling capacity, the SNR improves at the higher Iph, whereas, the relatively higher quantization noise for low Iph reduces the SNR at 1nA. The pixel array has a non-uniform SNR distribution curve at 77K which is plotted on a Gaussian curve by taking SNR measurements of pixels from multiple chip

samples. Mean value of SNR is 45.2 dB with standard deviation of 6.7 dB. ±1σ, 2σ and ±3σ distribution are indicated on the graph in Fig. 3.

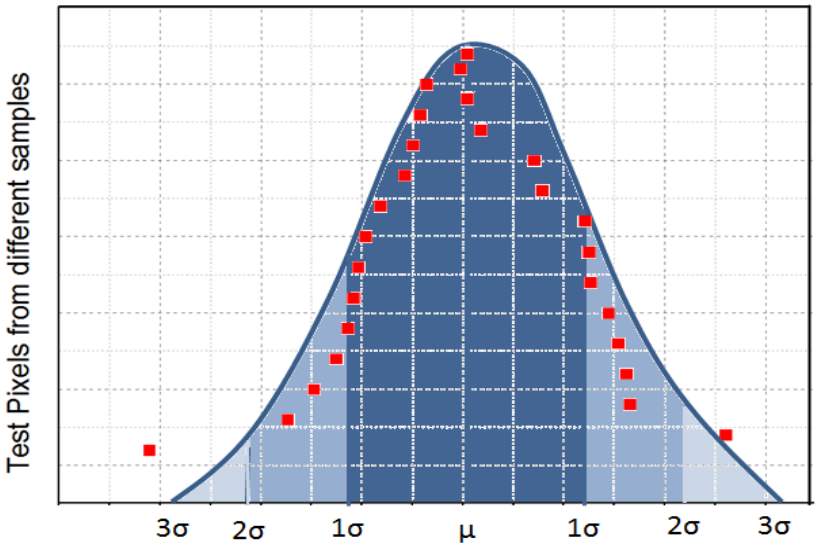

Figure 3. 32x32 pixel array average measured SNR response

The power dissipation of each block has been measured separately for 20nA of detector current at 250fps for a fair comparison with power dissipation reported at 300K [7]. The power dissipation for the comparator has been significantly reduced at cryogenic temperature as presented in Table 2. Even with the increased power dissipation of digital blocks (memory, counters, drivers and control circuit) and IO circuits as consequence of higher supply voltage, the overall power dissipation of 32x32 pixel array is still close to power dissipation at the room temperature reported in [7] due to notable reduction of comparator power dissipation attributing to the fact of gm enhancement and leakage currents suppression for MOS at cryogenic temperature.

Table 2. Power Dissipation for I_{ph} of 20nA at 250fps

Block	**Average current**	**Supply voltage (V)**	**32x32 Power (uW)**
Comparator	34 nA	1.1	38.36
Reset circ, memory,counters	363 nA	1.4	520
Control circ.,ALU, Drivers	138 uA	1.53	211
I/O pads	140 uA	1.53	214
I/O pads	238 nA	1.1	0.26
I/O pads	130 uA	2.5	325
Total			**1.3mW**

4. CONCLUSION

This paper presents to the best of our knowledge for the first time in the literature, an overview of the response of a LWIR DROIC array with a high charge handling capacity and relatively low power for cryogenic operation. Additionally, the stand-alone test transistor I-V curves are measured and compared with the available spice models. The deviation of test transistor I-V curves from the spice models in the plots show the extent of error that a device can add to the overall performance of a ROIC in 90nm CMOS while operated at cryogenic temperatures. The results also present the robustness of digital pixel ROIC in terms of power and maximum charge handling capacity even with lack of optimum cryogenic device models as compared to . It also provides the understanding of physical device behavior at

low temperatures which would lead to design of DROICs with optimum and improved performance the desired low temperature.

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