

Digital pixel readout integrated circuit architectures for LWIR

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ABSTRACT

This paper presents and discusses digital pixel readout integrated circuit architectures for long wavelength infrared (LWIR) in CMOS technology. Presented architectures are designed for scanning and staring arrays type detectors respectively. For scanning arrays, digital time delay integration (TDI) is implemented on 8 pixels with sampling rate up to 3 using CMOS 180nm technology. Input referred noise of ROIC is below 750 rms electron meanwhile power dissipation is appreciably under 30mW. ROIC design is optimized to perform at room as well as cryogenic temperatures. For staring type arrays, a digital pixel architecture relying on coarse quantization with pulse frequency modulation (PFM) and novel approach of extended integration is presented. It can achieve extreme charge handling capacity of 2.04Ge^- with 20 bit output resolution and power dissipation below 350 nW in CMOS 90nm technology. Efficient mechanism of measuring the time to estimate the remaining charge on integration capacitor in order to achieve low SNR has employed.

Keywords: Infrared (IR), Digital readout integrated circuit (DROIC), pixel parallel ADC, pulse frequency modulation (PFM), digital time delay integration (TDI)

1. INTRODUCTION

Infrared (IR) imaging systems ubiquitously cover a broad range of applications in both civil and military realm. Newer paradigms in biomedical, automotive, environmental monitoring, security and surveillance, space and astronomy applications are driven mainly by the enhanced aspects of the IR imaging systems [1] [2]. The IR system mainly employs a detector to convert the infrared detected radiation to an electrical signal and a read-out integrated circuit (ROIC) improvises processing of the electrical signal to stream-out video signal. Modern IR imagers are developed either by employing monolithic or hybrid methodologies. A hybrid approach is considered a dominant choice for demanding applications in terms of high speed, low power, and ultra-low noise. The choice of detectors depends upon wavelength of interest, quantum efficiency, noise, and cooling requirements specific to the application. Whereas ROICs are fabricated in deep submicron CMOS technology enabling provision of compactness, low power dissipation, and superior integration capabilities.

A typical signal flow of ROIC is initiated with the integration of photocurrent onto an integrating capacitor by the pixel preamplifier for fixed amount of integration time. The front-end preamplifiers are generally based on a direct injection, capacitive transimpedance amplifier or a buffered direct injection type followed by a source follower buffer and a sample hold stage. Discrete-time (DT) filters then condition the integrated voltages. The conditioned signal is then time-multiplexed to the output, which is either digitized using an on-chip analog-to-digital convertor (ADC) or is dispatched off-chip through the analog output buffer.

The on-chip ADC deployment opens-up the possibility of on-chip digital signal processing resulting in a compact integrated system. However, analog signal within the pixel necessitates preamplifiers to equip either a higher load-drive or longer sampling-time to drive the capacitive load of shared column lines, therefore deteriorating settling, and increasing power consumption. The problem exacerbates further for large sensor arrays. An alternate readout scheme is to employ digital pixel read-out architecture that incorporates an ADC at the pixel level[3]. A DROIC is readout circuit that improvises digital output in addition to digital storage of integrated photo current. Embedding memory cells as digital storages leads exponential increment of charge handling capacity with respect to pixel area contrary to linear increment in case of analog pixel. The enormous charge handling capabilities can be attained in limited pixel area. Moreover, large charge handling capability enables very high signal to noise ratios (SNR) for high flux density or low frame rate applications.

The vast majority of the infrared imaging systems are staring array or focal-plane array (FPA) based systems where

sensor pixels are arranged in matrix of rows and column. Compared to scanning array, FPA allows higher frame rate at higher pixel numbers. The main advantage of staring array system in addition to the absence of moving mechanical parts is that the FPA covers the whole field-of view (FOV) simultaneously for the entire frame. This causes reduced bandwidth for each detector resulting in SNR improvement. The scanning array systems are still utilized in some applications such as commander sight systems, surveillance systems, fire control systems for tanks. The scanning array systems offer the advantage over the staring systems in terms of radiometric accuracy caused by the fact that radiation from all image pixels is detected by only one detector element [4].

2. READOUT ARCHITECTURES

For scanning type detector, a ROIC has been designed using digital TDI algorithm to increase signal-to-noise ratio (SNR). This method employs couple of detector columns to produce a single column final image. All detectors perceives the same radiation and finally all the data is summed up and averaged, which effectively increases the integration time of the system, hence improving SNR[5].

For staring type FPA, a DROIC has been designed that aims to reduce the quantization noise of digital readout meanwhile elevating the charge handling capabilities. Various digital ROICs have been reported in the literature with serial, column parallel and pixel parallel conversion [6].

2.1 TDI Architecture for scanning FPAs

There is vast diversity in implementations of TDI algorithm, though predominance of analog is well renowned. However, analog TDI implementations suffer from substantial chip area, immense power consumption, inaccuracies, and non-uniformities. Plenty of storage capacitors or great deal of summing amplifiers is required for implementation of analog TDI which in consequence occupies considerable amount of chip area. Consequently, power dissipation is increased significantly. Furthermore, transferring the charge stored in unit cells in pixel to storage elements or summing amplifiers over a large chip area emanate switching errors, inaccuracies, and non-uniformities between rows and columns. On the contrary, digital TDI implementation renders better noise performance, higher dynamic range, lower power consumption, and smaller chip area compared to analog counterparts by virtue of in-pixel analog to digital conversion.

In addition, oversampling is implemented in conjunction with TDI algorithm, to escalate the spatial resolution which implies that the same scene is scanned from one detector to the nearest neighbor detector in several steps. The array size of the implemented ROIC is 90x8 and design is optimized to operate well both at cryogenic (77°K) and room temperatures.

The ROIC is combination of analog and digital blocks. The digital circuit is employed to generate control signals i.e integration signal (INT), multiplexer select signals and gain select switches. Digital control circuit is programmable through both serial and parallel interface that entitles to steer readout functionalities such as gain adjustments, scan direction, by-pass mode, pixel de-selection, and automatic gain adjustment.

The direct injection (DI) topology is adopted as front-end unit cell for sake of compactness and simplicity. The detector current is integrated onto the integration capacitor till it reaches maximum preset reference voltage V_{ref} . Once it is equal to V_{ref} , eventually the comparator is triggered and leading the counter to increment by 1. Subsequently the integration capacitor is reset, and ready to collect the forthcoming charges imminent from the detector. This sequence continues up until the end of the frame as determined by the signal INT. The counter value during the integration period constitutes the MSB (Most Significant Bit) fragment of the output data. Following the end of integration period, remaining charge on the integration capacitance is also counted with the aid of the previously employed comparator circuit constituting the LSB (Least Significant Bit) fragment of the output data. In order to do so, the remaining voltage on the integration capacitor is compared with ramp input from the on-chip ramp generator.

MSB and LSB counters are triggered by output of each pixel in a row. A common bus has shared for MSB and LSB signals as these operations takes place individually in successive manner instructed by control circuit. This common bus serves as MSB bus during integration period, later on as LSB bus as the integration period gets over. The switches are used to connect the bus to each MSB and LSB counter as shown in Fig. 1. In order to implement 8-stage TDI with

oversampling ratio of 3, number of MSB and LSB counters required for appropriate write and read operations is 23. These counters can be devoted as summation circuits also, as they basically count the charge packets imminent from the detectors implies that to improvise SNR they add the charge packets to instigate TDI.

2.1.1 TDI Circuit Implementation

TDI circuit implementation consists of front-end preamplifier stage, ramp generator, MSB and LSB counters and digital control logic block for events timing management.

Photocurrent integration takes place at the input stage. Direct Injection (DI) has been employed as preamplifier topology mainly due to low noise and area efficient design at the cost of inadequate injection efficiency in case of low photon flux. The MIM capacitors are used as charge storage. Self-biased differential amplifier is used for comparator which enables to draw less quiescent current meanwhile possess capability to source larger currents for desired speed for TDI implementation. Moreover, self-biased comparator does not require external bias voltage circumventing routing signal for each pixel.

Verilog HDL is used to generate control signals and standard cell libraries. Automatic placement and route tool has been employed for digital control block layout. Single master clock frequency is used for timing control of all digital blocks. Parallel interface mode of operation permits usage of fixed predetermined integration time and generate INT signal accordingly. Whereas serial mode caters privilege of any flexible amount of integration time required depending upon incoming photon flux. Standard cell library has used to design summation counters for MSB and LSB fragments, multiplexer circuits, and control switches. Ripple carry counter architecture is preferred as binary counter in order to minimize overall power dissipation.

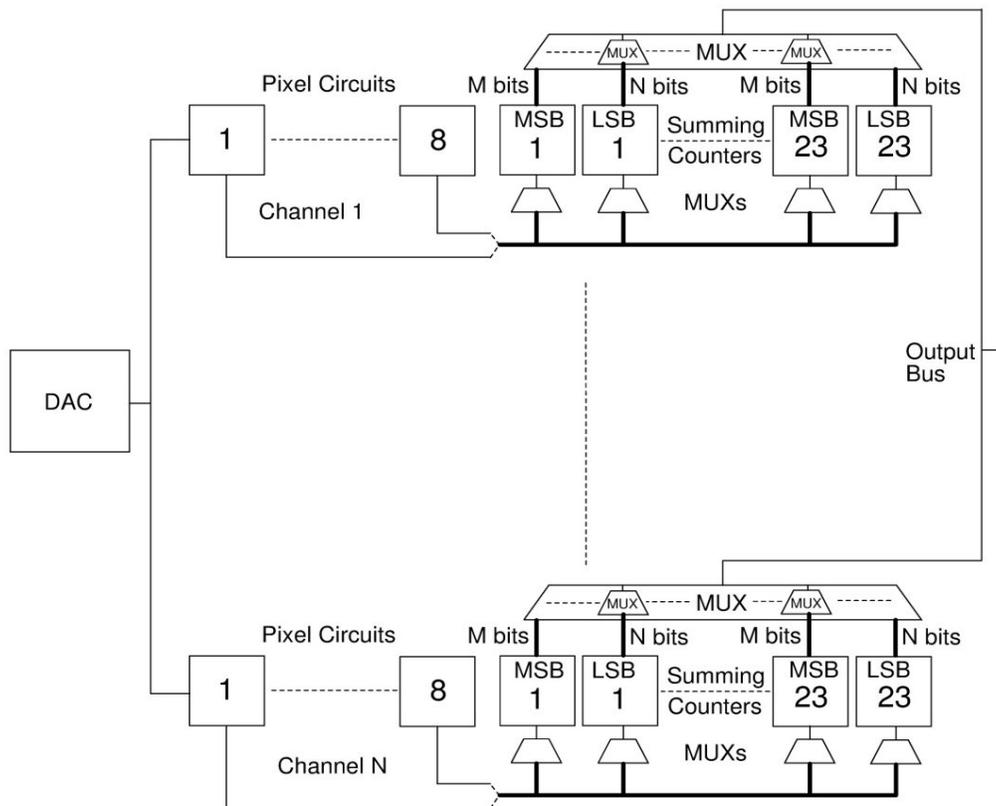


Figure 1. Block diagram of ROIC architecture for TDI implementation

2.1.2 Simulation Results

The simulation results of TDI implementation for LWIR are presented. Figure. 2 shows the output voltage developed across integration capacitor for incoming detector current. As soon the voltage developed across capacitor alleviates to preset V_{ref} , the comparator is triggered subsequently followed by reset of integration capacitor and startup of next integration. Comparator activity is monitored via output counters to store number of triggers counted during each frame marked as MSB fragment of output data. INT signal is active low in this scenario. As soon INT signal goes high the counter starts counting clock pulses and thereby generating LSB fragment of output data.

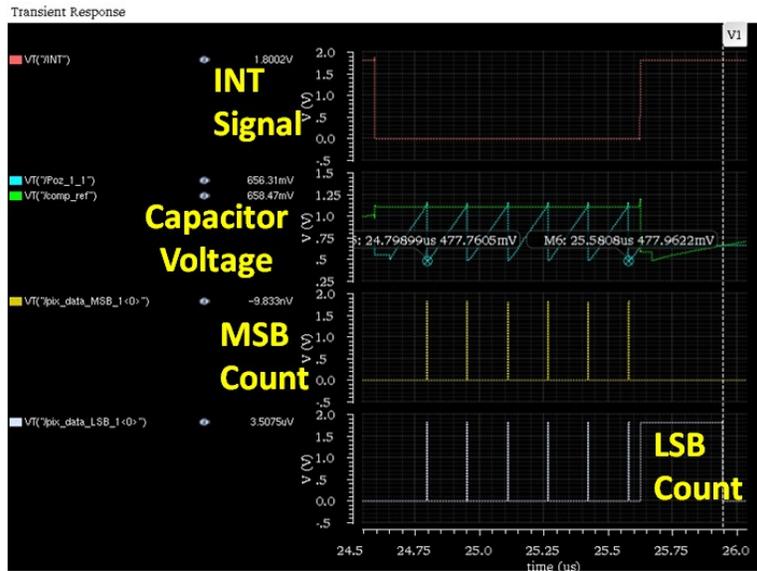


Figure 2. TDI Pixel level simulation results. MSB and LSB intervals are highlighted w.r.t detector input current and INT signal

Figure 3 presents pixel charge integration on capacitor is extremely linear in response to various amounts of detectors input currents within the range of 1nA-50nA.

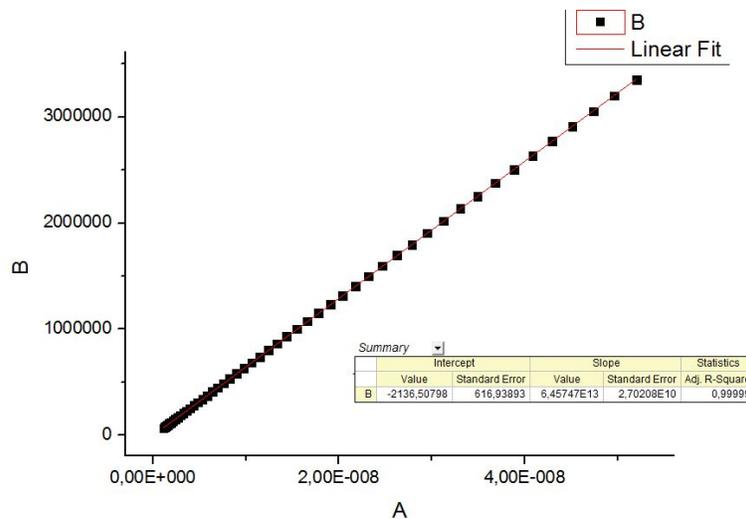


Figure 3. Pixel integration linearity for the input current range of 1nA-50nA

2.2 DROIC Architecture for starring FPAs

In general, Delta-Sigma modulation and Pulse Frequency Modulation (PFM) are two salient approaches for DROIC. Both approaches render on small in-pixel capacitor and comparator circuit which eventually resets capacitor right away as integrated voltage is equivalent to reference voltage. The fundamental difference amongst these approaches is that Delta-Sigma relies on clocked comparator as opposed to clock-free comparator in PFM. Higher charge handling capacity is achieved fairly well in both types of DROICs resulting in high SNR for lower frame rate or higher photon flux. However, both of them endure inferior SNR for low photon flux scenario [6].

An ordinary PFM pixel [7] consists of a direct injection (DI) preamplifier, an integration capacitor (C_{int}), a comparator and a counter as seen in Fig.5. A memory can be incorporated in the pixel for integrate while read (IWR) operation. During the operation, photo generated charges are accumulated on the integration capacitor that aggravates the capacitor voltage up to the comparator reference voltage. At that moment, comparator is triggered, a pulse is generated by the pulse shaping inverters which resets the integration capacitor, and the counter is incremented. By this way the total charge is measured via counting the number of resets and transferred to in-pixel memory register at the end of integration time. The counter is reset at the beginning of the new frame immediately after the transfer.

In this paper, using the extended integration method we report design perspectives for low power PFM DROICs. The proposed digital pixel operates in two phases: the coarse quantization phase is as in an ordinary PFM followed by a fine quantization phase of extended integration in time domain as shown in Figure 6. SNR of PFM DROICs with large charge packets are analyzed with a focus on quantization noise and kTC noise. It is shown that kTC noise contribution to SNR is independent of capacitor size and hence integration capacitor is a parameter for power optimization [7].

In order to achieve low quantization noise operation, novel residue measurement method of deploying a counter as clocked counter to determine the time allowed to ample further charge on integration capacitor to ultimately trigger comparator for an additional extra count.

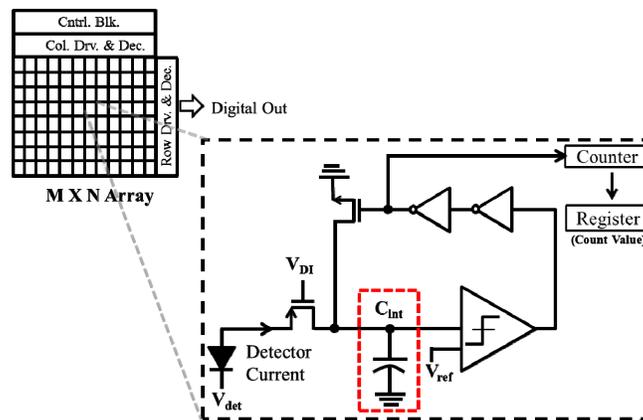


Figure 4. Ordinary PFM pixel and DROIC architecture

2.2.1 DROIC Pixel design and implementation

In order to reduce the quantization noise of PFM pixels, we have previously proposed a pixel employing extended integration method. Extremely low quantization noise levels of $161e^-$ with charge handling capacity of $2.33Ge^-$ have been measured [8]. The operation of the proposed pixel is split to two phases; coarse quantization in charge domain analogous to ordinary PFM and fine quantization in time domain using the extended integration method. In the first phase, for a given integration time, charge is measured through the asynchronous in-pixel counter. In the end of the

integration time, counter value is transferred to a memory and the counter is reset. Charge integration is not halted and the residual charge causing the quantization noise is to be measured through synchronous operation of the same counter. During this phase counter increments on each clock pulse as long as the comparator is not triggered. Immediately after the comparator threshold is exceeded one more time, counter is stopped and counter value is transferred to its memory registers at the end of residue measurement. Simultaneously new frame has started.

The frontend of the prototype pixel of Fig. 6 consist of DI unit cell superseded by the comparator circuit. In brief snapshot, prototype has mainly three core blocks: 32x32 pixel array, control unit and the ALU. The two inverters at the output node of the comparator are used for pulse shaping so that the counter can be triggered. The reset NMOS transistor is activated once comparator output is one and resets the integration capacitor, meanwhile the counter is incremented. Further ahead, M (14) bit value at the counter is transferred to the M bit register at the end of integration period. The counter operates as a clocked counter until the comparator threshold is exceeded for one additional trigger. Subsequently, the value of the counter is passed to N (11) bit register to be transferred to the ALU. This residue time is represented by the the time to trigger the comparator for an additional count. A next integration cycle can be started straightaway after transferring the count to the memory registers.

The master clock is used by the ALU, and the 20 bit output data is synchronized to the master clock. An internal slower clock generated by the master clock being used in the control unit. The control unit commands the data transfer to ALU from the 32x32 array. Programmable integration time is also accredited through control unit. ALU enumerates 20 bit output data using the data from the core array (14 bit count+11 bit residue time=25 bit total), and 20 bit integration time from the control unit. Finally the overall pixel data is transferred to the ALU unit and scaled to 20 bits by formula given in (1) and read out:

$$\text{Output Count} = \frac{(\text{Integration Time}) \times (\text{Count} + 1)}{(\text{Integration Time} + \text{Residue Time})} \quad (1)$$

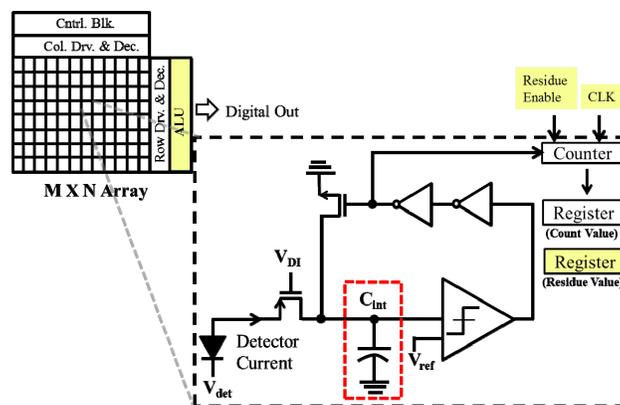


Figure 5. PFM pixel with extended integration and DROIC architecture

2.2.2 DROIC Measurement & Results

A new pixel utilizing extended integration method has been designed using 40fF integration capacitor within the pixel area of 30 x30um. As a tradeoff to design in [8] the remaining physical pixel area for digital circuits is reduced. 14 bit coarse quantization with step size of 125,000 electrons representing charge handling capacity of 2.04Ge-counter is accommodated in pixel with 11 bit residue measurement. Furthermore, 20bits representation is designated for output data in order to have appreciably higher charge capacity. Total power dissipation of the designed pixel is found to be well below 350 nW as shown in Fig.8.

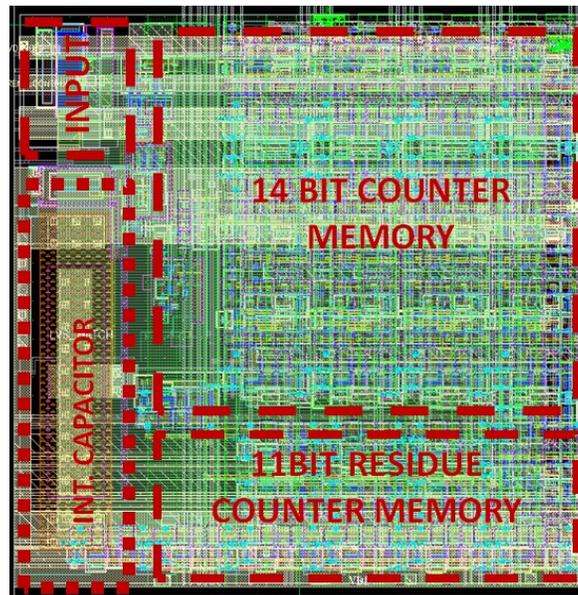


Figure 6. Frontend Pixel layout in $30\mu\text{m} \times 30\mu\text{m}$ area with 40fF integration capacitor

Layout of the designed $30\mu\text{m} \times 30\mu\text{m}$ pixel is represented in Fig. 7 with most of the circuit area still being occupied by the digital circuits. As expected power dissipation is significantly reduced by increasing the integration capacitor as presented in fig.8. The advantage is more apparent on higher input currents since the dynamic power dominates the power dissipation with great deal of switching activity. This behavior is observed mainly as a result of the slowly increasing ramp at the comparator input (integration node). Therefore, for a low power DROIC, using the largest possible integration capacitor that can be accommodated into the restricted pixel area is the optimum choice of design.

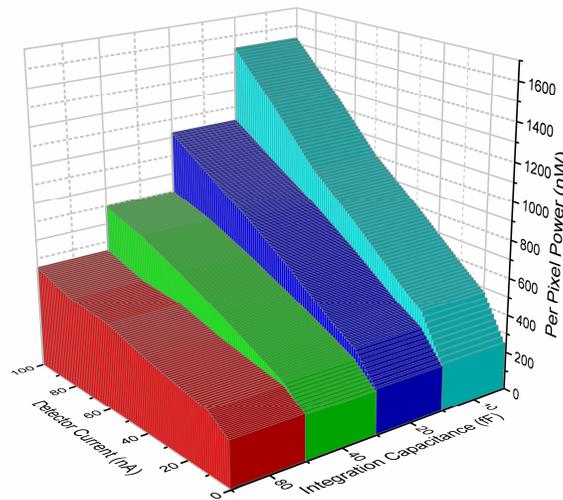


Figure 7. Power consumption per pixel with respect to input detector current for various integration capacitors

3. CONCLUSION

The digital pixel readout integrated circuit architectures for LWIR have been discussed particularly designed for scanning and staring arrays type detectors. A digital implementation of TDI algorithm is designed and implemented

which anticipate relatively lower power consumption, less chip area and low noise compared to analog counter designs. TDI is implemented on 8 pixels with sampling rate up to 3 using CMOS 180nm technology for scanning type detectors. Input referred noise of ROIC is below 750 rms electron meanwhile power dissipation appreciably under 30mW. ROIC design is optimized to perform at room as well as cryogenic temperatures.

For staring type arrays, a DROIC architecture relying on coarse quantization (PFM) is presented. It can achieve extreme charge handling capacity of 2.04Ge⁻ with 20 bit output resolution and power dissipation well below 350 nW in CMOS 90nm technology. Low power design approach has been described for DROICs. The design approach is based on PFM methodology utilizing extended integration by resizing the integration capacitor to the maximum possible value that can be accommodated in the 30 μ m x 30 μ m pixel area, thereby, moderately degrading the quantization noise. The improvement in power dissipation per pixel is considerable low with respect to [8] for higher photocurrent values. This power reduction is exceptionally significant since it extends the use of PFM DROICs for fast frame rate large scale (1024x1024) FPAs whereas no trade-off to quantization noise and charge handling capacity specification for the same pixel area.

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