An X-Band Slow-Wave T/R Switch in 0.25-μm SiGe BiCMOS

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***Abstract*—This brief presents a fully integrated X-band transmit/receive (T/R) switch using slow-wave transmission lines for X-band phased-array radar applications. The T/R switch was fabricated in a 0.25-μm SiGe bipolar CMOS (BiCMOS) process and occupies 0.73-mm^2 chip area, excluding pads. The switch is based on shunt–shunt topology and employs isolated n-channel (NMOS) transistors and slow-wave microstrip lines. Additionally, resistive body floating and dc biasing are employed to improve the power-handling capability ($P_{1\,\mathrm{dB}}$) of the switch. The T/R switch resulted in a measured insertion loss of 2.1–2.9 dB and isolation of 39–42 dB from 8 to 12 GHz. The input referred $P_{1\,\mathrm{dB}}$ is 27.6 dBm at 10 GHz. To our knowledge, this brief presents the utilization of slow-wave transmission lines in T/R switches for the first time. Furthermore, it can simultaneously satisfy stringent isolation, insertion loss, and power-handling capability requirements for implementing a fully integrated SiGe T/R module.**

***Index Terms*—Body floating, CMOS integrated circuits, MOSFET switches, SiGe bipolar CMOS, single-pole double-throw switch, transmit/receive (T/R) switch.**

I. Introduction

THE PHASED arrays consist of thousands of antenna elements spaced at the fractional wavelength of operation to steer the radiated beam electronically. The performance of these systems is determined using several figures of merit (FOMs) for search and track accuracy. Among these, the power–aperture–gain product for tracking is a widely used FOM for performance evaluation [1]. It shows a cubic relationship with the number of elements since total radiated power, antenna aperture, and antenna gain depend linearly on the number of antenna elements. Therefore, for a given track FOM, the radiated power per element can be drastically reduced at the expense of a modest increase in the number of radiating elements [2]. Exploiting this fact, the cost of next-generation radar systems could be significantly reduced by moving toward the use of lower power transmit/receive (T/R) modules in a low-cost technology with high integration capabilities. However, the power for each T/R module cannot be too low since, otherwise, impractical numbers of elements would be required. For the next-generation low-cost T/R modules, the optimum power levels are 0.5–2 W [2].

With the recent advances in heterojunction bipolar transistors, SiGe bipolar CMOS (BiCMOS) technology is capable of putting out the required power levels at X-band while also preserving the cost and yield advantages of the CMOS process. Therefore, it has been considered a viable and cost-effective solution for next-generation T/R modules. Recent works in the literature have demonstrated high-performance low-noise amplifiers [3], [4], phase shifters [5], and watt-level power amplifiers [6] for X-band T/R modules in SiGe. However, implementation of a high-performance T/R switch that can handle high transmit power levels and provide high isolation and a low insertion loss is still a major bottleneck for realizing fully integrated SiGe BiCMOS T/R modules. Therefore, single-ended RF switch design at X-band has become an active area of research in recent years. X-band CMOS single-pole double-throw switches based on shunt and series–shunt topology was reported in [8] with $\sim$2-dB loss, $\sim$23-dB isolations, and 10.1–11.1-dBm power-handling capabilities. By using a diode connected to 200-nm SiGe heterojunction bipolar transistors, an insertion loss of $\sim$2 dB and isolation of 35–58 dB were demonstrated in [9] at X-band, but with a limited power-handling capability ($\sim$11 dBm). An ultra broadband switch using synthetic transmission lines, body-floating, and biasing techniques demonstrated a considerably higher power-handling capability of 25.4 dBm at 10 GHz. Although good performances for insertion loss and isolation were achieved in previous works, none of the them was able to handle the output power levels required for viability of SiGe T/R modules ($>$ 27 dBm) while also achieving good isolation and insertion loss at the same time. While promising results on power-handling capability (28.2 dBm) with good isolation have been reported in the technology same as in this brief [7] by combining body-floating, impedance transformation, and source/drain biasing techniques, its insertion loss is quite high to be of practical use. The high insertion loss in that switch is mainly attributed to the isolated n-channel MOS (NMOS) transistors models. The main switching function in [7] is performed by series transistors, which are placed in the signal path. The insertion loss is mainly dominated by the series switches in series–shunt switch configuration so that modeling discrepancies have a direct impact on the insertion loss. To design a T/R switch that

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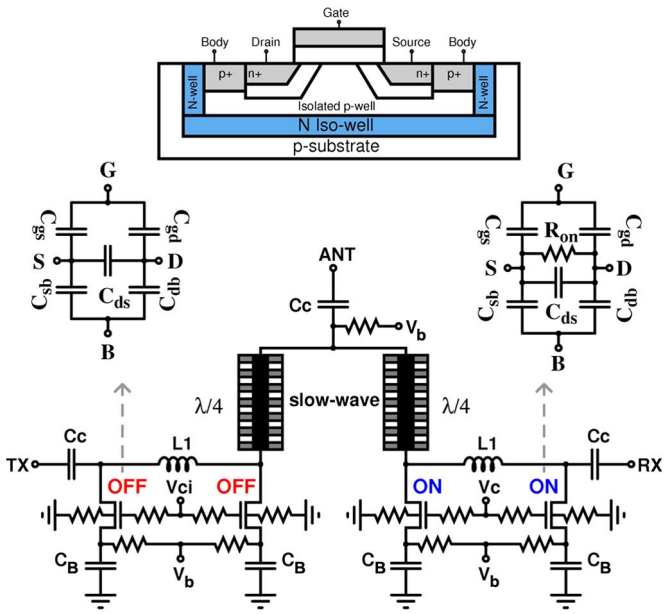

Fig. 1. Schematic view of the X-band slow-wave T/R switch and the cross-sectional view of a typical isolated NMOS transistor on the top.

is less vulnerable to the modeling issues, this brief replaces series switching transistors with on-chip slow-wave transmission lines.

This brief presents the design and implementation of a fully integrated single-ended X-band T/R switch that can satisfy all the stringent requirements of an X-band T/R module. This brief also presents the utilization of slow-wave transmission lines for the T/R switch design for the first time in CMOS technology. The remainder of the brief is organized as follows. Section II presents the design of the T/R switch. In Section III, the measurement results of the switch are given. Finally, conclusions are drawn in Section IV.

II. Circuit Design

Fig. 1 presents the schematic of the T/R switch using slow-wave quarter wavelength $(\lambda/4)$ transmission lines. The T/R switch is based on shunt–shunt configuration in order to further improve isolation. The operation of the switch is as follows. When V_c is high and V_{ci} is low, the T/R switch operates in the transmit mode. In this mode, the $\lambda/4$ line between the antenna (ANT) and receiver (RX) ports transforms the low ON resistance of shunt switches into high impedance to isolate the RX port from the transmitter (TX) port while the RF signal is routed from the TX port to the ANT port. Due to symmetry, operation of the T/R switch is similar when the control voltages are inverted. This configuration allows improvement in insertion loss over conventional series–shunt topology (particularly in less scaled technologies such as 0.25 μm) since it does not employ series transistors that usually bring relatively high parasitics in the signal path.

The main challenge in this configuration is to implement high-quality quarter length transmission line in a relatively small chip area at X-band. For that purpose, slow-wave microstrip lines are employed [10]. Figs. 2 and 3 show the structure and cross section of the slow-wave microstrip transmission

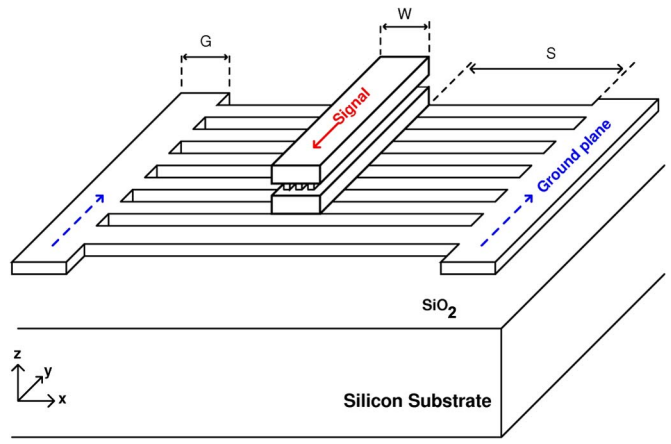

Fig. 2. Structure of the S-MSL.

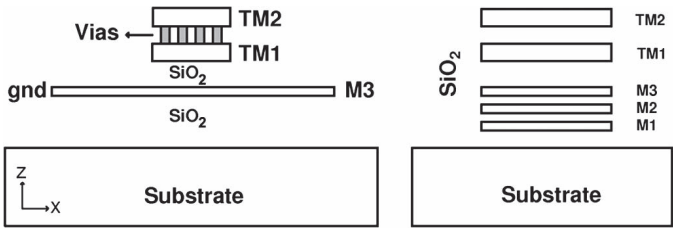

Fig. 3. Simplified cross section of the slow-wave transmission line and metal layers in the technology.

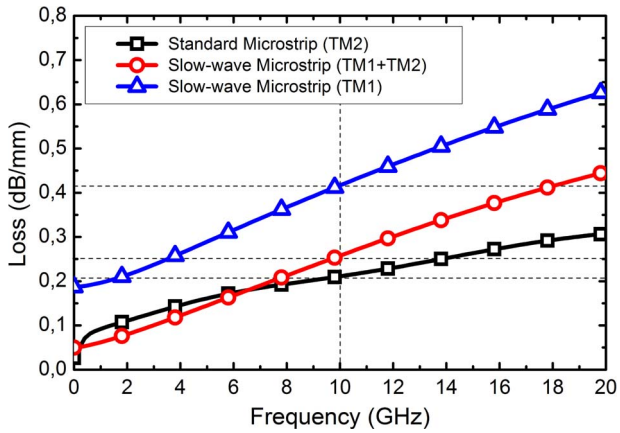

Fig. 4. Comparison of the slow-wave microstrip to the conventional microstrip and effect of metal stacking on the loss.

lines (S-MTLs) embedded in the back-end-of-line step of the IHP SG25H3 process. The back end of this technology offers three thin aluminum metal layers along with two thick metal layers for high-quality on-chip inductor and transmission-line design. The 50-Ω transmission lines are built by stacking 3-μm thick TM2 and 2-μm thick TM1 top metal layers with a width of 6 μm to reduce the loss. Fig. 4 compares the simulated losses of a slow-wave microstrip line using only TM1 and one with a TM1 and TM2 stack as a signal layer. Stacking TM1 and TM2 layers reduces the loss by 0.17 dB/mm. This improvement could be explained by a skin-effect phenomenon. The typical number of skin depth at 10 GHz is around 0.7 dB/mm. Since the skin depth is the depth at which conductor's current is reduced to 1/e of the surface values, increasing

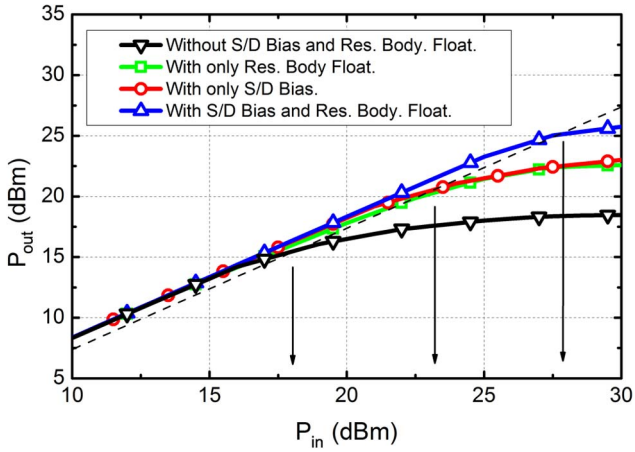

Fig. 5. Simulated input $P_{1\,\mathrm{dB}}$ of the T/R switch at 10 GHz, with and without source/drain biasing and resistive body-floating techniques.

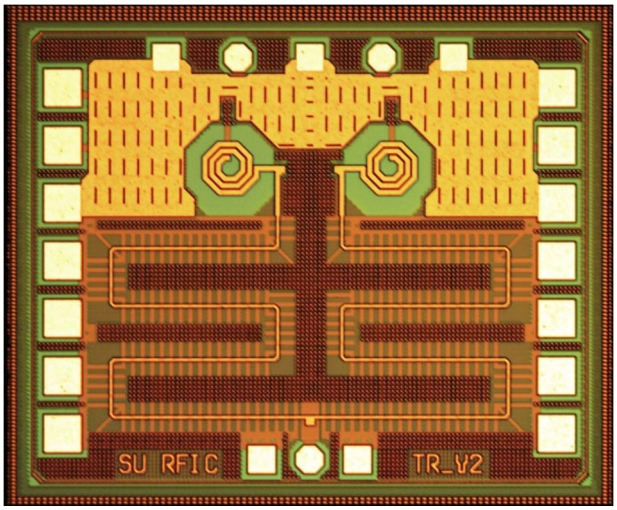

Fig. 6. Die photo of the T/R switch. The active chip area is 0.77×0.95 mm^2.

the line thickness would negligibly improve the loss after 4–5 skin depth (2.8–3.7 μm at X-band). Similarly, loss could be further improved by stacking multiple layers to create a ground plane.

The signal line is periodically loaded with capacitance using grounded metal stripes that are orthogonal to the signal propagation direction to reduce the phase velocity of the signal. The ground plane is placed on the M3 layer to increase the capacitance per length. The distance between the signal line and the ground plane is 0.9 μm. Additionally, high inductance per unit length is provided by the fact that the return current in the signal direction can only flow far away from the signal line since the metal stripes under the signal line are orthogonal to the propagation direction. The width of the grounded metal stripes is set to 10 μm and they are separated by slot widths of 10 μm. The ground plane with metal slots also prevents electric fields from penetrating into the lossy substrate and thus reduces the attenuation of S-MSL. The EM simulations of the S-MSL were performed in Sonnet. The electrical length of $\lambda/4$ is achieved with 1700-μm-long S-MSL with a simulated loss of 0.25 dB/mm at 10 GHz (see Fig. 4). This correlates to a 50% reduction in wavelength at 10 GHz. The loss of a regular

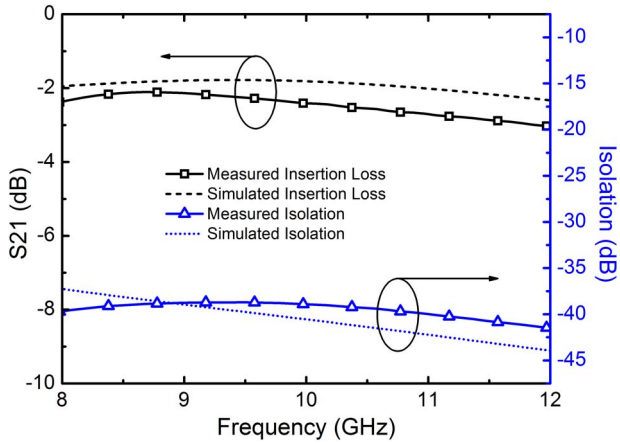

Fig. 7. Measured insertion loss and isolation of the S-MSL-based T/R switch.

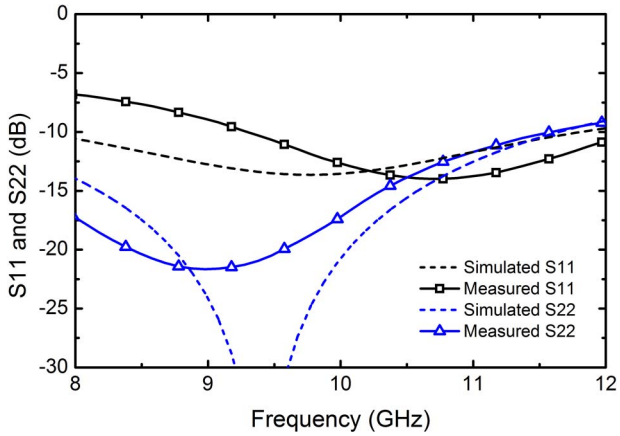

Fig. 8. Measured return losses of the S-MSL-based T/R switch.

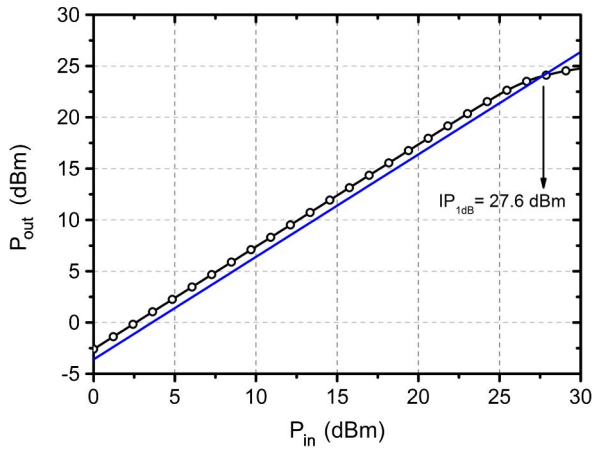

Fig. 9. Measure input $P_{1\,\mathrm{dB}}$ of the T/R switch at 10 GHz.

microstrip line using TM1 and TM2 as the signal layer is 0.22 dB/mm. The increased loss in the slow-wave microstrip can be attributed to the fact that the signal layer is not perfectly shielded from the substrate and that it is experiencing the lossy substrate through the slots on the ground plane. The total loss of the quarter wavelength line (0.42 dB) is quite better than that of a conventional microstrip (0.75 dB) due to the reduction in wavelength.

TABLE I
COMPARISON OF THE SWITCH WITH REPORTED WORKS AT X-BAND

Frequency (GHz)	Figures of Merit			Chip Area (mm^2)	Technique	Technology	Ref.
	IL (dB)	Isolation (dB)	P_{1dB} (dBm)				
8-12	**2.1-2.9**	**39-42**	**27.6**	**0.73**	**Shunt, Body floating, S-MSL, S/D biasing**	**0.25 µm SiGe BiCMOS**	**This work**
8-12	3.2 – 4.1	23.2-34.8	28.2	0.44	Body floating, ITN, Parallel Resonance, S/D Biasing	0.25 µm SiGe BiCMOS	[7]
10	1.81	21.9	10.1	0.67	Shunt	0.13 µm SiGe BiCMOS	[8]
	2.25	23.1	11.1	0.58	Series/Shunt		
3-10	3.1 ± 1.3	25–32	18-20	0.62	Distributed Topology	0.18 µm CMOS	[13]
3-10.6	2.2 – 4.2	33–37	-	0.9	Synthetic Transmission Line	0.25 µm CMOS	[14]
DC-20	0.7 @10 GHz	32 @10 GHz	25.4 @10 GHz	0.06	Synthetic transmission line, body floating and biasing	0.18 µm CMOS	[15]

In addition to the slow-wave concept, various techniques were incorporated into the design to improve the power-handling capability (input $P_{1\,\mathrm{dB}}$) [11]. First, drains and sources of the transistors are biased with 2 V to improve $\mathrm{IP}_{1\,\mathrm{dB}}$. Additionally, a resistive body-floating technique is used to further improve the power-handling capability. The isolated NMOS transistors are used to separate the body of each transistor from the common p-substrate. The transistor bodies are tied to the ground using 5-kΩ resistors to improve the power-handling capability. The effect of these two techniques are simulated and shown in Fig. 5. Without the source/drain biasing and resistive body floating, the input $P_{1\,\mathrm{dB}}$ is around 18 dBm. Fig. 5 shows that each technique improves $P_{1\,\mathrm{dB}}$ around 5 dB. A transistor width of 300 μm was chosen for shunt transistors, considering the tradeoff between the insertion loss and isolation. These transistors exhibit ON-resistance R_{on} of 3.2 Ω, OFF-capacitance C_{off} of 255 fF, and a source/drain breakdown voltage $\mathrm{BV}_{\mathrm{dss}}$) of 4.8 V. The OFF-state capacitance of the shunt transistors are resonated out by 600-pH L1 inductor [12].

III. MEASUREMENT

The die photo of the T/R switch is shown in Fig. 6. The active chip area, excluding pads, is $0.77\ \mathrm{mm} \times 0.95\ \mathrm{mm} = 0.73\ \mathrm{mm}^2$. L1 inductors lay out on the signal path and they are custom designed using the thickest top metal layer in the process to achieve higher quality factors.

The measurements of the switch were directly performed on the die using Cascade Microtech 40-GHz GSG probes. Pad-to-pad S-parameter measurements were performed using the 20-GHz Agilent 8720ES network analyzer under a bias of 2 V with control voltages of 4.5 and 0 V. Fig. 7 shows the simulated and measured insertion loss and isolation of the T/R switch. The T/R switch resulted in a measured insertion loss of 2.3 dB and isolation of 39 dB at 10 GHz. The insertion loss of the switch is between 2.1 and 2.9 dB across the X-band frequencies. The isolation of the T/R switch is between 39–42 dB at X-band. The RF pads were simulated in the Sonnet EM solver between the simulation and measurement results are 0.3–0.7 dB for the insertion loss and $\pm$2.5 dB for the isolation. The return losses at the TX port vary from 7 to 14 dB at X-band and the return loss at the ANT port changes from 9 to 22 dB across the X-band frequencies (see Fig. 8). The isolation of the T/R switch is between 39–42 dB at X-band. The RF pads were simulated in the Sonnet EM solver and resulted in a loss of $\sim$0.1 dB at 10 GHz. The discrepancy between the simulation and measurement results are 0.3–0.7 dB for the insertion loss and $\pm$2.5 dB for the isolation. The return losses at the TX port vary from 7 to 14 dB at X-band and the return loss at the ANT port changes from 9 to 22 dB across the X-band frequencies (see Fig. 8).

Insertion loss and return losses are almost the same in both transmit and receive modes due to the symmetry of the switch. The power-handling capability of the switch is measured using the Agilent E4417A power meter. Fig. 9 shows the input referred $P_{1\,\mathrm{dB}}$ of the T/R switch for a single-tone input signal at 10 GHz. As shown, input $P_{1\,\mathrm{dB}}$ is 27.6 dBm at 10 GHz.

Table I summarizes the performance of the reported switch versus other state-of-the-art single-ended CMOS T/R switches. This brief achieves an excellent isolation, a high power-handling capability and competitive insertion loss simultaneously at X-band. This can be attributed to utilization of slow-wave transmission lines, which is the first time in CMOS T/R switch design, as well as combining various techniques, such as body floating and source/drain biasing, in an effective way.

IV. CONCLUSION

This brief has presented a fully integrated X-band T/R switch fabricated in 0.25-μm SiGe BiCMOS technology. The T/R switch exhibit a measured insertion loss of 2.1–2.9 dB, isolation of 39–42 dB and input $P_{1\,\mathrm{dB}}$ of 27.6 dBm at X-band. Thus, it can simultaneously satisfy all the stringent requirements (high power-handling capability, high isolation, and low insertion loss) for X-band T/R switches, which can pave the way for implementing fully integrated T/R modules in SiGe technology.

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