REALIZATION of READOUT INTEGRATED CIRCUIT (ROIC) for an ARRAY of 72×4, P-on-N type HgCdTe LONG WAVE INFRARED DETECTORS

by

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Keywords: Readout integrated circuit (ROIC), focal plane array (FPA), scanning FPA, time delay integration (TDI)

Abstract

Infrared Focal Plane Arrays (IRFPAs) are important and high-tech systems, which are used in many strategic applications, such as medical imaging, missile guidance, and surveillance systems. The most important building blocks of IRFPAs are detectors and Readout Integrated Circuit (ROIC). Both of them need careful design and implementation for the overall system to be succesful. Detector part produces the photon induced current and sent to the input of ROIC. Detector design and fabrication determines the operating wavelength and main noise performance of the imaging system. On the other hand, ROIC is the interface element between the detector and microcomputer of the IRFPA system, and determines important performance parameters of the overall system; such as linearity, dynamic range, injection efficiency, noise performance (less effective than detector), and power consumption. Therefore it is important to design and implement a ROIC, that fits best to the desired application.

In this thesis, a CMOS ROIC is designed and implemented for scanning type of 72×4 P-on-N HgCdTe detector array in 0.35 μm, 4 metal 2 poly AMS CMOS process. Current Mirror Integration (CMI) is used as the unit cell of the ROIC. For the signal processing, Time Delay Integration (TDI) over 4 elements with an optical supersampling rate of 3 is used for improved Signal-to-Noise Ration (SNR). The designed and implemented ROIC has the properties of bidirectional scanning, variable integration time, adjustable gain settings, bypass functionality, automatic gain adjustment, and pixel selection/deselection functionality. ROIC is programmable through a serial and a parallel interface. Gain settings, TDI scanning direction, information of mulfunctioning pixels, ROIC operation mode (test or TDI) can be programmed by using these interfaces. Operating frequency of the ROIC is up to 5 MHz, while the dynamic range is 2.8 V.

72×4, P üzeri N türü HgCdTe UZUN DALGA BOYU KIZILÖTESİ DEDEKTÖR DİZİNİ için ENTEGRE OKUMA DEVRESİNİN GERÇEKLEŞTİRİLMESİ

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Anahtar kelimeler: Entegre okuma devresi (ROIC), odaksal düzlem dizileri (FPA), taramalı FPA, zaman geciktirmeli toplama (TDI)

Özet

Kızılötesi görüntüleme sistemleri medikal görüntüleme, güdümlü füze ve gözetleme sistemleri gibi stratejik uygulamalarda kullanılan önemli, yüksek teknoloji içeren sistemlerdir. Bu sistemlerin iki en önemli bileşeni dedektör ve okuma devresidir (ROIC). Her iki bileşen de sistemin en yüksek performansla çalışabilmesi için dikkatli tasarım ve uygulama gerektirir. Dedektör kızılötesi ışımayı foton akımına dönüştürerek okuma devresine gönderir. Dedektör aynı zamanda sistemin hangi dalga boyunda çalışacağını ve gürültü performansını belirler. Okuma devresi (ROIC) ise dedektör ile görüntü sinyalini işleyecek olan mikrodenetleyici arasında bir arayüzdür, ve doğrusallık, salınım aralığı, foton akımının yüksek oranda alınması, gürültü performansı, güç tüketimi gibi sistem performansını belirleyen önemli parametreleri belirler. Bu sebeple istenilen özelliklere uygun ve uygulamaya en iyi şekilde cevap verebilecek okuma devresini (ROIC) tasarlamak ve uygulamak önem teşkil eder.

Bu tezde N katmanı üzerine P katmanıyla oluşturulmuş, 72×4 HgCdTe kızılötesi dedektör dizisi için, 0.35 µm'lik AMS üretim sistemiyle bir CMOS okuma devresi (ROIC) tasarlanmış ve fiziksel serimi yapılmıştır. Okuma devresinin giriş hücresi olarak akım aynalamalı entegrasyon (CMI) kullanılmıştır. Daha iyi sinyal-gürültü oranı (SNR) için sinyal işleme algoritması olarak 4 piksel üzerinde 3 örnekleme ile uygulanan zaman geciktirmeli entegrasyon (TDI) tekniği kullanılmıştır. Tasarlanan okuma devresinin çift yönlü tarama yapabilme, hatalı piksel belirleme, belirlenen hatalı piksellere göre piksellerin seçilip seçilmemesinin tayin edilebilmesi, hatalı piksellere göre otomotik kazanç ayarı yapılabilmesi, değişken kazanç seviyeleri seçebilme, değişken zamanlarda entegrasyon yapabilme ve seri/paralel olarak programlanabilme özellikleri mevcuttur. Kazanç seviyesi, tarama yönü, hatalı piksel bilgisi, okuma devresinin operasyon modu seri/paralel arayüz tarafından programlanabilir. Okuma devresinin çalışma frekansı 5 MHz, çıkış salınım aralığı ise 2.8 V'tur.

Acknowledgement

I have been working on this project since summer 2006 after I graduated from Sabancı University. At the end of two years of study for MSc degree in Sabancı University, I feel the technical improvement I have gained, which motivated me for further study in PhD in Electronics Enginnering. In this period, I have taped out four different chips, and measured three of them. To be a part of a team whose chips working and functioning properly is a great pleasure for me, which motivates me for further studies in this area. I would like to thank those people; my professors, co-workers, and friends; for all kinds of support they have provided for me to be part of that team.

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1 INTRODUCTION

1.1Introduction

Infrared (IR) radiation was found first in 1880 by Sir William Herschel when he was repeating Newton's experiment. He detected the heat in the region just above the visible spectrum. Planck formulated the amount of energy radiated from a blackbody as a function of temperature and wavelength in 1900. Then, during the World War II period, origins of the modern infrared (IR) imaging technologies emerged. During 1950's and 1960's infrared sensors were built using single element cooled lead salt detectors, while important improvements were made in narrow bandgap semiconductors, which would help improving wavelength and sensing capabilities. In 1970s, forward looking infrared systems (FLIR) systems were developed and charge coupled device (CCD) was invented. In the following 20 years, improvements in VLSI technology led to the design of large array sized CCD devices, which took place in parallel with the improvements in Infrared Focal Plane Arrays (IRFPA); arrays of detectors with its readout electronics on the focal plane. CCD devices are used in visible spectrum, while IRFPA devices are used in IR spectrum. In CCD technology, both detector and readout electronics are on silicon, while in IRFPA technology, due to the need to small bandgap materials, detectors and readout electronics are built on different materials which are flip chip bonded later [1].

Infrared imaging systems are used in number of applications such as medical examination, astronomy, FLIRs, missile guidance, surveillance systems and some other strategic equipments. An infrared imaging system generally consists of four parts: optical part, with scan system if it is a scanning type device, detector, readout electronics and signal processing part as shown in Fig. 1.1.

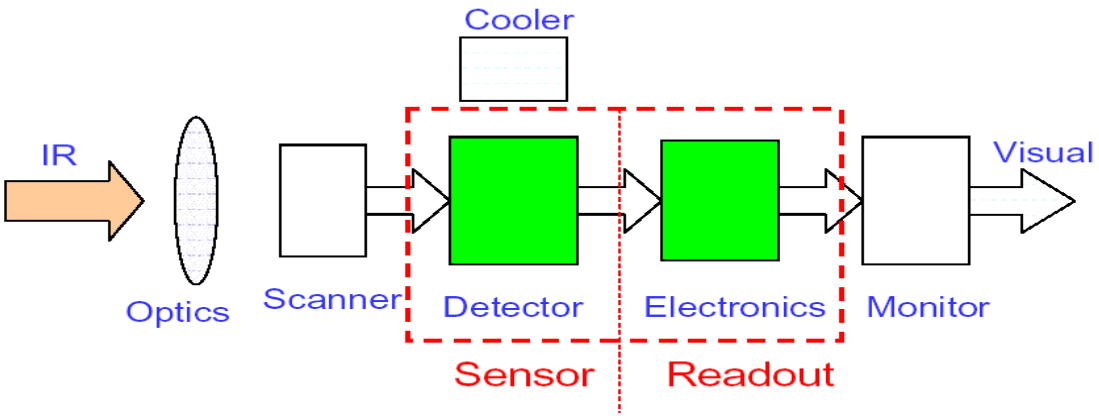

Figure 1.1: General architecture of scanning array IR imaging system

There are a couple of classification methods for FPAs, one of which is the image capturing system. In the image capture system, there two types of FPAs: Scanning Arrays and Staring Arrays:

In scanning array systems, there is one column of detector to capture the image. According to the noise reduction technique used, there can be four or seven detectors for a column of image. This type of FPAs scan the image with a constant speed and take the image column by column. Due to the scanning functionality, frame rates of these systems are slower than staring array systems. Super sampling rate, hence number of detectors for a column, should be increased to enhance the spatial resolution of scanning FPAs.

On the other hand, staring array FPAs do not use an optical scanner, instead all detector array is fabricated such as 2040×2040 array. So, there is no need to scan the image, because there are enough number of detectors to capture the image. Staring array systems have better spatial resolution and higher frame rate.

Another classification method for FPAs is based on the integration method of detector and readout electronics. There are mainly two type of structures: Monolithic array structure and hybrid array structure.

In monolitic array structure, both the detector and multiplexing part are on the same substrate, meaning that monolithic arrays are limited to silicon compatiple process. Some examples of monolithic array structures are Schottky barrier detectors, micromachining bolometers and extrinsic detectors on silicon substrate. Due to the limitation of detector types feasible for silicon process to be used in monolithic structure, their sensitivity and spectrum is limited [2].

In hybrid array structure, detector array and readout electronics are built on different substrates. They are connected through indium bumps or loophole interconnection as shown in Fig. 1.2 [3]. The interconnection method using indium bumps to connect the aligned detector array with the readout electronics is called flip chip bond technique. With this technique, every single detector is connected to its corresponding readout part via indium bumps.

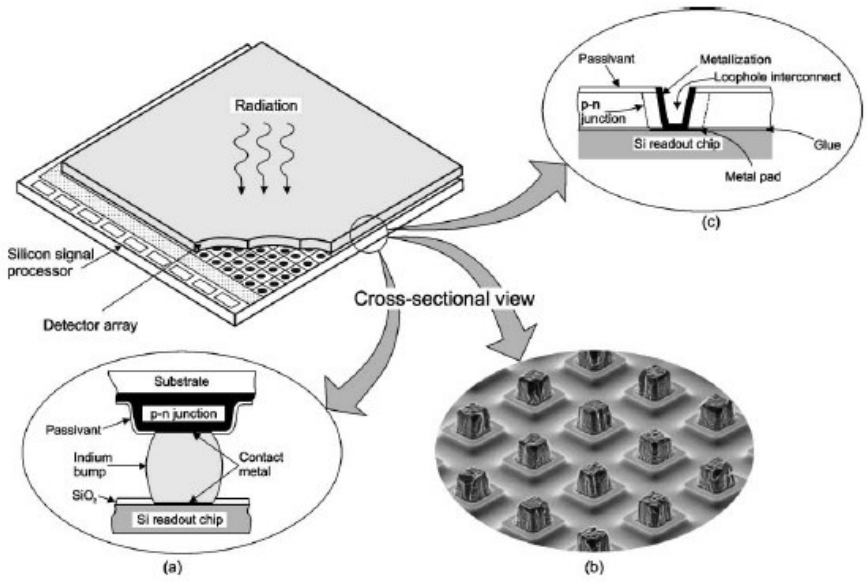

Figure 1.2: Hybrid detector array with indium bump and loophole connection techniques [3]

IRFPAs are also classified according to their detector types, which are thermal and photon detectors. The way they detect the IR illumination is different for thermal and photon detectors.

In thermal detectors, the incident radiation absorbed by the crystal lattice leads to a temperature change which changes the physical and electrical properties of the detector. They are generally operated at room temperature and have wider spectral response [2]. Due to the fact that their operation depend on temperature change, their response time is slower. Two of most general thermal detectors are pyroelectric detectors and bolometer detectors:

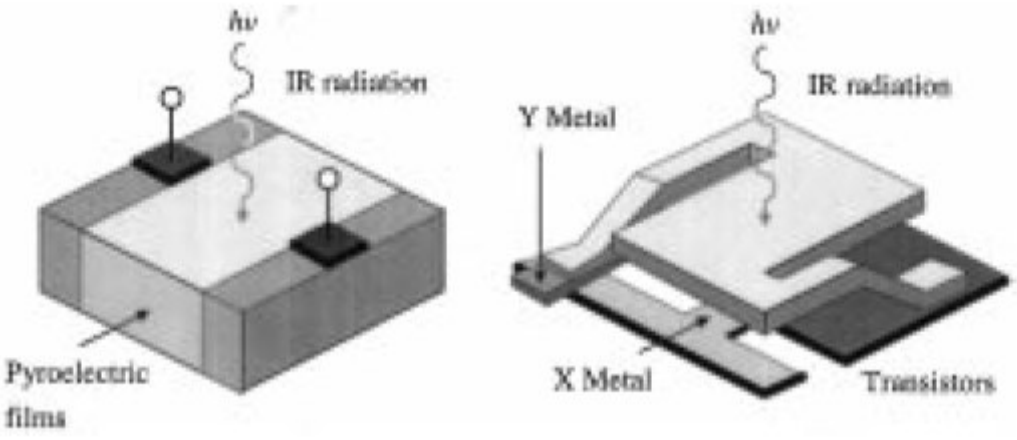

Figure 1.3: Pryoelectric detector and bolometer [2]

Pryoelectric detectors utilize pryoelectric films as shown in Fig. 1.3. Pryoelectric materials change their electrical polarization arised from a temperature change in the pryoelectric material, which causes charges to flow and generate current detected by the readout circuit. Bolometers also operate with the temperature change due to IR illumination, changing the electrical resistance of the detector. Working principle of bolometers and photoconductive detectors is similar in terms of resistance change due to IR radiation. The difference between them is that, resistance change in bolometers is directly due to heat change, while it is photon-latice interaction in photoconductive materials [2].

On the other hand, photon detectors' working principle depends on the carrier excitation due to IR radiation. IR radiation helps electrons and holes to jump between energy levels leading to photocurrent. There are some concepts such as responsivity and detectivity related to photodetectors. Responsivity is related to the quantum efficiency "η" and photoelectric gain "g". Quantum efficiency is defined as the number of electron-hole pairs

per incedent photon, while photoelectric gain is defined as carriers passing contacts per one generated pair, which means photoelectric gain is a measure of how well electron-hole pairs converted to current [4].

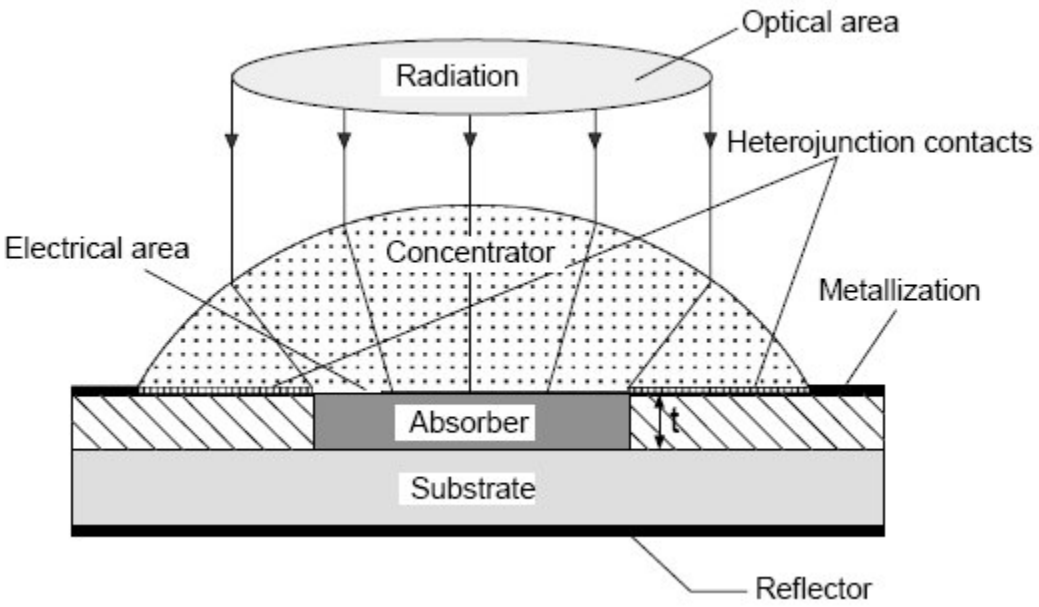

Figure 1.4: Model of photodetector [4]

Responsivity and detectivity is given in [4] as the following:

$$R_i = \frac{\lambda\eta}{hc} qg \qquad D^* = \frac{\lambda}{hc}\left(\frac{A_o}{A_e}\right)^{1/2} \eta[2(G+R)t]^{-1/2} \tag{1.1}$$

where "λ" is wavelength, "h" is Planck's constant, "c" is velocity of light, "q" is electron charge, G and R generation and recombination rates, "t" is the thickness of the detector, A_0 is optical area and A_e is the electrical area as shown in Fig. 1.4.

The most common photodetectors are phovoltaic (PV) detectors and photoconductive (PC) detectors. In PV detectors, IR radiation that has energy greater than band gap of the junction leading to electron-hole pairs, hence photocurrent. On the other hand, in PC detectors, increase in conductance of photoconductive material under constant electric field

is generated by free carriers due to photon energy. If the dopant material is intrinsic, electron-hole pairs are generated, whereas the dopant is extrinsic majority carriers are excited in PC detectors [2].

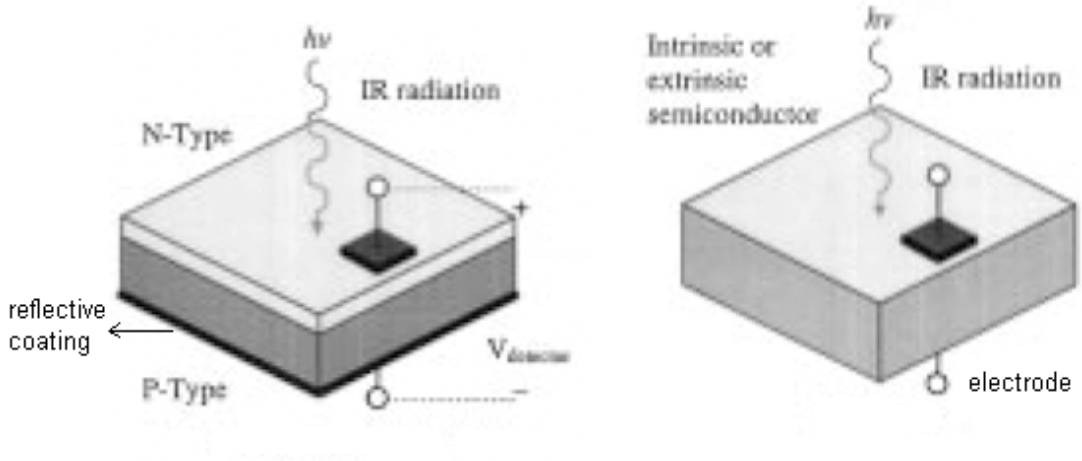

Figure 1.5: PV and PC detectors [2]

Comparison of thermal detectors and photon detectors is shown in Table 1.1[4]. According to [5], the most suitable material for infrared detection is HgCdTe, although it has disadvantages like process dificulty due to bulk growth of HgCdTe in high vapour pressure of Hg at 950 ^{0}C, cost, toxiticity and non-uniformity over large area. On the other hand, HgCdTe material has the following advantages which make it favoriable for IR detector: adjustable band gap between 0.7 µm and 25 µm, direct band gap with high absorbtion coefficient, moderate index of refraction, moderate thermal expansion coefficient and avaliability of more lattice matched materials for epitaxial growth.

Detector type			Advantages	Disadvantages
Thermal (thermopile, bolometers, pyroelectric)			Light, rugged, reliable, and low cost Room temperature operation	Low detectivity at high frequency Slow response (ms order)
Photon	Intrinsic	IV–VI (PbS, PbSe, PbSnTe)	Easier to prepare More stable materials	Very high thermal expansion coefficient Large permittivity
		II–VI (HgCdTe)	Easy bandgap tailoring Well developed theory & exp. Multicolour detectors	Non-uniformity over large area High cost in growth and processing Surface instability
		III–V (InGaAs, InAs, InSb, InAsSb)	Good material & dopants Advanced technology Possible monolithic integration	Heteroepitaxy with large lattice mismatch Long wavelength cutoff limited to 7 μm (at 77 K)
	Extrinsic (Si:Ga, Si:As, Ge:Cu, Ge:Hg)		Very long wavelength operation Relatively simple technology	High thermal generation Extremely low temperature operation
	Free carriers ($PtSi$, Pt_2Si, IrSi)		Low-cost, high yields Large & close packed 2-D arrays	Low quantum efficiency Low temperature operation
	Quantum wells	Type I (GaAs/AlGaAs, InGaAs/AlGaAs)	Matured material growth Good uniformity over large area Multicolour detectors	High thermal generation Complicated design and growth
		Type II (InAs/InGaSb, InAs/InAsSb)	Low Auger recombination rate Easy wavelength control	Complicated design and growth Sensitive to the interfaces
	Quantum dots	InAs/GaAs, InGaAs/InGaP, Ge/Si	Normal incidence of light Low thermal generation	Complicated design and growth

Table 1.1: Comparison of thermal and photon detectors [4]

The IR region is divided into five parts nearly all of them captured by different alloys of HgCdTe detectors, which are near infrared region (NIR), small wavelength infrared region (SWIR), middle wavelength infrared region (MWIR), long wavelength infrared region (LWIR) and very long wavelength infrared region (VLWIR). These infrared regions and their wavelength intervals are represented in table 1.2.

Region (abbreviation)	Wavelength range (μm)
Near infrared (NIR)	0.78–1
Short wavelength IR (SWIR)	1–3
Medium wavelength IR (MWIR)	3–6
Long wavelength IR (LWIR)	6–15
Very long wavelength IR (VLWIR)	15–1000

Table 1.2: IR wavelength intervals

Readout integrated circuits (ROICs) are important elements of IR imaging systems within the wavelengths mentioned in Table 1.2. They are the interface block between the detector and microcomputer of the imaging system,which determine the important parameters of the overall system. The general architecture of ROICs is represented in Fig. 1.6. Detector is connected to the unit cell of the ROIC through indium bumps. There are several types of unit cells, each of which has trade-offs. Unit cell is one of the most important building block of ROICs, because it determines the noise performance, dynamic range, linearity, injection efficiency, power consumption, and area of the ROIC. Unit cell is connected to a transimpedance amplifier in general, in order to transfer the charge it absorbed from the detector to the video amplifier or output buffer. This part is called the signal processing part of the ROIC. Finally, the output of video amplifier or output buffer is sampled by a off-chip or on-chip analog-to-digital converter (ADC).

One of the most important parameters of ROICs is the signal-to-noise ratio (SNR). Unit cell and amplifier noise performances are the key parameters to improve the SNR, although ROICs have considirable lower noise than the detector itself. Best noise performance for

improved SNR, wider dynamic range, less power consumption, higher linearity, small area, higher injection efficiency are desired for the best performance of ROICs, although it is most likely impossible to have all of them in onel. Therefore, the designer should choose the best unit cell for the desired application.

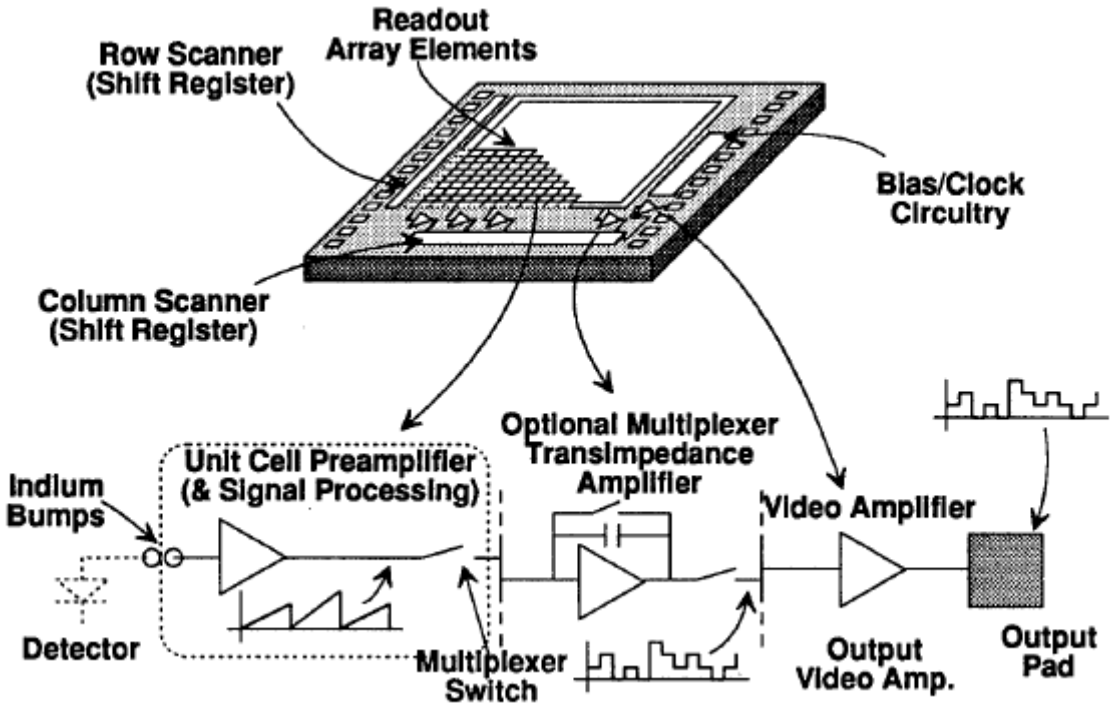

Figure 1.6: General ROIC architecture [7]

1.2 Motivation

IRFPAs are important and high-tech devices, which are used in many applications, such as medical imaging, missile guidance, and surveillance systems. ROIC is the interface element between the detector and microcomputer of the IRFPA system, and determines important performance parameters of the overall system. Therefore, it is important to design and implement this type of strategic devices in order to have the technologic capability. As it is mentioned in the previous section, two types of IRFPAa exist in general: Staring Array Systems and Scanning Array Systems. Although the frame rate and spatial resolution of staring array systems exhibit better performance; difficulty of integrating large size of

detector arrays, non-uniformity problem over large area, cost of production are disadvantages of staring array systems. It is easy and cheap to implement scanning array systems due to their relative smaller size.

In this thesis, a CMOS ROIC is designed and implemented for scanning type of 72×4 P-on-N HgCdTe detector array in 0.35 µm, 4 metal 2 poly AMS CMOS process. Current Mirror Integration (CMI) is used as the unit cell of the ROIC. For the signal processing, Time Delay Integration (TDI) over 4 elements with an optical supersampling rate of three is used for improved Signal-to-Noise Ration (SNR). The designed and implemented ROIC has the properties of bidirectional scanning, variable integration time, adjustable gain settings, bypass functionality, and pixel selection/deselection functionality. The organization of thesis is given in section 1.3.

1.3Organization of Thesis

In Chapter 2, building blocks of ROICs are explained in detail with their advantages and disadvantages. First, unit cell as the input building block of ROIC is discussed, and several unit cell architectures are examined and compared in term of linearity, dynamic range, injection efficiency, power consumption, area, and noise performance. Then, signal processing part of the ROICs is discussed, and time delay integration (TDI) algorithm, which is used in scanning array systems, are explained in detail.

In Chapter 3, implementation of ROIC for 72×4 P-on-N detector array is discussed. First, requirements of ROIC are given, and architecture of ROIC is explained. Then, design and implementation of the building blocks, some of which is discussed in Chapter 2, are explained. These building blocks are CMI unit cell, and TDI stage over 4 element with supersampling rate of 3. Following the TDI implementation, automatic gain adjustment stage, which is used to compansate the effect of dead pixels; and offset cancellation stage, which is used to subtract the erroneous voltage due to parasitic effects and switching errors, are explained. Then, output buffer stage implementation is given. Finally, design and implementation of digital control block, serial/parallel interface, and channel and address decoder are discussed.

In Chapter 4, simulation and measurement results are given. Simulations are done with minimum current, 25 nA average current, and maximum current. Simulation data is taken from integration capacitor, TDI output, offset cancellation stage, and finally output buffer stage of a 72×4 P-on-N part, which represents the whole design. Measurement results are taken from the fabricated ROIC for 4×4 P-on-N detector array, as a building block of 72×4 design. Some comments about simulation and measurement results are also provided considering the problems faced during the design and implementation process.

Finally, in Chapter 5, conclusion of this work is given, and future work is discussed.

2 ROIC BUILDING BLOCKS

2.1 Introduction

Readout integrated circuits (ROICs) are the important element of detector systems. They get the photocurrent from the detector by the help of a unit cell. Then, they process and reduce the noise level of the signal by the help of a signal processing algorithm, and finally sent the signal to the microprocessor by the help of an ADC.

Unit cells are important, because they determine most of the ROIC performance parameters, such as injection efficiency, linearity, noise contribution, dynamic range. There are several unit cell architectures, which are discussed in section 2.2 with their advantages and disadvantages.

Signal processing unit determines the noise performance of the ROIC. There are three main signal processing algorithms such as sample and hold, correlated double sampling (CDS), and time delay integration (TDI) to improve the SNR performance of the ROIC. Signal processing techniques are discussed in section 2.3.

Most of the ROICs also have additional functionalities such as variable integration time [5], adjustable gain settings [17], bidirectional scanning and by-pass mode.

By the use of variable integration time property, input photon induced current coming from the detector, can be integrated for varying amount of time, according to applications. If current integration time amount is not enough for a clear image, integration time can be increased, or for high flux irradiances it can be decreased. Adjustable gain setting is similar to the variable integration time, they are correlated. For high flux applications, the capacitor value can be increased to store more current.

By using the by-pass (test) mode, dead pixels can be determined, and ROIC can be programmed according to these data. The determined malfunctioning pixels are programmed, and these pixels are not selected during ROIC operation by the help of the pixel selection/deselection property.

Bidirectionality property allows to change the scan direction of the ROIC, which provides flexibility to the user.

At this part of the thesis, ROIC building blocks and their features are explained in detail.

2.2 Unit Cells (Preamplifiers)

2.2.1 Self Integrating Input Cell

Self integrating unit cell (SI) is the most basic unit cell that consists of a single MOSFET transistor as a switch. Photon induced charge due to infrared illumination integrates onto the stray capacitance in the unit cell which is mainly due to detector capacitance. The stray capacitance also includes the MOSFET capacitance and interconnect capacitance connected to the detector as shown in Fig. 2.1. If it is desired to increase the storage capacity, additional capacitance can be included in the unit cell.

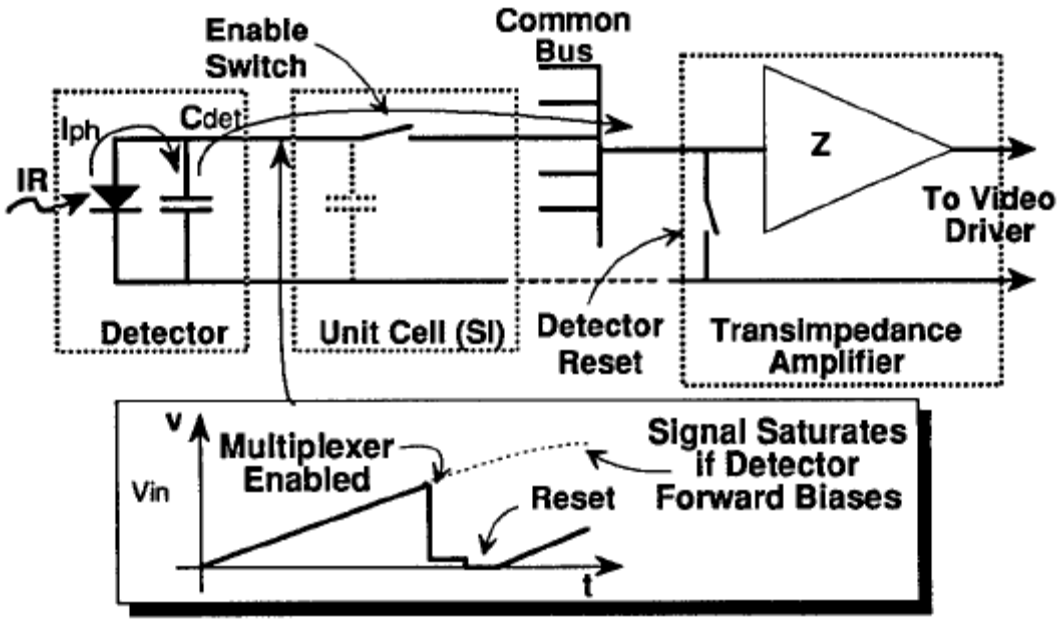

Figure 2.1: Schematic of SI unit cell and v-t graph showing the capacitance voltage with respect to time [7]

After the charge is integrated during the whole frame, stored charge in the stray capacitance is transferred to the transimpedance amplifier which has low input impedance and gain of Z as shown in Fig. 2.1[7]. After the charge transfer the transimpedance amplifier is resetted by the detector reset and the unit cell is ready for the next frame integration. The transfer function of the SI unit cell during the integration time t_{int} is given as the following in [7]:

$$V_{out} = Z \int_0^{t_{int}} I_{ph}(t)dt + ZQ_r \ [V] \quad (2.1)$$

where Q_r is the initial charge on the input node and Z is the charge-to-voltage gain.

The SI unit cell is the simplist unit cell with only one device, hence has the minumum area when compared with other unit cells. On the other hand, it has no gain in the unit cell and detector bias changes during the integration causing noise and nonlinearity. As the photon induced charge is integrated over the capacitance, it forms a ramp like voltage as in Fig. 2.1. If the integration period is long enough, the detector turns into forward-bias condition, which causes to nonlinearity due to forward-bias detector and additional shot noise. The voltage ramp will follow the (I-V) characteristics of the detector, hence the voltage in the input node will follow the the characteristics of the diode. The I-V characteristics of the diode is highly nonlinear due to the change in the diode from reverse-biased condition to forward-biased condition.[7] The dynamic range of the SI unit cell also depends on the voltage of the input node which is not desirable. SI unit cell suffers from the kTC noise like all other switched capacitor applications, together with thermal noise and photon noise.

2.2.2 Source Follower per Detector Input Cell

Source follower per detector unit (SFD) is very similar to SI unit cell, except the additional MOSFETs for voltage mode output and reset operation. It is advantageous for small unit cell requirements like SI unit cell.

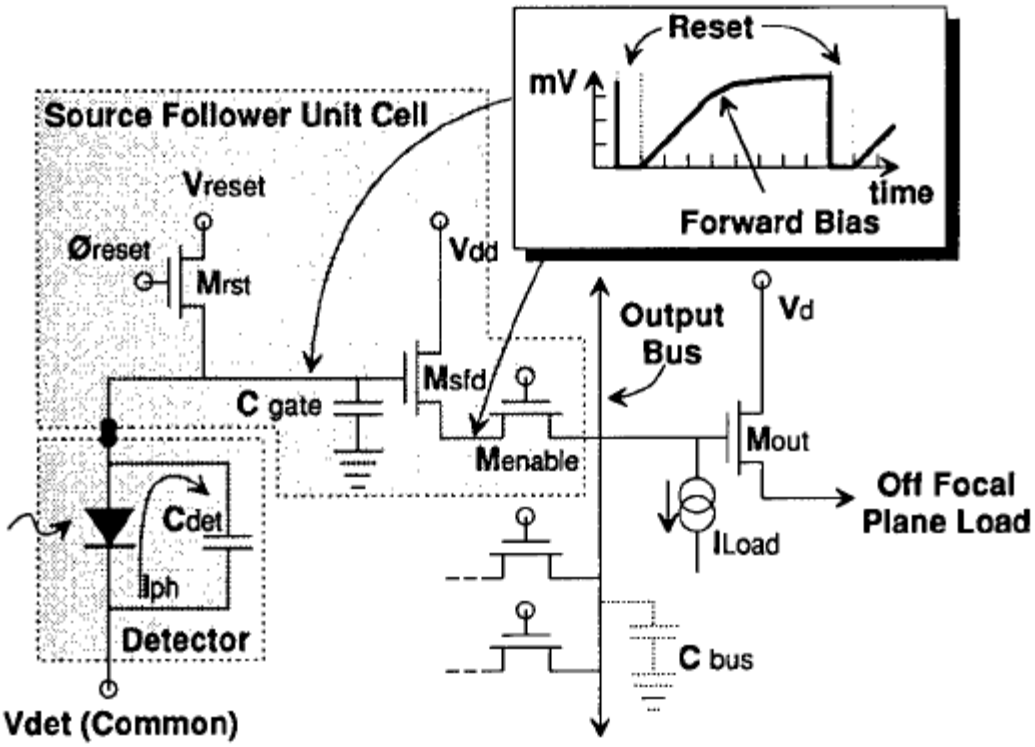

Figure 2.2: Schematic of SFD unit cell [7]

Photon induced current is integrated onto the capacitance formed by the gate of the source follower MOSFET, interconnect and detector capacitance as in Fig. 2.2. The ramp input voltage of the SFD is buffered by the source follower, where it is different from SI unit cell [7]. Since the SFD unit cell has voltage mode output due to source follower, there is no need for bus amplifier. After the integration is completed at the end of the frame, the input node is reset by the reset MOSFET and SFD unit cell becomes ready for the next integration cycle. The dynamic range of SFD unit cell is also limited by the I-V characteristics of the detector like the SI unit cell [7]. The dark and photon current I_{det} is stored on the stray capacitance C during the integration time t_{int} and results in a voltage at the input node:

$$V_{in} = \frac{I_{det}\ t_{int}}{C}\ [V] \tag{2.2}$$

If the input node voltage exceeds the voltage limit, the detector will become forward-biased leading to nonlinearity and shot noise like the SI unit cell. Additional capacitance option is also available for SFD unit cell according to the application. SFD is suitable for low background application, where long integration time is possible without violating linearity concern. SFD unit cell also suffers from kTC noise as well as 1/f noise and MOSFET thermal noise.

2.2.3 Capacitor Feedback Transimpedance Amplifier Unit Cell

Capacitor feedback transimpedance amplifier (CTIA) unit cell is compatible with various detectors and has a good performance in terms of detector bias stability, high injection efficiency, high gain and low noise [7].

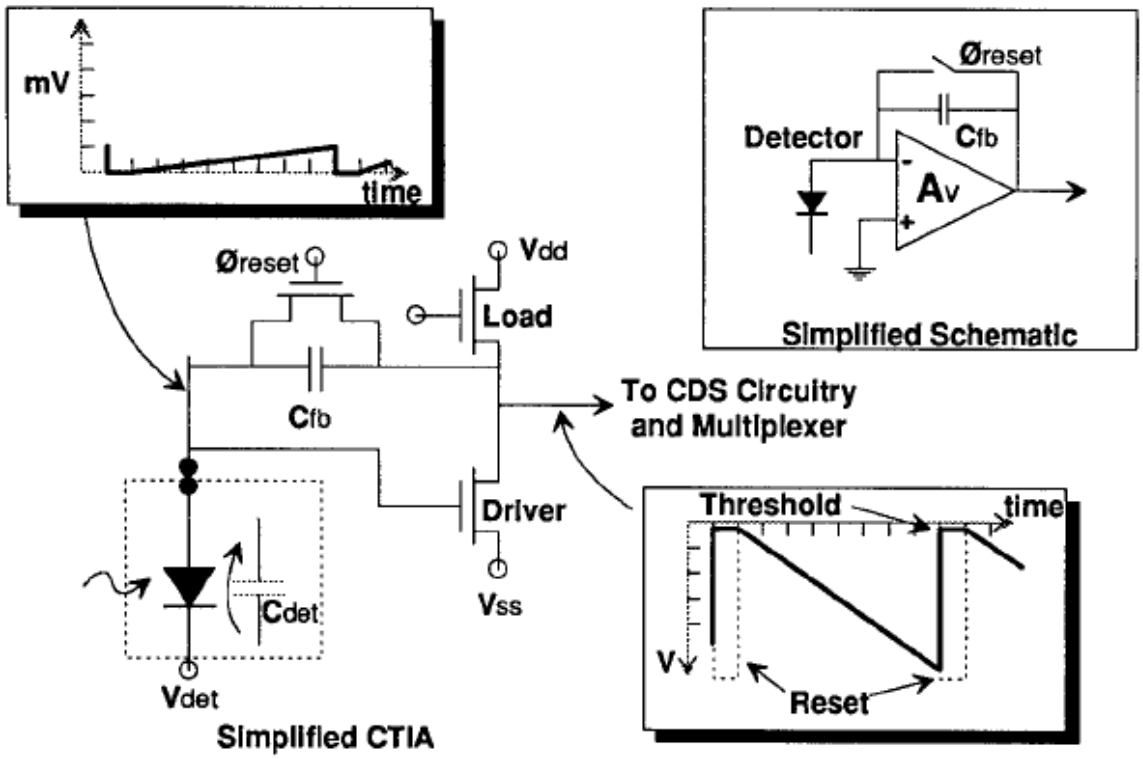

Figure 2.3: Schematic of CTIA unit cell [7]

The photon induces charge causes a slight change at the inverting input of differential amplifier, which has a high open loop gain. The amplifier responds this slight input change

with a sharp output voltage reduction, which causes charges to flow onto the feedback capacitor as an opposition to the initial effects of charges. Detector current is integrated onto the feedback capacitor by this mechanism during the frame, which causes a decreasing ramp at the output of the amplifier. At the end of the integration time, the voltage output is sampled and multiplexed to the output, then the amplifier is reset for the next frame and integration period. Correlated double sampling (CDS) signal processing technique is used with CTIA unit cell architecture in general.

$$V_{out} = \frac{I_{ph} t_{int}}{C_{fb}} \; [V] \tag{2.3}$$

The CTIA gain can be expressed like in equation 2.3, where C_{fb} is the feedback capacitor, while CTIA transimpedance Z_t is defined as in equation 2.4 [7].

$$Z_t = \frac{V_{out}}{I_{ph}} = \frac{t_{int}}{C_{fb}} \; [\frac{V}{A}] \tag{2.4}$$

The main noise contributor of CTIA unit cell architecture is the input transistors of the differential amplifier, while other noise sources can be negligible with the use of some techniques mentioned in [7].

2.2.4 Direct Injection Unit Cell

Direct injection (DI) unit cell is the second smallest unit cell that is used in medium and high photon irradiance applications. In low irradiance conditions, small amount of current is not enough for high g_m, which is required for low impedance and stable biased detector. Low impedance drops the injection efficiency of the detector, which results in lower signal-to-noise (SNR) ratio also.

The photon induced current is injected through the source of the MOSFET and integrated onto the integration capacitor, which is in reset position before as shown in Fig. 2.4. After the charge integration is completed throughout the frame, integration capacitor is reset, and the circuit is ready for the next frame. Gain of the DI unit cell is determined by the

integration capacitor, which is not dependent on stray capacitance. A source follower can be used for voltage mode output.

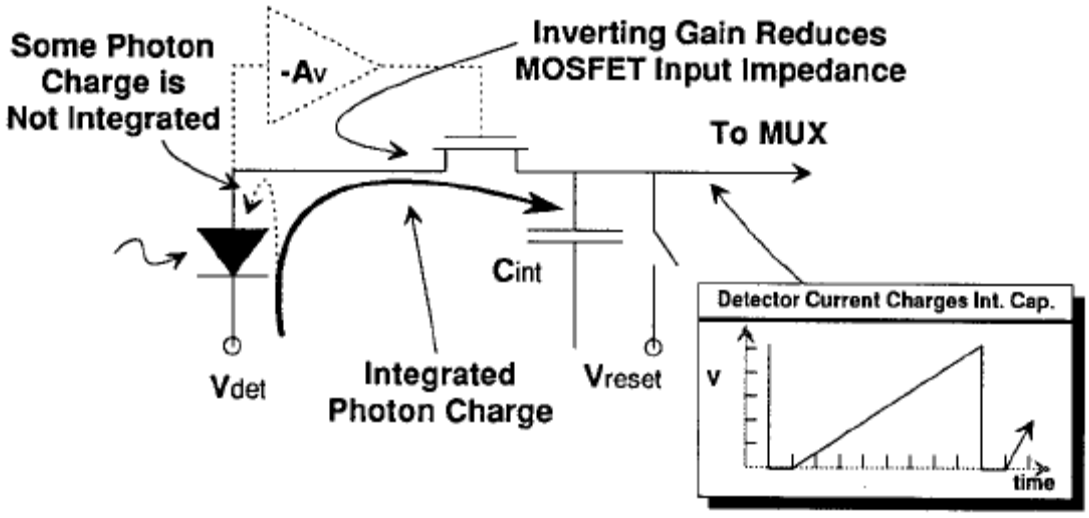

Figure 2.4: Schematic of DI and BDI unit cells [7]

In order to reduce the detector noise, stable near-zero voltage should be supplied to the detector, especially for LWIR detectors, because they have significant dark current in reverse bias condition [7]. In DI unit cell detector bias is not given directly to the input node, instead, threshold voltage of the MOSFET is added to the gate voltage of the MOSFET. Due to the 10-50 mV MOSFET threshold voltage variations, an appropriate detector common voltage should be given to prevent higher detector noise near forward bias condition. This comes with a disadvantage of excessive reverse bias for some detectors, which leads to more 1/f noise and more detector dark current [7].

The input cell also should provide low input impedance to the detector for stable detector bias and high injection efficiency. If the input impedance of the unit cell is high, some part of the photon current can be injected into the source of MOSFET and lost, resulting in a loss of SNR. The injection efficiency is defined as the following where, I_{int} is the

integration current, I_{ph} is the photon current, r_{det} is the detector resistance and g_m is the transconductance of the MOSFET:

$$Injection\ efficiency = \frac{I_{int}}{I_{ph}} = \frac{r_{det} g_m}{1 + r_{det} g_m} \left[\frac{A}{A}\right] \tag{2.5}$$

The transconductance gm of the MOSFET in weak inversion (subthreshold) region depends on the current, where DI unit cell mostly operates [7]. The relationship between the drain current of the MOSFET and gate-to-source voltage in subthreshold region is given as the following for n-channel MOSFET, where K_1 includes geometry and operational characteristics of MOSFET in [7]:

$$I_d = \frac{W}{L} \mu_n K_1 exp\left(V_g - \frac{mkT}{q}\right) [A] \tag{2.6}$$

The transconductance g_m the derivative of the drain current with respect to gate-to-source voltage:

$$g_m = \frac{\delta I_d}{\delta V_{gs}} = \frac{I_d q}{mkT} [mhos] \tag{2.7}$$

As it is seen from the equation 2.7, g_m is independent of device geometry, direct function of drain current I_d. Because of this reason, DI unit cell is suitable for high flux applications, in low flux applications, due to low gm value, injection efficiency is low.

Low gm value also affects the bandwidth of the detector, causes frame to frame crosstalk. If gm is the dominant impedance on the detector node, frequency of the detector is given as the following in [7] where C_{gs} is the MOSFET gate-to-source capacitance:

$$f(-3\ dB) = \frac{g_m}{\pi\left(C_{\text{det}} + C_{gs}\right)} [Hz] \tag{2.8}$$

Due to the fact that g_m is proportional to drain current of the MOSFET, DI unit cell is not suitable for high speed and low flux applications, because with low flux g_m value is smaller, results in less bandwidth according to equation 2.8.

The noise contributors for DI unit cell are same, MOSFET noise, kTC thermal noise and 1/f noise. One difference of DI unit cell is that, the input MOSFET noise of the DI unit cell results in the output current as a function of detector resistance. If the detector resistance is dominant resistance meaning high injection efficiency, MOSFET noise becomes negligible with respect to the detector noise [7].

2.2.5 Buffered Direct Injection Unit Cell

Buffered direct injection (BDI) unit cell is very similar to DI unit cell, except the inverting amplifier between the gate of the injection MOSFET and detector as shown in Fig. 2.4. The inverting amplifier reduces the the input impedance of the DI unit cell and increases the injection efficiency and bandwidth as a plus to DI unit cell by introducing the feed-forward mechanism [7]. The injection efficiency becomes:

$$Injection\ efficiency = \frac{I_{int}}{I_{ph}} = \frac{r_{det} g_m (1 + Av)}{1 + r_{det} g_m (1 + Av)} \left[\frac{A}{A}\right] \tag{2.9}$$

BDI unit cell also suffers from low flux limitation because of the MOSFET's low g_m due to low drain current. The cut-off frequency of the DI unit cell is also improved due to the inverting amplifier between the detector and gate of the injection MOSFET. The C_{gs} gate-to-source capacitance of the MOSFET in equation 2.8 can be replaced by the new C_{gs} value:

$$Cgs' = Cgs(1 + Av) \tag{2.10}$$

The dominant noise contributor of the BDI unit cell is the MOSFET preamplifier noise of the inverting amplifier. The noise contribution of the injection MOSFET is negligible and reduced on the order of A_v. Other noise contributors for BDI unit cell are same with the DI unit cell.

2.2.6 Resistor Gate Modulation Unit Cell

The resistor load gate modulation (RL) unit cell utilize photon current to change the gate voltage, which results in an output current in the MOSFET. The detector bias of RL unit cell is a function of detector current, load resistor and resistor bias voltage [7] as shown in equation 2.11:

$$V_{in} = \left(I_{ph} + I_{dark}\right)R_l + V_d \quad [V] \tag{2.11}$$

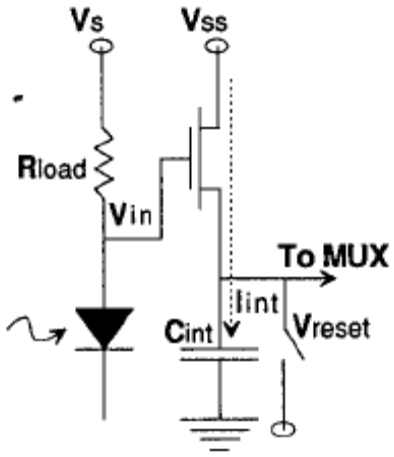

Figure 2.5: Schematic of RL unit cell [7]

The RL unit cell is suitable for high background flux applications, due to the fact that it can be adjusted in such a way that, in an environment of only background, detector and load biases can be adjusted for negligible drain current, hence integration of charge. By the help of detector and load bias adjustability, it can be used for different background high flux applications. As the signal is applied, the MOSFET drain current increases exponentially and rejects some level of background flux [7].

2.2.7 Current Mirror Gate Modulation Unit Cell

The difference of current mirror gate modulation (CM) unit cell from the RL unit cell is the MOSFET used in CM unit cell instead of the resistor used in RL unit cell as shown in Fig. 2.6.

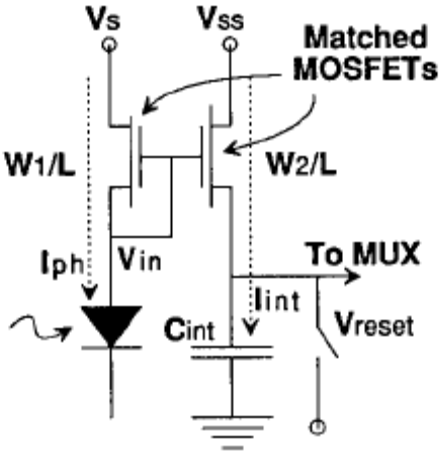

Figure 2.6: Schematic of CM unit cell [7]

The photon induced current flowing through the first transistor creates a common gate-to-source voltage change in the second transistor, hence same current flows through the second transistor, if V_s and V_{ss} bias voltages are same, known as the current mirroring. The integration current I_{int} is a linear function of the detector current I_{ph}, which is different from RL unit cell. In CM unit cell architecture, it also possible to scale up and down the integration current by changing the geometries of the MOSFET transistors as a property of current mirroring circuits as shown in equation 2.12:

$$I_{int} = I_{det} \frac{W_2/L_2}{W_1/L_1} \; [A] \tag{2.12}$$

The CM unit cell is used generally in very high background flux applications, where there is not enough space to accumulate detector current. In this case, by scaling down the width of the second transistor, determined fraction of the detector current is integrated. The current gain can also be changed by changing the bias voltages of the MOSFET transistors, which leads to nonlinear operation like in RL unit cell:

$$I_{int} = I_{det} \frac{W_2/L_2}{W_1/L_1} \exp(Vs - Vss)\ [A] \tag{2.13}$$

Non-uniformity from detector to detector can be large in CM unit cell structure due to threshold variation between current mirroring MOSFET pairs and injection efficiency variation because of detector resistance changes [7]. The advantage of CM unit cell over RL unit cell is the greater linearity and absence of load resistor.

2.2.8 Current Mirror Direct Injection Unit Cell

Current Mirror Direct Injection (CMDI) unit cell is proposed for detector bias stability and higher injection efficiency as an alternative to DI and BDI unit cells. Almost zero detector bias can be observed and almost 100% injection efficiency achieved with the CMDI architecture with the drawback of in-pixel capacitance.

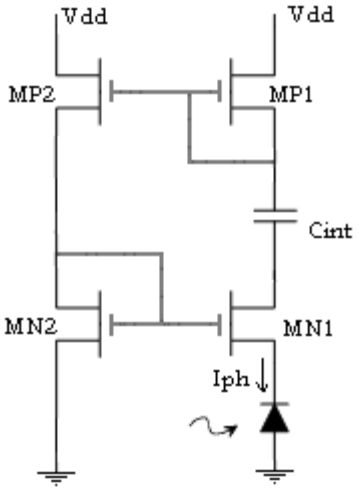

Figure 2.7: Schematic of CMDI unit cell

If same drain currents flow through two transistors that have the same sizes, it means their gate-to-source voltages V_{gs} is same. Two n-type MOSFETs M_{N1} and M_{N2} utilize this current mirroring mechanism, which means source voltage of MOSFET MN1 should be zero, because their gates are connected together (M_{N1} and M_{N2}). To have the same current flow through MOSFETs M_{N1} and M_{N2}, p-type MOSFETs M_{P1} and M_{P2} are connected as current mirror too. So, by using current mirroring both in detector side and power supply side, detector bias is equalized to zero, as well as same amount of current flow through both sides is same.

The photon induced current I_{ph} flows through M_{N1} and M_{P1}, same current flows through the M_{N2} and M_{P2} also. Since, the drain currents of both M_{N1} and M_{N2} are same, and their gates are connected together, detector bias is fixed to zero.

However, one of the important problems of high density FPAs, is the uniformity issue, the threshold voltage variations of the MOSFETs, which affects the detector bias. The detector bias with respect to threshold voltage changes of N-type and P-type MOSFETs is given in equation 2.14[9]:

$$V_{det} = \Delta V_{TN} - \Delta V_{TP} \tag{2.14}$$

This equation means that detector bias voltage is determined by the threshold voltage mismatches of N-type and P-type MOSFETs. It is also stated in [9] that, using CMDI unit cell as an alternative to DI unit cell, reduces the effect of threshold mismatches to detector bias on the order of three.

The injection efficiency of the CMDI unit cell is also improved with respect to DI unit cell. It is given in equation 2.15:

$$\eta_{CMDI} = \frac{R_D}{R_D + R_{IN}} = \frac{g_{mN1} R_D}{g_{mN1} R_D + (1 - \gamma_{gm})}$$

$$\text{where } \gamma_{gm} \text{ is defined as } \gamma_{gm} \equiv \frac{g_{mP2}}{g_{mP1}} \frac{g_{mN1}}{g_{mN2}} \tag{2.15}$$

As it is seen from the equation 2.15, with careful design that γ_{gm} is approximately 1, 100% injection efficiency can be achieved regardless of detector resistance R_D. The same result can be achieved by BDI unit cell with an amplifier of gain 100, but amplifier noise and difficulty of designing a small area amplifier make BDI unit cell unfeasible. Comparison of DI, BDI and CMDI unit cells with respect to injection efficiency, power consumption and detector bias variation is given in Table 2.1.

Although it advantageous in terms of detector bias stability and injection efficiency, CMDI unit cell has noise disadvantage due to current mirrors. It has also in pixel capacitance which occupies greater area than DI, SI like unit cells.

	DI	BDI	CMDI
ΔI_D (when ΔI_{ph} = 20nA	1.17nA	8.92nA	10.15nA
Injection efficiency ($\Delta I_D / \Delta I_{ph}$)	11.7%	89.2%	101.5%
Unit cell power consumption	~ $V_{DD} \cdot I_{ph}$	~ $V_{DD} \cdot I_{ph}$ + amplifier power	~ $2 V_{DD} \cdot I_{ph}$
Cell to cell detector bias variation	Within ~ 50mV over FPA	Within ~ 2.5mV over FPA	Within ~ 0.5mV over FPA

Table 2.1: Comparison of DI, BDI, and CMDI unit cells [9]

2.2.9 Current Mirroring Integration Unit Cell

The main difference of current mirroring integration (CMI) unit cell from CMDI unit cell is the integration capacitor in CMDI unit cell. CMI unit cell provides same or better performance than CMDI unit cell in terms of injection efficiency, almost rail-to-rail dynamic range and input impedance without using in-pixel amplifier or capacitor.

The working principle of the CMI unit cell is very similar to CMDI unit cell. The photon induced current flows through the N-type MOSFET MN1 and is mirrored to MN2 as using the high-swing cascade current mirror formed with P-type MOSFETs MP1-MP4 as shown in Fig. 2.8 [10]. Similar to the CMDI unit cell architecture, due to the fact that gates of MN1 and MN2 are connected together, source of MN1 is forced to zero detector bias, because they should have equal gate-to-source voltage with the same drain currents.

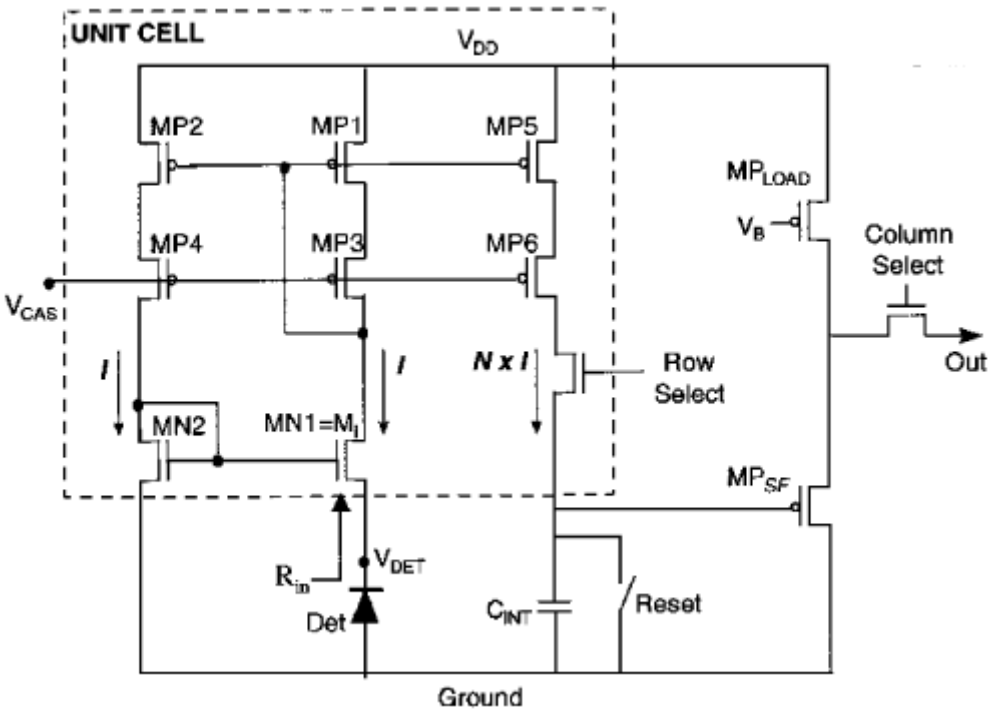

Figure 2.8: Schematic of CMI unit cell [10]

The input impedance of the CMI unit cell is same with the input impedance of CMDI unit cell and it is very low, which results in a high injection efficiency. The induced detector current is taken by the help of high injection efficiency, and transferred to an off-pixel integration capacitor with transistors MP5 and MP6. It is possible to transfer the detector current with a gain by changing the geometries of the mirroring transistors. The column select transistor transfers the capacitor voltage to the signal processing unit of the ROIC. After the read operation, integration capacitor C_{int} is reset and ready for the next frame operation.

The noise performance of the CMI unit cell is same with the CMDI unit cell except the effect of current mirroring. The total equivalent noise CMI unit cell at the input transistor is large due to current mirrors [10].

2.2.10 Comparison of ROIC Unit Cells

Unit cells are initial building blocks of ROIC architectures which are directly connected to the detectors generally by indium bumps, and transfers the photon induced current created by the detector to the signal processing unit of the ROIC with the help of multiplexers. There are different types of unit cells for various applications, depending on level of irradiance, injection efficiency, power consumption, area, dynamic range and noise performance.

A high performance unit cell should provide a stable and almost-zero detector bias to reduce the dark current and detector noise. It should also have a low input impedance for higher injection efficiency to efficiently transfer the photon induced current produced by the detector to the integration capacitor, to increase its bandwidth and to decrease the input referred noise level [10]. It should have a large dynamic range to store more charge on the integration capacitor. In addition to these needs, it should also have a lower power consumption and smaller area with the help of an off-pixel capacitor.

There are several unit cell architectures described here, that come with trade-offs. Thus, for different type of applications, different type of unit cell architectures can fit on the needs.

The SI, SFD and DI unit cells are simple and occupy small area, but do not satisfy some needs of higher performance needed systems. SI unit cell is the simplest one which has a

charge mode output. A source follower is added to the SI unit cell to provide voltage mode output. The main problem of SI and SFD unit cells is the changing detector bias causing non-linearity, and there is no gain provided by the SI and SFD unit cells.

The CTIA unit cell solves the detector bias stability and gain problem of SI and SFD unit cells with the addition of a high-gain inverting differential amplifier into the feedback loop. The photon induced charges are stored on the feedback capacitor of the differential amplifier. However, CTIA unit cell occupies significantly large area, because it is difficult to design a high-gain, low noise differential amplifier with a small area.

The DI unit cell is basic, have a good noise performance and also have a high gain, which can be determined by the integration capacitor. The main problem of DI unit cell is the injection efficiency. At low detector current levels, it exhibits very high input impedance resulting in unstable detector bias. Due to that injection efficiency problem, its use is limited to medium and high photon flux applications.

In the BDI unit cell, an inverting amplifier is added between the detector and MOSFET gate of DI unit cell, which results in lower input impedance. With the addition of the amplifier and lower input impedance, BDI unit cell can be used for lower photon flux applications. Both DI and BDI unit cells provide charge mode outputs.

For very high irradiance levels, it is not feasible to store the charge in the unit cell. For this reason, photon induced current should be scaled down before to be stored on the integration capacitor. CM unit cell is used for this purpose, as well as the RL unit cell. In RL unit cell, instead of MOSFET a resistive load is used. Both CM and RL unit cells suffer from the frequency response and detector bias stability problems.

The CMDI unit cell solves the problems of injection efficiency and detector bias stability of the CM and RL unit cells. However, it includes an in-pixel capacitor and has low dynamic range. To overcome these problems of CMDI unit cell, CMI unit cell is proposed. CMI unit cell have high dynamic range and off-pixel capacitor, in addition to stable detector bias and high injection efficiency. The problem of CMI unit cell is the worse noise performance due to current mirrors.

A summary of unit cell architectures and their properties is given in Table 2.2.

Preamplifier	**Input Impedance**	**Detector Bias Stability**	**Size**
SI	Self integrator	Not stable, changes during integration	Small
SFD		Not stable, changes during integration	Small, 3 transistors
DI	$1/g_m$	Not stable, changes during integration (10-50mV)	Small, only 1 transistor
BDI	$1/g_m x\ (1+A_v)$	Stable, controlled by op-amp feedback	Large, due to in pixel amplifier and integration capacitor
CTIA	Amplifier input impedance	Stable, controlled by op-amp feedback	Large, due to in pixel amplifier and integration capacitor
RL	Load resistor	Not stable, depends on photocurrent	Large due to in pixel resistor and capacitor
CM	$1/g_m$	Stable, controlled by current mirrors	Large due in pixel capacitor
CMDI	$1-\gamma / g_{mi}$	Stable (1-2.5mV)	Large due to in pixel integration capacitor and four transistors
CMI	$1-\gamma / g_{mi}$	Stable (1-2.5mV)	Small,9 transistors but off-pixel integration capacitor

Table 2.2: Comparison of unit cells

2.3Time Delay Integration (TDI)

There are different types of signal processing techniques for ROICs, such as sample and hold, correlated double sampling (CDS), and time delay integration (TDI).

The sample and hold technique provides simultaneous integration by employing a sample/hold capacitor outside the unit cell. Previous frame data is sampled by the sample switch and hold on the sample/hold capacitor, allowing simultaneous integration for the current frame [7].

Correlated double sampling (CDS) technique is used to eliminate the offset problems of op-amps for better dynamic range and to eliminate the low frequency flicker noise of op-amps [13]. The CDS operation stores the amplifier noise in one phase, and stores a new sample of amplifier noise in the subsequent phase. Then, it subtracts the one from another, which results in DC zero in frequency domain, virtually eliminating flicker noise, however parasitic capacitance effects prevent this idealization [14].

Another signal processing technique to improve the signal-to-noise ratio (SNR) of the ROIC is the time delay integration (TDI) method. Time delay integration means getting the same signal from different pixels with a time delay. Due to the fact that actual signal is correlated while the noise is uncorrelated, signal is increased by factor of n while noise is increased by factor of square root n, if n detectors are used in the design [15].

The TDI method is quantitatively explained as follows: The first pixel is exposed to radiation, after Δt amount of time delay the following pixel is exposed to the same radiation, and it goes on like that n times, where n is the number of pixels that TDI is implemented on. Therefore, the output voltage is the sum of all detector pixel contributions as given in equation 2.16:

$$V_{total} = \sum_{i=1}^{n} V_i(t1 + (i-1)\Delta t) \tag{2.16}$$

where Vi is the voltage of ith pixel output.

On the other hand, noise is added by power like in equation 2.17:

$$v_{noise,total}^2 = \sum_{i=1}^{n} v_{noise,i}^2(t1 + (i-1)\Delta t) \tag{2.17}$$

Therefore, SNR improvement becomes:

$$S/N = \frac{V_{total}}{V_{noise,total}} = \sqrt{N}(\frac{S}{N}) \tag{2.18}$$

For example, if 4 detector pixels are used for TDI, total voltage at the output becomes 4V, where V is one of the outputs. On the other hand, square of total noise voltage becomes 4 times the square of one pixel output voltage. Therefore, noise voltage will be $2V_{noise}$, which means a $\sqrt{4} = 2$ improvement in SNR.

TDI implements the time delay addition by employing number of storage elements, and a summing device. When the image is on the first pixel of the detector array, it is stored on a storage element, namely a capacitor, to be used in the summation when the same image data is ready on all pixels. Therefore, in a TDI on 4 elements implementation without oversampling, the same image on the first detector will be on the fourth detector 4 frames later. Due to the fact that, TDI adds all the contributions of 4 detectors for the same image, first detector should store the value for the first image for 4 frames. In order to have a output at each clock cycle, with 4 pixel detector array without oversampling, first detector should have 4 storage elements, second detector 3 storage elements, third detector 2 storage elements, and the last detector 1 storage element. The block diagram of TDI algorithm over 4 pixel array without oversampling is shown in Fig. 2.9.

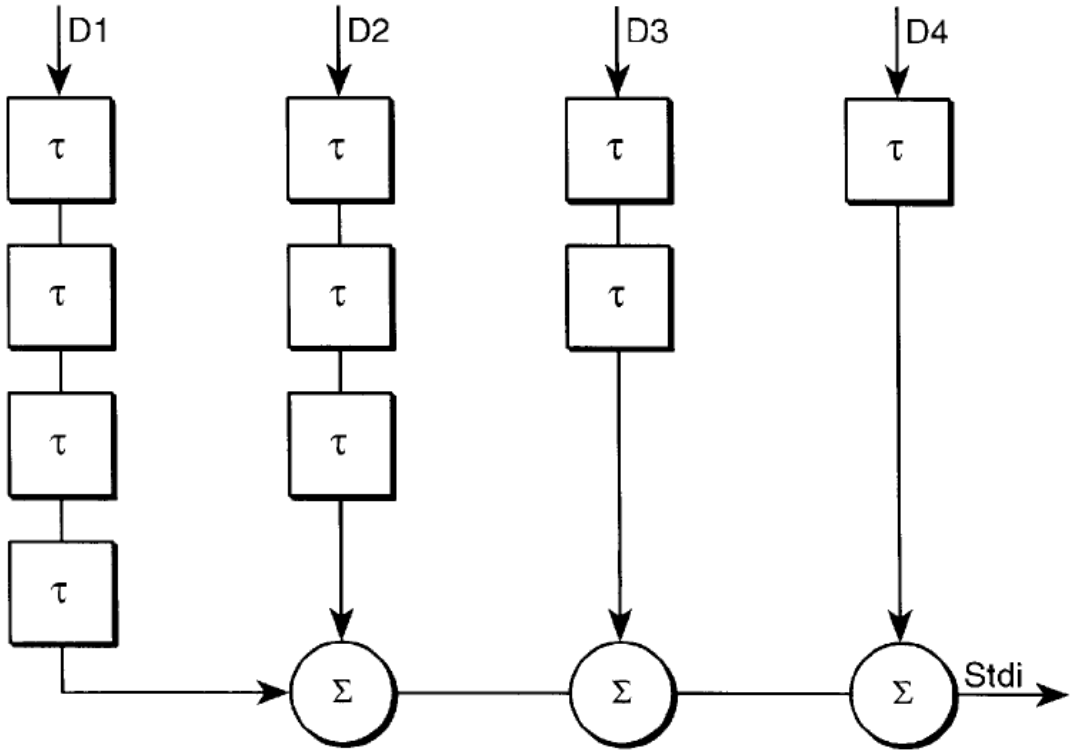

Figure 2.9: Block diagram of TDI algorithm [16]

For the TDI algorithm to be implemented an optical scanner is needed, because the same image has to be on all pixels subsequently for the TDI operation. The position of the same image in subsequent frames is shown in Fig. 2.10. For the TDI on 4 elements (pixels) without oversampling, the same image has to be on fourth pixel, after 4 frames it is on the first pixel.

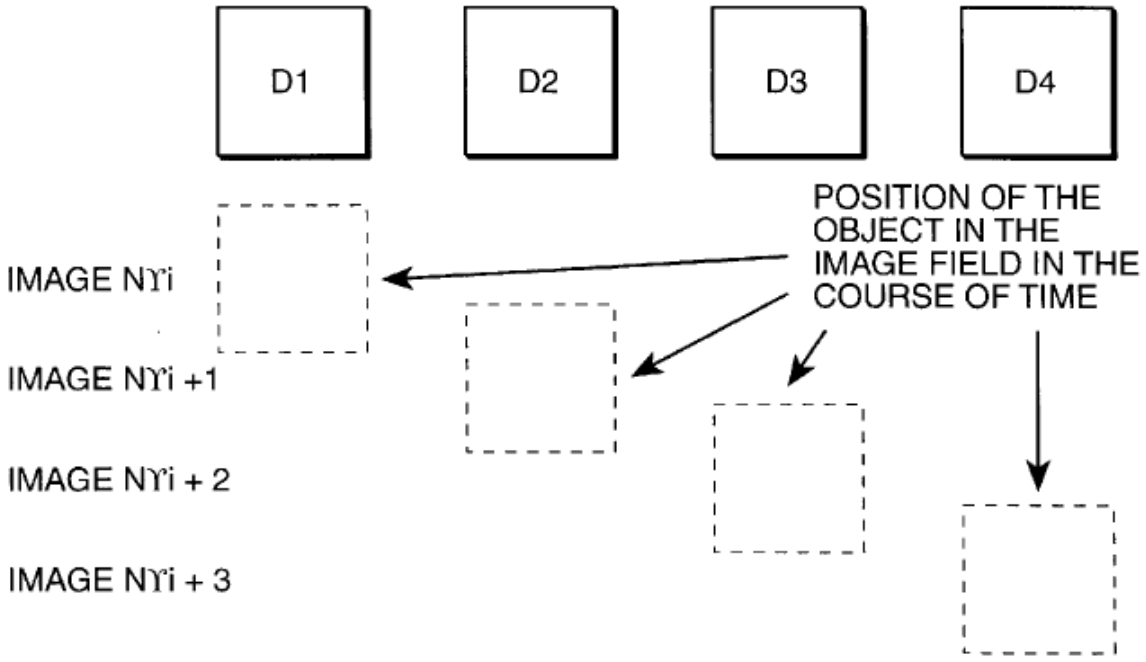

Figure 2.10: Position of image in TDI without supersampling [16]

As it is shown in Fig. 2.10, for the first image data the stored data at frame 1 of first detector, the stored data at frame 2 of second detector, the stored data at frame 3 of third detector, and the stored data at frame 4 of fourth detector should be summed up. The formula showing this is given in equation 2.19.

I1 = D1 (image frame i) + D2 (image frame i+1) + D3 (image frame i+2) + D4 (image frame i+3) [16] (2.19)

To increase the spatial resolution of the image, supersampling can be used. As its name implies, supersampling means to take more than one data sample from a pixel. For instance, if the optical scanner goes from one detector pixel to another in three steps, it called supersampling rate of three. The formula of first image with TDI over four elements with an optical supersampling rate of three is given in equation 2.20.

I1= D1 (image frame i) + D2 (image frame i+3) + D3 (image frame i+6) + D4 (image frame i+9) [16] (2.20)

The position of the same image on different detector pixels with an optical supersampling rate of three is shown in Fig. 2.11.

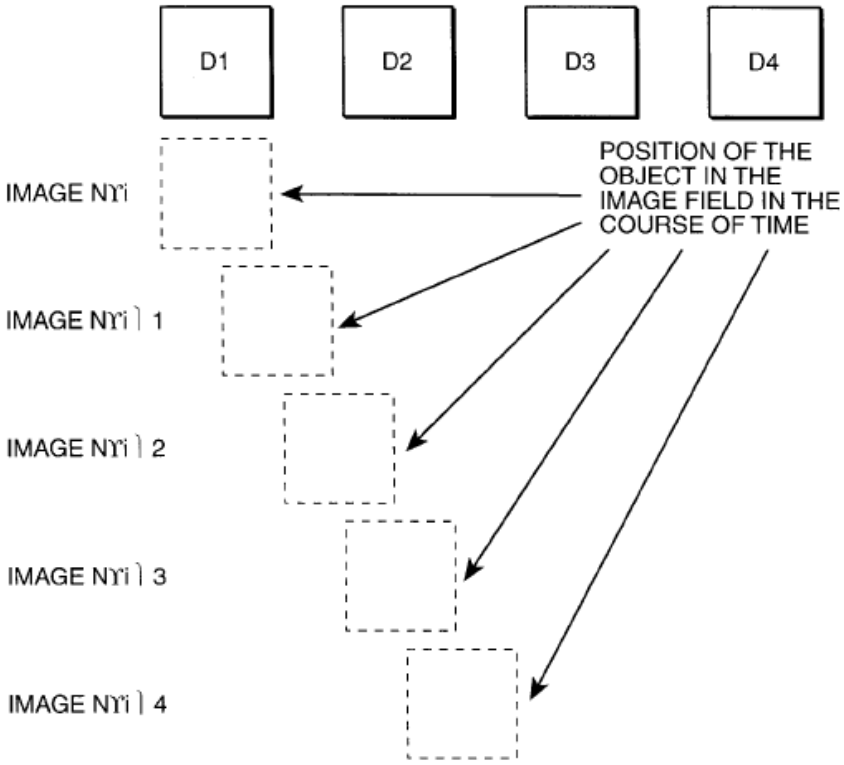

Figure 2.11: Position of image with supersampling rate of three in TDI [16]

There are two possible methods to implement TDI algorithm. The first method is to store the data coming from different detectors of the same image in a single storage element. The second method is to use multiple storage elements and single adder for the same image, whose data come from different detectors. Both of them have advantages and disadvantages for different applications. The first approach uses multiple adder, hence consumes more power than the second approach. On the other hand, second approach uses much more storage element than the first approach, hence occupies more area. The designer should choose one of them, which fits best to the desired application.

The block diagram of the first TDI approach is shown in Fig. 2.12. Since TDI over four element with optical supersampling rate of three is implemented, 12 storage elements are needed, 10 to be used for storage of delays, 1 to be used for storage to make capable integration operation during read operation, and 1 to be used for storage while reset operation.

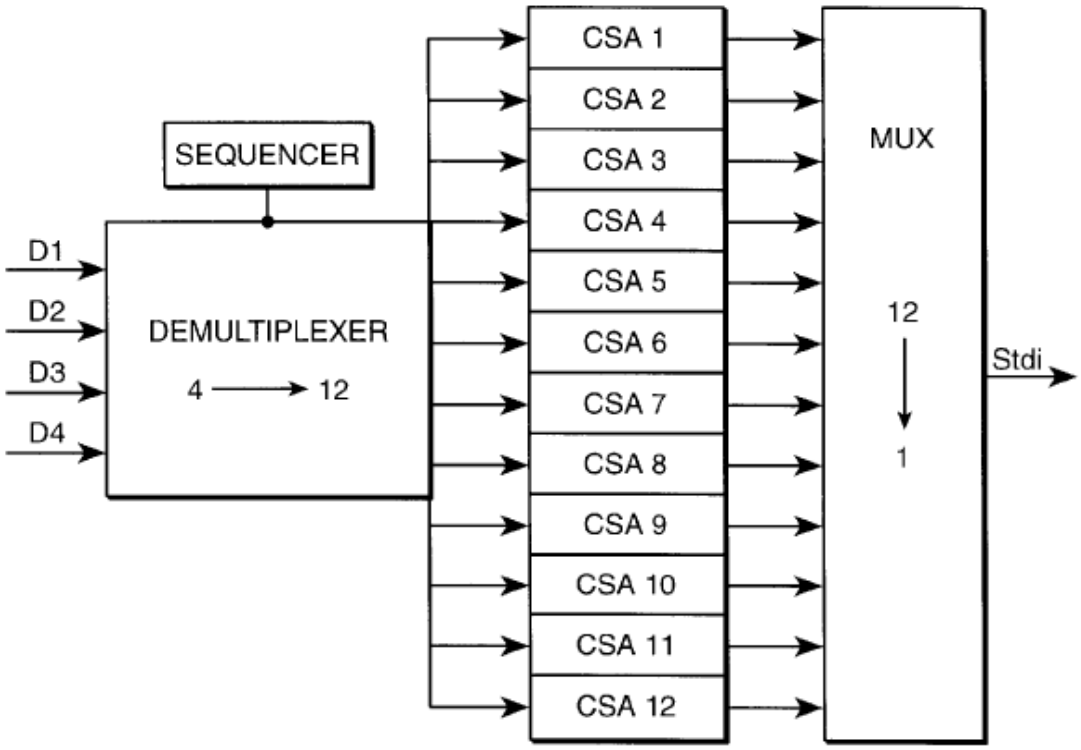

Figure 2.12: Implementation of TDI method 1 [16]

At frame i first detector's contribution is integrated to CSA 1, at frame i+3 second detector's contribution is integrated to CSA 1, at frame i+6 third detector's, and at frame i+9 fourth detector's. At frame i+10, first image is read, and finally at frame i+11 it is reset. Table 2.3 shows the write, read and reset operations for the first TDI approach.

Due to the power limitations of first approach, the second TDI approach is also used in ROIC designs. In the second TDI approach, first detector has 11 storage elements, second has 8, third has 5, and finally fourth detector has 2 storage elements, 26 storage elements in

total, to store the delayed frames to be used in appropriate frame. Since, the first image comes to the fourth detector after ten frames; first detector should store the data of first image for 10 frames. The block diagram of second TDI approach is shown in Fig. 2.13.

Frame N°	CSA 1	CSA 2	CSA 3	CSA 4	CSA 5	CSA 6	CSA 7	CSA 8	CSA 9	CSA 10	CSA 11	CSA 12
i	D1											
i + 1		D1										
i + 2			D1									
i + 3	D2			D1								
i + 4		D2			D1							
i + 5			D2			D1						
i + 6	D3			D2			D1					
i + 7		D3			D2			D1				
i + 8			D3			D2			D1			
i + 9	D4			D3			D2			D1		
i + 10	READ	D4			D3			D2			D1	
i + 11	RESET	READ	D4			D3			D2			D1
i + 12	D1	RESET	READ	D4			D3			D2		
i + 13		D1	RESET	READ	D4			D3			D2	
i + 14			D1	RESET	READ	D4			D3			D2
i + 15	D2			D1	RESET	READ	D4			D3		
i + 16		D2			D1	RESET	READ	D4			D3	
i + 17			D2			D1	RESET	READ	D4			D3
i + 18	D3			D2			D1	RESET	READ	D4		
i + 19		D3			D2			D1	RESET	READ	D4	
i + 20			D3			D2			D1	RESET	READ	D4
i + 21	D4			D3			D2			D1	RESET	READ
i + 22	READ	D4			D3			D2			D1	RESET
i + 23	RESET	READ	D4			D3			D2			D1

Table 2.3: Write / Read operation sequence of TDI method 1 [16]

The data of the first image is stored in first detector's first storage element, but other detector's contributions are not ready. Therefore, for the same image to go to the fourth detector, first detector's first storage element should keep the data to be summed up with fourth detector's contribution. After ten frames, first detector's 1st storage, second detector's 4th storage, third detector's 7th (2nd, because it has 5 storage elements) storage, and fourth detector's 11th (1st, because it has 2 storage elements) storage should be added at TDI amplifier to be sent to the output as the first image data. Table 2.4 shows the writing operation sequence to the storage elements, while Table 2.5 shows the reading operation sequence of storage elements.

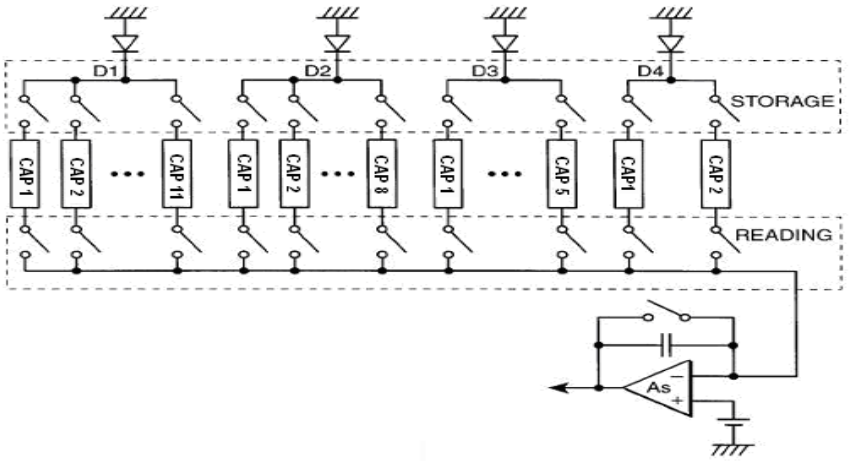

Figure 2.13: Implementation of TDI method 2 [16]

	DETECTOR Nº 1											DETECTOR Nº 2								DETECTOR Nº 3					DETECTOR Nº 4	
FRAME	1	2	3	4	5	6	7	8	9	10	11	1	2	3	4	5	6	7	8	1	2	3	4	5	1	2
1	x											x								x					x	
2		x											x								x					x
3			x											x								x			x	
4				x											x								x			x
5					x											x								x	x	
6						x											x			x						x
7							x											x			x				x	
8								x														x				x
9									x			x											x		x	
10										x			x											x		x
11											x			x						x					x	
12	x														x						x					x
13		x														x						x			x	
14			x														x						x			x
15				x														x						x	x	
16					x														x	x						x
17						x						x									x				x	
18							x						x									x				x
19								x						x									x		x	
20									x						x									x		x
21										x						x				x					x	
22											x						x				x					x
23	x																	x				x			x	
24		x																	x				x			x
25			x									x												x	x	

Table 2.4: Write operation sequence of TDI method 2 [16]

The second TDI method, which is also implemented on this ROIC design, is more advantageous in terms of linearity and power consumption than the first method. Due to the fact that TDI over four elements with optical supersampling of three, the second method is chosen. However, if TDI over seven elements with optical supersampling rate of three is desired, it is impossible to implement the second method, because it requires 77 storage elements. Therefore, for the future work of 576x7 ROIC design, which requires TDI over 7 elements with optical supersampling rate of three, the first method is thought to be used.

	DETECTOR N° 1											DETECTOR N° 2								DETECTOR N° 3					DETECTOR N° 4	
FRAME	1	2	3	4	5	6	7	8	9	10	11	1	2	3	4	5	6	7	8	1	2	3	4	5	1	2
1																										
2																										
3																										
4																										
5																										
7																										
8																										
9																										
10																										
11	x											x								x					x	
12		x											x								x					x
13			x											x								x			x	
14				x											x								x			x
15					x											x								x	x	
16						x											x			x						x
17							x											x			x				x	
18								x														x				x
19									x			x											x		x	
20										x			x											x		x
21											x			x						x					x	
22	x														x						x					x
23		x														x						x			x	
24			x														x						x			x
25				x														x						x	x	

Table 2.5: Read operation sequence of TDI method 2 [16]

3 72x4 P-on-N ROIC IMPLEMENTATION

3.1 ROIC Definition and Requirements

In this thesis, a 72x4 P-on-N type readout integrated circuit (ROIC) is designed in Austria Microsystems (AMS) 0.35 µm, 4 metal, 2 poly CMOS process as a part of 288x4 P-on-N ROIC. It is designed for 228x4 FPA array, and P-on-N type Mercury Cadmium Telluride (HgCdTe-MCT) detectors which are sensitive to long wave infrared radiation (LWIR) between 7.7 and 10.3 µm. In the complete detector system, there are 288 lines, each of them consisting of 4 detectors. These 288 lines consist of 4 blocks of 72 lines. In this work, one of these blocks is designed. Total detector width is 383 µm while length is 8064 µm. Each detector pixel's size is 25 µm. The separation between the center of the last pixel of first set and first pixel of second set is 100 µm. The geometry of the detector is shown in Fig. 3.1.

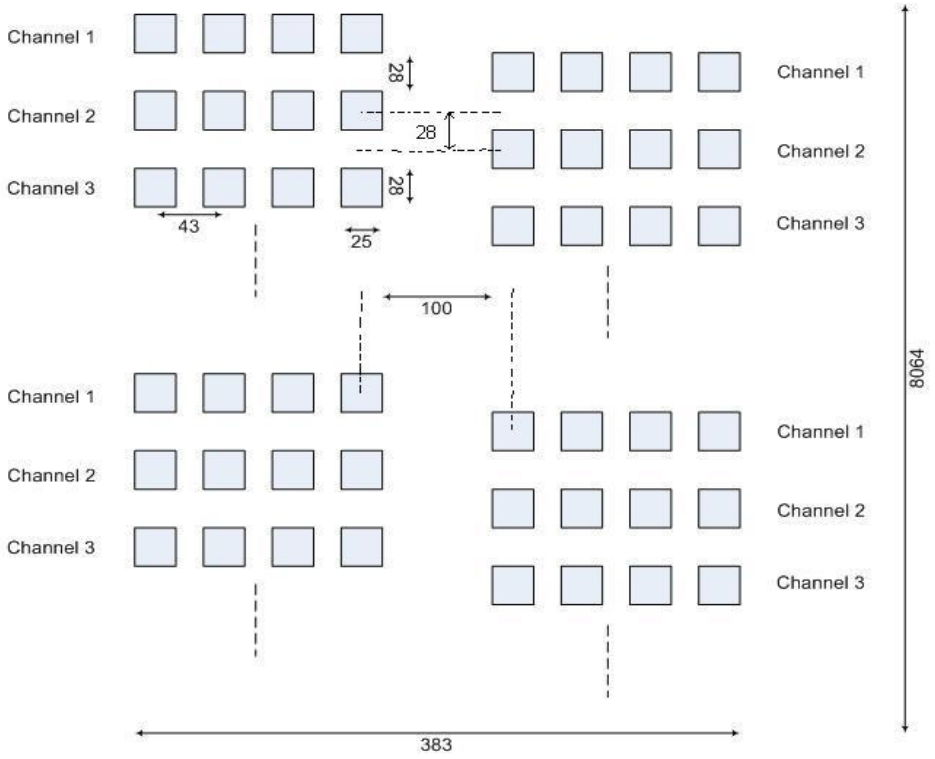

Figure 3.1: Geometry of the detector array

The 72x4 block is one of the four blocks shown in Fig. 3.1, which means one output from the ROIC, at the frequency up to 5 MHz. The ROIC implements bidirectional TDI scanning over 4 elements for signal processing with an oversampling rate of 3. Additional ROIC requirements and features are listed below.

Input Requirements

Minimum detector input impedance is 1MΩ. Input current range is 1.2 – 55nA. Nominal current value is 12.3 nA at 293 K background.

ROIC Features

- Integration period adjustment
- Multigain adjustment
- Bidirectionality of TDI scanning
- Pixel select/deselect option with automatic gain adjustment
- Bypass property
- Parallel/Serial programmability

Output Requirements

Dynamic range of ROIC output is 2.8 V and the output voltage at zero irradiance should be 1.7 V, so that maximum output voltage is 4.5 V. The output should be ready within first 100 ns of the frame to be sampled by an off-chip ADC. ROIC output should drive a 10 pF capacitance with a 1 MΩ shunt resistance.

Noise Requirements

Maximum allowed input referred noise level is 2100 electrons.

Power Consumption Requirements

Maximum allowed power consumption of ROIC is 50 mW.

3.2 ROIC Architecture

The 72x4 P-on-N ROIC consists of 72 channels, which are connected to a 72x4 multiplexer. In each cycle, one of the channel outputs is sent to the output to be received by an off-chip ADC. General architecture of the 72x4 ROIC is shown in Fig. 3.2.

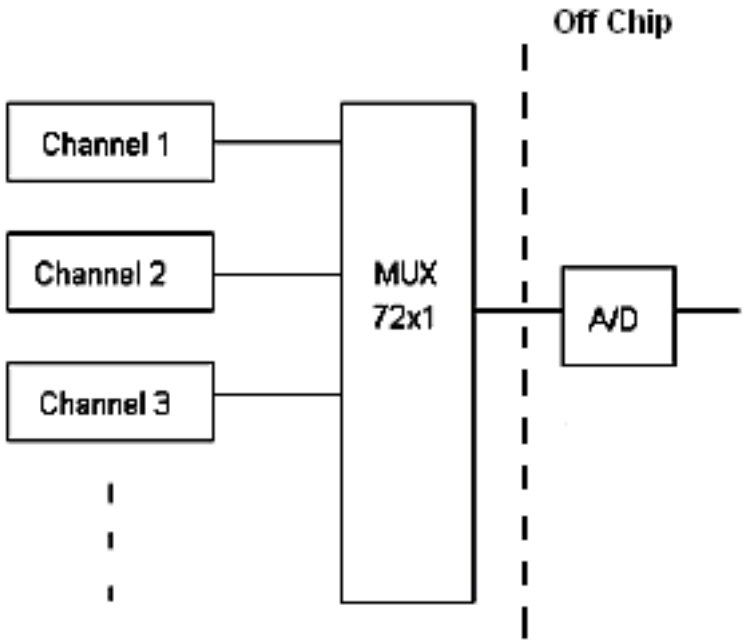

Figure 3.2: ROIC architecture

The detailed architecture of the 72x4 ROIC is given Fig. 3.3. The interface circuit, digital control block, channel select decoder and address decoder constitute the digital part of the ROIC. Digital part controls the analog part, which consists of 72 channels, TDI stage, offset cancellation, automatic gain adjustment stage and output buffer stage.

Each of the 72 channels have its own 26 capacitor sets, pixel select/deselect latches, bidirectionality switches and latches, and 4 unit cells for 4 detector pixels. The channel architecture is shown in Fig. 3.4.

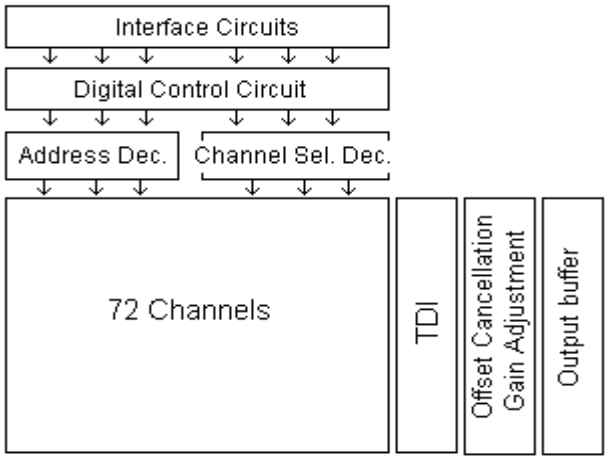

Figure 3.3: ROIC detailed architecture

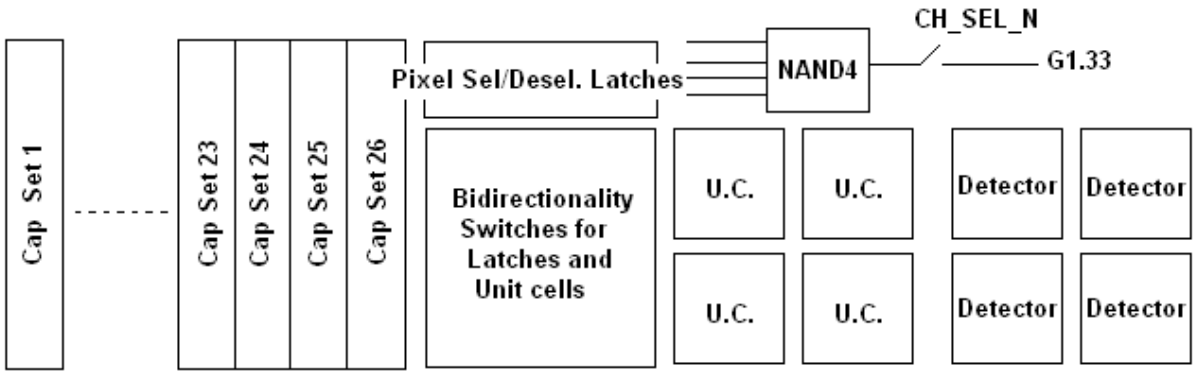

Figure 3.4: Architecture of a channel

3.3 ROIC Implementation

The ROIC building blocks are unit cell, input integration capacitor stage, TDI stage, offset cancellation and automatic gain adjustment stage, and the output buffer stage. The CMI unit cell as the unit cell architecture is implemented for P-on-N type ROIC. At TDI stage, the second approach mentioned in section 2.3, single summing amplifier with multiple

storage elements, is implemented. Amplifiers designed and implemented for TDI, offset cancellation, and output buffer is also explained in this chapter.

3.3.1 Input Stages

Unit cell and integration capacitor stage constitute the input stages of ROIC. CMI unit cell is used as the unit cell architecture of the ROIC.

3.3.1.1 Unit Cell Design

Several input cell architectures are discussed in section 2.1. As it is mentioned previously, there are trade-offs that the designer has to deal / select based on the application. The important parameters of unit cells are input impedance for high injection efficiency, detector bias stability for reduced dark current and improved noise performance, dynamic range for enhanced charge storage, linearity for better images, background flux irradiance, circuit area and power consumption. The designer should choose the most appropriate unit cell architecture in term of the needs of the application.

The input impedance specification of the 72x4 P-on-N ROIC requires a low input impedance unit cell for higher injection efficiency for 1 MΩ detector impedance, which is a low detector impedance. Another important specification of the P-on-N ROIC is the linearity. The area of the ROIC should be small, and the power consumption should be less than 50 mW. Due to the capacitor sets used for TDI over 4 elements with an oversampling rate of 3, less area should be allocated to the unit cells. Also, the chosen unit cell should not consume much power, because there are power consuming amplifiers and buffers at the other stages of the ROIC. Among the smallest in area and less power consuming unit cells, due to the excellent detector bias stability and low input impedance, CMI unit cell is chosen, in spite of its moderate noise performance.

Several simulation runs are performed for the comparison of CMI and DI unit cells in terms of detector bias stability and input impedance performance. The comparison of CMI and DI unit cells in terms of detector bias stability is given in Table 3.1.

Current	DI - Detector Bias	CMI – Detector Bias
1nA	112.8mV	477µV
10nA	79.5mV	562µV
30nA	47.8mV	752µV
50nA	32.4mV	867µV
70nA	22mV	940µV
100nA	10.75mV	1004µV

Table 3.1: Comparison of detector bias voltages of DI and CMI unit cells

Table 3.1 shows that the detector bias stability of CMI unit cell is much better than DI unit cell, which helps to reduce the dark current effect.

It is also observed in the simulations that input impedance of DI unit cell changes from 250 kΩ to 2.5 MΩ in the current range of 100 nA to 3 nA, while input impedance of CMI unit cell changes from 64.3 kΩ to 1.7 kΩ in the same current range. This means that input impedance performance of CMI unit cell is much better as predicted in section 2.1.

However, CMI unit cell comes with a trade-off beside these advantages, which is the moderate noise performance due to the current mirror structure. Noise simulation results show that CMI unit cell's noise is 414 electrons, while DI unit cell's noise is 69 electrons, which is considerably lower than CMI unit cell's noise.

The P-on-N CMI unit cell is structure shown in Fig. 3.5, which is different than the structure depicted in section 2.1. Since detector polarity of P-on-N detectors is different than the polarity of the N-on-P detectors, corresponding changes in the conventional N-on-P structure has to be carried out. In P-on-N detector type, N-type doped bulk is exposed to the infrared radiation, and P-type doped part of the detector is connected to the ROIC with the help of indium bump.

One important change in the unit cell structure is the output of the unit cell. As it is seen in Fig. 3.5, output of the P-on-N CMI unit cell is in voltage mode, and the integration capacitor of the conventional CMI structure is out of the pixel. The voltage mode output of the unit cell is transferred to the capacitor sets via a long path due to the inherent geometry of the detector. The transferred voltage is converted to the current at the capacitor sets and stored onto the capacitors properly. The reason of carrying voltage instead of current is the parasitic capacitances due to long and close paths. Although line to ground parasitic can be reduced by careful layout such as using higher level metals, it is very difficult to eliminate the line to line parasitic capacitance. Due to the detector geometry, a channel and its routings should fit into 56 µm in height, which means tens of routing paths will be very close to each other, resulting in line to line parasitic.

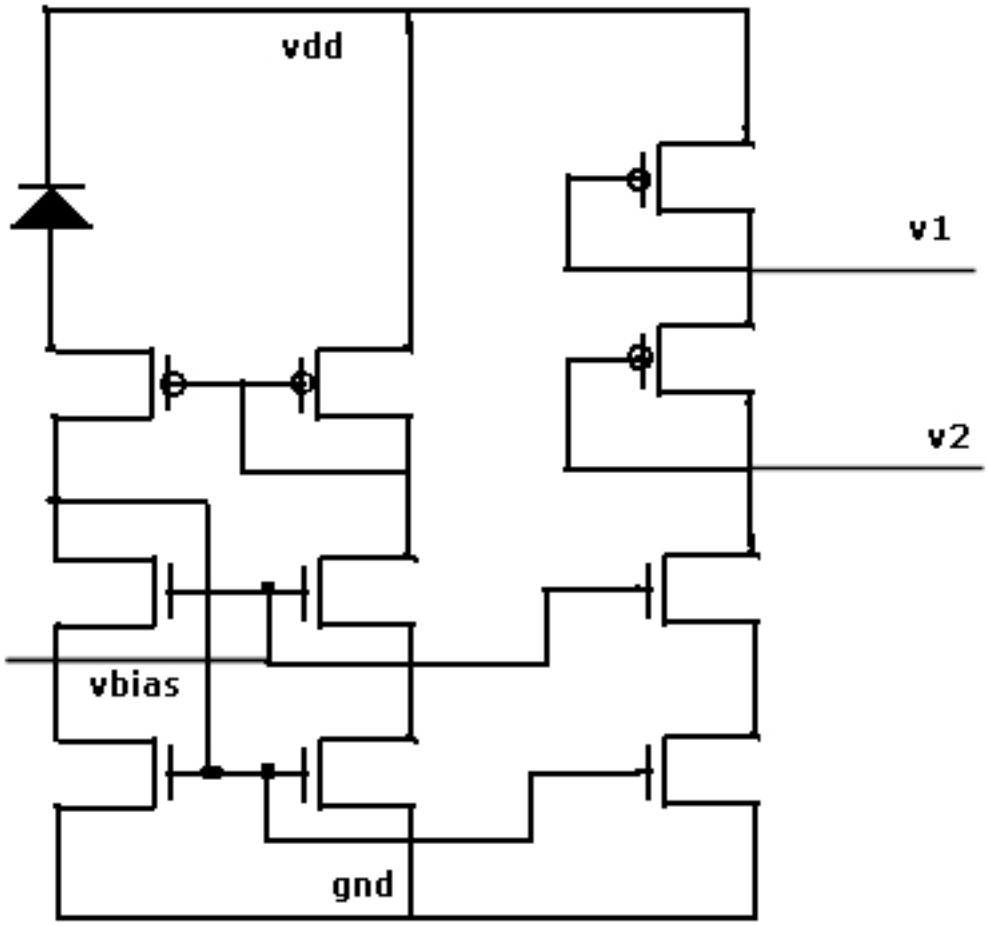

Figure 3.5: Schematic of P-on-N CMI unit cell

3.3.1.2 Input Capacitors

Input capacitor sets are important building blocks of the ROIC, because capacitor sets occupy most area of the ROIC. Since, the design is an area limited, different types of capacitors are simulated for best performance in small area. MOS capacitors are commonly used in similar applications, but its linearity is not good as the linearity of poly capacitors. The maximum integral non-linearity is defined as 1.7 mV for ROIC. It is impossible to achieve that result within the dynamic range of ROIC, with 0.35 µm AMS CMOS process.

Another option to reduce the size of the capacitor set size is to use MIM capacitor in parallel with poly capacitor, hence to increase the charge storage capacity in the same area. However, 0.35 µm AMS CMOS process does not support the use of MIM capacitors. Thus, to be safe on the linearity specification, poly capacitor is decided to be used.

The capacitor values and gain ratios are given in Table 3.2.

Gain state	Equivalent Capacitance (pF)	Storage Capacitance (pC)	Gain Ratio
0	0.35	0.98	1.30
1	0.46	1.29	1.00
2	0.70	1.96	0.66
3	0.92	2.58	0.50

Table 3.2: ROIC gain settings and corresponding capacitor values

As it is seen from Table 3.2, for different gain setting there should be different equivalent capacitance value. For this purpose, MOS switches are used between capacitors whose values are 0.35 pF, 0.11 pF, 0.24 pF and 0.22 pF. The circuit implementation of the capacitor set is shown in Fig. 3.6. For gain setting of 1.30, only the 350 fF capacitor is used, while for gain setting of 0.50 all the capacitors are connected in parallel to obtain 920 fF capacitance.

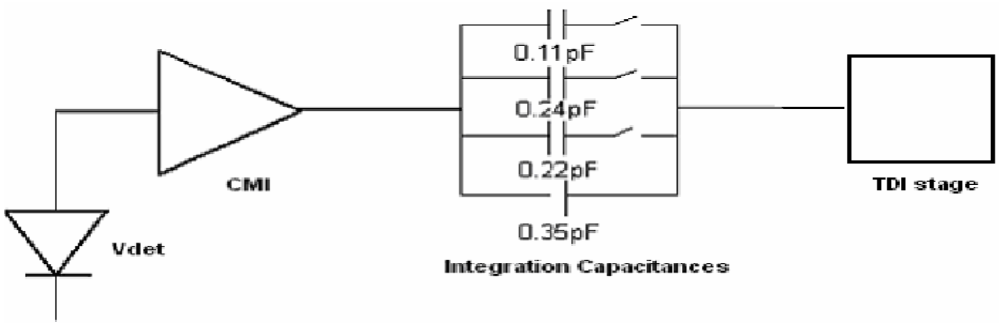

Figure 3.6: Architecture of input capacitor stage

3.3.2 Implementation of TDI stage

Time delay integration (TDI) over 4 elements with an oversampling rate of 3 is implemented with a single amplifier and 26 poly capacitors used as analog memories as explained in section 2.2. In this implementation, 11 capacitors for the first detector, 8 capacitors for the second detector, 5 capacitors for the third detector, and 2 capacitors for the fourth detector are needed for the oversampling rate of 3. To implement the bidirectional TDI scanning, switching capacitors concept is utilized. For the first TDI scan direction, detector 1 is connected to the capacitor set that has 11 capacitors; detector 2 is connected to the capacitor set of 8, detector 3 to capacitor set of 5, and detector 4 to capacitor set of 2. For the opposite TDI scan direction, capacitor sets should mirror their detector connection, which means detector 1 is connected to capacitor set of 2, detector 2 to capacitor set of 5, detector 3 to capacitor set of 8, and finally detector 4 to capacitor set of 11.

The implementation of the TDI algorithm is realized through the consecutive charge storage of detectors to the corresponding capacitor set. At each frame, one of the four detectors is connected to its corresponding capacitor set according to TDI direction, as mentioned earlier. For example, at frame 1, detector 1 stores its charge to the first capacitor of capacitor block that consists of 11 capacitors, detector 2 to the first capacitor of capacitor block that consists of 8 capacitors, detector 3 to the first capacitor of capacitor block that consists of 5 capacitors, and finally detector 4 to the first capacitor of capacitor block that consists of 2 capacitors. At frame 2, detector 1 stores its charge to second capacitor of 11, detector 2 to second capacitor of 8, detector 3 to second of 5, and detector 4 to second of 2. At next frame, detector 1, 2 and 3 store their charge to third of 11, 8 and 5 respectively, while detector 4 stores its charge to the first of 2, which means it turns to the beginning, and it goes on like that. At the required frame, contributions of four detectors are summed up at the TDI amplifier and sent to the output buffer to be sampled by the off-chip ADC.

There are four different switches controlling the charge transfer from detectors to TDI amplifier: INT, RESET, S1 and S2. RESET and INT switches are used to transfer the charge from detector to integration capacitor. RESET initializes the integration capacitor

voltage and INT switch connects the detector node to the integration capacitor. After the charge is transferred to integration capacitor, stored charge is transferred to the TDI capacitor with the help of TDI amplifier. S1 and S2 switches control the charge transfer of TDI amplifier. S1 switch is closed when photocurrent from the detector is transferred to the integration capacitor, connecting the bottom plate of the capacitor to the ground. S1 is open while the stored charge on the integration capacitor is transferred to TDI capacitor, forcing charges to go onto the TDI capacitor. S2 switch is open during the charge transfer to integration capacitor, whereas it is closed during the charge transfer to TDI capacitor, connecting the integration capacitor and negative input of the TDI amplifier as shown in Fig. 3.7.

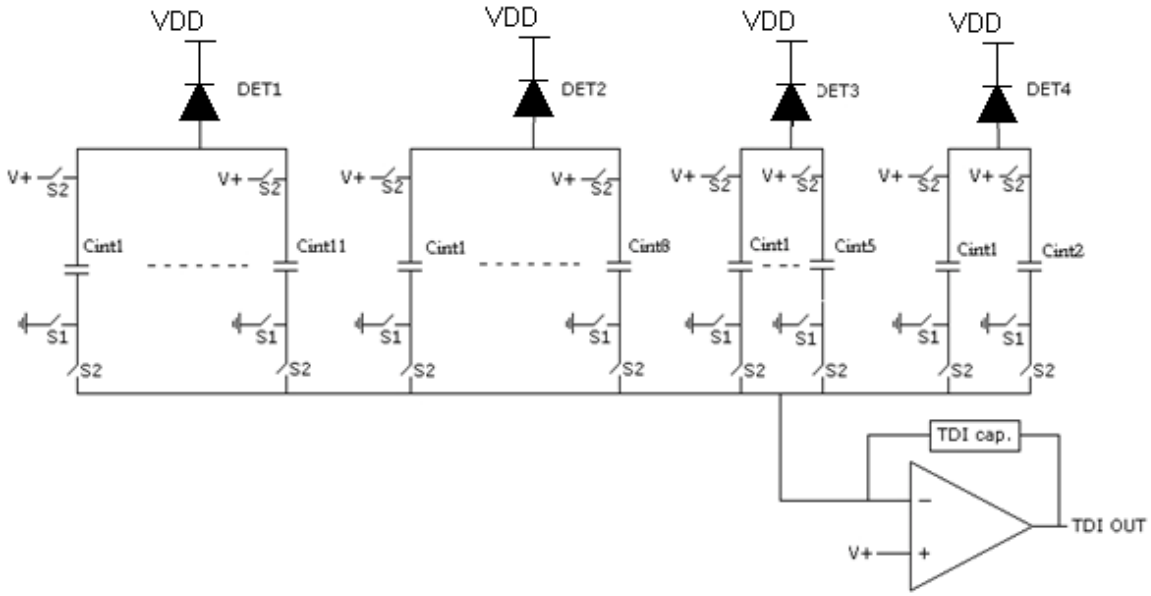

Figure 3.7: TDI implementation

There is one problem related to the charge transfer from integration capacitor to TDI stage. That is the poly capacitors having high parasitic from the poly 1 layer to the substrate. The desired capacitance between the poly 1 and poly 2 layers is 0.86 fF/μm^2, while the capacitance between the ploy 1 and substrate is 0.119 fF/ μm^2, which is comparable to the value of desired capacitance. During the charge transfer process, the stored charge on the integration capacitor is forced to move onto the TDI capacitance, by applying V+ (1.2 V) to

the capacitor. Therefore, the parasitic capacitance related to the bottom plate of the integration capacitor is also charged to 1.2 V, which results in undesired voltage at the output, because the stored charge to the parasitic capacitance is also transferred to the TDI capacitor as it is shown in Fig. 3.8.

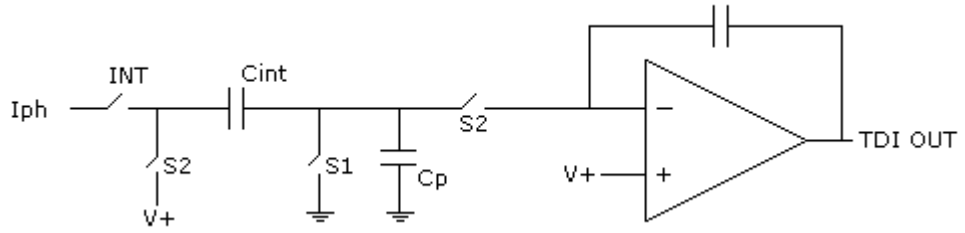

Figure 3.8: Schematic of TDI with parasitic capacitance

As a result of the undesired charge transfer due to the parasitic capacitance Cp, TDI output voltage can be expressed as the following:

$$V_{TDI} = V_{+} + \frac{V_{+}C_{p}}{C_{TDI}} + \frac{C_{int}V_{int}}{C_{TDI}} \tag{3.1}$$

Since the term related with the parasitic capacitance is undesired, it should be eliminated for the output to be correct. To eliminate the effect of the parasitic capacitance, a summation circuit is designed, which is described in the following section.

TDI amplifier is the key element in TDI stage, because it realizes the charge transfer from the integration capacitor to the TDI capacitor, supplying input to the offset cancellation and automatic gain adjustment stage. The TDI amplifier should have enough gain in order to keep the voltage at the inverting input of the amplifier at V+ (1.2V). Due to the fact that the amplifier should supply the stable output voltage in less than 100 ns, it should also be fast enough with an acceptable phase margin, to prevent ringing at the output. Possible maximum output swing and possible minimum power consumption is also desired to satisfy the specifications of the ROIC. Two stage differential amplifier followed by a common source stage with resistor compensation is chosen as the circuit topology of TDI amplifier. The gain of the amplifier is 66 dB, while power consumption is 1.82 mW. The

amplifier has a slew rate greater than 100 V/µs. Phase margin of the amplifier is 61 degrees. The resulting amplifier is shown in Fig. 3.9.

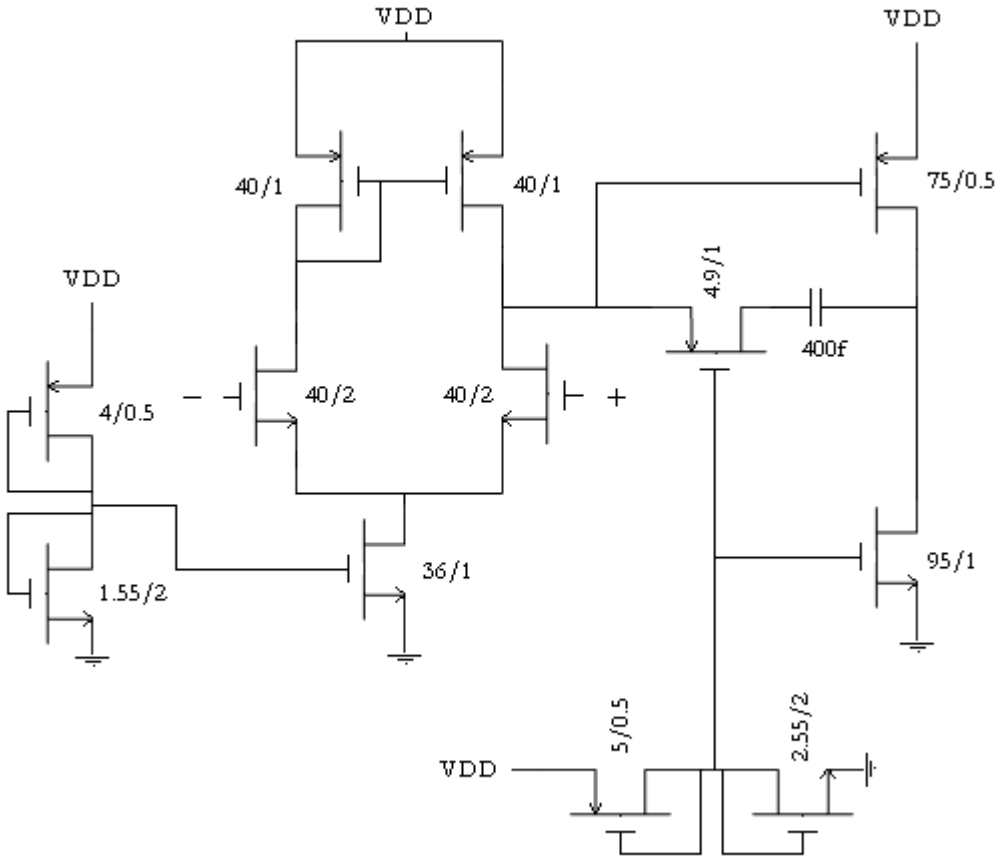

Figure 3.9: Schematic of TDI amplifier

3.3.3 Offset cancellation and Automatic gain adjustment stage

The offset cancellation stage is designed to subtract the erroneous voltage from the output, related to parasitic capacitance as explained in the previous section, and switching capacitor problems. There are two important problems related to the switching capacitor circuits, which are channel charge injection and clock feedthrough.

The charge injection problem is related to the distribution of the charges that exist when the transistor is on. When the MOSFET transistor is on, there should be a channel between the source and drain of the MOSFET, which consists of charges. When the MOSFET transistor becomes off, these charges between the source and drain of the MOSFET should go somewhere. Some of them go to the drain terminal, whereas some of them go to source terminal. Therefore, the charges those go to the output part of the MOSFET switch are stored onto the capacitance at that node, meaning an erroneous voltage on that capacitor [12].

In addition to the channel charge injection problem, clock feedthrough problem also causes erroneous charge storage on the sampling capacitor at one port of the MOSFET switch. The clock that drives the gates of the MOSFET switches couples to the sampling capacitor through the gate-to-drain or gate-to-source overlap capacitances. This is an inevitable problem of switched capacitor circuits, also exists in this design. The INT and RESET signals controlling the charge transfer to the integration capacitors, drive the gates of MOSFET switches, results in clock feedthrough problem.

There are several methods to reduce charge injection problem, which are using complementary switches, differential sampling and using dummy switch. Dummy switch approach is implemented in this design to reduce the effect of charge injection. In this approach, charge injected by the main transistor is removed by the dummy switch. These two transistors are fed by out-of-phase signal levels, which means one of them is on while the other is off. The channel charge of the main transistor is absorbed by the dummy transistor, to be used in its own channel creation, as it is shown in Fig. 3.10.

The clock feedthrough problem and parasitic capacitance between poly 1 and substrate layers, are tried to be solved by the offset cancellation stage. The method used to solve this problem related to the erroneous voltage due to the charge storage and transfer to the output, is to recreate the same erroneous voltage in another channel exactly same with the channels used in 72 channels, and to subtract this error from the total voltage. Same control signals driving the 72 channels are also sent to the dedicated channel to create the same voltage in that channel. The only difference is that, there is no input current coming to that

channel from the unit cell, so that it only creates the voltage due to switching problem and parasitic capacitance.

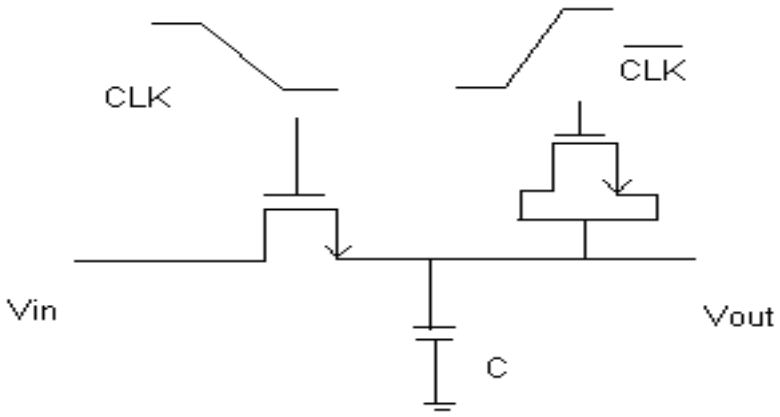

Figure 3.10: Dummy switch used to eliminate charge injection problem

The offset cancellation stage has the TDI amplifier and a channel crating the offset voltage. 1.7 V is added to the difference between the actual signal and offset signal, in order to be in output range of 1.7 V – 4.5 V, as a requirement of ROIC. The output voltage of the amplifier in Fig. 3.11 can calculated as the following:

$$V_{out} = V_{TDI} - V_{offset} + 1.7V \quad [V] \tag{3.2}$$

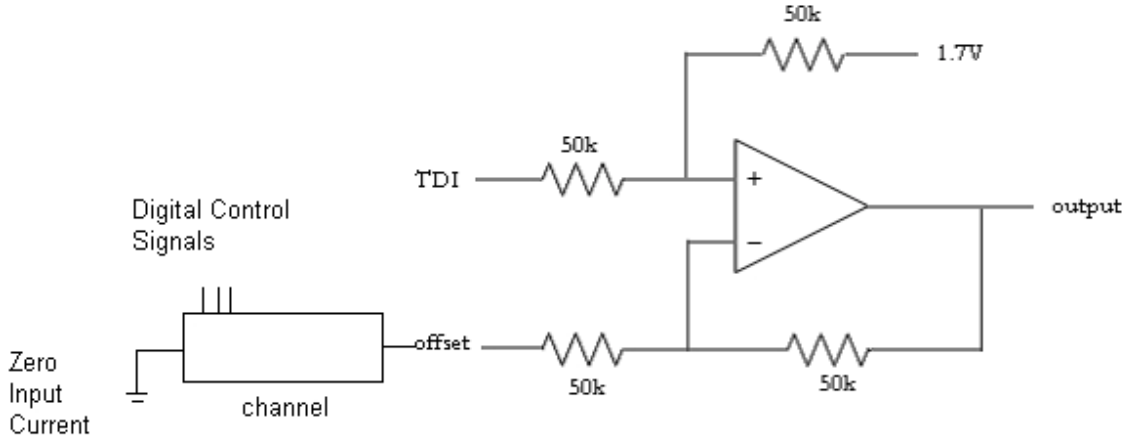

Figure 3.11: Schematic of offset cancellation stage

The amplifier used in the offset cancellation stage is similar to the amplifier used in TDI stage, a two stage differential stage followed by a common source stage with resistive compensation. The gain of the amplifier is 60.4 dB, phase margin is 71 degrees, and power consumption is 2 mW. The slew rate of the amplifier is 100 V/µs with a 1 pF load. The schematic of the offset cancellation amplifier is shown in Fig. 3.12.

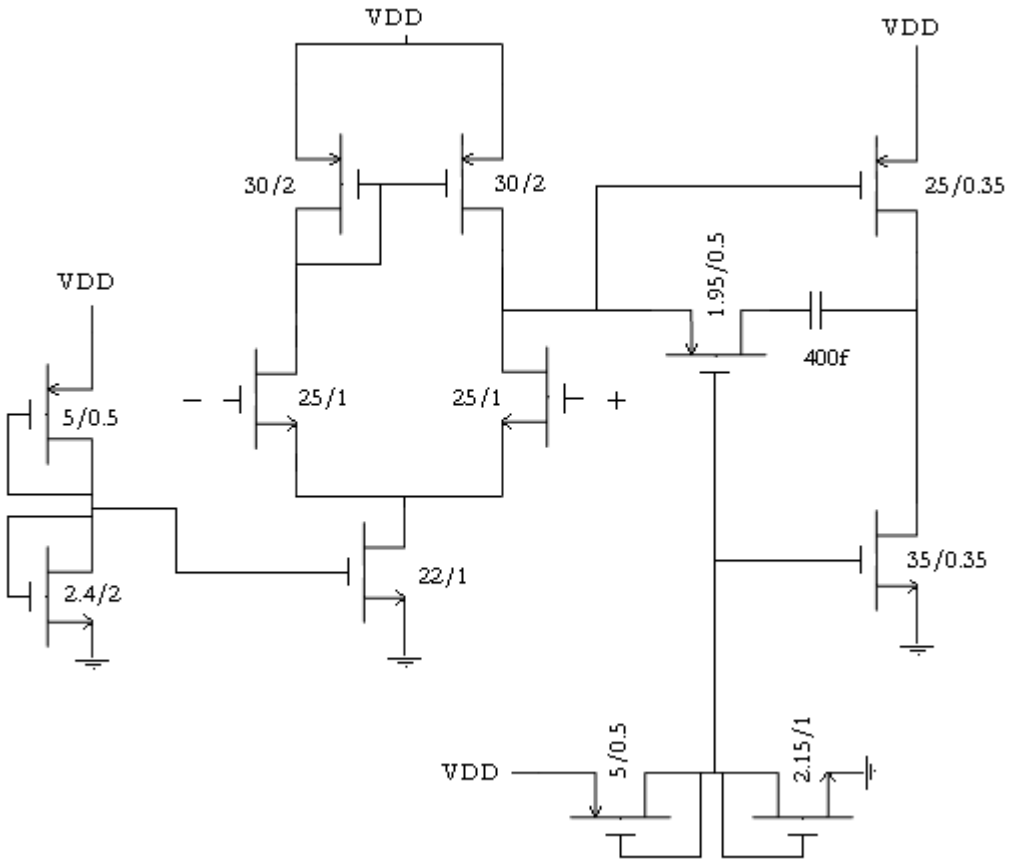

Figure 3.12: Schematic of offset cancellation amplifier

One important addition to the offset cancellation stage is the automatic gain adjustment property in the case of a malfunctioning pixel in one of the four detector pixels. Dead pixels are determined in detector tests and, the information of dead pixels is programmed through the serial interface of the ROIC. Each pixel has the latch to hold the data, whether it functions properly or not. If a pixel is programmed to be malfunctioning, the gain of the amplifier is multiplied by 1.33 in order to compensate the dead pixel. However, this dead pixel property is valid for one pixel out of four pixels. If more than one pixel is dead, the

gain is also multiplied by 1.33. This is done by changing the values of resistors of the amplifier, by switching additional two transistors as shown in Fig. 3.13.

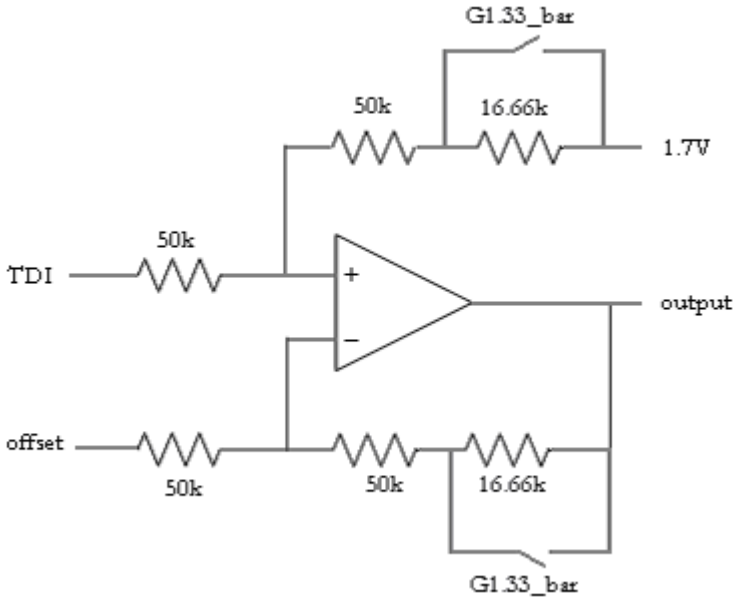

Figure 3.13: Schematic of automatic gain adjustment

If there is no dead pixel, G1.33_bar switch is on, and the resistor ratio is same of the original design. However, if one or more of the pixels are dead, G1.33_bar switch is off, and resistor ratios become 4/3 (1.33) to compensate the dead pixel, and the new output voltage of the amplifier becomes:

$$V_{out} = (V_{TDI} - V_{offset})1.33 + 1.7V \quad [V] \tag{3.3}$$

The G1.33_bar switch input is created by a simple four input NAND gate and an inverter. The latches of all detector pixels are programmed through the serial interface. All of the four latch data are connected to the NAND gate. If at least one of the pixels is dead, NAND gate output becomes logic 1, which is G.133 signal level.

The resistors used in the amplifier design are chosen as 50 kΩ, however if more power consumption is allowed, smaller resistors can be used. There is a trade-off between the noise performance and power consumption. If resistors are larger, they have worse noise performance, if they are smaller, there is more power consumption.

3.3.4 Output Buffer Stage

The output buffer is designed for 10 pF load capacitance and 1 MΩ shunt resistance as the output requirement of ROIC. 1 mV settling error is allowed within 100 ns rise time. High slew rate with a good phase margin is also desired. The required output waveform is given in Fig 3.14.

Similar to the TDI amplifier and offset cancellation and automatic gain adjustment amplifier, a two stage differential amplifier followed by a common source amplifier is used as the circuit topology of output buffer. Its output is connected to the negative input of the amplifier.

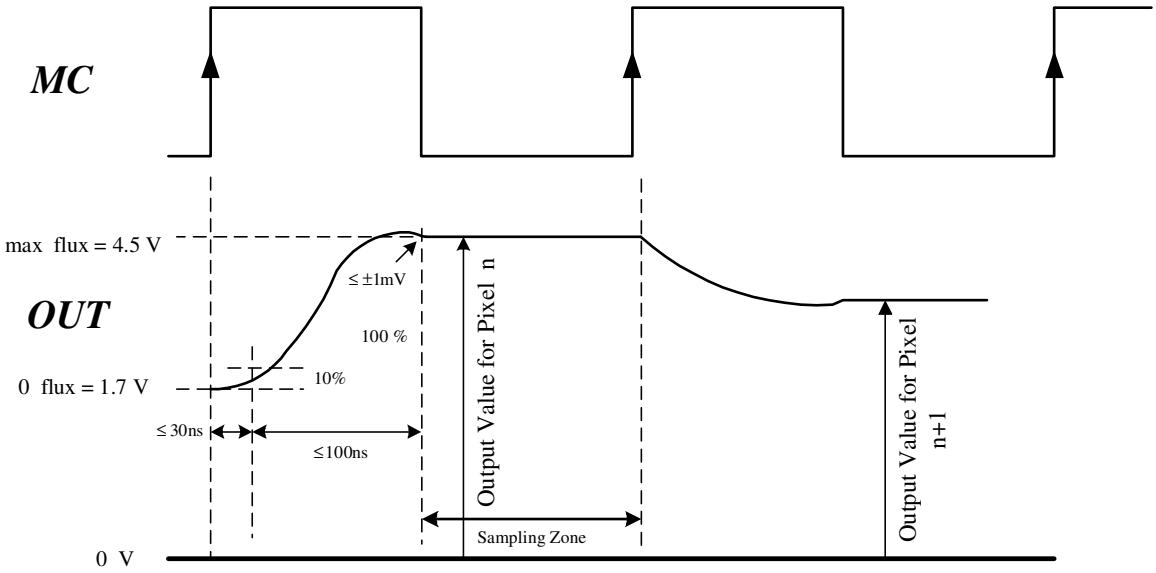

Figure 3.14: Output waveform of ROIC

The designed amplifier has 68.7 dB gain with a phase margin of 45 degrees. Power consumption is 5.9 mW, whereas the slew rate is 65 V/µs. The designed amplifier schematic is given in Fig. 3.15.

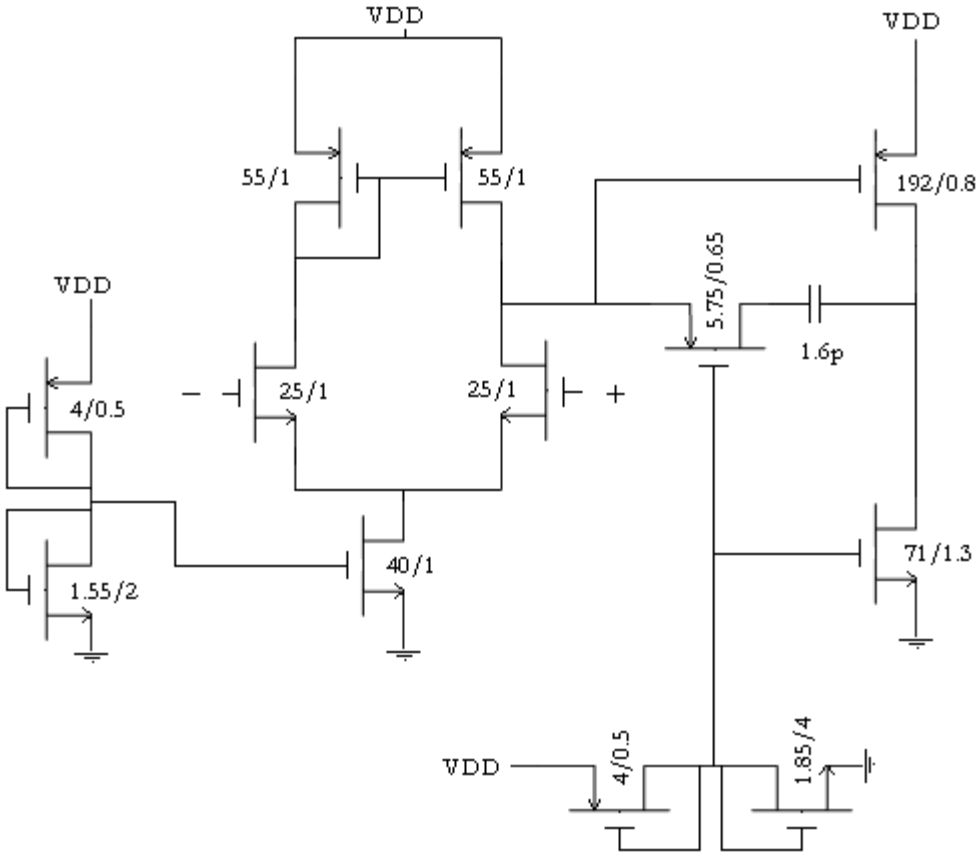

Figure 3.15: Schematic of output buffer amplifier

3.3.5 Digital Circuit Design

Digital part of the readout integrated circuit (ROIC) consists of a main digital block, a parallel/serial interface, a level shifter, an address decoder, a channel select decoder, decoders for S1, S2, INT, RESET signals and flip-flops to prevent glitches. The top view of digital circuit is shown in Fig. 3.16.

Task of the main digital block is to produce the S1, S2, RESET and INT signals for the analog circuitry. According to the timing of these signals and integration time together with the gain setting, analog circuitry writes on the capacitor blocks and reads from them thanks to the TDI algorithm. S1 ve S2 switches are used for reading from the capacitor blocks and writing to capacitor blocks, while RESET switch is used to reset the capacitor blocks. The

INT switch is used to charge the capacitor blocks. Duration of this signal, determined by integration time set by the user, affects how much time capacitor blocks are charged by the detectors.

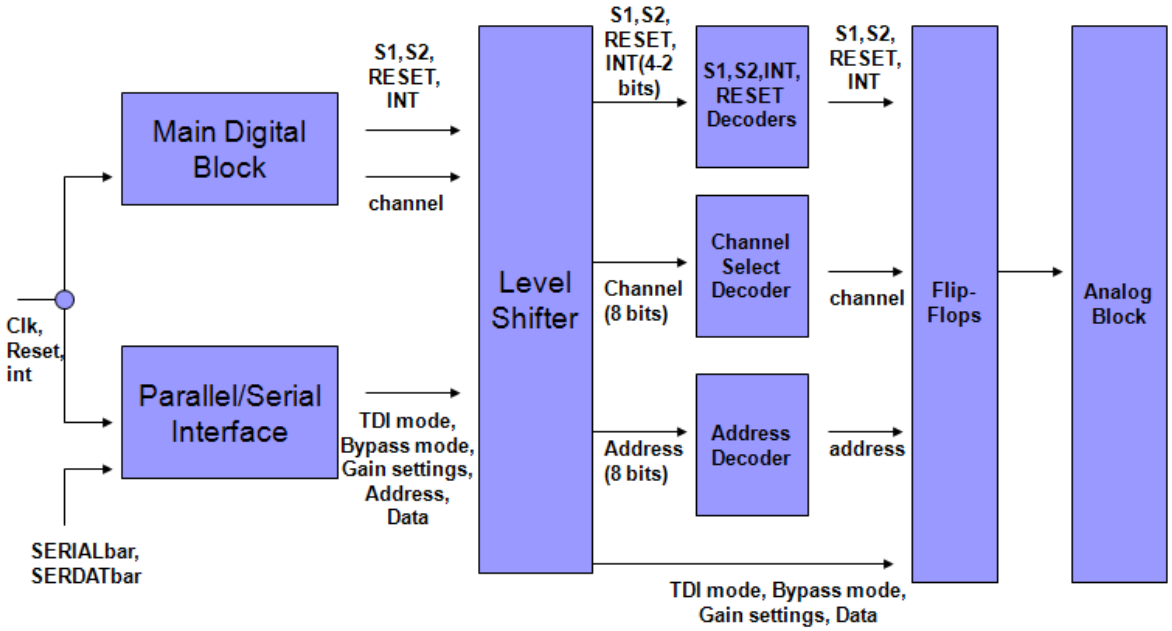

Figure 3.16: Digital architecture of ROIC

There are two interfaces possible for the operation of the ROIC: parallel interface and digital interface. The main digital block is driven by one of these interfaces. User determines the type of interface with the SERIALbar signal.

Parallel interface is used for the basic operation of ROIC which is to use the ROIC just with the TDI direction and gain settings. BYPASS mode is also supported by the parallel interface to test the circuit.

On the other hand, serial interface adds the functionality of pixel deselection to the parallel interface. To determine which pixel is selected or not, an interface to set the pixel data and addresses, is added to the circuit.

Level shifter converts the signal levels of main digital block and parallel/serial interface from 3.3 V to 5 V, due to the fact that analog part of the design operates at 0-5 V range.

Since the level shifter consumes much of the power of digital circuit, in order to minimize the power consumption, decoders are put out of the synthesized part, although it is much easier to implement decoder with Verilog HDL language and to synthesize it.

Channel select decoder is used to select the appropriate channel to be connected to the TDI stage, hence to the output. Address decoder is used to program the pixel select/deselect latches, to give the proper addressing. According to the pixel address, data is written to the latches of that pixel through the serial interface. Finally, flip-flops are put to prevent the glitches, because glitches might appear at the outputs of decoders, which is unacceptable for the analog part of ROIC.

3.3.5.1 Main Digital Circuit

The main digital block can be driven both by the parallel interface or serial interface. That is to say, this block controls the analog circuitry by the commands of parallel interface or serial interface. This choice is done by the user. If user want to use the functionality of pixel deselection, then serial interface is mandatory. If pixel deselection functionality is not needed, parallel interface will be the choice.

The block diagram of the main digital block is given in Fig. 3.17. There are four detectors, hence four different detector datapaths. They are very similar. The only difference between the detector datapaths is the number of bits. Since there are different number of capacitors for each detector, signals going to these detectors have different number of bits.

Read start module takes its input from the frame counter module and sends its out signal to the detector datapath module. After frame counter 11 block, which is used for detector 1, counts to 11, read start signal is activated and the datapath starts reading the capacitor set.

Frame counter module as its name implies, counts the number of frames. There are four different frame counter modules for each of detectors. Frame count 11 counts for detector 1, frame count 8 counts for detector 2, frame count 5 counts for detector 3, and finally frame count 2 counts for detector 4 as a consequence of TDI (time delay integration) algorithm.

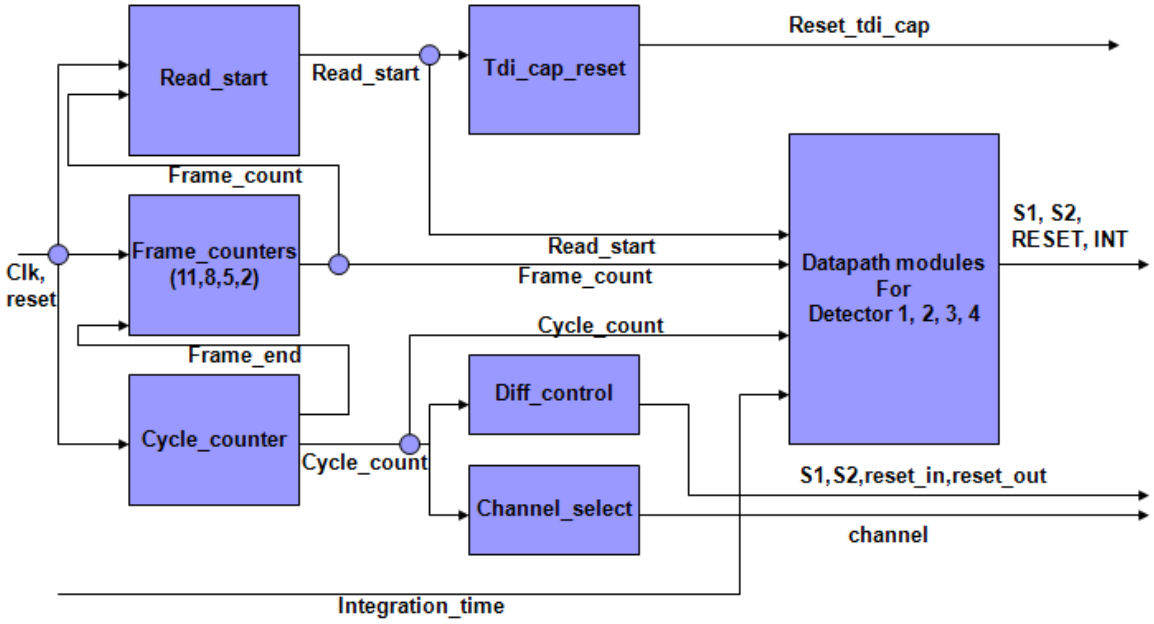

Figure 3.17: Architecture of digital control block

Cycle count module counts the number of clock cycles, and at the end of 256 successive cycles, it produces the frame end output signal. This frame end signal cause the frame counters to increase by 1.

Detector datapath modules are the main modules that produce the necessary S1, S2, RESET and INT signals for the analog circuitry. These detector datapath modules take the frame counter outputs as their inputs, and produce the appropriate signals for each frame. For each different frame, there are different signal combinations going to the analog circuitry.

Another block of the digital main block is the channel selection part. Channel selection circuitry is put in each channel of the analog part. This part is also controlled by the digital part. Cycle counter has 8 bits output to count 256 cycles. Since, 72x4 ROIC is implemented in this version, 72 channel is needed. For this purpose, lower 7 bits of the cycle counter is used. Then, a 7x72 decoder is used for the channel selection. First 72 outputs of the 128 outputs are used for the channel selection. Since the address decoder is implemented by the combination of 3x8 decoders, 9 3x8 decoders are used for this address decoder. In the first 4 cycles, there is no operation. After the fourth cycle the first output of the address decoder

is activated and it continues accordingly. The outputs of the channel select decoder drive the channel selection circuitry in the analog part.

Another block in the digital main block is the diff_control block. This block is used to produce appropriate signals for the offset cancellation stage in the analog part. Desired switching activities are implemented by the diff_control block and are sent to the offset cancellation stage. This error produced by the offset cancellation stage is then subtracted from the main signal, and more accurate data is given to the output buffer stage. In order to produce the correct error signal, diff_control block should exactly mimic the behavior of the detector datapath circuits. The switching activities of S1, S2, RESET and INT signals has to be mimicked correctly by this circuit.

The digital main block is implemented using Verilog HDL, simulated by Modelsim, synthesized by Synopsys Design Vision and placed & routed by Silicon Ensemble using AMS 0.35 µm CORELIB.

3.3.5.2 Parallel/Serial Interface Circuit

The ROIC can be programmed both with parallel interface and serial interface. Parallel interface is the basic programming mode with default properties. Serial interface adds the functionality of pixel select/deselect through supplying relevant data to the pixel address decoder and pixel latches. The block diagram of the parallel/serial interface is shown in Fig. 3.18.

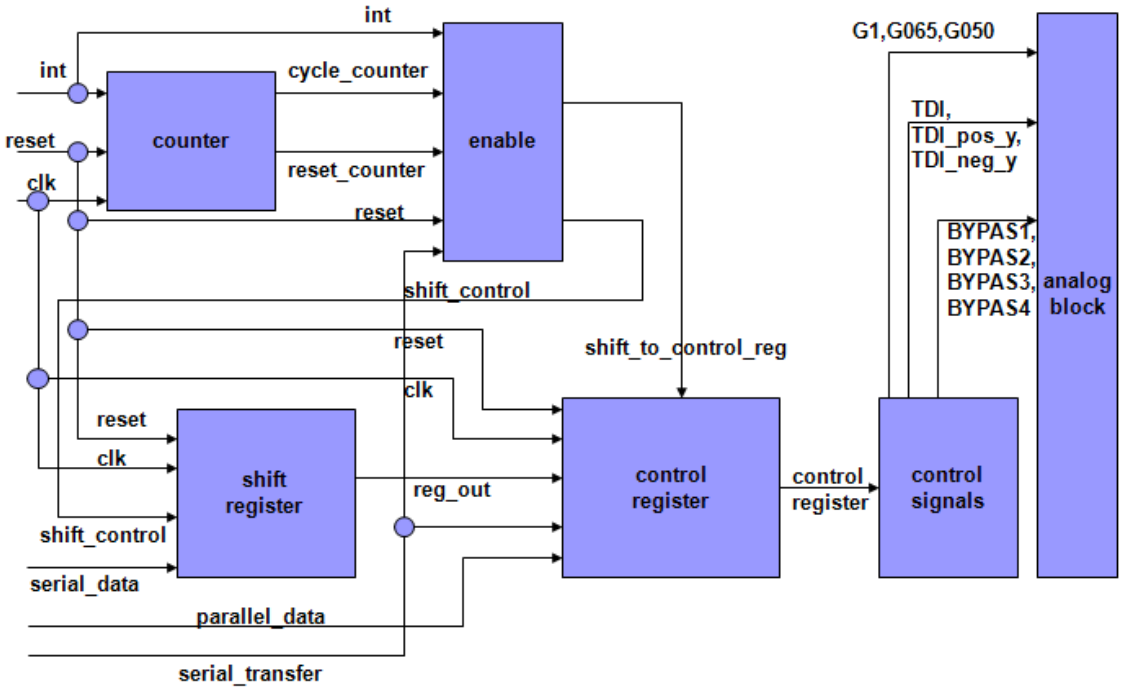

Figure 3.18: Architecture of parallel/serial interfaces

3.3.5.2.1 Parallel Interface

The parallel interface is the basic operation mode of ROIC. With the parallel interface in active mode, ROIC can be operated with TDI mode or BYPASS mode. Bidirectionality and gain adjustment are also possible with the parallel interface.

There are six inputs of the parallel interface:

SERIALbar: This input is used to determine the operation mode of the ROIC. If SERIALbar=1 which also means SERIAL=0, it means that the ROIC is in parallel mode. The default value of the SERIALbar is high.

PGAIN2bar: One of the two bits of gain adjustment. Default value is high.

PGAIN1: One of the two bits of gain adjustment. Default value is high.

PDIRbar: This input determines the direction of the TDI scan. Default value is high.

PBYPAS2bar: One of the two bits of BYPASS adjustment.

PBYPAS1bar: One of the two bits of BYPASS adjustment.

Two bits are needed for gain adjustment and BYPASS modes, because there four possible gain settings and four possible BYPASS modes. With the default values stated above, ROIC is in TDI mode scanning in the +y direction and has the gain setting of 1.

Four different gain settings and corresponding gain ratios are given in Table 3.3:

GAIN2	GAIN1	Cint(pF)	Gain Ratio
0	0	0.35	1.30
0	1	0.46	1
1	0	0.70	0.65
1	1	0.92	0.50

Table 3.3: Control bits for gain settings of ROIC

Six different settings with TDI or BYPASS modes are given in Table 3.4:

DIR	BYPAS2	BYPAS1	MODE
0	0	0	TDI along +Y (default)
0	0	1	BYPASS on diode 1
0	1	0	BYPASS on diode 2
1	0	0	TDI along –Y
1	0	1	BYPASS on diode 4
1	1	0	BYPASS on diode 3

Table 3.4: Control bits for TDI direction and test mode

3.3.5.2.2 Serial Interface

Serial interface is activated if the serial_transfer is high. In serial mode, in addition to the different gain settings and bypass modes, pixel deselection functionality can also be used. For this purpose, control register is used. The SERDAT bar is the external input to load the control register.

There is a two stage pipelined architecture consisting of a shift register and a control register. SERDAT bar input is connected to the shift register. Shift register continuously shifts the inputs. After 24 cycles the 24 bit control register data is ready on the shift register. In the following cycles with the negative edge of the INT signal, this 24 bit data is parallel loaded to the control register.

So, in order to operate the ROIC in the serial mode, first serial_transfer input is to be set to logic high. After serial transfer is activated, negative edge of the INT signal is waited. With the negative edge of the INT signal, SERDAT bar input is started to be loaded to the shift register cycle by cycle. This load operation of the shift register takes 24 cycles. After 24 cycles, the interface waits the negative edge of the INT signal for the shift register to be parallel loaded to the control register. If serial transfer input remains logic high, then with the next negative edge of the INT signal, next 24 bits can be loaded to the control register with the same procedure. So, ROIC is programmed by this way in the serial mode.

The important thing while programming the circuit is not to make INT signal up and down with the intervals shorter than 24 cycles, because this is not a valid input pattern. If serial mode is selected and INT signal is made up and down, that means the start of the serial transfer. Serial data has to be provided for the following 24 cycles, then INT signal can be changed again in order to load the data from shift register to control register.

Control register consists of 24 bits, which are 8 bits control word, 8 bits data word and 8 bits address word, which is shown in Table 3.5. Control word consists of the following bits:

CNT: At logic high level it allows to write on the registers GAIN2, GAIN1, DIR, BYPAS2, BYPAS1 and SELECT. At logic low level, it locks the access to these registers.

GAIN2 and GAIN1: Gain setting bits same as mentioned in the parallel interface.

DIR, BYPAS2 and BYPAS1: TDI direction and bypass mode adjustment bits as mentioned in the parallel interface.

SELECT: At logic low level, it enables pixel deselection functionality, at logic high level it forces all pixels to be selected.

PGM: At logic low level, it deactivates the data writing to the data word part of the control register. At logic high level, it allows the data writing for selection or deselection at the address indicated in the address word.

SIGNAL	CNT	GAIN2	GAIN1	DIR	BYPAS2	BYPAS1	SELECT	PGM	8 bit data for selection/deselection of pixel								8 bit pixel program address							
bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
	WORD CONTROL : 8 BITS								DATA WORD : 8 BITS								ADDRESS WORD : 8 BITS							

Table 3.5: Control register bits of ROIC

One data word holds the information of 8 pixels. If the data word is logic high for a pixel, then it means that this pixel is selected. If it is logic low, then this pixel is deselected. The first four bits hold the information of channel (2n-1), while the last four bits hold the information of channel 2n.

The address word bits are used as the following: The bit <7> is used for the selection of addressed channel block (lower part or higher part of the array). The lower 7 bits starting from bit <6> to the last bit <0> address 72 lines. By this way 144 lines can be addressed, and there are two channels in a line, which means all 288 channels can be addressed.

Verilog HDL code implementing the parallel/serial interface functionality is written and simulated in Modelsim environment. Interfaces are synthesized in Synopsys Design Vision and placed & routed in Silicon Ensemble using AMS 0.35 µm CORELIB library, like the digital main block.

4 SIMULATION and MEASUREMENT RESULTS

Simulations for 72×4 P-on-N ROIC are done with different amount of input currents, and with different gain settings, in order to test the effect of input current and gain settings. Simulation results are taken from four different stages, which are integration capacitor stage, TDI output, offset cancellation/automatic gain adjustment output, and output buffer. The integrated voltage on the integration capacitor should be same with the output voltage, if 1.7 V amplifier offset is subtracted from the output voltage. It is also possible to see that, the difference of TDI output and offset cancellation stage output is same with the integration capacitor voltage and output voltage, if 1.7 V amplifier offset is subtracted from the output voltage.

4.1 Simulation Results of Minimum Input Current

Results in Figs 4.1 – 4.4 show that 35 mV is integrated onto the integration capacitor. At TDI stage, with addition of the switching and parasitic effects, 158 mV is added. At the offset stage 133 mV is observed, while the output voltage is 27 mV, which is close to the integrated voltage at the input capacitor.

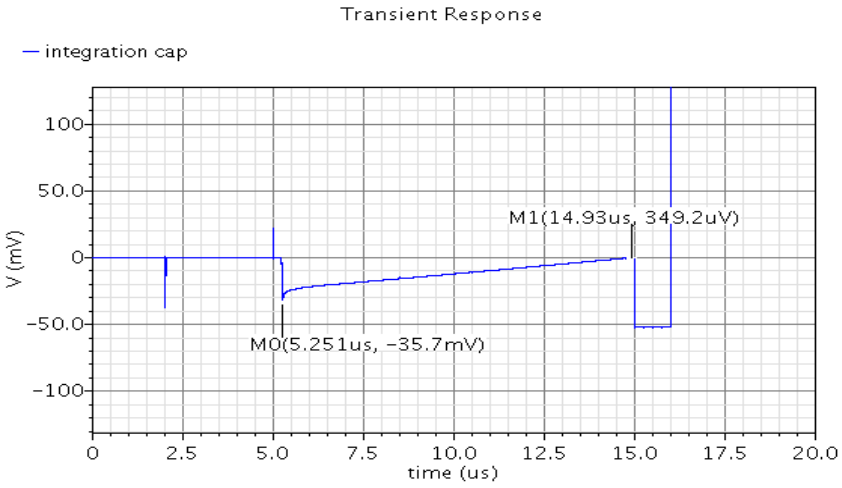

Figure 4.1: Voltage at the integration capacitor for 10 µs integration time with G1 setting for minimum input current

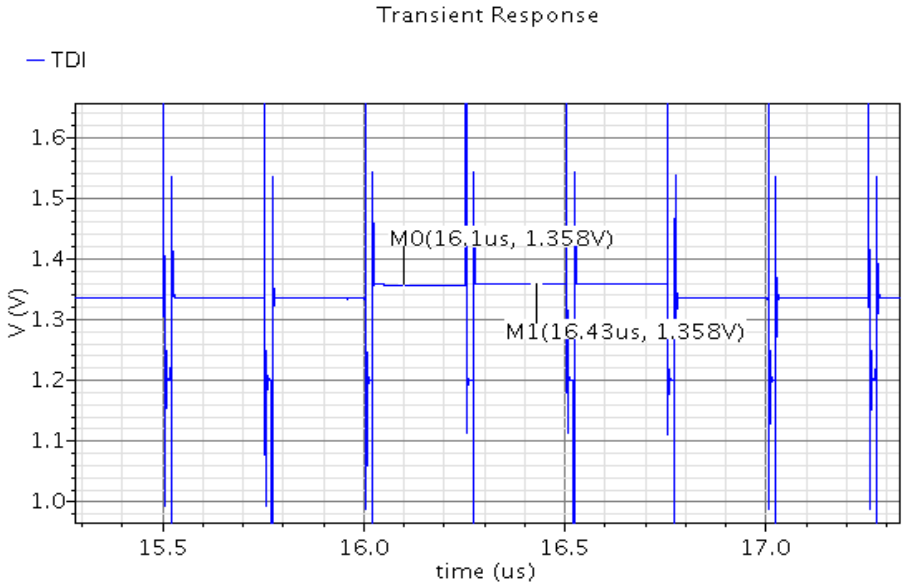

Figure 4.2: Voltage at TDI output for 10 µs integration time with G1 setting for minimum input current

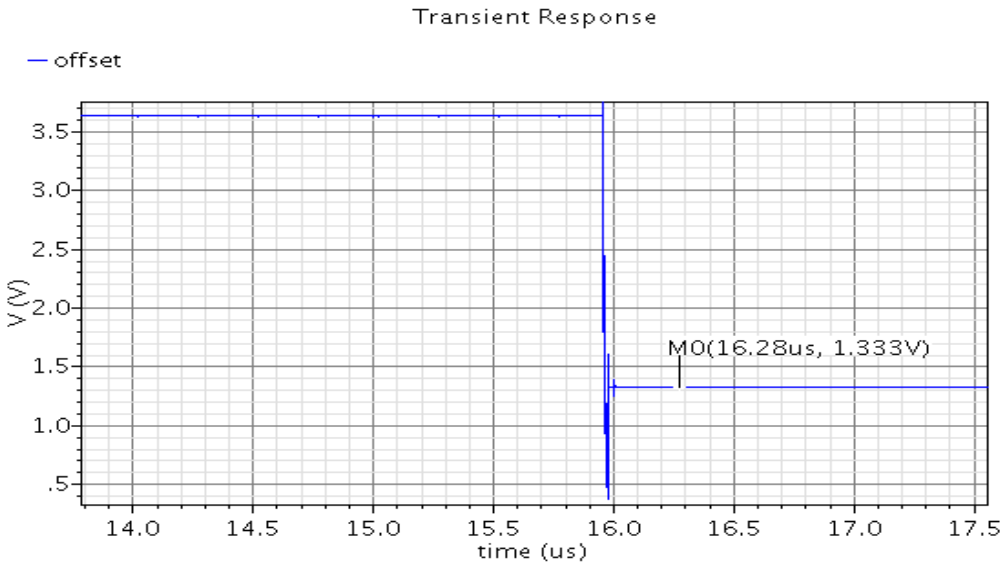

Figure 4.3: Voltage at offset cancellation stage output for 10 µs integration time with G1 setting for minimum input current

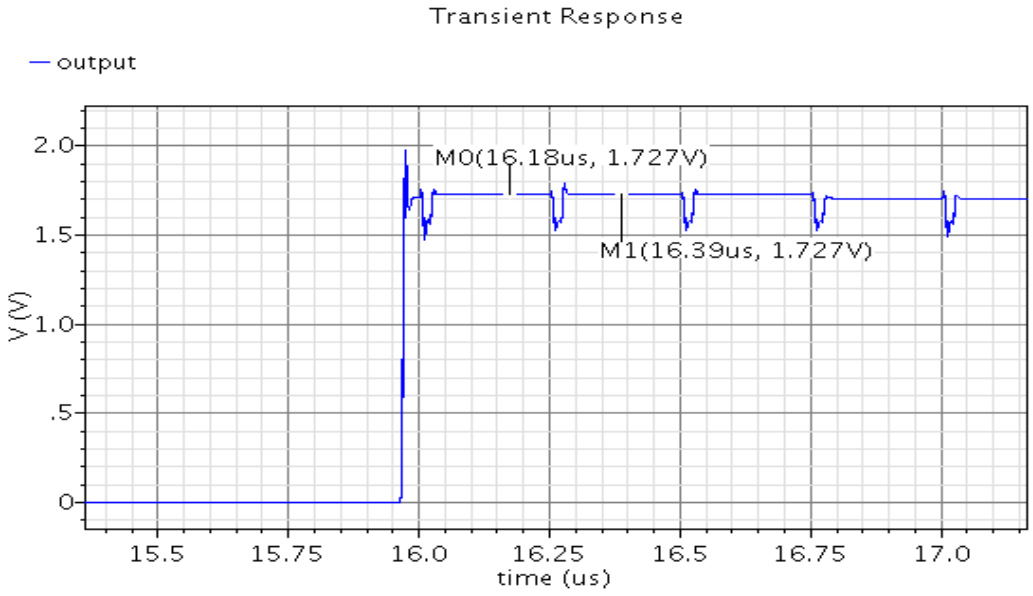

Figure 4.4: Voltage at the output for 10 µs integration time with G1 setting for minimum input current

4.2Simulation Results of 25 nA Input Current

Results in Figs. 4.5 – 4.8 show that 537 mV is integrated onto the integration capacitor. At TDI stage, with addition of the switching and parasitic effects, 667 mV is added. At the offset stage 133 mV is observed, while the output voltage is 539 mV, which is close to the integrated voltage at the input capacitor.

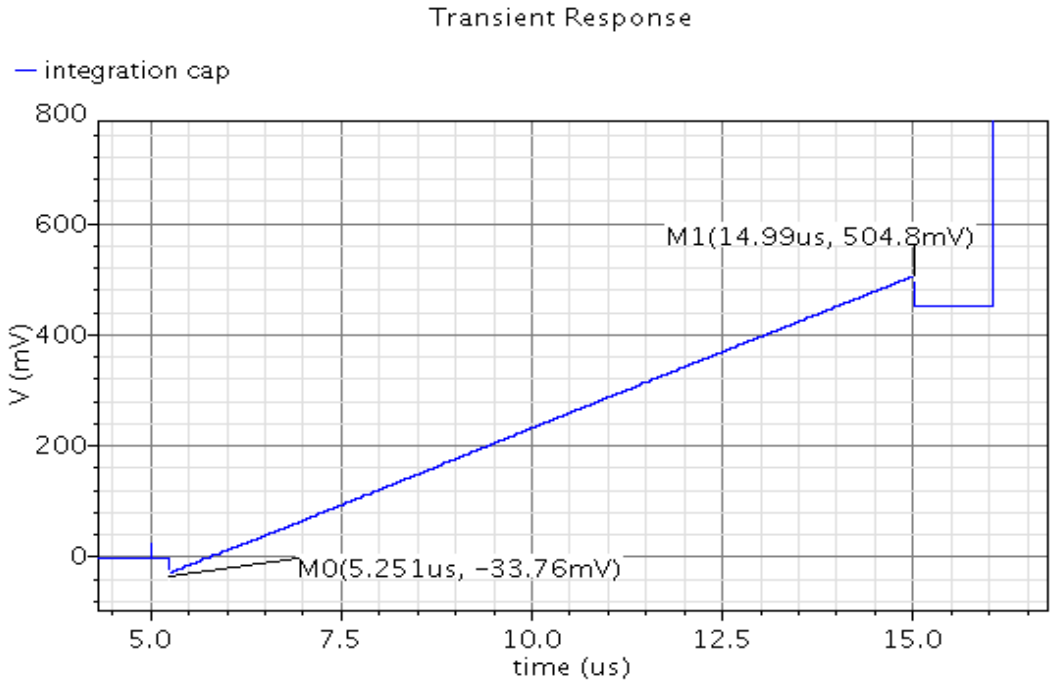

Figure 4.5: Voltage at the integration capacitor for 10 µs integration time with G1 setting for 25 nA input current

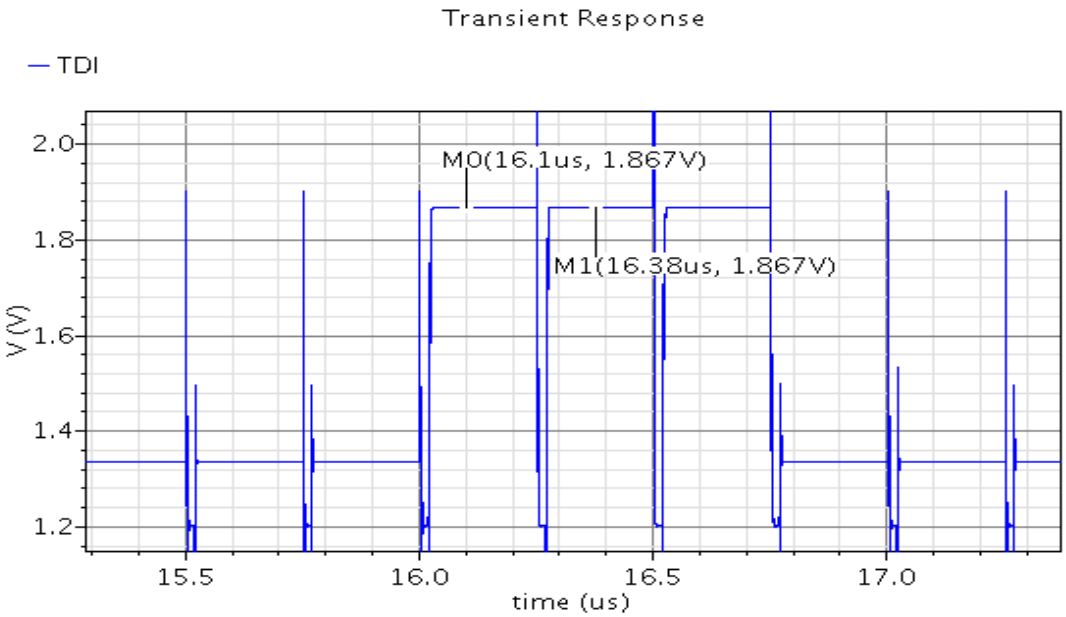

Figure 4.6: Voltage at TDI output for 10 µs integration time with G1 setting for 25 nA input current

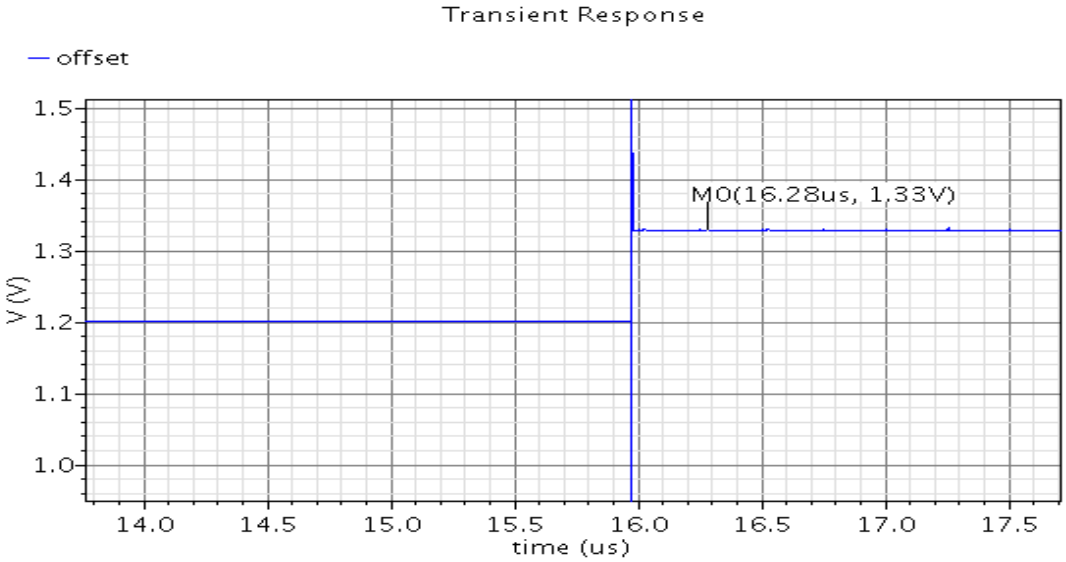

Figure 4.7: Voltage at offset cancellation stage output for 10 µs integration time with G1 setting for 25 nA input current

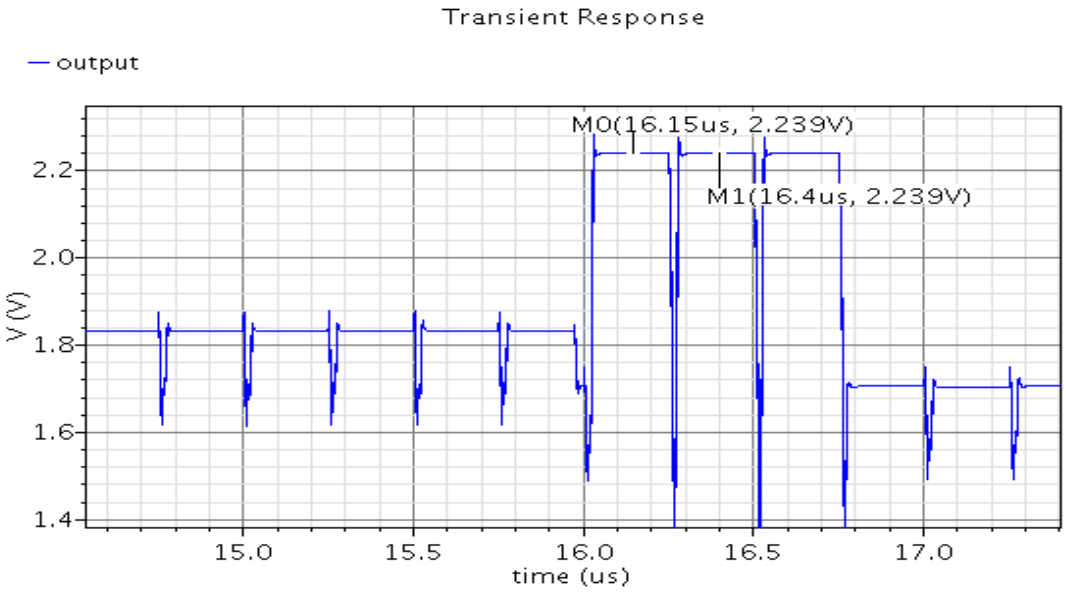

Figure 4.8: Voltage at the output for 10 µs integration time with G1 setting for 25 nA input current

4.3Simulation Results of Maximum Input Current

Results in fig. 4.9 -4.12 show that 1088 mV is integrated onto the integration capacitor. At TDI stage, with addition of the switching and parasitic effects, 1218 mV is added. At the offset stage 133 mV is observed, while the output voltage is 1091 mV, which is close to the integrated voltage at the input capacitor.

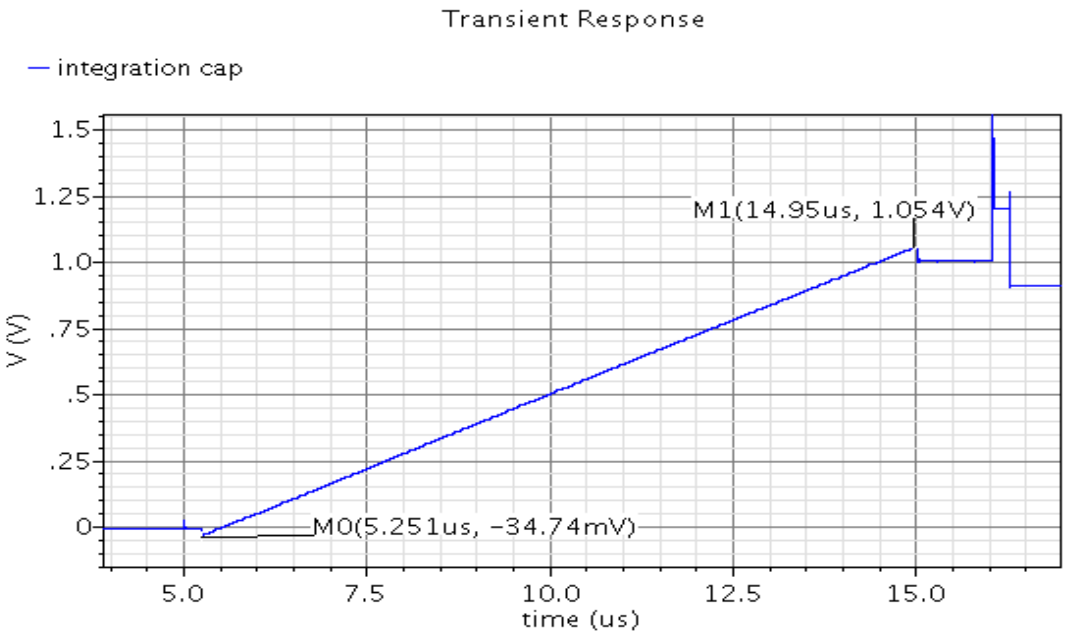

Figure 4.9: Voltage at the integration capacitor for 10 µs integration time with G1 setting for maximum input current

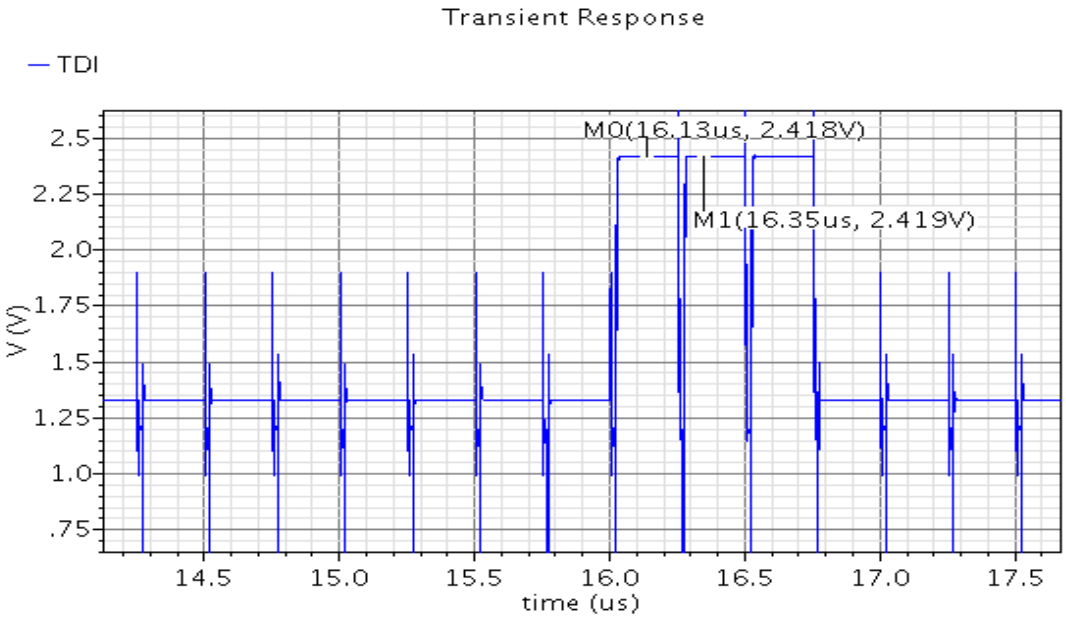

Figure 4.10: Voltage at TDI output for 10 µs integration time with G1 setting for maximum input current

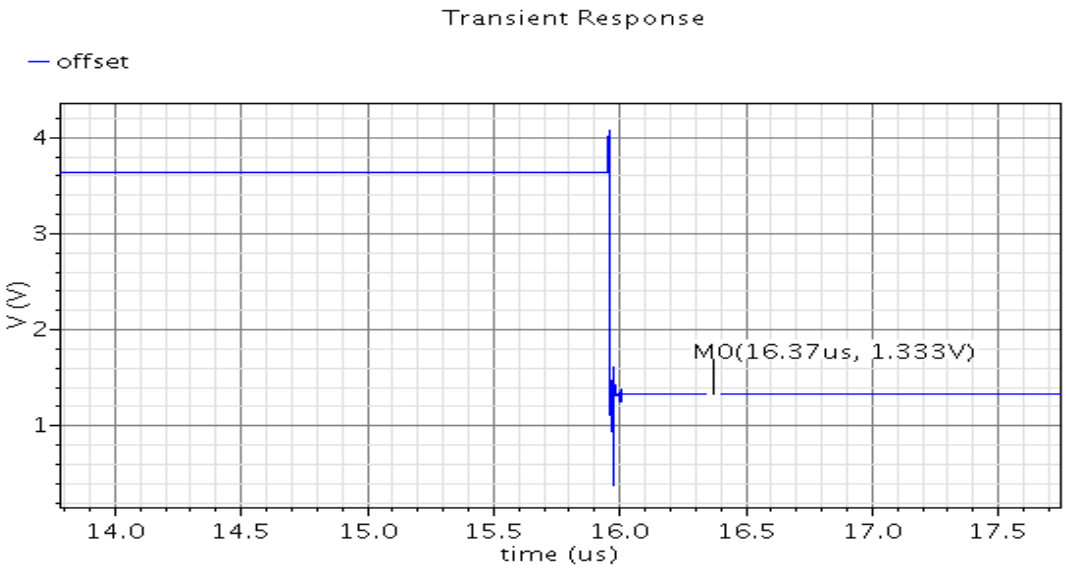

Figure 4.11: Voltage at offset cancellation stage output for 10 µs integration time with G1 setting for maximum input current

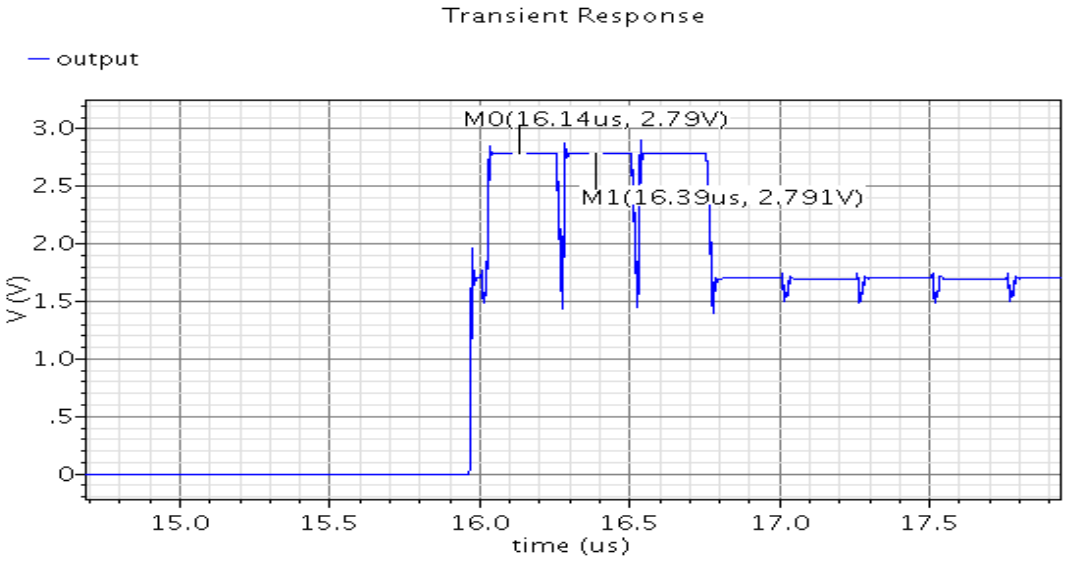

Figure 4.12: Voltage at the output for 10 µs integration time with G1 setting for maximum input current

4.4Simulation Results with G0.50 Setting

Results in Figs. 4.13 – 4.16 show that 551 mV is integrated onto the integration capacitor. At TDI stage, with addition of the switching and parasitic effects, 617 mV is added. At the offset stage 64 mV is observed, while the output voltage is 555 mV, which is close to the integrated voltage at the input capacitor. This simulation shows that G0.50 setting works fine, because at gain G0.50 setting, the voltage at the output is expected to be the half of the voltage with gain setting G1, with the same integration time and current. At gain setting G1, output voltage is 1091 mV, while it is 555 mV at gain setting G0.50, which is an acceptable error offset of 19 mV.

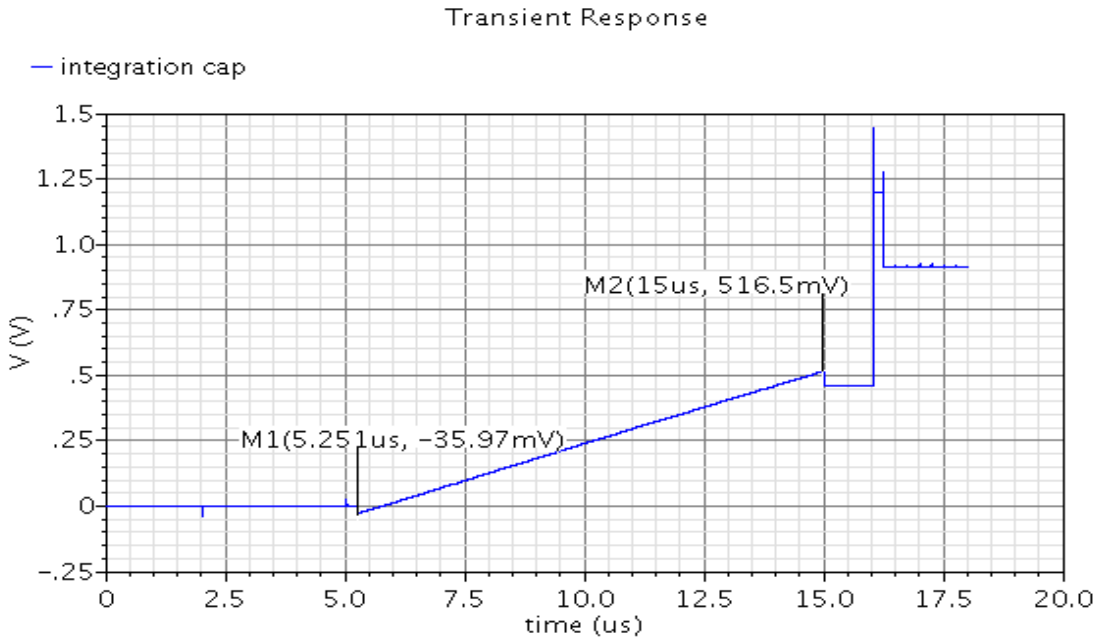

Figure 4.13: Voltage at the integration capacitor for 10 µs integration time with G0.50 setting for maximum input current

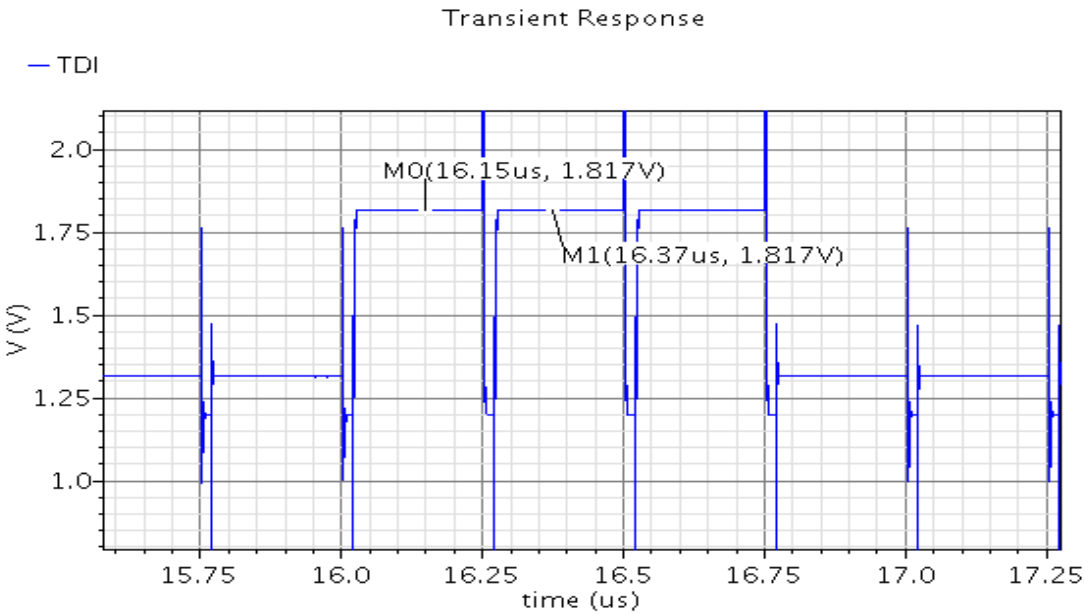

Figure 4.14: Voltage at TDI output for 10 µs integration time with G0.50 setting for maximum input current

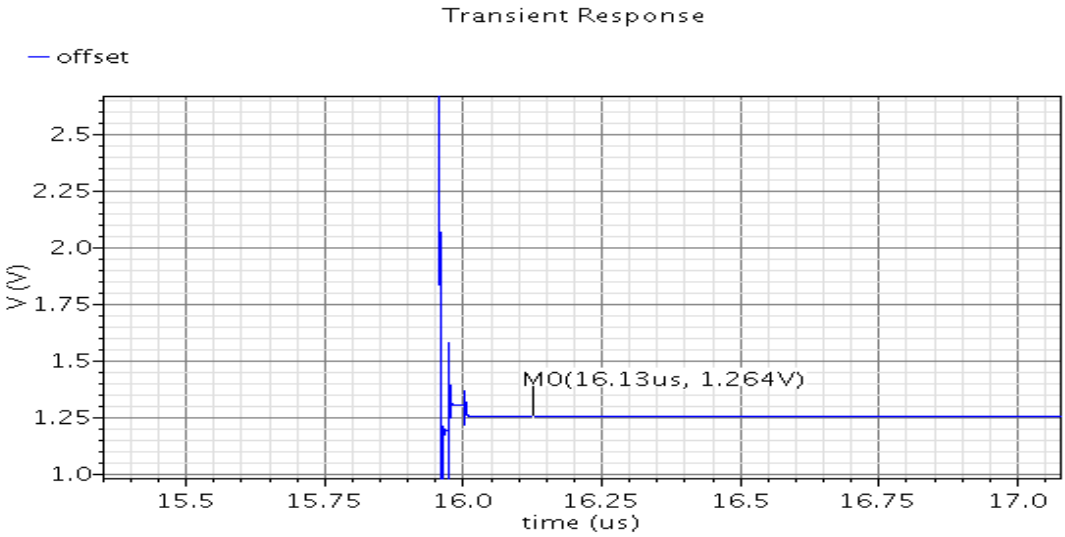

Figure 4.15: Voltage at offset cancellation stage output for 10 µs integration time with G0.50 setting for maximum input current

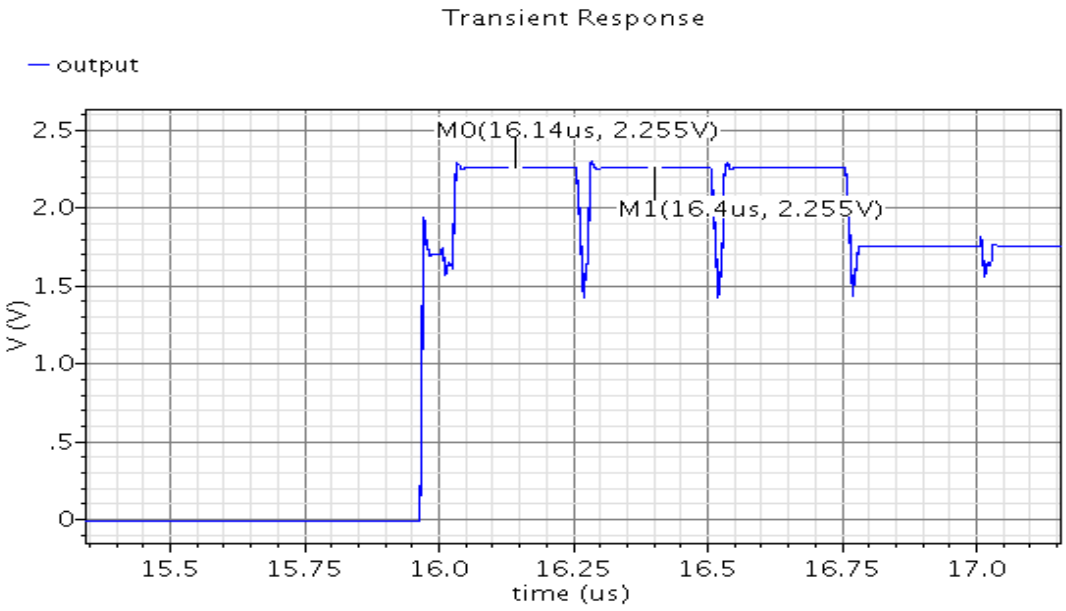

Figure 4.16: Voltage at the output for 10 µs integration time with G0.50 setting for maximum input current

4.5Comments on Simulation Results

Simulation results show that ROIC design works successfully. As explained in previous sections, the output voltage should be the addition of difference between TDI – Offset and 1.7 V. This value should be same with the addition of the integration capacitor voltage and 1.7 V. Simulation results show that there is a difference of 2-8 mV between the output voltage and ideal voltage, which is fine. Simulation results of maximum current with G1 setting and G0.50 setting, also shows that gain settings of ROIC function properly. Since the capacitor size of G0.50 setting is twice the G1 setting, half of the voltage of G1 setting should be integrated in G0.50 setting, which is correct.

	Integration Capacitor	TDI	Offset	Output Simulated	Output Ideal
3nA / G1	35mV	1358mV	1333mV	1727mV	1735mV
25nA / G1	537mV	1867mV	1333mV	2239mV	2237mV
55nA / G1	1088mV	2418mV	1333mV	2791mV	2788mV
55nA / G0.50	551mV	1817mV	1264mV	2255mV	2251mV

Table 4.1: Voltage levels for minimum, 25 nA, and maximum current at 4 different stages of ROIC and corresponding ideal output voltage

4.6 Noise Simulations

Noise analysis is done by transient noise analysis of Cadence Spectre CAD tool. In order to determine the noise contribution of each stage of ROIC, simulation results at the outputs of each stage is taken. For noise analysis multiple run is done for better results, however due to simulation time limitation, noise analysis for 3 runs is used in this analysis. The rms values of noise are calculated according to the equations 4.1 and 4.2.

Equation 4.1 shows the rms values of continuous signals:

$$f_{\text{rms}} = \sqrt{\frac{1}{T_2 - T_1}\int_{T_1}^{T_2} [f(t)]^2\, dt} \tag{4.1}$$

Equation 4.2 shows the rms value calculation of multiple noise data:

$$x_{\text{rms}} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} x_i^2} = \sqrt{\frac{x_1^2 + x_2^2 + \cdots + x_N^2}{N}} \tag{4.2}$$

First rms value of noise simulation run is found using the equation 4.1. Then, multiple rms values are used in equation 4.2 in order to find the total rms noise.

The resulting rms voltage value is converted into charge domain by using the equation 4.3

$$Q = CV \tag{4.3}$$

To find the number of electrons Q is divided by q, which is the charge of an electron.

It is observed that important noise contributors of the ROIC are input unit cell stage and offset cancellation stage as expected. Input unit cell has moderate noise due to CMI unit cell's current mirrors, and offset cancellation stage has large resistors.

The first and second iterations of three iterations done for transient noise analysis are shown in the following sections.

4.6.1 Noise Analysis at the Integration Capacitors Stage

As presented in Figs. 4.17 and 4.18, input referred V_{rms} noise value is found to be 286 µV for this stage. For 460 fF integration capacitance it corresponds to 821 electrons.

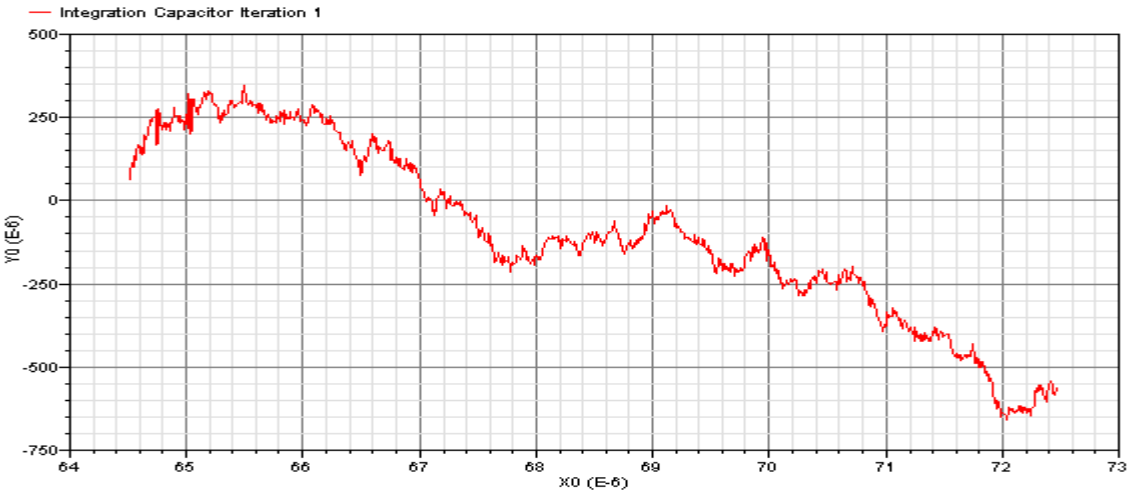

Figure 4.17: Iteration 1 for input referred V_{rms} noise at integration capacitor stage

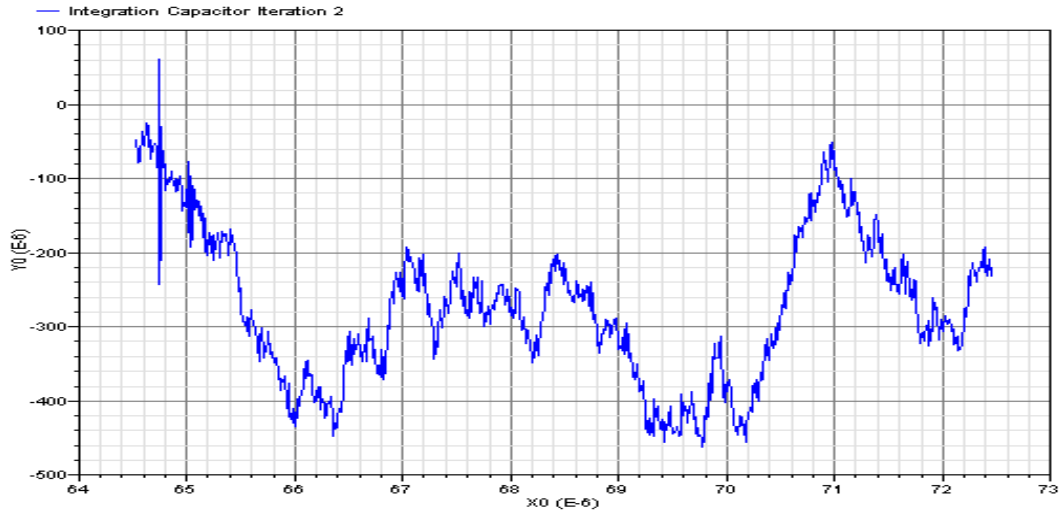

Figure 4.18: Iteration 2 for input referred V_{rms} noise at integration capacitor stage

4.6.2 Noise Analysis at TDI Stage

Input referred Vrms noise value at the output of TDI stage in Figs. 4.19 and 4.20 is found to be 449 µV. With 460 fF capacitance it corresponds to 1289 electrons.

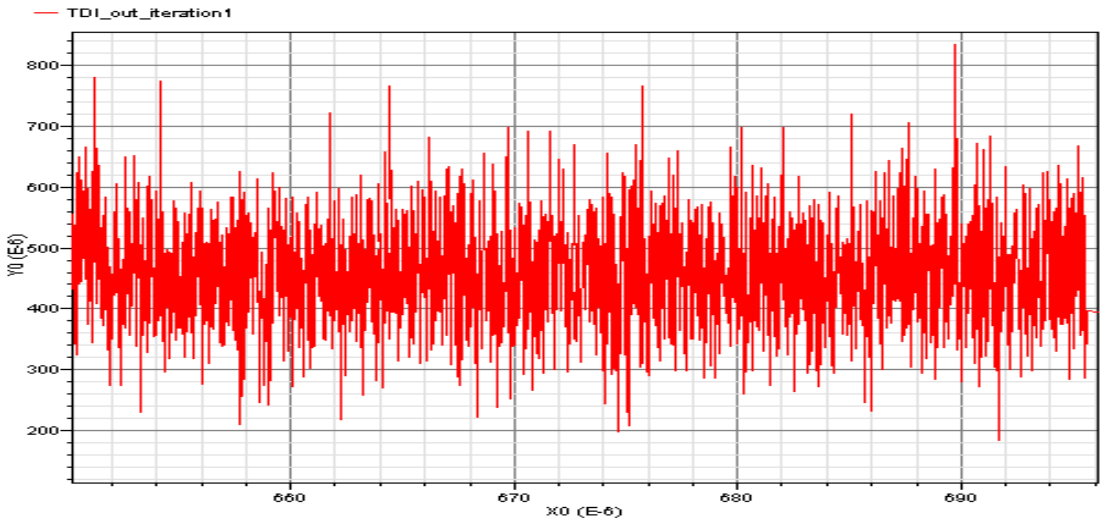

Figure 4.19: Iteration 1 for input referred V_{rms} noise at TDI stage

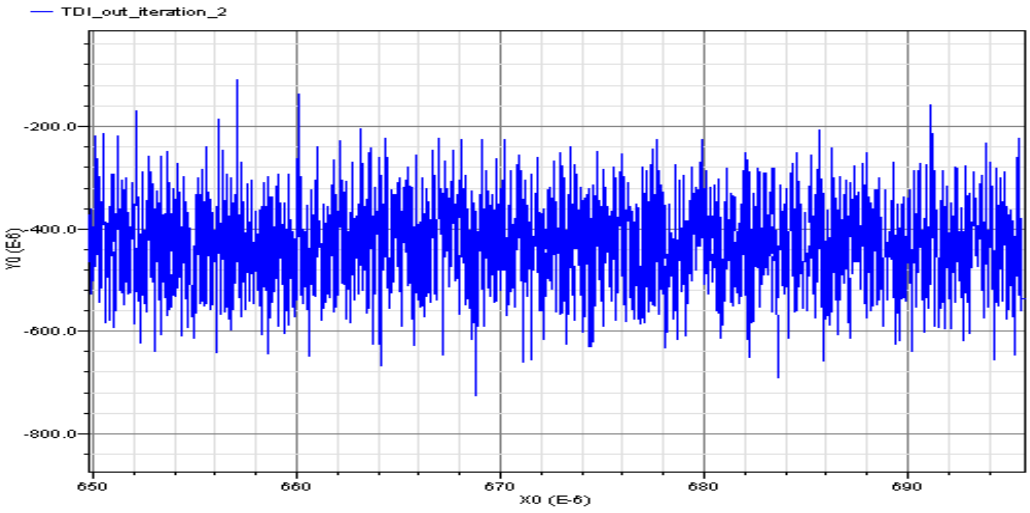

Figure 4.20: Iteration 2 for input referred V_{rms} noise at TDI stage

4.6.3 Noise Analysis at Offset Cancellation Stage

Input referred Vrms noise value at the output of TDI stage, seen in Figs. 4.21 and 4.22 is found to be 1034 µV. With 460 fF capacitance it corresponds to 2969 electrons.

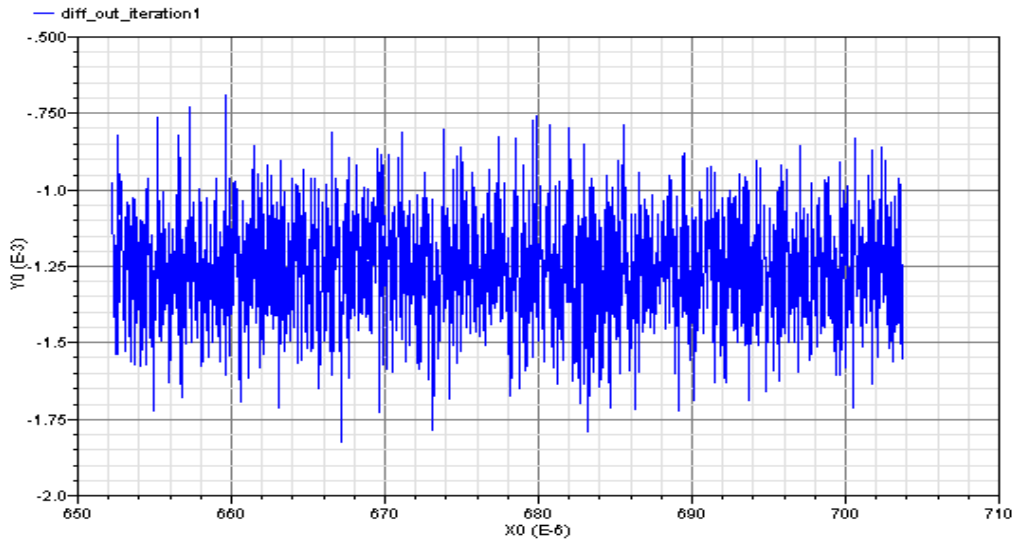

Figure 4.21: Iteration 1 for input referred V_{rms} noise at offset cancellation stage

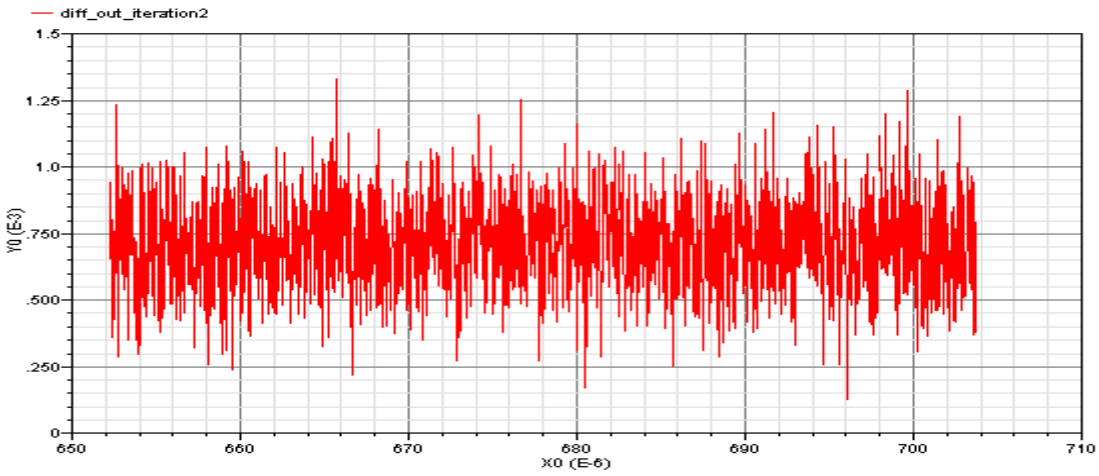

Figure 4.22: Iteration 2 for input referred V_{rms} noise at offset cancellation stage

4.6.4 Noise Analysis at the Output Stage

Input referred Vrms noise value at the output of whole ROIC structure, as presented in Figs. 4.23 and 4.24, is found to be 1037 µV. With 460 fF capacitance it corresponds to 2978 electrons.

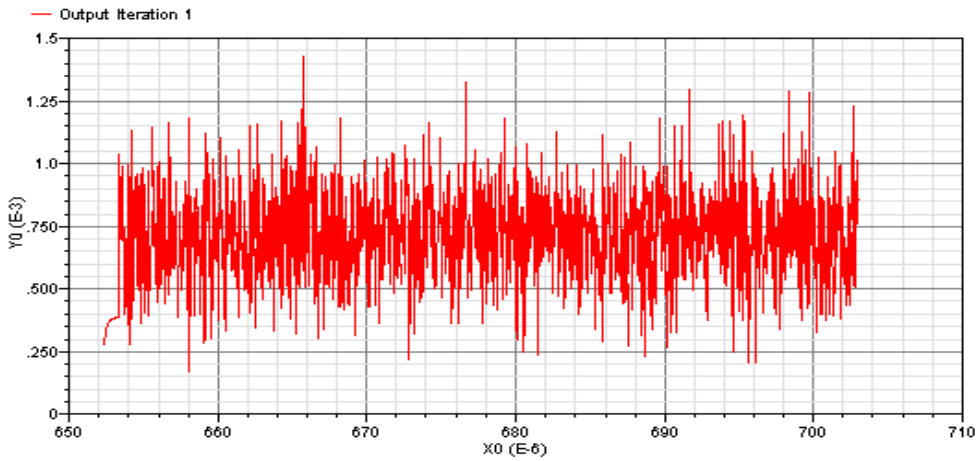

Figure 4.23: Iteration 1 for input referred V_{rms} noise at output stage

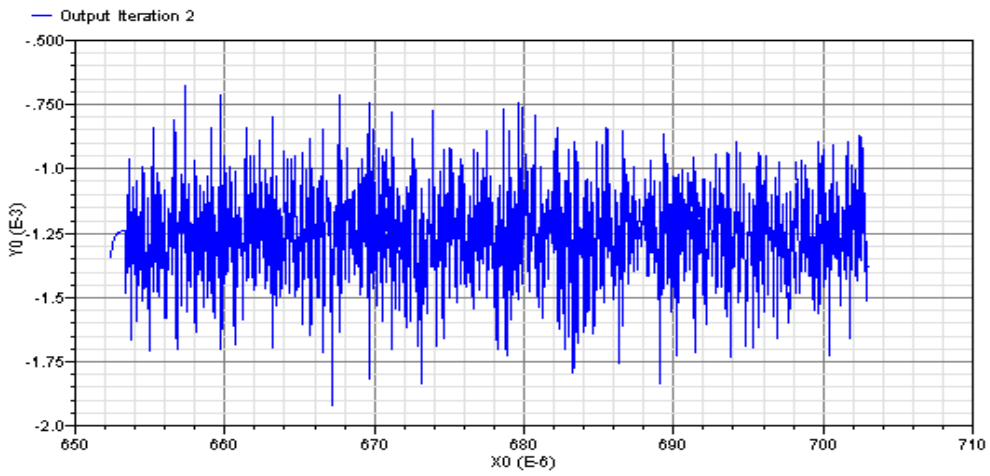

Figure 4.24: Iteration 2 for input referred V_{rms} noise at output stage

4.7 Measurement Results

The measurement results are taken from 4×4 P-on-N ROIC, which is designed and fabricated using AMS 0.35 µm 4 metal 2 poly CMOS process. In 4×4 ROIC, there are 4 channels, each of them giving output subsequently. In 4×4 P-on-N ROIC design, variable integration time, and adjustable gain settings properties are implemented, whereas serial/parallel interface is not implemented. The fully functional ROIC with all functionalities is 72×4 P-on-N ROIC.

For the measurement of 4×4 P-on-N ROIC a printed circuit board (PCB) is designed and fabricated, which is shown in Fig. 4.25. The desired input signals are given by a couple power supplies and function generator, and outputs are measured with the help of an oscilloscope. The fabricated 4×4 P-on-N ROIC chip is inserted into the CQFP socket.

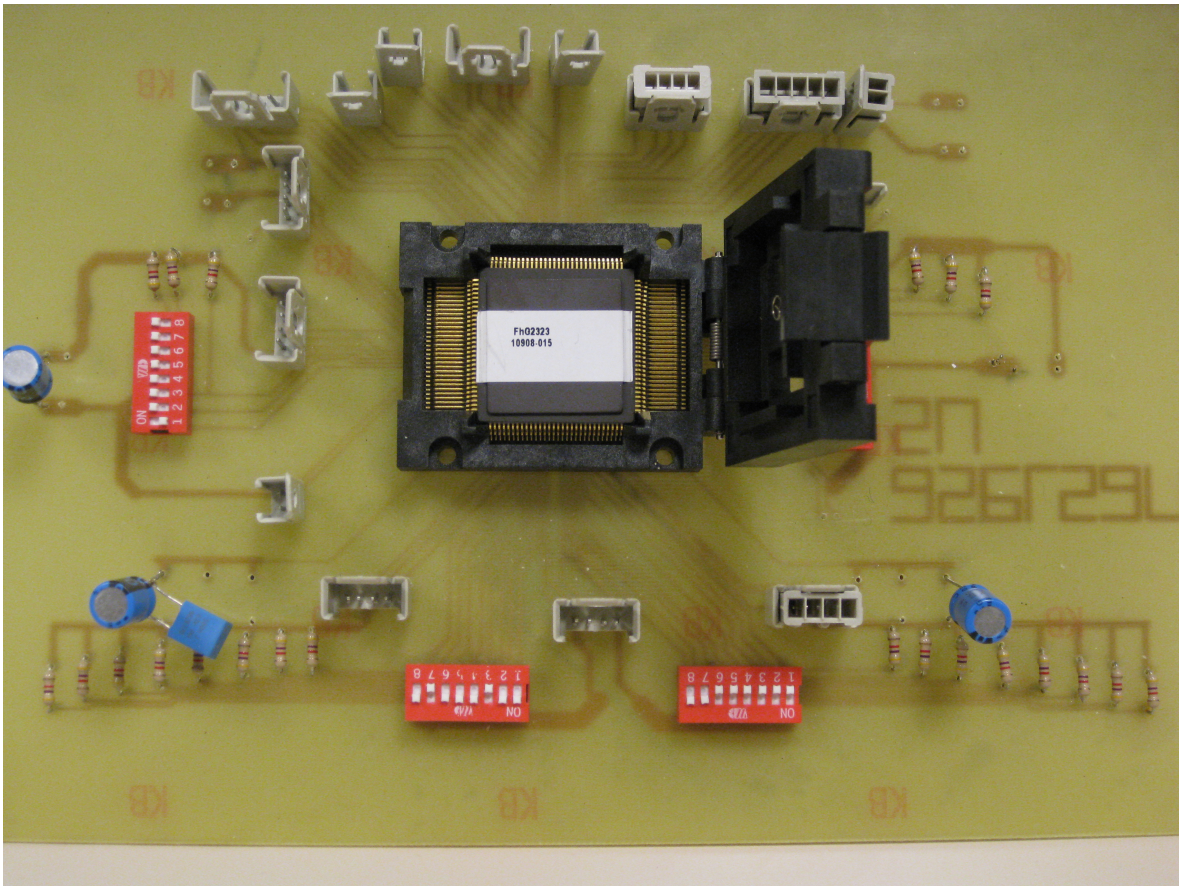

Figure 4.25: PCB for the measurement of 4×4 P-on-N ROIC

CQFP 120 package type is preferred for the 4×4 P-on-N ROIC because of the availability of more than 100 leads, which provides to take measurements from different locations of the chip. The 4×4 P-on-N ROIC within CQFP 120 package type is shown in Fig. 4.26.

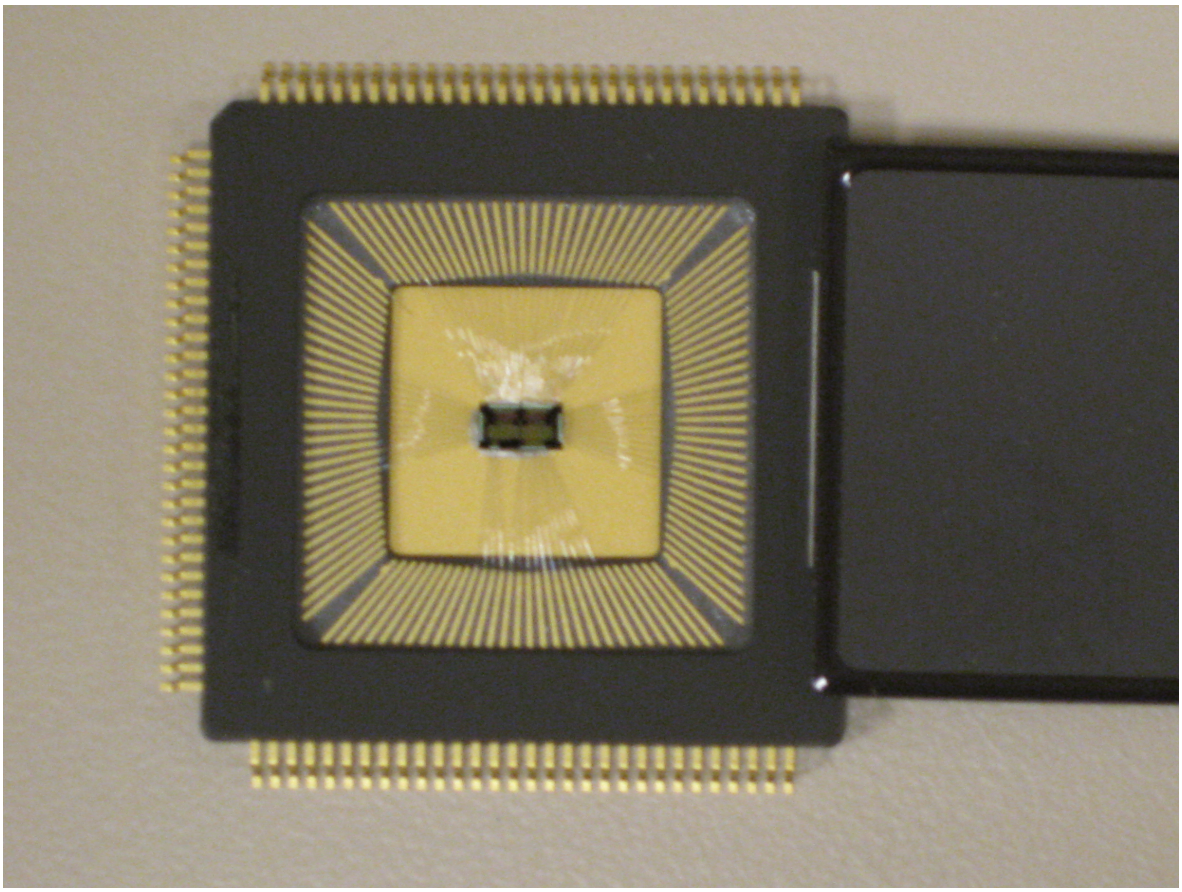

Figure 4.26: 4×4 P-on-N ROIC within CQFP 120 package type

Measurement results show that, 4×4 P-on-N ROIC linearly integrates with the changing integration time, and the digital circuit controlling the analog part of ROIC works properly. Fig. 4.25-4.28 show the voltage on the integration capacitor with 4 different integration times. All these measurement result are taken from detector 4.

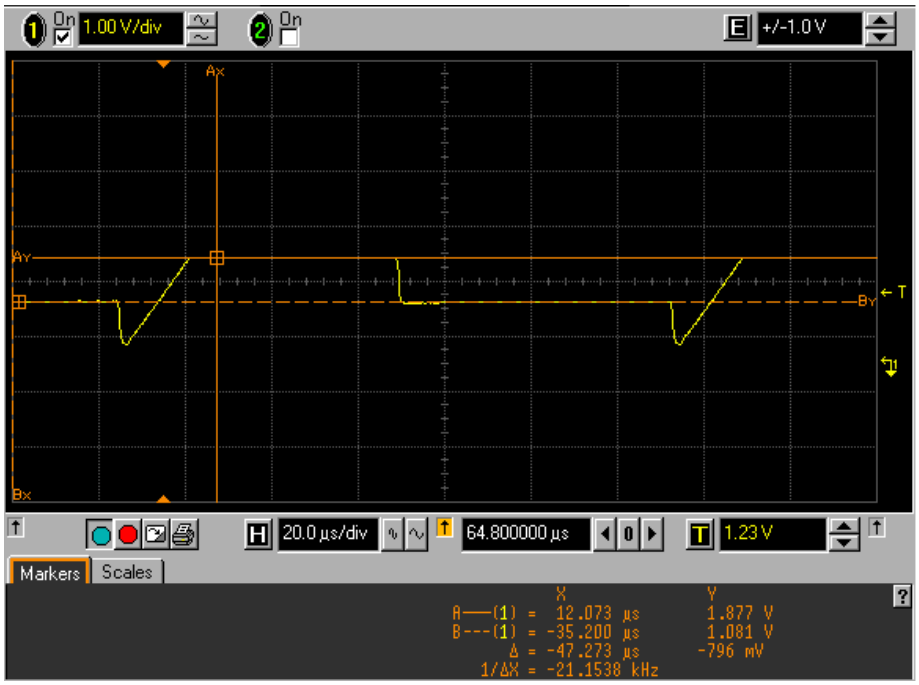

Figure 4.27: Voltage on integration capacitor with 16 µs integration time, gain setting 1.30

Voltage on the capacitor is measured to be 1.87 V for 16 µs integration time.

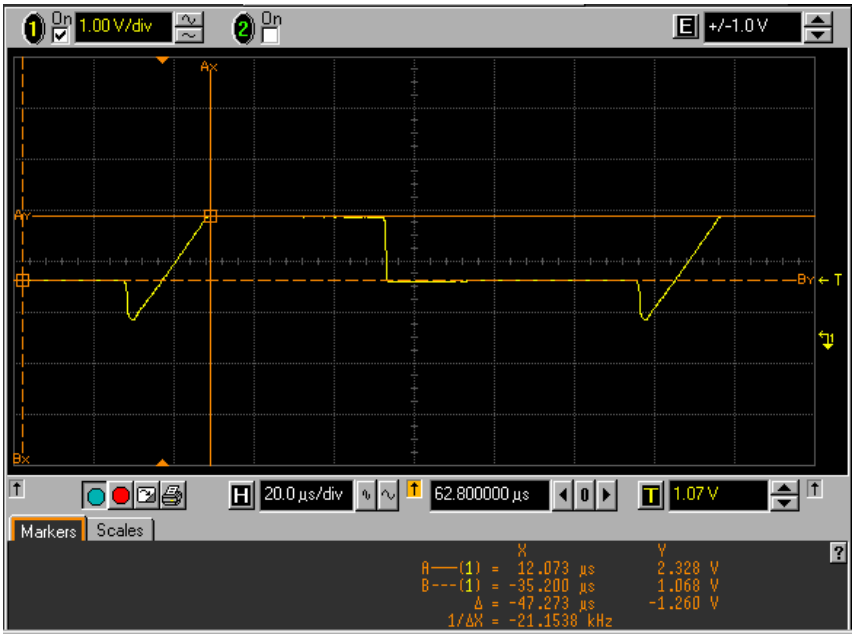

Figure 4.28: Voltage on integration capacitor with 20 µs integration time, gain setting 1.30

Voltage on the capacitor is measured to be 2.32 V for 20 µs integration time.

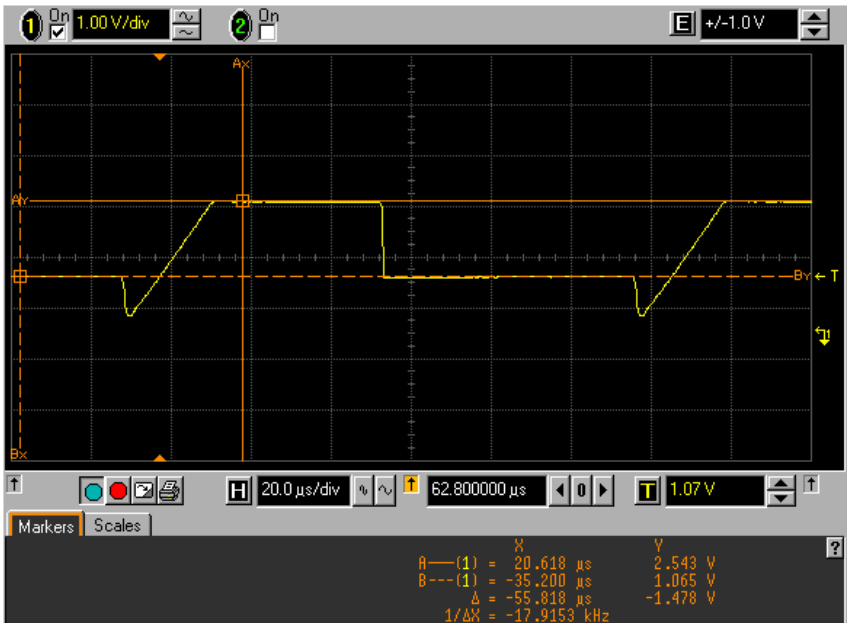

Figure 4.29: Voltage on integration capacitor with 22 µs integration time, gain setting 1.30

Voltage on the capacitor is measured to be 2.54 V for 22 µs integration time.

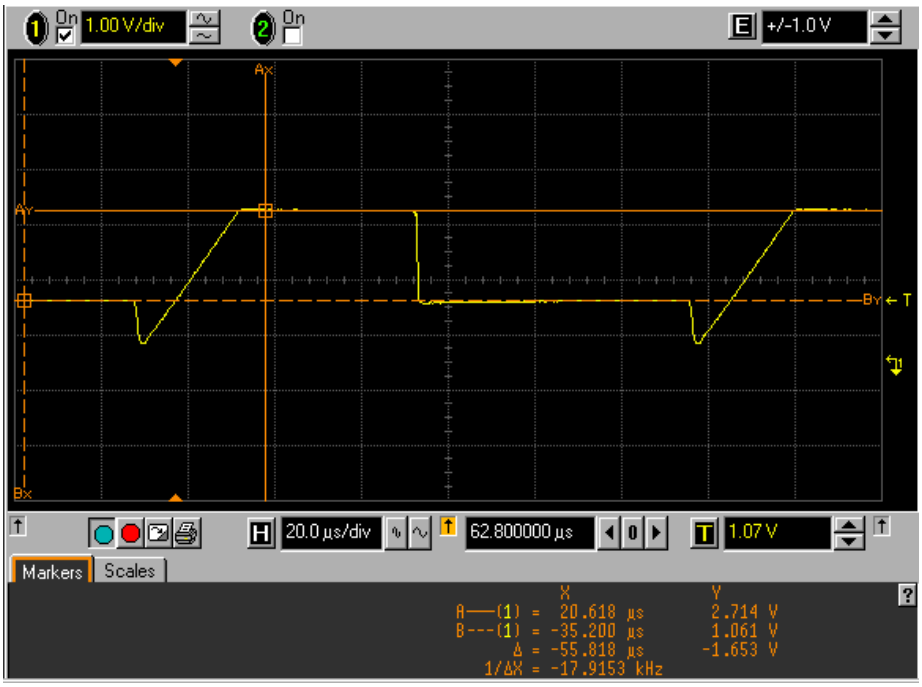

Figure 4.30: Voltage on integration capacitor with 23.75 µs integration time, gain setting 1.30

Voltage on the capacitor is measured to be 2.71 V for 23.75 µs integration time.

The following measurement results from Fig. 4.29 to 4.32 show the voltages on the integration capacitors of different detectors. Each detector is linearly integrating the voltage to the input capacitors, but the integrated voltage is different for all of them. This means that, there is no problem with the linear integration of charge to the capacitor blocks, but the problem is different amount of charge storage.

To investigate the reason of this difference, several simulations are done. It is observed that the metal paths carrying current from the detectors to the storage capacitors are too long, and their lengths are different for all detectors, which results in huge parasitic capacitance different between detectors. To solve this problem, the circuit topology of the unit cell is changed, and voltage is decided to be carried to the storage capacitors instead of current, because during current carrying current operation, a lot of charge is lost due to parasitic capacitance associated with long paths. Another solution to overcome this problem is to rearrange the channel architecture by changing capacitor places in such a way that, all detectors see more or less the same amount of parasitic capacitance. The 72×4 P-on-N ROIC is designed and implemented in this way, therefore this voltage difference at detectors is not expected for the 72×4 ROIC.

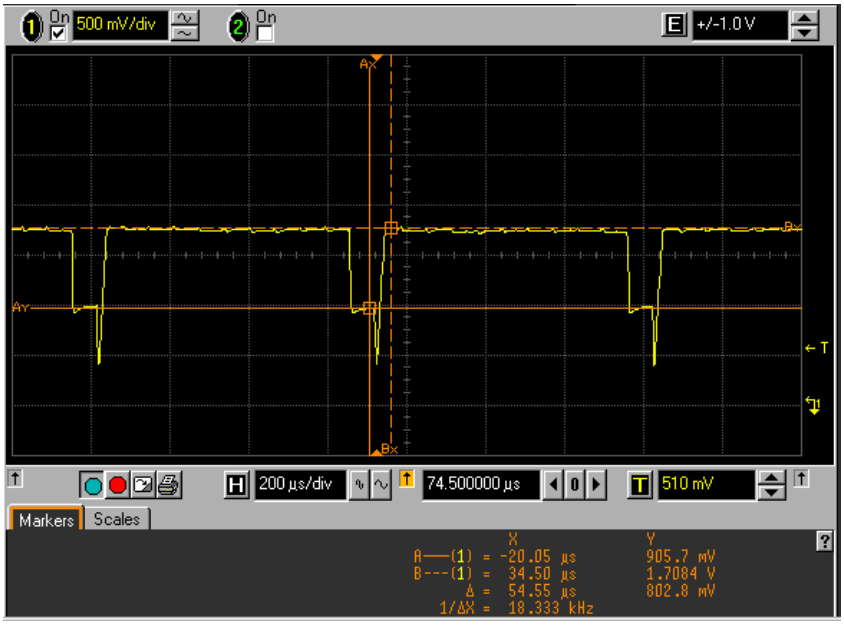

Figure 4.31: Detector 1 voltage with 24 µs integration time, gain setting 1.30

Detector 1 voltage is measured to be 905.7 mV for 24 µs integration time.

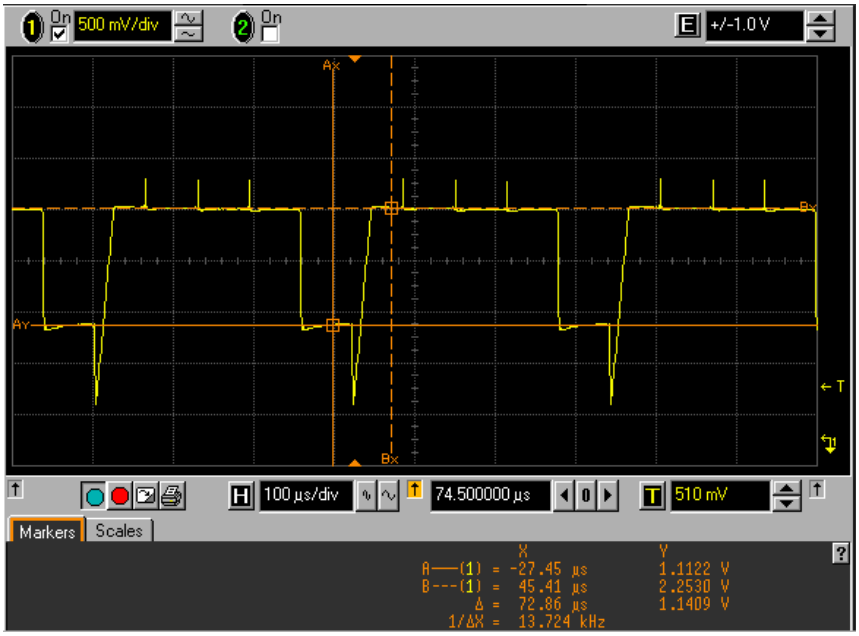

Figure 4.32: Detector 2 voltage with 24 µs integration time, gain setting 1.30

Detector 2 voltage is measured to be 2.253 V for 24 µs integration time.

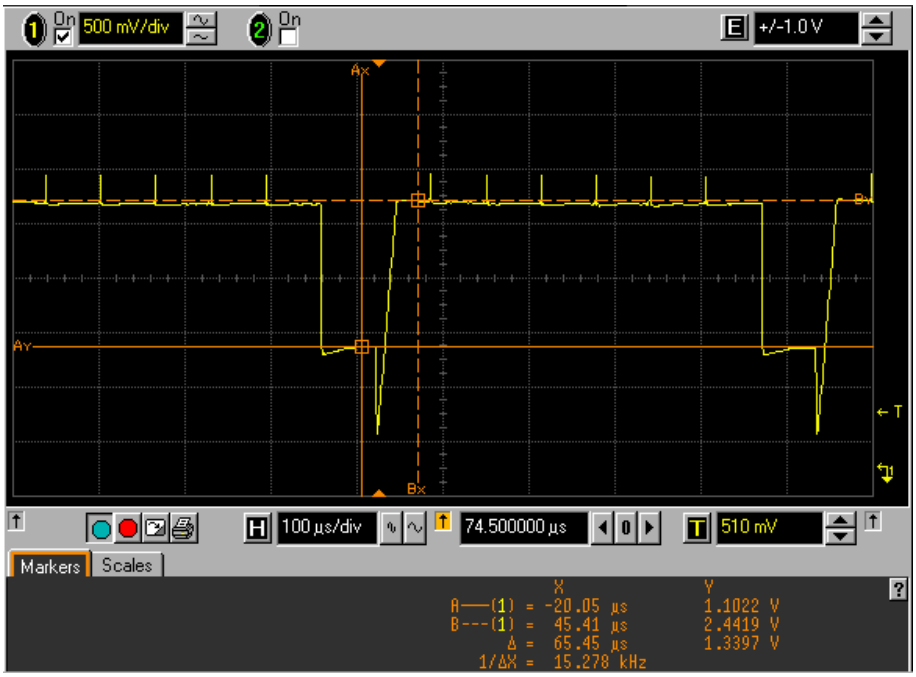

Figure 4.33: Detector 3 voltage with 24 µs integration time, gain setting 1.30

Detector 3 voltage is measured to be 2.441 V for 24 µs integration time.

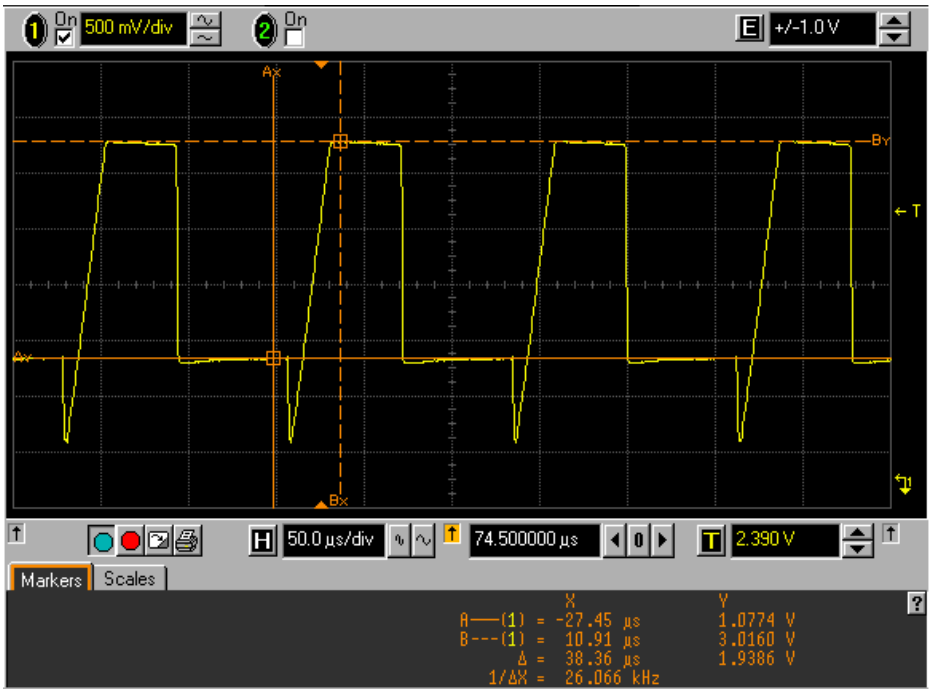

Figure 4.34: Detector 4 voltage with 24 µs integration time, gain setting 1.30

Detector 4 voltage is measured to be 3.016 V for 24 µs integration time.

5 CONCLUSIONS

In this thesis, a 72×4 ROIC for 72×4 P-on-N HgCdTe long wave infrared detector array is designed and implemented. In the first chapter, a general view about the infrared imaging systems, detectors, and ROICs is given. In the second chapter, building blocks of ROICs, which are input unit cell and time delay integration (TDI) stage, are introduced. Several unit cell architectures are compared in terms of their advantages and disadvantages, and two implementation methods of TDI algorithm is discussed. In the third chapter, a detailed description of ROIC implementation is given. Used ROIC architecture, channel architecture is first introduced. Implementation of unit cell and TDI stages are explained in detail. Offset cancellation/automatic gain adjustment stage, output buffer stage is explained and the amplifiers used in these stages are given. Digital control stage and serial/parallel interface stage are also explained in the third chapter. Finally in the fourth chapter, simulation results for 72×4 P-on-N ROIC and measurement results for 4×4 P-on-N ROIC

for the functionality and noise analysis of ROIC is given, and some comments about simulation and measurement results are provided.

As the input unit cell architecture, current mirroring integration (CMI) unit cell is chosen for its stable detector bias voltage, low input impedance, high linearity, and good dynamic range, that comes with the drawback of moderate noise performance. The main reason to select CMI unit cell architecture is the 1 MΩ detector resistance. For the high injection efficiency for that resistance value, CMI unit cell architecture provides very good results, together with very stable detector bias voltage.

In the TDI stage of the ROIC, single summation amplifier with multiple storage elements is used. The alternative TDI implementation is the multiple summation amplifiers with less storage elements. TDI over four elements with a supersampling rate of three is implemented. For this implementation, one TDI amplifier and 26 storage capacitors are used for single channel. 11 storage elements for the first detector, 8 storage elements for the second detector, 5 storage elements for the third detector, and 2 storage elements for the fourth detector are needed to implement that TDI method. These multiple storage elements are required to store the image data to be used in coming frames, because the same image comes to the fourth detector after 10 frames than it comes to the first detector. The TDI algorithm should add the contributions of four detector pixels for the same image, so that much storage elements are used for TDI over four elements with supersampling rate of three.

After the image data is stored in the corresponding storage elements, they are integrated in the TDI amplifier with the help of S1, S2, RESET, and INT control signals. INT signal controls the integration capacitor switch while RESET signal controls the reset switch of the TDI amplifier. S1 and S2 signals control the flow of charges from integration capacitors to TDI capacitor, and reading of these charges to the offset cancellation stage.

TDI stage suffers from the bottom plate capacitance effect and switching capacitors effect. The switching capacitors exhibit charge injection problem and clock feedthrough problem. In order to eliminate these effects an offset cancellation stage is needed. The offset cancellation stage is the copy of a channel producing the same offset error including the

parasitic capacitance and switching capacitor effects. This erroneous voltage is subtracted from the TDI voltage in the offset cancellation stage and sent to the output buffer stage. Automatic gain adjustment is also done in offset cancellation amplifier with switching resistors based on the information of pixel selection/deselection. If one or more of four detector pixels are malfunctioning, the resulting voltage of the amplifier is multiplied by 1.33 to compensate the dead pixels.

The output of the offset cancellation/automatic gain adjustment stage is sent to the output buffer stage. The output amplifier is designed and implemented based on the requirements of 10 pF output load with 1 MΩ resistance. The output amplifier should be settled in less than 100 ns with reasonable phase margin and slew rate. The slew rate of the output op-amp with the above mentioned output load is 65 V/µs.

A digital control circuit produces the controlling signals of analog building blocks, and a parallel/serial interface programs the digital control block. Digital control block and parallel/serial interface is written in Verilog HDL language, synthesized in Synopsys Design Compiler, and placed/routed with Silicon Ensemble to the AMS 0.35 µm CMOS CORELIB library to be used in the layout of ROIC. The digital synthesized part is operated with 3.3 V, while the analog part is operated with 5 V inputs. The reason for the digital part to be 3.3 V is that, 5V digital libraries of AMS are not available. The interface between the digital part and analog part is the level shifter block. Level shifter takes the 3.3 V signals from the digital part, and shifts the signal level to 5 V to drive analog part of the ROIC. The address and channel selection decoder are full custom designs operating with 5V signal level.

Functionalities of the 72×4 P-on-N ROIC is simulated and results are given. Measurement results of 4×4 P-on-N ROIC is also given. Data available from the measurement results are evaluated and 72×4 P-on-N ROIC is designed and implemented based on these data. Some problems encountered in 4×4 ROIC helped to change some parts of the ROIC, and problems observed in the measurement results are tried to be eliminated in 72×4 P-on-N ROIC. Simulation and measurement data show that ROIC functions properly.

The designed 72×4 P-on-N ROIC has the properties of bidirectional TDI scanning, variable integration time, adjustable gain settings, by-pass(test) mode, pixel selection/deselection, and automatic gain adjustment. It can be programmed through the parallel/serial interface. Parallel interface is the basic operation mode including all properties except pixel selection/deselection property. In serial mode, dead pixel information which is determined in by-pass mode is supplied to the ROIC, and ROIC utilizes this information to determine whether that line of the image uses automatic gain adjustment or not.

All requirements of the ROIC are met except the noise requirement. In the future design the noise performance can be improved with different unit cell architecture and lower resistor values in the offset cancellation amplifier. The success of the project led to the next project of 576×7 ROIC design, which uses TDI over seven elements with an optical supersampling rate of three.

REFERENCES

[1] D.A. Scribner, M.R. Kruer, J. M. Killiany, "Infrared Focal Plane Array Technology," *Proceedings of IEEE.* Vol. 79 No.1, pp 66-85, January 1991

[2] C.C. Hsieh, C.Y.Wu, F. W. Jih, T. P. Sun, "Focal Plane Arrays and CMOS Readout Techniques of Infrared Systems," *IEEE Transactions on Circuits and Systems for Video Technology,* Vol.7, No 4, pp. 594-605, 1997

[3] A. Rogalski, "Infrared Detectors: an Overview," *Infrared Physics & Technology 43*, pp.187-210, 2002

[4] A. Rogalski, "Infrared Detectors:Status and Trends," *Progress in Quantum Electronics 27*, pp.59-210, 2003

[5] Raytheon Infrared Operations "CRC 774 – 320x240 Readout Integrated Circuit, Users Guide and Operating Manual," 2001

[6] F. Pistone, P. Tribolet, M. Vuillermet, "High Resolution Staring Arrays Answering Compact MW and LW Applications," *SPIE Warshaw,* 2005

[7] J.L.Vampola "Readout Electronics for Infrared Sensors," *IR/EO Handbook,* pp. 285-342

[8] E. R. Fossum, B. Pain, "Infrared Readout Electronics for Space Science Sensors: State of the Art and Future Directions," *Proc. of SPIE* vol.2020, pp. 262-285,1993

[9] N. Yoon, B. Kim, H. C. Lee, C. K. Kim, "High Injection Readout Circuit for Low Resistance Infrared Detector," *Electronics Letters* Vol.35, No 18, 1999

[10] T. Akin, H. Kulah, "A Current Mirroring Integration Based Readout Circuit for High Performance Infrared FPA Applications" *IEEE Transactions on Circuits and Systems-II Analog and Digital Signal Processing* Vol.50, No 4, 2003

[11] A.Rogalski, K. Chrzanowski, "Infrared Devices and Techniques," *Optoelectronics Review 10(2),* pp.111-136, 2002

[12] B. Razavi, "Design of Analog CMOS Integrated Circuits," New York, 2001

[13] C. C. Enz, G. C. Temes, "Circuit Techniques for Reducing the Effects of Op-amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization," *Proceedings of IEEE* Vol84, No 11, 1996

[14] O. Oliaei, "Noise Analysis of Correlated Double Sampling SC-Integrators" *IEEE,* 2002

[15] G. Jun, L. Wengao, L. Jing, C. Wentao, T. Ju, C. Zhongjian, J. Lijiu, "Design of High Performance CMOS Linear Readout Integrated Circuit," *IEEE,* 2003

[16] E. Mottin, P. Pantigny "Device for Reading Detector Arrays with TDI Effect" *United States Patent*, Patent Number: 5828408, October 1998.

[17] A. Documentation, "1280C_SF, Preliminary Datasheet," AIM

[18] P. E. Allen, D. R. Holberg, "CMOS Analog Circuit Design," New York, Oxford, Oxford University Press, 2002

[19] H. Kayahan, A. Ergintav, Ö. Ceylan, Y. Gürbüz, A. Bozkurt, "Realization of a ROIC for 72x4 PV-IR detectors," *Proceedings of SPIE,* Vol. 6890, 2008

[20] F. F. Sizov, Y. P. Derkach, S. V. Korinets, V. P. Reva, "576x6 ROIC for MCT LWIR Arrays," *Proceedings of SPIE,* Vol. 5726, 2005