REALIZATION OF A VOLTAGE CONTROLLED OSCILLATOR USING 0.35 μm SiGe-BiCMOS TECHNOLOGY FOR MULTI-BAND APPLICATIONS

by

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Abstract

The stable growth in wireless communications market has engendered the interoperability of various standards in a single broadband frequency range from hundred MHz up to several GHz. This frequency range consists of various wireless applications such as GSM, Bluetooth and WLAN. Therefore, an agile wireless system needs smart RF front-ends for functioning properly in such a crowded spectrum. As a result, the demand for multi-standard RF transceivers which put various wireless and cordless phone standards together in one structure was increased. The demand for multi-standard RF transceivers gives a key role to reconfigurable wideband VCO operation with low-power and low-phase noise characteristics. Besides agility and intelligence, such a communication system (GSM, WLAN, Global Positioning Systems, etc.) required meeting the requirements of several standards in a cost-effective way. This, when cost and integration are the major concerns, leads to the exploitation of Si-based technologies.

In this thesis, an integrated 2.2-5.7GHz Multi-band differential LC VCO for Multi-standard Wireless Communication systems was designed utilizing 0.35µm SiGe BiCMOS technology. The topology, which combines the switching inductors and capacitors together in the same circuit, is a novel approach for wideband VCOs. Based on the post layout simulation

results, the VCO can be tuned using a DC voltage of 0 to 3.3V for 5 different frequency bands (2.27-2.51 GHz, 2.48-2.78GHz, 3.22-3.53GHz, 3.48-3.91GHz and 4.528-5.7GHz) with a maximum bandwidth of 1.36GHz and a minimum bandwidth of 300MHz. The designed and simulated VCO can generate a differential output power between 0.992 dBm and -6.087 dBm with an average power consumption of 44.21mW including the buffers. The average second and third harmonics level were obtained as -37.21 dBm and -47.6 dBm, respectively. The phase noise between -110.45 and -122.5 dBc/Hz, that was simulated at 1 MHz offset, can be obtained through the frequency of interest. Additionally, the figure of merit (FOM), that includes all important parameters such as the phase noise, the power consumption and the ratio of the operating frequency to the offset frequency, is between -176.48 and -181.16 and comparable or better than the ones with the other current VCOs. The main advantage of this study in comparison with the other VCOs, is covering 5 frequency bands starting from 2.27 up to 5.76 GHz without FOM and area abandonment.

0.35 µm SiGe-BiCMOS TEKNOLOJİSİ KULLANILARAK ÇOKLU BAND UYGULAMALARI İÇİN GERİLİM KONTROLLÜ OSİLATÖR DEVRESİNİN GERÇEKLENMESİ

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Anahtar Kelimeler: Gerilim kontrollü osilatör (VCO), çok bandlı ve çok standardlı alıcı vericiler, faz gürültüsü, geniş band gerilim kontrollü osilatör

Özet

Kablosuz iletişim piyasasındaki büyüme, 100 MHz'lerden GHz'lere kadar uzanan geniş frekans bandında çalışan standardlarıda beraberinde getirdi. Bu frekans bandındaki uygulamalardan bazıları; GSM, Bluetooth ve WLAN'dır. Kablosuz sistemlerin böylesine karmaşık spektrumlarda çalışabilmesi için akıllı RF devrelerine ihtiyaç vardır. Bunun sonucu olarak birçok standartta çalışabilen ve bunları tek yapıda toplamış radyo frekansında devrelere ihtiyaç artmıştır. En çekici rf bloklarından biri olan dar bandlı osilatör devreleri yerini çok bandlı devrelere bırakmıştır. Çok standartlı alıcı verici devreleri düşük güç tüketimli, düşük faz gürültülü ve yapılandırılabilir osilatörlere kritik bir rol vermiştir. Bunun yanı sıra sistemin maliyet açısından da efektif olması gerekmektedir. Maliyet ve entegrasyon söz konusu olduğunda Silikon tabanlı teknolojiler ön plana çıkmaktadır. Heterojen bipolar transistörlerin (HBT), CMOS ve pasif elemanların entegrasyonundaki rahatlık da bu teknolojinin avantajlarındandır.

Bu tezde, 2,2-5,7 GHz frekans aralığında çalışabilen çok kanallı diferansiyel LC gerilim kontrollü osilatör devresi (0.35 µm SiGe-BiCMOS teknolojisi kullanılarak) tasarlanmıştır. Aynı topoloji içerisinde endüktans ve kapasitans anahtarlama, geniş bandlı osilatör devrelerinde yeni bir yaklaşımdır. Devrenin serim sonrası sonuçlarında, beş farklı frekans band aralığında (2.27-2.51 GHz, 2.48-2.78GHz, 3.22-3.53GHz, 3.48-3.91GHz ve 4.528-

5.7GHz) maksimum 1.36 GHz ve minimum 300MHz band genişliğinde çalıştığı gözlemlenmiştir. Devre, 0.992 dBm ve -6.087 dBm arasında değişen diferansiyel çıkış gücüne sahiptir. Ayrıca, buffer katı da dahil olmak üzere ortalama 44.21 mW güç tüketimi vardır. Faz gürültüsü değerleri 1 MHz offset frekansında, seçilen frekans bandına göre -110.45 den -122.5 dBc/Hz ’e kadar değişmektedir. Bunun yanında osilatör için en önemli parametreleri içinde bulunduran figure of merit (FOM), kıyaslanan osilatörlerle hemen hemen aynı veya daha iyi bulunmuştur. Bu çalışmayı öne çıkaran en önemli faktör alan ve FOM ‘den taviz vermeksizin beş farklı frekans bandında çalışabilen bir yapı olmasıdır.

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My thesis is fully devoted to my mother...

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CHAPTER 1 INTRODUCTION

1.1 The briefing on the Wireless LAN Standards

The fastest growing segment of the semiconductor industry has been the wireless communication market in the recent years. For the indoor access, wireless local area networks (WLANs) have been introduced as a set of standards to provide a simple and flexible way for people plugging into a network. IEEE 802.11 is a set of standards for wireless local area network (WLAN) computer communication, developed by the IEEE LAN/MAN Standards Committee (IEEE 802) in the 5 GHz and 2.4 GHz public spectrum bands. Furthermore, IEEE developed a new standard called Wireless Metropolitan area networks (WMANs) for urban area coverage wireless access [1]. IEEE 802.16 WMANs standard uses frequency band from 2 to 11 GHz. The following sections include brief information about IEEE frequency bands which are widely used in wireless communication.

1.1.1 IEEE 802.11a

IEEE 802.11a devices and many wireless devices use Unlicensed National Information Infrastructure (U-NII) band which operates around 5 GHz. In comparison with 802.11b, it employs a different multiplexing technique: orthogonal frequency division multiplexing (OFDM). The OFDM system uses parallel subcarriers to transmit and receive a single data stream [2,4]. In 802.11a [4], each channel contains 52 sub-carriers as 48 data carriers and 4 pilot carriers.

U-NII band includes three subbands: U-NII lower sub-band, from 5.15 GHz to 5.25 GHz; U-NII middle sub-band, from 5.25 to 5.35 GHz; and U-NII upper band, from 5.725 to 5.825 GHz. The lower and middle U-NII sub-bands accommodate eight channels in a single band with a total bandwidth of 200 MHz. The upper U-NII band accommodates four channels in a 100-MHz bandwidth. The channel frequency spacing is 20 MHz and the occupied channel bandwidth is 16.6 MHz. The U-NII bands with channel locations are shown in Figure 1.

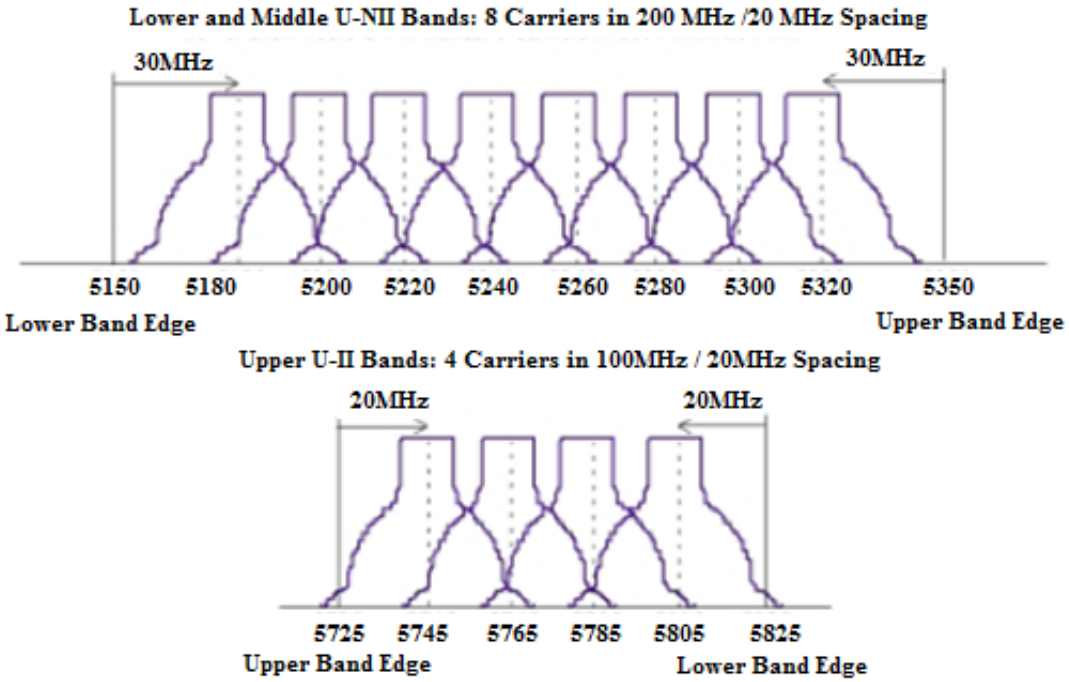

Figure 1 802.11a OFDM system channel frequency locations[4]

1.1.2 IEEE 802.11b

In USA (FCC) and Europe (ETSI), the operating frequency band for 802.11b is in the range of 2.4–2.4835 GHz. Additionally, it is allocated by the regulative authority of Japan as 2.471–2.497 GHz. For high data rate channels in the USA, three channels centered at 2412, 2437 and 2462 MHz have been allocated. The channel spacing is 25 MHz and null-to-null bandwidth is 22 MHz. France allows in the range of 2.4465–2.4835 GHz, and also this operation is allowed in the range of 2.445–2.475 GHz band in Spain. The frequency channel plan of IEEE 802.11b for each country is indicated in Table 1[3].

CHNL_ID	**Frequency** *(MHz)*	**X'10'** *FCC*	**X'20'** *IC*	**X'30'** *ETSI*	**X'31'** *Spain*	**X'32'** *France*	**X'40'** *MKK*
1	*2412*	*x*	*x*	*x*	-	-	-
2	*2417*	*x*	*x*	*x*	-	-	-
3	*2422*	*x*	*x*	*x*	-	-	-
4	*2427*	*x*	*x*	*x*	-	-	-
5	*2432*	*x*	*x*	*x*	-	-	-
6	*2437*	*x*	*x*	*x*	-	-	-
7	*2442*	*x*	*x*	*x*	-	-	-
8	*2447*	*x*	*x*	*x*	-	-	-
9	*2452*	*x*	*x*	*x*	-	-	-
10	*2457*	*x*	*x*	*x*	*x*	*x*	-
11	*2462*	*x*	*x*	*x*	*x*	*x*	-
12	*2467*	-	-	*x*	-	*x*	-
13	*2472*	-	-	*x*	-	*x*	-
14	*2477*	-	-	-	-	-	*x*

Table 1 Frequency channel plan for IEEE 802.11b

1.1.3 IEEE 802.11g

IEEE 802.11g is the 802.11a standard which operates in the 802.11b band (2.4 GHz Industrial, Scientific and Medical band). IEEE 802.11a OFDM system has a higher maximum data rate (54 Mbit/s) than 802.11b (11 Mbit/s). However, 802.11a has higher free space path loss than 802.11b, because its operation frequency is higher than IEEE 802.11b. This means that 802.11a has a shorter range compared to 802.11b for the same transmitted power. The 802.11g standard was designed for supporting high data rate and a larger range at the same transmitted power.

1.1.4 IEEE 802.11n

IEEE 802.11n is an amendment version of previous wireless local area network standards such as IEEE 802.11b and IEEE 802.11g. IEEE 802.11n was developed by adding Multiple Input and Multiple Output (MIMO) system and 40 MHz operation to the physical layer (PHY). MIMO uses multiple receiver and transceiver system to improve the system performance. In order to support higher data rates, 802.11n provides wider bandwidth (40MHz) than the previous 802.11 operation.

1.1.5 HIPERLAN/2

For countries outside of the USA, the wireless LAN may or may not be compatible with the 802.11 standards. But it is worthwhile to briefly introduce another important wireless LAN standard: high performance local area network type 2 (HIPERLAN/2) standards. HIPERLAN/2 is used in Europe and its territories, and defined by the European Telecommunication Standards Institute (ETSI). HIPERLAN/2 is very similar to the IEEE 802.11a standard expect its operation frequency range [4]. HIPERLAN/2 operates in two sub-bands 5.15-5.35 GHz, and 5.47-5.725 GHz. The OFDM system in HIPERLAN/2 is almost similar to 802.11a.

1.1.6 IEEE 802.16

In order to give wireless access to the urban areas, IEEE 802.16a wireless Metropolitan Area networks(WMANs) standard was introduced firstly on 1 April 2003 [2]. This system utilizes frequencies from 2 to 11 GHz. There are licensed and un-licensed bands in the wide frequency band. The licensed bands are 2.3 GHz (WCS), between 2.5 to 2.7 GHz (MMDS), between 3.5 to 3.7 GHz (ETSI), and unlicensed bands are 2.4 GHz (ISM) and 5.8 GHz (U-NII) in which WLANs operates as well [4-5]. As a result, multi-band multi-standard transceiver architecture should have five different frequency bands in a wide range as represented in Figure 2.

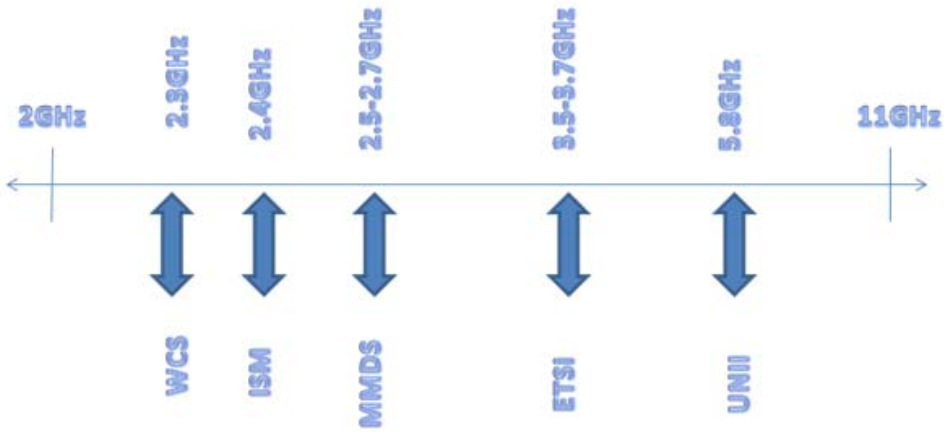

Figure 2 Operation frequencies for wireless communication

1.2 Communication Transceivers

Figure 3 shows the diagram of the major sub-circuit blocks of a typical super heterodyne communication transceiver. The sub-block are commonly the same for all transceivers.

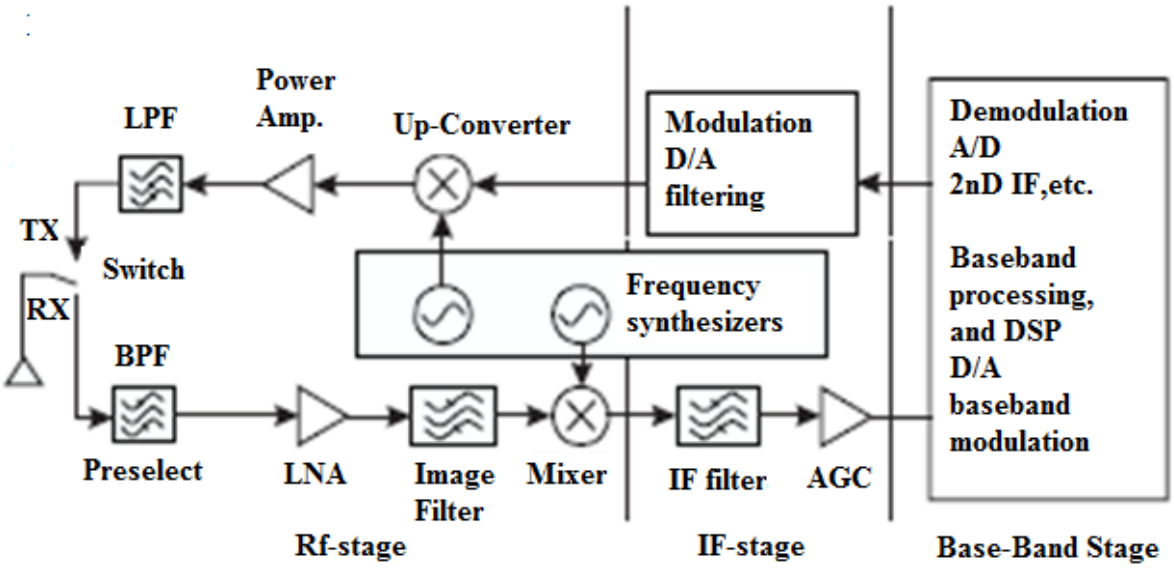

Figure 3 Typical super heterodyne communication transceiver [6]

The antenna connects both the transmit side and the receive side. Depending on the communication state the antenna transmits or receives a signal through antenna switch or

duplexer. At the receiver part, firstly the input pre-selection filter takes the broad spectrum of signals coming from the antenna and removes the signals that are not in the band of interest. This process prevents overloading of the low-noise amplifier(LNA). The main goal of LNA is amplifying the input signal without adding much noise. This process should be performed firstly, because the input signal that comes to the antenna at lower power has to be amplified without a distortion. Thus, any noise added after this stage becomes less of concern for the system. The signals that are at the same distance at the above and below of the LO produce an output at the same frequency. The frequency that we do not want to receive is called the image. We can write the relations for the frequencies as $f_{rf} = f_{lo} - f_a$ and $f_i = f_{lo} + f_a$. Where are f_i the image problem frequency and f_a the desired frequency. This means that there will be a problem if we have a station at RF frequency and at the image. This problem is called as image problem. The image reject filter selects only the RF frequency for removing the image as shown in Figure 4.

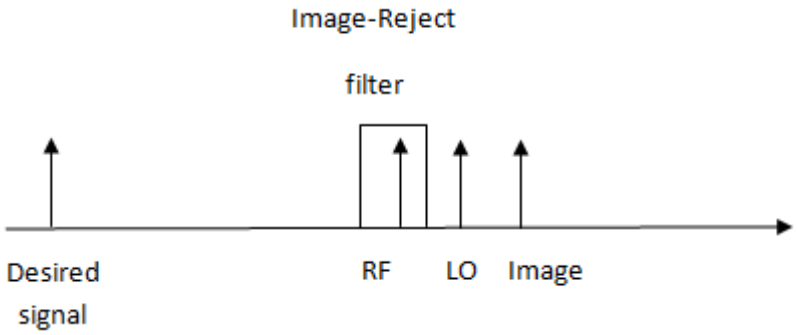

Figure 4 Removal of the image

The output of the mixer is the addition and subtraction of the RF and LO frequencies. The addition is filtering by using intermediate frequency filter. Thus, after the IF filter, the RF signal is translated down to the IF frequency. The other input of the mixer is coming from a voltage-controlled oscillator located inside a frequency synthesizer.

There may be many different channels or frequency bands at the input of the radio. Therefore, the local oscillator should have a controlled block to get the same intermediate frequency. Before the signal passes on to the back end of the receiver, the automatic gain control (AGC)

stage has to bring the signal to a specific amplitude level. After that operation, the signal will be digitalized through the use of an analog-to-digital converter.

The aforementioned receiving process could be seen as a reverse function of transmitter part. The back-end digital signal is used to modulate the carrier in the IF stage. A mixer converts the modulated signal and IF carrier up to the desired RF frequency. As in receiver part, the other input for the mixer comes from the local oscillator. A power amplifier must be used to increase the signal power, because the RF carrier and associated modulated data have to be transmitted over large distances through the loss media. Depending on the application, the power should be increased from the milliwatt range to a level in the range of hundreds of milliwatts. In order to avoid transmission of the unwanted frequencies after the PA operation, a low pass filter sould be used for removing any possible harmonics.

1.3 Thesis Overview

Chapter II start with application areas of Voltage Controlled Oscillators. Additionally, specific performance parameters such as phase noise, power consumption, operation frequencies, stability and output power were described. At the end of the chapter, VCO topologies were introduced with a brief comparison.

The topology and design procedure that were used in this design have been described in Chapter III. The core part of the VCO, LC tank, was defined through the detailed investigations of the of tank inductances, the tank capacitances, the switching method and the varactors. Moreover, the other parts of VCO like $G_{m,\ buffer}$, fine tuning, bias and switched circuits were presented. Following the small signal model of whole design, layout issues, post-layout simulation and measurement results were presented.

Finally, the performance and novel characteristics of the multi-band voltage controlled oscillator were covered in Chapter IV. This section also includes the future work for developing the performance of the multi-band VCO.

CHAPTER 2 OSCILLATORS IN TRANSCEIVERS

In communication systems, the oscillators are utilized for providing the clock signals in digital circuits and frequency conversion in analog circuits. The oscillators are called as Local oscillators when used for frequency conversion. In this thesis, the voltage controlled oscillator was designed as a local oscillator in a radio transceiver.

The proceeding sections include a literature survey about typical frequency operation, performance parameters and topology types of local oscillators. Finally, as a result of the literature survey, the appropriate topology and technology was chosen for the multi-band operation.

2.1 Frequency operations by using Oscillators

The typical application of LO (with a mixer) in the front-end of a typical receiver is downconverting the incoming radio frequency (RF) signal to a lower, intermediate frequency (IF).

Another usual implementation of LO is PLL (Phase Locked Loop). A typical PLL is composed of a reference frequency oscillator, voltage-controlled oscillator (VCO), a loop filter, a phase detector, and a frequency divider, as shown in Figure 5.

A PLL forces the output frequency to become exactly equal to the input frequency. In order to provide a stable high frequency signal, the reference signal is compared with the divided version of the VCO output. If the divider has value N, then the output frequency will be N times of the input frequency. Furthermore, if the divider value is adjustable, we can generate different LO frequencies by simply changing N. If phase comparator detects a difference between these signals, the following circuits operate for removing the difference. A fixed, low-frequency (~10 MHz) reference oscillator can be used to generate multiple LO frequencies in the low-GHz range. Typically, a crystal oscillator is utilized as the reference oscillator due to its high stability.

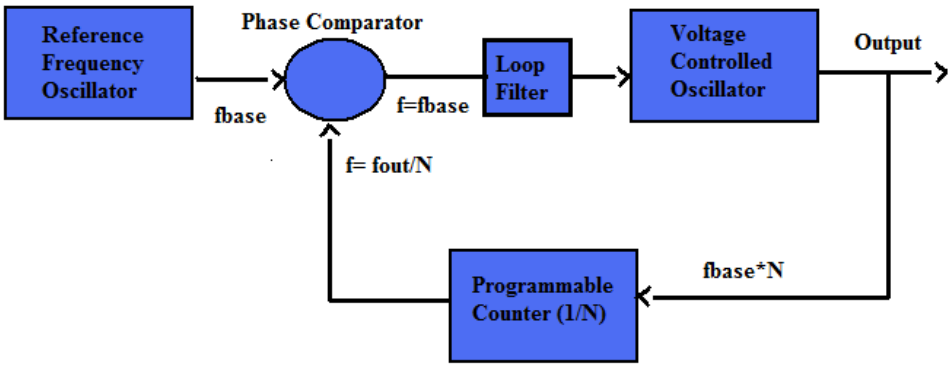

Figure 5 Phase-Locked Loop

The output contains noise characteristics of the reference signal, the phase detector, the loop filter, the divider, and the VCO. Out of the loop bandwidth, the output only contains the noise characteristics of the VCO. Therefore, the spectral purity of the VCO affects the phase noise performance of the PLL.

2.2 Performance Parameters

The spectral purity, which is usually characterized by phase noise, is the most critical specification when designing a VCO. In many wireless transceivers, the design goal is the minimum power consumption. However, there is a trade-off between power consumption and phase noise. The other specifications are the operating frequency, the stability, the output power. In this section, the affects of each parameter on the oscillation performance were explained.

2.2.1 Phase Noise

The most important charateristic of an oscillator is its phase noise. The spectral purity is a measurement of the power distribution around the center frequency and its harmonics. Ideally, the spectrum of an oscillator is an impulse located at the desired frequency. However, all practical oscillators have im-perfect spectral purities and so they develop skirts as shown in Figure 6. This is an undesirable power distribution around the oscillation frequency and the harmonics are known as the *phase noise*.

In order to understand the negative effect of phase noise, consider the receiver's front-end. The desired signal is shown in the presence of a stronger signal in an adjacent channel in Figure 7. As shown in the figure, the phase noise of the VCO is modulated onto the stronger signal at IF. This phenomenon reduces the signal-to-noise ratio (SNR) of the desired signal at IF and limits the proximity of the placement of the channels [7]. Similarly, in a transmitter, LO phase noise is modulated onto the desired signal, resulting in unwanted energy being transmitted outside of the desired band.

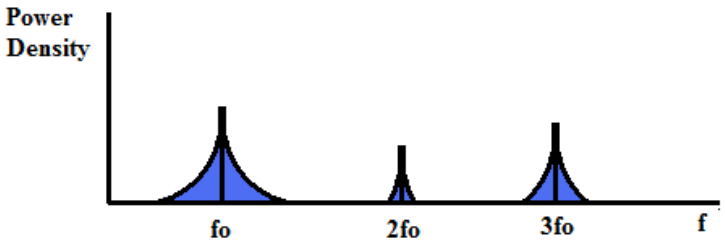

Figure 6 Spectrum of a typical oscillator

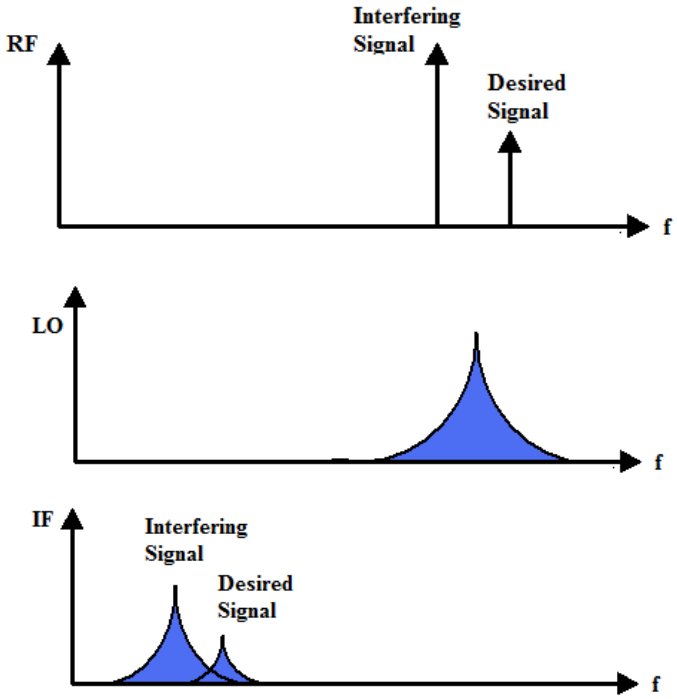

Figure 7 SNR degradation

2.2.2 Power Consumption

An arbitrarily small phase noise can be achieved by simply increasing the bias current, but there are practical limitations such the possible smallest phase noise achievement. Increasing

the bias current means much more amplification in gm stage and it also means rise at the VCO's output voltage amplitude. However, any MOS transistor has a maximum voltage that may not be exceeded without permanent damage. Also, in usual applications the n-well in a PMOS device is connected to the power supply. The drain cannot exceed the power supply voltage by more than about 0.6 V because the drain-well diode will be turned on resulting in clipping of the output voltage. As a result, the bias current directly depends on the process. Also, we would like to minimize current consumption of the VCO as much as possible (considering the phase noise trade-off) to maximize battery life of transceiver.

2.2.3 Operating Frequency

The operating frequency is the major issue for Voltage Controlled Oscillator. In section I, the wireless communication standards were given in terms of the frequency band aspects. If VCO is used for a multi-standard application, output oscillation must satisfy all frequency bands that are standardized by the multi-band transceiver block.

A multi-band multi-standard RF frontend for IEEE 802.6a and IEEE 802.11 a/b/g applications have been designed [8]. This design could be a reference for the frequencies cover in VCO in a multi-band RF transceiver. For IEEE 802.11 b/g, and WCS and MMDS bands of 802.16a that share nearly same frequency bands aroud 2.4 GHz, the first local oscillator was located between 3.45 to 4.05 GHz. Moreover, IEEE 802.11b and UNII band of IEEE 802.16a was covered by providing 3.85-4.37 frequency band from VCO.

Another example could be given from a multi-band dual-conversion zero IF Receiver that was designed for IEEE 802.11a/b/g standards. The bands required to be covered are 2.4-2.5 GHz, 5.15-5.35 GHz and 5.725-5.825 GHz. For this operation the frequency plan of the multi-band WLAN receiver is presented in Table 2 [9].

Band (GHz)	LO (GHz)	IF(MHz)	Image (GHz)
2.4 – 2.5	2.9	400 – 500	3.3 – 3.4
5.15 – 5.35	4.8	350 – 550	4.25 – 4.45
5.725 – 5.825	5.275	450 – 550	4.725– 4.825

Table 2 The frequency plan of multi-band WLAN receiver

2.2.4 Stability

The stability is another performance parameter that affects the peripheral circuitry of the oscillator. In a transceiver block, if we have unstable frequency, we cannot get the desired RF or IF signal at the output of the mixer. From the PLL perspective, a stable and fixed signal at the output will not be guaranteed at the presence of an unstable VCO.

2.2.5 Output power

In typical applications, oscillators always drive circuits such as mixer in transceiver and divider in PLL. So, the output power becomes an important parameter when designing the whole circuit.

2.3 Topology and Technology

The main concern while choosing RF technologies for wide ranging communication applications is optimization for performance and or cost. This leads to the exploitation of Si-based technologies when cost and integration are the major concerns. The convenience of integration of high performance HBTs with the state-of –art CMOS and passive elements is the main advantage of SiGe BiCMOS technology against the other technologies [10].

As a consequence of second and third generation wireless systems, the multi-band and multi-standard mobile communication systems are required. The recent transceiver components must also cover the frequency band of various systems. With the introduction of the Ultra Wide Band (UWB), the communication standards operate in the frequency ranges up to 10 GHz. As a result, the demand for multi-standard RF transceivers which put various wireless and cordless phone standards together in one single structure is increased. So, the narrowband voltage controlled oscillators, which are one of the most attractive blocks among the RF building blocks, were replaced with single low noise wideband VCO. The demand for multi-standard RF transceivers imposes a key role to reconfigurable wideband VCO operation with low-power and low-phase noise characteristics [11-13].

The Voltage Controlled Oscillators (VCOs) are one of the essential building blocks of modern RF transceiver architectures. The LC-tank VCO topology is the most popular implementation

among others due to its higher spectral purity which is mentioned in section 3.2.1 in details. Below, various types of oscillators and a comparison between their performances will be presented.

2.3.1 Ring Oscillator

Basically, the odd number of the cascaded invertors in a feedback loop constructs a ring oscillator. The oscillation frequency is $f_{osc} = \frac{1}{2T_d M}$ which is related to the delay and number of each stage (T_d is the delay of each stage and M is the number of stages).

Figure 8 shows a three-stage differential ring oscillator. The ring oscillators are not faster and also cover lesser area relative to the other types of oscillators. However, the main disadvantages of ring oscillators are the lower operating frequency, poor spectral purity (Low pass behavior due to lacking inductors) and higher power consumption.

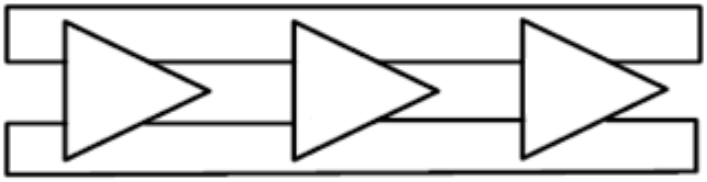

Figure 8 Ring Oscillator

2.3.2 Relaxation Oscillator

The relaxation oscillators, presented in Figure 9 are resonatorless oscillators. The ring oscillators could be given as the example of relaxation oscillators. In the topology, the positive feedback transistors (M1 and M2) enable the oscillation in this topology.

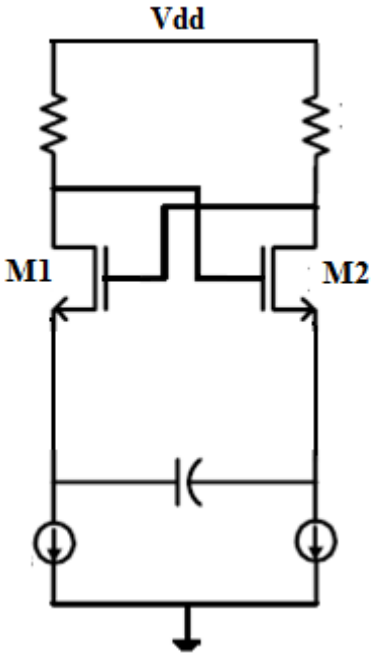

Figure 9 Relaxation Oscillator

The major advantage of the resonatorless oscillators is lack of large passive devices such as inductors and capacitors. This advantage makes relaxation oscillators small-sized and suitable for integration. However, the lacking of passive devices will cause no filtering of noise at the output signal. So, resonatorless circuits will suffer from phase noise performance, and this topology is not suitable for our application.

2.3.3 LC Oscillators

In order to get a better phase noise, the resonators have been added to the feedback network. A very simple resonator is an LC tank. The oscillator that is shown in Figure 10 resonates at frequency $\omega_c = \frac{1}{\sqrt{LC}}$.

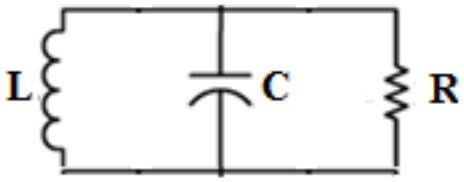

Figure 10 Parallel LC resonator

In theory, the impedances of the inductor and capacitor are equal with opposite signs at resonance frequency. The formula of the ideal circuit is $\left|\frac{1}{j\omega_c C}\right| = |j\omega_c L|$, which makes the impedance of the tank equal to infinite at this frequency. However in practice both the inductor and capacitor suffer from resistive components. Additionally, Q_c and Q_L are the quality factors of capacitor and inductor, and they are defined as $\frac{1}{\omega R_S C}$ and $\frac{\omega L}{R_S}$. Generally, the quality factors of the capacitors are much higher than the quality factors of the inductors [7]. Thus, the resulting parallel resistance of the tank, R_P, is mainly determined by the inductor ($R_P \approx R_{PL}$).

According to the model in Figure 11, the impedance of the circuit could be given as the paralleled impedance of the inductor, capacitor and resistor. At resonance, impedance of the inductance and capacitance are equal and the voltage gain equals $+g_m R_P$. It should be noted that Barkhausen's criteria [7] has to be fulfilled to start the oscillation.

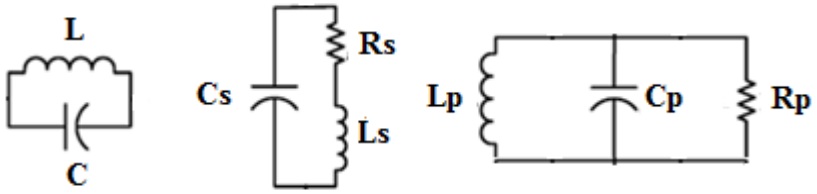

Figure 11 Impedance of the Tank

$$L_p \approx L_s \qquad C_p \approx C_s$$
$$R_{pL} \approx Q_L^2 . R_{sL} \qquad R_{pC} \approx Q_C^2 . R_{sC}$$
$$For\ Q_L \gg 1 \qquad For\ Q_C \gg 1$$

Topology Types

There are different approaches in designing an LC oscillator. The most common methods are Colpitts oscillator, Hartley oscillator, and Cross-Coupled oscillator. Colpitts and Hartley, shown in Figure 12, use one transistor to provide sufficient gain and phase shift. The frequency of oscillation in both topologies is $\omega_C = \frac{1}{\sqrt{L_{eq} C_{eq}}}$.

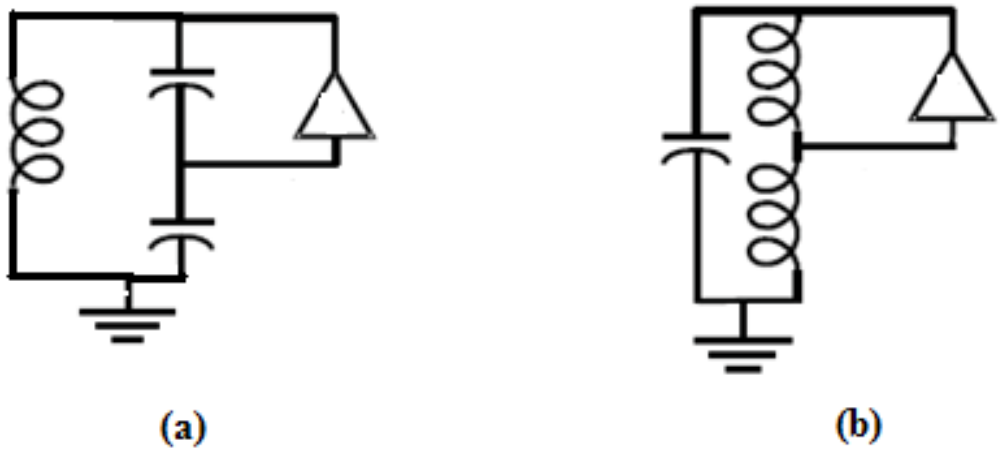

Figure 12 (a) Colpitts and (b) Hartley Oscillators

The Colpitts oscillator is known by its using a tapped capacitor and amplifier to form the feedback. Apart from Colpitts, the Hartley oscillator uses tapped inductor to form the loop. Because of using only one inductor, the Colpitts oscillator is smaller and more suitable for integrated circuits than the Hartley oscillators. The gain equation for colpitts oscillator is driven from small signal analysis;

$$g_m R_P = \frac{(C_1+C_2)^2}{C_1 C_2} \quad (1)$$

where g_m is the gain of the amplifier (generally MOSFET transistor) and R_P is loss of the LC tank. The minimum required gain occurs when $\frac{C_1}{C_2} = 1$, resulting the following expression to fulfill the Barkhausen's criteria;

$$g_m R_P \geq 4 \quad (2)$$

Another approach in designing an LC oscillator is Cross-Coupled oscillator, which is divided into three different types in
Figure 13 , PMOS-Only, NMOS-Only and Complementary Cross-Coupled.

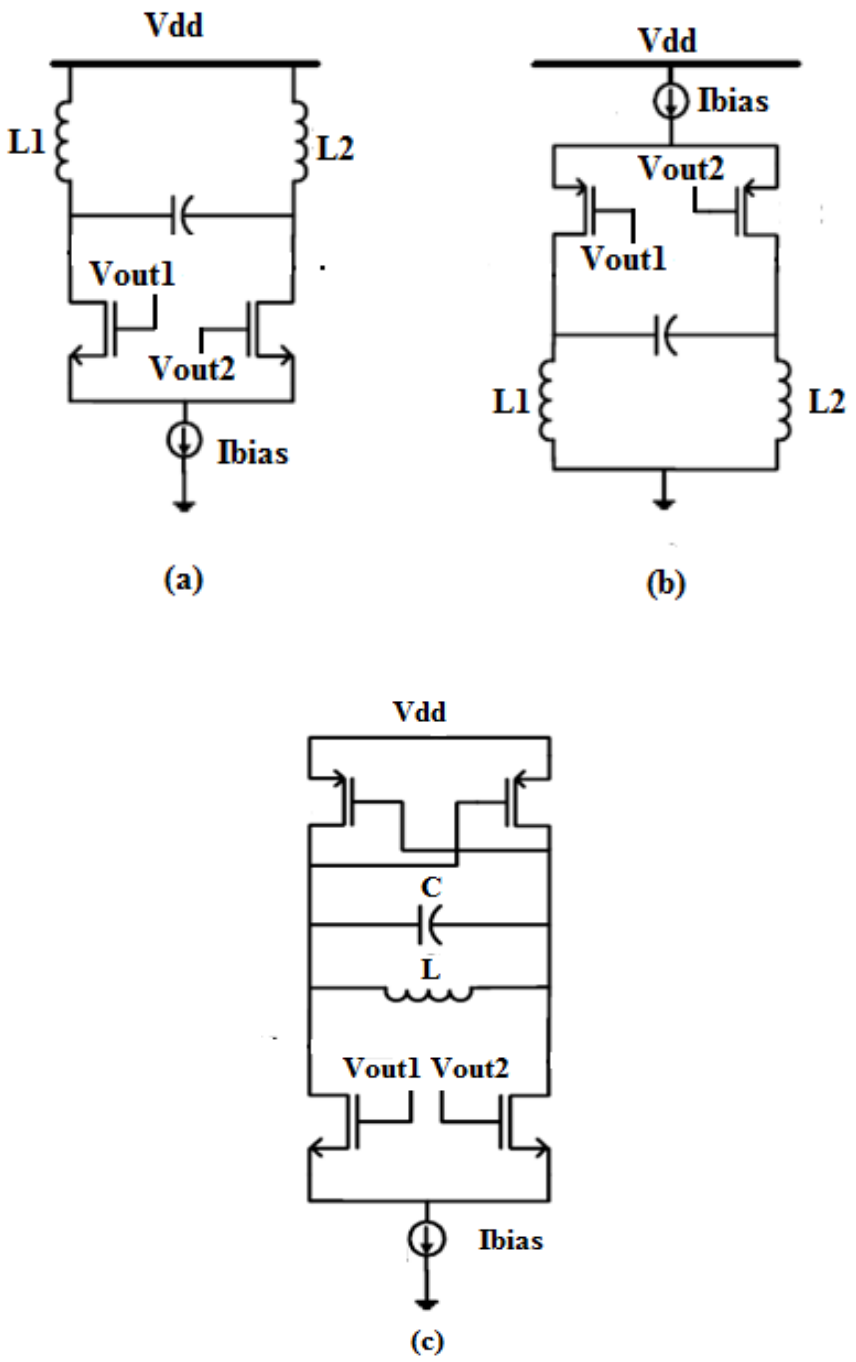

Figure 13 Cross-coupled Oscillators (a) NMOS only (b)PMOS only (c) Complementary

In [7] it is presented that the total phase shift around the loop is zero at resonance, because each stage provides a zero frequency dependant phase shift, resulting in the following limitation on gain to start the oscillation:

$$g_{m1}R_P g_{m2}R_P \geq 1 \longrightarrow \left(g_m R_p\right)^2 \geq 1 \qquad (3)$$

When choosing between Colpitts oscillator and Cross-Coupled oscillator, it should be noted that Colpitts suffer from two drawbacks; Firstly, with regards to equations (2) and (3) it can be seen that the gain has to be 4 times higher in Colpitts with identical LC tank, resulting with either larger transistor size or higher biasing current and as a consequence of this higher power consumption. Secondly, there is no differential output in Colpitts oscillators. Here, it should be mentioned here that maximum noise rejection is feasible in fully differential oscillator compared to the one in single mode oscillator, and the level of SNR (Signal to Noise Ratio) is higher in differential circuit. Consequently, a fully differential model has been chosen for this project.

CHAPTER 3 VCO DESIGN

In this chapter, a 2.2-5.7 GHz Multi-band Differential LC Voltage Controlled Oscillator (VCO) for the Multi-band Multi-standard is presented. It was designed for a multi-band transceiver architecture that utilizes a controllable VCO which operates at different frequencies in a wide frequency range. The advantages of Multi-band Differential LC VCO topology are: 1) 5 controllable frequency bands, which are utilized by multi-standard; by the help of switching inductor and capacitor method 2) the provision of low phase noise by using all PMOS current sources topology which has minimum intrinsic and extrinsic sources of noise. Five frequency bands, which are obtained from wireless communication standards in Section I, are the multi-band view of the design. Additionally, another goal is achieving multi-band operation with low phase noise. The circuit is designed with AMS 0.35μm SiGe BiCMOS process that includes high-speed SiGe Heterojunction Bipolar Transistors (HBTs). 0.35 um Sige BiCMOS is fairly old technology. However, in this project, technology is not major concern. Figure of merit of the project is comparable with the previous VCO designs that are used newer technology. The advantage of this project is covering wider frequency band than the other VCOs. This is succeed by adding a novel switch approach to the circuit which was defined in this chapter.

3.1 Topology and Design procedure

VCO Circuit Design Review

Various material systems and transistor technologies such as InGaP/GaAs HBT, SiGe BiCMOS, Si CMOS, and Silicon-on-insulator (SOI) CMOS can be used to meet the specification of multi-communication standards mentioned in Section I.

A CMOS dual band Voltage Controlled Oscillators realized with 0.18μm CMOS technology operates at 2.15 GHz - 2.756 GHz and 4.756 GHz - 4.996 GHz [47]. This VCO demonstrates a phase noise of -121.45 and -118.4 dBc/Hz at 1MHz offset from the frequencies of 2.4 and 4.86 GHz. The tuning range is relatively low in comparison with 5-6GHz coverage of the standard. Moreover, the design with two different LC tanks providing dual-band oscillation is not a cost-effective design when compared to single LC tank topology.

A remarkable work performed with 0.13µm SOI CMOS demonstrates a 3.065-5.612 GHz coverage with -114 dBc/Hz phase noise at 1 MHz offset while drawing 2mA from 1V supply. This performance is succeeded by taking the advantage of SOI structure and eliminating the adverse effect of Accumulation mode varactors (AMOS) using band switching topology [23].

The Ultra-wide band voltage controlled oscillator (VCO) have been designed by using 0.35 um SiGe BiCMOS technology [45]. The VCO provides an oscillation band between 2.67 to 4.37 GHz. Novel resonant circuit, which consists of three NMOS varactor pairs, p-n diodes, two spiral inductors and a control unit, allows the VCO to have a wideband tuning range. At a collector voltage of 4.0 V, the DC current consumption of the VCO is 5.8 mA. A phase noise of -111 dBc/Hz at 1 MHz offset at an oscillation frequency of 4.37 GHz was ensured.

All-PMOS wideband VCO having Automatic Amplitude controller for multi-band multi-standard radios was fabricated by using improved capacitor switching method in TSMC 0.18 µm CMOS technology. The frequency band and tuning voltage are 2.78-3.78 GHz and 0-1.8 V, respectively. The measured phase noises at 1 MHz from carrier frequencies of 2.83, 3.24, and3.77 GHz are -126.5, -125.0 and -122.7 dBc/Hz, respectively. With 1.8 V voltage supply, the current flowing into the VCO core varies between 4.9 mA to 5.7 mA[47].

VCO Design in this work

The ring oscillators [17], multivibrator oscillators [6] and Resonator (LC) based oscillators [19] can be used as an RF VCO topology. The Multi-vibrator oscillators are utilized for very high tuning ranges. The ring oscillator topology that is composed of an odd number of inverter stages has also high tuning range. However, these oscillators usually have less spectral purity than does their LC counterparts. The LC based oscillators are the most appropiate topology for low phase noise designs.

In a practical circuit, the oscillators will die away unless feedback is added in order to sustain the oscillation. The feedback (or negative resistance) is usually provided by tapped inductor and amplifier (Hartley oscillator), two amplifiers ($-G_m$ oscillators) or tapped capacitor and amplifiers (Collpitts oscillator). Due to the difficulties in IC tapped-inductor implementations, Hartley topology is usually not prefered. Although there are some successful realizations of

Collpitts configurations, - G_m topology generally results in higher performance wireless applications [6].

The differential LC - G_m configuration shown in Figure 14 is chosen for Multi-band VCO because of meeting the phase noise requirements of the communication standards and topological advantages. In an RF transceiver block, VCO usually drives the mixer which is composed of differential Gilbert Cell. Moreover, differential topology enhances the output power in exchange with the increased power consumption, the larger chip area and the increased complexity. Finally, differential LC $-G_m$ configuration provides a higher common-mode rejection ratio (CMRR), thus higher linearity [20].

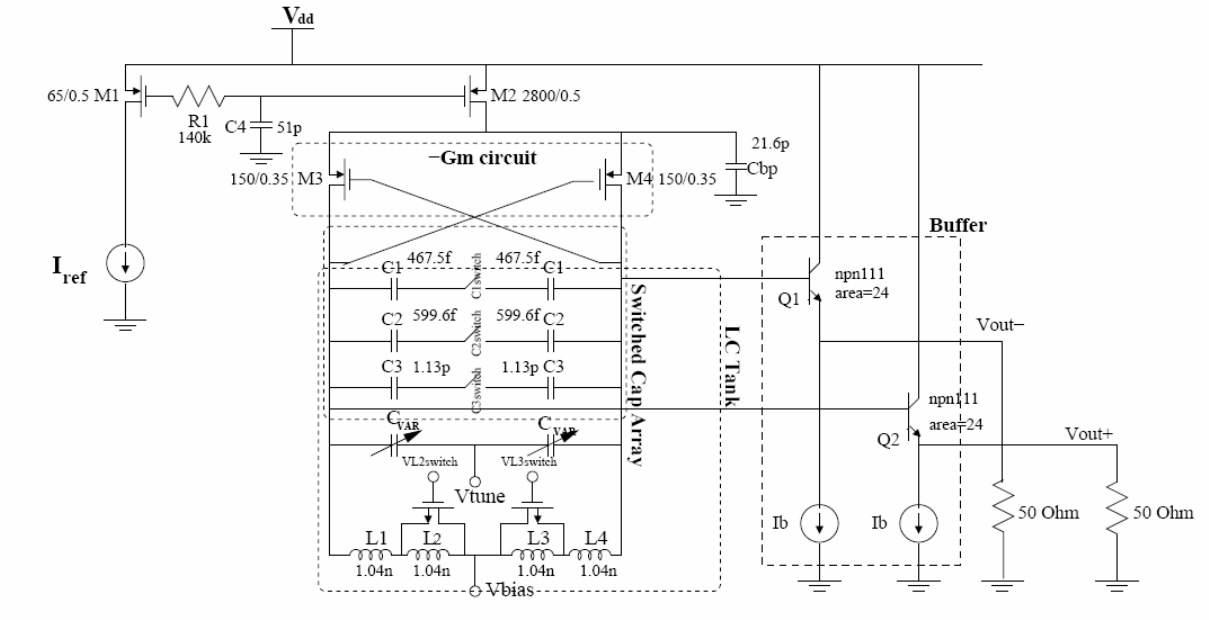

Figure 14 Multi-band VCO schematic including LC switched resonators

The NMOS, PMOS, or complementary cross-coupled designs can be used as LC VCO circuit topologies for wideband VCOs. Since it consumes less current to compensate losses in the tank and has lower upconversion factor of flicker noise, a complementary cross-coupled VCO is quite attractive. However, it reduces the voltage headroom of the current source, and introduces more parasitic capacitance as well as noise sources to the tank [21]. Thus, a non-complementary topology is used for the thesis project.

All-PMOS VCO topology is the most appropriate in terms of low phase noise performance because the topology has minimum intrinsic and extrinsic sources of noise [24]. The Cross-Coupled has two more transistors compared to PMOS Only, resulting in almost five times

more parasitic capacitance and hence degradation in tuning range and the introduction of more noise sources. The reason why an all-PMOS VCO topology is chosen is explained in detail in section 3.4.

3.2 LC Tank Design

The method which is used to design the capacitive and inductive part of the LC-tank, was based on information about the desired VCO characteristics in section I and II. In order to cover the desired bands, VCO tank is divided into three blocks as switched inductor, switched capacitance and fine tuning circuitry. The detailed information is given about these three parts in the following sections and also all sections define why the designed topology or type of component was chosen.

3.2.1 Tank inductance

The low Q values of inductors implemented in BiCMOS with RF operation are the drawbacks of VCO design. The lowest Q value means that the loss in the LC tank was mainly caused by the inductor. Therefore, the quality factor of the inductor is the dominant influence on the phase noise performance of the VCO. The selection of the inductor could be seen as a starting point of VCO design because of limited library of AMS. This chapter studies necessary considerations for utilization of inductors implemented in BiCMOS. Finally, the inductor that will be used in actual VCO design is presented.

Previously, the discrete components and usually surface-mounted devices were utilized in the circuit. Because of cost and size issues that approach is unsuitable today. Based on the fact that monolithic on-chip inductors are now widely utilized in radio frequency integrated circuit design. They are typically used in resonators such as in VCO or matching networks. In both applications, the critical parameter for the inductors is the quality factor because it improves circuit performance in terms of efficiency, insertion loss, gain and noise figures. The metal and substrate losses are the reasons for low Q-value inductors in BiCMOS technology.

The integrated spiral inductors are the square, circular and octagonal shapes, as shown in Figure 15. The Q-value and the utilization of minimum die area are the selection criteria for a specific type of geometry. An obvious and efficient inductor structure is the circular shape that was based on a smooth continuous circular conductor. Therefore the circular shape has

minimum die area for a given inductance and provides the best area/length relationship compared to the other inductor shapes. The trace length determines the series resistance while the area determines the inductance. However, the process technologies set limitations regarding inductor shapes because of limitations in the masking process.

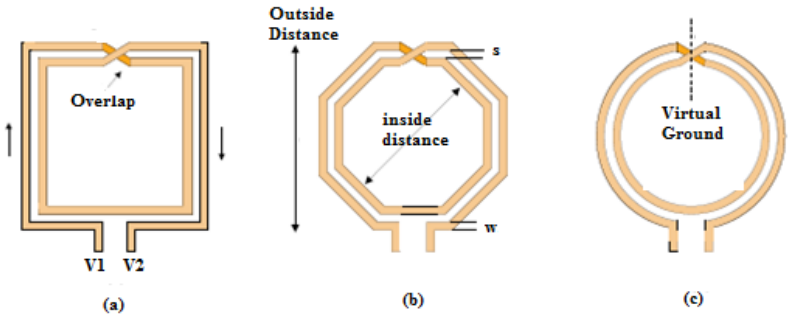

Figure 15 Inductor Geometries ; (a)square (b) octagonal, (c) circular

The differential inductors are preferred such as those depicted in Figure 15 when designing cross-coupled VCOs. This symmetry enables the cross-coupled VCO to be completely symmetric and thereby ensures that a virtual ground exists at the plane of symmetry. In the designed case where the VCO is an PMOS only type, a center tap is added to the differential inductor thereby enabling DC biasing through the inductor.

Inductor Model

The differential and single-ended inductors can be shown by an equivalent circuit in terms of a two-port π-network consisting of lumped passive components. The equivalent circuit represents different assumptions and correspondingly exhibits different complexity. The equivalent lumped model used for modeling is depicted in Figure 16.

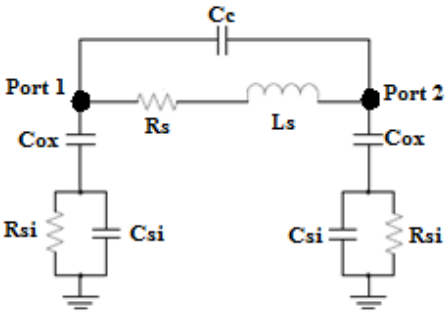

Figure 16 Inductor Modeling: Lumped –model of the two port spiral inductor

R_s: The series conductor loss is represented by the series resistance R_s.

C_c (C_p): The capacitive coupling between the turns and the coupling originating from over/underpass

L_s: Self and mutual inductances.

C_{ox}: The oxide capacitance found between the inductor and the silicon substrate.

$R_{si:}$ The resistance of the conductive silicon substrate

$C_{si:}$ The parasitic capacitance found in the substrate.

If the inductor has to perform single-ended operation as in the VCO, the port-2 of the equivalent π-model shown in Figure 16 must be connected to ground as Figure 17 thus obtaining the definition of the single-ended Q-factor [25]:

$$Q_{L,11} = \frac{imag(Z_{11})}{real(Z_{11})} = \frac{imag(\frac{1}{Y_{11}})}{real(\frac{1}{Y_{11}})} \tag{4}$$

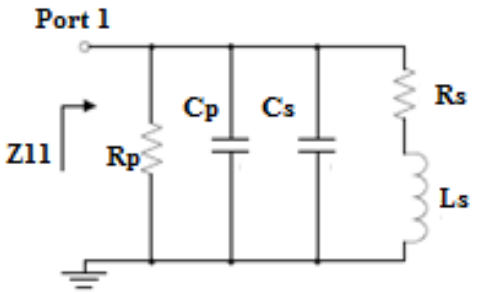

Figure 17 Equivalent circuit of one port grounded inductor

The same principle applies for derivation of the single-ended inductance:

$$L_{11} = \frac{imag(Z_{11})}{2\pi f} = \frac{imag(\frac{1}{Y_{11}})}{2\pi f} \tag{5}$$

The quality factor of the overall tank circuit is determined from the parasitic conductance of capacitance and inductance. Since the accumulation mode MOS varactors have relatively

higher Q values than on-chip inductors, inductor Q is the main determining factor of the overall Q of the tank circuit.

The inductors and capacitors in LC tank are simulated and analyzed individually. The AMS library inductor is used as inductor of the LC tank; its characteristics can be observed in Figure 18 and Figure 19. From the Figure, the inductor has an inductance of 1.04nH with a quality factor varying between 8.7 at 2.4 GHz to 11.8 at 5 GHz.

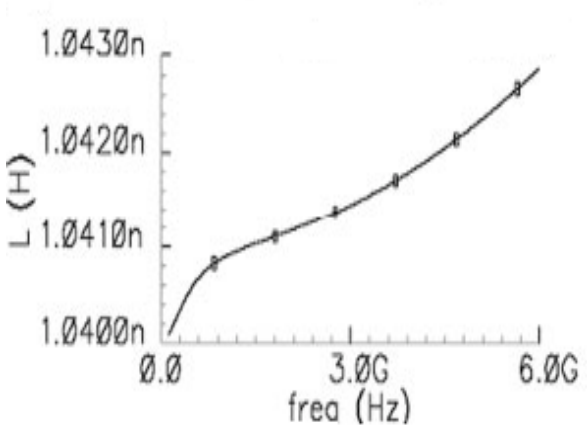

Figure 18 Inductance value of AMS library inductor.

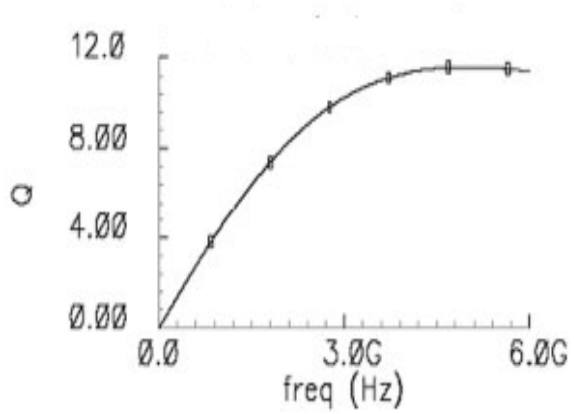

Figure 19 Quality factor of the AMS Library Inductor

The layout of the square-shaped AMS Library inductor is shown in Figure 20 Inductor Layout. The top metal layer is utilized for the traces of the inductor. Each inductor has an area of 287.4μm*264.4μm = 0.076 mm^2.

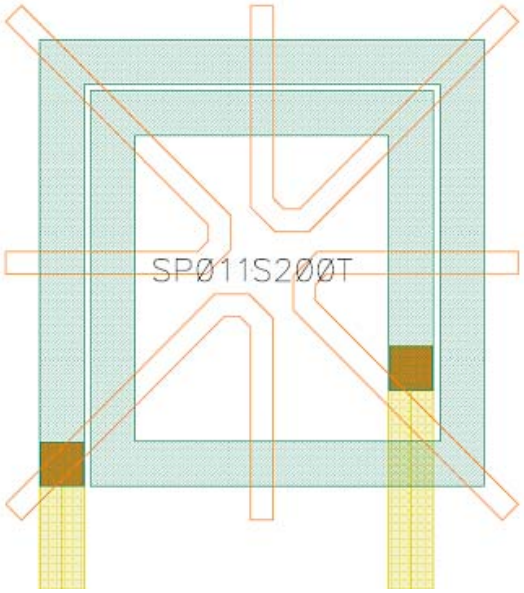

Figure 20 Inductor Layout

3.2.2 Tank Capacitance

In the BiCMOS process, the capacitors that use Metal–insulator-metal (MIM) capacitors [25,26], MOSFET gate oxide and Poly-insulator-gate (Double Poly) capacitors are the available capacitors. The MOS capacitors and junction capacitors that have higher capacitance density are not suitable for these applications because of their non-linearity that means their capacitance value changes with applied voltage. Also their values depend on temperature [25]. Additionally, MOS capacitors have a very poor quality factor due to the high series resistance. To achieve a better linearity and quality factor, the parallel plate metal-to-metal capacitors can be chosen. However, as a result of large vertical spacing between the plates means low capacitance value. The metal finger capacitors could be seen as a solution to increase the capacitance density of parallel plate capacitors.

The double poly capacitor is a well-established component but it suffers from the limited RF capability in multi-GHz range. Due to the the resistive losses in the plates and contacts and parasitic capacitance between passive component and the loss silicon substrate. The

limitations in the quality factor are naturally reduced for the MIM capacitor, where the bottom plate is positioned further from the substrate (Figure 21) and metal plates are inherently low in resistance. The MIM capacitors have much better voltage linearity, lower series resistance, much lower parasitic capacitance, and excellent matching. Moreover, the fabrication process of the MIM capacitors has less heat which is important for sub-micron transistors.

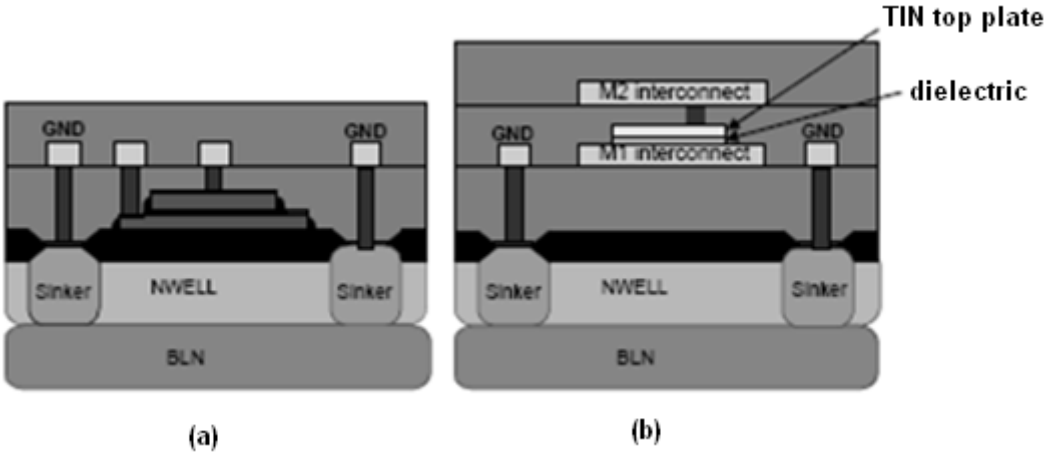

Figure 21 Cross Sections of (a)Double Poly capacitor (b) the MIM capacitor[27]

MIM capacitor was chosen for this design because of its advantages for the RF applications discussed above. The equivalent circuit model for an MIM capacitor is shown in Figure 22. In this circuit, C_s is the main element of the capacitor, R_s and L_s are the parasitics existing in the electrodes, and C_{ox1} and C_{ox2} are the parasitics that represent the capacitance to ground due to the bottom and the top plate metal, respectively.

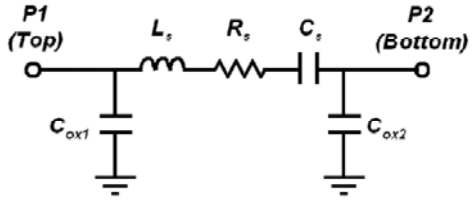

Figure 22 Equivalent circuit Model of an MIM Capacitor

A remarkable work regarding two-port, parallel plate, square structure MIM capacitors [28] helps to form an opinion about the parasitics of MIM capacitances. In this work, MIM capacitors that have different sizes (The width of the edge per side of the squares is 10, 15 ,25 and 50 μm) are utilized to describe the behavior of MIM capacitors for various device

geometries. After performing the measurements and extractions for each device, they drive the scaling rules as shown in Table 3 [29].

	Scaling Rule
R_s [Ω]	$14.52 / L_{MIM} + 0.91$
L_s [pH]	$404.93 / L_{MIM} + 132.82$
C_s [pF]	$0.00106*(L_{MIM} + 0.388)^2$
C_{ox1} [fF]	7.5
C_{ox2} [fF]	$0.00220*(L_{MIM} + 55.893)^2$

Table 3 Scaling Rules for a square MIM capacitor with L_{top} in the range of 10~50 μm. L_{MIM} is the edge per side of the MIM layer in μm

3.2.3 Switch Method

The total quality factor of the resonance tank limits the phase noise performance of an oscillator, whereas the capacitance ratio is important as it limits the achievable tuning range.

The traditional switch circuit implementation is presented at Figure 23. When the transistor is at ON state, there would be no DC current flowing through the capacitor and thereby the transistor. The transistor's drain-source DC voltage equals zero, therefore, MOSFET operates in the triode region [7].

The ON resistance of the transistor can be calculated by using a simple transistor model,

$$r_{ds0} = \frac{1}{g_{ds0}} \qquad g_{ds0} = \mu . C_{ox} . \frac{W}{L} . (V_{gs} - V_t) \tag{6}$$

where μ; C_{ox}; W, and L are the mobility, gate oxide capacitance per area, width, and length of the transistor.

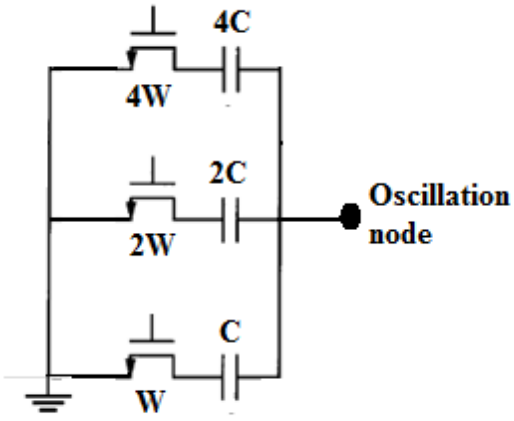

Figure 23 Binary weighted array of switched capacitors

The quality factor of the resulting series *RC*-link is, thus, equals to

$$Q = \frac{1}{2\pi f C\, r_{dso}} \tag{7}$$

In order to provide a high quality factor, the transistor dimensions (width and length) can be changed by designers. As can be seen at (6) equation, the minimum length should be used for best performance. The width will be determined by compromising between tuning range and quality factor. At the OFF state, the conductance g_{ds0} will be negligibly small. The C_{gd} and C_{db} capacitances (neglected at the ON state) dominate the transistor's impedance. There is a pn junction formed by the p-doped substrate and the n-doped drain between drain and bulk, whereas the gate-drain capacitance is due to the overlap between gateand drain.

$$C_{off} = Capacitance\ value\ of\ switched\ capacitor + drain\ capacitance$$

When the transistor is OFF, C_{off} , the capacitance of the tuning circuit seen by the oscillator, is the series connection of the capacitor being switched OFF and the drain capacitance C_d of the transistor ($C_d = C_{db} + C_{gd}$). The drain capacitance is related with the width of the transistor. A wide transistor thus increases the quality factor but reduces the tuning range, leading to a compromise. Since (7) contains the frequency in the denominator, obtaining a good compromise is difficult at higher frequencies. The following equations show that an

achievable performance can be related to the ratio of the transistor transition frequency f_t to the operating frequency

$$f_t = \frac{g_m}{2\pi C_g} \tag{8}$$

$$\frac{\Delta C}{C_{OFF}} = \frac{C_{ON} - C_{OFF}}{C_{OFF}} = \frac{C - \frac{C.C_d}{C + C_d}}{\frac{C.C_d}{C + C_d}} = \frac{C(C + C_d) - C.C_d}{C.C_d} = \frac{C}{C_d} \tag{9}$$

$$Q.\frac{\Delta C}{C_{OFF}} = \frac{1}{2\pi f r_{ds0} C_d} = \frac{g_m}{2\pi f C_g}.\frac{1}{g_m r_{ds0}}.\frac{C_g}{C_d}$$

$$= \frac{f_t}{f}.\frac{g_{ds0}}{g_m}.\frac{C_g}{C_d} \tag{10}$$

where gm: the transconductance of the transistor in saturation

ΔC: is the difference in capacitance between the ON and OFF state.

The last expression is used as a performance measure. In modern BiCMOS process, C_g/C_d is approximately equal to unity, but g_{ds0}/g_m which is equal to unity in the long channel low electric field situation, can be substantially larger for short channel devices with high gate voltages [7]. In such a situation, disregarding this term in (10) would lead to an underestimation of the achievable performance.

The novel idea here is to use just one transistor as shown in Figure 24 instead of two transistors for switching the same capacitance value in whole circuit. The performance of the switch circuit could be seen from (8), (9) and (10) equations. When a branch is ON it will contain two r_{ds0} in series going from one side of the differential circuit to the other. So this limits the quality factor. With the improved differential switched-tuning circuit the quality factor of the switch circuit will be doubled while keeping the transistor sizes the same and switching the same fixed capacitance. The purpose of the big resistors in the circuit is to ensure that the transistor is OFF at all times in an OFF state and obtain the maximum gate to

source (and drain) voltage in the ON state. Moreover, the other purpose of giving Vdd to drain and source at OFF state is reducing and getting a better control of reverse biased drain-bulk capacitance [15].

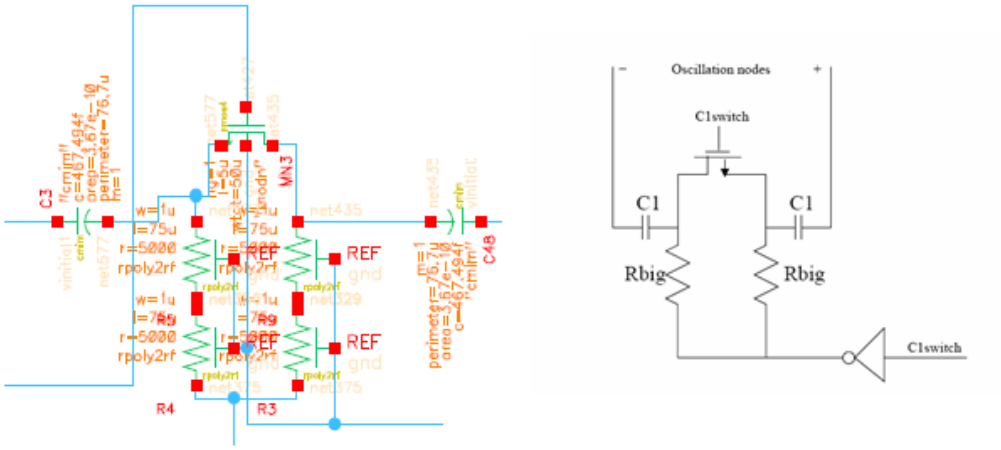

Figure 24 Improved differential switched-tuning circuit

The multi-band tuning concept in a wideband range has been attempted by a utilizing switched inductor with a poor phase noise outcome [30]. The switched inductor concept that is shown in Figure 25 is used for increasing the tuning range and for achieving low phase noise. According to the transistors ON and OFF states, the inductance that is seen between ports 1 and 2 is changed. At the OFF state, the total inductance is approximately the sum of the L1 and L2. When transistor is on, the branch is shorted and inductance seen from port 1 is decreased to L1. Also, the capacitance seen from L1 side is reduced because of shorting the transistor capacitances and the capacitances associated with L1 (partially) and L2 to the ground by a low resistance path. By the help of switching method, the circuit has the ability of simultaneously decreasing inductance and capacitance [31]. This tuning ability provides circuit flexibility for trade off between the phase noise and power consumption [32] compared to the case of using only switched capacitors [33].

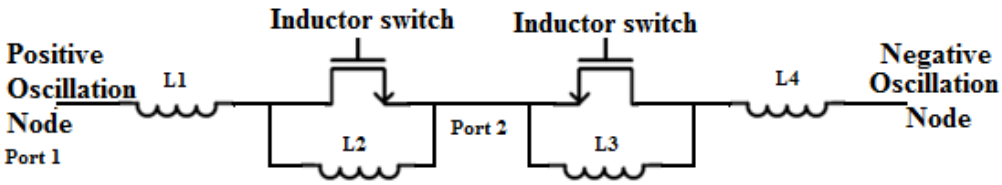

Figure 25 Schematic of switched resonator

3.2.4 Varactor

For the multi-standard operation, a VCO needs to cover a wide frequency range. Typically, in the LC-oscillators, the varactors are used for continuous frequency tuning. However, high tuning sensitivity means high sensitivity to noise and disturbances on the control voltage. Moreover, large metal–oxide-semiconductor (MOS) varactors convert harmless amplitude noise into harmful phase noise. In this work, an improved switching inductor and capacitance technique have been used as a controller concept of a LC tank to cover a wide frequency range and reduce the noise problem.

In the BiCMOS and CMOS technologies, the tuning range is also a critical performance parameter in designing VCO. The accumulation mode MOS varactors are commonly preferred for tuning owing to the fact that p-n junction varactors and inversion mode MOS varactors have limited tuning range. The AMOS varactors have the highest tuning range among other varactors types. Moreover, with AMOS varactors, VCO can be tuned more linearly [15].

This chapter presents an overview on different varactors configurations suitable for BiCMOS implementation. Furthermore, the AMOS varactor, which was chosen for this application as appropriate, was researched considering its large signal analysis and subcircuit model.

i. Varactor Types

The minimum and maximum capacitances and Q-value are the main specifications of a varactor. Because of dominant influence on the tuning linearity of the VCO frequency, the linearity of the tuning curve of varactors shown in Figure 26 is important.

The output frequency is expressed by: $\mathbf{f_{out} = f_o + K_{vco}.V_{const}}$, where $\mathbf{K_{vco}(voltage\ gain)}$ has the unit of Hz/V. Ideally, as shown in Figure 26, the slope of the line is constant. In practical, the gains of the varactors are not constant. The main differences between various types of varactors are found at their C-V characteristics and Q-values. The differences will be clear in the following subsections, where different varactor types suitable for BiCMOS implementation are introduced.

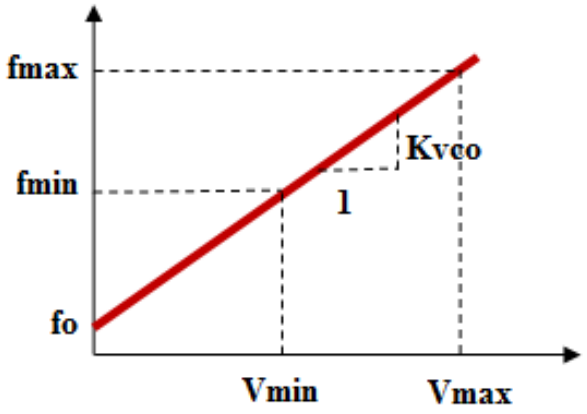

Figure 26 Ideal Frequency Tuning Curve

PN-JUNCTION VARACTOR

The first option for the realization of varactor tuning elements in SiGe BiCMOS process is pn-junction varactors. The varactor is obtained from p+/n- well junction also known as diode. A cross section of a junction capacitance is sketched in Figure 27.

Pn junction varactor operation was achieved by applying a reverse bias voltage, $V_{R,}$ across the anode (A) and cathode (C) terminals. The reversed bias voltage determines the width of depletion region, thereby the junction capacitance. Thus, the varactor capacitance value is related with the depletion region between the p+ diffusion and the n-well. A p /n-well structure can typically have a quality factor of 20 or better. The drawback of this varactor approach is that the diode can be forward biased if the signal voltage is high so that the diode enters the breakdown region. As a consequence, the varactor will be short circuited and will short circuit the two VCO nodes, thereby blocking the oscillation.

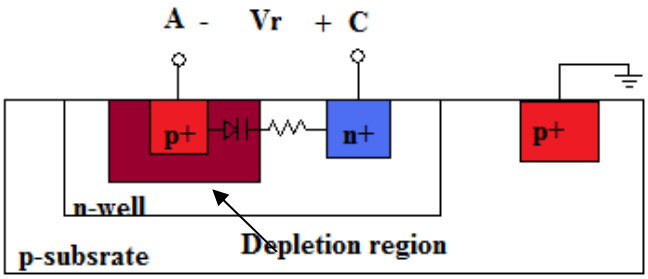

Figure 27 Cross section of p^+/n-well junction capacitance

MOS VARACTOR

By connecting drain, source and bulk (B,S,D) together, a MOS capacitor of whose capacitance value changes with V_{bg} could be realized. For a pMOS capacitor, an inversion channel with mobile holes builds up for $V_{bg} > |V_t|$. The condition $V_{bg} >> |V_t|$ guarantees that the MOS capacitor works in the strong inversion region. In this region, the MOS device shows a transistors behavior. The MOS device enters the accumulation region for $V_g > V_b$ where the voltage at the interface between gate oxide and semiconductor is positive and high enough to allow electrons to move freely.

The value of the MOS capacitance C_{mos} is;

$$C_{ox} = \frac{\varepsilon_{ox} \cdot S}{t_{ox}} \text{ (S: transistor channel, } t_{ox} \text{: oxide thickness region)}$$

in both strong and accumulation region.

The moderate inversion, the weak inversion, and the depletion are three more regions that change with intermediatevalues of V_{bg} [34]. When passing from the accumulation region to the depletion region the capacitance will drop because of the number of major carriers. After the depletion region, Vg will be less than Vb with a difference of $|V_t|$. So the inversion layer starts to be obtained under the gate oxide. As a result of the decreased gate voltage, capacitance will rise sharply because of the strong inversion layer. The characteristics for the PMOS capacitor are shown in Figure 28.

Figure 28 shows the C_{mos}–V_{bg} characteristics for a very small signal superimposed on the bias voltage. If the signal at the transistor gate (for MOS capacitances) is large, then the instantaneous value of capacitance changes throughout the signal period. The designer should not allow the capacitance changing of the LC tank (non-monotonicity). An almost monotonic function for C_{mos} can be obtained if the transistor does not enter the accumulation region for a wide range of values of V_g.

The monotonic function is obtained by breaking the connection between D-S and B, and giving the highest DC-voltage available in the circuit (V_{dd}) to the Bulk (Inversion MOS capacitor, Figure 29). Figure 30 shows the comparison between the typical C_{mos}-V_{sg}

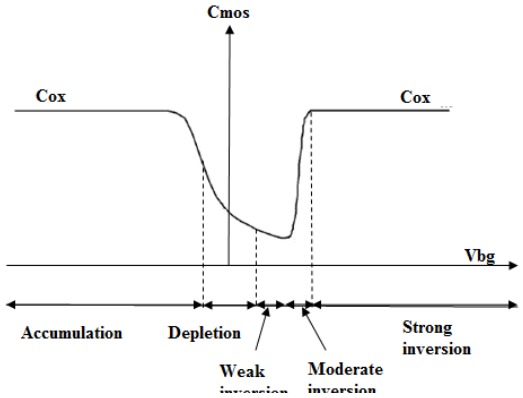

Figure 28 Typical tuning characteristics for the PMOS capacitor with B≡ $S \equiv D$

characteristics of pMOS capacitors and B=S=D capacitor. It can be seen that the tuning range of the IMOS capacitor is much wider than that of the previous capacitor, since the former capacitor is working in the strong, moderate, or weak inversion region only, and never enters the accumulation region.

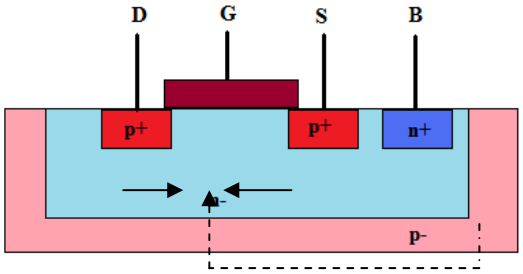

Figure 29 Charge carrier path for the IMOS capacitor

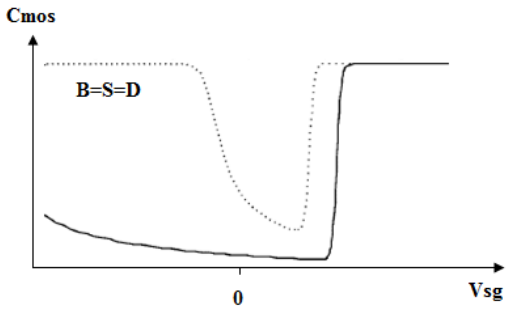

Figure 30 Typical tuning characteristics for the inversion mode varactor

The rationale of obtaining an AMOS (accumulation-mode MOS) type capacitor is to ensure that the formation of the strong, weak, and moderate inversion regions is inhibited (which

means the suppression of any injection of holes in the MOS channel). The structure, in turn, can be accomplished with the removal of the D–S diffusions (p^+-doped) from the MOS device (since we are dealing with circuits working at radio frequencies, we do not need worrying about thermal generation of hole-electron pairs). Implementation of the bulk contacts (n^+) in the left by D–S is required, as shown in Figure 31, for minimizing the parasitic n-well resistance of the device. The tuning characteristics of the A-MOS capacitor and also comparison with the B=S=D capacitor is shown in Figure 32.

In order to chose a suitable varactor type for VCO, research on VCO performance has been done [28]. Three different varactors (tuned by a diode varactor, an I-MOS varactor, and an A-MOS varactor, respectively) were utilized in VCO in order to obtain the tuning range and the center frequency. All varactors were designed for maximum Q (i.e., the lengths of the devices are the minimum lengths allowed by the process). Three important parameters were taken into account for comparing with the VCOs such as minimum current consumption, phase noise and tuning range. The minimum current consumption for oscillation measurement gives a rough indication of the (relative) parasitic resistance in the LC-tank. Also phase noise measurement is an important indication for comparison while the other parameters are equal [35].

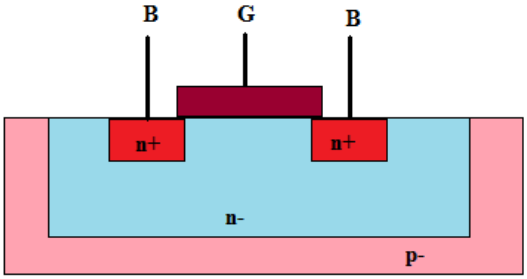

Figure 31 Accumulation-mode MOS capacitor

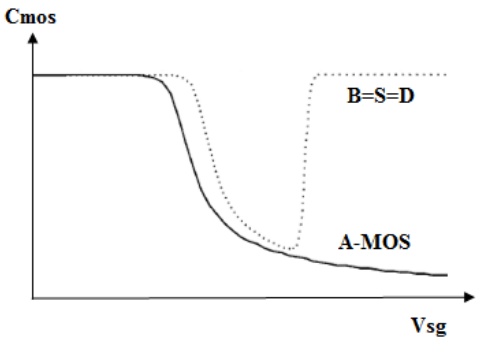

Figure 32 Typical tuning characteristics for the accumulation mode varactor

The measurement results given at Table 4 and 5, show that the performances of both MOS varactor VCO's are superior to that of the diode varactor VCO [28]. In particular, the accumulation-mode MOS varactor VCO clearly displays the lowest power consumption and the lowest phase noise at large offset frequencies from the carrier.

Varactor	f_L-f_H (Ghz)	f_C (GHz)	Tuning Range
Diode	1.73-1.93	1.83	10.9%
I-MOS	1.71-1.91	1.81	11.0%
A-MOS	1.70-1.89	1.80	10.6%

Table 4 Frequency Behavior of the VCOs

Minimum current consumption for all varactor types

A-MOS: 0.87 mA $< \boldsymbol{I_{dd}} <$ 0.99$\boldsymbol{mA}$

Diode: 1.80 mA $< \boldsymbol{I_{dd}} <$ 2.44 $\boldsymbol{mA}$

I-MOS: 1.45 mA $< \boldsymbol{I_{dd}} <$ 1.65$\boldsymbol{mA}$

Varactor	I_{dd} (mA)	Phase noise 100 kHz, 600 kHz, 3Mhz Offset from carrier (dBc /Hz)
Diode	4.5	-100, -116,-130
I-MOS	3.8	-100, -117, -132
A-MOS	2.7	-101, -121, -137

Table 5 Phase Noise Behavior of the VCOs

ii. Large signal analysis of MOS Varactors in –Gm LC VCOs

The specific MOS varactor topologies resulting from the connections and their corresponding C–V characteristics are detailed in previous section. It should be added that there were no AC signal analysis while defining the characteristics. When varactors are utilized in VCO tank circuit, there would be large signal swing of the VCO output oscillation that modulates the varactor capacitance in time. Thus, this utilization affects tuning curve as deviating from the typical C-V curve or the practical varactor device structure.

The instantaneous value of the capacitance changes throughout the signal period when the signal voltage swing across these devices is large (as it would be the case in VCO tank). The effective capacitance seen by the large signal will be a weighted average of the small-signal capacitance over a single period. Because of this "averaging" effect, the oscillator RF output frequency versus tuning voltage curve and the DC/smallsignal C–V curve will not be equivalent [36].

3.3 Design of gm stage

Initially, the design of the gm-stage was based on the inductor loss i.e. the inductor Q-value was assumed to be the dominating component regarding loss in the LC-tank hence $g_{\text{tank}} \approx g_{\text{L}}$. It was necessary to make this assumption, since the drain-source conductance values of the gm-stage FETs were not known at that time. The case was the same for the switch and fine tuning circuitry since the design of these sub-modules was based on the value of parasitics capacitances of the gm-stage.

The Q-value of the inductor is dominant and hence the R_{L} will be used as the target resistance that must be canceled out. The simulated Q-value of the inductor model is 11.8 at 5 GHz.

The loaded Q-value of the tank representing the total losses of the tank is stated as:

$$Q_{loaded} = \frac{R_p}{\omega_0 L} \tag{11}$$

where R_p is the equivalent parallel resistance modeling the total loss of the tank while ω_0 is the resonance frequency. The loaded Q-value is related to the Q-value of the inductive and capacitive components, as follows:

$$\frac{1}{Q_{loaded}} = \frac{1}{Q_L} + \frac{1}{Q_C} \tag{12}$$

Equation 12 defines the relation between the loaded Q-value and the individual Q-value of the inductor and capacitor. The component Q-value of the inductor is given by $Q_L = \frac{\omega_0 L}{R_s}$ where Rs symbolizes the series resistance of the inductor. The Q-value of the capacitor is stated as

$$Q_c = \frac{1}{R_s \omega_0 C} \tag{13}$$

where Rs denotes the series resistance of the capacitor. Based on the fact that the Q-value of the actual capacitive part of the tank is assumed to be sufficiently higher than the inductor Q-value, the following statement is valid:

$$Q_L \ll Q_c \Rightarrow Q_L \approx Q_{loaded} \tag{14}$$

Using the statement shown in Equation (13) the equivalent parallel resistance of the loss tank is defined by:

$$R_P = Q_{loaded} . \omega_0 . L = \frac{(\omega_0 . L)^2}{R_s} = (\frac{\omega_0 . L}{R_s})^2 . R_s = Q_L^2 . R_S \tag{15}$$

where R_s is the series resistance of the inductor. It is desirable to have the R_p as large as possible since this can be translated to a higher loaded Q-value and thereby lower series resistance of the tank. A higher loaded Q means better phase noise performance which is one of the main goals in VCO design. Furthermore, a lower series resistance is likewise beneficial, since the low resistance relaxes the requirement of the needed value of negative resistance to start and to maintain the oscillation. The series resistance of the inductor is the only resistive part influencing the equivalent parallel resistance of the tank.

Knowing that the Q-value of the actual inductor is 11.8 the parallel resistance of the tank can now be found. The inductance is then 1.05 nH (at 5GHz) which leads to the following value of *R*p:

$$R_P = Q_L^2.\left(\frac{\omega_o.L}{Q_L}\right) = (11.8)^2.(\frac{2\pi.5.10^9.1.05.10^{-9}}{11.8}) \cong 389\Omega \quad (16)$$

Using the computed value of R_P ,the parallel inductor conductance is found by:

$$g_L = \frac{1}{389\Omega} = 2.57mS \quad (17)$$

Since $g_L \approx g_{tank}$ is assumed to be valid, by using safety factor of two and the PMOS must be designed such that they all two individually exhibit a transconductance value of:

$$g_{mn} = 4.2.57mS = 10.28mS \quad (18)$$

Each of the amplifying transistors must have a conductance g_m of 10.28mS,

$$g_{mn} = \sqrt{2.\mu_o.C_{ox.}\frac{W}{L}.I_D} \quad (19)$$

where μ_0 is the mobility of the carriers in the channel while I_D is the drain current through the MOSFET. In order to determine the drain current, the desired single ended output voltage swing of the VCO must firstly be specified. The tank amplitude is given by:

$$V_{tank} = I_{bias}R_P = I_{bias}.\omega_o.L.Q_L \quad (20)$$

The desired tank amplitude is set to V_{tank} = 500 mV and thus the required bias current is:

$$I_{bias} = I_{tail} = \frac{0.5\,mV}{389\Omega} = 1.2\,mA \quad (21)$$

The drain current of each FET in the VCO is half the value of the bias current, since the bias current flows through the two VCO branches equally at DC. The remaining parameters of Equation (19), which must be specified, are the carrier mobility:

$$\mu_p = 126\ \mathrm{cm}^2/\mathrm{Vs}$$

and the oxide capacitance is :

$$C_{ox,n} = C_{ox,p} = \frac{\epsilon_r \epsilon_o}{t_{ox}} = 4.57 fF/\mu m^2$$

Using the shown values, the W/L ratio was computed for PMOS transistor

$$PMOS: \ \frac{W}{L} = 536$$

The structure of the gm-stage is depicted in Figure 33. The definition of *g*m shown in Equation (19) is a simplified model compared to the highly complex models utilized in simulation environments. Based on this fact, the found aspect ratios of the gm-stage were optimized in Cadence with the purpose of achieving the desired value of $g_{m,p}$. The bias current of the gm-stage was provided by a current sink that is designed as a current mirror and this provides the I_D of 2.44-6.32 mA.

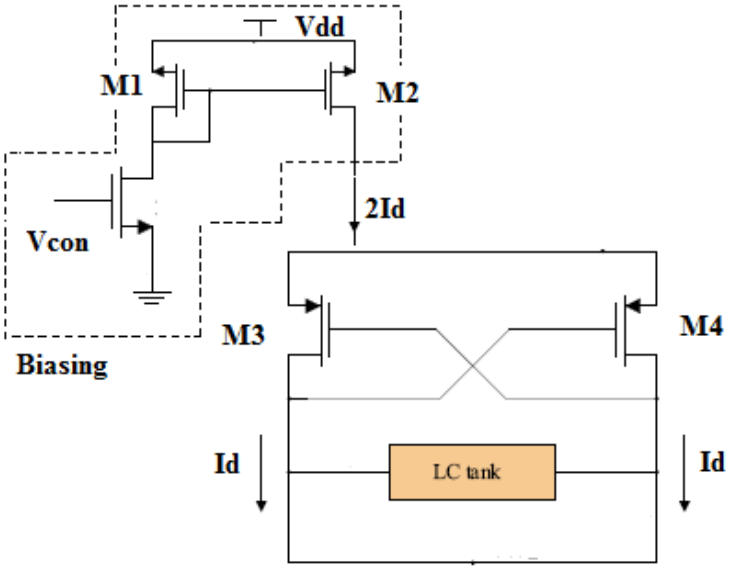

Figure 33 The configuration of the g_m stage that actually is the VCO core

The optimized aspect ratio of PMOS FETs is W/L = 430 yielding a *g*m of 6.42 mS. As observed, the simulated aspect ratios deviated from its hand-calculated counterpart, which was expected due to the simplified *g*m equation of the MOS model.

The final dimensions of the gm-stage FETs and their corresponding output resistances are shown in Table 6. The drain-source conductance values of the gm-stage FETs contribute to the LC-tank loss and the actual values were simulated and shown in Table 7. The output resistances of the gm-stage FETs are significantly higher than the equivalent parallel resistance of the inductor, namely Rp = 389 **Ω**. These output resistances are added to the inductor Rp as shown in Figure 34.

FET	L	W_f	N_f	W_{total}	Type
M1, M2	0.5µm	65µm,2800 µm	1 ,1	65 µm, 2800 µm	Pmos4
M3, M4	0.35µm	10 µm,10 µm	15,15	150 µm,150 µm	Pmos4
Mcont	1 µm	5 µm	1	5µm	Nmos4

Table 6 Physical dimensions of the four gm-stage FETs

FET	g_{ds}	1/ g_{ds}
M3, M4	383µS	2.61 kΩ

Table 7 Output Resistance of the gm- stage FETs.

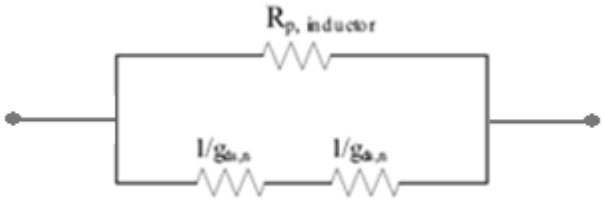

Figure 34 The Additional of gm-stage output resistance to $R_{L,inductor}$

Considering the FET output resistances, the new Rp equals:

$$R_p = \frac{1}{\frac{1}{389\Omega}+\frac{1}{2*2.61k\Omega}} = 362.12\ \Omega \qquad (22)$$

As observed in Equation 22, the total *R*p of the LC-tank is now reduced but it does not involve any critical consequences since the excess gain is still high enough to initiate oscillation.

3.4 Design of bias circuitry

The purpose of designing bias circuitry is to provide current for the $-G_m$ circuitry and filtering the current noise by the help of low pass filter. R_f and Cf values are 140kΩ and 51 pF. The low pass filter cut off frequency;

$$w_c = \frac{1}{2\pi RC} = 22.3\ kHz$$

The circuit of the designed current source is depicted in Figure 35.

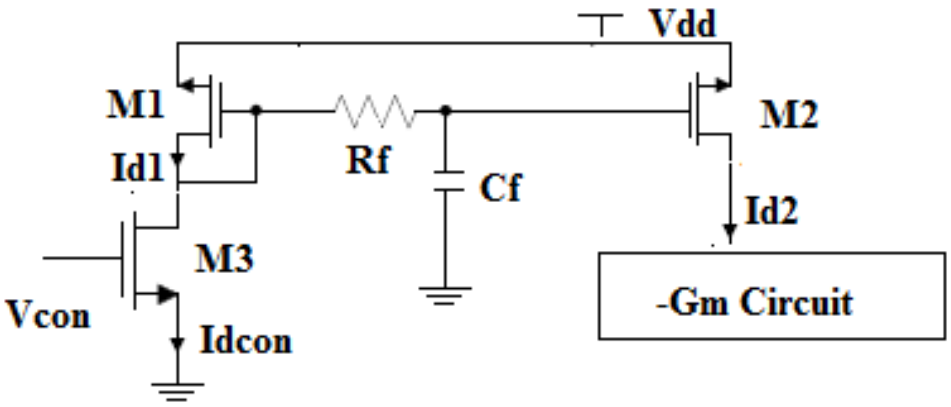

Figure 35 Current Mirror

For the same transistor size and gate over drive voltage, 1/f (flicker) noise of PMOS transistors is usually smaller than that of NMOS transistors in one order of magnitude [49]. For the same bias current and transconductance (gm), PMOS 1/f noise should be even lower because a PMOS transistor has lower mobility, so it needs larger size to keep the same transconductance compared to an NMOS transistor. In addition, a PMOS transistor has less

hot carrier effect. Hence, PMOS VCOs can achieve better phase noise performance than NMOS VCOs as described by the modified Leseson's Formula [50];

$$L(\Delta f, k_v) = 10\ log\left\{\left(\frac{f_0}{2Q\ \Delta f}\right)^2\left[\frac{FkT}{2P_s}\left(1+\frac{f_c}{\Delta f}\right)\right]+\left(\frac{k_v v_n}{2k_{LC}\ \Delta f}\right)^2\right\}$$

Here, Q is the quality factor, ∆f is the frequency offset from the carrier, F is the noise factor, k is the Boltzmann's constant, T is the temperature, P_s is the RF power produced by VCO, f_c is the Flicker noise corner frequency, f_0 is the frequency of oscillation, v_n is the common mode noise voltage, k_v is the varactor gain and k_{LC} is a constant that is a function of L and C of the resonator.

Furthermore, all-PMOS VCOs with top-biased current sources provide excellent suppression of power supply noise and minimize noise disturbances from the current source to the varactor through the use of ground referenced tank. In summary, an all-PMOS VCO topology is the most appropriate one in terms of low phase noise performance because it has minimum intrinsic and extrinsic sources of noise. Thus; PMOS VCOs have better phase performance – approximately 4 dB in the $1/f^2$ region or 9dB for offset frequencies from 10 kHz to 10 MHz- than NMOS VCOs [37].

Considering the channel-length modulation, λ, and assuming that $V_{DS} > V_{GS} - V_{th}$, the I_{dcon} and I_{d2} currents are approximately defined by [7]:

$$I_{d1} = \frac{w_1}{2.L_1}\ \mu_n C_{ox}\left(V_{gs} - V_{th}\right)^2(1+\lambda.V_{ds1}) \tag{23}$$

$$I_{d2} = \frac{w_2}{2.L_2}\ \mu_n C_{ox}\left(V_{gs} - V_{th}\right)^2(1+\lambda.V_{ds2}) \tag{24}$$

Then the current mirror ratio will be;

$$\frac{I_{d2}}{I_{d1}} = \frac{W_2/L_2}{W_2/L_2}.\frac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}} \tag{25}$$

Neglecting channel moduation effect (using table 6);

$$\frac{I_{d2}}{I_{d1}} = \frac{W_2/L_2}{W_2/L_2} \cong 43.02 \quad (26)$$

For 5 GHz oscillation frequency system needs 0.95 V voltage of Vcont;

$$I_{cont} = \frac{w_{cont}}{2.L_{cont}} \mu_n C_{ox}\left(V_{gs} - V_{th}\right)^2 = 51.32\mu A \quad (27)$$

This means;

$I_{d2} = I_{d1}$*43.02=2.207mA to provide the oscillation

3.5 Switched Circuitry

Recall that the purpose of the coarse tuning circuitry was providing a constant capacitance step so that the requirements for the tuning range of the fine tuning varactor could be relaxed. In order to achieve this functionality, the coarse tuning circuitry must be able to switch the desired capacitance into the tank and switch it out of the tank when desired. The coarse tuning circuitry used for this project provides this functionality and is depicted in Section 3.2.3.

The simplified model of the switched circuitry is shown in Figure 36. The FETs' physical dimensions, capacitor and inductor values are presented in Table 8. As mentioned before, the desired frequency achieved by using switches' ON/OFF states. The switch states and frequency bands will be shown in simulation results secition.

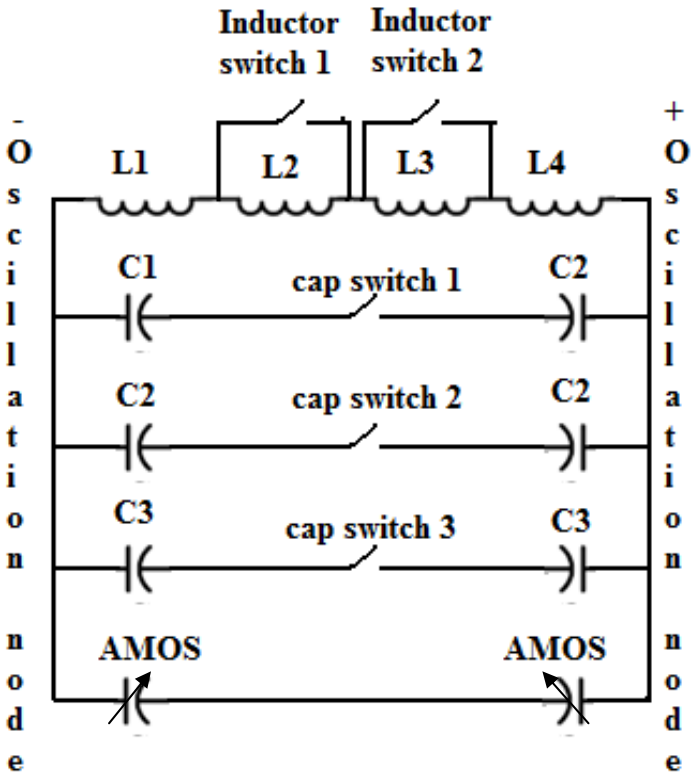

Figure 36 Simplified model of the switched circuitry

Component	L	W_f	N_f	W_{total}	Type	Value
M1,M2((inductor switch 1,2)	10µm	2000 µm	1	2800 µm	nmos4	-
M3 (cap switch 1)	5 µm	50 µm	1	50µm	nmos4	-
M4 (cap switch 2)	5 µm	30 µm	1	30 µm	nmos4	-
M5 (cap switch 3)	10 µm	50 µm	1	50µm	nmos4	-
L1,L2,L3,L4	-	-	-	-	square	1.02 nH
C1	-	-	-	-	cmim	467.5 fF
C2	-	-	-	-	cmim	599.94 fF
C3	-	-	-	-	cmim	1138 fF
R in cap switching circuit	-	-	-	-	presistor	10 kΩ

Table 8 Dimension for LC tank

3.6 Fine Tuning Circuitry

The accumulation-mode MOS varactors from the AMS library have been chosen instead of IMOS varactor for tuning concept due to the best overall performance on phase noise and power consumption [38,39].

An accumulation mode MOS capacitor that was implemented as three-terminal device is available as a varactor (Figure 37, Figure 38). The layout of the devices is composed of parallel connected small capacitors. The capacitance-voltage characteristics are modelled by the gate-bulk capacitance of a PMOS transistor. In addition the subcircuit model of the varactor contains parasitic resistors and diodes used for n-well/p-substrate junction capacitance modeling.

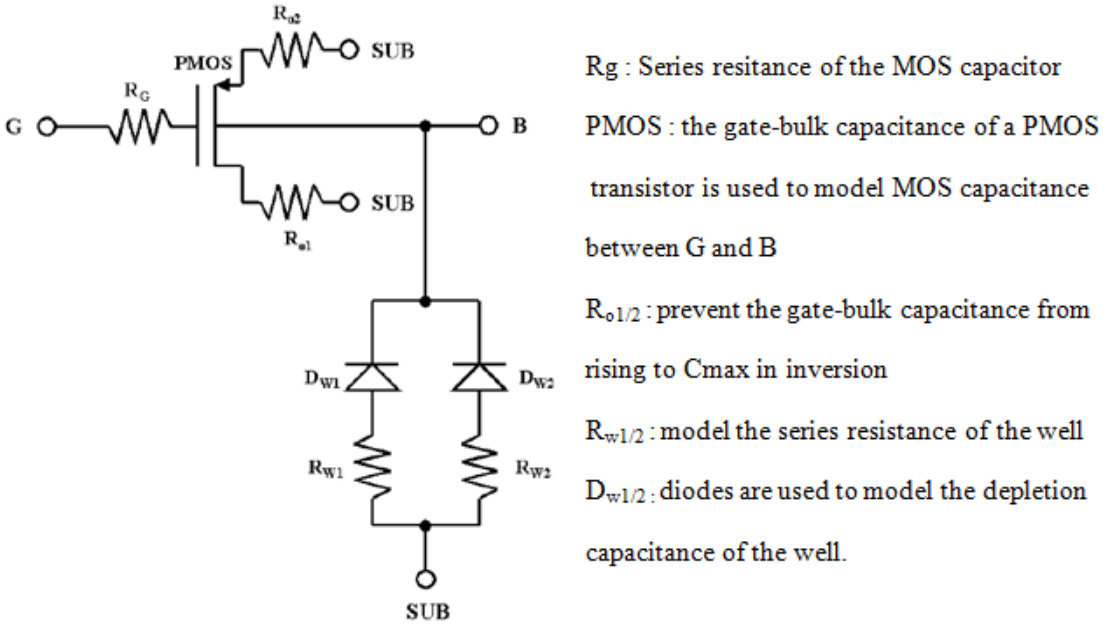

Figure 37 Subcircuit Model of Accumulation mode MOS varactor

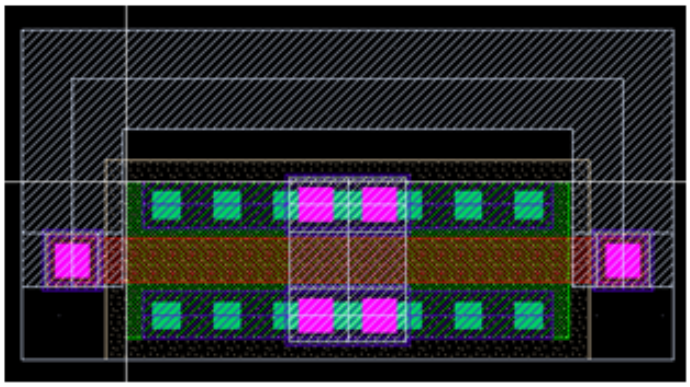

Figure 38 Layout of the A-MOS

Main parameters and Simulation results

Important electrical parameters were calculated using the impedance between gate and bulk ($Z=1/y_{11}$)

MOS Capacitance: $C = \frac{1}{-\omega.\mathrm{Im}(Z)}$

Series Resistance: $R=\mathrm{Re}(Z)=R_g$

Capacitance Tuning Range: $\gamma = \pm\frac{C_{max}-C_{min}}{C_{max}+C_{min}}$

Quality Factor: $Q = \left|\frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)}\right| = \left|-\frac{1}{\omega RC}\right|$

Where $\omega = 2\pi f$ $(f: frequency)$, Re(Z) and Im(Z) are the real and imaginary part of the impedance.

The C and R characteristics are independent of frequency. Q depends on frequency. The strong deviation in Q-V characteristics is due to the approximation of the nonlinear series resistance with a constant resistance. Table 9 shows measured C_{max}/C_{min} ratio, capacitance tuning range and minimum quality factor for different widths of varactor that is taken from AMS process documents. The width of the varactor that was used for the design is 158.4 µm.

W(μm)	C_{max}/C_{min}	γ (%)	Q_{min} (at 2.4 Ghz)
950.4	3.65	57.0	79.7
633.6	3.66	57.1	58.0
316.8	3.68	57.3	42.6
158.4	3.65	57.0	41.4

Table 9 Measured C_{max}/C_{min} ratio, capacitance tuning range and minimum quality factor [25]

The elements of LC tank were analyzed individually. The characteristics of a single AMS library varactor at 5.4 GHz are shown in Figure 39 and Figure 40. This varactor has a Cmax/Cmin about three over a tuning voltage of 2V. The quality factor has a maximum value of 60 and minimum value of 20, depending on the tuning voltage. The differential voltage between the varactors' nodes in the circuit is between -1 V and 1V, in this regard the simulations have been done in this range.

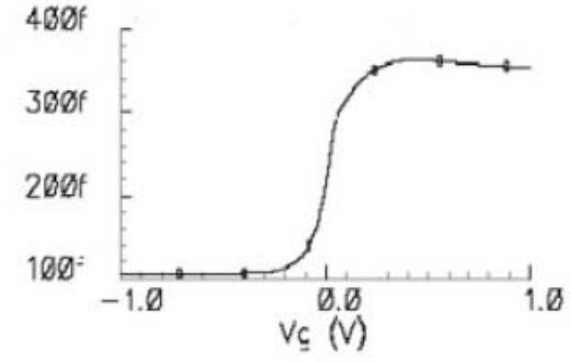

Figure 39 Varactor capacitance value versus voltage change

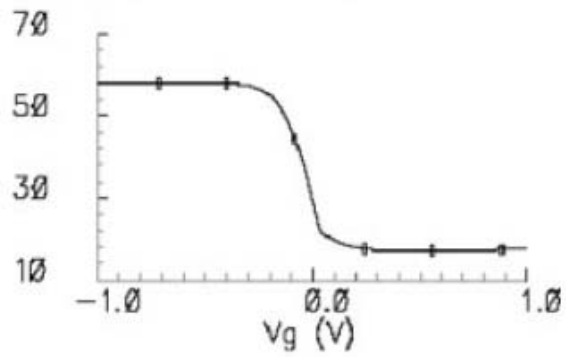

Figure 40 Quality Factor variation with voltage change

3.7 Design of VCO buffer

A buffer was typically placed between the VCO nodes and the actual load. This implementation was done to isolate the VCO and thereby protect the VCO from the load that otherwise would affect the VCO bias current and the VCO tank by contributing to the

capacitance, inductance and the loss of the tank. Through affecting these parameters, the load becomes able to influence the oscillation frequency of the VCO. The VCO load is typically constituted by either a PA, mixer, frequency divider etc. Furthermore, a VCO output buffer is necessary for measurement purposes on the VCO. Based on these arguments, a VCO buffer was designed in this design.

One of the requirements of the VCO buffer is that its input impedance must be large enough so that it does not influence the tank loss. Furthermore, it is desirable that the physical dimensions of the buffer FETs are kept at a minimum, thereby obtaining minimum parasitic capacitance that contributes to the tank capacitance. Initially, the buffer was designed for measurement purposes on the VCO and due to this fact the buffer load was specified as 50 Ω in parallel. The requirement of the output voltage swing of the buffer is to keep it within reasonable range. In contrast, no requirements were specified for the power consumption of the buffer.

The designed VCO output buffer sketched in Figure 41. The buffer was connected to the VCO nodes through capacitors that provided the desired AC coupling.

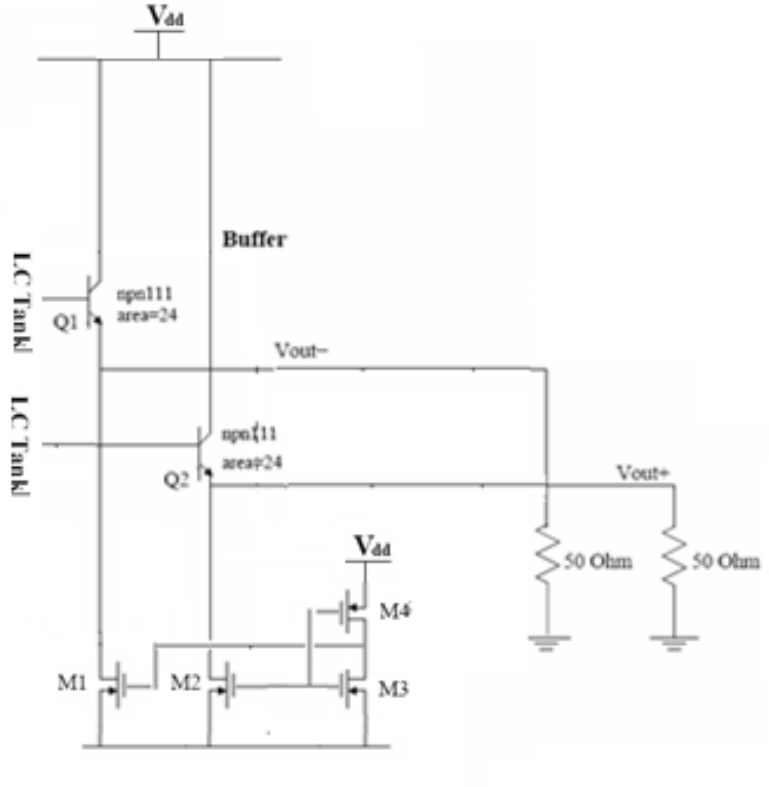

Figure 41 Buffer Circuit

Table 10 gives the buffer circuit component parameters. The current source circuit was designed to provide 9.06 mA current for buffering operation. The value of the current was found as there would be no clipping on the output signal for every five frequency bands. Table 10 gives the parameters of the buffer circuit. NMOSrf and PMOSrf are AMS library elements such as the other transistors, and their models are valid up to 6.

Component	L	W_f	N_f	W_{total}	Type	Device Area
M1,M2	0.35µm	8 µm	5	40 µm	nmosrf	-
M3	0.35µm	5 µm	1	5µm	nmosrf	-
M4	0.35µm	5 µm	11	55 µm	pmosrf	-
Q1,Q2	-	-	-	-	npn111	24

Table 10 Buffer circuit component parameters

3.8 Small Signal Analysis

Designing a complementary LC oscillator requires that the available design variables should be identified. These variables determine the specifications of the VCO submodules and thereby directly affect the performance of the VCO. The relevant variables are specified below.

Spiral inductor: inductance, L, and the corresponding Q-value.

Transistors: width of NMOS and PMOS FETs, Wn, Wp and the channel lengths L_n, L_p.

Fine tuning varactor: maximum value C_v, max and minimum value C_v, min.

Switch Circuitry: fixed capacitance and width of NMOS FET Wn and the channel length L_n

Load capacitance: C_{load}

Bias current: bias current in the oscillator core, I_{bias}.

In this particular design, the inductor parameters are not variable since a specific inductor was chosen for the purpose and thus the remaining design variables must be adapted to the inductor specifications such that the desired VCO performance could be obtained.

In addition to these variables, the VCO performance was likewise affected by undesired parasitic components that depended on the specified design variables. For instance, if the sizes of the FETs contained in the gm-stage are changed, the values of the associated parasitic capacitances of each FET will likewise change and thereby affect the total capacitance of the LC-tank. Consequently, the resonating frequency of the VCO will be influenced. In order to visualize the influence of parasitic components present in the oscillator circuit, the equivalent circuit model of the complementary LC oscillator is depicted in Figure 42.

The simplified VCO core schematic is shown in Figure 42(a), it includes on-chip inductors and on-chip varactors. The load (Z_{load}) usually is the input of BJT buffer circuits which is capacitive. The equivalent circuit model of the VCO (with the ON and OFF state of the switches) is shown in Figure 42(b), where the dashed lines in the middle represent either a common mode node or ground. The symmetric planar spiral inductor model of Figure 42(c) with identical RC loading on both terminals is used as a part of the tank model. The parasitic capacitance of inductors is represented by C_L, which is equal to $2C_s+C_p$. Rs is the parasitic resistance in series with inductance L. Rp represents the shunt resistance across the port and ground. The quality factor (Q_L) of the L-R series combination is then given by $Q_L=(\omega L)/R_s$, where ω is the operation frequency. The varactors were modeled with a capacitor Cv in series with a resistor Rv. In a similar way, output load is defined using a series combination of C_{load} and R_{load}. The quality factor for a capacitor (Q_C) is given as $Q_C = 1/(\omega RC)$, where ω is the operation frequency R is the parasitic resistance in series with capacitance C.

The parasitic capacitances of a MOS devices are C_{db}, C_{gs}, C_{gb} and C_{gd} [40]. The series resistance RMOS is mainly due to the substrate resistances associated with source/drain to substrate junction (C_{db}/C_{sb}) and gate to substrate (C_{gb}) capacitors. Large area substrate contacts are necessary to lower R_{MOS} to improve the quality factor of C_{MOS}. g_m and g_0 are small-signal transconductance and outputconductance of the transistors, respectively.

A VCO small signal equivalent circuit model including models of inductors, varactors, MOSFETs and loads is shown in Figure 42(b). This model can even be simplified as a parallel LC oscillator model as illustrated in Figure 42(d). Four parameters are used to describe a VCO circuit [41]: the loaded tank loss g_{tank}, effective negative conductance $-g_{active}$, tank inductance Ltank and tank capacitance C_{tank}. g_{active} are solely provided by the transistor transconductance, where:

$$g_{active} = g_m$$

If Q's of inductors and any capacitors (parasitic capacitors or varactors) are large enough (> 4), the L_{tank} and C_{tank} are approximately given as

L_{tank} = L (inductor switch on state)

L_{tank} = 2L (inductor switch off state)

$$C_{tank} = C_{mos} + C_L + C_{var} + C_{load} + C_{fix} \quad (28)$$

which;

$C_L = C_s + C_p$

C_{var}=100f-500f

C_{fix}=1.13pF, 600fF and 460fF (C_{fix} changes with the switch operations)

$$C_{load} = C_\pi + C_\mu.(1-K) \cong C_\pi \quad (29)$$

$$f_t = \frac{g_m}{2\pi.(C_\pi + C_\mu)} \gg 63Ghz \cong \frac{9{,}6.10^{-3}}{25.10^{-3}.2\pi.C_\pi} \gg C_\pi = 609fF \quad (30)$$

$$C_{mos} = 4C_{gd} + C_{db} + C_{gs} \quad (31)$$

$$C_{gd} = W.C_{ov} = 0.12\,{}^{fF}/_{\mu m}.150\mu m = 18fF \quad (32)$$

$$C_{ov} = \frac{\varepsilon_{ox}}{t_{ox}}.\Delta L.W = 0.12\,{}^{fF}/_{\mu m} \quad (33)$$

$$C_{gs} = W.C_{ov} + 2/3.W.L.C_{ox} = 158 \text{ fF} \quad (34)$$

$$C_{db} \approx 0\ fF$$

The oscillation frequency formula will be;

$$f_{osc} = \frac{1}{2\pi\sqrt{(S_1 L + S_2 L).(S_1.C_{mos} + S_v.C_{var} + C_{load} + S_i.(\mathrm{Cs} + \mathrm{Cp}) + (S_{11}.\mathrm{C_{fix1}} + S_{12}.\mathrm{C_{fix2}} + S_{13}.\mathrm{C_{fix3}}))}}$$

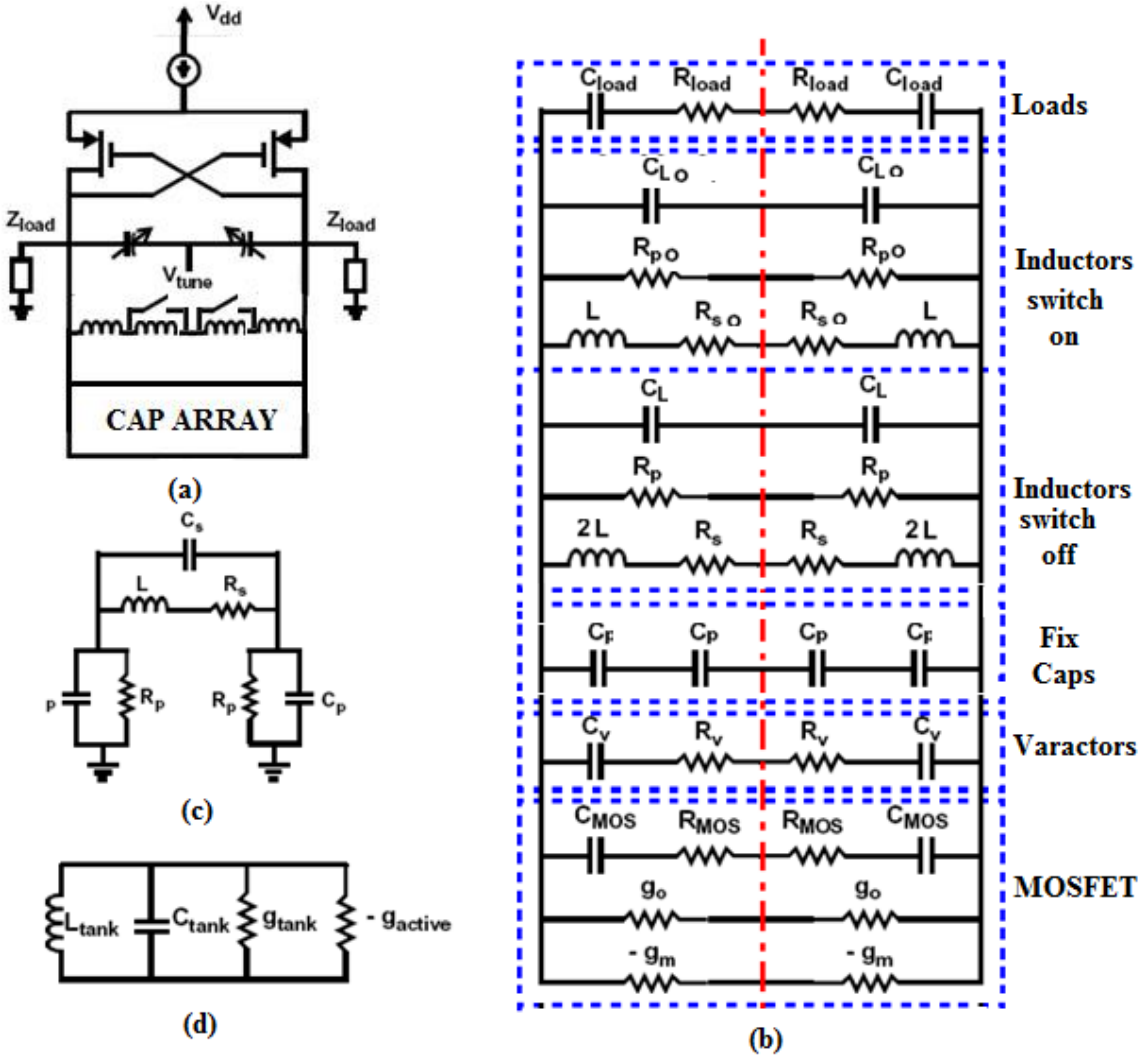

Figure 42 VCO small signal model. (a)Simplified VCO circuit schematic, (b)the equivalent small signal model for VCO, (c) equivalent circuit model for inductors and (d) a parallel LC oscillator model

The parameters that change with the operation of switches are shown at the Table 11.

	Band 1 2.2Ghz	Band 2 2.78Ghz	Band 3 3.5Ghz	Band 4 3.9Ghz	Band5 5.7Gz
S_1	1	1	1	1	1
S_2	1	1	0	0	0
S_v	1	5	5	5	5
S_{11}	1	1	0	0	0
S_{12}	1	0	1	0	0
S_{13}	0	0	1	1	0
S_i	0	0	0	0	0
C_{tank} simulated	2200fF	1600 fF	2028fF	1634fF	765fF
C_{tank} calculated	1800fF	1300fF	2300fF	1900fF	850fF

Table 11 Table for the Oscillation frequency formula

The loaded tank loss g_{tank} is due to the loss of transistor output conductance (g_0), transistor parasitic capacitance loss (g_{MOS}), inductor loss (g_L), varactor loss (g_v) and output load loss (g_{load}). Thus,

$$g_{tank} = g_0 + g_{mos} + g_L + g_v + g_{load} \tag{35}$$

.

The g_{MOS}, g_v, and g_{load} can be calculated from the general *RC* loss equation as $g = C.\omega/Q_C$, here *C* is capacitance from MOS, varactor or output load, and Q_C is their respective quality factor. The loss from inductors g_L is usually the dominant term and it is,

$$g_L = \frac{1}{R_p} + R_s/(L\omega)^2 \approx R_s/(L\omega)^2 \tag{36}$$

if $1/R_p$ is much smaller than the other term, which usually is the case. The VCO operation frequency ω is determined by L_{tank} and C_{tank}. At desired ω, the integrated VCO has to be optimized with minimum losses of g_0, g_{MOS}, g_L, g_v and g_{load}. In bulk CMOS technology, at frequencies lower than ~5 GHz, the dominant loss term is g_L, i.e. inductor loss.

One criterion for oscillation is $g_{active} = g_{tank}$. The transistor transconductance to satisfy this criterion is $g_{m,min}$. In order to guarantee oscillation, and also to have sufficient tank voltage swing to lower phase noise, each transistor must have transconductance $gm = k.g_{m,mi}$ where k is ~ 2 – 4 [42]. If only inductor loss is included in g_{tank}, then

$$g_m = k.\frac{R_S}{(L\omega)^2} = k.\frac{1}{R_S.{Q_L}^2} = k.\frac{1}{Q_L L\omega} \gg g_m = 5.4\ mA/V \quad (37)$$

3.9 Layout Design

Figure 43 shows the physical layout of the Multi-band VCO. The main design approach was reducing the parasitics and also sensitivity to parasitics. In order to minimize the even order distortion of the output waveform, the design of the layout was created to be as symmetric as possible.

The positive and negative oscillation nodes are the most critical nodes which must be designed to prevent capacitive and resistive parasitic effects. The parasitics at the oscillation nodes directly affect VCO performance parameters such as phase noise and oscillation frequency. In order to reduce the capacitance between metal layer and substrate, the top metal layer was used for the oscillation node connections. Also, for the oscillation node, the Metal-Insulator-Metal (MIM) capacitances were utilized because of their higher linearity and quality factor. It should be added that the quality factor of the inductor is dominant to determine the overall qualityfactor of the LC tank.

The thickness of the metal layer was designed considering their current capability. Moreover, the thicker lines increases the parasitic capacitance which probably mistunes the center frequency. Finally, the sharp turns and corners were avoided in the RF pads to prevent the degradation of RF signal from these regions.

The inductors, Varactors, Switch circuit array and the bias circuitry are the main subblocks of the layout design. Two series 1.04nH inductors were utilized instead of a single 2.08nH inductor to maintain the circuit symmetry. 2.5μm thick metal layer was used to form the spirals. The inductors were located to minimize path length as well as the magnetic effect.

The quality factor of the inductor, which is the most critical in the LC tank, was increased by using thick metal layer. The quality factor of the inductor changes from 8.7 at 2.4 GHz to 11.8 at 5.0 GHz. It has maximum value of 11.9 at 4.4GHz.

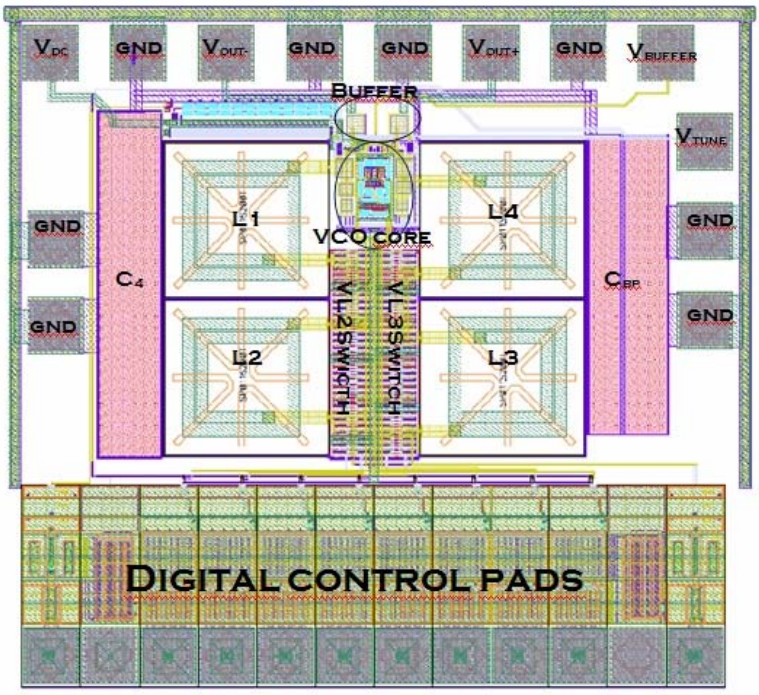

Figure 43 Multi-Band Layout

The oscillation obtained at the connection node of $-g_m$ circuitry, switched capacitance array, AMOS varactors and inductors. So the parasitics must be eliminated as much as possible at the VCO layout. Switched capacitance array was located between the output ports of two inductors. Furthermore, the inductors, AMOS varactors and $-g_m$ circuitry are located together in a limited area to reduce the parasitics as shown in Figure 44.

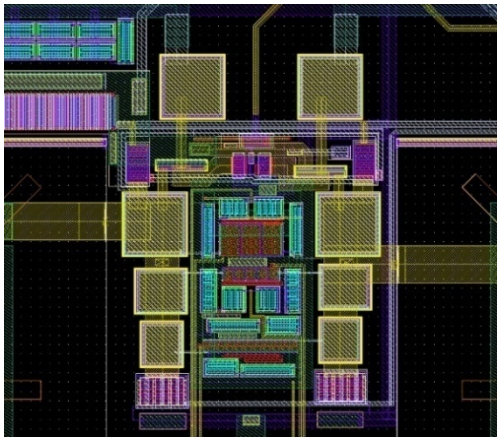

Figure 44 VCO layout detail

The layout of the Accumulation mode varactor is composed of parallel connected small capacitors. The capacitance-voltage characteristics are modeled by the gate-bulk capacitance of a PMOS transistor. The bias circuitry is formed by the transistors, low pass filter and by-pass capacitance. The maximum tail current of the LC tank is 6mA providing 3mA DC current for each branch. The poly capacitances were utilized for low pass filter and by-pass capacitors because of having much more capacitance value than CMIM. The resistors were formed by the second poly Si- layer of the process. Their resistance values are 140 kΩ at the Low pass filter and 10 kΩ for each branch at the capacitor switch. Detailed bias circuitry is illustrated in Figure 45

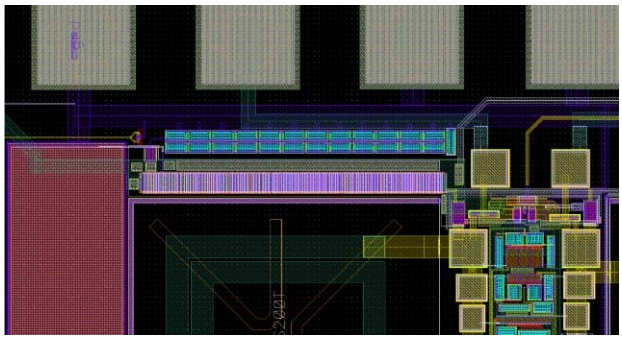

Figure 45 VCO layout detail bias circuitry.

The whole circuit has dimensions of 1.150 x 1.283mm^2 including RF, DC and digital pads occupying an area of 1.477mm^2 on Si die.

3.10 Simulation Results

Only C extraction has been done for the post-layout simulations because of the limitations of the simulator. The post layout simulation results of the VCO are presented in this section. The frequency bands are organized as 2.27-2.51 GHz, 2.48-2.78GHz, 3.22-3.53GHz, 3.48-3.91GHz and 4.528-5.7 GHz. First and second low frequency bands were provided by using inductor switches in OFF state (totally 4 inductors) and two switched capacitors were used for choosing first or second band. In the M5/M6 OFF state, the inductance that is seen from oscillation node is (doubled) approximately 2nH. The quality factor of 1nH differential inductor varies between 8.7 to 11.8 over 2.4GHz to 5GHz. The 3.22-5.7 GHz frequency bands are covered by two inductors (M5/M6 ON state) and three switched capacitors. The frequency bands versus tuning range plot are shown in Figure 46.

The VCO core draws current ranging changes from 3mA to 5mA according to the frequency bands, while the VCO buffer draws about 9mA from 3.3V power supply. Figure 47 shows the phase noise which varies from -122 to -110dBc /Hz over 2.2 GHz to 5.7 GHz. More importantly, the phase noise is essentially flat over the entire operating frequency band. The performance of the multi-band VCO is summarized in Table 12.

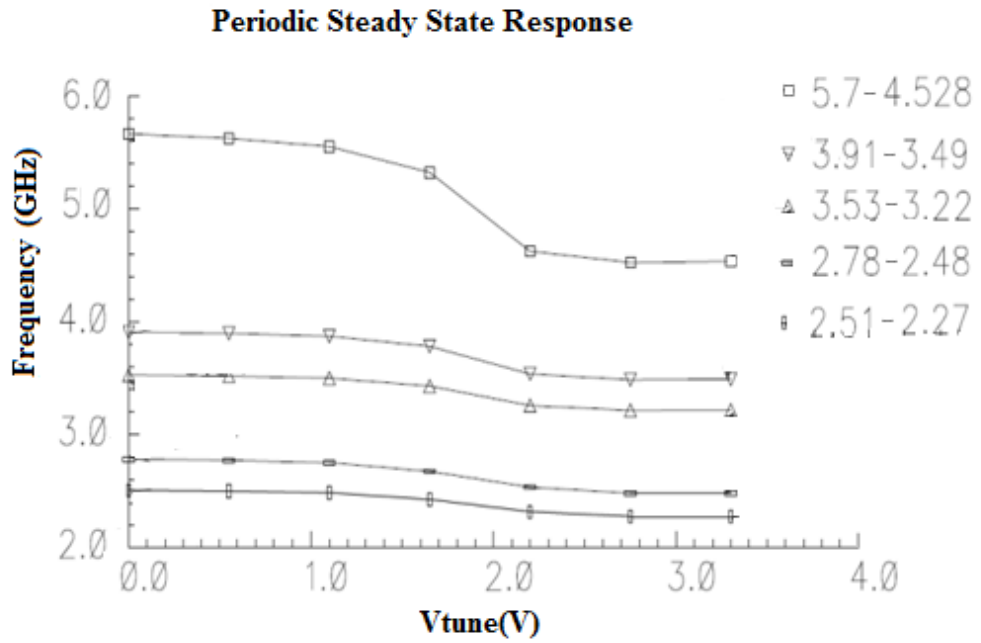

Figure 46 Frequency tuning range of Multiband VCO

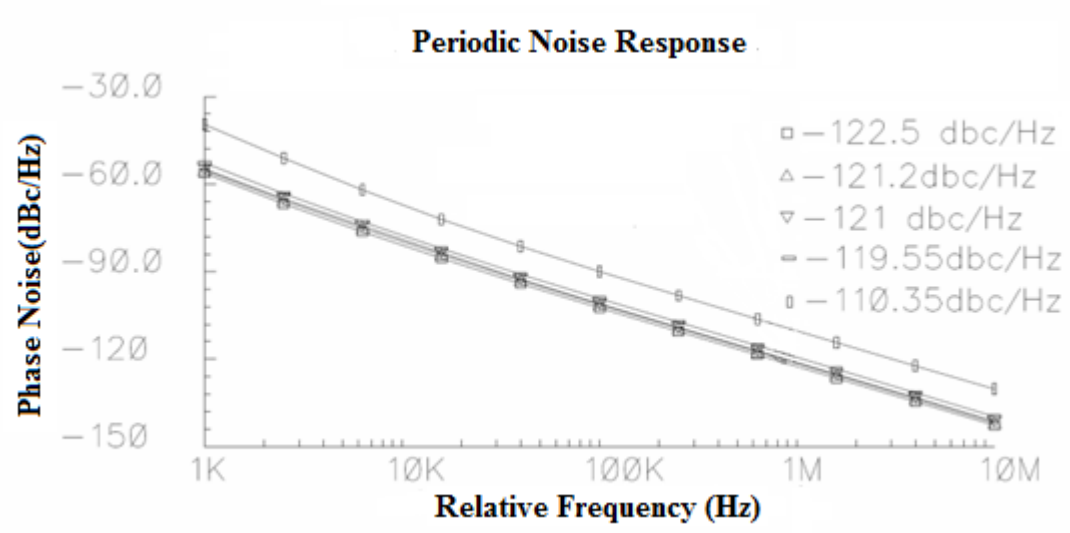

Figure 47 Phase Noise performance at three frequencies for multi-band VCO

A widely used figure of merit (FOM) [7] for the VCO is defined as,

$$FOM = L\{foffset\} - 20log\left(\frac{fo}{foffset}\right) + 10log\left(\frac{Pdc}{1mW}\right) \quad (38)$$

Here, L $\{f_{offset}\}$ is the measured phase noise at offset frequency f_{offset} from the carrier frequency f_0. P_{DC} is VCO power consumption in mW. The best measured FOM for the VCO is - 181.16 dBc/Hz at 3.91 GHz. Table 13 summarizes the performance of state-of-the-art wideband VCOs operating around 2.15 and 5 GHz. Power consumption of the buffer is excluded in comparison with wideband VCOs.

Table 12 The post layout performance summary of the VCO

	Band 1	Band 2	Band 3	Band 4	Band5
$V_{switchC1}$ (V)	3.3	3.3	0	0	0
$V_{switchC2}$ (V)	3.3	0	3.3	0	0
$V_{switchC3}$ (V)	0	0	3.3	3.3	0
$V_{switchL2,L3}$ (V)	0	0	3.3	3.3	3.3
V_{tune} (V)	0-3.3	0- 3.3	0-3.3	0-3.3	0-3.3
Tuning Range for Post-Layout Simulation	2.27-2.51	2.48-2.78	3.22-3.53	3.49-3.91	4.528-5.7
Simulated Frequency(GHz)	2.51	2.78	3.53	3.91	5.7
Tuning Range for Schematic Simulation	2.26-2.48	2.46-2.75	3.28-3.62	3.577-4.04	4.725-6.04
Phase Noise (dBc/Hz) at 1MHz for Schematic Simulation	-126.2	-124.3	-124.1	-122.5	-116.7
Phase Noise(dBc/Hz) at 1MHz for Post-Layout Simulation	-122.5	-121.2	-121	-119.55	-110.35
Vdd (V)	3.3	3.3	3.3	3.3	3.3
I_{vcore} (mA)	6.326	5.506	4.378	3.248	2.4
Output Voltage swing (V_{pp})	0.708	0.734	0.54	0.52	0.5

The output power of an oscillator is another concern in the design which was optimized for delivering sufficient power to the following stage in the transceiver architecture. Overloading the input of the next block is another critical design issue during optimization. The fundamental frequency power, that is obtained from 50-Ohm terminals at the output of the buffer, changes according to the frequency bands. The DC biasing conditions of the circuit alter by the operating frequency bands and as a result of these conditions, the differential peak

to peak voltage swing at the buffer output changes between 0.5 V and 0.743 V. The fundamental output power can be observed in Figure 48 that varies between -6.087 dBm and 0.992 dBm. The second and third harmonic output power need to be suppressed for uniform output signal. An average of suppression of -37.21 dBm in the second harmonic is shown in Figure 49. The third harmonic level is also adequately suppressed and has an average of -47.6 dBm throughout the 2.2-5.7 GHz band as shown in Figure 50.

Table 13 Comparison with published wideband VCOs

Ref.	Technology(μm)/ Results	Oscillating frequency (GHz)	Phase Noise(dBc/Hz)	Power (mW)	f_{offset}(MHz)/f_0(GHz)	FOM	Area (mm^2)
N. Fong[23]	0.13 SOI Measurement Results	3.065-5.612	-114.6	1V*2mA	1/3.065	-185.8	0.299
			-120.8	1V*2mA	1/5.612	-186.6	-
S.Kurachi [45]	0.35 SiGe BiCMOS Measurement Results	2.67-4.27	-111	4V*5.8mA	1/4.37		0.657
S.L. Jang[46]	0.18 CMOS Measurement Results	2.15-2.75	-121.45	3.88V*1.8mA	1/2.4	-180.2	-
		4.75-4.99	-118.49	3.1V*1.8mA	1/4.8	-184.6	-
P. Vaananen [43]	0.35 BiCMOS Measurement Results	3.3-5.3	-113	2.5V*14,6mA	0.6/4.4	-174.7	1.5125
J. Maget[44]	0.25 CMOS Measurement Results	3.28-4.11	-117	2.5V*3mA	1/4	-180.2	1
Q.D.Bui[47]	0.18 CMOS Measurement Results	2.78-3.78	-126.5	1.8V*5.7mA	1/2.83	-185.4	0.806
			-122.7	1.8V*4.9mA	1/3.77	-184.8	-
This Work	0.35 SiGe BiCMOS Post-Layout Simulation Results	2.27-2.51	-122.5	3.3V*6.326mA	1/2.51	-177.31	1.477
		2.48-2.78	-121.2	3.3V*5.506mA	1/2.78	-178.38	-
		3.22-3.53	-121	3.3V*4.378mA	1/3.53	-180.45	-
		3.48-3.91	-119.55	3.3V*3.248mA	1/3.91	-181.16	-
		4.528-5.7	-110.35	3.3V*2,4mA	1/5.7	-176.48	-

The power dissipation is a key performance parameter of the VCO design and it is minimized with proper DC bias. The HBTs, which were utilized for buffering (Q_1 and Q_2) should have larger emitter widths ($24\mu m^2$) to obtain better isolation from the measurement equipment. Considering the biasing constraints and oscillation conditions, the VCO core draws an average of 4.37mA from current source whereas 9mA is dissipated in the buffer circuitry. The average current drawn from the 3.3V supply is 13.37mA, which means a DC power consumption of 44.12mW.

According to the Table 13, the phase noise performance of the VCO in each frequency bands are above the average of the other wideband VCOs. This work consumes less power than the other 0.35 SiGe BiCMOS VCOs. Also, the figure of merit for the VCO has an excellence when compared with same technology VCOs. The FOM and area abandonments are not major concern on the overall comparison with the others, if the advantage of operating in 5 frequency sub-bands in a wideband (2.27-5.7 GHz) is taken into account.

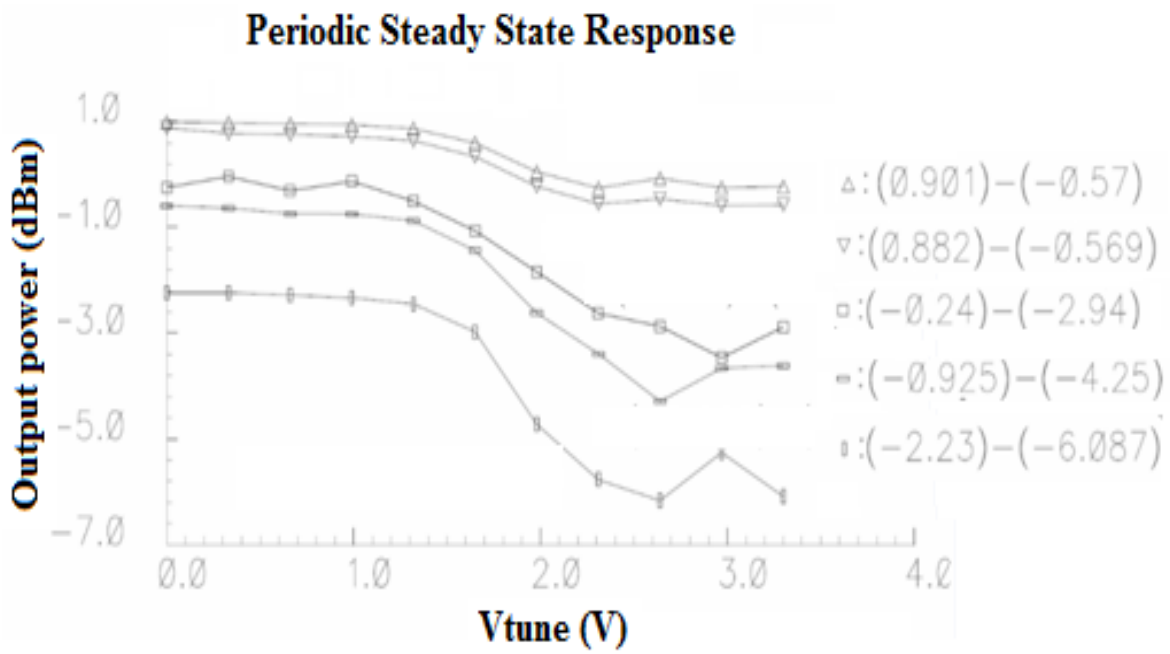

Figure 48 Fundamental frequency output power vs. tuning voltage

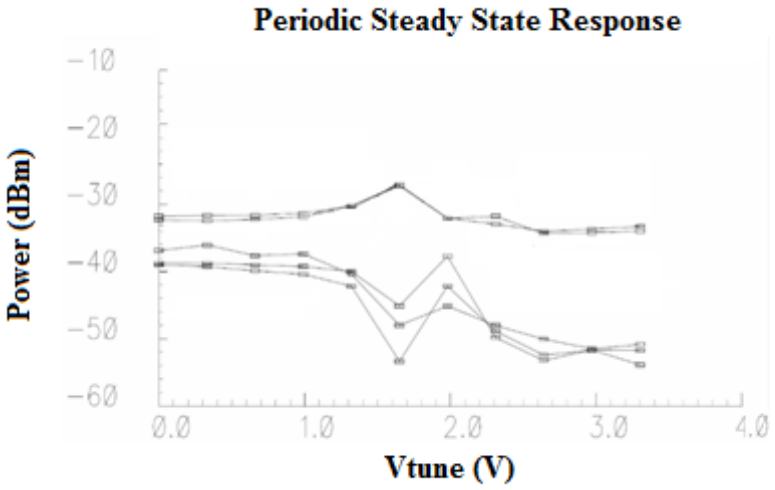

Figure 49 Second harmonic output power vs. tuning voltage

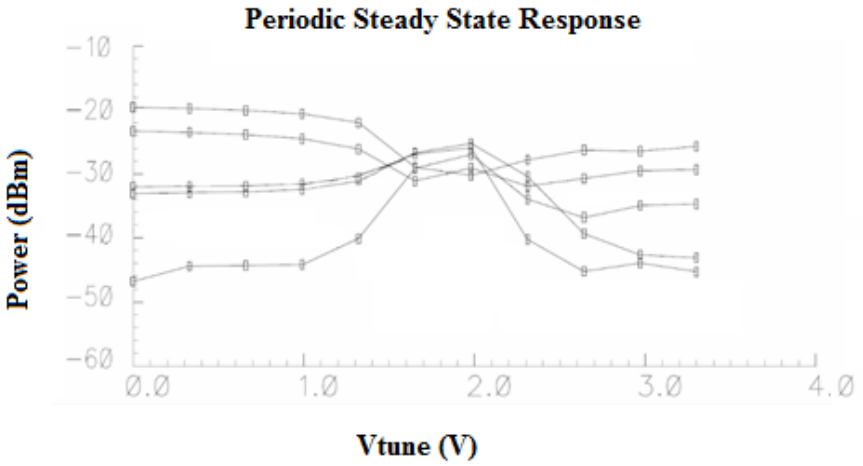

Figure 50 Third harmonic output power vs. tuning voltage

3.11 Measurement Results

In this part, the measurement process and results of VCO circuit, in whose the layout and postlayout simulations have been performed by using AMS 0.35um SiGe BiCMOS technology process and design rules, are presented.

The die, which includes the VCO of concern, a PA and some matching circuits, is shown in Figure 51 . Die area is 6.25 mm^2. The VCO circuit has nearly quarter area of the die (1.477mm^2). Much closer view of multi-band VCO could be seen from the Figure 52.

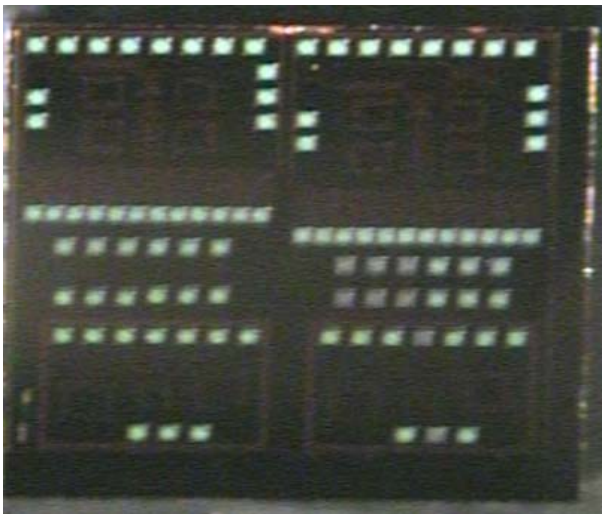

Figure 51 The fabricated chip

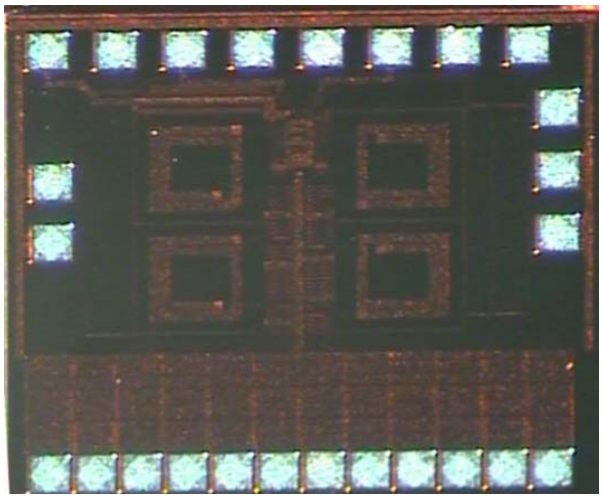

Figure 52 The multi-band VCO part of the chip

The measurement setup was prepared in order to test the DC characteristics of the VCO as shown in Figure 53. The Multi-band operation was provided with 15 DC supply, 2 Vcc, 1 GND and 2 RF port as mentioned before in design sections. For the minimum operation, chip needs four DC probes (2 Vcc, 1 Vin and 1 Vdc), and one RF probe that contains two ground probes and one RF output. The RF ground was connected to circuit ground in layout, thereby there is no need to connect DC ground to the circuit separately. The total current that is drawn from 3.3 Vcc voltage of the circuit is 20 mA. This means 66 mW DC power consumption which is reasonable when compared with the consumption in postlayout simulation (72.6 mW). Also the current of buffer circuit was measured as 9 mA while this value is 9.06 mA according to the postlayout simulation.

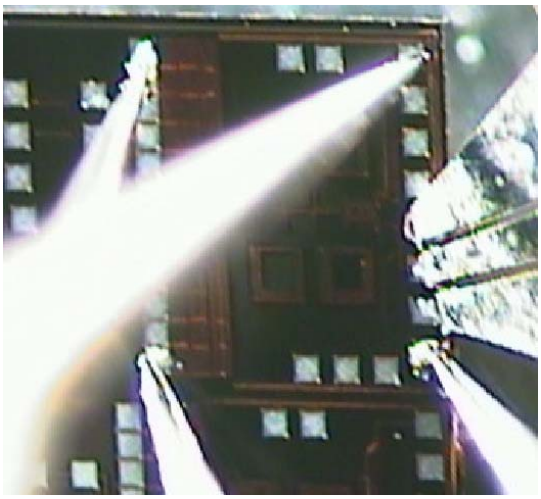

Figure 53 The measurement setup

As a second measurement setup, a package die is prepared to obtain much more exact results. Die is mounted to the package base with a conductive material in order to connect die base to ground as shown in Figure 54. Afterwards, pads are connected to package pins by using wire bond technique. Much closer view of the package is presented in Figure 55. VCO pads are connected to the pins apart from six RF probe pads.

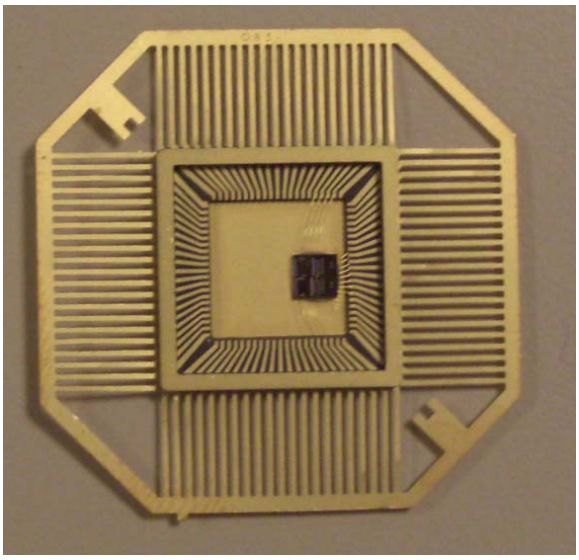

Figure 54 Die Package

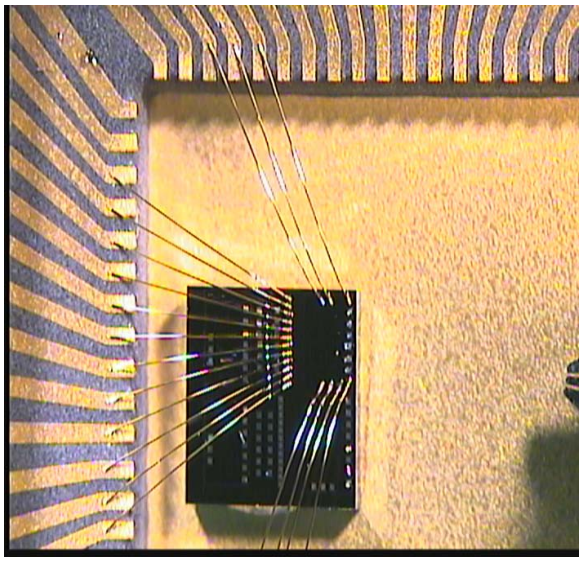

Figure 55 Closer view of Package

DC supply voltages are provided by using Agilent E3631A triple output DC power supply. Measurement setup which is consists of RF probe, board and supply voltages is shown in Figure 56 Measurement Setup. Moreover, Figure 57 presents much closer view of the measurement setup.

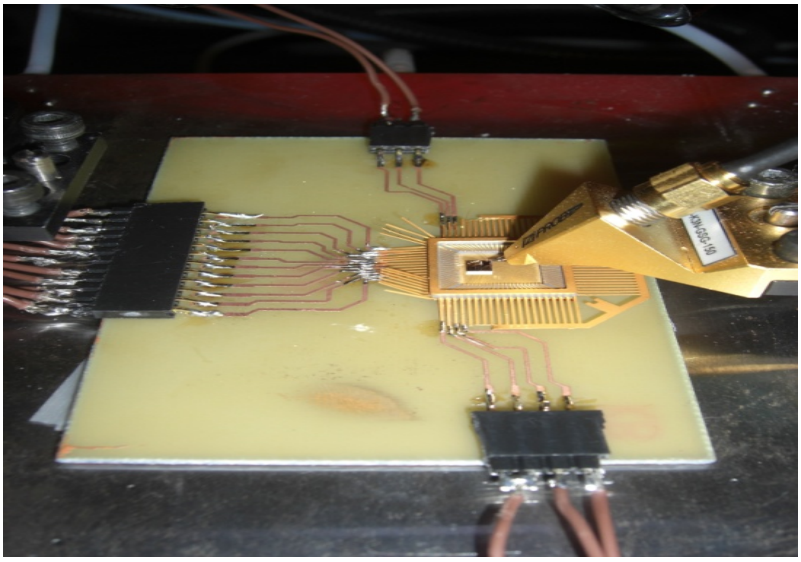

Figure 56 Measurement Setup

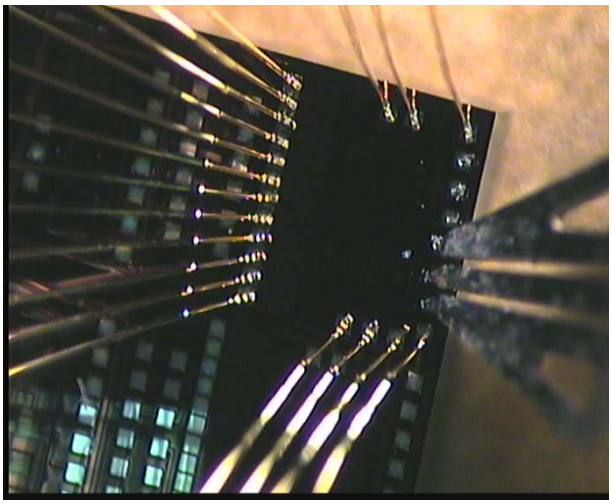

Figure 57 Closer view of Measurement Setup

As an measurment results, the total current that is drawn from 3.3 Vcc voltage of the circuit is 23 mA. This means 75.9 mW DC power consumption which is reasonable when compared with the consumption in postlayout simulation (72.6 mW). Also the current of buffer circuit was measured as 8 mA while this value is 9.06 mA according to the postlayout simulation.

CHAPTER 4 CONCLUSION AND FUTURE WORK

This thesis presents a study on designing a multi-band multi-standard voltage controlled oscillator and its simulation and measurement results. The target applications are wireless local area networks (802.11 a/b/g/n WLAN) and wireless metropolitan area networks (802.16 WMAN standard). The flow of the thesis starts with researching operating frequencies of these communication standards. After that, other important specifications such as phase noise, current consumption, tuning range and design issues such as inductor and capacitor switch , -Gm, buffer, LC tank circuits were formed from the published VCO papers and IEEE standard documentations. The challenge of designing multi-band VCO is working in a wide frequency band. As the frequency increases, the parasitics of the circuit start to dominate the operation of the VCO i.e the oscillation frequency. The important part relates to wide range operation in this thesis. For multi-band operation that starts from 2.2 GHz to 5.7GHz, a new approach have been introduced. The idea was implementing both inductor switching and capacitor switching circuit in the same VCO tank.

The Multi-band differential LC VCO was designed utilizing 0.35µm SiGe BiCMOS technology. Based on the post layout simulation results, the VCO can be tuned using a DC voltage of 0 to 3.3V for 5 different frequency bands with a maximum bandwidth of 1.36 GHz and a minimum bandwidth of 300 MHz. The designed and simulated VCO can generate a differential output power of between 0.992 dBm and -6.087 dBm with an average power consumption of 44.21mW including buffers. The average second and third harmonics levels were obtained as -37.21 dBm and -47.6 dBm, respectively. The phase noise of -110.45 to -122.5 dBc, simulated at 1 Mhz offset, can be obtained through the frequency of interest. Additionally, figure of merit (FOM) , that includes all important parameters such as phase noise, power consumption and division of operating frequency to offset frequency, is between -176.48 and -181.16 being comparable with the other current VCOs. The main advantage of this work in comparison with the other VCOs is covering 5 frequency bands starting from 2.27 to 5.76 Ghz without FOM and area abandonment. Moreover, the switching inductor and capacitor models in this circuit were used separately in other wideband VCOs. The designed topology, which combines switching inductors and capacitors together in the same circuit, is a novel approach for wideband VCOs.

The future work includes designing a new inductor that have a better quality factor and implementing a digital circuit that controls the switches switches to reduce DC I/O pad requirements. Also to have tuning capabilitty over DC biasing would help to search for better operation conditions. As mentioned before, the design is started with choosing inductor from the limited AMS inductor library. The inductor that has best quality factor and minimum value of inductance have been chosen for multi-band VCO. A new inductor designed with using CAD tools and modeled properly, could have a better quality factor. Hence, VCO could have a better phase noise performance since the losses in the inductor dominates rather than the other components in the circuit. Moreover, reducing the losses can help the circuit to work with less current; thereby VCO could operate in the same bands with lower power consumption. By the help of the digital part, the desired frequency band or frequency could be provided by lower control voltages.

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