Design of a tunable multi-band differential LC VCO using 0.35 μm SiGe BiCMOS technology for multi-standard wireless communication systems

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ABSTRACT

In this paper, an integrated 2.2–5.7 GHz multi-band differential LC VCO for multi-standard wireless communication systems was designed utilizing 0.35 μm SiGe BiCMOS technology. The topology, which combines the switching inductors and capacitors together in the same circuit, is a novel approach for wideband VCOs. Based on the post-layout simulation results, the VCO can be tuned using a DC voltage of 0 to 3.3 V for 5 different frequency bands (2.27–2.51 GHz, 2.48–2.78 GHz, 3.22–3.53 GHz, 3.48–3.91 GHz and 4.528–5.7 GHz) with a maximum bandwidth of 1.36 GHz and a minimum bandwidth of 300 MHz. The designed and simulated VCO can generate a differential output power between 0.992 and −6.087 dBm with an average power consumption of 44.21 mW including the buffers. The average second and third harmonics level were obtained as −37.21 and −47.6 dBm, respectively. The phase noise between −110.45 and −122.5 dBc/Hz, that was simulated at 1 MHz offset, can be obtained through the frequency of interest. Additionally, the figure of merit (FOM), that includes all important parameters such as the phase noise, the power consumption and the ratio of the operating frequency to the offset frequency, is between −176.48 and −181.16 and comparable or better than the ones with the other current VCOs. The main advantage of this study in comparison with the other VCOs, is covering 5 frequency bands starting from 2.27 up to 5.76 GHz without FOM and area abandonment. Output power of the fundamental frequency changes between −6.087 and 0.992 dBm, depending on the bias conditions (operating bands). Based on the post-layout simulation results, the core VCO circuit draws a current between 2.4–6.3 mA and between 11.4 and 15.3 mA with the buffer circuit from 3.3 V supply. The circuit occupies an area of 1.477 mm^2 on Si substrate, including DC, digital and RF pads.

1. Introduction

The stable growth in wireless communications market has engendered the interoperability of various standards in a wide frequency range from 100 MHz up to several GHz. This frequency range encloses numerous wireless applications such as GSM, Bluetooth and WLAN. Additionally, the adoption of UltraWide-Band (UWB) and WiMAX is likely to bring challenging tasks to RFIC designers for accurate and efficient utilization of this frequency range. Therefore, an agile wireless system needs smart RF front-ends to function properly in such a crowded spectrum. Besides agility and intelligence, such a communication system (GSM, WLAN, Global Position Systems, etc.) needs to meet the demands of several standards in a cost-effective way [1].

The main concern while choosing RF technologies for wide ranging communication applications is optimization for performance or/and cost. This leads to the exploitation of Si-based technologies when cost and integration are the major concerns. The convenience of integration of high performance HBTs with the state-of-art CMOS and passive elements is the main advantage of SiGe-BiCMOS technology against the other technologies [1]. As a consequence of second and third generation wireless systems, multi-band and multi-standard mobile communication systems are desired. Recent transceiver components should also cover the frequency band of various systems. With the introduction of UltraWideBand, communication standards operate in the frequency range of up to 10 GHz. As a result, the demand for multi-standard RF transceivers which put various wireless and cordless phone standards together in one structure has been rised. Hence, narrowband voltage controlled oscillators, one of the main blocks in the transceivers, replaced with single low-noise wideband VCO. The demand for multi-standard RF transceivers gives a key role to reconfigurable wideband VCO operation with low-power and low-phase noise characteristics [2–4].

For multi-standard operation, a VCO needs to cover a wide frequency range. The LC-tank VCO topology is the most popular implementation among others due to its higher spectral purity. Typically, in LC-oscillators varactors are used for continuous frequency tuning. However, higher tuning sensitivity means higher sensitivity to noise and disturbances on the control

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voltage. Moreover, larger area varactors, such as MOS-based ones, convert harmless amplitude noise into harmful phase noise. To achieve wider tuning range and linearity in integrated VCOs, accumulation-mode MOS varactors (AMOS) are commonly preferred since p-n junction varactors and inversion mode MOS varactors have limited tuning range and non-linear behavior [5].

Various material systems and transistor technologies such as InGaP/GaAs HBT, SiGe BiCMOS, Si CMOS, and silicon-on-insulator (SOI) CMOS have been implemented to meet the specification of multi-communication standards. A CMOS dualband VCO realized with 0.18 μm CMOS technology, operating at 2.15–2.756 GHz and 4.756–4.996 GHz [6]. The VCO demonstrated a phase noise of 121.45 and 118.4 dBc/Hz at 1 MHz offset and the frequencies of 2.4 and 4.86 GHz. Tuning range of this work was relatively low when compared with standard's 5–6 GHz coverage. Moreover, two different LC tank circuit used to provide dual-band capability, not a cost/area effective. A remarkable work was performed using 0.13 μm SOI CMOS, demonstrating a 3.065–5.612 GHz coverage with −114 dBc/Hz phase noise at 1 MHz offset while drawing 2 mA from 1 V supply [7]. These performances were achieved using the advantage of SOI structure and eliminating the adverse effect of AMOS varactors by band switching topology [7]. From the application perspective, SiGe BiCMOS technology offers more advantages [8,9]. This is because it combines the cost and integration advantages of Si material system along with the performance advantages of SiGe HBTs. Moreover, because of vertical structure of HBTs, phase noise performance is expected to be lower [10].

The target bands for his work were obtained from the standards, widely used for wireless communication, such as IEEE 802.11a, 80211b, 802.11g, 802.11n, 802.16 and HIPERLAN/2. IEEE 802.11a devices and many wireless devices use Unlicensed National Information Infrastructure (U-NII) band, operating around 5 GHz. In USA (FCC) and Europe (ETSI), the operating frequency band for 802.11b is in the range of 2.4–2.4835 GHz. Additionally, it is allocated by the regulative authority of Japan as 2.471–2.497 GHz. For higher data rate channels in the USA, three channels centered at 2412, 2437 and 2462 MHz have been allocated [11]. IEEE 802.11g is the 802.11a Standard which operates in the 2.4 GHz Industrial, Scientific and Medical band. IEEE 802.11n is an amendment version of previous wireless local area network standards such as IEEE 802.11b and IEEE 802.11g. For countries, excluding the USA, the wireless LAN may or may not be compatible with the 802.11 standards. But it is worthwhile to briefly introduce another important wireless LAN standard: high performance local area network type 2 (HIPERLAN/2) standards. HIPERLAN/2 operates in two sub-bands 5.15–5.35 GHz, and 5.47–5.725 GHz. The OFDM system in HIPERLAN/2 is similar to 802.11a [12]. In order to give wireless access to the urban areas, IEEE 802.16a wireless Metropolitan Area networks (WMANs) standard was introduced, first time on 1 April 2003 [13]. This system utilizes frequencies from 2 to 11 GHz. There are licensed and un-licensed bands in the wide frequency band. The licensed bands are 2.3 GHz (WCS), between 2.5 and 2.7 GHz (MMDS), between 3.5 and 3.7 GHz (ETSI), and unlicensed bands are 2.4 GHz (ISM) and 5.8 GHz (U-NII) in which WLANs operates as well [11–14].

In this work, we aim to present the combination of tuning and switching methodologies and compare the finding with alternative approaches in the literature. We selected an integrated LC-tank, differential, $-G_m$ VCO as circuit topology, capacitor and inductor switching approach for band selection and finally AMOS varactor for fine-tuning within each band. This combined approach has yielded a figure-of-merit (FOM) values that are better and/or compatible values when compared to other approaches for obtaning multi-band operation in literature. Following sections presents the VCO design in detail, giving the design issues for the core, buffer, and LC tank in Section 2. Section 3 analyzes and discusses the post-layout simulation results. Section 4 describes the layout issues and approaches of the circuit. Finally, Section 5 is the conclusion of this work.

2. Multi-band VCO topology

2.1. Circuit topology

Ring oscillators [15], multi-vibrator oscillators [16] and resonator (LC)-based oscillators [17] can be used as an RF VCO topology. Multi-vibrator oscillators are utilized for very high tuning ranges. Ring oscillator topology that is composed of odd number of inverter stages also has again high tuning range. However, these oscillators usually have less spectral purity than their LC counterparts. LC-based oscillators are most compatible topology for low phase noise designs. LC resonator, that determines the frequency of oscillation, forms part of the feedback mechanism used to obtain sustained oscillations. In a practical circuit, oscillators will die away unless feedback is added in order to sustain the oscillation. Feedback (or negative resistance) is usually provided by tapped inductor and amplifier (Hartley oscillator), two amplifiers ($-G_m$ oscillators) or tapped capacitor and amplifiers (Collpitts oscillator). Due to the difficulties in IC tapped-inductor implementations Hartley topology is not usually prefered. Although there are some successful realizations of Collpitts configurations $-G_m$ topology generally results in higher performance wireless applications [16]. Differential LC–G_m configuration is chosen for Multi-band VCO because of meeting the phase noise requirements of communication standards and the topological advantages. In an RF transceiver block, VCO usually drives the mixer, most of which is composed of differential Gilbert Cell. Moreover, differential topology enhances the output power at the expense of increased power consumption, larger chip area and increased complexity. Finally, differential LC–G_m configuration provides a higher common-mode rejection ratio (CMRR), thus higher linearity [18]. NMOS, PMOS, or complementary cross-coupled designs can be used as LC VCO circuit topologies for wideband VCOs. Because of consuming less current to compensate for losses in the tank and having lower up conversion factor of flicker noise, a complementary cross-coupled VCO is quite attractive. However, it reduces the voltage headroom of the current source, and introduces more parasitic capacitance (C) as well as noise sources to the tank [19]. A non-complementary topology is used in this project.

For the same transistor size and gate over drive voltage, $1/f$ (flicker) noise of PMOS transistors is usually smaller than that of NMOS transistors in one order of magnitude [20]. For the same bias current and transconductance (gm), PMOS $1/f$ noise should be even lower because a PMOS transistor has lower mobility, so it needs larger size to keep the same transconductance compared to an NMOS transistor. In addition, a PMOS transistor has less hot carrier effect. Hence, PMOS VCOs can achieve better phase noise performance than NMOS VCOs as described by the modified Leseson's Formula [7]

$$L(\Delta f, k_v) = 10\log\left\{\left(\frac{f_0}{2Q\Delta f}\right)^2\left[\frac{FkT}{2P_s}\left(1+\frac{f_c}{\Delta f}\right)\right]+\left(\frac{k_v v_{yz}}{2k_{LC}\Delta f}\right)^2\right\} \quad (1)$$

Here, Q is the quality factor, Δf is the frequency offset from the carrier, F is the noise factor, k is the Boltzmann's constant, T is the temperature, P_s is the RF power produced by VCO, f_c is the Flicker noise corner frequency, f_0 is the frequency of oscillation, v_n is the common mode noise voltage, k_v is the varactor gain and k_{LC} is a

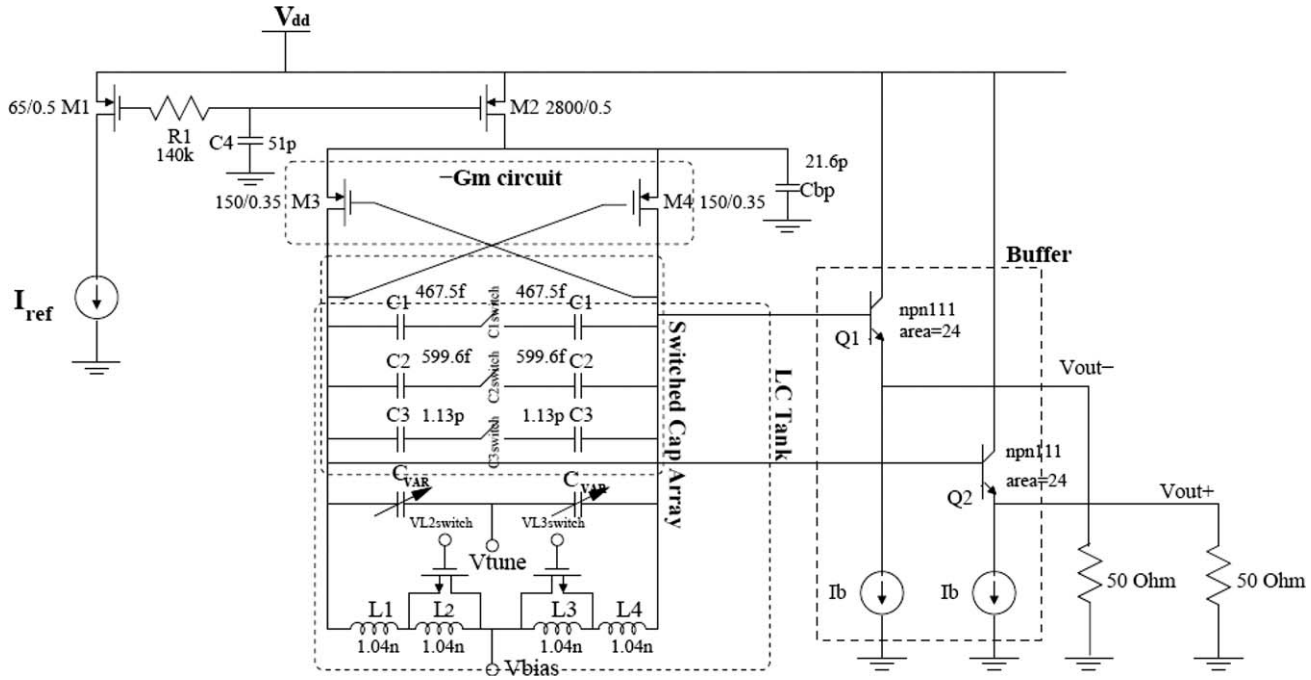

Fig. 1. Multi-band VCO schematic including LC switched resonators.

constant that is a function of L and C of the resonator [21]. Furthermore, all-PMOS VCOs with top-biased current sources provide excellent suppression of power supply noise and minimize noise disturbances from the current source to the varactor through the use of ground referenced tank. In summary, an all-PMOS VCO topology is the most appropriate one in terms of low phase noise performance, because it has minimum intrinsic and extrinsic sources of noise [22]. Thus, PMOS VCOs have better phase performance—approximately 4 db in the $1/f^2$ region or 9 db for offset frequencies from 10 kHz to 10 MHz—than NMOS VCOs [23].

The design is classified into three parts as the core, the LC tank, and the buffer, and is discussed in detail below.

2.2. VCO core

A fraction of 0.35 μm four-metal double-poly SiGe BiCMOS process of Austria Microsystems (AMS) with a thick metal option is used as a design technology. This technology has high-speed SiGe HBTs with 59 and 63 GHz f_t and f_{max} values, respectively [24].

Multi-band, differential $-G_m$ LC configuration is given in Fig. 1. It consists of three parts, the LC tank (L and $C_{var,}$ switches) the $-G_m$ circuit (M_3, M_4) and the buffer (Q_1, Q_2). The PMOS transistors in the $-G_m$ part are used to provide additional negative resistance. Si MOSFETs are utilized for the $-G_m$ cell instead of bipolar transistors. The reason is that Si MOSFETs benefit from the lower transconductance and capacitance per unit gate width and from the layout dependence of gate resitance to achieve lower noise figures than those of SiGe and InP HBTs of comparable or higher f_T and f_{MAX} [25]. As seen from Fig. 1 LC tank circuit consists of switched inductors, accumulation mode MOS varactors, and switched capacitor array. Accumulation-mode MOS varactors have been chosen instead of IMOS varactor for tuning concept due to the best overall performance on phase noise and power consumption [26,27]. Frequency tuning range is divided into 5 sub-bands by using switched inductor and capacitor to achieve a wide frequency range with a low tuning sensitivity.

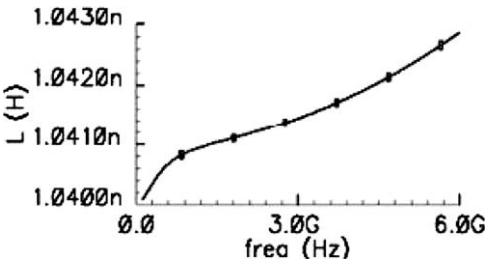

Fig. 2. Inductance value of AMS library inductor.

2.3. LC tank

The quality factor of the overall tank circuit is determined from the parasitic conductances of capacitance and inductance. Since accumulation mode MOS varactors have relatively higher Q values than on-chip inductors, inductor Q is the main determining factor of the overall Q of the tank circuit.

Inductors and capacitors in LC tank is simulated and analyzed individually. AMS library inductor is used as inductor of the LC tank and its characteristics can be observed in Figs. 2 and 3, indicating an inductor value of 1.04 nH with a quality factor varying from 8.7 at 2.4 GHz to 11.8 at 5 GHz. At lower frequencies, coupling between both inductors increases in proportion to mutual inductance and frequency. At higher frequencies, above 10 GHz, shunt parasitics will dominate reducing overall coupling. Also resonator coupling is proportional to the quality factor of inductor.

The elements of LC tank is analyzed, individually. The characteristics of a single AMS library varactor at 5.4 GHz are shown in Figs. 4 and 5. This varactor has a C_{max}/C_{min} ratio of about three over, a tuning voltage range of 2 V (Fig. 4). The quality factor has a maximum value of 60 and minimum value of 20, depending on the tuning voltage (Fig. 5). The differential voltage between the varactors' nodes in the circuit is between −1 and 1 V that is also the range of our simulations.

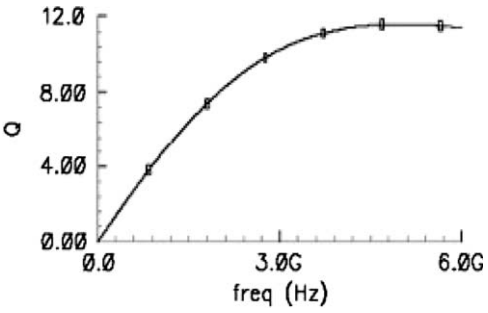

Fig. 3. Quality factor of the AMS library inductor.

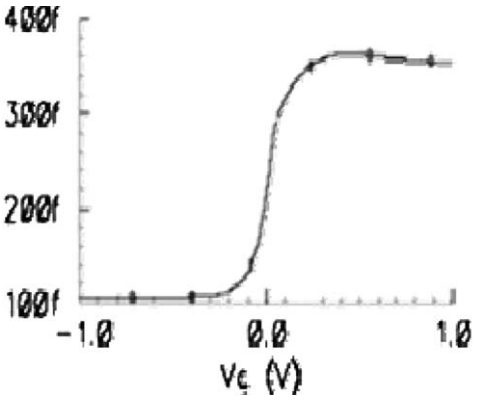

Fig. 4. Capacitance value of AMS library varactor.

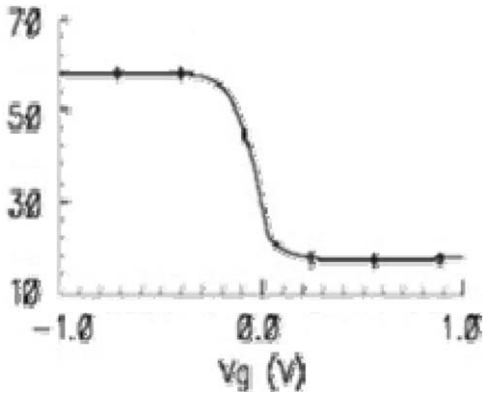

Fig. 5. Quality factor of the AMS library varactor.

Multi-band tuning concept in a wideband range has been attempted by utilizing switched inductor with poor phase noise outcome [23]. The switched inductor concept, shown in Fig. 1, is used for increasing the tuning range and achieving low phase noise. Total inductance between ports 1 and 2 is determined by the transistors' ON- and OFF-state. At the OFF-state, total inductance is approximately sum of the L1 and L2. When transistor is ON, the branch is shorted and inductance seen from port 1 is decreased to L1. Also, the capacitance seen from L1 side is reduced because of short-transistor capacitances and parasitic capacitances associated with L1 and L2 with respect to the ground. By the switching method, as applied in this work, one can decrease the inductance and capacitance, simultaneously [28]. This tuning/switching ability also eases the trade-off phase noise and power consumption [29], when compared to using only switched capacitors [30].

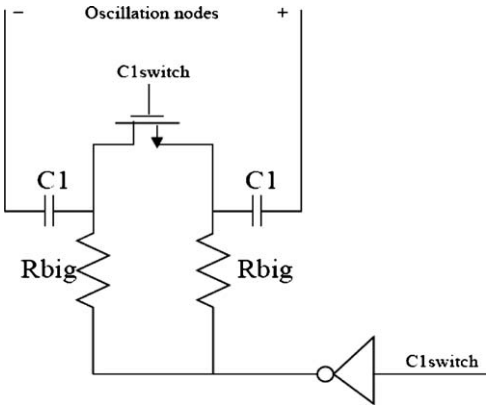

Fig. 6. Improved differential switched-tuning circuit.

In addition to the switched inductor, improved switched capacitance model has also been applied, in this work, for multi-band operations. The advantage of this model is getting a better phase noise when compared to the traditional models. The switched-capacitor tuning circuit is illustrated in Fig. 6. It is based on using one transistor, instead of two, to switch two AMS library capacitances. The quality factor of each capacitor is doubled due to a decrease in ON-resistance of the switched branch, which in turn, improves the phase noise, when compared to the use of one transistor for one capacitor. Resistors are used in Fig. 6 for guaranteeing transistor's OFF-state and the maximum gate to source (and drain) voltage during the ON-state. By forcing drain and source nodes to V_{dd} during OFF-state, capacitance of the reverse biased drain–bulk junction is reduced and controlled better [31].

3. Post-layout simulation results

Capacitance extraction has been done for the post-layout simulations because of the limitations on simulation tools and computing power. The frequency bands are organized as 2.27–2.51 GHz, 2.48–2.78 GHz, 3.22–3.53 GHz, 3.48–3.91 GHz and 4.528–5.7 GHz. First and second lower-frequency bands are provided by using OFF-state inductor switches and two switched capacitors. In the M5/M6 OFF-state, inductance that is seen from oscillation node is approximately 2 nH. Quality factor of 1 nH differential inductor varies from 8.7 to 11.8 over 2.4 to 5 GHz. 3.22–5.7 GHz frequency bands are covered by two inductors (M_5/M_6 ON-state) and three switched capacitors. Frequency bands versus voltage-tuning range plots are shown in Fig. 7.

The VCO core draws current that varies from 3 to 5 mA, depending on the frequency bands, while the VCO buffer draws a current of 9 mA from 3.3 V power supply. Fig. 8 shows the phase noise, varying from −122 to −110 dBc/Hz over 2.2 to 5.7 GHz frequency range. More importantly, the phase noise is essentially flat over the entire operating frequency band. The performance of the multi-band VCO is summarized in Table 1.

A widely used figure of merit (FOM) [7] for the VCO is defined as

$$\mathrm{FOM} = L\{offset\} - 20\log\left(\frac{f_0}{offset}\right) + 10\log\left(\frac{P_{dc}}{1\,\mathrm{mW}}\right) \quad (2)$$

Here, $L\{f_{offset}\}$ is the phase noise at offset frequency f_{offset} from the carrier frequency f_0. P_{dc} is VCO power consumption in mW. The best-measured FOM for the VCO is—181,16 dBc/Hz at 3,91 GHz. Table 2 summarizes the performance of state-of-the-art wideband VCOs operating around 2.15 and 5 GHz. Power consumption of the buffer is excluded from our calculations for

comparison purposes with other similar work in literature. As observed from Table 2, the phase noise performance of our VCO for each frequency bands is better or compatible with other wideband VCOs in the literature. Power consumption values are better when compared to the same technology but slightly higher when compared to other technologies. This can be attributed to the technology of our choice and also the complexity of biasing concept for five different frequency bands. More importantly, the figure of merit for our VCO is much better when compared to other VCO studies in the literature, indicating the strength of our design approach.

Output power of the oscillator was another concern, during the design, directly effecting the input of the proceeding stage in applications such as a transceiver architecture. Overloading the input of the proceeding stage is usually the problem if the output power is not properly optimized. Fundamental frequency power, that is obtained from 50-Ω terminals at the ouput of the buffer, changes according to the frequency band of operation. DC biasing conditions of the circuit altered by the operating frequency bands, resulting a differential peak-to-peak voltage swing at the buffer output changing between 0.5 and 0.743 V. Fundamental output power can be observed in Fig. 9, varying between −6.087 and 0.992 dBm. Second and third harmonic output power need to be suppressed to generate a uniform output signal. The −37.21 dBm of average, suppressed power in the second harmonic is shown in Fig. 10. The third harmonic level is also adequately suppressed and has an average value of −47.6 dBm throughout the 2.2–5.7 GHz band, as presented in Fig. 11.

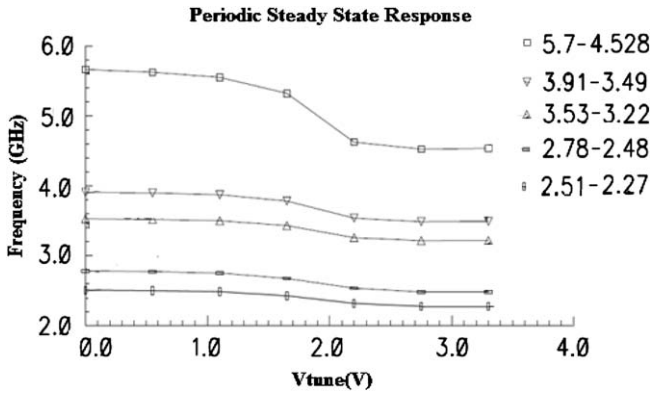

Fig. 7. Frequency tuning range of the Multi-band VCO.

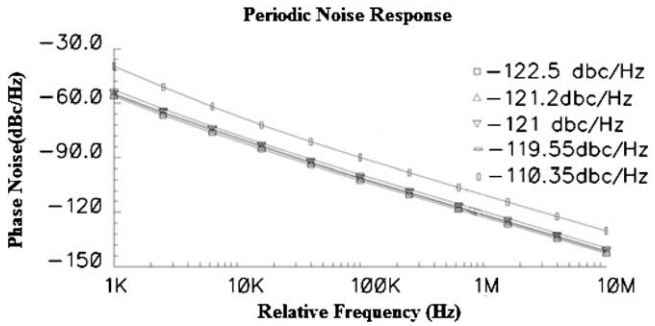

Fig. 8. Phase noise performance at three frequencies for multi-band VCO.

Power dissipation is a key performance parameter of the VCO design and was minimized with selecting appropriate DC bias values for each frequency band of operation in our study. HBTs, utilized in the buffer stage (Q_1 and Q_2), should have larger emitter widths ($24\,\mu m^2$) to obtain a better isolation from external components/equipments. Considering the biasing and oscillation conditions, the VCO core draws an average of 4.37 mA from current source whereas 9 mA is drawn by the buffer circuitry. The average current drawn from the 3.3 V supply is 13.37 mA, providing a DC power consumption value of 44.12 mW.

4. Layout design

Fig. 12 shows the physical layout of the Multi-band VCO. The main design consideration in the physical layout generation was to reduce the static parasitics and also sensitivity to parasitics. To minimize the even order distortion of the output waveform, symmetric layout was also another major concern. Positive and negative oscillation nodes are the critical nodes, designed to prevent capacitive and resistive parasitic effects. The parasitics at the oscillation nodes directly affect VCO performance parameters such as phase noise and oscillation frequency. To reduce the capacitance between metal layer and subsrate, top metal layer is used for the oscillation node connections. Metal-insulator-metal (MIM) capacitances at the oscillation nodes because of their higher linearity and quality factor.

The thickness of the metal layers were designed to handle higher current, where necessary, and minimized to reduce their parasitic contributions. Finally, sharp turns and corners were avoided in the RF pads so as to prevent the degradation of RF signal from these regions. Inductors, Varactors, Switch-circuit arrays and the bias circuitry are the main subblocks of the layout design. Two series 1.04 nH inductors were utilized, instead of a single 2.08 nH inductor, to keep the circuit symmetry. 2.5-μm-thick metal layer was used to form the spirals. The inductors were placed in areas to minimize path length as well as the magnetic effect. The quality factor of the inductor was also increased by

Table 1
The post-layout performance summary of our VCO.

	Band 1	Band 2	Band 3	Band 4	Band 5
$V_{switchC1}$ (V)	3.3	3.3	0	0	0
$V_{switchC2}$ (V)	3.3	0	3.3	0	0
$V_{switchC3}$ (V)	0	0	3.3	3.3	0
$V_{switchL2,L3}$ (V)	0	0	3.3	3.3	3.3
V_{tune} (V)	0–3.3	0–3.3	0–3.3	0–3.3	0–3.3
Tuning range for post-layout simulation	2.27–2.51	2.48–2.78	3.22–3.53	3.49–3.91	4.528–5.7
Simulated frequency (GHz)	2.51	2.78	3.53	3.91	5.7
Tuning range for schematic simulation	2.26–2.48	2.46–2.75	3.28–3.62	3.577–4.04	4.725–6.04
Phase noise (dBc/Hz) at 1 MHz for schematic simulation	−126.2	−124.3	−124.1	−122.5	−116.7
Phase noise (dBc/Hz) at 1 MHz for post-layout simulation	−122.5	−121.2	−121	−119.55	−110.35
Vdd (V)	3.3	3.3	3.3	3.3	3.3
I_{vcore} (mA)	6.326	5.506	4.378	3.248	2.4
Output voltage swing (V_{pp})	0.708	0.734	0.54	0.52	0.5

Table 2
Comparison of our results with the ones published in the literature.

Ref.	Technology (μm)/results	Oscillating frequency (GHz)	Phase noise (dBc/Hz)	Power (mW)	f_{offset} (MHz)/f_0 (GHz)	FOM	Area (mm^2)
[7]	0.13 SOI measurement results	3.065–5.612	−114.6	1 V*2 mA	1/3.065	−185.8	0.299
			−120.8	1 V*2 mA	1/5.612	−186.6	–
[32]	0.35 SiGe BiCMOS measurement results	2.67–4.27	−111	4 V*5.8 mA	1/4.37		0.657
[6]	0.18 CMOS measurement results	2.15–2.75	−121.45	3.88 V*1.8 mA	1/2.4	−180.2	–
		4.75–4.99	−118.49	3.1 V*1.8 mA	1/4.8	−184.6	–
[33]	0.35 BiCMOS measurement results	3.3–5.3	−113	2.5 V*14.6 mA	0.6/4.4	−174.7	1.5125
[34]	0.25 CMOS measurement results	3.28–4.11	−117	2.5 V*3 mA	1/4	−180.2	1
[20]	0.18 CMOS measurement results	2.78–3.78	−126.5	1.8 V*5.7 mA	1/2.83	−185.4	0.806
			−122.7	1.8 V*4.9 mA	1/3.77	−184.8	–
This work	0.35 SiGe BiCMOS post-layout simulation results	2.27–2.51	−122.5	3.3 V*6.326 mA	1/2.51	−177.31	1.477
		2.48–2.78	−121.2	3.3 V*5.506 mA	1/2.78	−178.38	–
		3.22–3.53	−121	3.3 V*4.378 mA	1/3.53	−180.45	–
		3.48–3.91	−119.55	3.3 V*3.248 mA	1/3.91	−181.16	–
		4.528–5.7	−110.35	3.3 V*2,4 mA	1/5.7	−176.48	–

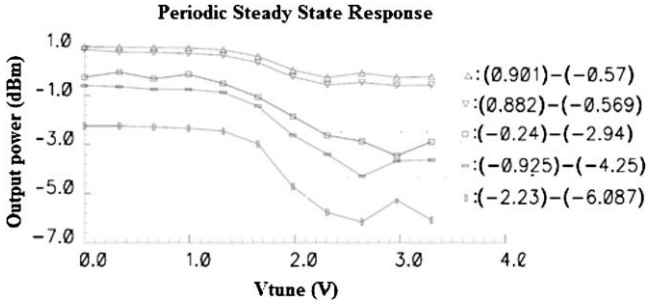

Fig. 9. Fundamental frequency output power vs. tuning voltage.

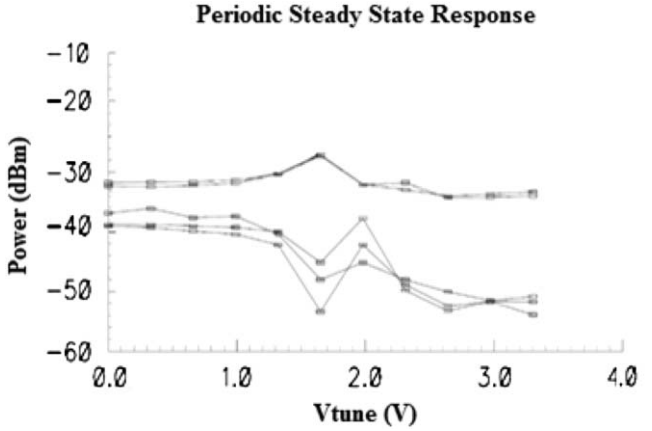

Fig. 10. Second harmonic output power vs. tuning voltage.

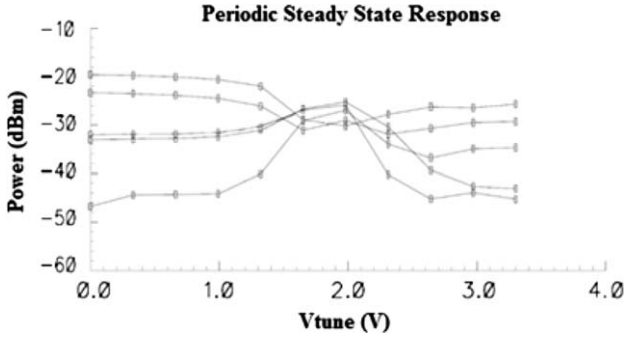

Fig. 11. Third harmonic output power vs. tuning voltage.

using thick metal layer, changed from 8.7 at 2.4 GHz to 11.8 at 5.0 GHz. It has a maximum value of 11.9 at 4.4 GHz.

The oscillation obtained at the connection node of $-G_m$ circuitry, switched-capacitance array, AMOS varactors and inductors. For the purpose of area optimization, switched-capacitance array was located between the output ports of two inductors. Furthermore, inductors, AMOS varactors and $-G_m$ circuitry were located together in a smaller area to reduce the parasitics as shown in Fig. 13.

The layout of the accumulation mode varactor is composed of parallel connected small capacitors. The capacitance–voltage characteristics are modeled by the gate-bulk capacitance of a PMOS transistor. Bias circuitry is formed by the transistors, low-pass filter and a by-pass capacitance. The maximum tail current of the LC tank is 6 mA, providing 3 mA DC current for each branch. Poly capacitances were utilized for low-pass filter and by-pass capacitors because of having much higher capatitance value than

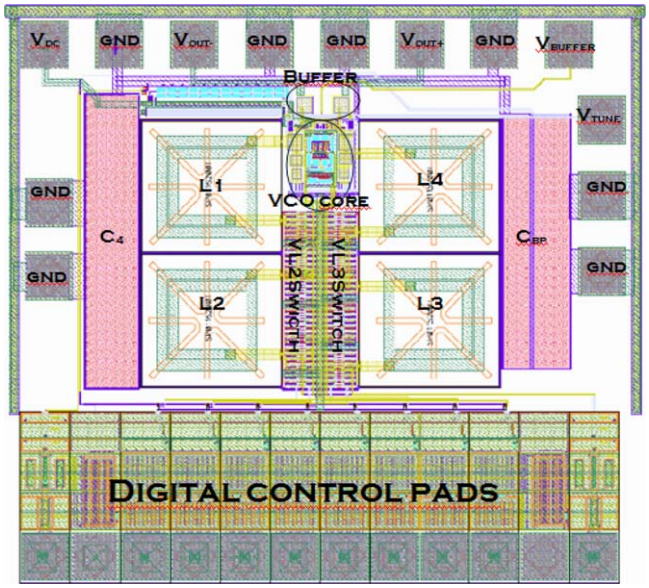

Fig. 12. Multi-band VCO layout.

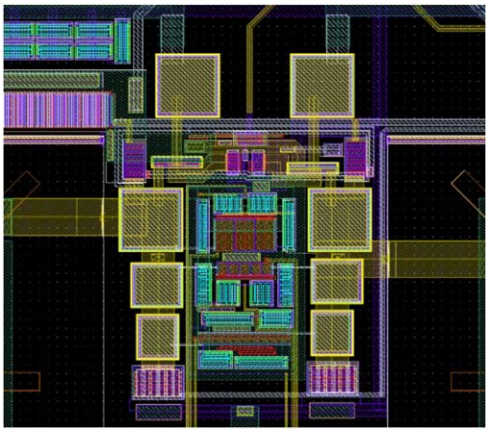

Fig. 13. VCO layout detail.

C_{MIM}. Resistors were formed by the second poly Si- layer of the process. Their resistance values are 140 kΩ at the low-pass filter and 10 kΩ for each branch at the capacitor switch. A detailed, layout view of the bias circuitry is illustrated in Fig. 14.

The total circuit occupies an area of $1.150 \times 1.283\ mm^2$, including the buffer stage, RF, DC and digital pads.

5. Conclusion

An integrated 2.2–5.7 GHz Multi-band, differential LC VCO for Multi-standard Wireless Communication systems is designed, utilizing 0.35 μm SiGe BiCMOS technology. Based on the post-layout simulation results, the VCO can be tuned at 5 different frequency bands with a maximum bandwidth of 1.36 GHz and a minimum bandwidth of 300 MHz. The designed and simulated VCO can generate a differential output power of between 0.992 and −6.087 dBm with an average power consumption of 44.21 mW, including buffers. Average second and third harmonics level are obtained to be between −37.21 and −47.6 dBm, respectively. Phase noise of −110.45 to −122.5 dBc, simulated at 1 MHz offset, can be obtained through the frequency of interest. Additionally, figure of merit (FOM), that includes all important parameters such as phase noise, power consumption and division

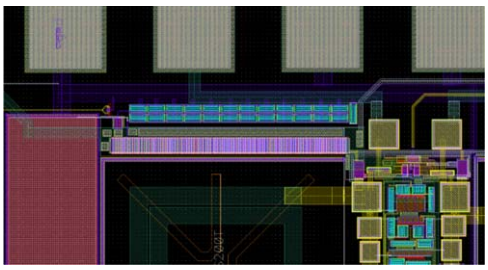

Fig. 14. VCO layout detail, bias circuitry.

of operating frequency to offset frequency, is between −176.48 and −181.16 and comparible or better than other similar VCO works in the literature. The main advantage of our work, when compared to the other VCOs works in the literature, is its ability to cover 5 frequency bands starting from 2.27 to 5.76 GHz, without FOM and area abandonment. Moreover, combined the switching inductor and capacitor models were used in this study, for the first time, to obtain our findings.

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