Design of a 4.2-5.4 GHz Differential LC VCO using 0.35 μm SiGe BiCMOS Technology

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Abstract **In this paper, a 4.2-5.4 GHz, $-G_m$ LC voltage controlled oscillator (VCO) for IEEE 802.11a standard is presented. The circuit is designed with AMS 0.35μm SiGe BiCMOS process that includes high-speed SiGe Heterojunction Bipolar Transistors (HBTs). Phase noise is -110.7 dBc/Hz at 1MHz offset from 5.4 GHz carrier frequency and -113.5 dBc/Hz from 4.2 GHz carrier frequency. A linear, 1200 MHz tuning range is obtained utilizing accumulation-mode varactors. Phase noise is relatively low due to taking the advantage of differential tuning concept. Output power of the fundamental frequency changes between 4.8 dBm and 5.5 dBm depending on the tuning voltage. The circuit draws 2 mA without buffers and 14.5 mA from 2.5 V supply including buffer circuits leading to a total power dissipation of 36.25 mW. The circuit occupies an area of 0.6 mm^2 on Si substrate including RF and DC pads.**

Index Terms— **VCO, SiGe BiCMOS, WLAN, Differential tuning, RFIC.**

I. INTRODUCTION

5-6 GHz Unlicensed National Information Infrastructure (UNII) band has been authorized in many countries for WLAN high-speed applications. As the numbers of products grow and the types of the products evolve, high performance oscillators with low phase noise, low power dissipation, satisfactory output power and tuning range increase their importance in today's wireless applications [1].

Integrated voltage controlled oscillators (VCOs) are utilized in a number of applications as the sources of signal generation as a part of data or clock recovery systems. Among these applications of VCOs, design for wireless communications has more stringent specifications than for other applications. IEEE 802.11a standard uses Orthogonal Frequency Multiplexing (OFDM) based modulation scheme which is more sensitive to phase noise compared to single carrier modulation schemes. Thus, phase noise is probably the most stringent specification for a wireless VCO. In order to meet the the requirements for IEEE 802.11a standard, the phase noise of the VCO should be lower than -110 dBc/Hz at 1MHz offset from the carrier frequency [2].

Tuning Range is also an important performance parameter and has been a major problem for VCOs in CMOS or BiCMOS technologies. Due to the limited tuning range of p-n junction varactors and inversion MOS varactors, accumulation mode is generally preferred. The tuning range of accumulation-mode MOS varactors is proven to be the highest among other varactor types. In addition, the VCO circuit can be tuned more linearly with accumulation-mode MOS varactors [3].

Another issue in VCO design is high varactor sensitivity. A high C_{max}/C_{min} ratio over a low voltage tuning range degrades the phase noise performance. Differential tuning provides a simple but effective solution to avoid the drawbacks of this effect [4]. Output power and power dissipation are other parameters determining the performance of VCOs. A well-designed VCO should send enough power to its output to drive the mixer and should dissipate the minimum power for a longer battery lifetime.

A VCO meeting the specifications of IEEE 802.11a standard may be implemented utilizing various technologies and topologies. Recently published works include realizations with GaAs HBT [5], SiGe BiCMOS [6], Si CMOS [7] and Silicon-on-insulator (SOI) CMOS [4]. Among these technologies SiGe BiCMOS technology leads others from an application point of view. This is because it combines the cost and integration advantages of Si material system with the performance advantages of SiGe HBTs.

Considering topologies, RF VCOs can be realized as resonator (LC) based oscillators, ring oscillators or multivibrator oscillators. Among the three topologies, LC based oscillators are most prominent ones due to their relatively low phase noise [8].

Keeping the stringent phase noise requirement, other performance parameters and topological advantages in mind, differential LC $-G_m$ configuration is chosen in this work. Differential topology is utilized for its advantages such as higher common mode rejection ratio (CMRR) and higher output power. Besides, VCO mostly drives the mixer most of which is composed of differential Gilbert cell.

0.35 μm SiGe BiCMOS is decided as the suitable technology since it combines the cost and integration advantages of Si with the performance advantages of band-gap engineered SiGe HBTs. With this technology and topology, a low phase noise, high tuning range VCO for UNII band applications is designed. The proposed VCO is tunable from 4.2 to 5.4 GHz with a worst case phase noise of -110 dBc/Hz at 1 MHz offset from 5.4 GHz carrier. The layout occupies 0.6

mm^2 on Si substrate drawing 14.5 mA from 2.5 V supply including buffers.

The organization of the paper is as follows; Section II develops the VCO design in detail giving the design issues for the core, buffer and LC tank separately; section III analyses and discusses the post layout simulation results; section IV describes the layout design of the circuit and finally section V concludes the paper.

II. DIFFERENTIAL -G$_M$ LC VCO DESIGN

A. VCO Core

The technology used in this design is a 0.35 μm 4-metal double-poly SiGe BiCMOS process of Austria MicroSystems (AMS) with a thick metal option. It includes high-speed SiGe HBTs with 59 GHz and 63 GHz f$_t$ and f$_{max}$ values respectively. HBTs with two base contacts are utilized to reduce the base resistance, the critical source of noise in bipolar transistors.

The topology for the VCO is a differential –G$_m$ LC configuration, given in Figure 1. It consists of three parts, namely the -G$_m$ circuit (Q1, Q2, M1, and M2), the LC tank (L and C$_{var}$) and the buffer (Q3 and Q4). The PMOSs together with the npn HBTs in the -G$_m$ part are utilized to obtain additional negative resistance. Also DC level of the oscillation nodes is adjusted by these PMOS devices.
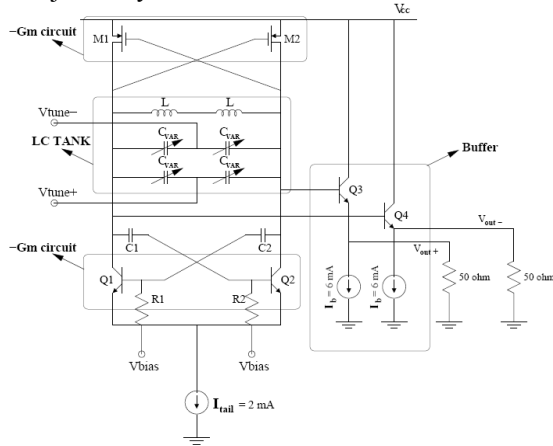

Figure 1 Schematic of the Voltage Controlled Oscillator

This HBT-PMOS cross-coupled pair brings two important improvements over the HBT-only structure; first, it has bigger tank amplitude for a given current reducing the power dissipation; second, it can be optimized to have more symmetrical output wave leading to a better phase noise.

The core of the oscillator benefits from HBT transistors which have the high f$_T$ and f$_{max}$, lower 1/f noise, reduced broadband shot noise and thermal noise compared to that of FETs and higher transconductance for a given bias [9]. The HBTs also operate better at lower dc current values providing lower phase noise at lower power dissipation. The VCO illustrated in Figure 1 is operated at the current limited regime in order to reduce power consumption and obtain higher spectral purity [10]. In the current limited regime, the tank amplitude is proportional to the tail current or equivalent

parallel tank resistance, while V$_{dd}$ or a change in the operation mode limits it in the voltage-limited regime. This can be expressed as the following

$$V_{\tan k} = I_{bias} / g_{\tan k} \text{ in Current-Limited Regime} \quad (1)$$

$$V_{\tan k} = V_{\lim it} \text{ in Voltage-Limited-Regime} \quad (2)$$

B. LC Tank

The main difference of the circuit topology from the conventional differential LC tank structure is the differentially tuned accumulation MOS varactors. Differential tuning provides a solution to avoid the drawbacks of high varactor sensitivity (k$_v$) effect. A high C$_{max}$/C$_{min}$ ratio over a low voltage tuning range, meaning high varactor sensitivity, degrades the phase noise performance as described by the modified Leeson's Formula [4];

$$L(\Delta f, k_v) = 10 \log \left\{ \left(\frac{f_0}{2Q\Delta f} \right)^2 \left[\frac{FkT}{2P_s} \left(1 + \frac{f_c}{\Delta f} \right) \right] + \left(\frac{k_v v_n}{2k_{LC}\Delta f} \right)^2 \right\} \quad (3)$$

Here, f$_o$ is the frequency of oscillation, Q is the quality factor, Δf is the frequency offset from the carrier, F is the noise factor, k is the Boltzmann's constant, T is the temperature, P$_s$ is the RF power produced by the VCO, f$_c$ is the Flicker noise corner frequency, v$_n$ is the common mode noise voltage and k$_{LC}$ is a constant that is a function of L and C of the resonator.

Utilizing differentially-tuned varactors at the tank circuit enables one to suppress common mode noises, such as flicker noise from being upconverted to the carrier frequency, resulting in a better phase noise performance.

The elements of LC tank are analyzed separately. The varactor has a C$_{max}$ / C$_{min}$ about three over a tuning voltage of ± 800mV. The quality factor has a maximum value of 60 and minimum value of 20, depending on the tuning voltage. The inductor is from AMS library and has an inductance value of 1.04nH with a quality factor of 11.8 at 5 GHz. Quality factor of the overall tank circuit is determined from the parasitic conductances of capacitance and inductance. Since accumulation mode MOS varactors have relatively higher Q values than on-chip inductors, inductor is the main determining factor of the overall Q of the tank circuit.

The utilization of the capacitances C1 and C2 is a refinement to the –G$_m$ topology and can also be thought as the parts of the LC tank. They are added to the design in order to get larger swings by decoupling the base from the collector. In addition, the center frequency can be fine-tuned without changing the tuning range with C1 and C2.

C. Buffer

Buffer is the link between the output stage of the VCO core and the output port. It should provide adequate power to the output 50-Ohm termination impedances as well as adequate isolation between the output and the VCO core. The input impedance of the buffer must be high enough to prevent the

measurement equipment from degrading the Q-factor of the LC tank. If we connect the outputs of the core directly to the 50-Ohm ports, the resultant swing reduces considerably, due to the reduction in the parallel tank resistance. Furthermore, the degradation of the output swing may be so high that the circuit does not oscillate.

III. POST LAYOUT SIMULATION RESULTS

In this design, we mainly aimed for a low phase-noise to meet the phase noise specification of the IEEE 802.11a standard. High and linear tuning range capability is another design target as well as minimized power dissipation and reasonable output power.

Phase noise at a given offset for a linear time variant (LTV) oscillator can be improved by maximizing the Q of the resonator, maximizing the carrier power or minimizing the varactor sensitivity effect, as shown in (3). Resonator Q is limited by the tank inductance even if buffering prevents the degradation of the resonator Q with its high input impedance. So, highest Q inductor of the library is selected for the design. After the values of LC tank elements is set, the minimum current for oscillation is calculated and for a safe oscillation, about three times higher current than the minimum current for oscillation is provided by the tail current (for each oscillation node). However, the phase noise is still under demands of the standard with this output power and is increased to four times the minimum current leading to 1 mA from each oscillation branch.

Other design strategies for an improved phase noise are minimizing the varactor sensitivity effect and choosing active devices with low $\omega_{1/f}$ frequencies. As briefly explained in Section II, differential tuning of the varactors improves the varactor sensitivity related degradation of the phase noise. Furthermore, HBTs with lower $\omega_{1/f}$ frequencies than MOS counterparts are utilized for a better phase noise. Phase noise at 1MHz offset from 5.4 GHz carrier is -110.7 dBc/Hz and it is -113.5 dBc/Hz from 4.2 GHz carrier, as shown in **Figure 2**. Both of these values exceed the phase noise specification of the standard, which is −110 dBc/Hz for the same offset.
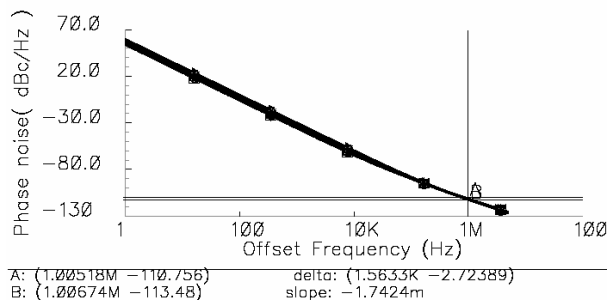
A: (1.00518M −110.756)   delta: (1.5633K −2.72389)
B: (1.00674M −113.48)   slope: −1.7424m

Figure 2 Phase noise of the voltage controlled oscillator

Frequency tuning is performed by changing differential $V_{tune(+)}$ and $V_{tune(-)}$ over a fixed value of 1.2V which is approximately $V_{CC}/2$. 1.2 V is chosen so as to obtain a higher tuning range. Choosing the zero-tuning voltage at about $V_{CC}/2$ for a differentially-tuned VCO, one is able to get higher

voltage headroom for tuning the circuit. In addition, it decreases the oscillator sensitivity. So the effect of high varactor sensitivity, which degrades phase noise, is reduced. This DC value can be easily set by the PMOS transistors. Actually, $V_{tune (+)} = - V_{tune (-)} = V_{tune}$; thus changing V_{tune} from -0.8V to 0.8V effectively changes the total voltage from 0.4V to 2V. This is the interval where tuning range can be assumed linear, as illustrated in Figure 3.
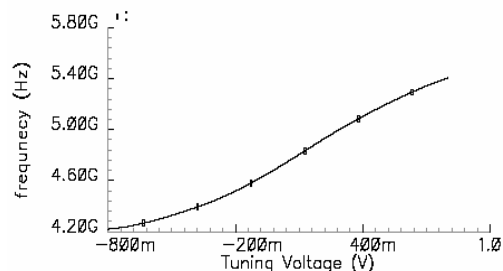
Figure 3 Output frequency vs. differential tuning voltage

Output power of an oscillator should be high enough so that it can deliver enough power to the following stage in the transceiver architecture, the mixer. After the buffer stage is connected and for 50-Ohm terminations at the output of the buffer, fundamental frequency power is obtained between 4.8 dBm and 5.5 dBm at the corners of the tuning voltage. The differential peak-to-peak voltage swing at the buffer output is 1.2V. Fundamental output power can be observed in Figure 4.
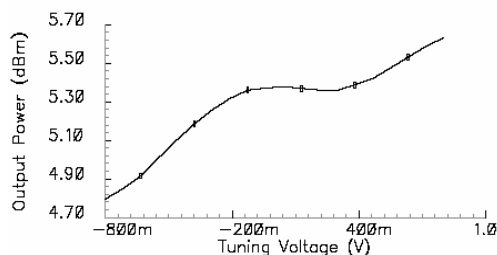
Figure 4 Fundamental Frequency output power vs. differential tuning voltage

The difference in the power levels for different tuning voltages can be explained as the result of wide frequency coverage. The power levels for the whole tuning range can be equalized; however, this approach is avoided since will increase circuit complexity and power consumption. Second and third harmonic output power need to be suppressed for neat and clear signal at the output. The -82 dBm (87.5 dBc) suppression in the second harmonic is remarkable, as in Figure 5. This is due to differential circuit topology that rejects the common mode noise and provides a linear tuning across the covered frequency band. The third harmonic level is also adequately suppressed and is -21 dBm (26.5 dBc) throughout the 4.2-5.4 GHz band.
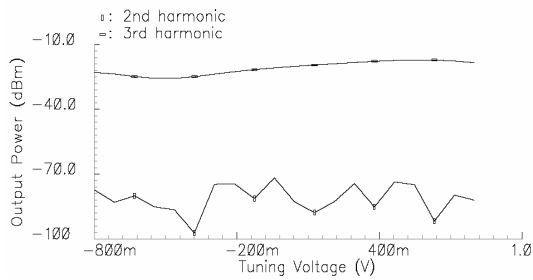
Figure 5 2nd and 3rd harmonic output powers vs. Differential tuning voltage

To minimize the power dissipation and prevent the distortion of the output signal, the HBTs are operated within their current-limited regime instead and biased between maximum β and maximum f$_t$. Additionally, increasing the transistor size lowers 1/f noise but increases power consumption. The emitter width of the HBTs utilized in the VCO core (Q1 and Q2) is 21.5 μm^2. Buffer HBTs (Q3 and Q4), however, have emitter widths of 24 μm^2 for better isolation from the measurement equipment. After the biasing constraints and oscillation condition is taken into account, the VCO core draws 2 mA from current source whereas 12.5 mA is dissipated in the buffer circuitry. The total current drawn from the 2.5 V supply is 14.5 mA, which means a DC power consumption of 36.25 mW.

IV. LAYOUT DESIGN

The physical layout of the VCO is shown in Figure 6. Some efforts are made to reduce the parasitics as well as the sensitivity to parasitics. The layout is symmetric as in general differential analog designs to minimize the even order distortion of the of the output waveform.

The most critical nodes are the positive and negative oscillation nodes which have to be carefully designed to prevent capacitive and resistive parasitic effects. The connections of these nodes is done by the top metal layer of the process to reduce the capacitance with substrate.
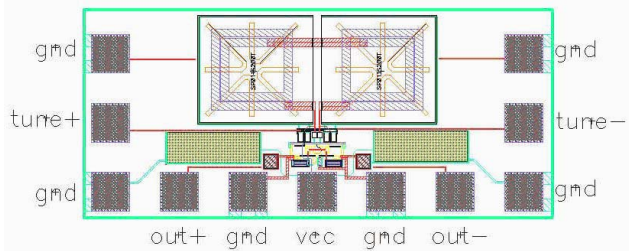

Figure 6 Voltage Controlled Oscillator Layout

Again for the oscillation node, Metal-Insulator-Metal (MIM) capacitances are utilized due to their higher quality factor and linearity. However, this may not bring much improvement since the quality factor of the resonator is determined by the inductor. Instead of one 2.1 nH inductor, two series 1.05 nH inductors are used to keep the circuit symmetry. Thinner lower-metal lines are avoided since their current carrying capability is lower than higher-metal lines.

Also, thicker lines increases the parasitic capacitance which probably mis-tunes the center frequency. Finally, corners and sharp turns are avoided in the RF path to prevent the degradation of RF signal from these regions. The whole circuit has dimensions of 1.16mm*0.52mm occupying an area of 0.6 mm^2 on Si die including RF and DC pads.

V. CONCLUSION

A fully integrated 4.2-5.4GHz VCO for wireless applications was designed using 0.35μm SiGe BiCMOS technology. The VCO can be tuned using a DC voltage of 0.4 to 2 V for a bandwidth of 1.2 GHz. The designed VCO can generate a differential output power of 5.5 dBm with a total power consumption of 36.44 mW including buffers. Typical second and third harmonics levels are –82 (87.5 dBc) dBm and –21 (26.5 dBc) dBm, respectively. Phase noise of –110.7 to –113.5 dBc at 1 MHz offset can be obtained through the frequency of interest, which satisfies the IEEE 802.11a standard requirement in UNII band.

(1) Acknowledgment

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