Electrical Balance Duplexer Based In-Band Full Duplex System for 5G (28 GHz) Communication Systems

by

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Electrical Balance Duplexer Based In-Band Full Duplex System for 5G (28 GHz) Communication Systems

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Keywords: In-Band Full Duplex, 5G, EBD, SiGe BiCMOS, Integrated Circuits.

Abstract

The evolution of wireless communication systems is witnessed every day by their users. Currently, 4G meets the needs of the users in terms of data-rate and latency. 4G is spreading to the world and dominating the worldwide market. However, ever-increasing user demands for higher data-rate, lower latency, and an increased number of users are generating new challenges that 4G could not manage to meet the demands. To overcome the challenges in 4G, the institutions are studying the next generation (5G) communication systems. With the introduction of 5G, the utilization of various new technologies such as full-duplex becomes necessary to meet the demand for higher data-rate and lower latency. With the in-band full-duplex operation, the spectrum efficiency is doubled theoretically. The improvements in the SiGe BiCMOS technology have made them be a good candidate for low-cost and high-performance transceivers. In this thesis, the design of an electrical balance duplexer based in-band full-duplex system for 5G (28 GHz) communication systems implemented in IHP's 0.13 μm SiGe BiCMOS technology is presented.

The electrical balance duplexer is constructed with a hybrid transformer and an impedance tuner to suppress the leakage from the transmitter to the receiver by reducing the mismatch between the antenna and balance port impedances. The duplexer achieves isolation between the transmitter and receiver sides more than 40 dB for various antenna impedances at 28 GHz. The transmitter gain of the system is more than 30 dB by achieving $OP1_{dB}$ of 12 dBm whereas the receiver gain of 5 dB is obtained. The minimum noise figure of the receiver is 8.2 dB.

5G (28 GHz) Haberleşme Sistemleri için Elektriksel Denge Dupleksleyici Bant-içi Tam Dupleks Sistem

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Özet

Kablosuz iletişim sistemlerinin evrimine her gün kullanıcıları tarafından tanık olunmaktadır. Şu anda 4G, veri hızı ve gecikme açısından kullanıcıların ihtiyaçlarını karşılıyor. 4G dünyaya yayılıyor ve dünya pazarına hakim. Bununla birlikte, daha yüksek veri hızı, daha düşük gecikme süresi ve artan sayıda kullanıcı için giderek artan kullanıcı talepleri, 4G'nin talepleri karşılayamayacağı yeni zorluklar yaratmaktadır. Kurumlar, 4G'deki zorlukların üstesinden gelmek için yeni nesil (5G) iletişim sistemlerini inceliyor. 5G'nin piyasaya sürülmesiyle, daha yüksek veri hızı ve daha düşük gecikme süresi talebini karşılamak için tam çift yönlü gibi çeşitli yeni teknolojilerin kullanılması gerekli hale geldi. Bant içi tam çift yönlü işlemle, spektrum verimliliği teorik olarak iki katına çıkar. SiGe BiCMOS teknolojisindeki gelişmeler, onları düşük maliyetli ve yüksek performanslı alıcı-vericiler için iyi bir aday haline getirmiştir. Bu tezde, IHP'nin 0.13 μm SiGe BiCMOS teknolojisinde uygulanan 5G (28 GHz) iletişim sistemleri için elektriksel denge duplexer tabanlı bir bant içi tam çift yönlü sistemin tasarımı sunulmuştur.

Elektrik denge dupleksleyici, anten ile denge portu empedansları arasındaki uyumsuzluğu azaltarak vericiden alıcıya sızıntıyı bastırmak için bir hibrit transformatör ve bir empedans ayarlayıcı ile inşa edilmiştir. Dupleksleyici, 28 GHz gibi çeşitli anten empedansları için verici ve alıcı tarafları arasında 40 dB'den fazla izolasyon sağlar. Sistemin verici kazancı, 12 dBm'lik OP1 $_{dB}$ elde edilerek 30 dB'nin üzerindedir, oysa 5 dB'lik alıcı kazancı elde edilir. Alıcının minimum gürültü rakamı 8.2 dB'dir.

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List of Abbreviations

3GPP	3rd Generation Partnership Project
AMTS	Advanced Mobile Telephone Service
ANT	Antenna
ATT	Attenuator
BAL	Balance
BEOL	Back-End-of-Line
BJT	Bipolar Junction Transistor
BV_{CEO}	Collector-Emitter Breakdown Voltage
CB	Common-Base
CDMA	Code Division Multiple Acces
CE	Common-Emitter
CMOS	Complementary Metal-Oxide-Semiconductor
CMRR	Common-Mode Rejection Ratio
EBD	Electrical Balance Duplexer
FDMA	Frequency Division Multiple Access
FDD	Frequency Division Duplexing
FPGA	Field Programmable Gate Array
GPRS	General Packet Radio Service
GaAs	Gallium-Arsenide
HBT	Heterojunction Bipolar Transistor
HT	Hybrid Transformer
IBFD	In-Band Full-Duplex
IC	Integrated Circuit
IF	Intermediate Frequency
IL	Insertion Loss
IP	Internet Protocol
IMT	International Mobile Telecommunication
IMTS	Improved Mobile Telephone Service
InP	Indium-Phosphide
IP_{1db}	Input 1-dB Compression Point
ITU	International Telecommunication Union
LNA	Low Noise Amplifier
LO	Local Oscillator
MIM	Metal-Insulator-Metal
MIMO	Multiple-Input-Multiple-Output
MMS	Multimedia Messaging Service
MOM	Metal-Oxide-Metal
MTS	Mobile Telephone Systems
mm-Wave	Millimeter-wave
NF	Noise Figure
NMT	Nordic Mobile Telephone
OFDMA	Orthogonal Frequency Division Multiple Access
OP_{1db}	Output 1-dB Compression Point
PA	Power Amplifier
PTT	Push to Talk
RF	Radio Frequency

RX	Receiver
SAW	Surface Acoustic Wave
SiGe	Silicon-Germanium
SIC	Self-Interference Cancellation
SMS	Short Message Service
SNR	Signal to Noise Ratio
SOLT	Short-open-load-thru
SPDT	Single-Pole-Double-Throw
SPI	Serial-to-Parallel
SSB	single-sideband
TDMA	Time Division Multiple Access
TDD	Time Division Duplexing
TX	Transmitter
UHD	Ultra High Definition
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Domain Multiple Access

1 Introduction

1.1 Evolution of Communication Systems

Long-distance communication is an old phenomenon whose methods, tools, and medium varies throughout human history. For example, utilizing smoke signals was one of the ancient communication methods from a long distance. Bad weather conditions (fog, rain, etc) were one of the main obstacles for smoke signals. As can be seen from this example, long-distance communications have drawbacks, and people work to overcome challenges such as the transfer time of information, the quality of the transfer, and the number of connected people. These efforts brought about wireless communication which is the information transfer between two or more devices apart from each other without a cable or "wire". The first appearance of these types of devices was the mobile radio telephony system. Since these systems were the ancestor of mobile phones, they are referred to as "0G". Technologies in these systems contained PTT (Push to Talk), MTS (Mobile Telephone Systems), IMTS (Improved Mobile Telephone Service), and AMTS (Advanced Mobile Telephone Service). Autoradiopuhelin started to be used in 1971 as the first commercially operated mobile phone network in Finland [1]. The history of mobile network generations until 2016 is presented in Fig. 1. Almost every 10 years, a new mobile network generation is introduced to the world-wide market [2].

With the invention of cell phones, the first-generation of wireless telecommunication technologies, "1G" started to emerge in 1979 in the United States [3]. 1G was built on analog telecommunication techniques and used Frequency Division Multiple Access (FDMA). Devices in 1G technologies were bulky and had non-uniform coverage [4]. Different parts of the Earth deployed different and incompatible telecommunication systems with each other. For instance, Advanced Mobile Phone System, which could provide a 19.2-kbps data rate, launched in North America or Nordic Mobile Telephone (NMT), was utilized in Nordic Countries, Eastern Europe, and Russia [1, 4]. Incompatibility of these systems made roaming between the countries more difficult, especially in Europe [3]. Moreover, the security and privacy of communication was an issue that 1G technologies weak about. Unlike 1G, digital communication was fundamental in 2G technologies in the 90s. Code Division Multiple Acces (CDMA) and Time Division Multiple Access (TDMA) were the most dominant methods in 2G. The utilization of digital encoding led to an improvement in voice quality and less power consumption that increases battery life [1]. Also, the Short Message Service (SMS) and Multimedia Messaging Service (MMS) came to live with 2G. General Packet Radio Service (GPRS) introduced in the era of 2G enabled

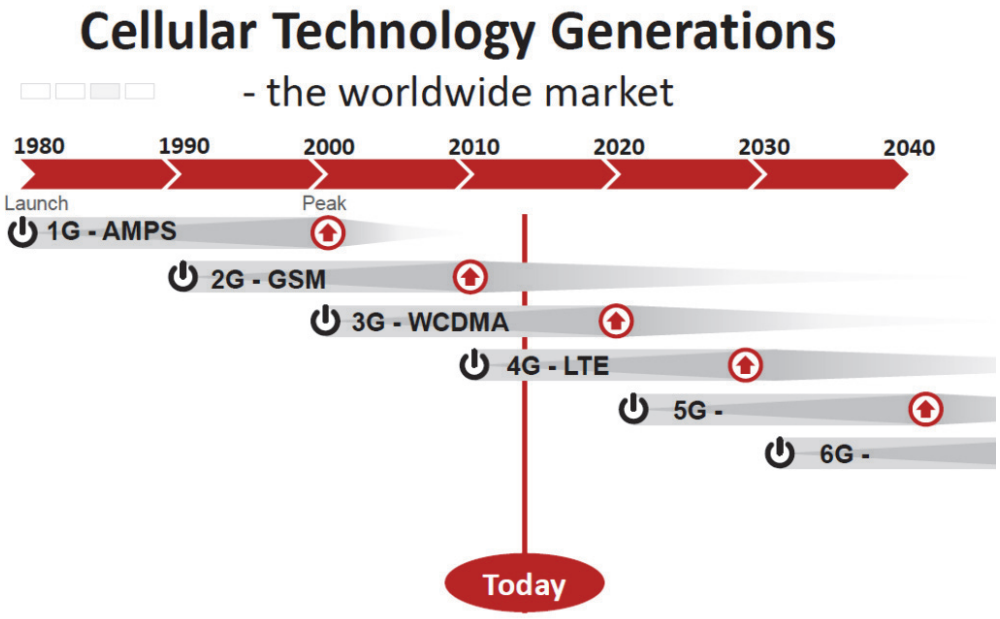


Figure 1: Cellular-technology generations in the world-wide market in the past decades [2]

its users to transfer data through the web. High-speed data transfer was one of the most significant factors that resulted in the transition to third-generation (3G). The fundamentals and standards of 3G technologies were built by International Mobile Telecommunication - 2000 (IMT-200), and The 3rd Generation Partnership Project (3GPP). 2G devices suffered from multipath delay spread, and band compression of voice that affects the cost of the system and the cost of service. Considering these effects alongside the limited frequency spectrum, efficiency in the utilization of the network became another driving force for 3G technologies. The usage of wideband CDMA (WCDMA) made it possible to obtain mobile data rate up to 2 Mbps [3]. The improvements obtained by 3G technologies enabled their users to have a live video conference or make a video call, watch TV from the internet, and play online games.

International Telecommunication Union - Radiocommunication Sector (ITU-R) targeted maximum data rate as 100 Mbps for mobile communication and 1 Gbps for immobile, fixed communication networks with IMT-Advanced standards for 4G. 4G technologies are based on the Orthogonal FDMA (OFDMA) method. Internet Protocol (IP) packet switching is fundamental in all 4G networks. The channel capacity or coverage is adjusted dynamically by changing the user patters to avoid congested communication links [3]. With 4G technologies, The major issues with 4G communication systems are reduced battery life due to increased power consumption, and the impossibility of making voice calls in the 4G communication system during international travel without an additional software update. Shannon

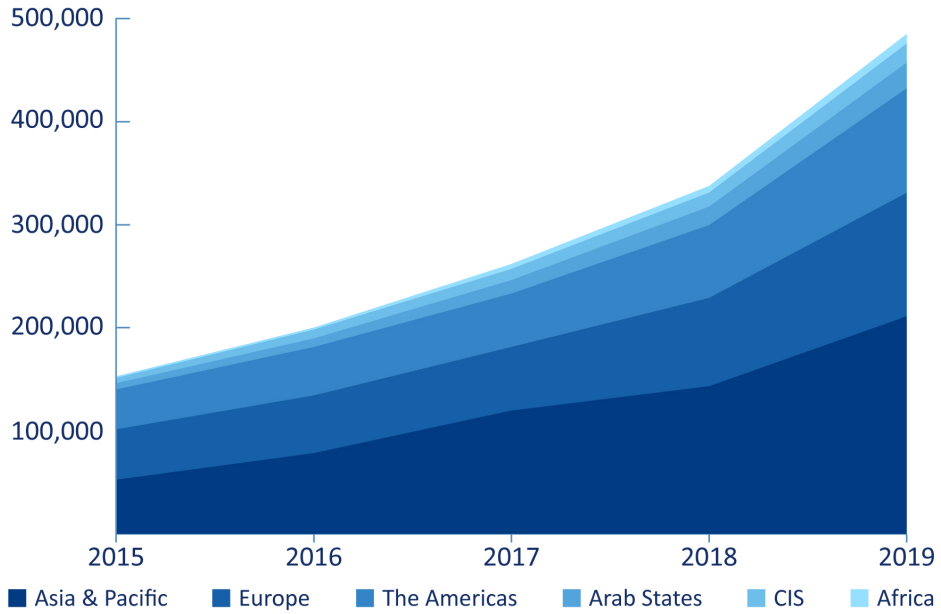


Figure 2: Bandwidth usage by region between in Gbps 2015 - 2019 [5]

capacity at the link-level, defined as the maximum transferred data without error over a communication channel, is almost reached [2].

Current technology manages to meet the demands for today's users in terms of data-rate, capacity, etc. The ever increasing demand for higher data rates and faster communication with better quality still exists and will exist in the future. According to statistics that ITU gathered, the total usage of bandwidth on the Earth has been growing. Fig. 2 indicates the bandwidth usage by region between 2015 and 2019 where the data that belong to 2019 were estimated. The total bandwidth in 2019 usage reached approximately 5 times the total bandwidth in 2015. On top of the growing bandwidth, the number of internet users has been gradually increasing from 16.8 billion in 2005 to 53.6 billion in 2019 as shown in 3. Also, the current trend in the subscriptions is on the side of mobile subscriptions. The data in Fig. 4, which demonstrates the change in the mobile and fixed subscriptions, support the statement about the trend in the subscriptions [5]. Mobile-cellular telephone subscriptions have been increasing regularly while fixed telephone subscriptions have been declining. On the other hand, the data indicate a rise in both fixed and active mobile-broadband subscriptions. The increase in fixed-broadband subscriptions is a way slower than in active-mobile broadband subscriptions that have been increasing dramatically.

The demands from the communications systems are not the only reason for a revolutionary move but also anticipated application areas are other driving forces. In addition to wide-area coverage consideration, other considerations such as dense

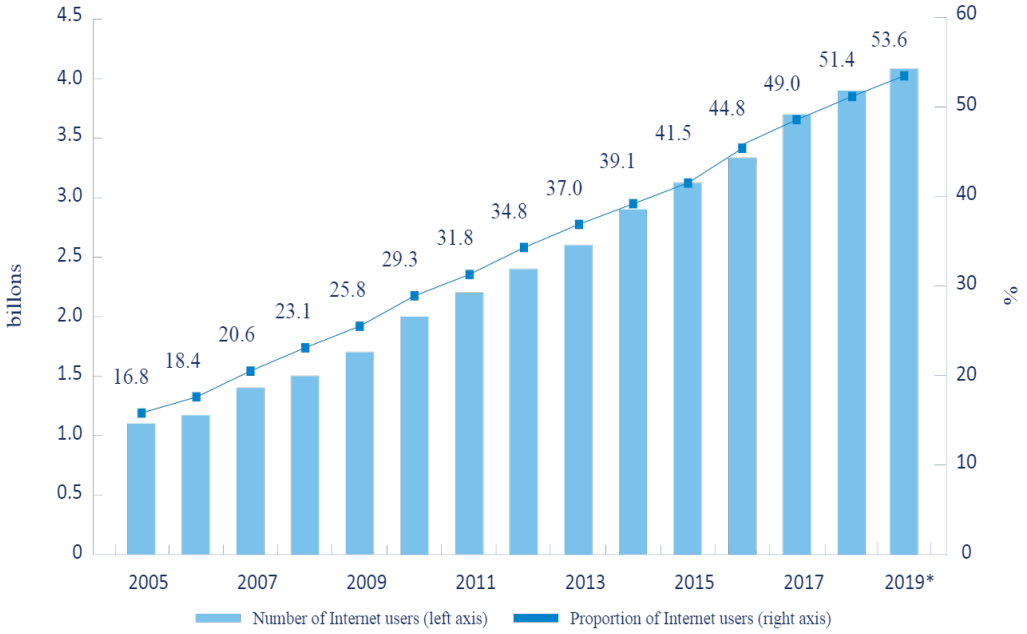


Figure 3: The number of people using internet in 2005-2019 [5]

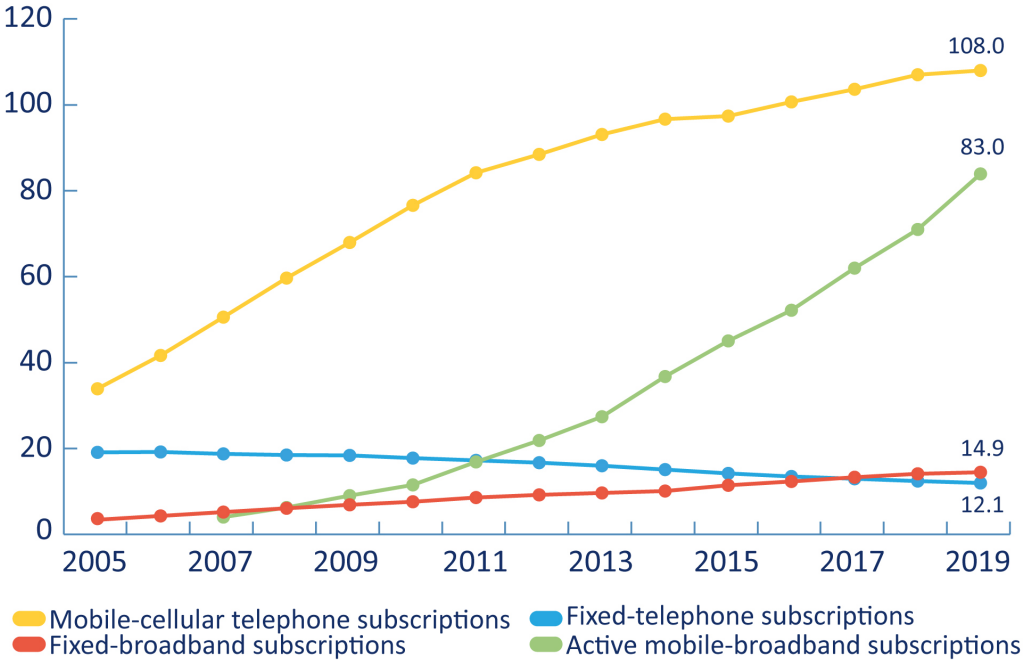


Figure 4: Evolution of mobile and fixed subscriptions between 2015-2019 [5]

hot spots, machine-to-machine communications, vehicle-to-vehicle communications, and outdoor big gathering have arisen with the offered application scenarios for 5G [6]. Industry 4.0, transportation, healthcare systems, video services such as immersive Ultra High Definition (UHD) and three dimensional (3D) video, mobile cloud, virtual reality, augmented reality, and smart home are some of the significant areas that 5G technology will play a key role in as shown in Fig. 5 [7].



Figure 5: Application areas of 5G [7]

ITU has worked on the specifications to meet the increasing demands and to provide infrastructure for the application areas. The specifications have been updated during these studies. The latest specifications determined by ITU in IMT-2020 are demonstrated in Fig. 6: Peak data rates up to 20 Gb/s, 100 Mb/s of user experienced data rate, three times the spectral efficiency of IMT-Advanced, 100 times the network energy efficiency of IMT-Advanced, mobility up to 500 km/h, around 1 M simultaneous connections per km^2, close to 10 $Mbit/s/m^2$ area traffic capacity, and latency less than 1 ms [7]. To satisfy these specifications, the use of new techniques such as full-duplex, millimeter-waves (mm-Waves), and massive Multiple-Input-Multiple-Output (MIMO) has become inevitable [7]. One of the important improvements that full-duplex and massive MIMO brings is increased spectral efficiency. The utilization of mm-Waves will enable us to use more bandwidth and to obtain higher data-rates.

1.2 SiGe BiCMOS Technology

IC designs rely on three major technologies: III-V technologies (such as gallium-arsenide (GaAs) and indium-phosphate (InP)), CMOS technologies, and SiGe BiCMOS technology. III-V technologies have superiorities over other technologies in terms of higher gain, lower noise figure (NF), and higher output power which are critical for RF IC frontends. Even though III-V technologies offer better performance, their higher defect densities, proneness to breakage results in a more difficult fabrication process. Also, they suffer from low yield property [8]. These difficulties

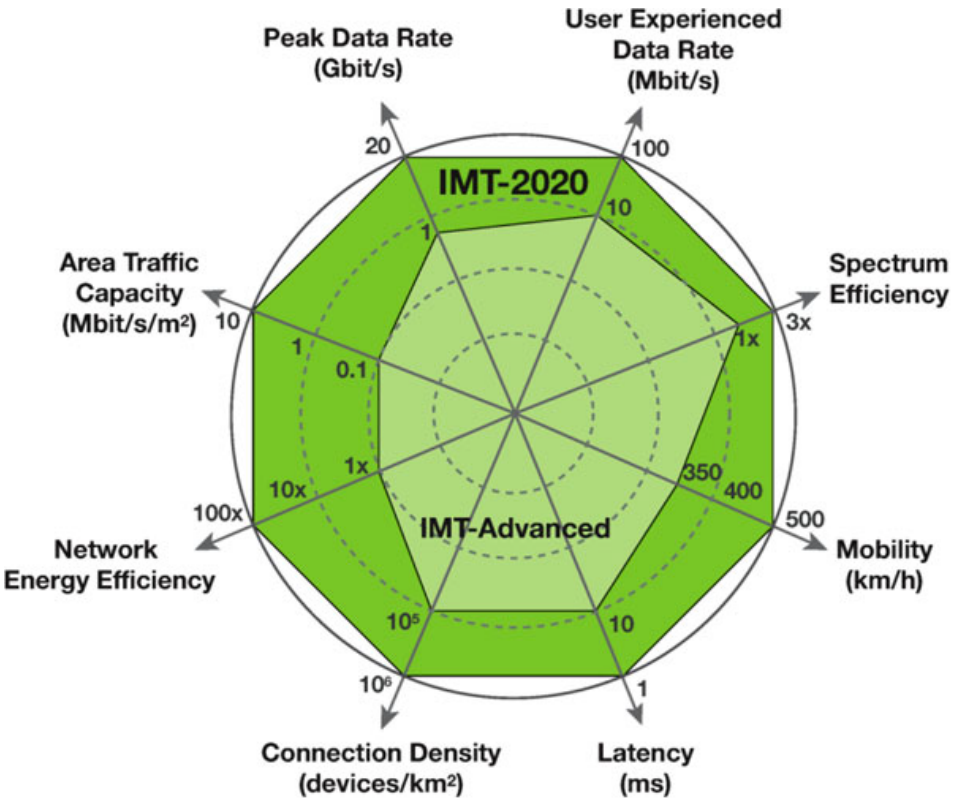


Figure 6: Improvements of significant features from IMT-Advanced to IMT-2020 [7]

increase the cost of fabrication dramatically. Their higher cost prevents them to be used in industries that require mass production. The integration of III-V technologies to the other technologies is not possible which leads to that each sub-block is designed in separate ICs to obtain adequate system performance. The higher output power of III-V technologies enables them to be selected in high power applications such as in base stations.

Si is one of the most abundant materials on Earth. The capability of defect-free larger Si wafers contributes to an increase in ICs in a wafer. Thanks to these properties of Si, CMOS technologies offer the lowest cost among these technologies [8]. Recent improvements in f_T, f_{max} and NF_{min} of CMOS technologies have made them better choice for high frequency communications systems. Since the dominant technologies in the digital IC industry are CMOS technologies, the integration level is high. Therefore, the idea of "system-on-a-chip" is achievable. However, these technologies suffer from process variations. The deviations in parasitic capacitance and resistance values change the performance of the designed circuits. This situation generates a reliability issue for these technologies.

SiGe BiCMOS technology emerged to increase the performance of Si technolo-

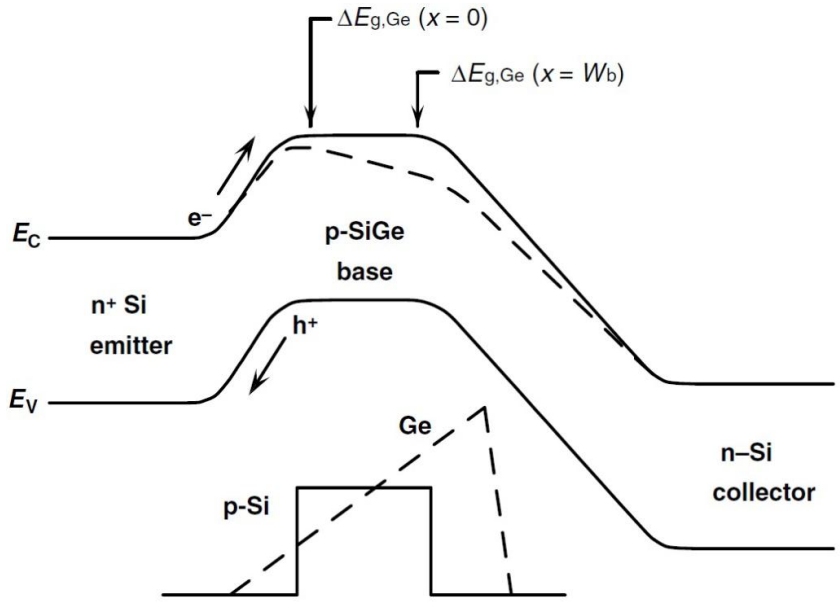


Figure 7: The representation of the energy band diagram of SiGe HBT (top) and Si BJT (bottom) [9]

gies by adopting bandgap engineering. SiGe alloy is grown epitaxially in this process. The bandgap energy of Si and Ge is 1.12 eV and 0.66 eV, respectively. Introducing more Ge leads to a reduction in the bandgap energy of the alloy. Having a smaller bandgap will increase the electron injection in the device. This increase will result in a higher current gain, Beta. Moreover, the introduction of Ge is done in a graded way as shown in Fig. 7 instead of making it constant to construct a built-in potential which accelerates the minority carriers in the base region. Thus, the base transit time, τ_b, of these carriers will be reduced. Forming graded SiGe alloy in the base region increases the fabrication cost. Yet, the fabrication is found as cheap compared to III-V technologies. SiGe technologies do not suffer from low yield numbers as III-V technologies and process variations as CMOS technologies. The performance of SiGe technology competes with the performance of III-V technologies. The effect of these extra processes on pure Si wafer can be seen in the expressions of f_T, f_{max} and NF_{min}. f_T and f_{max} are considered as critical parameters that indicate the frequency limit of an electronic device. f_T is the frequency where the short circuit current gain drops to unity. f_T formula is given in equation (1) where τ_b and τ_c are the base and collector transit time, g_m is the transconductance of the device, C_π and C_μ are base-emitter and base-collector capacitances respectively, and r_e and r_c are emitter and collector resistances [9]. f_T can be modified during the design phase since g_m and the capacitance values depend on bias and device size. However, the designer cannot change the transit times because it is process dependent. Reduced base transit time due to graded doping of Ge contributes to an increase in f_T as

equation (1) indicates.

$$f_T = \frac{1}{2\pi}\left(\tau_b + \tau_c + \frac{1}{g_m}\left(C_\pi + C_\mu\right) + \left(r_e + r_c\right)C_\mu\right)^{-1} \tag{1}$$

The other critical frequency parameter, f_{max}, is the maximum oscillation frequency. The formula of f_{max} is presented in equation (2) where r_b is the intrinsic base resistance. The improvement in f_T will increase in f_{max} since they are proportional. Adjustments can be made in Ge grading in the base region to reach higher doping levels. As a result, the lower values of the intrinsic base resistance can be obtained which translates to higher f_{max} without sacrificing the current gain. On the other hand, lower intrinsic base resistance in Si BJTs can be obtained by increasing the dopants in the base region as well. The cost is the reduction in the current gain.

$$f_{max} = \sqrt{\frac{f_T}{8\pi C_\mu r_b}} \tag{2}$$

The last one of the figures of merit mentioned above is the minimum achievable noise figure, NF_{min}. The formula of NF_{min} is given in equation (3) where β_{DC} is the DC current gain, J_c is the collector current density, and n is emitter-base junction ideality factor. As in the f_T case, the designer has a room for control over NF_{min} by adjusting J_c or β_{DC}. However, since the intrinsic resistances and threshold voltage are process dependent, the designer cannot play with them. Reducing r_b without the deterioration of the current gain in SiGe HBT unlike in a normal Si BJT improves NF_{min}. Also, one can say that higher f_T results in lower NF_{min}.

$$NF_{min} = 1 + \frac{n}{\beta_{DC}} + \sqrt{\frac{2J_c}{V_t}\left(r_e + r_b\right)\left(\frac{f^2}{f_t^2} + \frac{1}{\beta_{DC}}\right) + \frac{n^2}{\beta_{DC}}} \tag{3}$$

Relative performance comparison of numerous IC technologies is presented in Table 1. To summarize, III-V technologies have performance advantages over other technologies but, their high cost and low yield numbers limit their usage to application-specific designs such as power amplifiers with high output power. Despite the advances in CMOS technologies, process variations remain the main drawback of these technologies. Nowadays, RF IC front-ends can be designed in SiGe BiCMOS technology with low cost and high integrability, and comparable performance to III-V technologies.

Table 1: Performance comparison of numerous device technologies for radio frequency integrated circuits (Excellent: ++; Very Good: +; Good: 0; Fair: -; Poor: --) [8]

Performance Metric	SiGe HBT	SiGe BJT	Si CMOS	III-V MESFET	III-V HBT	III-V HEMT
Frequency Response	+	0	0	+	++	++
1/f and Phase Noise	++	+	–	– –	0	– –
Broadband Noise	+	0	0	+	+	++
Linearity	+	+	+	++	+	++
Output Conductance	++	+	–	–	++	–
Transconductance	++	++	– –	–	++	–
Power Dissipation	++	+	–	–	+	0
CMOS Integration	++	++	N/A	– –	– –	– –
IC cost	0	0	+	–	–	– –

1.2.1 IHP 0.13 μm SiGe BiCMOS (SG13S) Tehcnology

In this thesis work, IHP Microelectronics 0.13 μm SG13S technology process was preferred. It is reported that IHP's 0.13 μm SiGe BiCMOS technology provides HBTs with f_t/f_{max} of 250/340 GHz and BV_{CEO} of 1.7 V. The cross-section of the SG13S process is illustrated in Fig. 8. The process consists of five thin (M1-M5) and two thick metal (TM1-TM2) layers. The thick metal layers are located at the top. TM1 and TM2 are generally used to implement high quality-factor inductors and low loss transmission lines. The metal-insulator-metal (MIM) capacitor resides between TM1 and M5. The process offers three different polysilicon resistors (rsil, rppd and rhigh).

1.3 Motivation

The challenging specifications such as higher data-rate and network capacity for the next generation (5G) technologies resulted in both academia and industry to pay more attention to full-duplex methods for 5G technologies since 5G technologies will spread every part of the human life and full-duplex operation improves the spectral efficiency. It is expected a transceiver to have low cost, high performance, and high integration. Nowadays, the techniques for full-duplex operation employ heavy, large, and expensive components with low integration levels. Recent research has focused on integrated on-chip duplexers to lower the cost and area. High-cost and low-yield numbers of III-V technologies and process variations in CMOS technologies prevent them to be used widely in transceivers. With the improvements in SiGe BiCMOS technology, it offers comparable performance to III-V technolo-

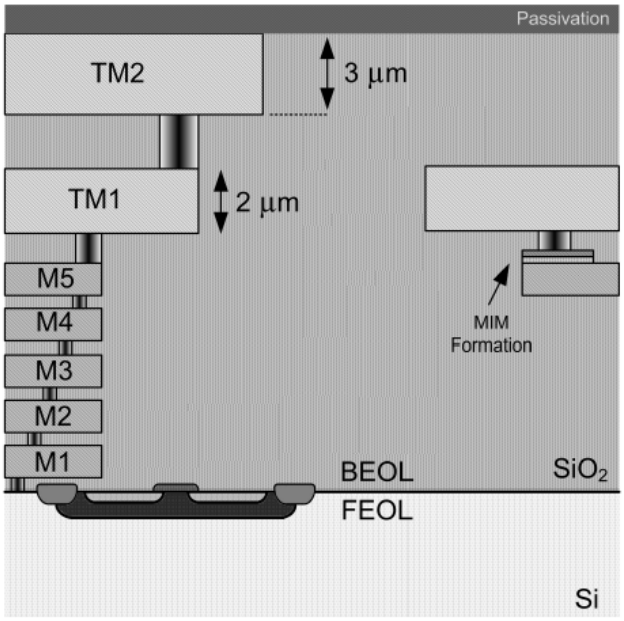


Figure 8: The cross-section of IHP's 0.13 μm SiGe BiCMOS SG13S technology [10]

gies with low cost and high integration level close to CMOS technologies. Due to these features of SiGe BiCMOS technology, it would be the best candidate for 5G transceivers.

The main objective of this thesis is to design a core chip block that employs In-Band Full-Duplex (IBFD) operation at 28 GHz for 5G communication systems. Electrical Balance Duplexer (EBD) is utilized to enable to have a single antenna rather than two antennas which separate TX and RX. Employing a single antenna reduces the size and cost of the product. The first prototype contains a hybrid transformer (HT), an impedance tuner, a low noise amplifier (LNA), and a power amplifier (PA). After testing the first prototype, the system was extended with an up and down converter mixer to obtain TX input and RX output at an intermediate frequency (IF).

1.4 Organization

The rest of this thesis is organized as follows: Chapter 2 provides fundamental information about the types of communication links and duplexing theory. Different types of duplexers are briefly explained. Electrical Balance Duplexer (EBD) working principle and design are analyzed with the inductance equations.

Chapter 3 contains the analysis and simulation of the designed IBFD core chip for 5G communication systems. At the beginning of this chapter, the system-level considerations of the designed system are described. Then, the design of the hybrid transformer is presented with the simulation results. The core of the system is completed with the explanation of the designed balancing network. The prototype for IBFD core chip at 28 GHz, which contains an HT, an LNA, a PA, an impedance tuner, was fabricated and measured. The measurement results will be provided in this chapter. The chapter continues with the design of the extension of the prototype, which contains downconverter and upconverter mixers, Single-Pole-Double-Throw (SPDT). Finally, the performance comparison of the proposed system with state-of-the-art works is demonstrated.

Chapter 4 provides a summary of the work and opens up a discussion for the limitations and possible solutions to these limitations. A list of future work finalizes the thesis.

2 Background

2.1 Duplex Systems in Communication Links

Duplex is a telecommunication term that refers to two way point-to-point communication between two or more devices. Each end-point device has the capability to send and receive information so that the communication can be established in both directions. Telephone links and walkie-talkies are examples of duplex communication systems. Duplex communication systems are divided into two with respect to the time and frequency that communication happens.

2.1.1 Half-Duplex vs. Full-Duplex

A half-duplex system is a two-way communication system which does not employ simultaneous transmission and reception at the same carrier frequency. In other words, one device in a communication network can only send or receive information at a time instant. Transmission and reception for a device happen by turn-based plan, as shown in Fig. 9. Both operations cannot be active at the same time. This operation is named as Time Division Duplexing (TDD). One way to establish TDD is to employ an SPDT switch between transmitter (TX) and receiver (RX) chains, and antenna as shown in Fig. 9. The connections between TX and antenna, and RX and antenna are controlled by the switch that allows only one of the chains. The insertion loss (IL) in the on-mode of the switch and the isolation in the off-mode of the switch are important parameters for the SPDT block. IL of the switch reduces the maximum obtainable output power for the TX side and degrades the NF of the RX side. Therefore, it should be minimized. Low isolation would lead to leakage from TX to RX. Walkie-talkies are a good example of half-duplex systems. Walkie-talkies have a push-to-talk button to send information by pressing on it. Releasing it changes the operation to the reception.

A full-duplex system is a two-way communication system in which transmission and reception occur simultaneously. Utilizing different frequency bands for each operation is required for the separation of transmission and reception operations as represented in Fig. 10. This operation is named as Frequency Division Duplexing (FDD). Fig. 10 demonstrates the block diagram of a full-duplex communication system. FDD has some challenges. One of these challenges can be stated as the bandwidth of the antenna. The antenna should work in both transmit and receive frequency bands. Designing an antenna with a large bandwidth would be problem-

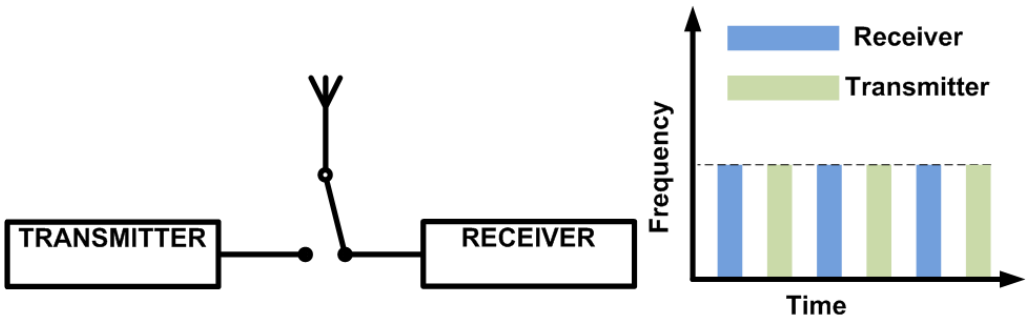


Figure 9: The block diagram and illustration of half-duplex communication

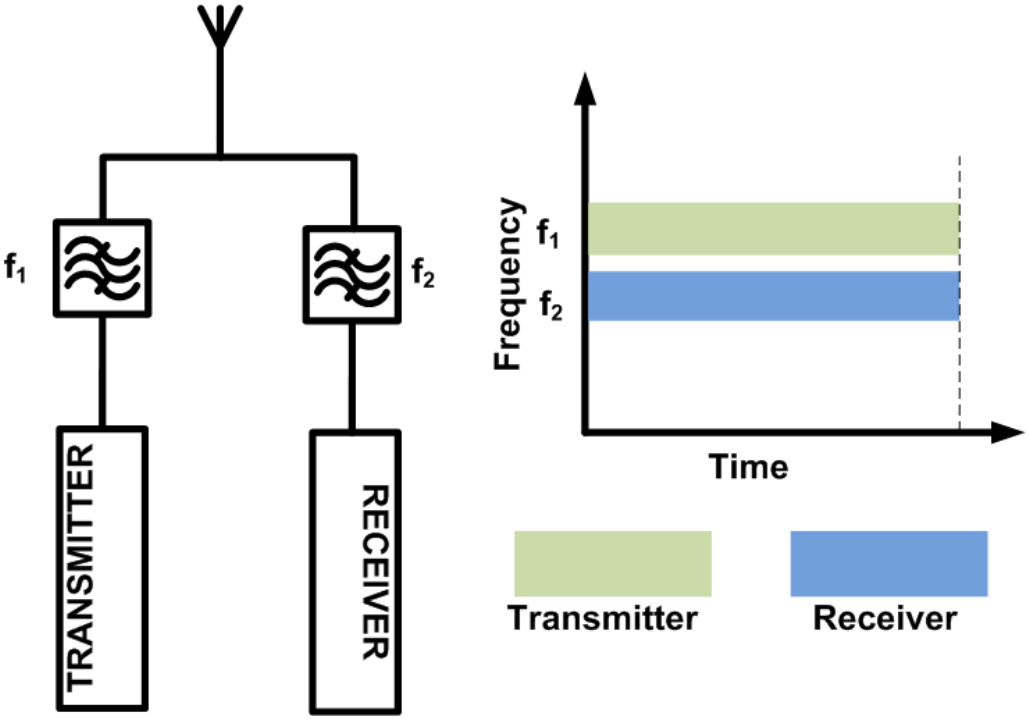


Figure 10: The block diagram and illustration of full-duplex communication

atic. Another challenge is that the system requires very sharp filters such as Surface Acoustic Wave (SAW) filter. However, they are bulky and expensive. The telephone is an excellent example of a full-duplex communication device. Two or more people can talk with and listen to each other on the phone at the same time.

2.2 Duplexers

As far as duplexing concerned, the time and bandwidth are the resources of the communication link. The systems that operates in half-duplex are very common today's wireless communication [7]. Both FDD and TDD cannot use spectral density with full capacity since both of them cannot transmit and receive simultaneously and

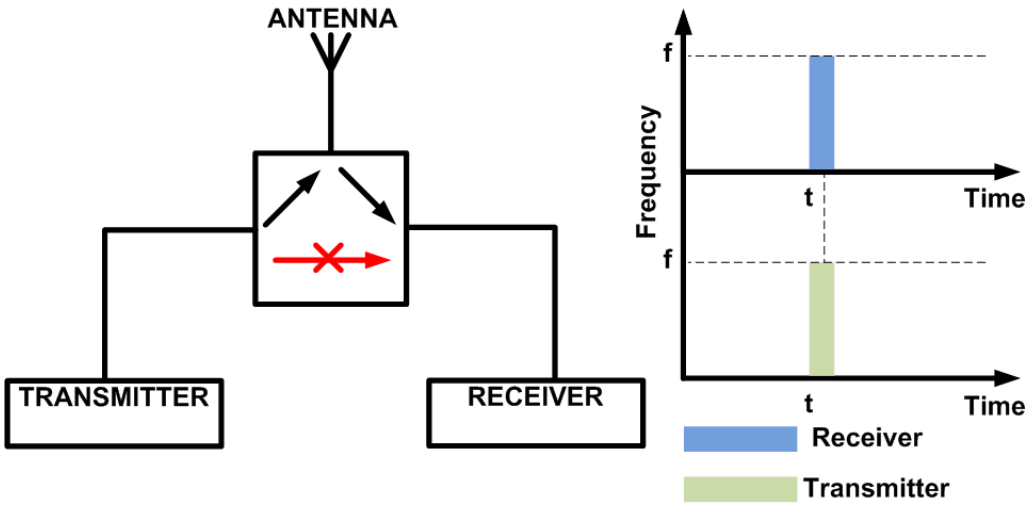


Figure 11: The block diagram and illustration of in-band full-duplex communication

the same frequency bands. FDD sacrifices bandwidth by distinguishing frequency bands for transmission and reception whereas TDD sacrifices time by separating the time intervals of transmission and reception. In order to meet the specifications for 5G, simultaneous transmission and reception must be enabled at the same frequency by increasing the spectral efficiency. In-band full-duplex communication systems allow simultaneous transmission and reception at the same frequency band by its definition. The frequency and time usage of IBFD systems are shown in Fig. 11.

The output signal of the transmitter must reach high power levels to establish communication from a distance. However, this strong output signal may leak to the receiver. Otherwise, the leaked signal will lead to the desensitization of the receiver and the degradation of the Signal-to-Noise Ratio (SNR). The most significant problem in IBFD systems arises from this leakage referred to as Self-Interference. The interference should be suppressed to the level lower than the noise floor to limit the effects of the interference on the SNR deterioration up to 0.5 dB [11]. The required suppression of the interference can be done with the techniques from three domains: propagation domain, (antenna separation, duplexers), analog domain, and digital domain [7]. Employing a separate antenna for each operation (TX and RX) would relax the system specifications. However, this will increase the size of the system, which translates to the increased cost.

A duplexer is a three-port block to allow IBFD operation. The duplexer resides between antenna, transmitter, and receiver, similar to the switch in TDD systems. The block diagram of IBFD systems is shown in Fig. 11. Similar to the switch, the duplexer must provide low IL between antenna and TX, and antenna and RX. The duplexer must suppress the transmitter output signal to leak into the receiver chain

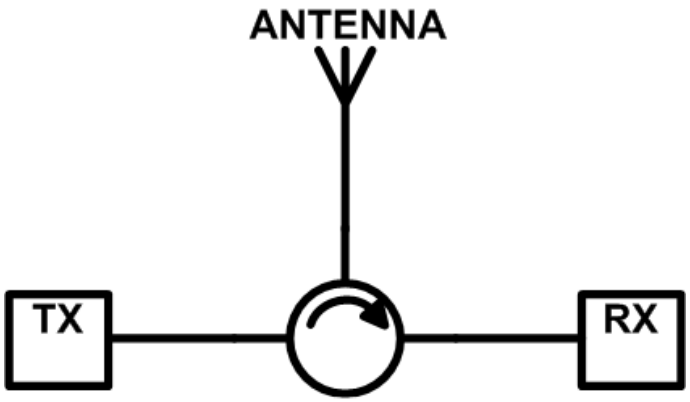


Figure 12: The block diagram of full-duplex communication with circulator

since both transmitter and receiver operate simultaneously at the same frequency band. Due to non-idealities in the circuit components, the leakage cannot be blocked completely. Recent research has focused on the suppression of the leakage signal by employing duplexers. Widely used duplexers are transducers, circulators, and EBD in the literature [12–17].

2.2.1 Circulators

A circulator is a three-port device that can be used as a duplexer since the circulator allows the transmission of a signal in only one direction between two ports while the other port is left isolated. From this definition, it can be stated that a circulator is also non-reciprocal. The block diagram of a circulator-based full-duplex communication system is illustrated in Fig. 12. In this figure, the rotation is clockwise. As Fig. 12 demonstrates the output signal of the transmitter is directed only to the antenna, the incoming signal to the antenna flows to the receiver, and any reflected signal at the receiver input goes to transmitter output. The IL in the first two situations must be low not to degrade the output power of the transmitted signal and the NF of the receiver. However, the last situation, which is the flow of the reflected signal at the receiver input due to the incoming signal to the communication system, may generate an issue that leads to malfunction in the system. The ideal S-matrix of a circulator is given in (4). The isolation is in the range of 20 dB to 60 dB depending on the size and cost [18].

$$S = \begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \tag{4}$$

Conventional circulators are based on ferromagnetic material that offers low IL and high-power handling capability [12]. However, they are bulky and expensive. Also, their integration is not feasible. On the other hand, recent studies have shown that the use of active devices in the on-chip implementation of circulators is possible [12–14, 19]. The impedance mismatch at the ports of the circulator has a huge impact on the isolation. Even though on-chip circulators provide compact and cheap solutions, they suffer from high insertion loss and narrow bandwidth.

2.2.2 Electrical Balance Duplexers

Another electronic device utilized as a duplexer is EBD that has four terminals: transmitter (TX), receiver (RX), antenna, and balance (BAL) terminals. The reason to have four terminals is that the hybrid transformer is the core of the EBD. The block diagram of a typical EBD constructed with hybrid transformers is shown in Fig. 13. The output of the transmitter is connected to the center tap of the hybrid transformer as shown in Fig. 13. The suppression of the high-power transmitted signal is possible when the transmitted signal from the PA is divided equally between the antenna and balance port. The equal division between the antenna and balance port takes place when the impedance values of the antenna and balance port are the same. However, the antenna impedance depends on the environmental changes such as user interaction [15]. The variance in the antenna impedance should be tracked by the balance network to keep the isolation high since isolation is obtained when these impedance values are equal.

The duplexer must provide low IL, high linearity, and high isolation in the targeted bandwidth [15]. The quality factor and capacitive coupling to the substrate of the inductor in the hybrid transformer limit the performance of the EBD by increasing the IL and degrading the isolation. Lately, the EBD draws the attention in the literature due to high integration capability for the frequencies lower than 3 GHz [15–17]. Employing dual-notch widens the bandwidth up to 160 MHz while providing isolation more than 40 dB [20]. Moreover, it is shown that EBD is promising for high frequencies [21]. The analysis of a hybrid transformer is provided in the next section.

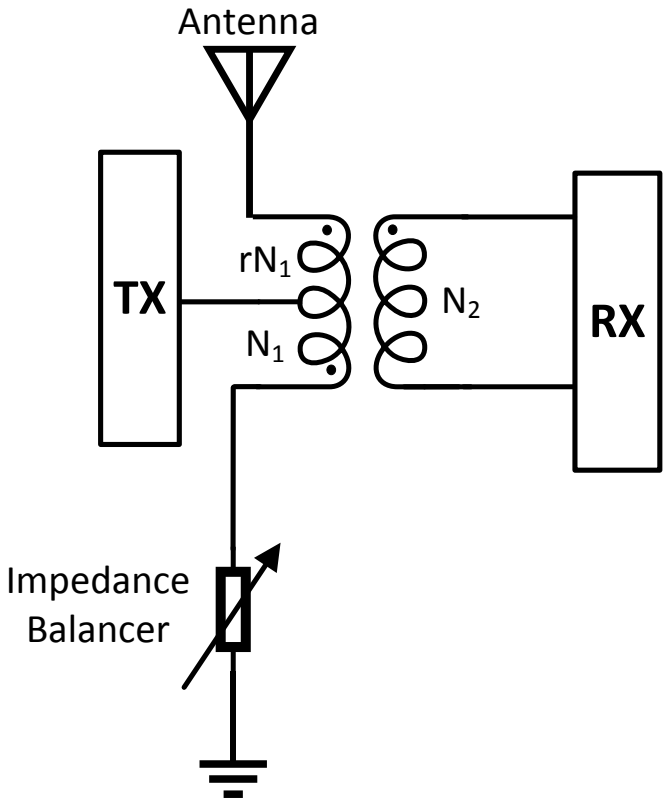


Figure 13: The block diagram of a typical EBD constructed with hybrid transformers

2.3 Hybrid Transformers

Hybrid transformers are not a new concept in the literature. They had been utilized widely in the telephone plant [22]. The hybrid transformers have regained popularity among the researchers with the increased demand for full-duplex operation since they enable simultaneous transmission and reception in the same frequency bands with SI cancellation up to decent levels.

As mentioned before, the four ports of the hybrid transformer employed in an EBD are connected to TX, RX, antenna, and the balance network as shown in 13. The hybrid transformer is constructed by two center-tapped coils. Generally, TX is connected to the center-tap of the primary coil. The antenna port and the balance network reside at the other terminals of the primary coil. Two ends of the second coil are the input connection of the RX.

The output signal of TX is divided into two paths: to the antenna and balance network. By assuming the hybrid transformer ideal, which means that it does not

cause additional IL due to the parasitic effects, the total power delivered to the antenna (P_{ANT}) and balance network (P_{BAL}) is equal to the power of the output signal of TX as shown in (5) [22]. In order to use generic expressions for a hybrid transformer, the center-tap is not placed in the middle of the primary coil. In other words, the primary coil is divided into two pieces with a power ratio, r, that is the ratio of P_{ANT} to P_{ANT} as given in (6). By combining (6) and (5), (7) and (8) can be obtained to find the relations between P_{ANT}-P_{TX}, and P_{BAL}-P_{TX}. The insertion loss in the TX path is defined as in (9).

$$P_{TX} = P_{ANT} + P_{BAL} \tag{5}$$

$$r = \frac{P_{ANT}}{P_{BAL}} = \sqrt{\frac{L_{ANT}}{L_{BAL}}} \tag{6}$$

$$\frac{P_{ANT}}{P_{TX}} = \frac{r}{r+1} \tag{7}$$

$$\frac{P_{BAL}}{P_{TX}} = \frac{1}{r+1} \tag{8}$$

$$IL_{TX} = 10log\left(\frac{r+1}{r}\right)[dB] \tag{9}$$

Hybrid transformers have a number of common characteristics that make them very useful in full-duplex systems. The first characteristic of the hybrid transformers is biconjugacy. The four ports of the hybrid transformer are defined as TX, RX, antenna, and balance port previously. When the balance between the antenna and balance port is satisfied by adjusting these port impedances as equal, TX and RX ports become conjugate under the ideal transformer condition. In other words, a signal coming out from TX-port cannot reach to the RX-port. If similar arrangements are done at the TX and RX terminations, the antenna and balance ports are also referred to as conjugate ports [22].

Another characteristic is the equality of the insertion losses in between the RX and balance port, and the TX and antenna port under the biconjugacy conditions [22]. Similar to the transmitted signal perspective, the set of equations can be written for the incoming signal to the antenna. The incoming signal is divided into two paths: TX and RX blocks. Thanks to the second-mentioned characteristic of

the hybrid transformer, the same power ratio, r, equals to the power of the signal in the path to TX side, (P_{TX}), divided by the power of the signal in the path to RX side, (P_{RX}) in the receive operation as given in (10) [22]. The sum of P_{RX} and P_{TX} is equal P_{ANT} during receiving the signal. Considering ideal transformer properties, and (10), P_{ANT} can be related to P_{TX} and P_{RX} separately in (10) (10). From the equation (10)-(12), IL in the RX path can be written as in (13). Fig. 14 shows the insertion losses in the RX and TX paths with respect to the power ratio, r.

$$r = \frac{P_{TX}}{P_{RX}} \tag{10}$$

$$\frac{P_{TX}}{P_{ANT}} = \frac{r}{r+1} \tag{11}$$

$$\frac{P_{RX}}{P_{ANT}} = \frac{1}{r+1} \tag{12}$$

$$IL_{RX} = 10log\,(r+1)\,[dB] \tag{13}$$

The relations between the port impedances are given in (14) where Z_{TX}, Z_{RX}, Z_{ANT}, and Z_{BAL} denote the impedance at the TX, RX, antenna and balance port, respectively [22]. N_1 and N_2 are the turn ratios of the corresponding inductors in Fig. 13.

$$Z_{TX} = Z_{RX}\left(\frac{r}{(1+r)^2}\right)\left(\frac{N_1}{N_2}\right)^2 = \frac{Z_{ANT}}{1+r} = Z_{BAL}\left(\frac{r}{1+r}\right) \tag{14}$$

By utilizing inductance relationship in (6), and the impedance relationships in (14), we can obtain the impedance expressions in terms of the inductance values of the coils, and the power ratio of P_{ANT} to P_{BAL}. In this way, the determination of the inductance values would be more straightforward.

$$Z_{ANT} = Z_{RX}\left(\frac{r+1}{r}\right)\left(\frac{L_{ANT}+L_{BAL}}{L_{RX}}\right)^2 = Z_{TX}\left(\frac{r+1}{r}\right) = \frac{Z_{BAL}}{r} \tag{15}$$

The last common property of the hybrid transformers states that the phase shifts in the transition of the TX-port to the antenna, the TX-port to the balance

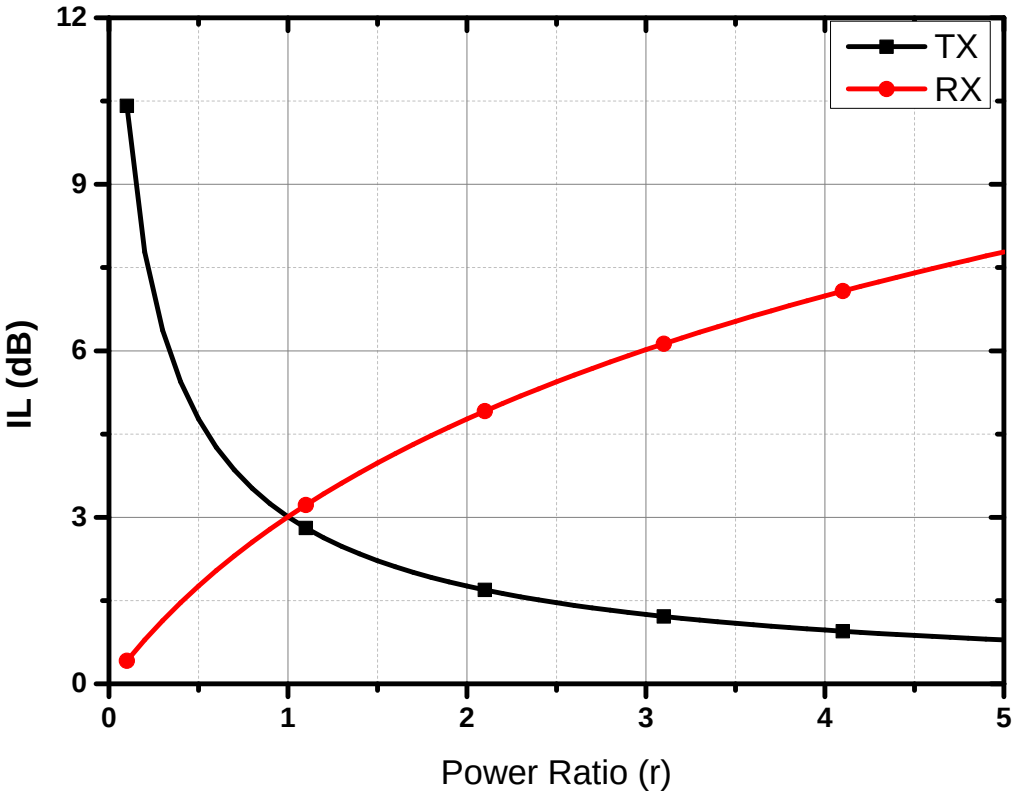


Figure 14: The insertion loss of the hybrid transformer in TX and RX path with respect to the power ratio

port, and the RX-port to the antenna are zero. On the other hand, the phase shift in the transmission from the RX-port to the balance port is 180° [22].

2.3.1 Working Principle

The working principle of the hybrid transformer is explained by separating the operations as transmit and receive. Firstly, an incoming signal will be captured by the antenna. The main objective in RX-mode is to deliver the signal to RX-chain with IL as low as possible. The RX-mode operation is demonstrated in Fig. 15. The captured signal is shown with yellow arrow numbered as 1, and the delivered signal to the RX-chain is shown with dark purple arrows numbered as 2. The grounded center-tap in the secondary coil enables to the generation of two differential signals with the same amplitude as shown in Fig. 15. Therefore, RX must operate with a differential input.

Finally, the TX-mode of operation is represented in Fig. 16 where the output signal of TX-chain is depicted with a red arrow numbered as 1. The signals delivered to the antenna and balance ports are shown with light blue arrows numbered as 2 while the leakage signal from the TX to the RX is depicted with green arrows

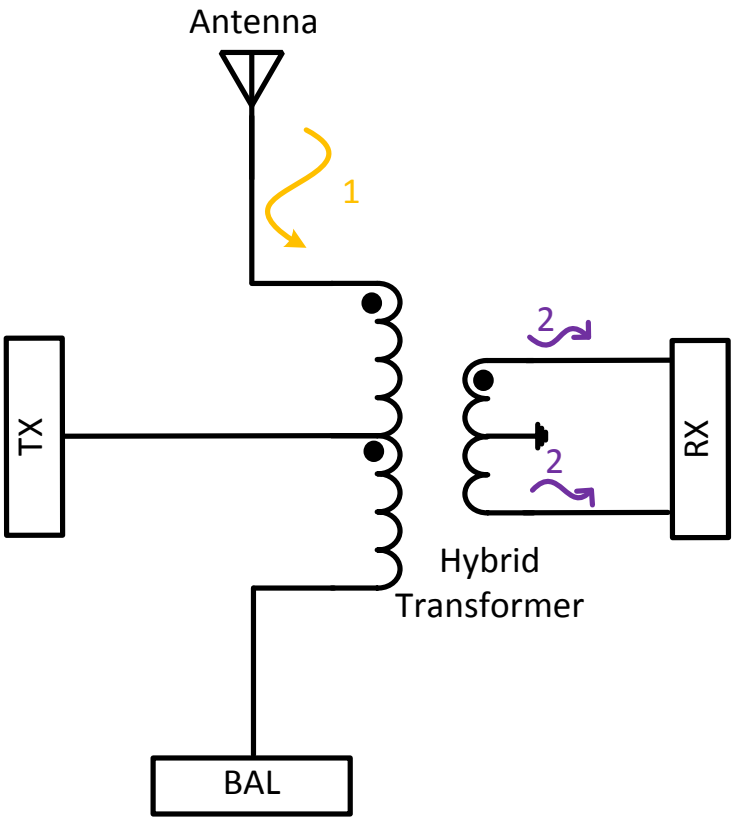


Figure 15: The illustration of the hybrid transformer operating in RX-mode

numbered as 3. The output signal of the TX, supplied to the hybrid transformer from the center-tap of the primary coil, is divided into two signals. Due to the coupling between the primary and secondary coil, the transmitted signal will leak to the RX port. If the power ratio mentioned previously is 1, the transmitted signal will be divided into two identical signals. As a result of the second-common property of the hybrid transformers mentioned in the previous section, the amplitudes of the leaked signals at the two ends of the RX port will be equal. Moreover, as the property of the hybrid transformers about the phase relations states, the leaked signals will have 180° phase difference. With the common-mode rejection ratio (CMRR) of the RX-chain, the leakage will be completely suppressed.

The explanation of the working principle of the hybrid transformer relies on the ideal transformer and the assumption of the biconjugate ports. The on-chip implementation of the hybrid transformers brings about the non-idealities such as ohmic connections and capacitive coupling to the substrate. Therefore, these non-idealities limit the suppression of the leakage signal, the NF performance of the

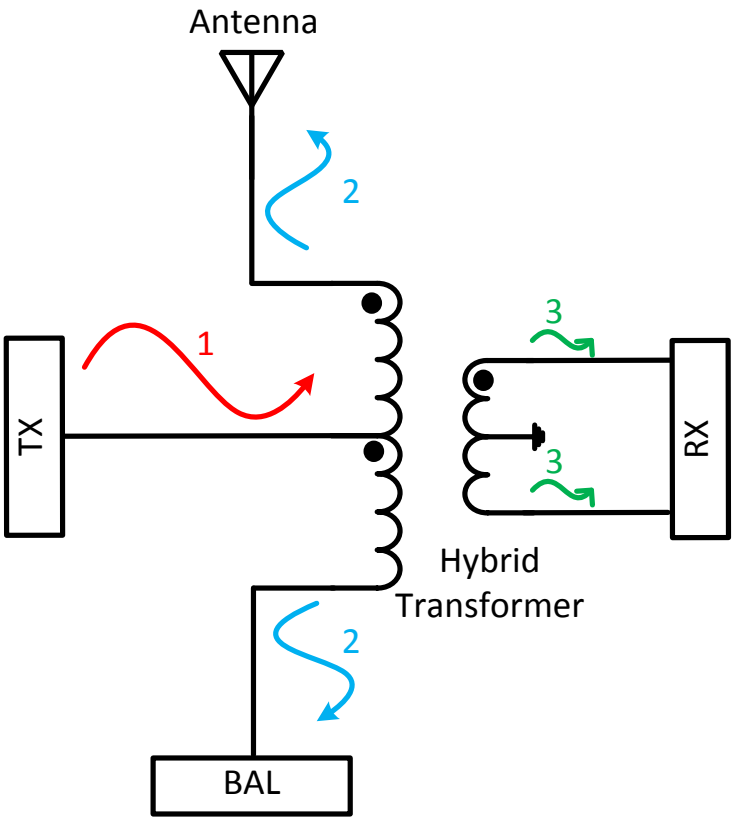


Figure 16: The illustration of the hybrid transformer operating in TX-mode

receiver, and the output power of the transmitted signal from the antenna.

2.3.2 The Balance Network

In order to suppress the leakage signal, the system should be balanced and satisfy the conditions for biconjugacy. As explained in the working principle, the impedance of the antenna and balance port should be equal. The isolation formula is given in (16) with respect to the frequency-dependent reflection coefficients at the antenna port, $\Gamma_{ANT}(\omega)$, and the balance port, $\Gamma_{BAL}(\omega)$, and the power ratio, r. The expressions for $\Gamma_{ANT}(\omega)$ and $\Gamma_{BAL}(\omega)$ are given in (17) and (18), respectively. $|\Gamma_{ANT}(\omega) - \Gamma_{BAL}(\omega)|$ in the isolation formula defines isolation circles in the Smith Chart. In other words, with a given antenna impedance, the impedance points on the Smith Chart that have equal distance to the antenna impedance offer approximately the same isolation numbers.

$$ISO_{TX_RX} = 20log|\Gamma_{ANT}(\omega) - \Gamma_{BAL}(\omega)| - 20log\left(\frac{r+1}{\sqrt{r}}\right)[dB] \tag{16}$$

$$\Gamma_{ANT}(\omega) = \frac{Z_{ANT}(\omega) - Z_0}{Z_{ANT}(\omega) + Z_0} \tag{17}$$

$$\Gamma_{BAL}(\omega) = \frac{Z_{BAL}(\omega) - rZ_0}{Z_{BAL}(\omega) + rZ_0} \tag{18}$$

Another aspect of (16) is that $|\Gamma_{ANT}(\omega) - \Gamma_{BAL}(\omega)|$ indicates the significance of the link between the difference in the port impedances of the antenna and balance port, and the isolation. The antenna impedance varies due to the change in the environmental conditions. Therefore, an impedance tuner at the balance port is required to track the changes in the antenna impedance. The tuning range, resolution of the impedance tuner have a significant impact on the isolation since the variations of the antenna impedance are unpredictable.

3 Electrical Balance Duplexer Based In-Band Full-Duplex System for 5G (28 GHz) Communication Systems

This chapter covers the construction of the designed system step by step. The workflow of the designed system is explained by providing the block diagram of the ultimate system. Considering the system level expectations, the specifications for each sub-block are determined. Starting with the hybrid transformer, the design steps and simulation results of each sub-block are provided. After the measurement results of the prototype, which consists of the hybrid transformer, impedance tuner, LNA, and PA, are presented, the extension of the prototype with frequency mixers is described. The design of both upconverter and downconverter mixers is explained. The simulation results for the extended system are demonstrated. Finally, the comparison with similar works from the literature is presented.

3.1 Design Considerations of the System

The most significant challenge in the IBFD operation is the suppression of SI. As mentioned previously, the suppression can be done in the RF domain by separating antennas or adopting a duplexer with a single antenna. The antenna separation requires two antennas for each transmit and receive operations. Adopting a duplexer has been preferred over the antenna separation method because it reduces the complexity in the system and size. Reducing the size leads to a cost-efficient system. The duplexer types are mentioned in the previous chapter. Due to the disadvantages of circulators such as non-integrability and high cost, EBD has been chosen as the duplexer in the designed system. Most importantly, EBD provides high SI cancellation (SIC) which is crucial for IBFD operation.

The block diagram of the system is shown in Fig. 17. A signal, which will be transmitted, reaches the input of the upconverter mixer from TX IN. The frequency of this signal is 3.3 GHz defined as an intermediate frequency (IF). The upconverter mixer takes the input signal at IF and converts it to a signal in between 27 and 29 GHz frequencies referred to as RF. An external local oscillator (LO) is used in this process. The frequency range of the LO can be at the upper or lower side of the RF band. The upper-side injection is selected to reduce the area of the filter and to ease the design of filters shown in Fig. 17. The output of the upconverter will be filtered to eliminate undesired signals. The filtered signal is transmitted to PA to

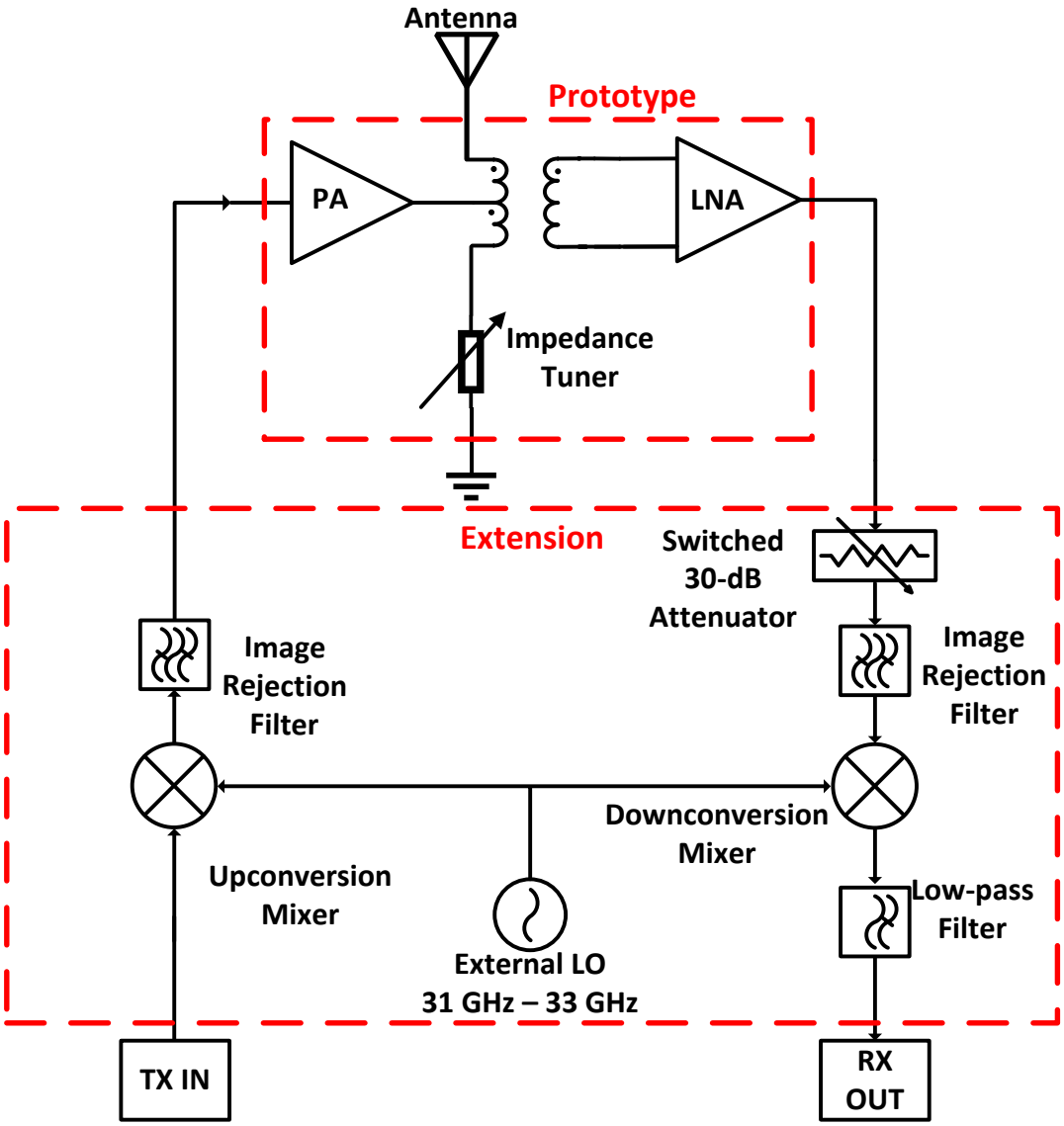


Figure 17: The block diagram of the system

be amplified before sending the signal from the antenna. The PA output is divided into two paths that go to the antenna and balance ports.

The hybrid transformer converts the incoming signal to a differential signal and transmits it to LNA. Therefore, the input of the LNA must be differential. In the meantime, the leakage from the TX also appears at the input of the LNA. As a result, the LNA must handle with a high-power input signal. If the leakage could not be suppressed, there will be a strong signal at the output of the LNA that may saturate the downconversion mixer. To prevent the saturation of the mixer, an SPDT serves as a switched attenuator to reduce the power of the signal at the output of the LNA. Considering the limitations of -14 dBm for the output power of the RX chain and the minimum isolation that the hybrid transformer can provide,

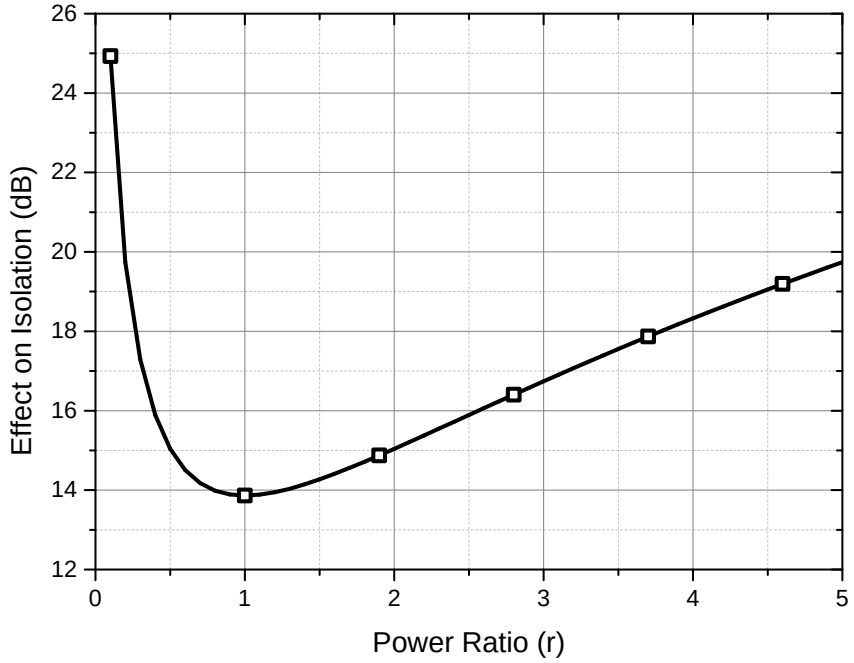


Figure 18: The effect of the power ratio on the isolation

the attenuator step is determined as 30 dB with a margin. An image rejection filter eliminates frequency elements other than the RF band. Downconversion mixer shifts the frequency of the input signal to IF by utilizing the LO signal that is common in the TX chain. The low-pass filter ensures that only the frequency elements in the IF band appear at the RX OUT.

The performance parameters for the hybrid transformer should be determined first since it is the core of the system and the gate to the environment. The IL in the TX and RX paths is significant because it cannot be compensated by any other block. The IL of the hybrid transformer in the RX path is directly added to the NF of the RX. Moreover, the output power of the system is reduced with the same amount of IL in the TX path. Considering the relationship between the power ratio and IL in the TX and RX paths shown in Fig. 14, the power ratio is selected to be as one where IL in both paths is theoretically the same, 3 dB. This selection affects the minimum isolation that the system can provide. In (16), the first term depends on the impedance mismatch between the antenna and balance port whereas the second term indicates the relationship between the isolation and power ratio. The effect of the second term, $20log\left(\frac{r+1}{\sqrt{r}}\right)$, is presented in Fig. 18. Even though the minimum is obtained when the power ratio equals to 1, the benefits of selecting another value do not match with its loss. For example, the power ratio is chosen as 3 that leads to approximately 1 dB IL in the RX path and extra 3 dB isolation. However, the power of the transmitted signal will be reduced by 3 dB. The 3 dB reduction in isolation can be tolerated by decreasing the impedance mismatch. On the other hand, the

reduction in the output power of the system cannot be compensated. Therefore, the power ratio is selected to be 1. The inductance values of L_{ANT} and L_{BAL} should be equal. By selecting L_{RX} as two times of L_{ANT}, the equation (15) can be rewritten as in (19).

$$Z_{ANT} = Z_{BAL} = 2Z_{TX} = \frac{Z_{TX}}{2} = 50\Omega \tag{19}$$

(19) indicates that lower impedance at the output of the PA and higher impedance at the input of the LNA. The lower impedance at the output of the PA ease to obtain high output power. The differential 100 Ω leads to an improvement in the gain and NF of the LNA.

The target for the output power of the system is 10 dBm. The PA is expected to provide 15 dB gain with approximately 14 dBm output compression point. The difference between the target for the system and PA arises from the duplexer. To reach these goals, the upconversion mixer must have high linearity so that, the gain of the PA would be enough to obtain 14 dBm at the output. Therefore, the linearity becomes the priority in the design of the upconversion mixer.

In general, NF and gain are the main considerations for an LNA design. On top of these parameters, LNA must deal with high-input power when the SIC cannot be satisfied by the EBD due to an impedance mismatch between the antenna and balance ports. The leakage may cause a strong signal at the output of the LNA. Similar to the upconversion mixer, the downconversion mixer prioritizes linearity. To reach higher linearity levels, the IL is sacrificed in the design of the downconversion mixer. The required linearity for the downconversion mixer is higher than the upconversion mixer. The design considerations for the filters are the rejection of the out-of-band signals and IL in the desired band.

3.2 The Prototype of IBFD System for 5G Communication Systems

3.2.1 Hybrid Transformer Design

The IL in the RX and TX paths and the isolation between the TX and RX ports are crucial parameters that must be paid attention to in the design process. The theoretical bounds for IL in the TX and RX paths are dependent on the power and turn ratios. The power and turn ratios of the hybrid transformer are determined in

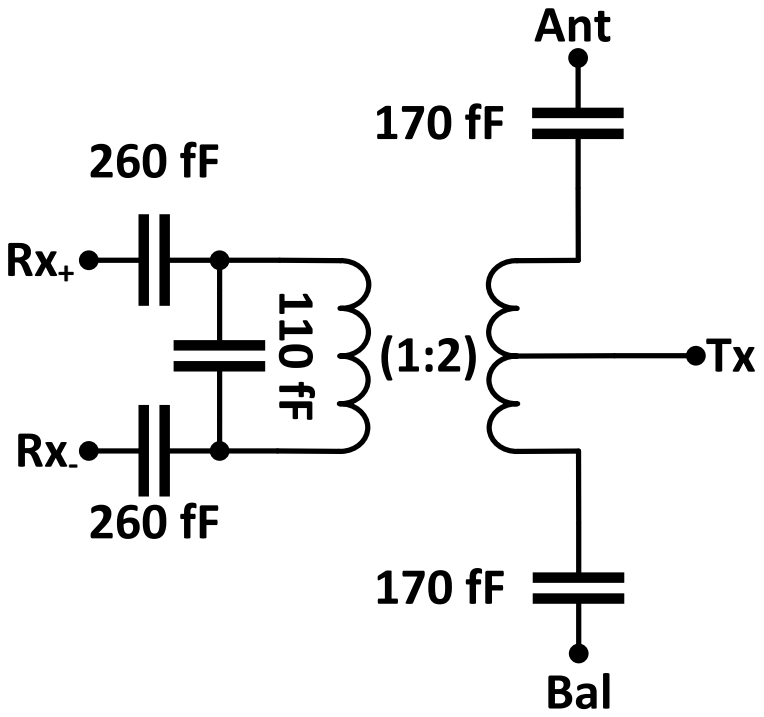


Figure 19: The schematic of the designed hybrid transformer

the system-level consideration as to be 1 and 2, respectively. The isolation depends on the biconjugacy property of the hybrid transformer. The biconjugacy is reached when the port impedances are adjusted to satisfy the impedance conditions in (19).

In the next step of designing the hybrid transformer, the lumped component model is constructed to obtain the inductance values in the primary and secondary coils. as shown in Fig. 19. The value of the coupling coefficient is obtained in the electromagnetic simulations as to be 0.62. The inductance value of the primary coil is found to be 240 pH. Since the transformer consists of inductors, its physical parameters and geometry have a huge impact on the RF performance of the transformer. The octagon shape for the inductors is preferred to obtain higher quality factors which reduce the IL. The thickness and metal resistances of the layers, the dielectric constant, and the distance to the substrate affect the performance dramatically. Selecting a thicker metal layer in technology for an inductor design is a good decision since the thicker metal layer provides better conductivity which results in a lower ohmic loss in the inductor. The thickest metal layer in IHP's SG13S technology is TM2 layer which has a thickness of 3 μm. Moreover, TM2 is the topmost layer in the technology which translates to lower coupling to substrate and loss. If there is an overlap in the winding of the inductor, it will be dealt with changing the metal layer to TM1 or even Met5. The spacing between the windings is 2 μm and

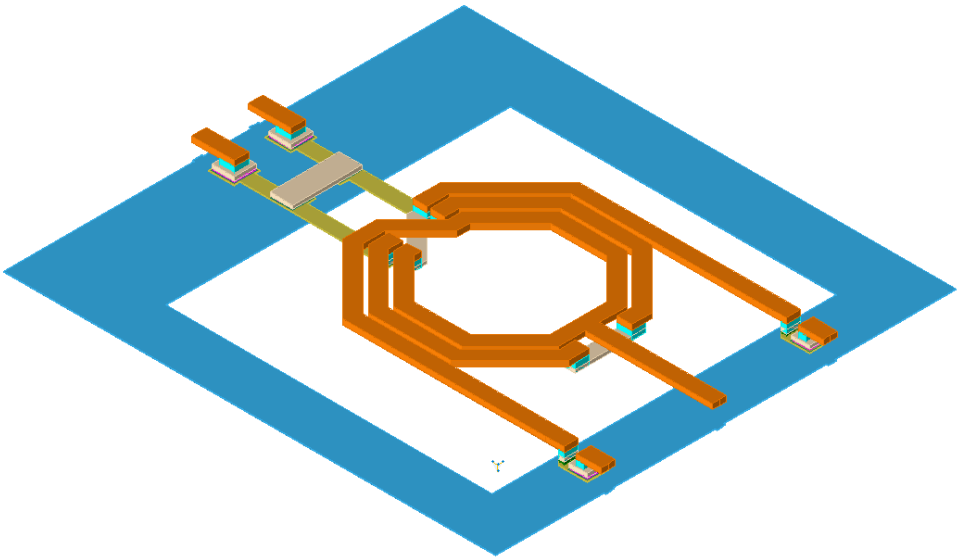


Figure 20: The 3D view of the designed hybrid transformer

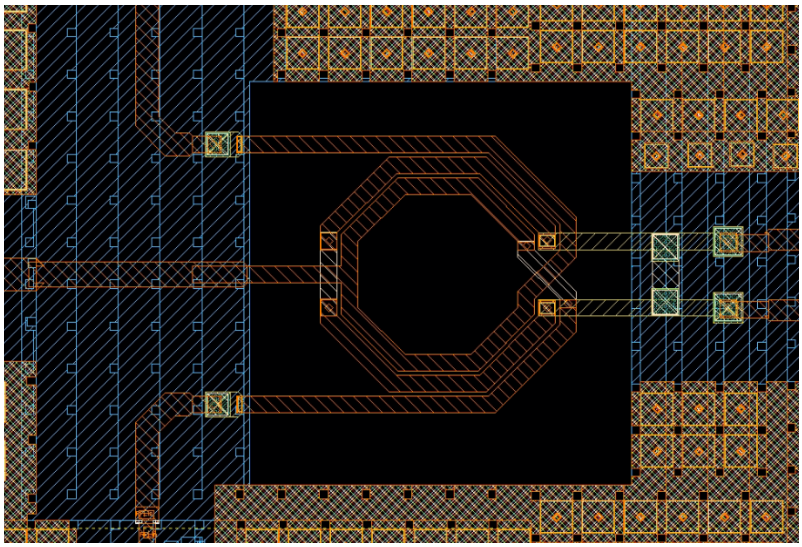


Figure 21: The layout of the designed hybrid transformer

the width of the traces is 8 μm. The radius of the secondary coil is 62 μm whereas the primary coil has a radius of 52 μm.

170 fF series capacitors at ANT and BAl ports enable to match the port impedance to 50 Ω. At the RX port, a 110 fF shunt capacitor and 260 fF series capacitors provide differential 100 Ω matching. The shunt capacitor is realized with two series capacitors placed symmetrically between RX_+ and RX_-. The 3D view and layout of the designed hybrid transformer are shown in Fig. 20 and Fig. 21, respectively.

The effective area of the designed hybrid transformer is 0.274 mm$\times$0.276 mm

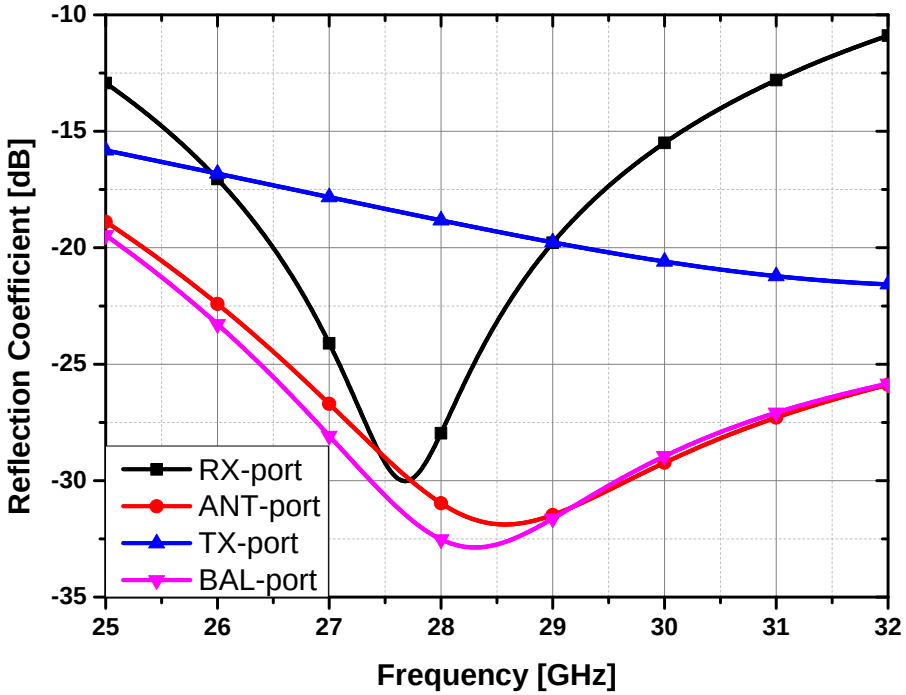


Figure 22: The reflection coefficients at each port of the designed hybrid transformer

(0.07 mm^2). The simulated results of reflection coefficients for each port are presented in Fig. 22 with respect to impedance configuration in (19). The return loss of each port is better than 10 dB between 25 - 32 GHz. Fig. 23 indicates that the IL in TX path is lower than 3.5 dB, and the IL between the antenna and RX is lower than 5 dB between 27 - 29 GHz. For the isolation simulation, ANT and BAL ports are terminated with fixed 50 Ω to obtain the maximum isolation theoretically. The isolation between the TX and RX ports is higher than 50 dB in the target frequency range as shown in Fig. 24. The phase difference between RX_+ and RX_- ports is between +0.5 and -0.5 when the signal is applied from TX port as demonstrated in Fig. 25. Ideally, the leaked signal from TX is divided into two signals which are in-phase so that, the in-phase signals that reach the differential input of the receiver will be canceled out.

3.2.2 Impedance Tuner Design

The isolation is dependent on the impedance mismatch between the ANT-port and BAL-port of the hybrid transformer as (16) implies. In general, the antenna impedance is matched to a fixed impedance. However, the environmental variations result in the deviations in the antenna impedances. The mismatch arises between the antenna and balance port if there is a fixed impedance at the balance port [15].

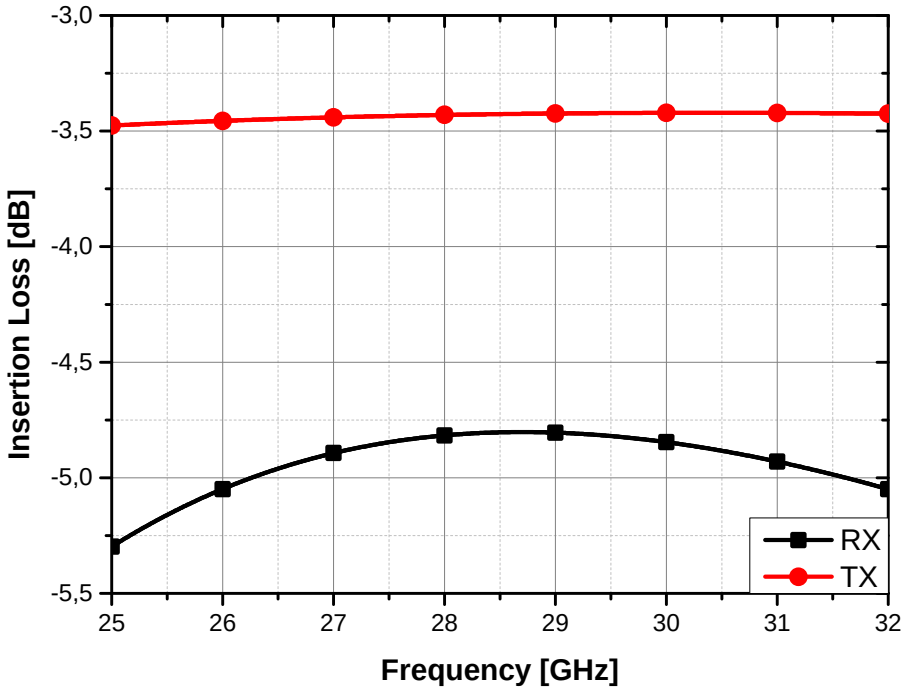


Figure 23: The insertion loss of the designed hybrid transformer in RX and TX paths

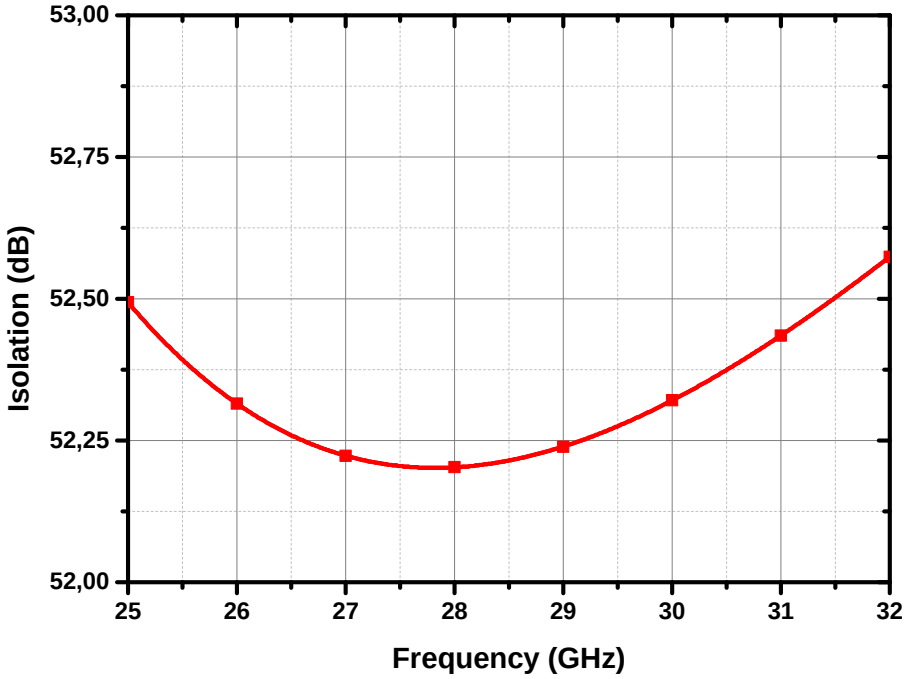


Figure 24: The isolation between of the designed hybrid transformer TX and RX ports

As the impedance mismatch increases, the isolation decreases. As a result, the leakage from the TX chain to the RX chain cannot be suppressed. This strong leakage signal leads to the saturation of the receiver, and the incoming signal may not be differentiated from the leakage. Therefore, the isolation must be satisfied by

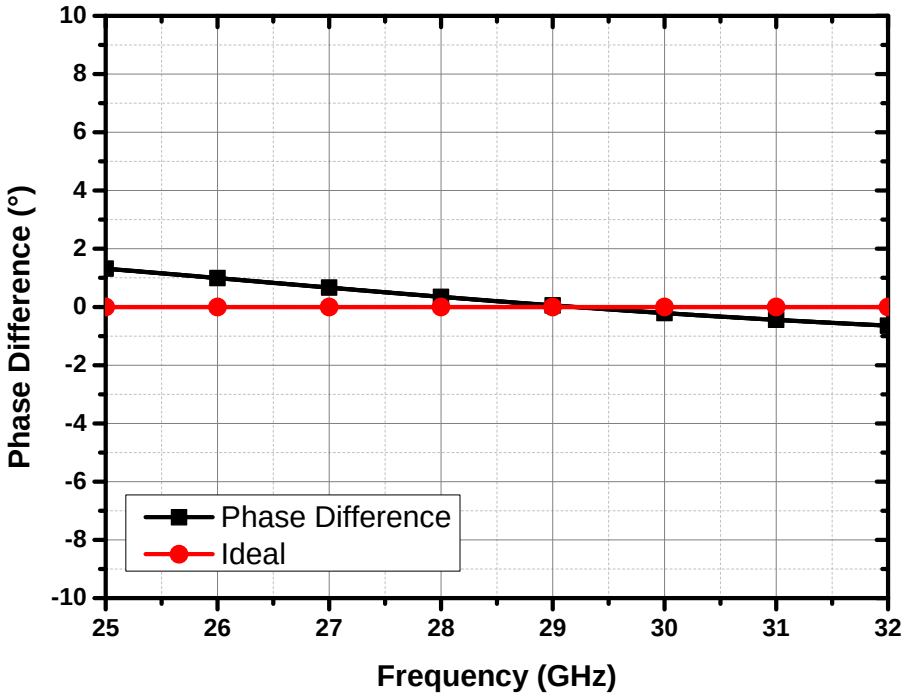


Figure 25: The phase difference between RX ports

the balance network at the BAL-port that must follow the changes in the antenna impedance. The balance network is constructed by an impedance tuner.

The design considerations of the impedance tuner are tuning range and resolution, and the linearity. There is no pre-determined antenna for the system. Therefore, the tuner should cover a set of impedance values to track the antenna impedance. Moreover, the unpredictable variations in the antenna impedance require a wider impedance-range for the impedance network. Missing an impedance value would cause a degradation of the isolation since the isolation depends on the mismatch between the impedances of the ANT-port and BAL-port. Therefore, the tuning resolution is significant as much as the tuning range. Since the transmitted signal is divided into two signals and one of them goes to the BAL-port, a strong signal appears at the input of the impedance tuner. The performance of the tuner should not change with the existence of a strong signal to sustain the isolation level. Therefore, the high-power handling capability is a crucial parameter for the impedance tuner.

The impedance tuners are divided into two in terms of their control method: analog and digital. With the analog control method, variable inductors, capacitors, and resistors can be implemented such as varactors. The impedance of analog-controlled variable components depends on the bias voltage of the component. They can provide finer tune-resolution than the digitally controlled tuners. On the other

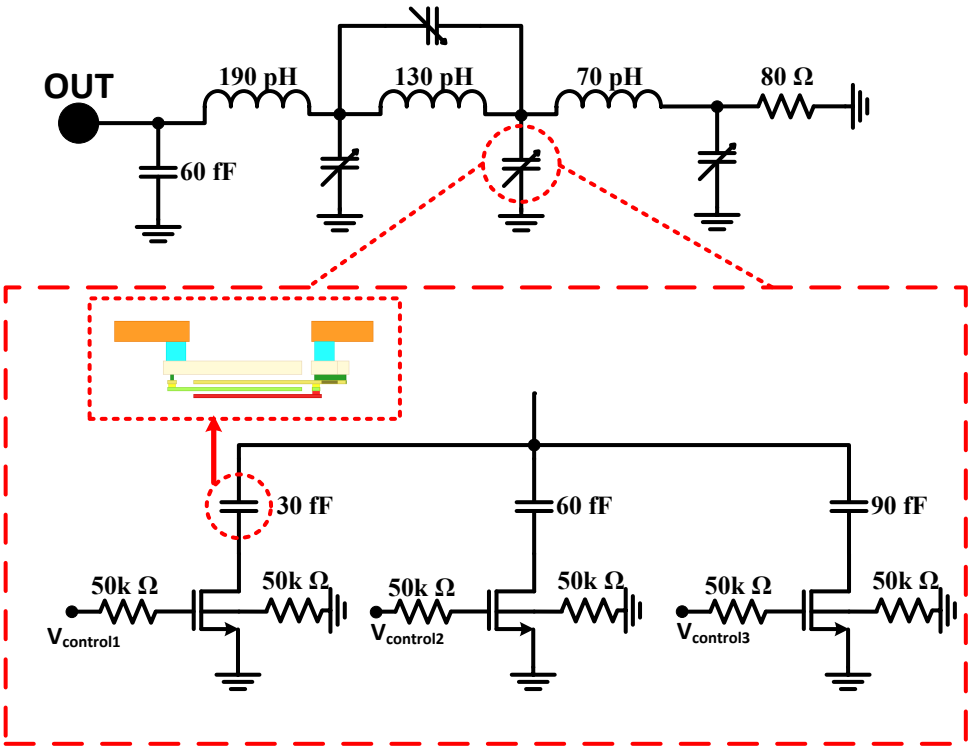


Figure 26: The schematic of the designed impedance tuner

hand, digital control is more preferable in communication systems since analog control is hard to adjust autonomously. Analog variable components can be controlled via digital-to-analog converters. However, this will increase the complexity of the system. The digital control method relies on the switches to change the impedance. The switches ease to control the impedance in a communication system.

The tunable inductors can be used as a variable component in the impedance tuner. However, they are hard to design, and utilizing switched inductors increases the area dramatically. Another option to obtain a variable component is a variable resistor. Variable resistors lead to a decrease in the linearity of the duplexer [15]. Lastly, variable capacitors can be utilized to implement an impedance tuner. Varactors are tunable capacitors controlled by changing the bias voltage. Capacitors can be switch to obtain variable capacitors. Since switched capacitors are easy to integrate with the system due to digital control, they are preferred in this thesis to realize the variable component in the system.

The schematic of the designed impedance tuner is shown in Fig. 26. The design of the impedance tuner started with the switched capacitor elements. The impedance tuner aims to cover the voltage-standing-wave-ratio (VSWR) 2 circle on the Smith Chart. In order to widen the covered impedance area and tuning resolution, the number of capacitors in a bank can be increased. On the other hand,

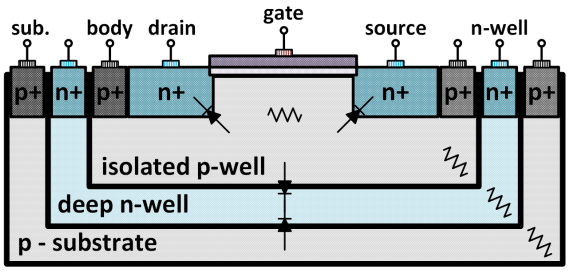


Figure 27: The cross-section view of the isolated NMOS [23]

increasing the number of capacitors leads to the increased chip size and longer measurement time to obtain every state of the impedance tuner. Also, having more capacitors would increase the complexity to follow the variations of the antenna impedance if it is an autonomously controlled balance network. The number of capacitors in a capacitor bank is set to 3. To cover the target area, the step size of the switched capacitors is determined as to be 30 fF. All of the variable capacitor banks are identical as shown in Fig. 26. 60 fF and 90 fF capacitors are implemented by utilizing a metal-insulator-metal (MIM) capacitor included in SG13S technology. Since 30 fF is a small capacitance value, it is prone to the process variations if it is realized with MIM capacitors. Therefore, 30 fF is implemented with a metal-oxide-metal (MOM) capacitor. The size of the MOM capacitor is 12.5×23.5 μm^2. The layers between TM2 and Met4 are utilized to implement MOM capacitor.

As mentioned before, the linearity of the impedance tuner is significant. The switching operation should not be affected by a high-power transmitted signal at the input of the tuner. For example, by assuming that the power of the output signal of the PA is 15 dBm, a 12 dBm signal appears at the input of the tuner after the theoretical loss between the TX and BAL-ports. This signal should not affect the impedance seen from the input of the impedance tuner. In other words, the switches in the capacitor banks must have a high power-handling capability. It is shown that isolated NMOS offers better power-handling capability than NMOS [23]. Therefore, the switches are realized with isolated NMOS which is available in SG13S technology. The cross-section view of isolated NMOS is shown in Fig. 27. In the isolated NMOS, the p-well where the transistor resides is separated from the main p-well by a deep n-well region as illustrated in Fig. 27. This isolation enables to bias isolated p-well region and the main p-well separately. Connecting a high resistance to the body terminal of the isolated p-well region, referred to as the body-floating technique, results in an improvement in the power-handling capability of the switch.

The width of the isolated NMOS plays a key role in the performance of the switch. As the width of the NMOS increases, the resistance of the NMOS in on-mode decreases. However, increasing the width of the NMOS leads to higher parasitic

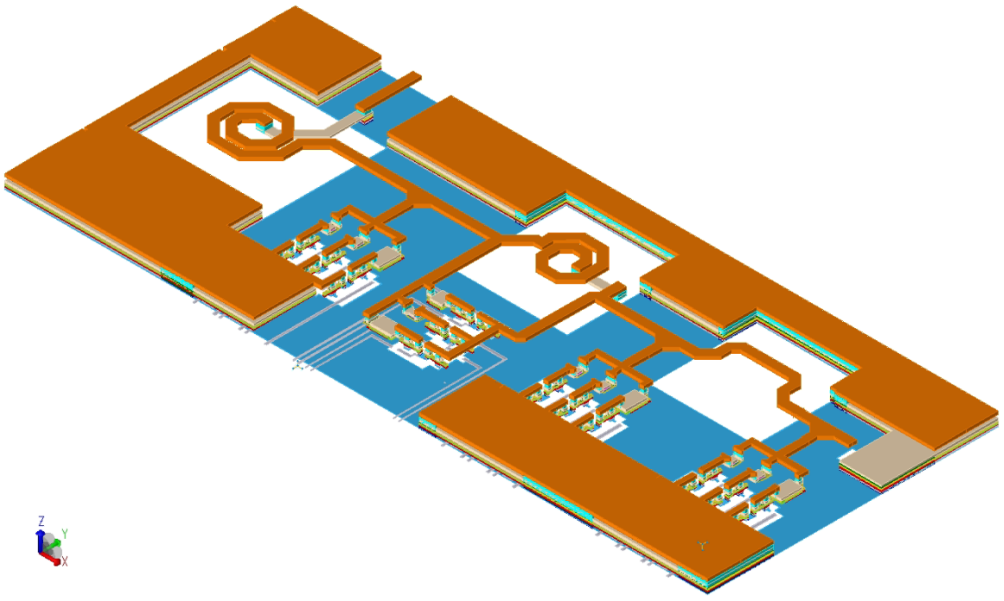


Figure 28: The 3D view of the designed impedance tuner

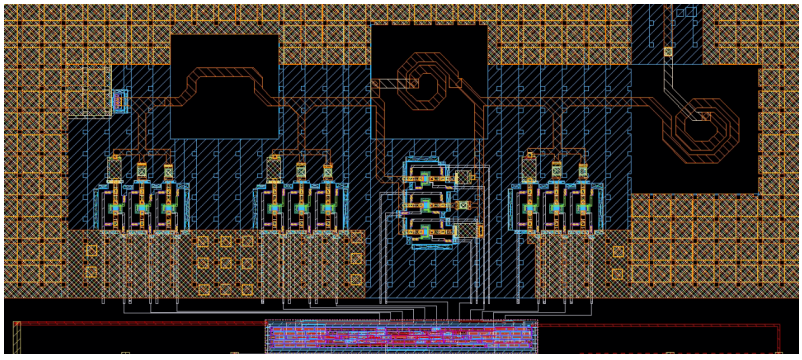


Figure 29: The layout of the designed impedance tuner with digital control circuit

capacitance values. Higher on-resistance or off-capacitance changes the impedance seen from the input of the capacitor bank. Considering the trade-off between the on-resistance and off-capacitance, the width of the isolated NMOS is found to be 30 μm with 8 gates. 50k Ω resistors are used to prevent leakage to bias paths and to employ the body-floating technique.

The fixed resistor at the end of the tuner indicates the starting impedance point of the tuner. It is determined to be 80 Ω realized with four 320 Ω *rppd* components in parallel to reduce the effect of the process variations on the resistance value. The tuner is finalized with the determination of the inductance values as shown in Fig. 26. Electromagnetic simulations were carried out by using ADS Momentum software. The 3D view and layout of the designed impedance tuner are presented in Fig. 28 and Fig. 29, respectively.

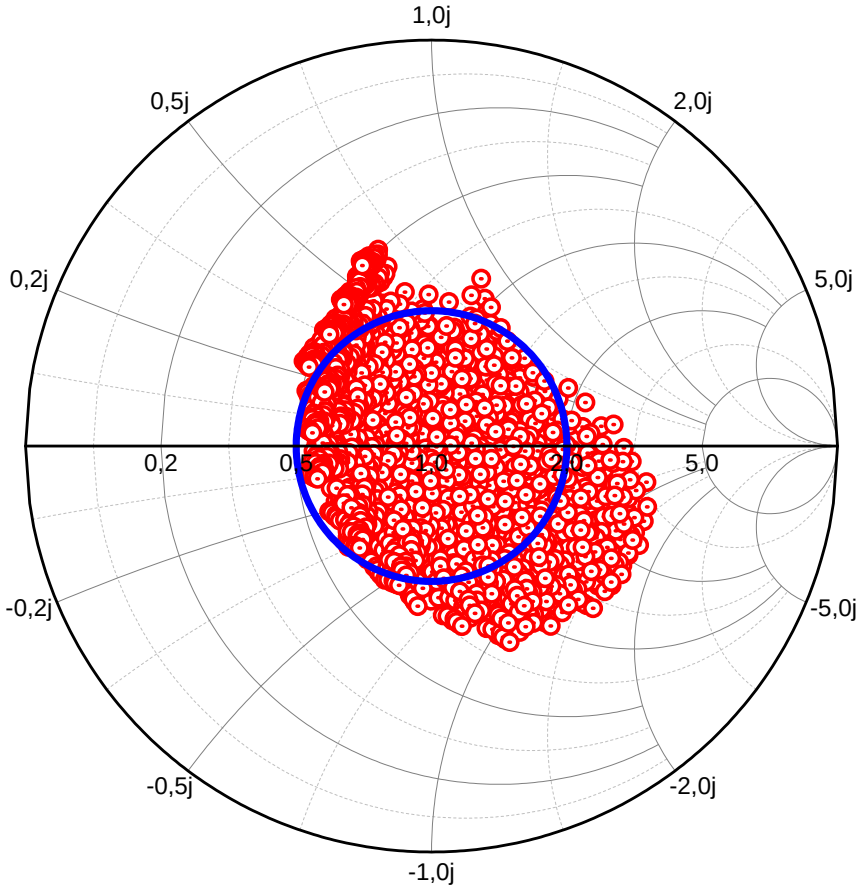


Figure 30: The impedances covered by the impedance tuner at 28 GHz

There are twelve capacitors to be switched in the impedance tuner. Twelve DC pads are required to control these switches. However, this number of DC pads increases the size and cost of the design. It increases the complexity to control each DC pads in an autonomous way. Moreover, routing these DC lines may generate a problem in the system. Thus, a serial-to-parallel interface (SPI) was implemented as a digital control unit to arrange the DC biases of the switches. In each clock cycle, one bit of the input is pushed to the unit. After collecting the pre-determined number of bits, the collected inputs are delivered to the system in parallel. A verilog code, which provides the functionality above, was written, tested, and verified by using Xilinx ISE Design Suite. Synopsis software is used to convert the verilog code to a netlist file. The generated netlist file is used to generate the layout of the SPI concerning the design rules of the technology in Cadence Encounter software. Abdurrahman Burak, who is a member of SUMER Research Group, designed the SPI. The generated SPI is shown in Fig. 29.

The chip area that the designed impedance tuner occupies, including the SPI, is 0.238 mm^2 (0.7 mm$\times$0.34 mm). The simulated impedance values that the impedance tuner covers at 28 GHz are presented in Fig. 30. The blue circle depicts the targeted

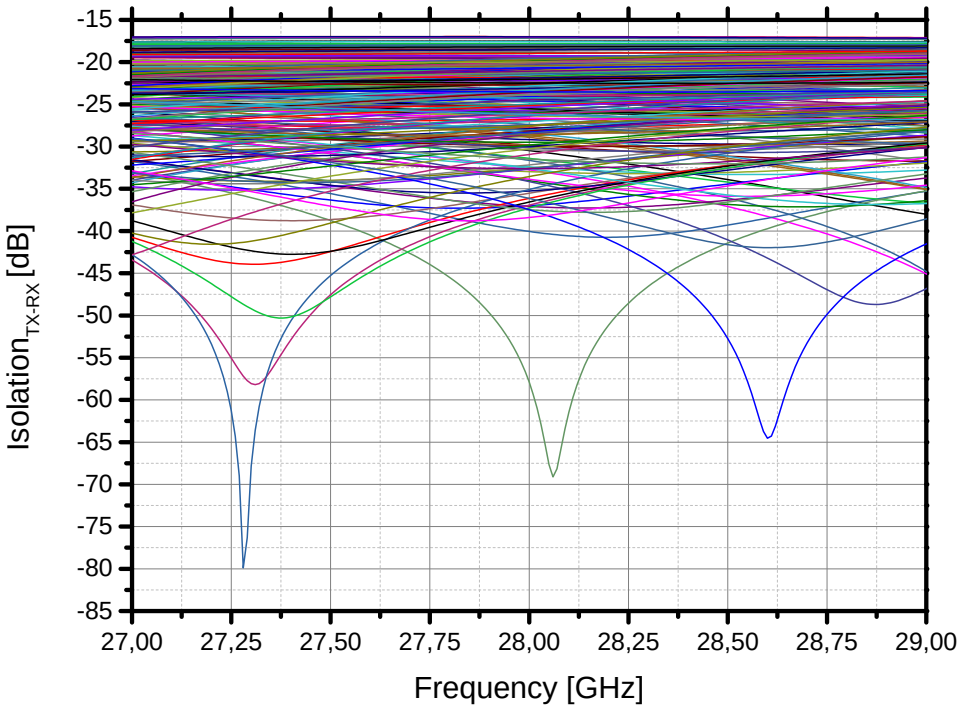


Figure 31: The isolation results for the combination of the hybrid transformer and impedance tuner ($Z_{ANT} = 50\ \Omega$)

VSWR 2 circle and the red circles show all 2^{12} different impedance states. The results indicate that the tuner covers most of the impedances in VSWR 2 circle. Fig. 31 presents the simulated isolation results for the combination of the hybrid transformer and impedance tuner. In this simulation, the antenna impedance is fixed to 50 Ω and the results for half of the different impedance states are presented. From the isolation values in Fig. 31, the duplexer, which consists of the hybrid transformer and impedance tuner, provides isolation better than 40 dB.

3.2.3 Low Noise Amplifier Design

Si-based common emitter (CE) and cascode topologies that aim for high gain and low NF have been presented recently in the literature [24–30]. CE topology has the advantage of lower NF and power consumption. However, it requires multiple stages to satisfy the gain requirements of the LNA. Due to base-collector capacitance that forms a feedback path to the input, it suffers from low reverse isolation which is crucial for stability. On the other hand, cascode topology is favorable over CE topology in terms of reverse isolation and gain [29]. Considering these trade-offs and goals, the selected design is based on a two-stage cascode topology that provides the design flexibility to distribute the performance parameters among stages. Achieving low NF and high gain is the focus of the first stage while the second stage aims to

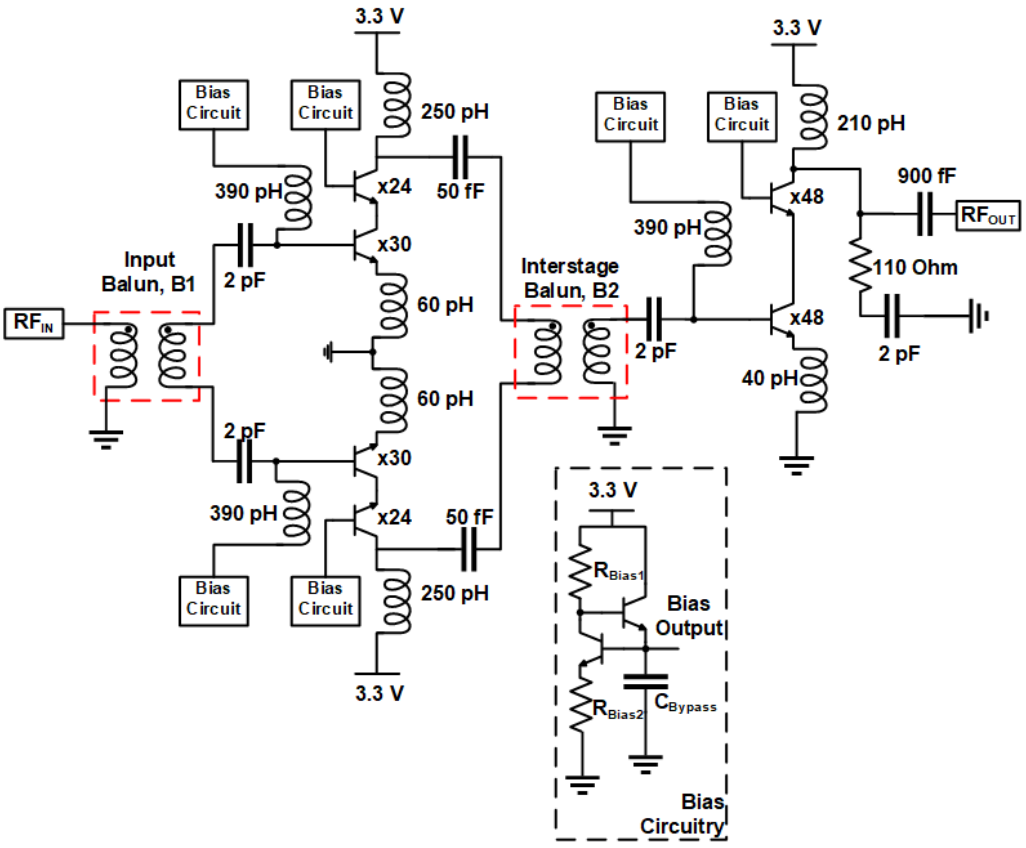


Figure 32: The schematic of LNA

have high gain and linearity. The schematic of the LNA is shown in Fig. 32 where the shunt and series capacitors for balun matchings are not shown for brevity.

To measure LNA with single-ended probes, a balun, which converts a single-ended 50 Ω to a differential 100 Ω, was required at the input. The balun, B1, in [31] was utilized at the input by modifying the capacitance values to improve the matchings. To obtain the impedance transformation, the inductance values of primary and secondary coils are 200 pH and 440 pH, respectively. The primary coil was constructed with a single-turn top-metal 2 trace while the secondary coil was realized with a two-turn top-metal 1 trace to get the inductance values. The width and inner diameter of the primary coil were 12 μm and 80 μm. 10 μm and 43 μm were chosen as the width and inner diameter of the secondary coil. The coupling coefficient, k, was 0.59 [31]. 150 fF shunt metal-insulator-metal (MIM) capacitor was utilized at the single-ended side. Two series 140 fF MIM capacitors formed 70 fF shunt capacitance between the differential output to ensure symmetry.

The EBD has a differential output, where the LNA's output should be single-ended. Therefore, the design should include a balun, B2 which has the opposite functionality of B1. If the differential-to-single ended conversion is favored to be

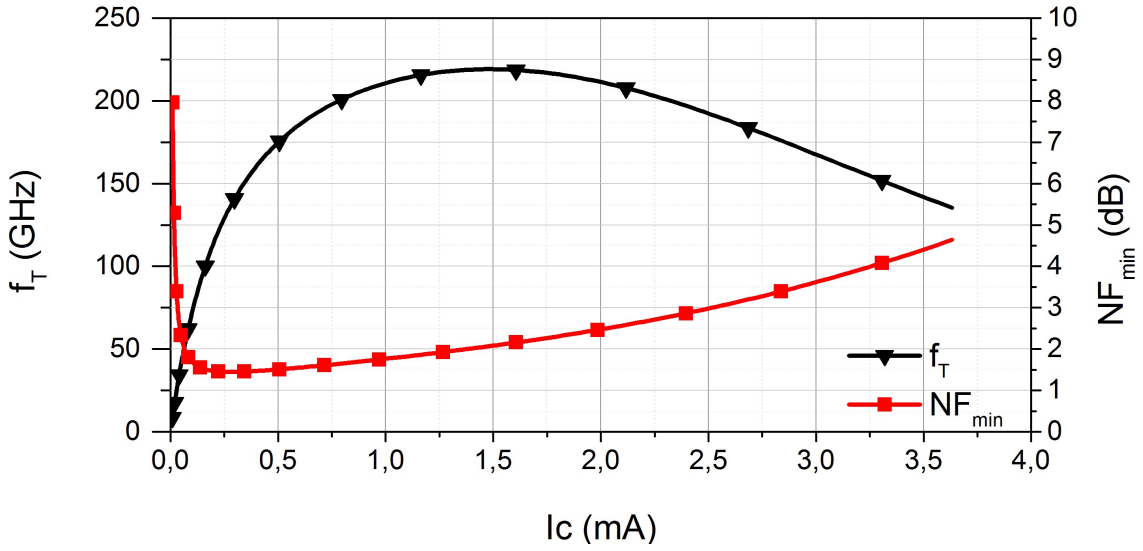


Figure 33: NF_{min} and f_T with respect to the collector current

done at the input, the NF of the LNA will be dominated by the balun. This transition might also be done at the output. However, the power consumption of the LNA would increase due to carrying on as a differential amplifier. As a solution to this problem, B2 was employed between the first and the second stages as shown in Fig. 32; NF of B2 was suppressed by the gain of the first stage. The same primary and secondary coils were utilized in B2. The capacitance values were modified to reduce the loss between stages.

The first stage is designed in a pseudo-differential configuration based on simultaneous noise-and-power matching technique [32]. The design starts with the selection of the collector current for a unit device ($l_e = 0.84$ μm and $w_e = 0.12$ μm) which minimizes NF_{min}. f_T and NF_{min} versus I_C graphs for optimum bias current are shown in Fig. 33. Even though 297 μA collector current provides the lowest NF, 177 μA collector current is chosen to reduce the power consumption with an acceptable sacrifice in NF_{min}. After determining the collector current for unit device size, the number of transistors is chosen as 30 to set the optimal source resistance for noise matching to 50 Ω. Common base transistors are selected as 24 instead of the same size as CEs to increase the gain of the first stage by increasing the output impedance. As reported in [25], the base inductor is removed to decrease the noise and area, without sacrificing from impedance termination. Since inductor guarantees constant V_{BE} when high-power input appears at the input, an inductor is preferred over resistor as a feed component. The shunt bias inductor completes the input matching circuit. The symmetry in both component parameters and layout was paid attention in the design of the first stage not to degrade common-mode rejection ratio (CMRR) of LNA. The simulation results of the common-mode rejec-

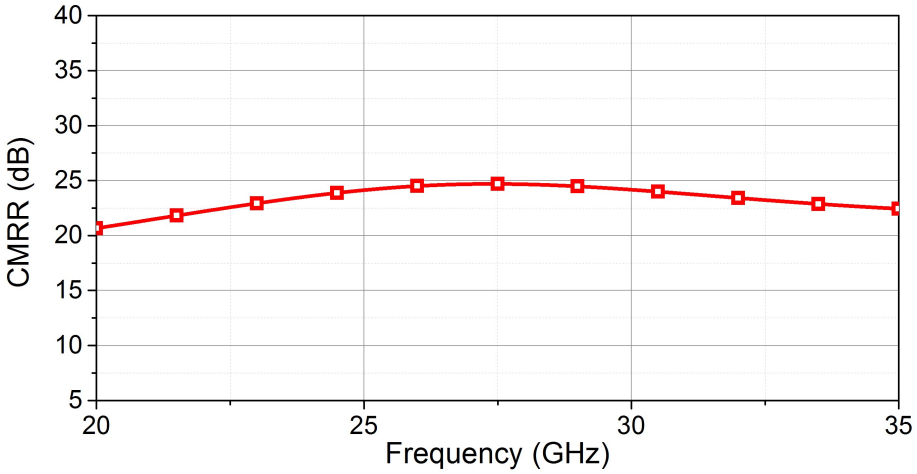


Figure 34: The simulated common-mode rejection ratio of LNA

tion of LNA is presented in Fig. 34. All biases excluding for the collector terminals were supplied through bias circuits as shown in Fig. 32. Bypass capacitors were added to supply lines to eliminate low-frequency stability issues.

The main focus of the second stage is to increase the output power handling capability. The gain from the first stage results in higher input power for the second stage. In the design of the second stage, the power level at the input and desired output power level were considered for the selection of the device sizes. To handle the high input power by increasing the current, the number of transistors in the second stage was chosen as 48. NF was sacrificed to reach high output power in the second stage. The passive components are custom-designed for the desired performance. A shunt resistor is used to reduce the quality factor of the collector inductor in the second stage.

The designed LNA was fabricated in IHP's 0.13 μm SiGe BiCMOS technology which provides HBTs with f_t/f_{max} of 250/300 GHz and BV_{CEO} of 1.6 V. Fig. 35 shows the chip photo of the measured LNA which occupies 1.35 mm^2 including the pads. The LNA draws a total of 20 mA current from a 3.3 V supply. The total power consumption is 66 mW.

The S-Parameters of the LNA was measured from 10 GHz to 40 GHz with Cascade Microtech 40-GHz GSG probes by using Keysight N5224A PNA with -20 dBm input power to obtain results in the linear region of LNA. NF was measured between 20-35 GHz by using a Keysight E4448A PSA and a 346CK01 noise source. The output power measurements of the LNA were done between 20-33 GHz by using the Keysight E4448A PSA. The noise and linearity measurement setups are demonstrated in Fig. 36 and Fig. 37, respectively. In the figures, some of the DC connections are shown as an example.

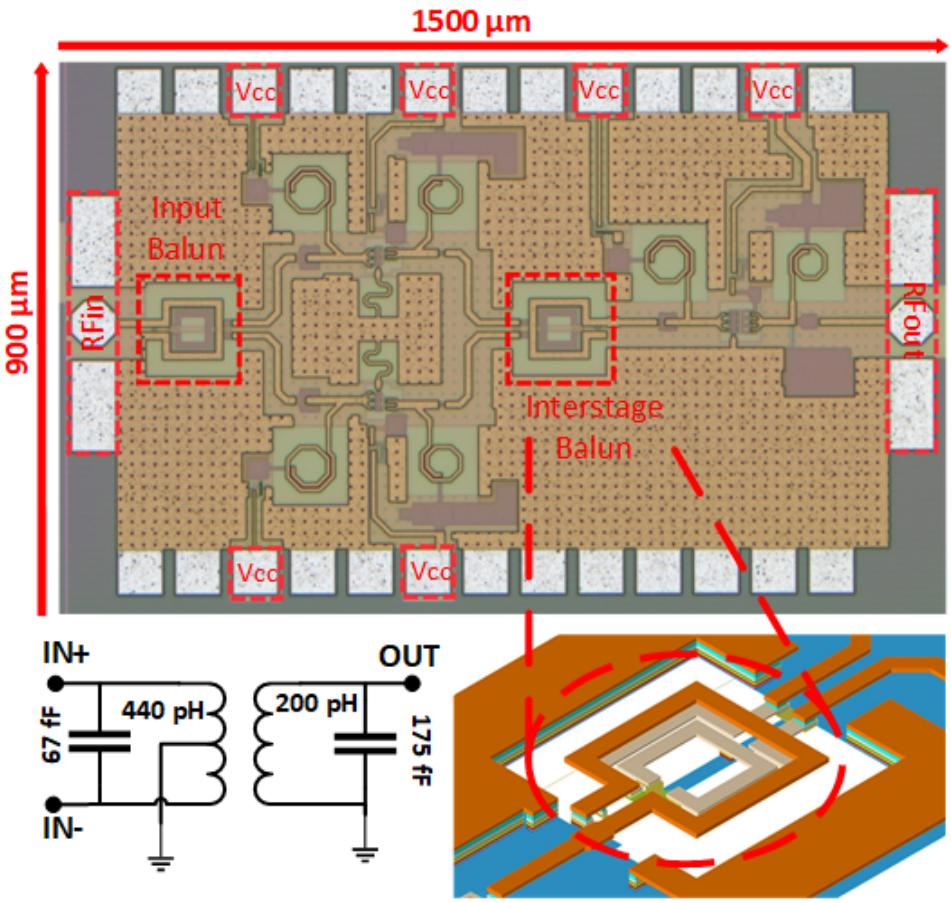


Figure 35: Chip photo of the measured LNA and schematic and 3D view of the interstage balun

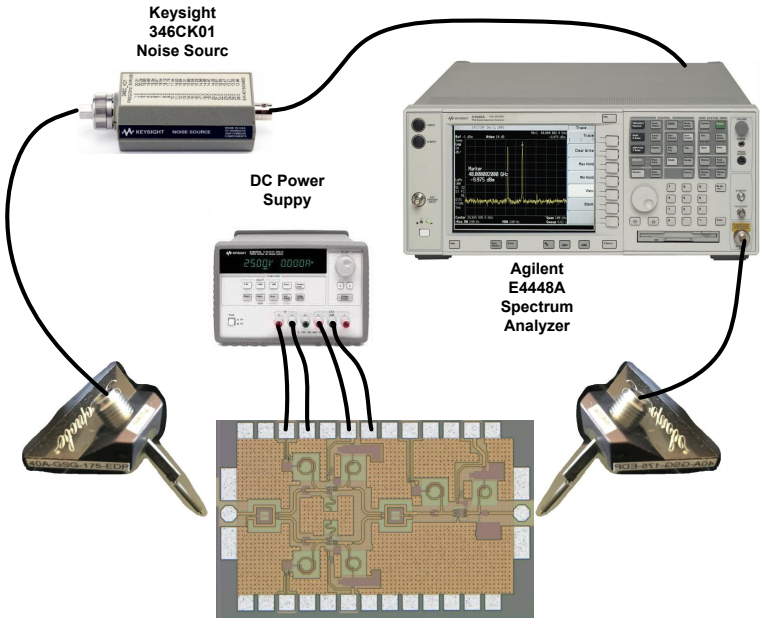


Figure 36: Noise measurement setup

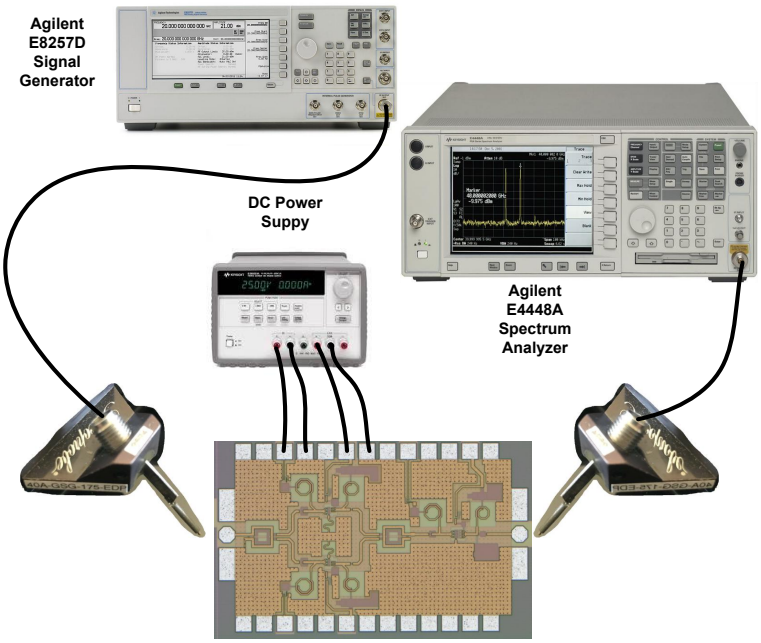


Figure 37: Linearity measurement setup

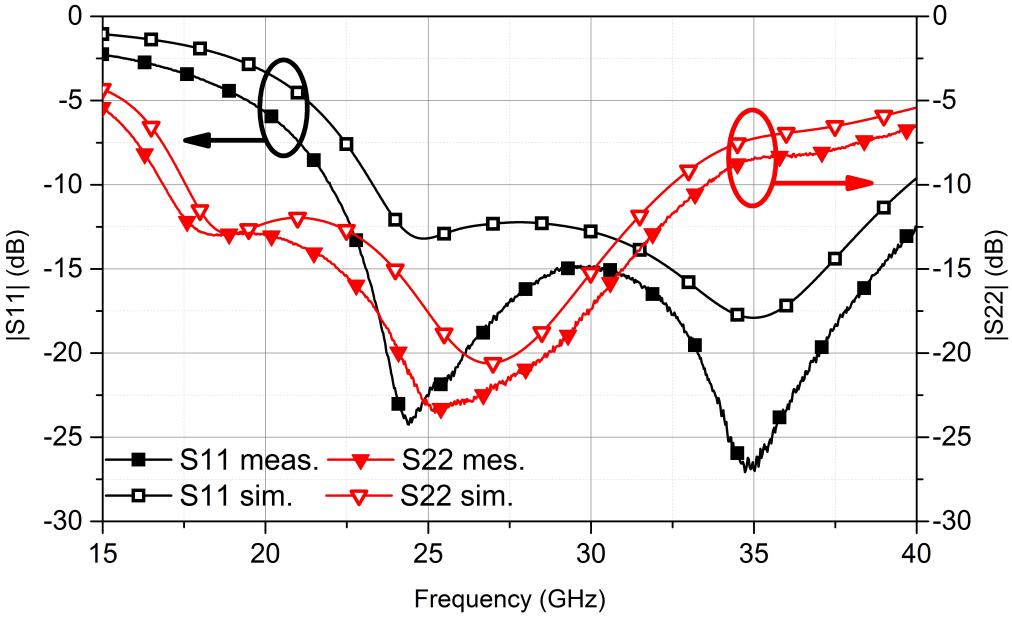


Figure 38: Input and output matchings of the designed LNA

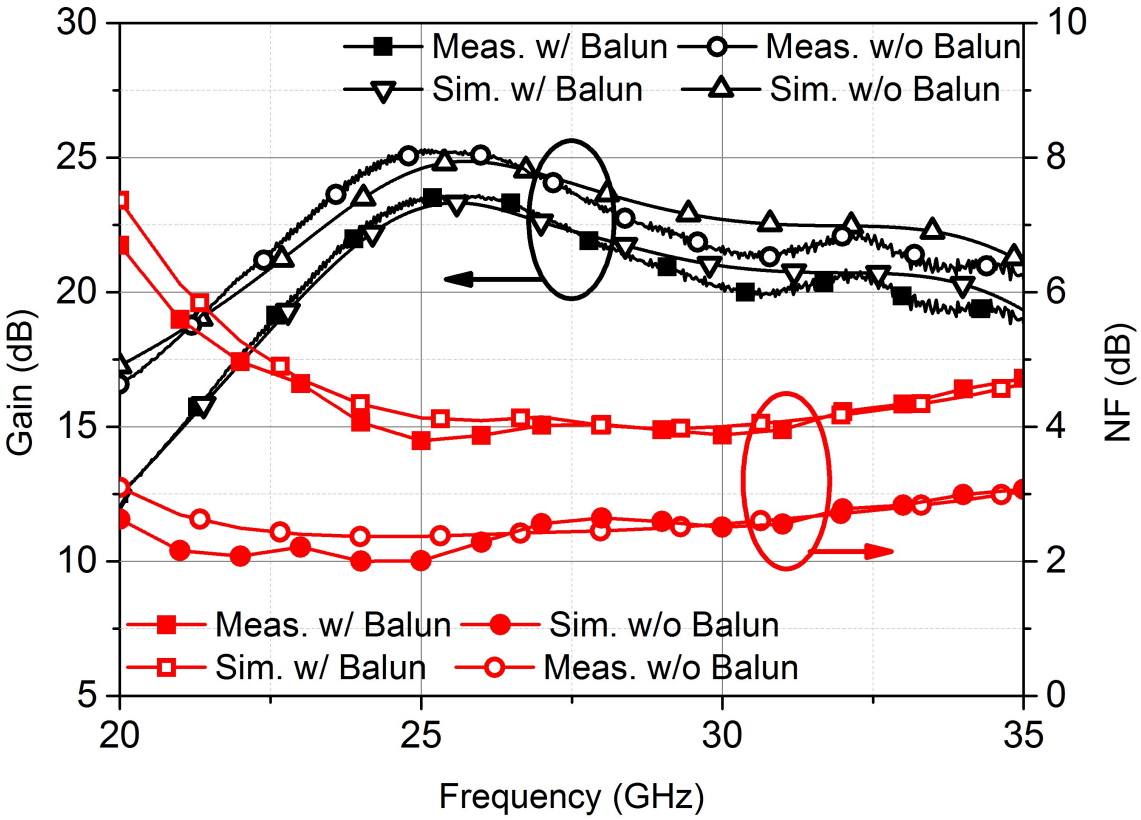


Figure 39: Measured and simulated gain and NF of the designed LNA

As shown in Fig. 38, the measured input, and output matchings are lower than -10 dB between 22-33.5 GHz. The reverse isolation was measured higher than 55 dB. The measurements are in line with the simulations. Since the input balun was placed before the amplification as mentioned in the previous section, the input balun deteriorates the NF and gain of the LNA by a minimum of 1.3 dB. Considering the coherency between the measurements and simulations, the effects of B1 were excluded from the LNA measurements by subtracting the loss of B1 to present the design capabilities more clearly. The gain measurements, shown in Fig. 39, show that the 3-dB bandwidth of the LNA is 23-30 GHz. The peak gain was found to be 25.3 dB at 25 GHz. The NF performance of the LNA is demonstrated in Fig. 39 which indicates 2 dB NF at 25 GHz. The effect of B1 was also excluded from P1dB results. The IP_{1dB} and OP_{1dB} of LNA was measured as -10 dBm and 14.1 dBm, respectively at 25 GHz as shown in Fig. 40 which presents them with respect to frequency. The performance comparison of the designed LNA with the previous works in the literature is provided in Table 2. The expression for the figure of merit (FoM) is given in (20).

$$FoM = \frac{Gain}{F-1} \cdot \frac{IP_{1dB}(mW)}{P_{dc}(mW)} \cdot 10 \tag{20}$$

Table 2: Comparison of the presented LNA with similar works in the literature

Ref.	Tech.	Freq. (GHz)	NF. (dB)	Gain. (dB)	IP_{1dB} (dBm)	P_{DC} (mW)	Area (mm^2)	FoM
[26]	0.13 μm SiGe BiCMOS	28-60	2.36 @ 28 GHz	19.25	-27.3 @ 28 GHz	26.8	0.148*	0.08
[24]	0.25 μm SiGe BiCMOS	24-34	2.1 @ 30 GHz	26.4	-14.9 @ 30 GHz	134	0.165*	1.69
[27]	65 nm CMOS	25-30	3.7 @ 26 GHz	18	-12.6 @ 28 GHz	10	0.17*	2.76
[28]	0.13 μm SiGe BiCMOS	28-35	4.2 @ 28 GHz	10	-5 @ 30 GHz	43	0.12*	0.42
[30]	45 nm CMOS SOI	25-31	2.7 @ 28 GHz	8.5	-3 @ 28 GHz	12	0.4	3.43
This Work**	**0.13 μm SiGe BiCMOS**	**23-30**	**2 @ 25 GHz**	**25.3**	**-10 @ 25 GHz**	**66**	**1.35**	**8.77**

*: Excluding Pads **: Input Balun excluded results

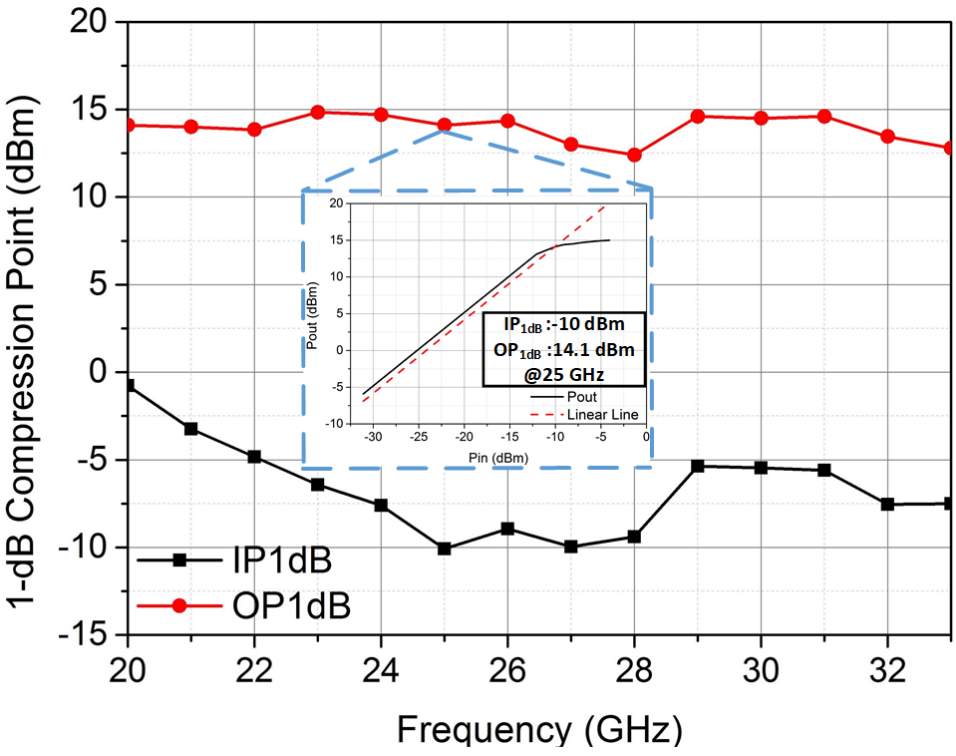


Figure 40: The measured IP_{1dB} and OP_{1dB} of the LNA

3.2.4 Power Amplifier Design

PA is the last block in the transmitter chain. In other words, the last amplification block for the transmitted signal is PA. Therefore, the output power that PA can provide is the most crucial performance parameter for a PA. Since the main objective is to obtain high output power, the reverse gain of the amplifier becomes more significant in order to prevent stability problems. In the scope of this thesis, the PA is expected to provide 15 dBm of output 1-dB compression point (OP_{1dB}) with moderate gain with Class-A operation. In order to obtain a moderate gain of approximately 15 dB, a two-stage structure is determined. The first stage is a driver amplifier, whereas the second stage aims to reach high output power levels. CE and cascode topologies are widely used topologies in the literature. The comparison between CE and cascode topologies is provided in the design of the LNA. Since cascode topology offers higher output power, the second stage is chosen to be cascode topology. Also, the cascode topology provides lower reverse-gain. As a result, a more robust design against stability problems can be achieved. The CE topology is selected for the driver stage. With the selection of CE topology for the first stage, the power consumption is reduced. The design and measurements of the PA were carried out by Alper Güner, who was a member of the SUMER Research Group. The collector voltage is set to 1.6 V due to the collector-emitter breakdown voltage (BV_{CEO}). The base bias is 900 mV, and the number of the unit device is 24. The collector current is 18 mA. The schematic of the designed PA is shown in Fig. 41.

The main objective of the second stage is to obtain high output power. Therefore, there must be a high current that flows through the second stage. In order to maintain the high current, the number of transistors is selected to be 48, and the base bias of the bottom transistors is 920 mV that results in the collector current of 59 mA. With this current flow, the base bias of the upper transistors is set to 2.2 V to widen the swing range at the output node by reducing the collector voltage of the CE part. The output of the PA is mathced to 25 Ω since Z_{TX} of the hybrid transformer is 25 Ω as mentioned before. The topology of the bias circuits in the designed PA is the same as in the designed LNA. Theoretically, the base of the common base part in the cascode topology must see RF-short for the desired frequency range. However, the base node might not be RF-shorted due to the parasitic of the utilized layers. Therefore, a by-pass capacitor resides at the base node. The value of this component is crucial for high power applications because it may lead to a strong oscillation. Therefore, the value of the by-pass capacitor is determined to be 350 fF to tune out the parasitic inductance at the base of the common base transistor.

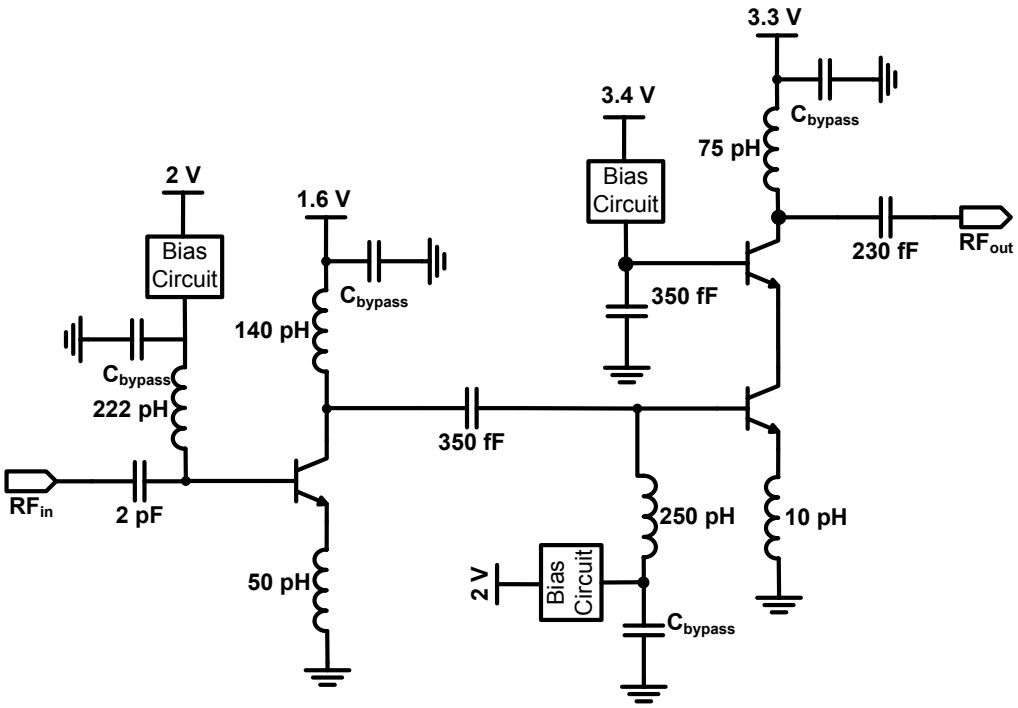


Figure 41: The schematic of the designed PA

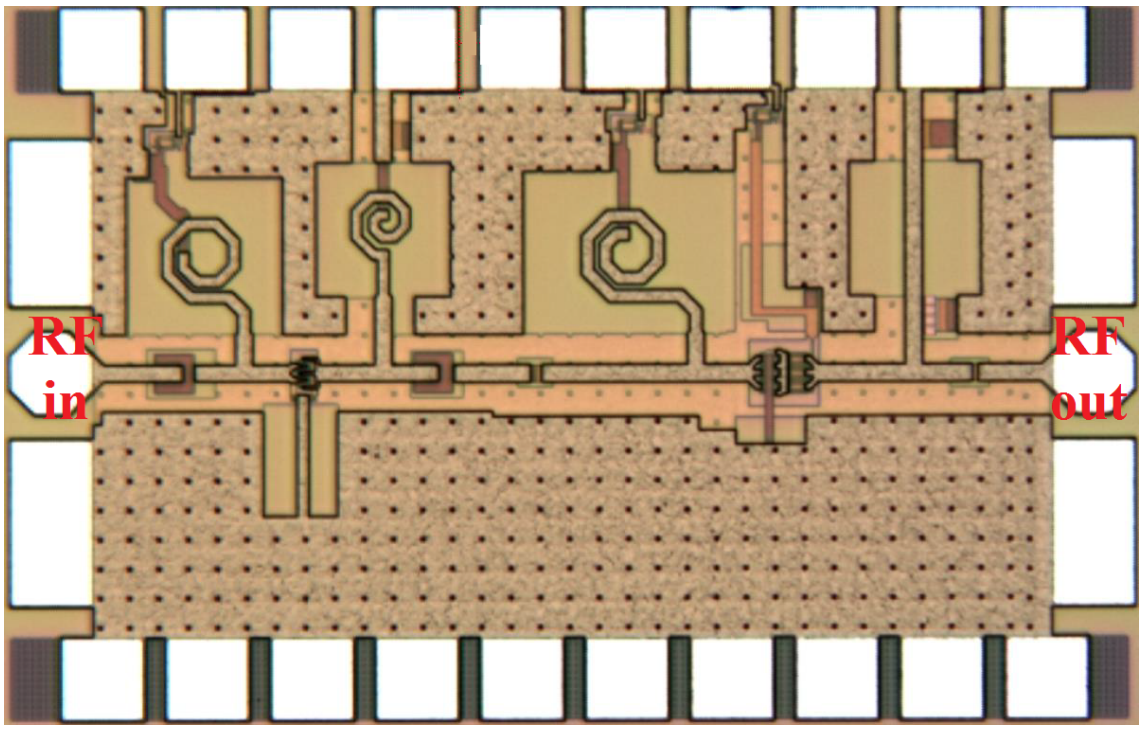


Figure 42: The chip photo of the designed PA

Electromagnetic simulations for passive characterizations were done with the help of ADS Momentum and Sonnet software. Cadence virtuoso is utilized to obtain the layout.

The chip photo of the designed PA is shown in Fig.42. The area of the de-

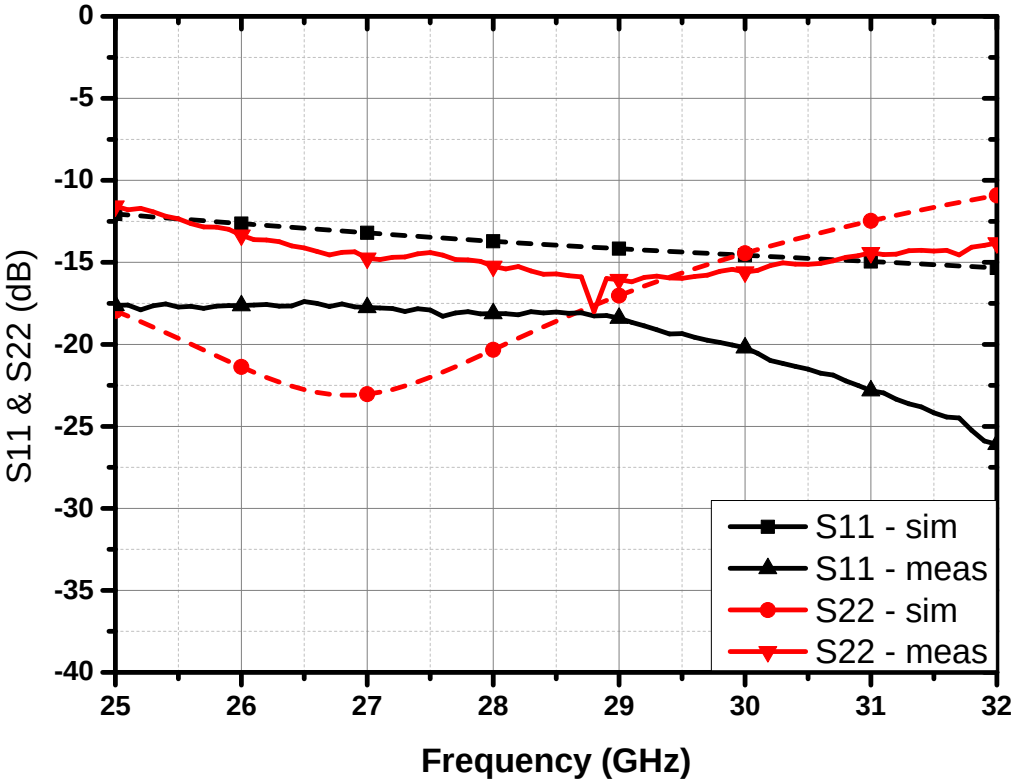


Figure 43: The return losses of the designed PA

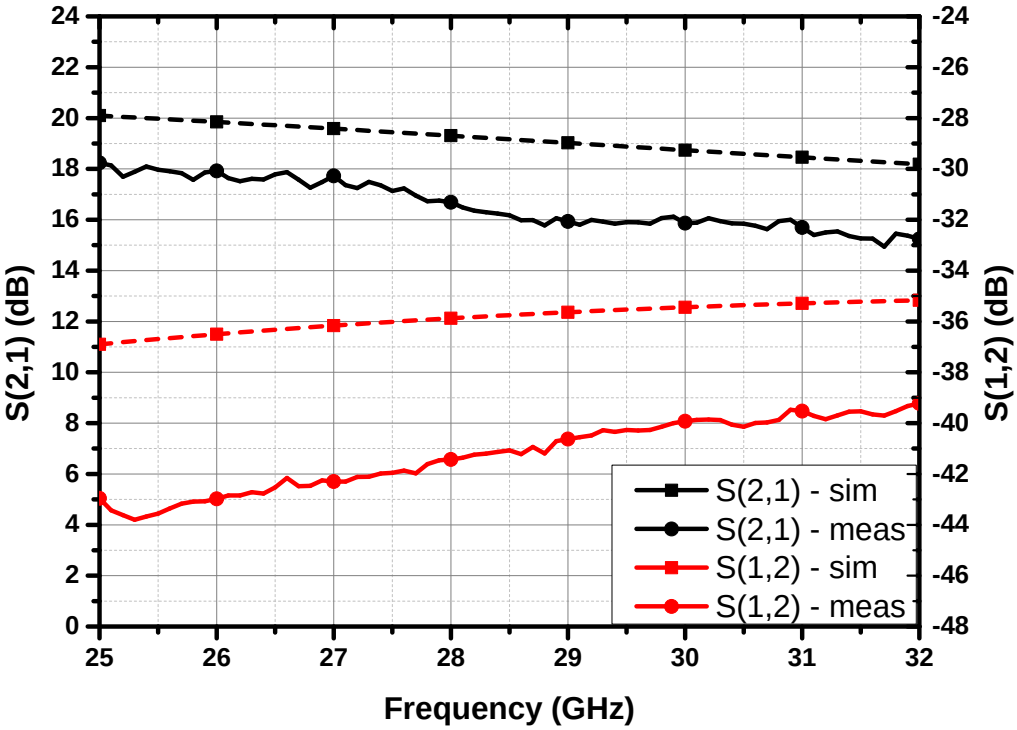


Figure 44: The forward and reverse gain of the designed PA

signed PA is 0.45 mm$\hat{2}$ (0.9mm×0.5 mm). The measurements were done by Alper Güner. The S-parameter and linearity measurement methods are the same as in the measurements of the LNA. Fig. 43 presents the measured return losses of the

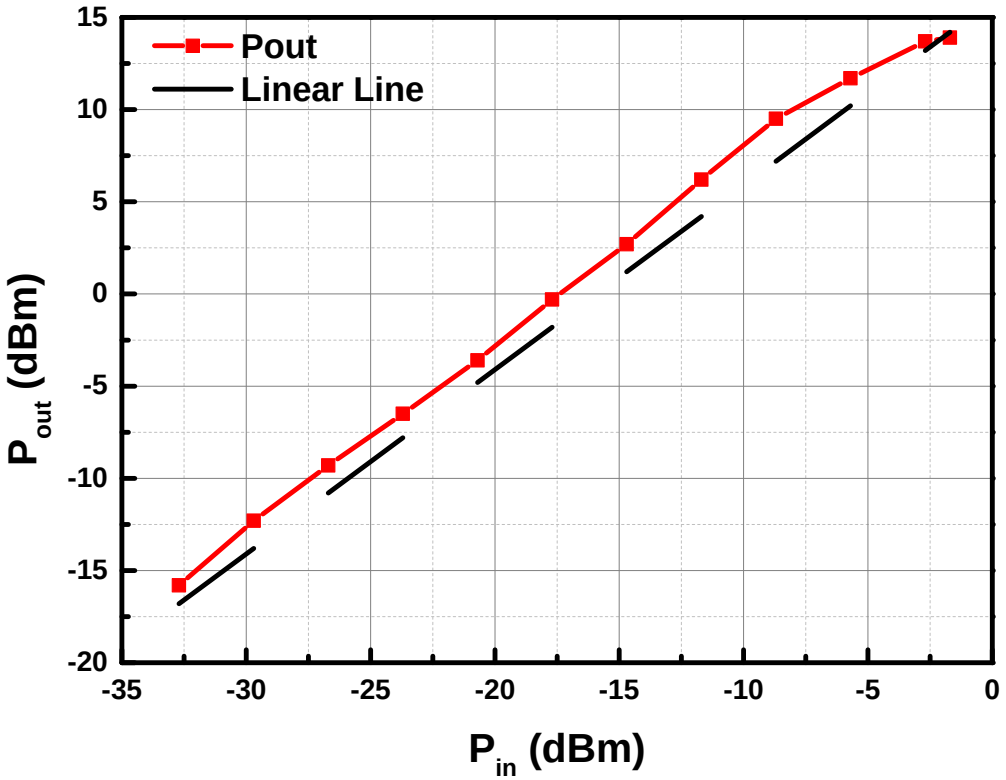


Figure 45: P_{out} vs P_{in} of the designed PA

fabricated PA. The input and output return losses are higher than 10 dB between 28 - 32 GHz. The measured gain at 28 GHz is 17 dB as shown in Fig. 44. As Fig. 45 indicates, the output of the PA compresses when -2.5 dBm input signal appears at the input of the PA. The OP_{1dB} of the PA is 14 dBm.

3.2.5 Measurements of the System

As Fig. 17 shows, the prototype consists of PA, LNA, hybrid transformer, and impedance tuner among the designed blocks. The PA is connected to TX-port, and the LNA is connected to the RX-port of the hybrid transformer. The B1, mentioned in the LNA part, is removed since the reason why it exists is to measure the designed LNA with single-ended probes. The impedance tuner is placed at the BAL-port of the hybrid transformer. The antenna port is terminated with pads to be connected to a network analyzer as the input of the PA and the output of the LNA. In this way, the collected data can be used to sweep the antenna impedance by utilizing software such as ADS or MATLAB. The chip photo of the fabricated prototype is presented in Fig. 46.

In the preparation of the measurements, the chip was bonded to a QFN package with in-house facilities by Abdurrahman Burak. After bonding, the package was

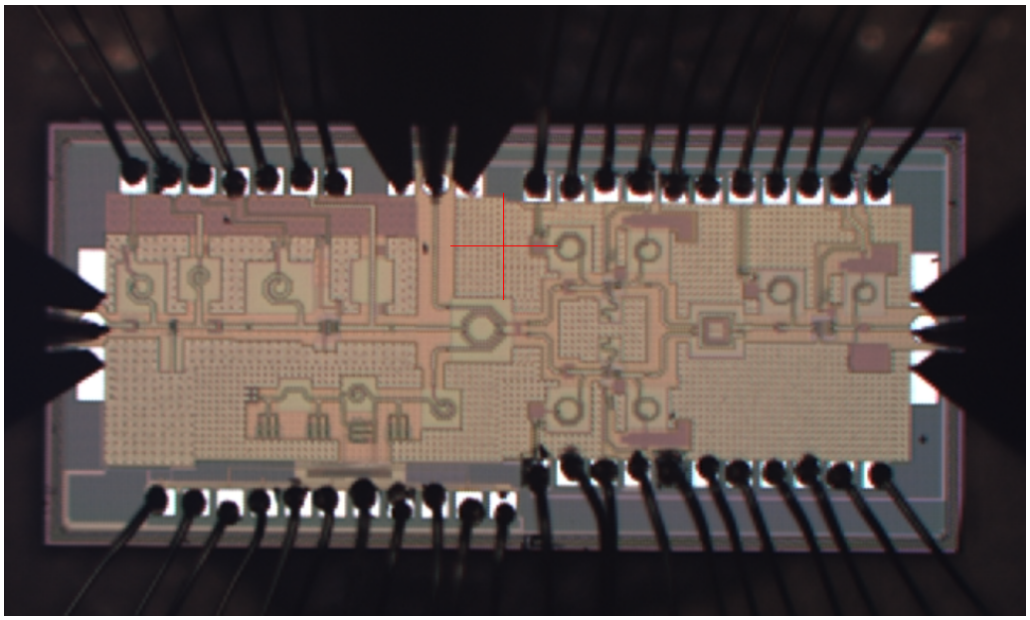


Figure 46: The chip photo of the fabricated prototype

soldered to the PCB designed with the DC routing for this package. Unlike the S-parameter measurements of the LNA and PA, the system measurements were carried out with three-port measurements. The measurements were done with Cascade Microtech 40-GHz GSG probes by using Keysight N5224A PNA. Short-open-load-thru (SOLT) calibration was applied to all three ports according to the guidance. Also, to test and verify the functionality of the impedance tuner, 4096 (2^{12}) different states must be observed by changing the digital input of the tuner. The digital input was provided by Field-Programmable-Gate-Array (FPGA). A verilog code is written to obtain appropriate outputs from FPGA. Moreover, the period of a clock-cycle in the FPGA is adjusted to the operating time of LabView software, which collects the data from the network analyzed in the s3p format. Without this period adjustment, some states might be missed or the state might change during the collection of the data so, the collected date would have been wrong. The Verilog code is given in APPENDIX A. The linearity measurements were conducted with the same methods in the measurements of the PA and LNA.

The collected S-parameter measurements were imported into the data item in the ADS software environment. The port which corresponds to the ANT-port was terminated with 50 Ω. The TX input and RX output matchings for ten of the swept states are demonstrated in Fig. 47. TX input and RX output return loss are better than 10 dB in the measured frequency band. Also, another statement can be deducted that TX input and RX output matchings are not related to the impedance at the BAL-port due to the cascode topologies in the PA and LNA which have low reverse gain. Fig. 48 shows the sampled ten TX-gains of the prototype. It is hard

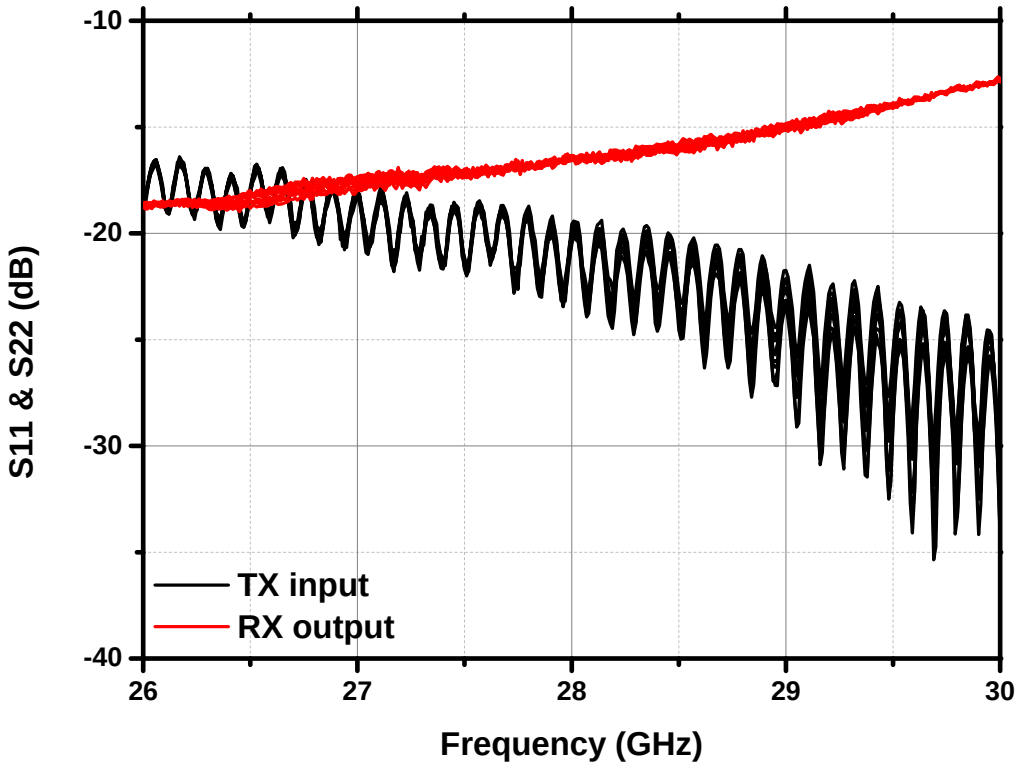


Figure 47: The return losses of TX-input and RX-output of the prototype

to put all states into one graph. To give insight into measurement results, ten of the states were selected randomly. The average TX-gain is also presented in Fig. 48. The TX-gains vary between 14 and 16 dB at 28 GHz where the average is 14.5 dB at the same frequency. Similar to TX-gains, ten samples are shown in Fig. 49 because of the same reason. The RX-gains vary between 17.5 and 18.5 dB at 28 GHz as the state of the impedance tuner changes. The average RX-gain is 18 dB at 28 GHz. The isolation cannot be reached directly. The value of the isolation can be estimated very closely by utilizing the formula in (21):

$$Isolation_{TX-RX} = S21(dB) - S31(dB) - S23(dB) \tag{21}$$

where S31 and S23 refer to the TX-gain and RX-gain and S21 is the difference in the power of the leakage signal from the TX-output to RX-input. The calculated isolation values are presented in Fig. 50. The results indicate that 40 dB isolation between the TX-port and RX-port of the hybrid transformer is achieved between 26 and 30 GHz with small missing frequency ranges.

After gathering S-parameters for all impedance tuner stats and observing the results in ADS, NF and linearity measurements were conducted by setting the impedance tuner to one of the states that provide isolation more than 35 dB. The measurement setups for noise and linearity were similar to the measurements in the

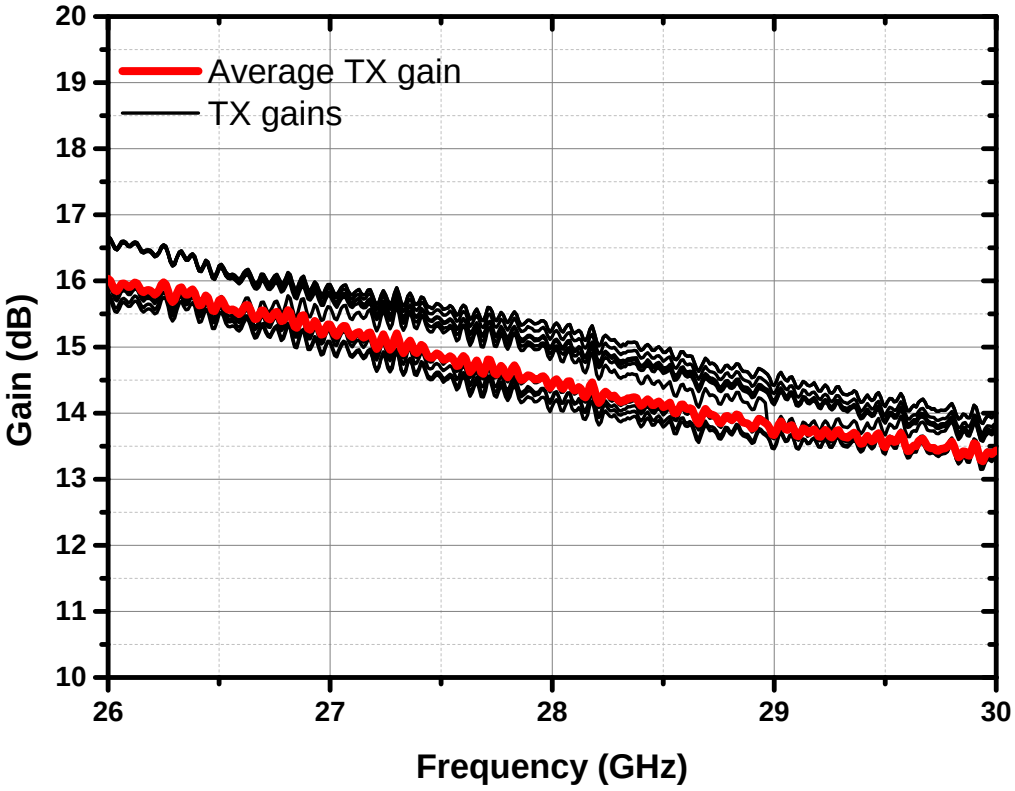


Figure 48: Sampled ten TX-gains with the average of all the TX gains of the prototype

LNA. The NF of the receiver part is shown in Fig. 51. With the combination of the loss in the RX path of the hybrid transformer and the NF of the LNA, the minimum NF of the receiver was measured as approximately 7.5 dB. The NF of the receiver is lower than 8.2 dB in the frequency range of 27 - 29 GHz. Fig. 52 shows the 1-dB compression point of the receiver side. The IP_{1dB} and OP_{1dB} were measured as -3 dBm and 13 dBm, respectively. The linearity performance of the transmitter is presented in Fig. 53. The IP_{1dB} and OP_{1dB} were measured as -6 dBm and 9.75 dBm, respectively. The difference between the OP_{1dB} of the PA and transmitter stems from the loss from the TX-port to the ANT-port of the hybrid transformer.

In ADS, the measurement results are visualized for a fixed antenna impedance. Sweeping both antenna impedance and the measurement state in ADS is not feasible to interpret the results. Therefore, the software is switched from ADS to MATLAB. The collected s3ps are imported to MATLAB. However, MATLAB has the capability of making calculations with two-port networks. In order to overcome this problem, the three-port network is reduced to a two-port network by defining an impedance to the excluded port. For example, to obtain TX gain, the output of the LNA is terminated 50 Ω. Since that port is terminated, a two-port network can be generated. This method is applied all three-ports to calculate the isolation according

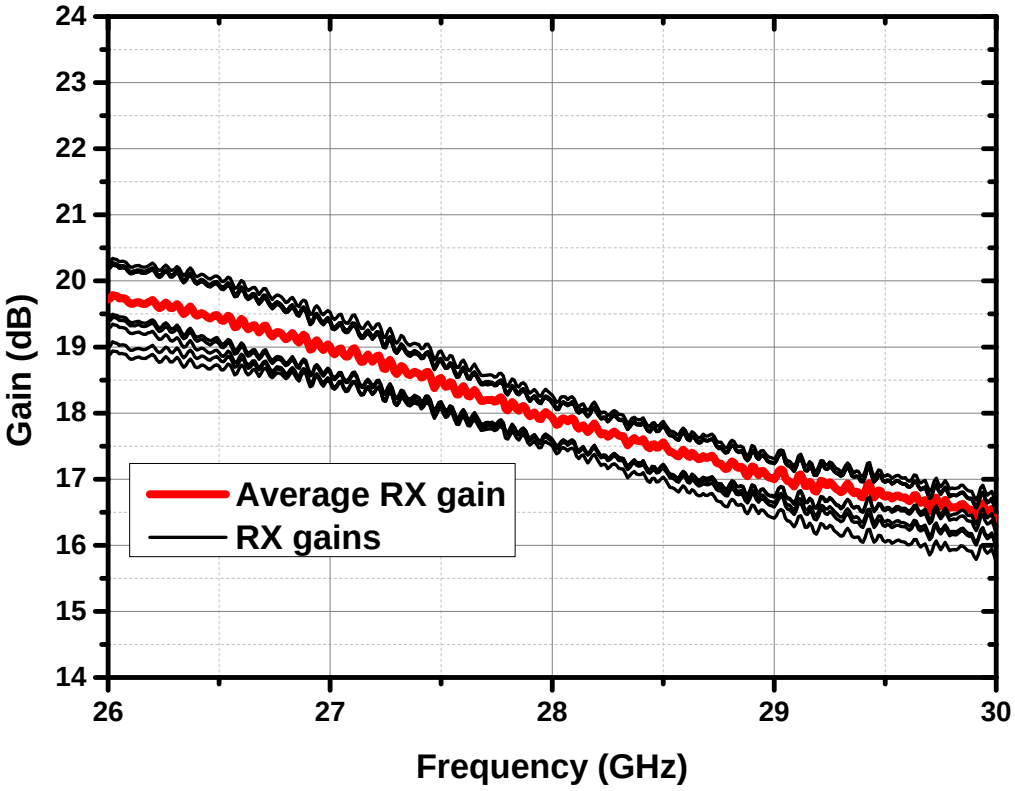


Figure 49: Sampled ten RX-gains with the average of all the RX gains of the prototype

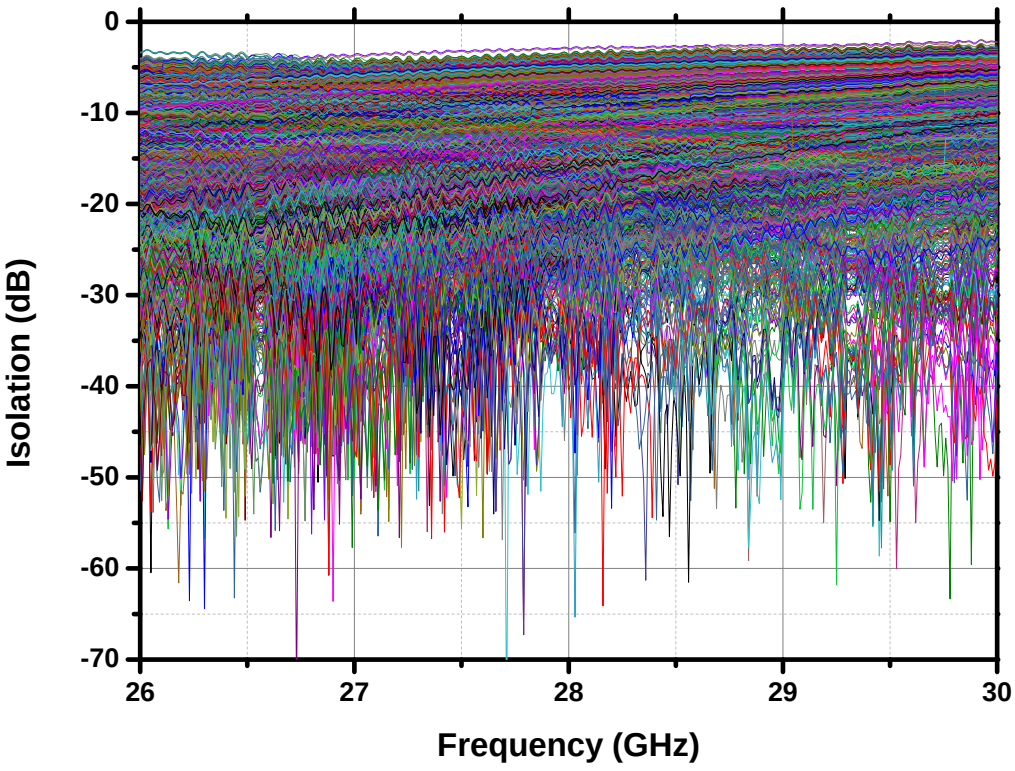


Figure 50: The isolation for every state of the impedance tuner

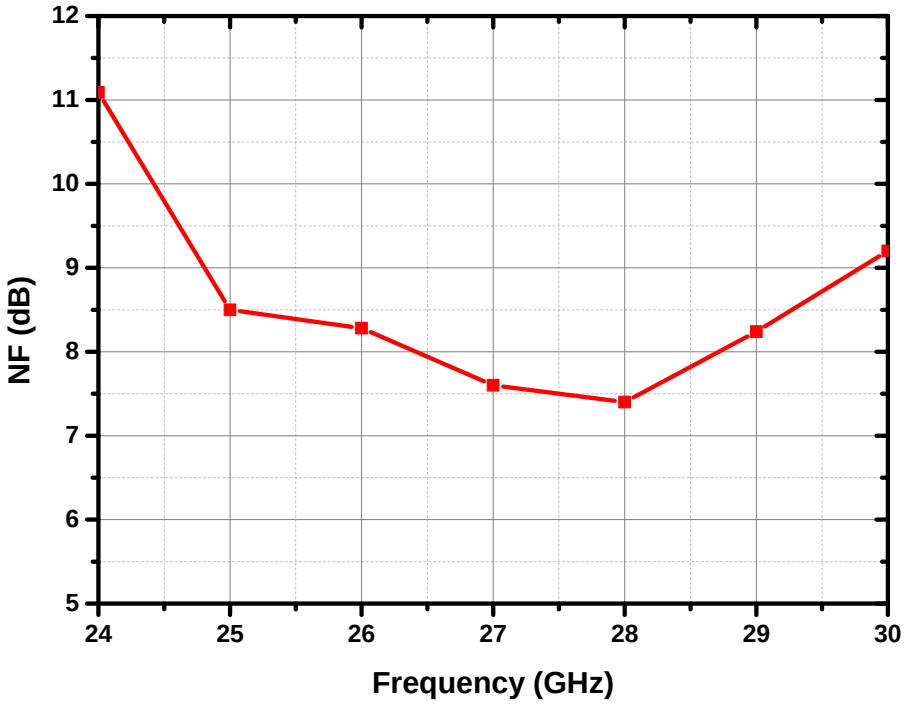


Figure 51: The NF of the receiver

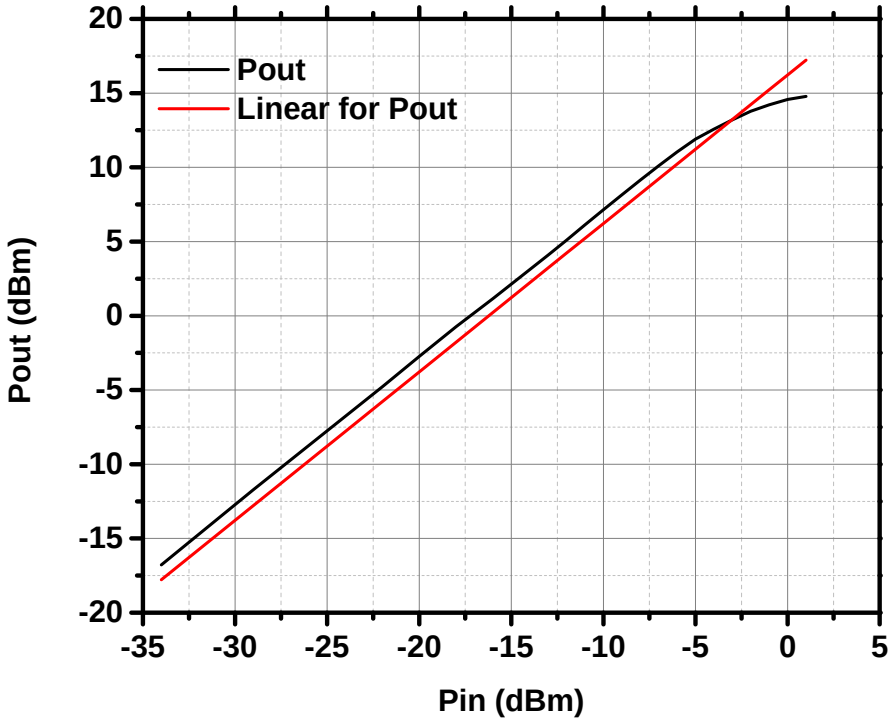


Figure 52: P_{out} vs P_{in} of the receiver

to (21). The written MATLAB code is given in APPENDIX B. For an arbitrary impedance that resides in the VSWR 2 circle, the impedance tuner states are swept and the isolation between TX and RX is calculated. According to these calculations, Fig. 54 shows the antenna impedances that the impedance tuner matches and a

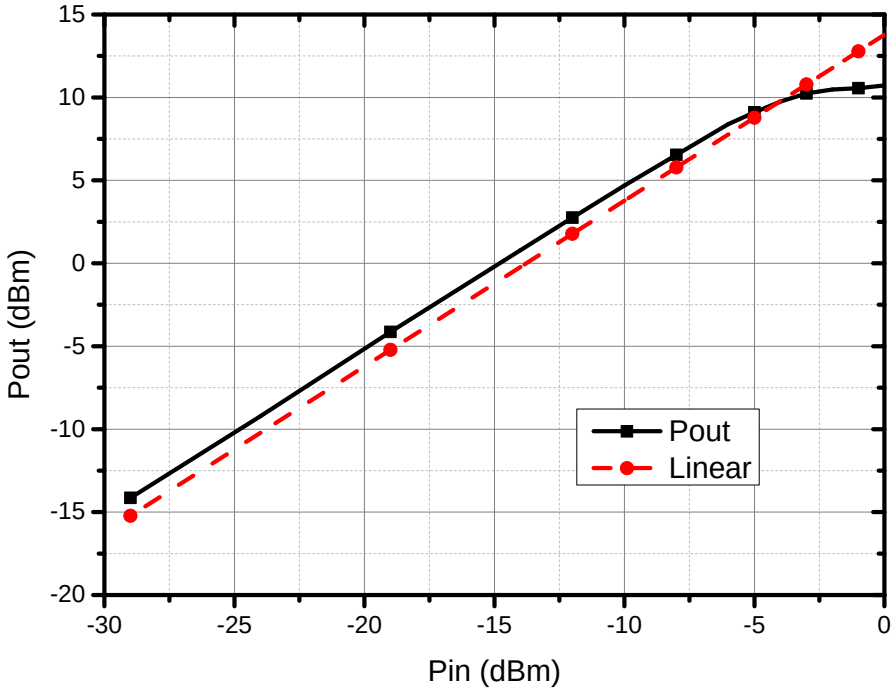


Figure 53: P_{out} vs P_{in} of the transmitter

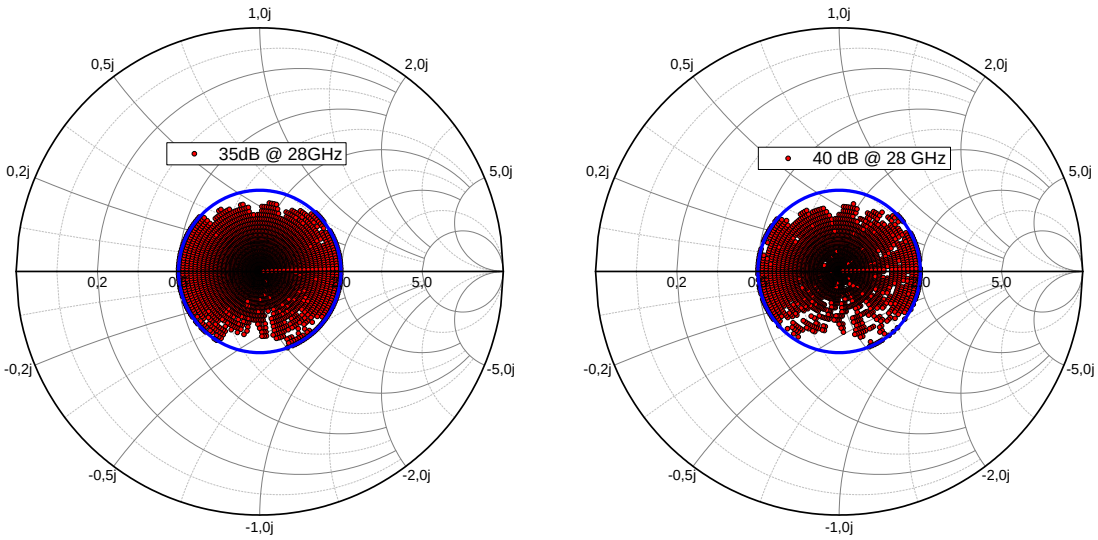
certain level of isolation are obtained. In Fig. 54a, the antenna impedances are shown when 40 dB isolation is obtained whereas 35 dB isolation is the limit for the isolation in Fig. 54b.

3.3 Extension Blocks

After the measurements and interpretation of the collected data were finished, the design of the extension block could be started. In this section, the design of the extension block are explained with the updates in the prototype. The ultimate system which is the combination of the prototype with the mixers was sent to fabrication.

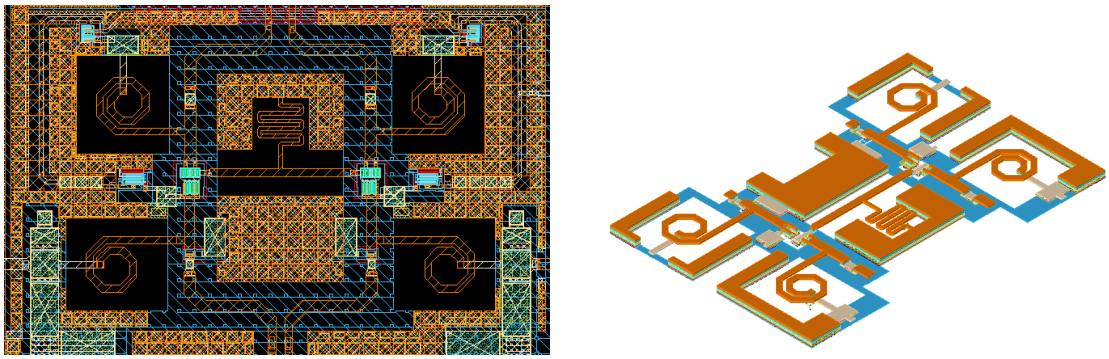
3.3.1 Updates in the Prototype

The prototype was measured with wire-bond packaging. The ultimate system should be suitable for flip-chip packaging. Therefore, the substrate file which had been used in the electromagnetic simulation was modified to have a ground layer 60 μm above the passivization layer rather than having the ground layer below the Si layer. Each block was simulated with the new substrate file to observe the difference in the performance. It is preferred that the results of the electromagnetic



(a) **(b)**

Figure 54: The antenna impedances that 35 dB (a) and 40 dB (b) of isolation is obtained



(a) **(b)**

Figure 55: The layout (a) and 3D view (b) of the first stage of the updated LNA

simulations are presented in the system-level simulations rather than presenting the change in the performance of each block in this section. The sub-blocks except LNA meet the specifications as in the prototype. Due to the updates in the technology pdk and the modification in the substrate file, a stability issue has occurred in the performance of the LNA. Therefore, the first stage of the LNA, which is the reason for the stability problem, is redesigned. the 3D view and layout of the first stage of the LNA are shown in Fig. 55. The updates in the LNA can be listed as the change in the bias points and additional tail inductor which increases CMRR and improve the isolation between TX and RX. The second stage of the LNA was not updated.

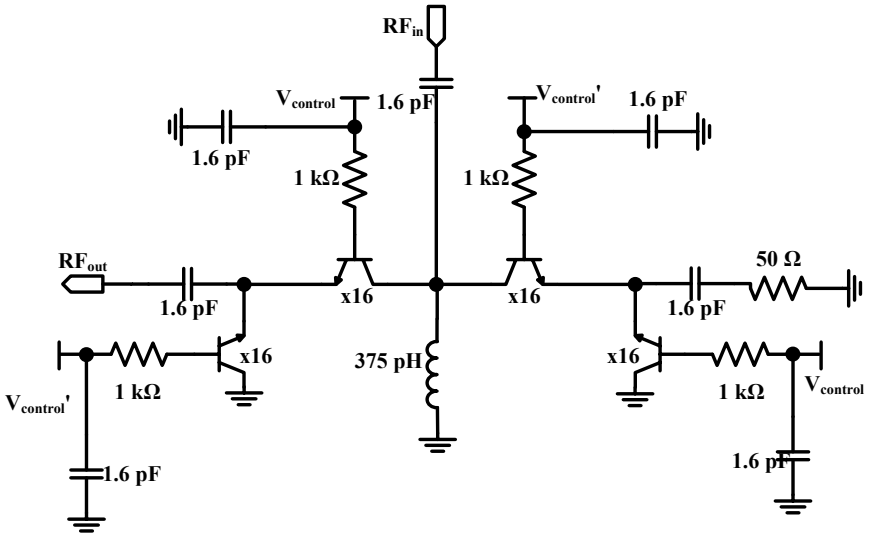
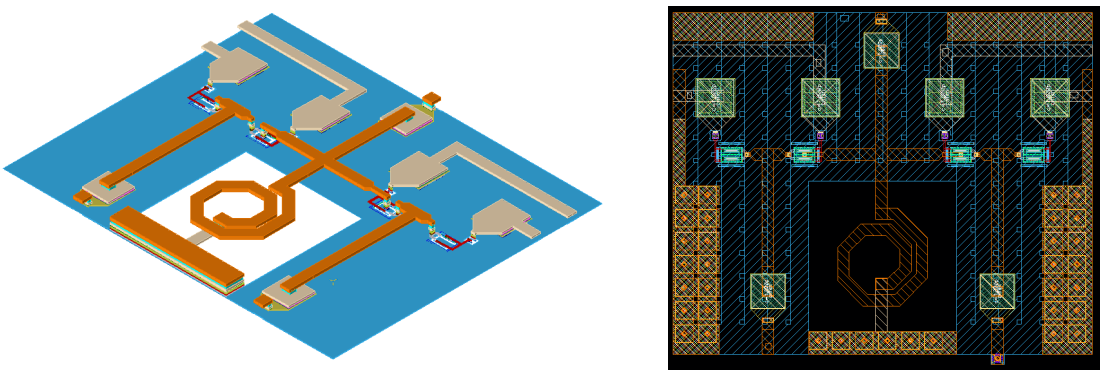


Figure 56: The schematic of the designed SPDT

3.3.2 SPDT Design

When the SIC cannot be provided due to the impedance mismatch, the SI signal appears at the output as a high-power signal and leads to the saturation of the proceeding blocks. In order to prevent this saturation, an attenuator is necessary after the LNA. The attenuator will be turned on when there is a powerful leakage signal. Otherwise, it will be turned off. The determined attenuation step is 30 dB. Obtaining 30 dB attenuation with one attenuator block would require a network for phase compensation. The attenuation step can be divided into smaller attenuator blocks. However, this would increase the area dramatically. Another way to obtain target attenuation is to employ an SPDT with high isolation and low insertion loss. Various attenuator works that have been published recently have achieved to get IL of around 1 dB and isolation of 30 dB [33, 34]. The difference between insertion loss and isolation values can be seen as the attenuation step. To use the SPDT as an attenuator, one port should be terminated with a fixed 50 Ω to get a two-port network. Another advantage of the SPDT is that the terminated port can be connected to a power detector to observe the signal at the output of the LNA. The power detector takes an input RF signal and converts it to a DC value with respect to the power level of the RF signal. In this system, 50 Ω termination is preferred. The specifications for the SPDT are insertion loss of 2 dB and isolation of 32 dB with reasonable matchings.

In general, the switches are constructed with NMOS. However, it is shown that the utilization of the reverse-saturated SiGe HBTs offers better IL and linearity performances [35]. Therefore, the SPDT was designed with the reverse-saturated SiGe HBTs. The topology consists of two series and two shunt switches. The series



(a) **(b)**

Figure 57: The 3D view (a) and layout (b) view of the designed SPDT

switch enables an RF signal to pass whereas the shunt switch opens a path to the ground to reduce the leakage to the undesired port. If a series switch is turned on in one path, the shunt switch in this path and the series switch in the other path is turned off. The shunt switch in the other path is turned on. With this configuration, a signal goes to only one end of the switch with a small IL. The size of the devices plays a key role in the RF performance of the switch. If the size of the series switch is selected to be large, the isolation decreases due to the increased OFF-capacitance of the series switch where signal leaks to the isolated port. If the size is small, then the IL increases due to the ON-resistance of the switch. For the shunt switches, larger size means larger OFF-capacitance that increases the IL and smaller size translates to higher ON-resistance that reduces the isolation. Considering this trade-off, the transistor sizes are found out to be as x16 of a unit device size. 1.6 pF MIM capacitors serve as DC block and bypass capacitors as shown in Fig. 56. A shunt inductor is used to match the port impedances. The 3D view and layout of the designed SPDT are shown in Fig. 57a and Fig. 57b, respectively. The electromagnetic simulations were carried out in ADS whereas the layout was prepared in Cadence Virtuoso. The SPDT was designed by Hamza Kandiş who is a member of the SUMER Research Group.

The area of the designed SPDT is 0.109 mm^2 (360 μm$\times$300 μm). The post-electromagnetic simulations of the designed SPDT are shown in Fig. 58 and Fig. 59. The input and output return losses are better than 10 dB between 25 - 32 GHz. The insertion loss is lower than 2 dB whereas the isolation is approximately 32 dB. There is a 30 dB difference between isolation and insertion loss. In other words, the designed SPDT can serve as a 30 dB attenuator in the system. Fig. 59 indicates that the IP_{1dB} of the designed SPDT is 19 dBm.

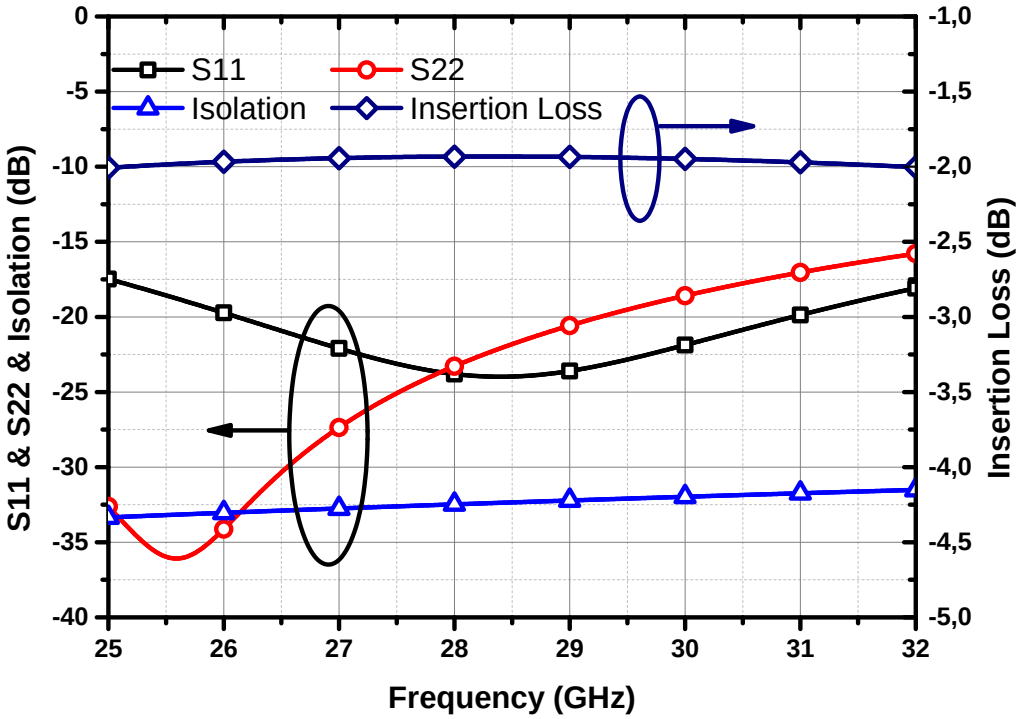


Figure 58: The S11 and S22, insertion loss and isolation of the designed SPDT

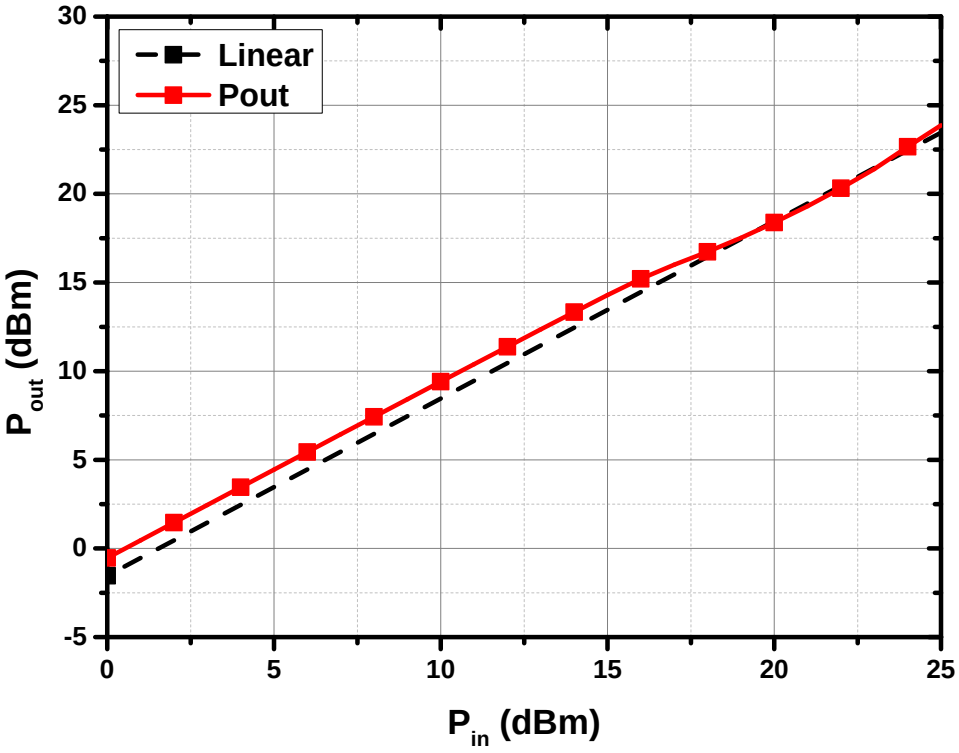


Figure 59: P_{out} vs P_{in} of the SPDT

3.3.3 Downconversion Mixer Design

The mixer is one of the significant blocks in transceiver architectures. Mixers enable to shift the operating frequency of a signal to another frequency. If the input frequency is lower than the output frequency, the mixer is referred to as Downconverter. The mixers that have the opposite functionality are named as Upconverter. Mixers can be divided into two types: active and passive mixers. The capability to provide conversion gain differentiates these two types of mixers [36]. Passive mixers do not have conversion gain. However, they are superior to active mixers in terms of linearity. Another classification of the mixer is done with respect to a topology: unbalanced, single-balance, and double-balanced. Unbalanced topology has the advantage of simplicity and low noise figure. However, the isolation between ports is the main drawback of this topology. On the other hand, double-balanced mixer topology provides the best port-to-port isolations among the mixer topologies. The cost of improved isolation is the complexity, power consumption, and noise figure. The single-balanced topology resides in the middle of unbalanced and double-balanced topology in terms of port-to-port isolation and the complexity of the circuit. In the single-balance mixer topology, the port isolations are better than the unbalanced topology but worse than the double-balanced topology. Compared to the single-balanced topology, the double-balanced topology contains one more BALUN other than BALUNs at the LO and output ports. The extra BALUN increases the area dramatically [36].

The linearity requirements of the downconversion mixer for the system are challenging. The linearity performance of the downconverter is the priority in the design. To satisfy the linearity requirements, the passive mixer structure is preferred since the passive mixers are favorable over the active mixers. Also, to boost the linearity performance, the power level of the LO input signal must be high. As a result of a high LO input signal, the rejection of LO to IF feedthrough becomes another challenge that must be overcome. Since double-balanced topology provides the best port-to-port isolation, it is chosen as the topology of the downconverter. The emitter is biased with 1.7 V to prevent substrate forward bias. The low-pass filter at the output and the image rejection filter at the input of the downconverter is integrated within the downconverter. Elliptic filter topology offers sharp response around the pass-band. The image-rejection filter at the input was designed with the third-order elliptic filter topology. The low-pass filter was also designed with third-order elliptic filter topology. Electromagnetic simulations for passive characterizations were done with the help of ADS Momentum and Sonnet software. Cadence virtuoso is utilized to obtain the layout. The schematic and layout of the downconverter are given

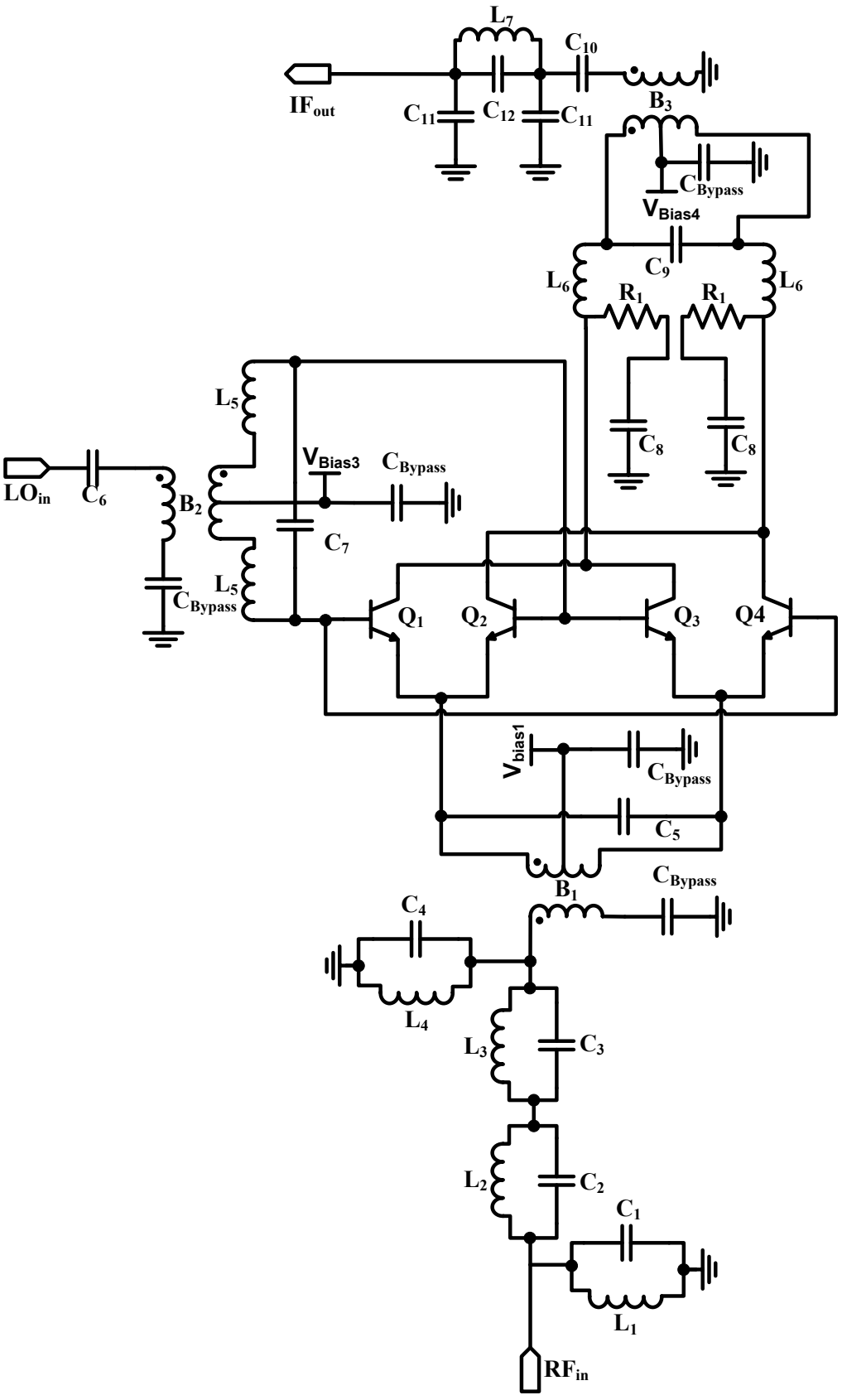


Figure 60: The schematic of the designed downconverter

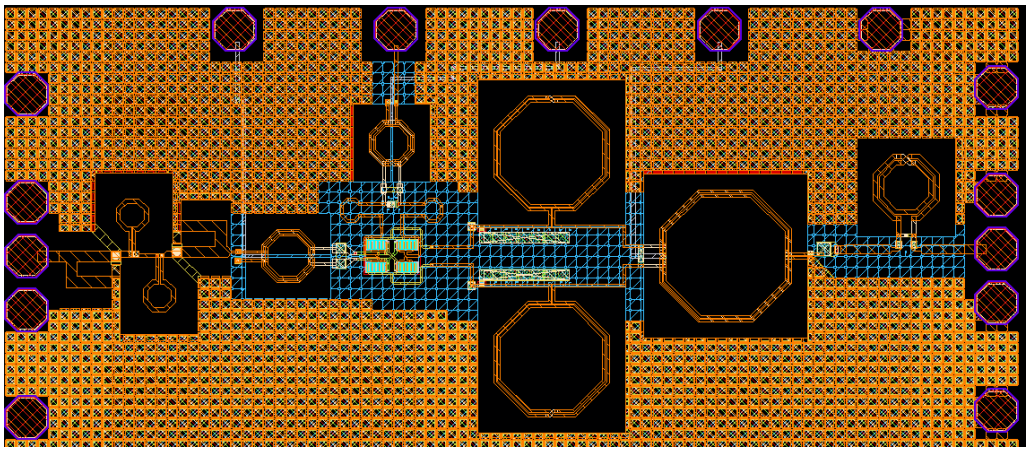


Figure 61: The layout of the designed downconverter

in Fig. 60 and Fig. 61, respectively. The downconverter was designed by Hamza Kandiş.

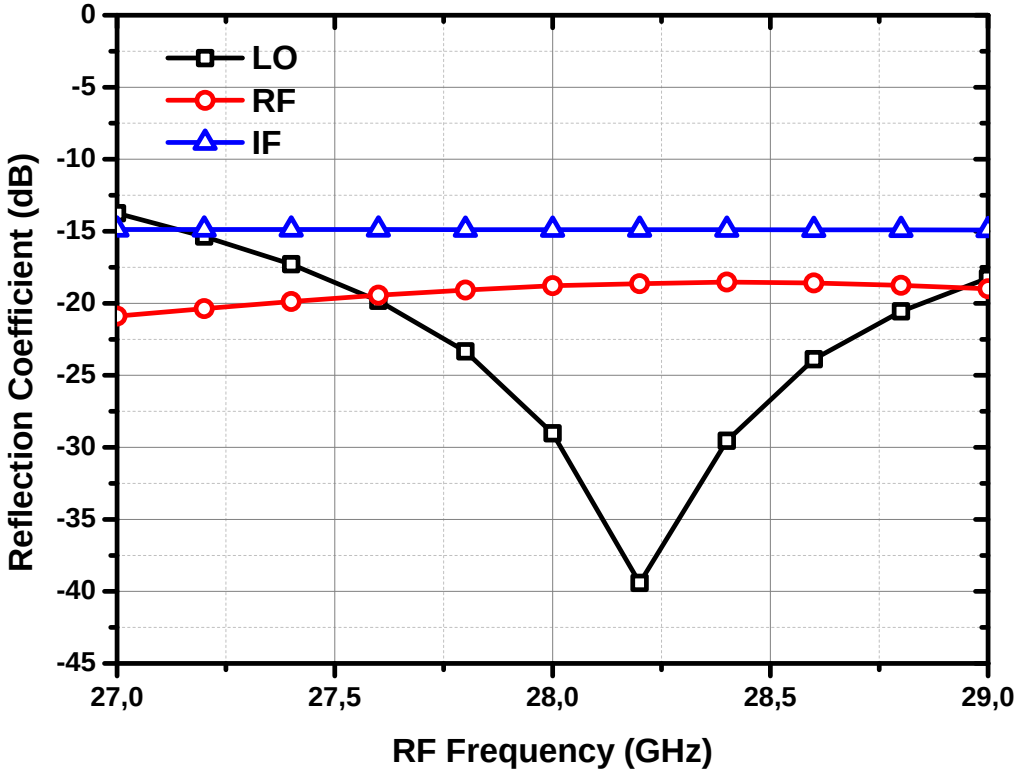


Figure 62: The layout of the designed downconverter

The designed downconverter occupies 1.68 mm×0.7 mm (1.176 mm^2) area. The simulation results of the return loss performance for each port are presented in Fig. 62. The return losses at each port are better than 10 dB in the target frequency range. Port-to-port isolation results are given in 63. The minimum isolation of approximately 45 dB is observed between the LO and RF ports of the downconverter. It should be kept in mind that the downconverter contains the filters. Fig. 63

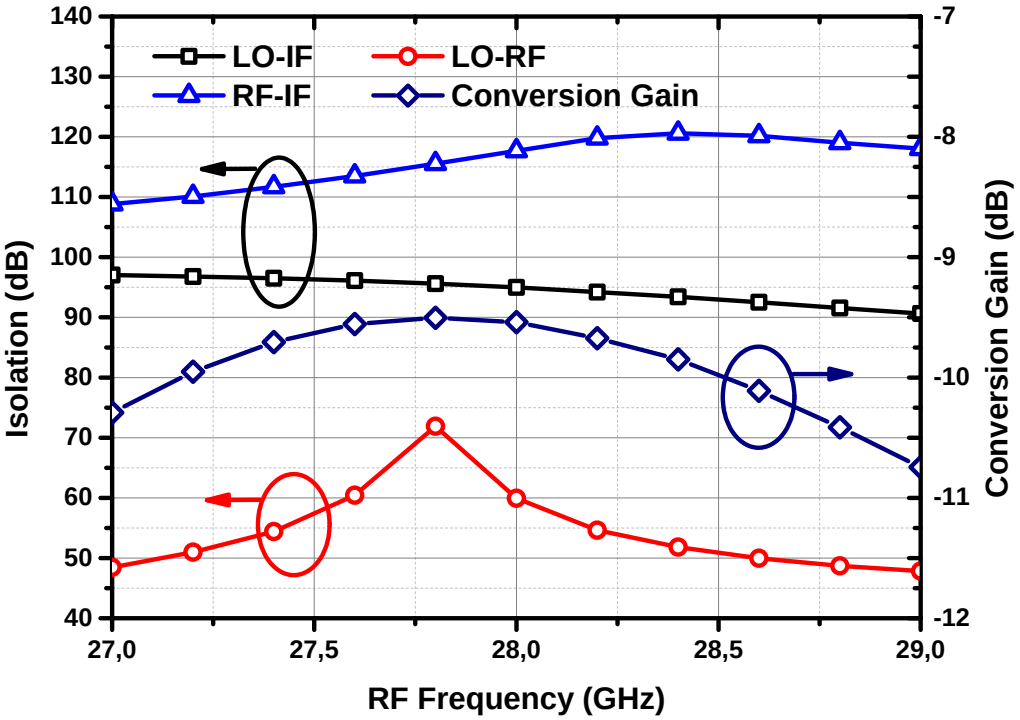


Figure 63: The layout of the designed downconverter

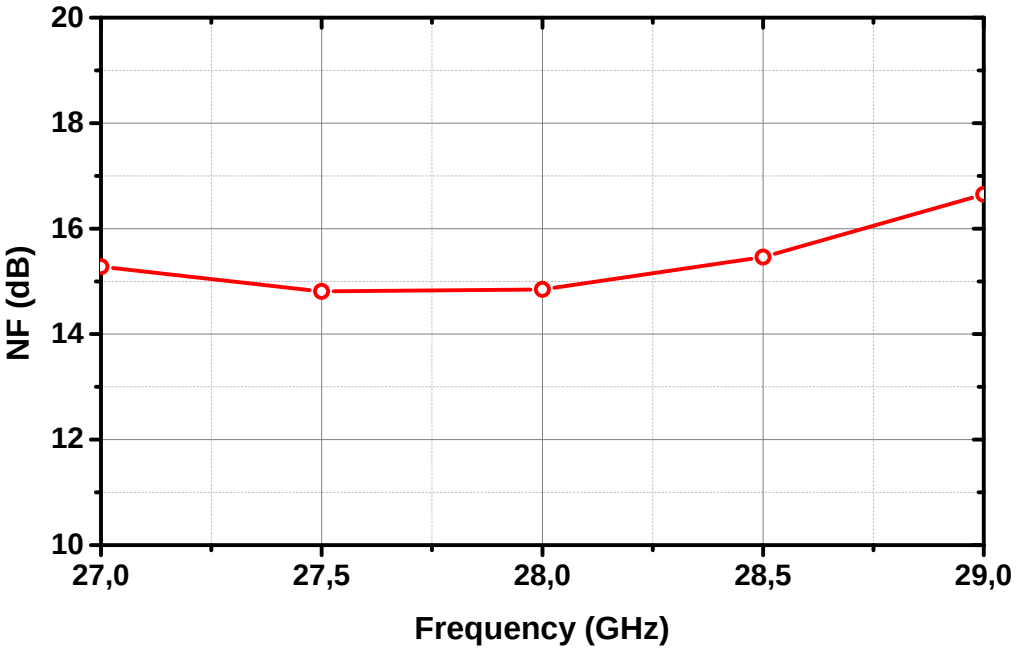


Figure 64: The SSB NF of the designed downconverter

indicates that the minimum conversion loss of 9.5 dB is observed. Fig. 65 indicates that the simulated IP_{1dB} is found to be 14.5 dBm. The single-sideband (SSB) noise figure was simulated to be 15 dB as shown in Fig. 64.

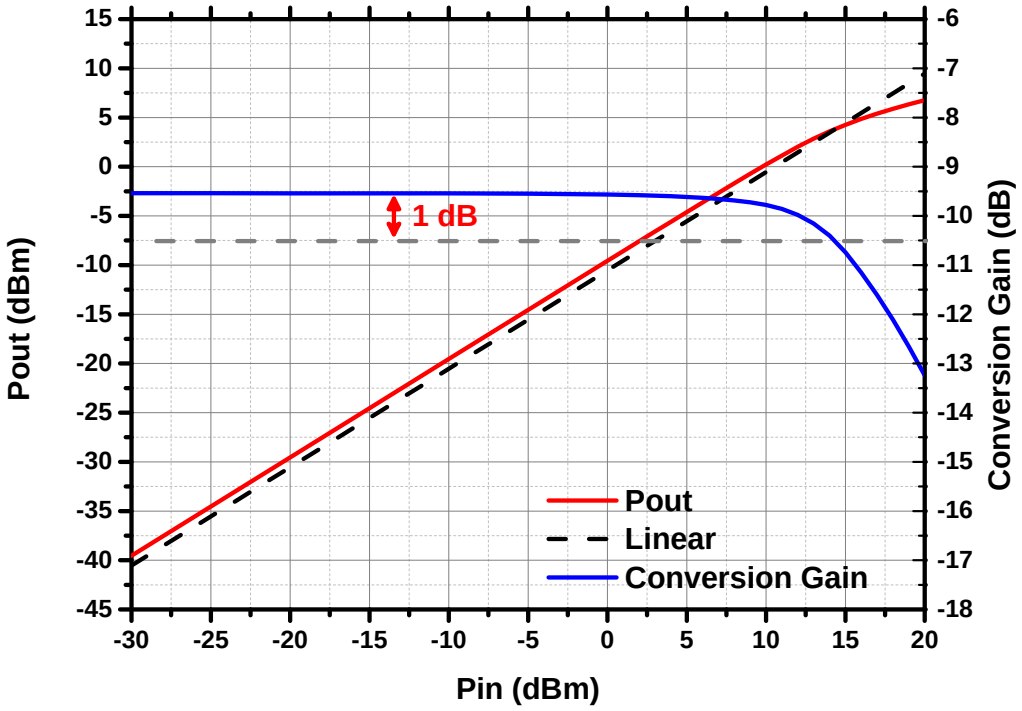


Figure 65: P_{out} vs P_{in} of the designed downconverter

3.3.4 Upconversion Mixer Design

The comparison between the mixer topologies is provided in the previous section. Similar to the downconverter, the rejection of feedthrough and linearity are crucial parameters. In light of the topology comparison in the previous section, the upconverter is designed with double-balance topology. Since a conversion gain is expected from the upconverter, it is an active mixer. Since the input of the upconverter is at IF (3.3 GHz), most of the area is occupied by the inductors. If the IF input was converted to differential signal at the input, the area occupied by the inductors would be doubled. In order to prevent that, the single-ended to differential conversion takes place between the g_m-stage and switching-stage. Another benefit of this configuration can be seen in the power consumption. In a general double-balanced mixer, the g_m-stage and switching-stage are stacked so, the collector voltage of the switching-quad is increased to maintain the linearity performance. However, with a BALUN in the middle, the collector voltage of the switching quad can be 1.8 V instead of 3.3 V. The base bias of switching quad is kept at the Class-B bias level which is the threshold to help switching operation. The BALUNs helped the port matchings. The RF BALUN at the output was included in the filter design. The image filter was designed as third order elliptic filter. The image filter at the output is used in the output matching of the upconverter. Electromagnetic simulations for passive characterizations were done with the help of ADS Momentum and Sonnet software. Cadence virtuoso is utilized to obtain the layout. The schematic

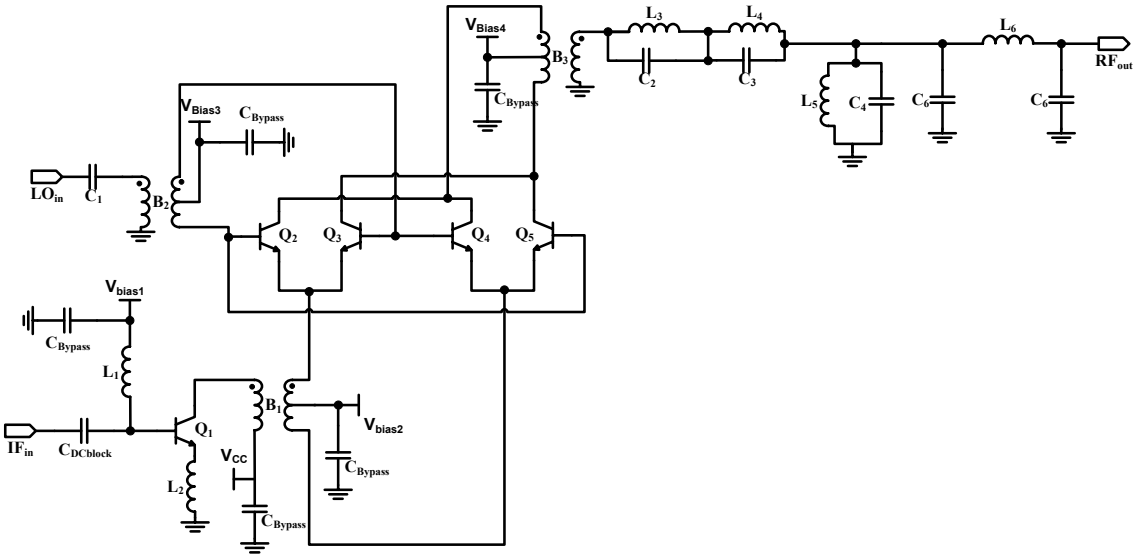


Figure 66: The schematic of the designed upconverter

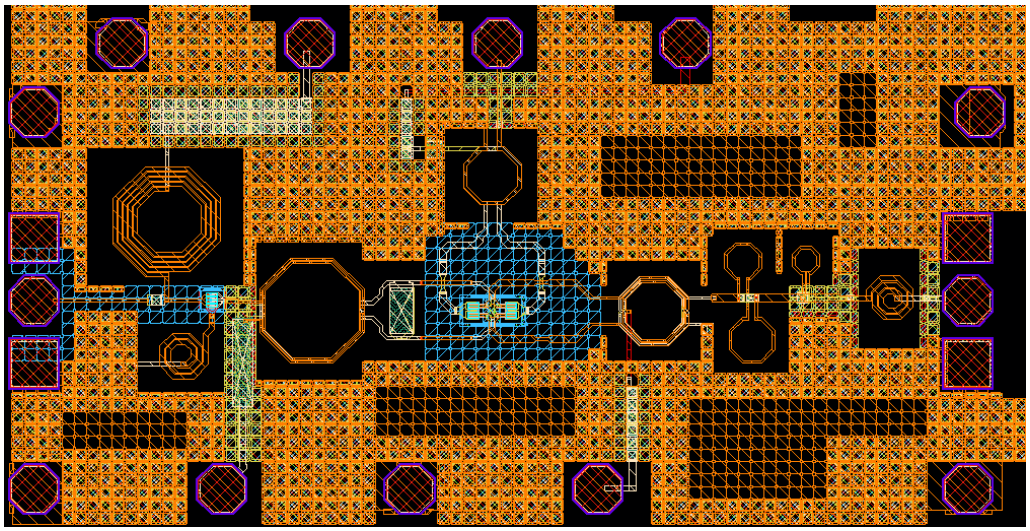


Figure 67: The layout of the designed upconverter

and layout of the upconverter are given in Fig. 66 and Fig. 67, respectively. The downconverter was designed by Işık Berke Güngör, who is a member of SUMER Research Group.

The designed upconverter occupies 1.42×0.65 mm^2 (0.923 mm^2) area. The simulation results of the return loss performance for each port are presented in Fig. 68. The return losses at each port are better than 10 dB in the target frequency range. Port-to-port isolation results are given in 69. The minimum isolation of approximately 42 dB is observed between the LO and RF ports of the downconverter. It should be kept in mind that the upconverter contains the filters. Fig. 69 indicates that the minimum conversion gain of 14 dB is observed. Fig. 70 indicates that the simulated IP_{1dB} and OP_{1dB} are found to be -12 dBm and 2.3 dBm, respectively. An

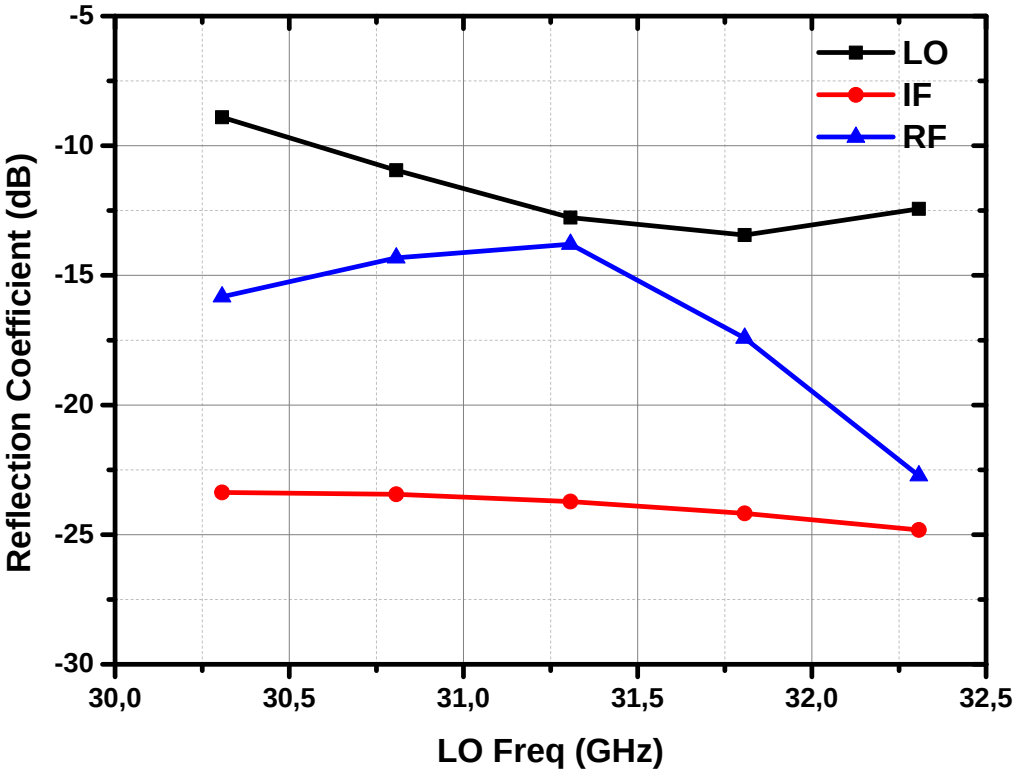


Figure 68: The RF, LO and IF return losses of the designed upconverter

example output spectrum is shown in Fig. 71 when the input power is -30 dBm. In the simulations for this spectrum, the input power was set to -30 dBm. LO input was selected to be 31.3 GHz and IF input was at 3.3 GHz.

3.3.5 System Level Simulations

The layout of the designed system is drawn and prepared to be sent to the fabrication in Cadence Virtuoso. The layout of the system is shown in Fig. 72.The total area of the designed system is 10.8 mm^2 (3.8mm×2.84mm). The pitch size of the pads in the layout is determined to be 300 μm due to the limitation in the PCB fabrication. Buffers from the standard-cell library of IHP technology were utilized in the transmission of the clock signal to prevent degradation in the clock signal. Most of the DC voltages which have the same value were combined to reduce the number of DC voltage pads. The metal 3 layer was used as the ground layer under the transmission lines in order to pass the DC lines under the transmission lines. Each high-frequency pad is surrounded by both sides by ground pads to enable them to employ grounded coplanar stripline on the PCB.

LO input is in the common use of both upconverter and downconverter. It must be distributed between downconverter and upconverter. Also, the required

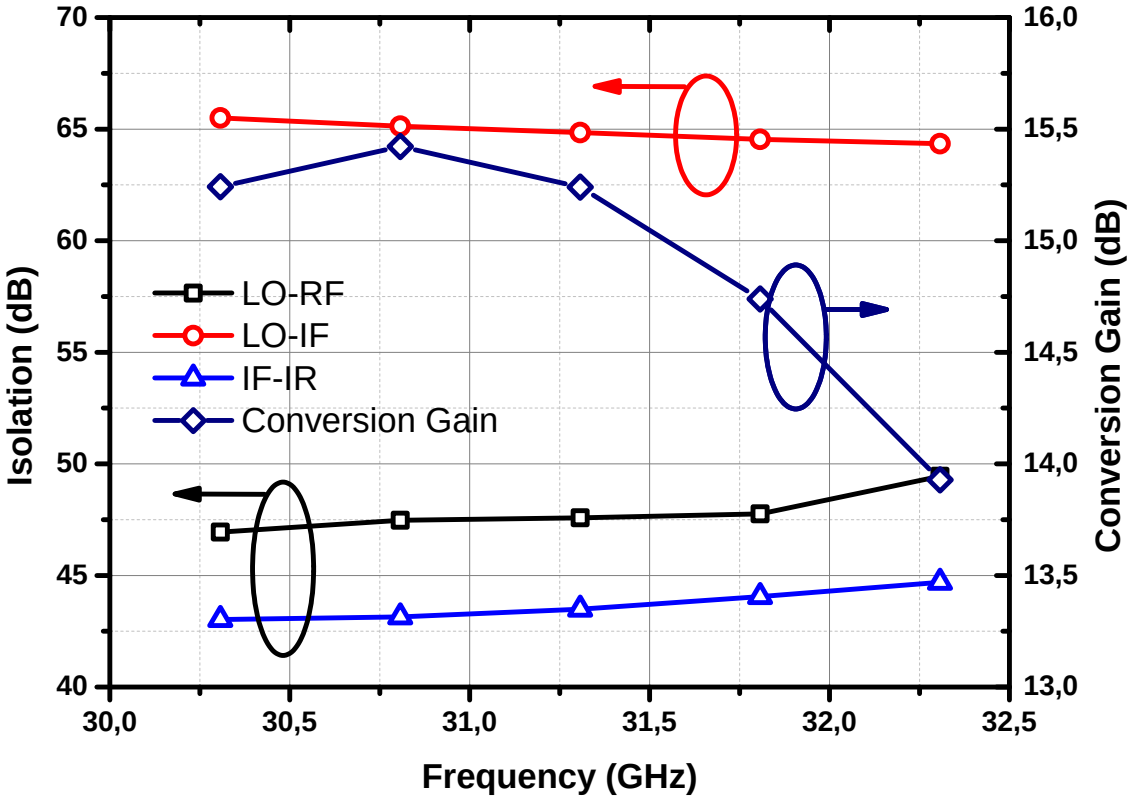


Figure 69: The port isolations and convergence gain of the designed up-converter

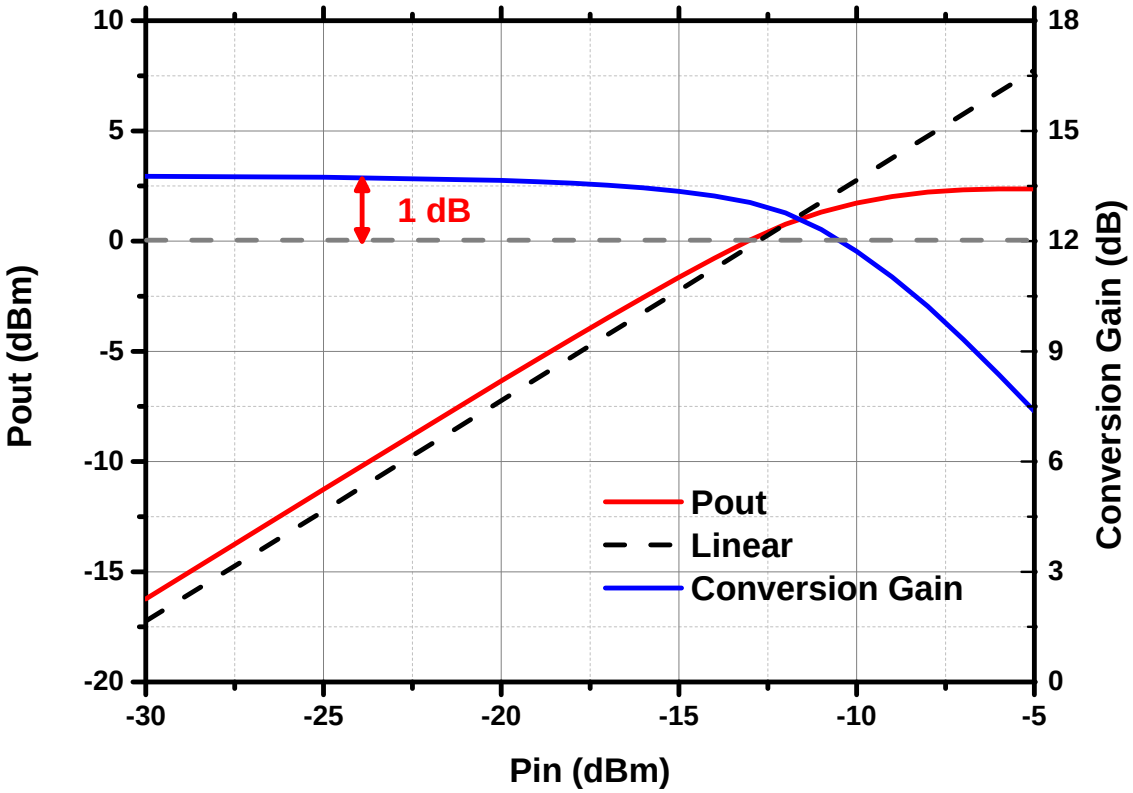


Figure 70: P_{out} vs P_{in} of the designed upconverter

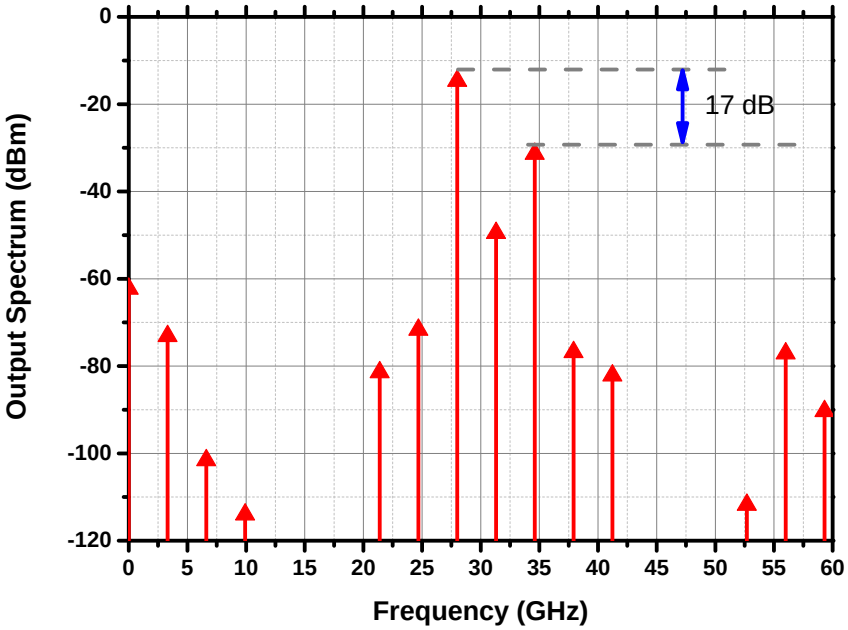


Figure 71: The output spectrum of the designed upconverter

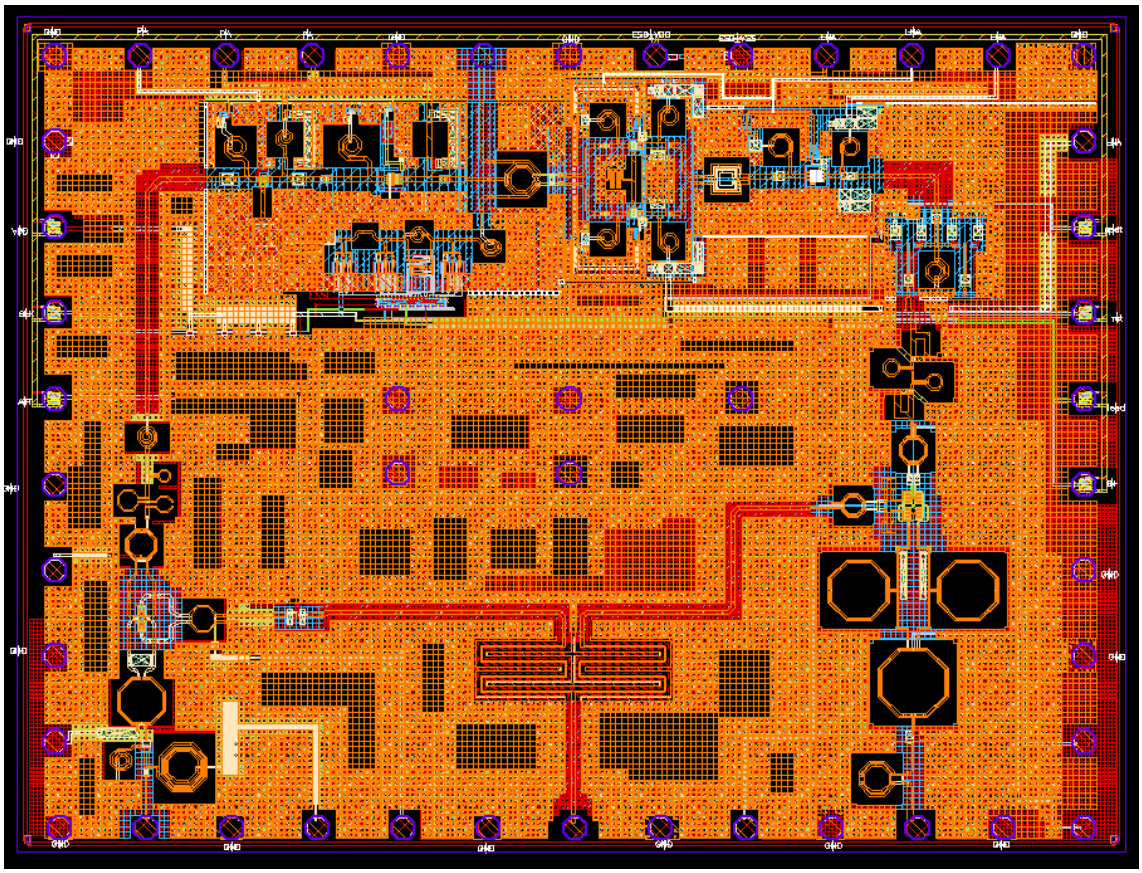


Figure 72: The layout of the designed system

power of the LO signals for upconverter and downconverter is different. In order to distribute the LO signal appropriately, an attenuator is employed in the upconverter path.

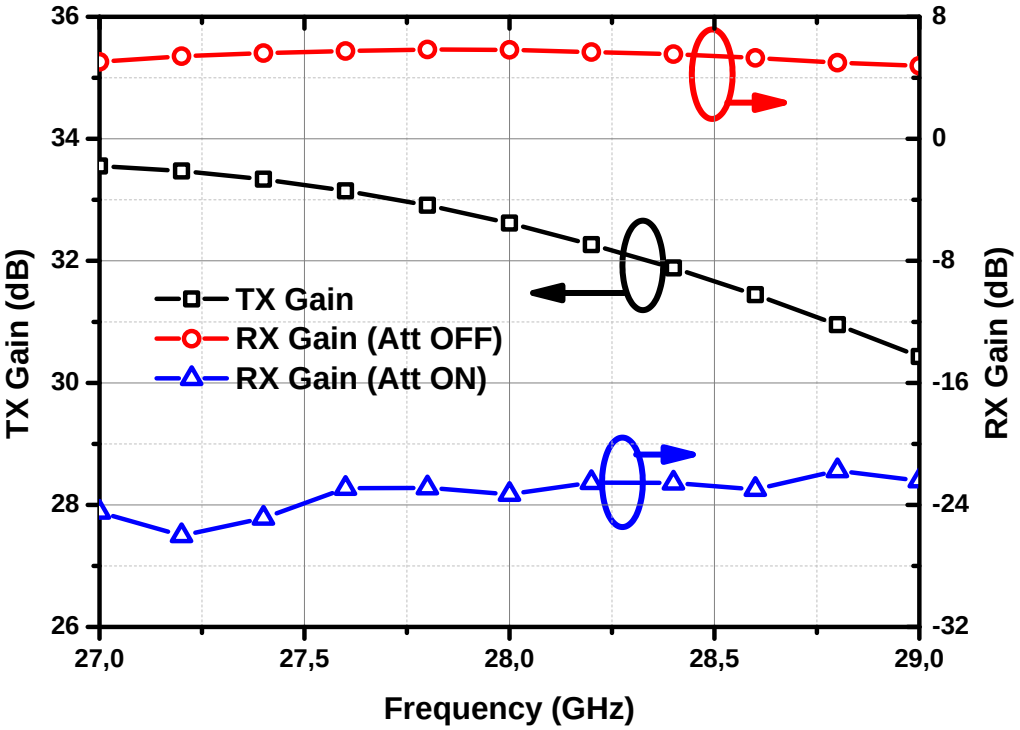


Figure 73: The TX and RX gain performances of the designed system

The electromagnetic simulation files are gathered in ADS to obtain the system performance parameters. Except simulations for isolation, the input of one chain in the system was disabled to obtain the results for the other chain. For example, the NF of the receiver chain was obtained by setting the input of the upconverter to -100 dB. The TX and RX gains are presented in Fig. 73 where the mismatch between the ANT and BAL-ports of the hybrid transformer is set to zero. Fig. 73 shows the functionally of the attenuator in the RX chain. The TX gain was simulated as 30 dB which includes the gain of the upconverter and PA, and the loss of the hybrid transformer. The RX gain is 5 dB as shown in Fig. 73 when the attenuator is disabled. When the attenuator is on, the RX gain drops to 24 dB. The NF simulation indicates that the minimum NF of 8.2 dB is achieved as shown in Fig. 74.

The input power of the upconverter was swept to find 1 dB compression point the transmitter. The output power of the transmitter is presented in Fig. 75 with respect to the input power. Also, Fig. 75 shows the change in the TX gain as the input power increases. The IP_{1dB} and OP_{1dB} of the transmitter are -17 dBm and 12 dBm, respectively. The linearity performance of the receiver was obtained similarly to the transmitter. Fig. 76 shows the change in the output power and gain of the receiver with respect to the input power. The IP_{1dB} and OP_{1dB} of the transmitter are -5 dBm and 0 dBm, respectively.

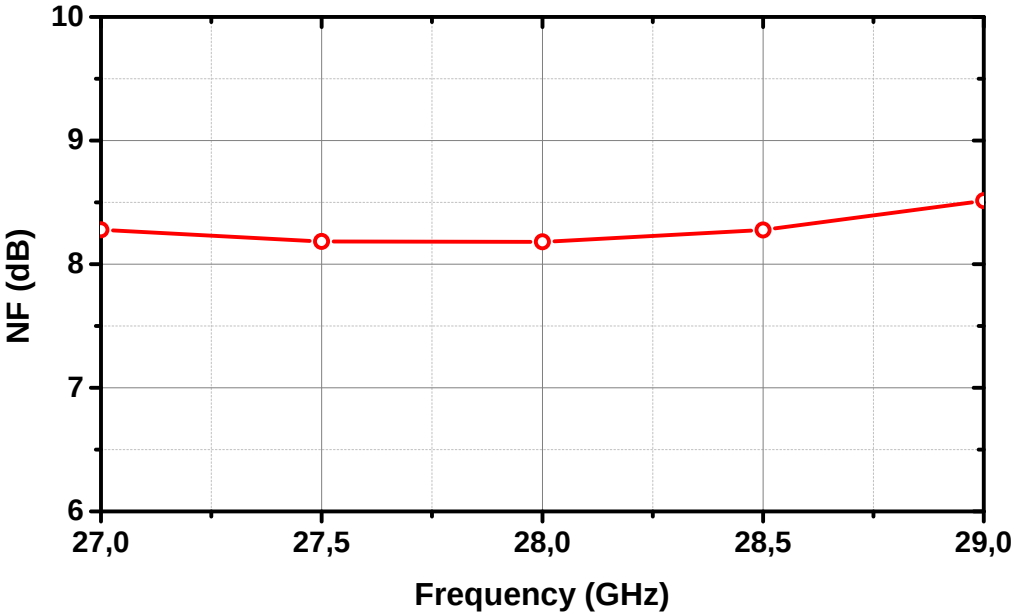


Figure 74: The NF of the receiver of the designed system

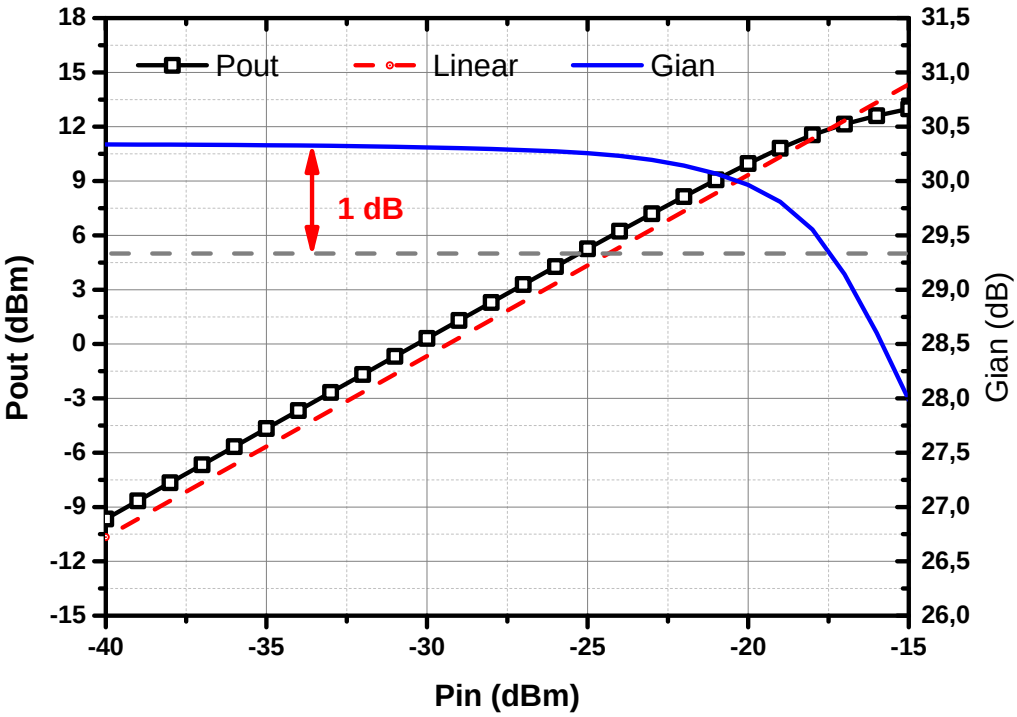


Figure 75: The TX output power and gain of the designed system with respect to the input power

In order to observe the isolation variations, two different scenarios were established, and two different simulations were conducted. To obtain high isolation, both of the impedances were set to 50 Ω. On the other hand, the antenna impedance was set to 40+30j Ω, and the impedance at the balance port was set to 40-30j Ω to see one of the lowest isolation values. The simulation results were shown in Fig. 77. With the perfect matched impedances, the isolation is approximately 40 dB while

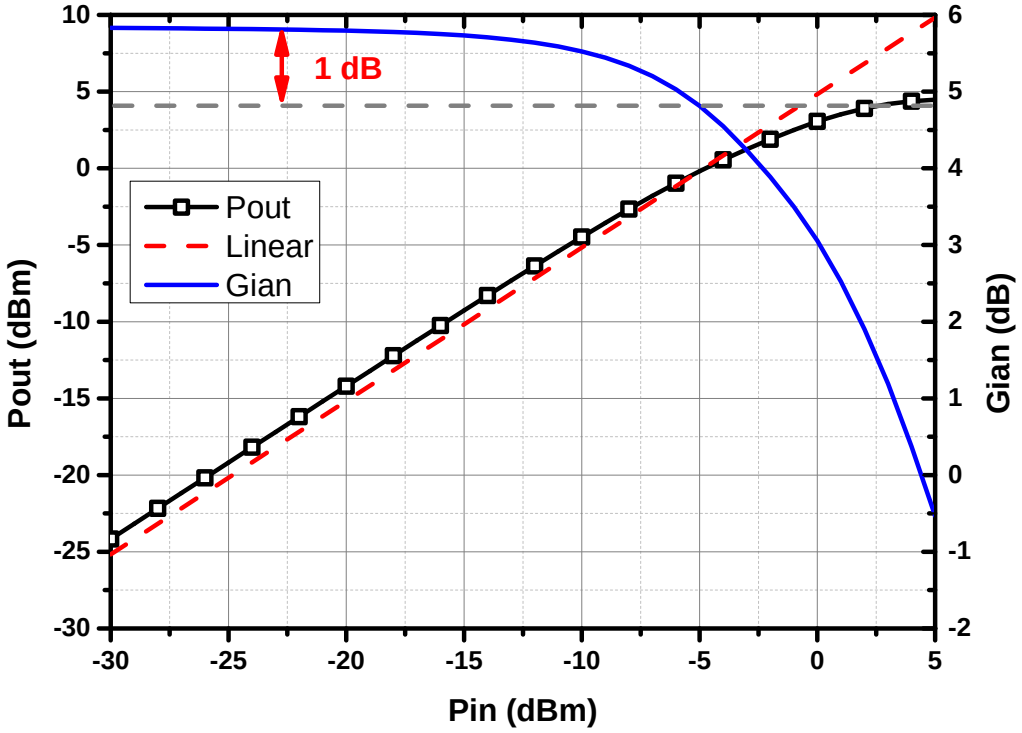


Figure 76: The RX output power and gain of the designed system with respect to the input power

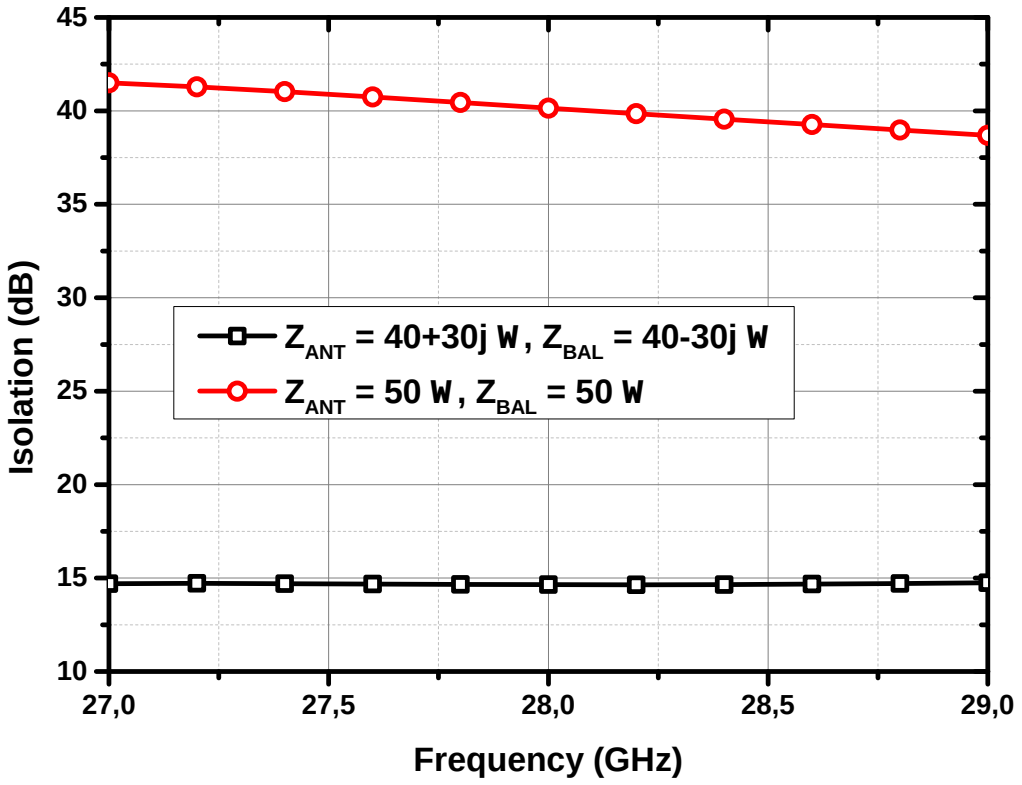


Figure 77: The isolation between the TX and RX ports of the designed system

the mismatch leads to a decrease in the isolation to 15 dB as shown in Fig. 77.

3.3.6 Comparison

The performance comparison of the designed electrical balance duplexer based system with similar works in the literature is provided in Table 3. As many examples of EBD-works are presented in the table, EBD concept has been employed mostly in sub-3GHz systems. With the enhancements in the process technologies, and increase in the target frequencies, the frequency, that EBD is used at, gets higher since it allows more compact transceiver design. The designed system is one of the few works that employ EBD for 5G communications systems. The maximum RX gain in the comparison table was achieved in [37]. On the other hand, in that work, the receiver consists of an LNA. The presented results for this work in the comparison table account for every block in the system including downconverter mixer. The maximum TX gain is obtained in this work compared to the other works in the table. The maximum TX power is 29.2 dBm obtained in [38] which does not have an amplifier before the duplexer.

Table 3: Comparison with similar works in the literature

Ref.	**Technology**	**Freqency (GHz)**	**RX NF (dB)**	**RX Gain (dB)**	**TX Gain (dB)**	**TX Power (dBm)**	**Total Area (mm^2)**	**Isolation (dB)**
[38]	0.18 μm CMOS SOI	0.7-1.0	9	5	-3.8	29.2	14.4	40
[39]	0.18 μm CMOS	1.6-2.2	6.5	-	-3.2	22	0.35	40
[15]	0.18 μm CMOS SOI	1.9-2.2	3.9	-3.9	-3.7	27	1.75	50
[20]	0.18 μm CMOS	1.75-2	-	-11	-3	-	0.67	50
[21]	40 nm CMOS	120	-	-12	-11	11.3	2.314*	30
[37]	0.25 μm SiGe BiCMOS	27-32	4	18	-3.1	-	0.062**	40
[40]	65 nm CMOS	1.5-2.1	5	-	-2.5	12	0.2	50
This Work* **	**0.13 μm SiGe BiCMOS**	**27-29**	**8.2**	**5**	**32**	**12**	**10.8**	**40**

*: Antenna Excluded
**: Only Duplexer Area
***: Simulation Results

4 Conclusion & Future Work

4.1 Summary of Work

It is expected that the next generation (5G) communication systems are going to meet the demands for higher data-rates, higher spectral efficiency, lower latency, and better cost-efficiency. To overcome these challenging specifications, the next generation of communication systems are required to employ technologies such as the utilization of mm-waves, and full-duplex operation. The operation in mm-waves leads to an increase in the bandwidth. The Full-duplex operation enables the spectrum to be used efficiently. Recent developments in SiGe BiCMOS technology enables the transceiver realized with this technology to achieve low-cost solutions without sacrificing the performance.

In this thesis, an electrical balance duplexer based in-band full duplex system for 5G (28 GHz) communication systems is presented targeting the challenging demands from the next generation communication systems. The designed system was implemented in IHP Microelectronics 0.13 μm SiGe BiCMOS SG13S technology. The duplexer core with LNA and PA had been designed, fabricated and measured. The measurement results show that the isolation of 40 dB between the TX and RX ports was achieved for different antenna impedances. The schematic design and implementation of the sub-blocks (LNA, PA, upconverter, downconverter, SPDT, impedance tuner and hybrid transformer) are presented. The simulation results of the sub-blocks, that were not fabricated, and the entire system were demonstrated. The transmitter gain of the system is more than 30 dB by achieving $OP1_{dB}$ of 12 dBm whereas the receiver gain of 5 dB is obtained. The minimum noise figure of the receiver is 8.2 dB.

4.2 Future Work

In the short term, a PCB board must be designed and fabricated for the measurements. After the fabricated chip will arrive, the chip will be packaged with flip-chip packaging. The simulation results of the designed system must be verified with the measurement results. Further, an antenna can be integrated in board-level to observe the effects of the environmental condition on the functionality. After test and verification, the complications will be investigated if there will be any. necessary updates will be applied.

In order to observe the isolation or construct a closed-loop for the control of the impedance tuner, a power detector can be connected to the unused port of the SPDT. The efficiency in the usage of area must be improved to reduce the chip size. This can be achieved with the modifications in the sub-block level.

As a long term future work, the designed transceiver can be combined to another chip, which has the capability of analog SIC, for further improvements in the isolation between TX and RX. For a communication system, the combination of SIC in RF, analog and digital domains is required to suppress the SI signal to the noise floor.

APPENDIX

A. Appendix

```
module talpertunersweepv2(rst,clk,outrst,outclk,outdata,load,LED5,LED0,LED2) //
Verilog code for FPGA;
input rst,clk;
output reg load;
output reg outdata;
output reg outclk;
output reg outrst;
output reg LED5,LED0,LED2;
reg [8:0] clkcounter;
reg [11:0] data;
reg [3:0] index;
reg [23:0] state;
always @ (posedge clk or negedge rst)
begin
if(rst)
begin
outrst = 0;
clkcounter = 0;
end
else if (clkcounter[8] && clkcounter[7]) // outclk freq 98 KHz = 10 us
begin
outrst = 1;
clkcounter = clkcounter + 1;
end
else
begin
outrst = 1;
clkcounter = clkcounter  1;
end
end
always @ (posedge outclk or negedge outrst)
begin
if(outrst)
state = 0;
```

```
else if (state == 1080000) //period is 11.1 sn
state = 0;//state;
else
state = state +1;
end
always @(posedge outclk or negedge rst)
begin
if(rst)
begin
index = 0;
load = 0;
data = 12'b 000000000000;
end
else if(state  1)
begin
load = 0;
data = data;
end
else if(state  13)
begin
load = 1;
index = 12 - state;
end
else
begin
load = 0;
end
end
always @(*)
begin
outclk = clkcounter[8];
outdata = data[index];
LED5 = clkcounter[8];
LED0 = load;
LED2 = outdata;
end
endmodule
```

B. Appendix

clear all;
clc;
numOfStates = 4095; gamma_Start = 0;
gamma_End = 1/3;
gammaIncrement = (gamma_End)/10; gamma_numOfStep = ((gamma$_E$nd−*gamma_Start*)/*gamm*
1;
$degree_Start = 0$;
$degreeIncrement = 4; degree_End = 360 - degreeIncrement$;
$degree_numOfStep = ((degree_End - degree_Start)/degreeIncrement) + 1$;
$total_numOfStep = (degree_numOfStep * gamma_numOfStep) - (360/degreeIncrement) +$
1;
$table_40dB_28GHz = zeros(total_numOfStep, numOfStates + 2)$;
$table_35dB_28GHz = zeros(total_numOfStep, numOfStates + 2)$;
$table_counter = 0$;
$z0 = 50$;
$zIn = 50$;
$dB_s21 = zeros(1, numOfStates)$;
$dB_s31 = zeros(1, numOfStates)$;
$dB_s23 = zeros(1, numOfStates)$;
$iso_array = zeros(1, numOfStates)$;
$forgammaAnt = gamma_Start : gammaIncrement : gamma_End$
$if(gammaAnt == 0)$
$degreeIncrement = 360$;
$else$
$degreeIncrement = 4$;
end
$fordegreeAnt = degree_Start : degreeIncrement : 360 - degreeIncrement$
$forcounter = 0 : 1 : numOfStates$
$filename_part1 =' C : _193p_meas_2'$;
$filename_part2 = int2str(counter)$;
$filename_part3 =' .s3p'$;
$filename = strcat(filename_part1, filename_part2, filename_part3)$;
$SingleEnded3Port = read(rfdata.data, filename)$;
$S = sparameters(SingleEnded3Port)$;
$numports = S.NumPorts$;
$freq = S.Frequencies$;

$numfreq = numel(freq);$
$z0 = S.Impedance;$
$freq = S.Frequencies;$
$center_freq = freq(401); gamma = gammaAnt*(cosd(degreeAnt)+(i*(sind(degreeAnt))));$
$zLoad = gamma2z(gamma, z0);$
$rLoad = real(zLoad);$

$xLoad = imag(zLoad);$
$system = nport(S,'system_28GHz');$
$ckt = circuit('system_s');$
$add(ckt, [123], system);$
$cktLoad = circuit('load');$
$rfel = rfelement('Zin', zLoad,'Zout', zLoad);$
$add(cktLoad, [45], rfel);$
$setports(cktLoad, [45], 'load_In''load_Out');$
$add(ckt, [30], cktLoad);$
$setports(ckt, [10], [20], 'PA_in''LNA_out');$
$S_new = sparameters(ckt, center_freq);$
$system2 = nport(S,'system_28GHz');$
$ckt2 = circuit('system_s');$
$add(ckt2, [123], system2);$
$add(ckt2, [20], resistor(50));$
$setports(ckt2, [10], [30], 'PA_in''Ant');$
$S_new2 = sparameters(ckt2, center_freq);$
$data_RF = rfdata.data;$
$data_RF.Freq = center_freq;$
$data_RF.S_parameters = S_new2.Parameters;$
$data_RF.ZL = zLoad;$
$data_RF.ZS = zIn;$
$[data1, params1, freq1] = calculate(data_RF,'Gt','dB'); system3 = nport(S,'system_28GHz');$
$ckt3 = circuit('system_s');$
$add(ckt3, [123], system3);$
$add(ckt3, [10], resistor(50));$
$setports(ckt3, [30], [20], 'Ant''LNA_out');$
$S_new3 = sparameters(ckt3, center_freq);$
$data_RF2 = rfdata.data;$
$data_RF2.Freq = center_freq;$
$data_RF2.S_parameters = S_new3.Parameters;$
$data_RF2.ZL = zIn;$

$data_RF2.ZS = zLoad;$
$[data2, params2, freq2] = calculate(data_RF2,'Gt','dB');$
$isolation = mag2db(abs(S_new.Parameters(2,1,:))) - (data11,1 + data21,1);$
$table_40dB_28GHz(table_counter + 1, 1) = zLoad;$
$table_35dB_28GHz(table_counter + 1, 1) = zLoad;$
$if(isolation < -40)$
$table_40dB_28GHz(table_counter + 1, counter + 2) = isolation;$
$elseif(isolation < -35)$
$table_35dB_28GHz(table_counter + 1, counter + 2) = isolation;$
end

end
$table_counter = table_counter + 1;$
end

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