

An Efficient FPGA Implementation of Versatile Video Coding Intra Prediction

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Abstract—Versatile Video Coding (VVC) is a new international video compression standard offering much better compression efficiency than previous video compression standards at the expense of much higher computational complexity. In this paper, an efficient FPGA implementation of VVC intra prediction for angular prediction modes of 4x4, 8x8, 16x16 and 32x32 prediction unit sizes is proposed. In the proposed FPGA implementation, four constant multiplications used in one intra angular prediction equation are implemented using two DSP blocks and two adders in FPGA. The proposed FPGA implementation of VVC intra prediction, in the worst case, can process 34 full HD (1920x1080) frames per second.

Keywords— VVC, intra prediction, hardware implementation, FPGA, DSP block.

I. INTRODUCTION

ITU and ISO are developing a new international video compression standard called Versatile Video Coding (VVC) [1]-[6]. VVC will have higher compression efficiency than H.264 and High Efficiency Video Coding (HEVC) standards at the expense of much higher computational complexity [7]-[10].

Intra prediction algorithm predicts pixels of a block from the pixels of its already coded and reconstructed neighboring blocks. Intra prediction algorithm used in VVC is more complex than intra prediction algorithm used in HEVC. In HEVC, intra prediction unit (PU) size can be 4x4, 8x8, 16x16 and 32x32, for the luminance component of a video frame. There are 35 intra prediction modes for each PU size including DC and planar modes. 14848 intra prediction equations should be calculated for all PUs in a 32x32 coding unit (CU). HEVC intra angular prediction equations are 2-tap FIR filters [10].

In VVC, intra PU size can be 4x4, 8x8, 16x16, 32x32 and 64x64, for the luminance component of a video frame. There are 67 intra prediction modes for each PU size including DC and planar modes. 41288 intra prediction equations should be calculated for all PUs in a 32x32 CU. VVC intra angular prediction equations are either 4-tap gaussian or 4-tap cubic filters.

Xilinx FPGAs have built-in full-custom DSP blocks which can perform constant multiplications faster and with less energy than adders and shifters. A DSP block can be used to perform different constant multiplications by providing proper constant value to its input. Therefore, it is more efficient to implement

constant multiplications using DSP blocks instead of using adders and shifters in an FPGA implementation.

In this paper, an efficient FPGA implementation of VVC intra prediction for angular prediction modes of 4x4, 8x8, 16x16 and 32x32 PU sizes is proposed. The proposed FPGA implementation uses 30 identical DSP datapaths (DDP). In the proposed FPGA implementation, intra angular prediction equations are manipulated in such a way that one intra angular prediction equation is implemented using two DSP blocks and two adders. Therefore, each DDP has two DSP blocks and two adders, and it can calculate any 4-tap gaussian and cubic filter used in VVC intra angular prediction in one clock cycle by changing DSP inputs.

The proposed VVC intra angular prediction hardware is implemented using Verilog HDL. The Verilog RTL code is verified to work at 119 MHz on a Xilinx Virtex 7 FPGA. The proposed VVC intra angular prediction hardware, in the worst case, can process 34 full HD (1920x1080) frames per second.

Two VVC intra prediction hardware implementations are proposed in [11]. Several HEVC intra prediction hardware implementations are proposed in the literature [12]-[15]. In Section III, VVC intra prediction hardware proposed in this paper is compared with VVC and HEVC intra prediction hardware in the literature.

The rest of the paper is organized as follows. In Section II, VVC intra angular prediction algorithm is explained. In Section III, the proposed FPGA implementation of VVC intra angular prediction is presented, and its implementation results are given. Finally, Section IV presents the conclusions.

II. VVC INTRA PREDICTION ALGORITHM

VVC intra prediction algorithm predicts the pixels in prediction units (PU) of a coding unit (CU) using the pixels in the available neighboring PUs. For the luminance component of a frame, 4x4, 8x8, 16x16, 32x32 and 64x64 PU sizes are available. As shown in Fig. 1, there are 65 angular prediction modes (Mode) corresponding to different prediction angles (Angle) for each PU size. In addition, there are DC and planar prediction modes for each PU size. An 8x8 PU, four 4x4 PUs in it, and their neighboring pixels are shown in Fig. 2.

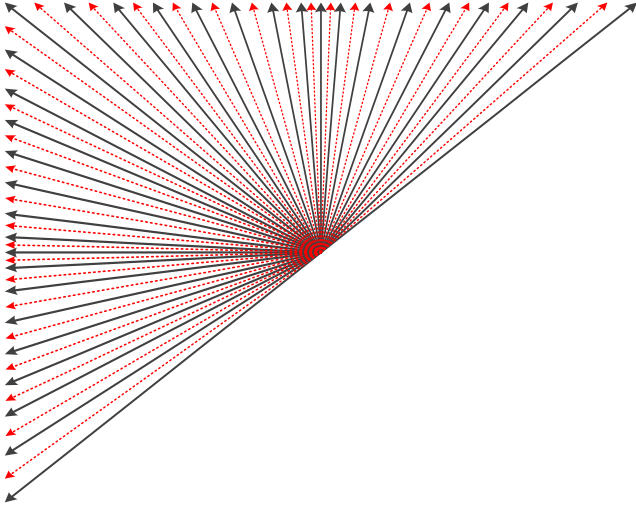


Fig. 1. VVC intra angular prediction modes.

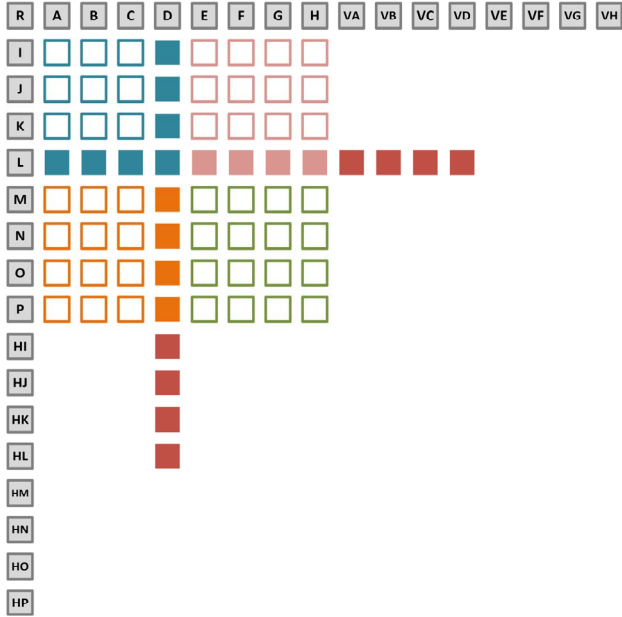


Fig. 2. Neighboring pixels of 4x4 and 8x8 PUs.

17 different 4-tap cubic filters and 17 different 4-tap gaussian filters are used as intra prediction equations. Cubic filters are used for 4x4 and 8x8 PUs. Gaussian filters are used for 16x16, 32x32 and 64x64 PUs.

In VVC intra prediction algorithm, first, reference main array is determined. Reference main array consists of pixels that will be used in intra prediction equations of the corresponding prediction mode and PU size. The reference main array is filled with above neighboring pixels if the prediction mode is equal to or greater than 34. However, if prediction angle is less than zero, first four pixels of the reference main array are filled with left neighboring pixels. The reference main array is filled with left neighboring pixels if the prediction mode is less than 34. However, if the prediction angle is less than zero, first four pixels of the reference main array are filled with above neighboring pixels.

TABLE I. INTRA ANGULAR PREDICTION EQUATION REDUCTIONS BY DATA REUSE

	Cubic Filters			Gaussian Filters		
	4x4 PU	8x8 PU	32x32 CU	16x16 PU	32x32 PU	32x32 CU
# of Pred. Equations	1040	4160	133120	16680	66560	133120
# of Pred. Equations with Data Reuse	405	1042	29478	2597	6641	11810
Reduction (%)	61.06	74.95	77.85	84.43	90.02	91.13

Then, ΔInt and $\Delta Fract$ values are calculated as shown in (1a) and (1b), respectively. ΔInt is used to determine the positions of the pixels, that will be used in intra prediction equations, in reference main array. The four pixels that will be used in intra prediction equations are adjacent pixels in the reference main array, but they may not be adjacent in the video frame. These four pixels are selected as shown in (2a)-(2e), where $p[0]$, $p[1]$, $p[2]$ and $p[3]$ are the selected pixels from reference main array. If $p[1]$ is the left-most pixel in the reference main array, $p[0]$ is equal to $p[1]$. If $p[2]$ is the right-most pixel in the reference main array, $p[3]$ is equal to $p[2]$. PU size is used to determine whether cubic or gaussian filters will be used. $\Delta Fract$ is used to determine which 4-tap filter among 17 4-tap filters will be used.

$$\Delta Int = ((y + 1) * Angle) \gg 5 \quad (1a)$$

$$\Delta Fract = ((y + 1) * Angle) \& 31 \quad (1b)$$

$$refMainIndex = x + \Delta Int + 1 \quad (2a)$$

$$p[1] = refMain[refMainIndex] \quad (2b)$$

$$p[2] = refMain[refMainIndex + 1] \quad (2c)$$

$$p[0] = (x == 0) ? p[1] : refMain[refMainIndex - 1] \quad (2d)$$

$$p[3] = (x == (width - 1)) ? p[2] : refMain[refMainIndex + 2] \quad (2e)$$

$$x = 0 \text{ to } (PU_{size} - 1), y = 0 \text{ to } (PU_{size} - 1)$$

III. PROPOSED VVC INTRA PREDICTION HARDWARE

In VVC, identical prediction equations are used in an intra angular prediction mode or in different intra angular prediction modes or in the intra angular prediction modes of different PU sizes. In the proposed hardware, data reuse technique is used to calculate identical prediction equations only once. There are 4×4 (PU size) \times 65 (intra angular prediction modes) = 1040 intra angular prediction equations for 4x4 PU size. Numbers of prediction equations for other PU sizes are shown in Table I. The number of prediction equations calculated for 4x4 PU size is reduced to 405 by using data reuse technique. Numbers of prediction equation reductions for other PU sizes are shown in Table I.

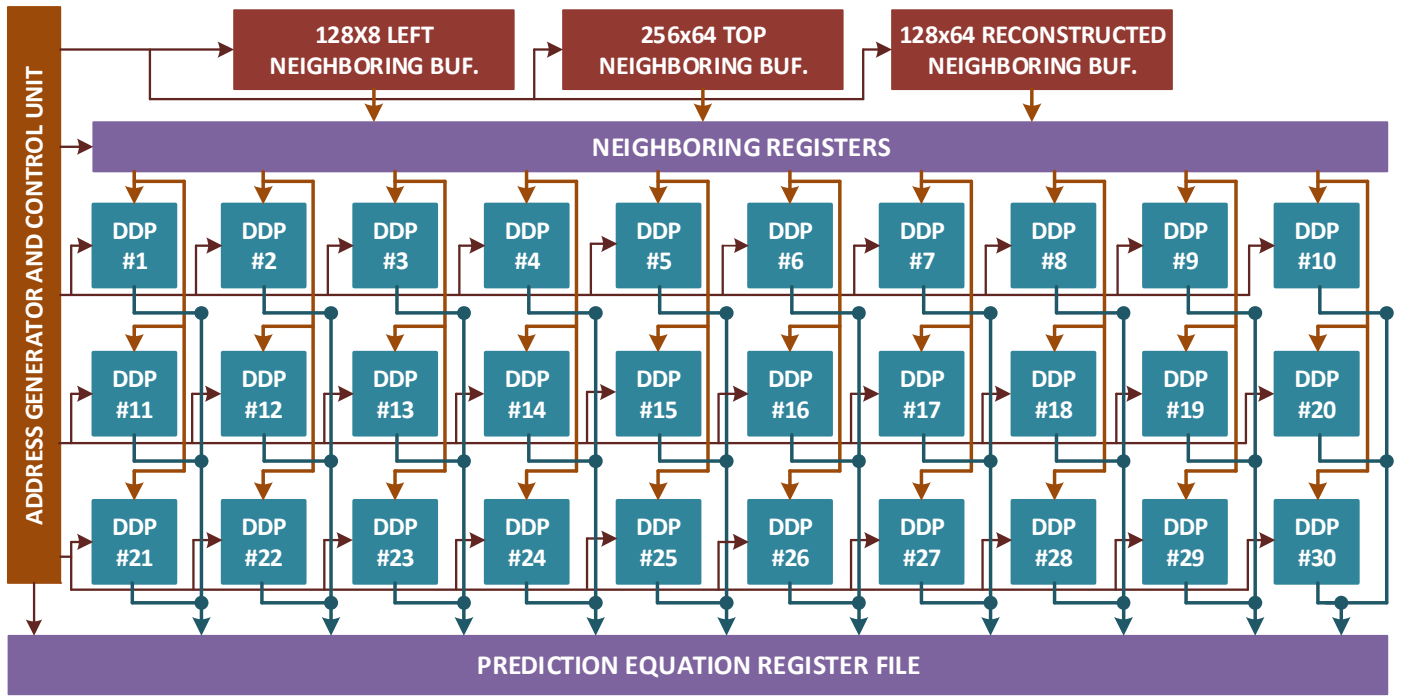


Fig. 3. Proposed VVC intra prediction hardware.

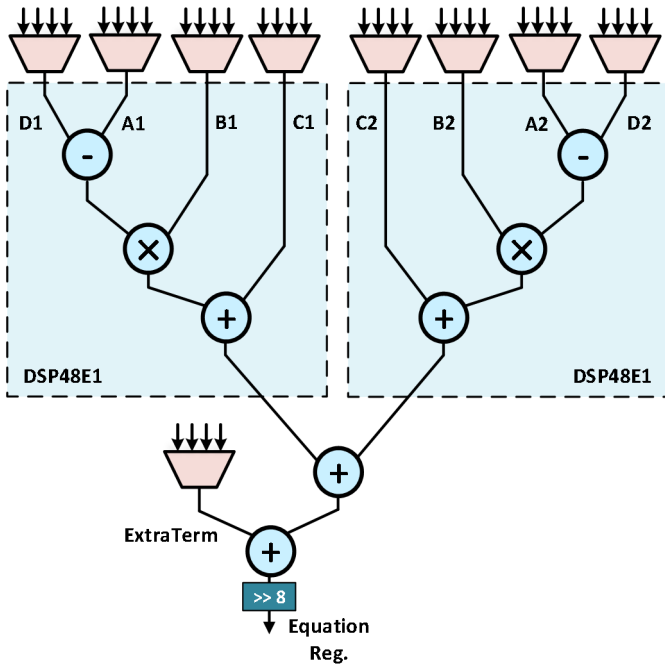


Fig. 4. Proposed reconfigurable DSP datapath (DDP).

Cubic filters are used for 4x4 and 8x8 PU sizes. Total number of cubic filter prediction equations for sixty-four 4x4 PUs and sixteen 8x8 PUs in a 32x32 CU without data reuse is 133120. Gaussian filters are used for 16x16 and 32x32 PU sizes. Total number of gaussian filter prediction equations for four 16x16 PUs and one 32x32 PU in a 32x32 CU without data reuse is 133120. The numbers of cubic filter prediction equations and gaussian filter prediction equations calculated are reduced by 77.85% and 91.13%, respectively with data reuse technique.

The proposed VVC intra prediction hardware is shown in Fig. 3. It implements 65 angular prediction modes for PU sizes from 4x4 to 32x32. It has thirty parallel reconfigurable DSP datapaths (DDP). One DDP, which can be configured to implement any of the 34 cubic and gaussian filters, is shown in Fig. 4.

32x32 coding unit (CU) is divided into 8x8 blocks and the neighboring pixels for the current 8x8 block and four 4x4 blocks within the current 8x8 block are loaded to registers. There are extra registers to store pixels from previous blocks, in case that an equation requires pixels from different 8x8 blocks. Therefore, the number of registers to store is decreased by storing only the neighboring pixels of 8x8 blocks, instead of keeping all neighboring pixels of 32x32 CU.

FPGAs have built-in full-custom DSP blocks which can perform constant multiplications faster and with less energy than adders and shifters. A DSP block can be used to perform different constant multiplications by providing proper constant values to its inputs. Therefore, it is more efficient to implement constant multiplications using DSP blocks instead of using adders and shifters in an FPGA implementation.

Xilinx DSP block architecture is shown in Fig. 5. It has one pre-adder, one multiplier and one arithmetic logic unit (ALU). It also has optional pipeline registers. A DSP block can be configured to implement different operations.

In VVC, each intra angular prediction equation requires four multiplication operations to multiply four pixels with corresponding filter coefficients and three addition operations to add the results of these four multiplications. Therefore, four DSP blocks are necessary for implementing an intra angular prediction equation in its original form as in [11].

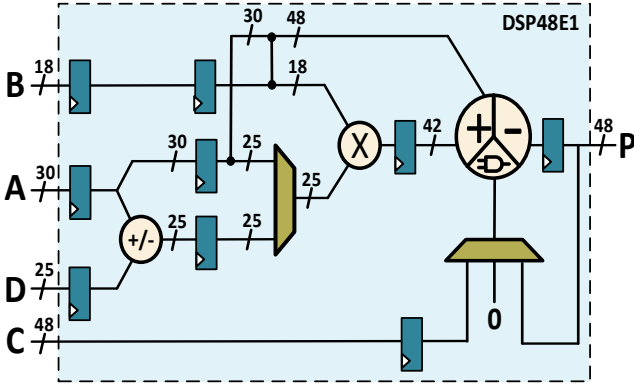


Fig. 5. Xilinx DSP48E1 block.

In the proposed FPGA implementation, intra angular prediction equations are manipulated in such a way that one intra angular prediction equation is implemented using two DSP blocks and two adders. Therefore, each DDP has two DSP blocks and two adders, and it can calculate any 4-tap gaussian and cubic filter used in VVC intra angular prediction in one clock cycle by changing A, B, C and D inputs of DSP blocks.

In the proposed FPGA implementation, DSP blocks are configured to implement equation (3). Each DDP implements equation (4).

$$P = B * (D - A) + C \quad (3)$$

$$P = (B1 * (D1 - A1) + C1) + (B2 * (D2 - A2) + C2) + ExtraTerm \quad (4)$$

Four filter coefficients used in 34 VVC intra angular prediction equations are shown in Table II. The A, B, C, D inputs of two DSP blocks and the extra term necessary for calculating each intra angular prediction equation using a DDP are also shown in Table II. The inputs of DSP blocks are shown in the order they appear in equation (4). Constant numbers are given to B inputs of two DSP blocks. Pixels or shifted pixels are given to D, A and C inputs of DSP blocks. Multiplexers are used to select the proper inputs for implementing each intra angular prediction equation.

For example, the intra angular prediction equation “Filter 1” shown in Table II is implemented using a DDP as shown in equations (5a), (5b), (5c).

$$P = (4 * (2 * p3 - p2) + 0) + (3 * (0 - p1) + (-p4)) + 256 * p2 \quad (5a)$$

$$P = (8 * p3 - 4 * p2 - 3 * p1 - p4 + 256 * p2) \quad (5b)$$

$$P = (-3 * p1 + 252 * p2 + 8 * p3 - p4) \quad (5c)$$

The proposed VVC intra prediction hardware is implemented using Verilog HDL. The Verilog RTL code is synthesized, placed and routed to a Xilinx XC7VX485T FFG1157 FPGA with speed grade 3 using Xilinx Vivado

2017.2. The FPGA implementation is verified with post place and route simulations. The proposed FPGA implementation uses 5766 DFFs, 46382 LUTs, 4 BRAMs and 60 DSP48E1s blocks. It works at 119 MHz. It can process 34 full HD (1920x1080) video frames per second (fps).

The proposed VVC intra prediction hardware is compared with HEVC and VVC intra prediction hardware in the literature in Table III. Since VVC intra prediction algorithm is more complex than HEVC intra prediction algorithm, the proposed VVC intra prediction hardware implementation and the two VVC intra prediction hardware implementations proposed in [11] are slower and have more area than the HEVC intra prediction hardware implementations [12]-[15].

RECON_AS hardware implements VVC intra prediction using adders and shifters [11]. It does not use DSP blocks. RECON_DSP hardware implements VVC intra prediction using DSP blocks [11]. It uses four DSP blocks and one adder for implementing an intra angular prediction equation. The proposed VVC intra prediction hardware is faster than both RECON_AS and RECON_DSP hardware. It uses 50% less DSP blocks than RECON_DSP hardware.

IV. CONCLUSION

In this paper, an efficient FPGA implementation of VVC intra prediction for angular prediction modes of 4x4, 8x8, 16x16 and 32x32 PU sizes is proposed. The proposed reconfigurable datapath uses two DSP blocks and two adders to implement an intra angular prediction equation. The proposed VVC intra prediction hardware can process 34 full HD (1920x1080) frames per second on a Xilinx Virtex 7 FPGA.

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