A SiGe BiCMOS Bypass Low-Noise Amplifier for X-Band Phased Array RADARs

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***Abstract* — This paper presents a bypass low noise amplifier (LNA) for X-band phased array applications in 0.25µm SiGe BiCMOS technology. The trade-off between gain and bypass modes is considered to achieve high gain as well as low noise figure for gain mode while maintaining reasonable insertion loss with high power handling capability in bypass mode. In gain mode, the LNA achieves a measured gain of 17-14.2 dB and a noise figure of 1.75-1.95 dB over the 8-12 GHz band while consuming 27.4mW of DC-power. The measured input-referred 1-dB compression point (IP_{1dB}) is -3.9 dBm at 10 GHz. When operating in bypass mode, the measured insertion loss is 6.5-5.95 dB over the entire X-band with the measured IP_{1dB} of 15.1 dBm at 10 GHz, and it dissipates only 1µW power. Thanks to the bypassing technique, an increase of about 19 dB is achieved for IP_{1dB} in bypass mode compare to the gain mode. The measured return losses are better than 10 dB for both operating modes over whole X-band. The effective chip area excluding the pads is 0.3 mm^2.**

Index Terms — low-noise amplifier, BiCMOS integrated circuits, phased array radar

I. Introduction

A transmit/receive (T/R) module, which enables fast beam scanning and electronics beam control, is a crucial part of the modern phased-array RADAR systems. The modern phased array RADAR systems consist of several thousands of T/R modules; therefore, the properties of a T/R module such as cost, size and integrability should be taken into consideration when building a phased array RADAR system. Recent advances and continued progress in the SiGe BiCMOS technology have made it possible to build low-cost and fully-integrated compact size T/R modules with a competitive, sometimes even better, performance compared to III-V counterparts [1]. In the recent years, X-band T/R module core-chips fabricated in the SiGe BiCMOS technology have been reported [2-3].

In a RADAR system, the dynamic range of the receiver channel is one of the most important parameters. Noise floor level of the receiver channel determines the lower limit of the dynamic range, which directly relates to noise figure and gain performance of the LNA. The upper limit of the dynamic range is predominantly determined by IP_{1dB} of the LNA. It is clearly that LNA is the key component of a T/R module to achieve the high dynamic range at the receiver channel. A direct method to increase IP_{1dB} is to increase bias currents, which results with more power consumption and higher noise figure. Even though the increase in the power consumption of the LNA can be acceptable, the higher noise figure causes higher noise floor and it increases the lower limit of the dynamic range. The way to overcome this trade-off is to bypass the LNA at large input power levels. Up to nowadays, only a few studies have been published that use this unique bypassing technique [4-5].

In this work, we present the design, implementation and measurement results of an X-band high dynamic range bypass LNA using IHP's 0.25µm SiGe BiCMOS process that offers three types of HBTs; high-performance, medium voltage and high voltage. The high - performance transistor has the highest f_t of 110 GHz and maximum oscillation frequency f_{max} of 180 GHz with a collector-emitter junction breakdown-voltage (BV_{CEO}) of 2.3V. The high voltage transistor has the highest breakdown voltage (BV_{CEO}>7V) but exhibits the f_t 25 GHz. The performance of the medium voltage transistor is in the middle with f_t of 45 GHz and BV_{CEO} of 5V. This FEOL process also offers MOS transistors which can be used as RF-switches

II. Circuit Design

The schematic view of the bypass LNA based on a single stage cascode topology together with a series switch at bypass path is shown in Fig. 1. When the V_{BYPASS} is applied and the V_{CC} voltage is set to zero, the switch M1 is "on" and a bypass path between the input and output terminals is formed. When the V_{CC} voltage is applied and the V_{BYPASS} voltage is set to zero, the switch M1 is "off" and the bypass LNA is operating as a conventional low-noise amplifier with a RC feedback because of the R_{off} resistance of the transistor M1 and the series capacitors C_S.

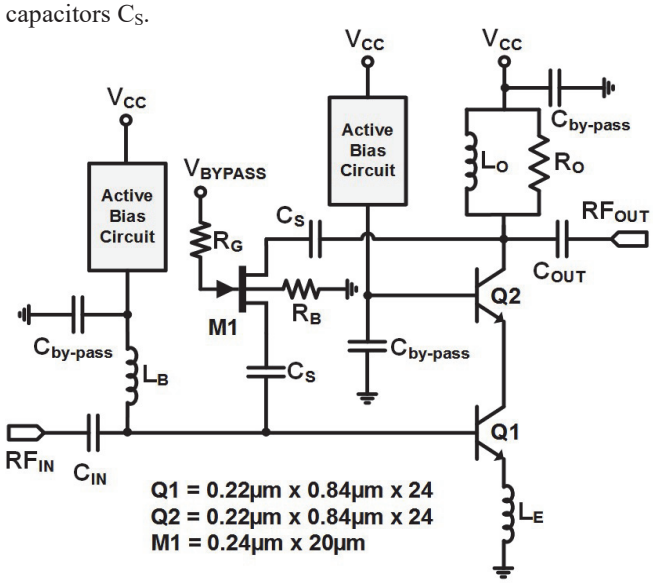

Fig. 1. Circuit schematic of the bypass LNA.

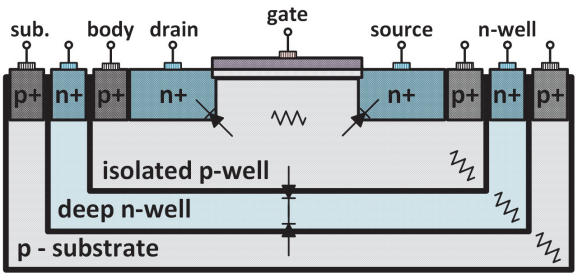

Fig. 2. Cross-sectional view of a typical isolated NMOS transistor.

The bypassing functionality was implemented by a series NMOS switch used between the input and output terminals of the bypass LNA. An isolated body created by a deep n-well was utilized to reduce loss due to the substrate conductivity [6]. Fig. 2 shows the cross-sectional view of a typical triple-well NMOS transistor with an isolated body from the substrate. Besides, the resistive body-floating technique was applied to improve the power-handling capability of the NMOS switch [7]. As could be seen from the Fig. 3, the drain-body and source-body diodes (D_{db} and D_{sb}) will be turned on at high powers, and the power performance of the conventional NMOS will be degraded earlier because of the rapid increase of the current on the diodes D_{db} and D_{sb}. However, for the isolated NMOS (iNMOS) with the body-floating technique, the current on the diodes D_{db} and D_{sb} increases smoothly because of the high-value resistance R_b placed between the body-terminal and the ground. Therefore, the body-floating technique leads to an improvement in the power handling capability as seen from the Fig. 4.

The bypass LNA was designed to obtain a high gain with low noise figure performance in gain mode and keep providing a reasonable insertion loss that can be compensated by large input signals in bypass mode. The significant determining factor of the insertion loss in bypass mode is the resistance of the NMOS in on-state. The use of larger NMOS would enable to obtain lower resistance which provides less insertion loss in bypass mode. However, larger transistor brings larger parasitic capacitance which deteriorates the gain performance of gain-mode. Therefore, the channel width of the switch was chosen as 20μm.

The bipolar cascode topology is used to improve stability and provide higher power gain. Noise figure value (NF_{min}) of HBT is inversely proportional to its f_t. For this reason, the common-emitter transistor Q1 was chosen as the high-performance transistor. The common-base transistor Q2 was also chosen as the high-performance transistor to keep its noise contribution as low as possible. The optimum base-emitter voltage of Q1 was determined to achieve both high-gain and low-noise figure. The input noise and power matchings were simultaneously performed by scaling the transistor Q1 and using the inductors L_E, L_B and the capacitors C_{IN}, C_S. The output of the bypass LNA was matched to 50Ω by L_O, R_O, C_{OUT}, and C_S. In order to improve the power linearity of the LNA in gain mode, the base-emitter bias voltage of the transistor Q1 was fed through the inductor L_B instead of a high value resistance to avoid significant amount of voltage drop for large input power levels.

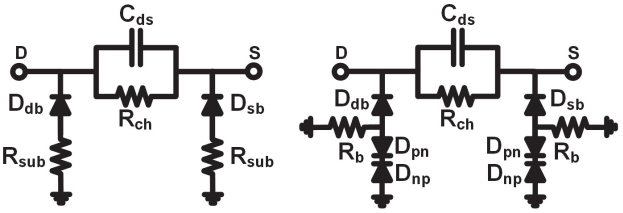

Fig. 3. Simplified equivalent circuit models of the switch to investigate the power linearity: (a) NMOS (b) iNMOS with body-floating.

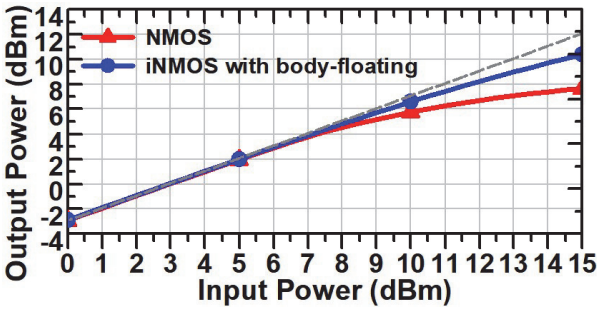

Fig. 4. Simulated on-state power linearity of the NMOS and iNMOS with body floating.

III. Simulation and Measurements Results

S-parameters were measured by the Rohde&Schwarz ZVL network analyzer calibrated by the two-port short-open-load-thru (SOLT) on-chip calibration technique at -20 dBm RF port-power. The noise figure of the LNA was measured by using the Agilent PSA-E4448A spectrum analyzer utilized with Agilent 346A noise source and Agilent 87405C pre-amplifier. When measuring IP_{1dB}, 10 GHz sinusoidal input signal was applied at different power levels by Agilent PSG-E8257D signal generator, and the output power was measured by Agilent E4417A power meter and E9325A power sensor. The die photo of the bypass LNA is shown in Fig. 5. The effective chip area excluding the pads is 0.3 mm^2.

A. Gain Mode

In gain mode, the LNA draws 9.8 mA from a 2.8V supply and the quiescent power consumption is 27.4 mW. Simulated and measured gain and isolation performances are presented in Fig. 6. The measured peak gain of the bypass LNA is 17 dB at 8.4 GHz and drops to 14.2 dB at 12 GHz. Fig. 7 demonstrates the simulated and measured return losses. The measured return losses are better than 10 dB from 8 to 12 GHz. Fig. 8 shows the simulated and measured noise figure (NF) of the LNA. The measured noise figure is lower than 1.95 dB across X-band, and its minimum value is 1.75 dB at 8.5 GHz. Fig. 9 shows the measured IP_{1dB} of -3.9 dBm at 10 GHz.

B. Bypass mode

In bypass mode, the power consumption of the bypass LNA is just 1 μW. Simulated and measured s-parameter results are shown in Fig. 10. The measured return losses are better than 10 dB from 7.5 to 12.5 GHz. The measured insertion loss is less

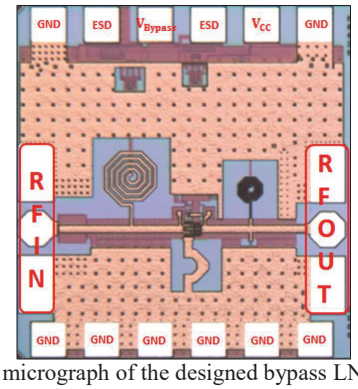

Fig. 5. Chip micrograph of the designed bypass LNA.

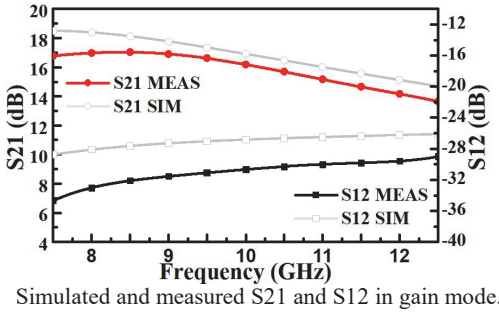

Fig. 6. Simulated and measured S21 and S12 in gain mode.

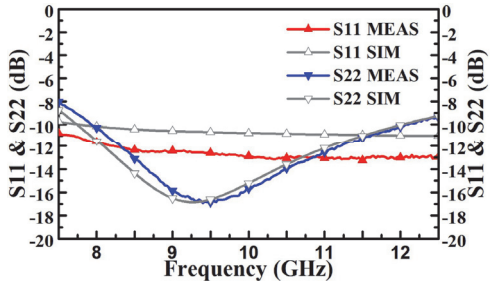

Fig. 7. Simulated and measured S11 and S22 in gain mode.

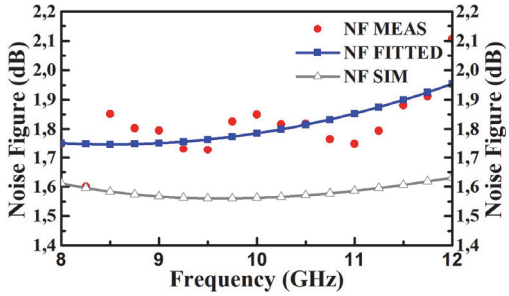

Fig. 8. Simulated, measured, and fitted noise figure in gain mode.

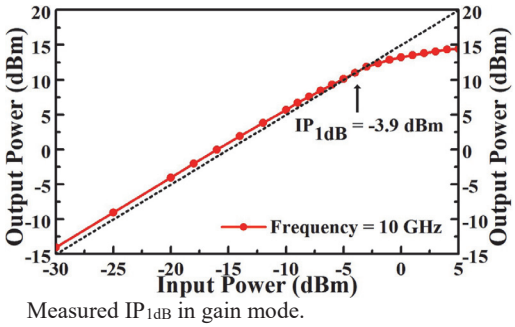

Fig. 9. Measured IP_{1dB} in gain mode.

than 6.5 dB over the whole X-band, and the minimum insertion loss is about 5.95 dB at 10.4 GHz. Fig. 11 shows that the measured IP_{1dB} of the bypass LNA is 15.1 dBm in bypass mode. There is an increase of about 19 dB for IP_{1dB} compare to the gain mode.

IV. Conclusion

Design, implementation and measurement results of a high dynamic range SiGe BiCMOS bypass LNA for X-band phased-array RADAR applications has been presented. The bypassing technique has been successfully employed to overcome the trade-off between lower and upper limits of the dynamic range. This work highlights the potential of the bypassing technique for X-band phased array radar applications in SiGe HBT BiCMOS technologies.

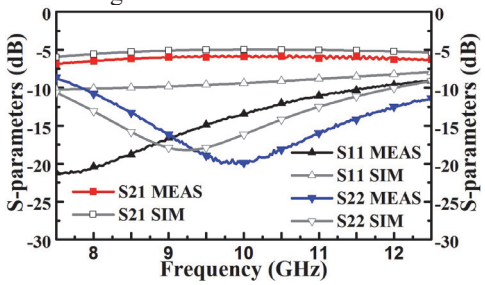

Fig. 10. Simulated and measured s-parameters in bypass mode.

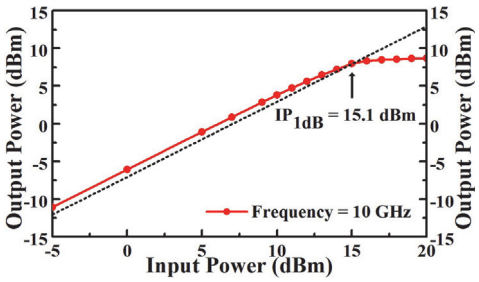

Fig. 11. Measured IP_{1dB} in bypass mode.

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